



Intel® Agilex™ Power Management User Guide



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1. Intel® Agilex™ Power Management Overview

The Intel® Agilex™ device family offers SmartVID standard power devices in all speed grades. Fixed-voltage devices are also available, but only in –4 speed grade. All SmartVID standard power devices must be driven by the Power Management BUS (PMBus*)-compliant voltage regulator, operating either in the PMBus master or PMBus slave mode.

Intel Agilex devices offer the following power optimization features:

- Digital signal processing (DSP) and M20K power gating
- Clock gating

This user guide describes the power-optimizing features of the Intel Agilex device family, and the power-up and power-down sequencing requirements for the Intel Agilex devices.

1.1. Power System Design Phases

Power system design is done in the following logical phases.

1.1.1. Choosing a Power Tree

A power tree topology is chosen based on the requirements of your device.

The requirements of the power supply may not yet be known, but you can access the supply voltage and connection requirements from the *Intel Agilex Device Family Pin Connection Guidelines* and the power tree selector guides in the *Intel Enpirion® Power Resource Center*. Any required power supply sequencing and SmartVID usage will impact the power tree topology.

Related Information

- [Intel Agilex Device Family Pin Connection Guidelines](#)
Provides more information about the supply voltage and connection guidelines of each pin.
- [Intel Enpirion Power Solutions](#)

1.1.2. Power Estimation

The amount of electrical power required by the various device power supplies is estimated using the Intel FPGA Power and Thermal Calculator tool and the Power Analyzer tool.

As the design evolves to the final configuration, the quality and type of information available improve and the estimation becomes more accurate.



1.1.3. Power Optimization

The device configuration can be optimized to reduce power.

This step involves the Intel Quartus® Prime software power optimization wizard, the SmartVID feature (available in all Intel Agilex devices except for –4F speed grade), system cooling decisions, and/or dynamic workload management strategies. This phase may occur several times during the evolution of the system and device design.

1.1.4. Power Generation

Voltage regulator modules (VRMs) are selected based on the power tree and electrical power estimates. VRM selection is critical to producing high-quality power systems with the minimum number and cost of bypass elements. Intel Enpirion VRMs are featured due to their high quality and fast load transient response.

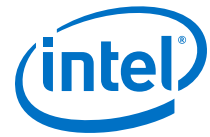
1.2. Power Supplies

For more information about the supported power supplies and the nominal voltages, refer to the *Intel Agilex Device Data Sheet*.

Related Information

[Intel Agilex Device Data Sheet](#)

Provides more information about the supported power supplies and the nominal voltages.



2. Intel Agilex Power Basics

2.1. Power Consumption

The total power consumption of an Intel Agilex device consists of the following components:

- Static power—the power that the configured device consumes when powered up but no user clocks are operating, excluding DC bias power of analog blocks, such as I/O and transceiver analog circuitry.
- Dynamic power—the additional power consumption of the device due to signal activity or toggling. Dynamic power is dependent on the operating frequency of your design, applied voltage, and load capacitance, which depends on design connectivity.
- Standby power—the component of active power that is independent of signal activity or toggling. Standby power includes, but is not limited to, I/O and transceiver DC bias power.

Intel Agilex devices minimize static and dynamic power using advanced process optimizations. These optimizations allow Intel Agilex designs to meet specific performance requirements with the lowest possible power.

2.2. Power Estimation Basics

The Intel power analysis features, including the Intel FPGA Power and Thermal Calculator tool and the Intel Quartus Prime software Power Analyzer, give you the ability to estimate power consumption from early design concept through design implementation, as shown in the following figure.

As you provide more details about your design characteristics, estimation accuracy is improved. Intel recommends that you switch from the Intel FPGA Power and Thermal Calculator to the Power Analyzer in the Intel Quartus Prime software once your design is available. The Power Analyzer produces more accurate results because it has more detailed information about your design, including routing and configuration information about all the resources in your design.

The accuracy of the power model is determined on a per-power-rail basis for both the Power Analyzer and the Intel FPGA Power and Thermal Calculator. For most designs, the Power Analyzer and the Intel FPGA Power and Thermal Calculator have the following accuracies, with final power models:

- Power Analyzer—within 10% of silicon for the majority of power rails and the highest power rails, assuming accurate inputs and toggle rates.
- Intel FPGA Power and Thermal Calculator—within 15% of silicon for the majority of power rails and the highest power rails, assuming accurate inputs and toggle rates. Recommended margins are shown in the **Report** tab, only after device power model status is final.

Figure 1. Power Analysis from Design Concept Through Design Implementation

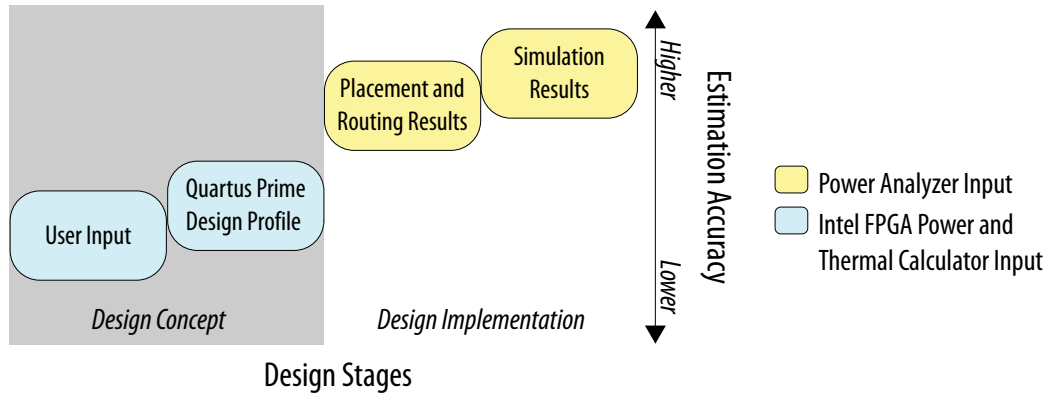


Table 1. Comparison of Intel FPGA Power and Thermal Calculator and Intel Quartus Prime Power Analyzer Capabilities

Characteristic	Intel FPGA Power and Thermal Calculator	Intel Quartus Prime Power Analyzer
When to use	Any time <i>Note:</i> For post-fit power analysis, you get better results with the Intel Quartus Prime Power Analyzer.	Post-fit
Software requirements	The Intel Quartus Prime software	The Intel Quartus Prime software
Accuracy	Medium	Medium to very high
Data inputs	<ul style="list-style-type: none"> Resource usage estimates Clock requirements Environmental conditions Toggle rates 	<ul style="list-style-type: none"> Post-fit design Clock requirements Signal activity defaults Environmental conditions Register transfer level (RTL) simulation results (optional) Post-fit simulation results (optional) Signal activities per node or entity (optional)
Data outputs	<ul style="list-style-type: none"> Total thermal power dissipation Thermal static power Thermal dynamic power Off-chip power dissipation Current drawn from voltage supplies 	<ul style="list-style-type: none"> Total thermal power dissipation Thermal static power Thermal dynamic power Thermal I/O power Thermal power by design hierarchy Thermal power by block type
continued...		



Characteristic	Intel FPGA Power and Thermal Calculator	Intel Quartus Prime Power Analyzer
		<ul style="list-style-type: none">• Thermal power dissipation by clock domain• Off-chip (non-thermal) power dissipation• Current drawn from voltage supplies

2.3. Intel FPGA Power and Thermal Calculator

The Intel FPGA Power and Thermal Calculator results for Intel Agilex devices are based on preliminary simulated data.

Any results obtained while using this estimator are preliminary. The Intel FPGA Power and Thermal Calculator for Intel Agilex devices provides a current and power estimate based on various conditions such as room temperature and nominal voltage.

The Intel FPGA Power and Thermal Calculator calculations are estimates only and shall not be construed as a specification or a guarantee of any kind. The actual currents must be verified during device operation, as this measurement is sensitive to the design implemented in the device and the environmental operating conditions.

2.4. Power Analyzer

The Intel Quartus Prime Power Analyzer allows you to estimate power consumption for a post-fit design.

To estimate power consumption before you compile the design, use the Intel FPGA Power and Thermal Calculator.

Related Information

[Intel Quartus Prime Pro Edition User Guide: Power Analysis and Optimization](#)

3. Intel Agilex Power and I/O State Sequencing

3.1. Overview

The Intel Agilex devices require a specific power-up sequence.

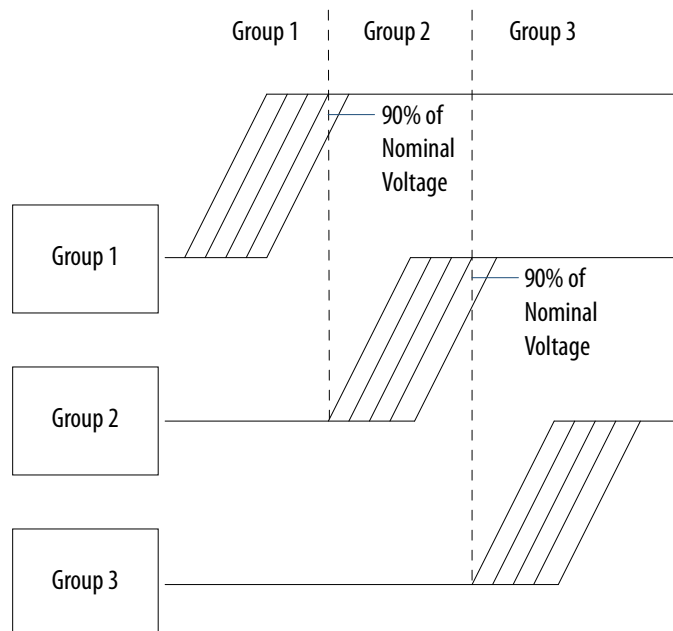
This section describes several power management options and discusses proper I/O management during device power up and power down. Design your power supply solution to properly control the complete power sequence. The requirements in this section must be followed to prevent unpredictable current draw to the FPGA device, which can potentially impact the I/O functionality.

3.2. Power-Up Sequence Requirements

The power rails in the Intel Agilex devices are divided into three groups.

The following figure shows the voltage groups of the Intel Agilex devices and their required power-up sequence.

Figure 2. Power-Up Sequence for the Intel Agilex Devices



Note: V_{CCBAT} is not in any of the groups below. V_{CCBAT} does not have any sequence requirements. V_{CCBAT} holds the content of the security keys.

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*Other names and brands may be claimed as the property of others.

**Table 2. Voltage Rails Group**

Power Group	FPGA Core and Hard Processor System (HPS)	Additional Voltage Rails			
		E-Tile	P-Tile	F-Tile	R-Tile
Group 1	V _{CC} V _{CCP} V _{CCH} V _{CCL_SDM} V _{CCH_SDM} V _{CCPLLDIG_SDM} V _{CCL_HPS} V _{CCPLLDIG_HPS}	V _{CCRT_GXE} V _{CC_HSSI_GXE} V _{CCRTPLL_GXE}	V _{CC_HSSI_GXP} V _{CCRT_GXP} V _{CCFUSE_GXP}	V _{CC_HSSI_GXF} V _{CCFUSECORE_GXF} V _{CCERT_UX_GXF} V _{CCERT1_BRK_GXF} V _{CCERT2_BRK_GXF}	V _{CC_HSSI_GXR} V _{CCPLL_REF_GXR} V _{CCERT_GXR}
Group 2	V _{CCPT} V _{CCPLL_SDM} V _{CCADC} V _{CCPLL_HPS}	V _{CCH_GXE} V _{CCCLK_GXE}	V _{CCH_GXP} V _{CCCLK_GXP}	V _{CCFUSEWR_GXF} V _{CCCLK_GXF} V _{CCH_UX_GXF} V _{CCERT_BRK_GXF}	V _{CCED_GXR} V _{CCCLK_GXR} V _{CCH_FUSE_GXR} V _{CCERT_GXR}
Group 3	V _{CCA_PLL} V _{CCR_CORE} V _{CCIO_PIO_SDM} V _{CCBAT} V _{CCIO_PIO} V _{CCFUSEWR_SDM} V _{CCIO_SDM} V _{CCIO_HPS}	—	—	—	V _{CCH_FUSE_GXR}

All power rails in Group 1 must ramp up (in any order) to a minimum of 90% of their respective nominal voltage before the power rails from Group 2 can start ramping up. The power rails within Group 2 can ramp up in any order after the last power rail in Group 1 ramps to the minimum threshold of 90% of its nominal voltage. All power rails in Group 2 must ramp to a minimum threshold of 90% of their nominal value before the Group 3 power rails can start ramping up. The power rails within Group 3 can ramp up in any order after the last power rail in Group 2 ramps up to a minimum threshold of 90% of their full value. For more information, refer to the *Intel Agilex Device Family Pin Connection Guidelines*.

All power rails must ramp up monotonically. The power-up sequence must meet the POR delay time. For the POR specifications of the Intel Agilex devices, refer to the *POR Specifications* section in the *Intel Agilex Device Data Sheet*.

For configuration via protocol (CvP), the total t_{RAMP} must be less than 10 ms from the first power supply ramp-up to the last power supply ramp-up. For the t_{RAMP} specifications, refer to the *Recommended Operating Conditions* section in the *Intel Agilex Device Data Sheet*.

For Intel Agilex devices, there is no power-down sequence requirement. Intel recommends that you reverse the power-up sequence when you power down your device.

Related Information

- [Intel Agilex Device Family Pin Connection Guidelines](#)
Provides more information about the power supply sharing guidelines.
- [Intel Agilex Device Data Sheet](#)
Provides more information about the t_{RAMP} and POR specifications.

3.2.1. Guidelines for I/O Pins in GPIO, HPS, and SDM Banks During Power Sequencing

Intel Agilex devices do not support hot-socketing and require a specific power-up sequence. Design your power supply solution to properly control the complete power sequence.

Adhere to the following guidelines to prevent unnecessary current draw on the I/O pins located in the GPIO, HPS, and SDM banks. These guidelines are applicable for unpowered, power up to POR, POR delay, POR delay to configuration, configuration, initialization, user mode, and power down device states.

- The I/O pins including the HPS and SDM shared I/O in the GPIO banks can be in tri-state, connected to ground or connected to `VCCIO_PIO`. The voltage level for these pins must not exceed the DC input voltage (V_I) value.
- The I/O pins in the HPS banks can be in tri-state, connected to ground or connected to `VCCIO_HPS`. The voltage level for these pins must not exceed 1.89 V.
- The I/O pins in the SDM banks can be in tri-state, connected to ground or connected to `VCCIO_SDM`. The voltage level for these pins must not exceed 1.89 V.
- These pins can tolerate a maximum of 10 mA per pin and a total of 100 mA per I/O bank for all conditions.

3.3. Power-On Reset

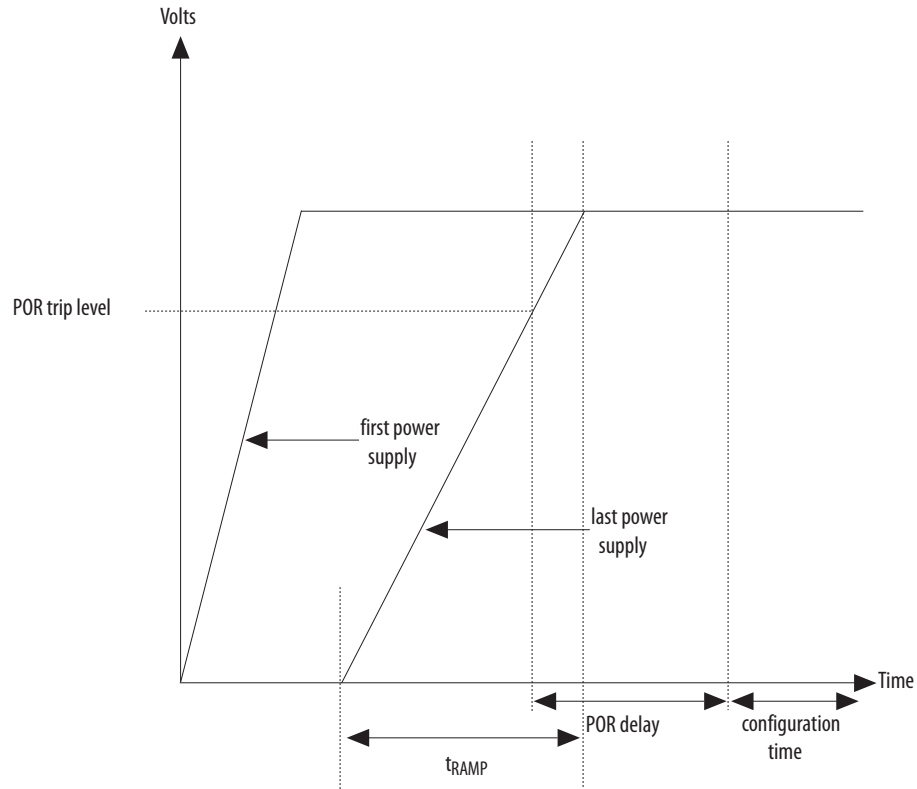
The power-on reset (POR) circuitry keeps the Intel Agilex device in the reset state until the power supply outputs are within the recommended operating range.

A POR event occurs when you power up the Intel Agilex device until all power supplies monitored by the POR circuitry reach the recommended operating range within the maximum power supply ramp time, t_{RAMP} . If t_{RAMP} is not met, the Intel Agilex device I/O pins and programming registers remain tri-stated, which may cause device configuration to fail.



Figure 3. Relationship Between t_{RAMP} and POR Delay

The boot ROM initialization sequence is part of the POR delay. For t_{RAMP} and POR delay specifications, refer to the *Intel Agilex Device Data Sheet*.



The Intel Agilex POR circuitry uses individual detection circuitry to monitor each of the configuration-related power supplies independently. The POR circuitry is gated by the outputs of all the individual detectors.

POR delay is the time from when the POR trips out to the final reset signal. For POR trip level, you can use the minimum value of the last power supply as a reference.

The Intel Agilex device is held in the POR state until all power supplies have passed their trigger point. After power supplies have passed the trigger point, the Secure Device Manager (SDM) will wait for a configurable delay time and then start device configuration.

Related Information

[Intel Agilex Device Data Sheet](#)

Provides more information about the t_{RAMP} and POR specifications.

3.3.1. Power Supplies Monitored by the POR Circuitry

The following power supplies are monitored by the Intel Agilex POR circuitry:

- $V_{\text{CCL_SDM}}$
- V_{CCPT}
- $V_{\text{CCIO_SDM}}$



- V_{CCADC}
- V_{CCBAT}
- V_{CC}
- V_{CCH_SDM}
- V_{CCL_HPS}
- $V_{CCIO_PIO_SDM}$
- V_{CCR_CORE}

4. Intel Agilex Sensor Monitoring System

Intel Agilex devices provide you with on-chip voltage and temperature sensors. These sensors may be used to monitor external voltages and on-chip operation conditions such as the internal power rail and on-chip junction temperature.

The Intel Agilex sensor monitoring system stores sampled data in the secure device manager (SDM). You can read the voltage and temperature values in the SDM by using the Mailbox Client Intel FPGA IP or the Mailbox Avalon® ST Client Intel FPGA IP.

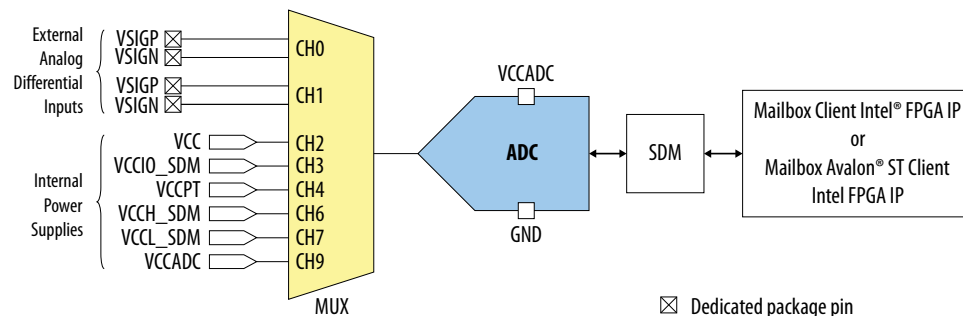
Related Information

- [Operation Commands, Mailbox Client Intel FPGA IP User Guide](#)
Provides information about the GET_VOLTAGE and GET_TEMPERATURE commands of the Mailbox Client IP.
- [Mailbox Avalon ST Client Intel FPGA IP User Guide](#)
Provides information about reading the voltage and temperature values using the Mailbox Avalon ST Client IP.

4.1. Voltage Monitoring System

The Intel Agilex voltage monitoring system uses a built-in 7-bit analog to digital converter (ADC). The ADC can sample up to one kilo samples per second (KSPS).

Figure 4. Intel Agilex Voltage Sensor



The voltage sensor has the following capabilities:

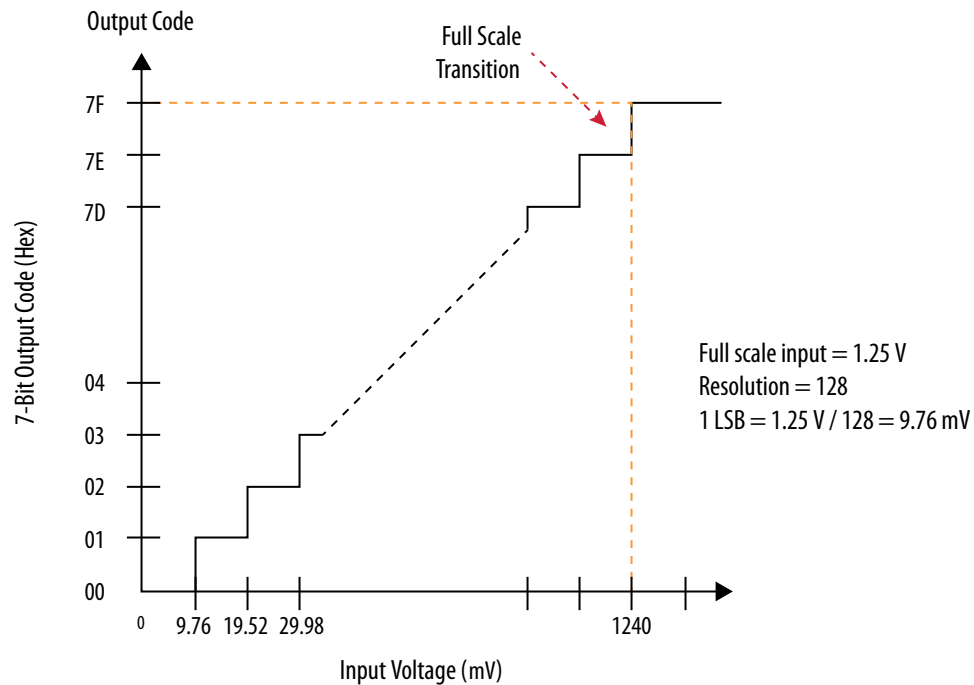
- Monitor external voltages up to 1.25 V through two pairs of differential input pins
- Monitor internal power supplies

4.1.1. Voltage Sensor Transfer Function

The Intel Agilex voltage sensor supports the ADC's unipolar operation mode.

Figure 5. Intel Agilex ADC 7-Bit Unipolar Transfer Function

The analog input scale has full scale code from 00h to 7Fh. The measurement can only display up to *full scale* – 1 LSB



4.2. Temperature Monitoring System

The Intel Agilex temperature monitoring system allows you to measure the on-chip temperature (T_{JUNCTION}) using a local temperature sensor or a remote temperature sensing diode (TSD).

Table 3. Overview of the Local and Remote Temperature Sensors

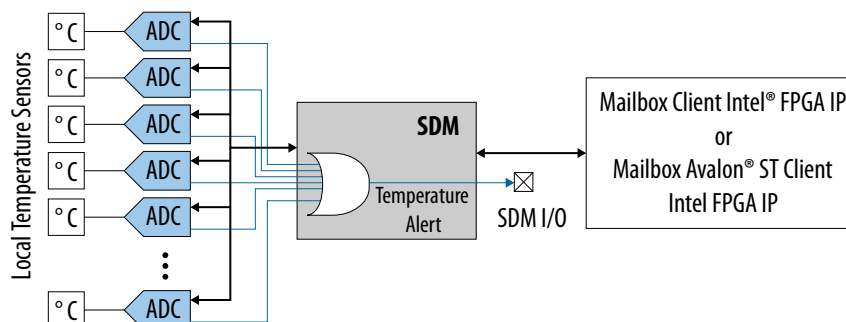
Feature	Local Temperature Sensor	Remote TSD
Temperature sensing	Uses the built-in ADC to sample the on-chip temperature	Interfaces the TSD with an external temperature sensing chip
Readout access	From the SDM mailbox through the Mailbox Client or Mailbox Avalon ST Client IPs	From the external temperature sensing chip
Operation capability	While the Intel Agilex device is in user mode	While the Intel Agilex device is powered on or off

4.2.1. Local Temperature Sensor

The Intel Agilex local temperature sensor uses a built-in 11-bit ADC and provides temperature readouts through the SDM mailbox.

Figure 6. Intel Agilex Local Temperature Sensor

This figure is a block diagram of the local temperature sensors. For the physical locations of the sensors, refer to the related information.



The Intel Agilex provides up to nine local temperature sensor channels for monitoring on-chip temperature:

- Five local temperature sensors in the core fabric allows you to monitor the local temperature of the core fabric location around each sensor.
- Up to four local temperature sensors, one in each transceiver tile, allows you to monitor the tile's temperature. The number of transceiver tiles varies among Intel Agilex device and package options.

Catastrophic Trip Signal

The catastrophic trip signal, `nCATTRIP`, is an optional signal that you can assign to any unused `SDM_IO` pin. If enabled, the `nCATTRIP` signal asserts when the core temperature is greater than 125° C. When the signal is asserted, you must immediately power down the FPGA to avoid permanent damage to the device.

Related Information

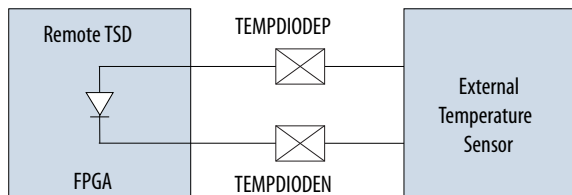
- [Temperature Sensor Channels and Locations](#) on page 16
- [SDM Pin Mapping, Intel Agilex Configuration User Guide](#)
Provides more details about enabling and assigning the `nCATTRIP` signal to an `SDM_IO` pin.

4.2.2. Remote Temperature Sensing Diode

The Intel Agilex remote TSD interface allows you to monitor the temperature of the core fabric and transceiver tiles using an external temperature sensor.

Figure 7. External Temperature Sensor Connection to the Intel Agilex Remote TSD

The remote TSD requires a two-pins connection.



- In the Intel Agilex device pin-out files, the remote TSD pins are marked as TEMPDIODEP and TEMPDIODEN.
- For the remote TSD characteristics, refer to the relevant section in the Intel Agilex device datasheet.

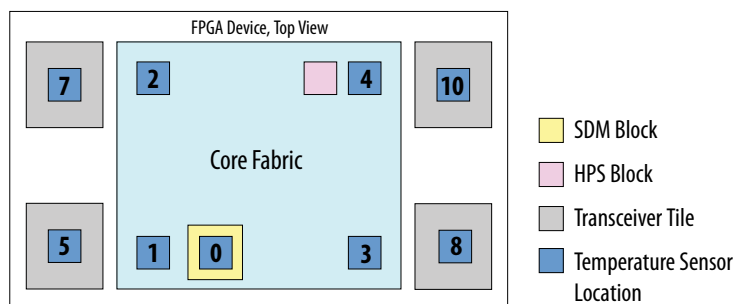
Related Information

Temperature Sensor Channels and Locations on page 16

4.2.3. Temperature Sensor Channels and Locations

The Intel Agilex local temperature sensors and remote TSDs are located in the core fabric and transceiver tiles. There are several local temperature sensors within the core fabric or individual transceiver tile die, depending on the transceiver type.

Figure 8. Locations of Intel Agilex Local Temperature Sensors and Remote TSDs



Note: The availability of the transceiver tiles varies among Intel Agilex devices. The HPS block is only available in Intel Agilex SoC FPGAs.

- To monitor the HPS temperature, use the temperature sensors in location 4.
- To monitor the SDM temperature, use the temperature sensors in location 0.

Table 4. Local Temperature Sensor Locations and Equivalent Remote TSD Pin Names

The temperature sensor locations are as shown in the preceding figure. Not all locations have remote TSD pins, even if the local temperature sensor location is available for the supported product lines.

Local Temperature Sensor Location	Availability in Product Line		Equivalent Remote TSD Pin Name
	<ul style="list-style-type: none"> • AGF 004 • AGF 006 • AGF 008 • AGF 012 • AGF 014 	<ul style="list-style-type: none"> • AGF 022 • AGF 027 • AGI 022 • AGI 027 	
0	Yes	Yes	TEMPDIODE0Ap / TEMPDIODE0An
1	Yes	Yes	—
2	Yes	Yes	TEMPDIODE0Cp / TEMPDIODE0Cn
3	Yes	Yes	—
4	Yes	Yes	—
5	Yes	Yes	TEMPDIODE1p / TEMPDIODE1n
continued...			



Local Temperature Sensor Location	Availability in Product Line		Equivalent Remote TSD Pin Name
	<ul style="list-style-type: none"> • AGF 004 • AGF 006 • AGF 008 • AGF 012 • AGF 014 	<ul style="list-style-type: none"> • AGF 022 • AGF 027 • AGI 022 • AGI 027 	
7	—	Yes	TEMPDIODE3p / TEMPDIODE3n
8	Yes	Yes	TEMPDIODE4p / TEMPDIODE4n
10	—	Yes	TEMPDIODE6p / TEMPDIODE6n

Related Information

- [Operation Commands, Mailbox Client Intel FPGA IP User Guide](#)
Provides information about the GET_VOLTAGE and GET_TEMPERATURE commands of the Mailbox Client IP.
- [Mailbox Avalon ST Client Intel FPGA IP User Guide](#)
Provides information about reading the voltage and temperature values using the Mailbox Avalon ST Client IP.

4.2.4. Retrieving Local Temperature Sensor Reading

To retrieve the temperature readings, provide the location and channel masks to the Mailbox Avalon ST Client Intel FPGA IP.

Table 5. Temperature Sensor Locations and Channels Bitmask

Reserved	Location	Channel
Bits [31..28]	Bits [27..16]	Bits [15..0]

Bits [27..16] represent the local temperature sensor location while bits [15..0] represent the channels.

- For an E-tile location, with up to four local temperature sensors in the same tile, channel bitmask [3..0] indicates which temperature sensor to read.
- For the core fabric or a P-tile location, which has only a single temperature sensor, the channel bitmask defaults to 0.

For example, to read one of the channels in an E-tile marked as location 5:

- Set 1 to bit 21.
- Set 1 to the channel mask in bit [0..3].

If you want to read the temperature from all temperature sensors in location 5, set 1 to all channel masks.

If the location has only one local temperature sensor, specify only the location mask.

Note: Intel recommends that you read all temperature channels in a tile location and use the highest temperature readout for the tile as the critical point.

Related Information

- [Operation Commands, Mailbox Client Intel FPGA IP User Guide](#)
Provides information about the GET_VOLTAGE and GET_TEMPERATURE commands of the Mailbox Client IP.
- [Mailbox Avalon ST Client Intel FPGA IP User Guide](#)
Provides information about reading the voltage and temperature values using the Mailbox Avalon ST Client IP.

4.3. Intel Agilex Sensors Design Considerations

To ensure the success of your designs, follow the recommended design guidelines. These guidelines apply to all variants of the device family unless noted otherwise.

4.3.1. Intel Agilex Voltage Monitor Design Guidelines

- Connect the power pins and VSIG pins according to the requirements in the Intel Agilex pin connection guidelines.
- If you use the voltage sensor in single-ended mode, tie the VSIGN pin to the GND pin.
- To prevent damage, do not drive VSIGP and VSIGN pins until the VCCADC power rail has reached 1.62 V.

4.3.2. Intel Agilex Temperature Monitor Design Guidelines

You can measure the on-chip temperature of the core fabric or transceiver tiles through the remote TSDs while the device is powered on or powered off. However, the local temperature sensors are available only after the device is powered up and configured.

- Connect the remote TSD pins to external temperature sensing devices to monitor the on-chip temperature.
- To interface with the remote TSD, use temperature sensing chips with features that allow you to perform calibration and measurement compensation to improve accuracy, such as:
 - Configurable ideality factor
 - Offset adjustment with or without Beta compensation
- Keep the resistance of both board traces to the remote TSD p and n pins to less than 0.2 Ω .
- Route both traces in equal lengths and shield them.
- Intel recommends a 10-mils width and space for both traces.
- Route both traces through the most minimum number of vias and crossunders possible to minimize the thermocouple effects.
- Ensure that the number of vias for both traces are the same.



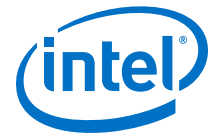
- To avoid coupling, insert a GND plane between the remote TSD pins traces and high-frequency toggling signals, such as clocks and I/O signals.
- To filter high-frequency noise, place an external capacitor between the traces close to the external sensors.
- If you use only the local temperature sensors, you can leave the remote TSD p and n pins unconnected.

For details about device specifications and connection guidelines, refer to the external temperature sensor manufacturer's documentation.

4.3.3. Intel Agilex E-Tile Transceiver Local Temperature Sensor Design Guidelines

The E-tile transceiver tile has four built-in local temperature sensors, spread across the transceiver die. When you query the sensors, the readings from the temperature sensors may vary slightly from each other because of the different activities run in each sensor location of the E-tile transceiver channel.

- For temperature reading through the SDM mailbox, you can query all local temperature sensor channels and remote TSDs.
- Intel recommends that you read all temperature channels in a tile location and use the highest temperature readout for the tile as the critical point.



5. Intel Agilex Power Optimization Techniques and Features

Intel Agilex devices leverage on advanced 10-nm process technology, an enhanced core architecture, and various optimizations to reduce total power consumption. The power optimization techniques and features are listed below:

- SmartVID Standard Power Devices
 - Temperature Compensation
- DSP and M20K Power Gating
- Clock Gating
- Power Sense Line

5.1. SmartVID Standard Power Devices

The SmartVID feature compensates for process variation by narrowing the process distribution using voltage adaptation.

This feature is supported in all Intel Agilex devices with the -V and -E power options only. For the -V and -E power option devices, you must connect the `PWRMGT_SCL` and `PWRMGT_SDA` pins in both the Power Management BUS (PMBus) master and PMBus slave modes. An additional `PWRMGT_ALERT` pin is required when you configure the Intel Agilex device in the PMBus slave mode. All connections required must be set up on the circuit board and in the Intel Quartus Prime software.

For more information about how to connect these pins on the circuit board, refer to the *Intel Agilex Device Family Pin Connection Guidelines*.

For instructions on how to set up the connections in the Intel Quartus Prime software, refer to the [Specifying Power Management and VID Parameters and Options](#) on page 29.

Note:

Intel Agilex standard power devices (-1V, -2V, -3V, and -3E power grades) are SmartVID devices. The core voltage supplies (V_{CC} and V_{CCP}) for each SmartVID device must be driven by a PMBus-compliant voltage regulator dedicated to the Intel Agilex -V device that is connected to that Intel Agilex device via PMBus. For Intel Agilex standard power devices, use of a PMBus-compliant voltage regulator for each device is mandatory. Intel Agilex devices will not configure or function correctly if the core voltage is driven by a non-PMBus compliant regulator with a fixed output voltage.

Intel programs the optimum voltage level required by each individual Intel Agilex device into a fuse block during device manufacturing. The Secure Device Manager (SDM) Power Manager reads these values and can communicate them to an external power regulator or a system power controller through the PMBus interface.



The SmartVID feature allows a power regulator to provide the Intel Agilex device with V_{CC} and V_{CCP} voltage levels that maintain the performance of the specific device speed grade. When the SmartVID feature is used:

1. Intel Agilex devices are powered up at 0.80V regardless of speed grade for both V_{CC} and V_{CCP} .
2. After the SmartVID value in the Intel Agilex device is determined and propagated to the external voltage regulator, both the V_{CC} and V_{CCP} voltages are regulated based on the SmartVID value.

Related Information

- [Intel Agilex Device Family Pin Connection Guidelines](#)
Provides more information about the connection guidelines of each pin.
- [Specifying Power Management and VID Parameters and Options](#) on page 29
Provides instructions on how to set up the connection in the Intel Quartus Prime software.

5.1.1. SmartVID Feature Implementation in Intel Agilex Devices

Devices supporting the SmartVID feature have a SmartVID value programmed into a fuse block during device manufacturing. The SmartVID value represents a voltage level in the range of 0.6 V to 1.0 V. Each device has its own specific SmartVID value.

The SmartVID value is sent to the external regulator or system power controller through the PMBus interface. Upon receiving the SmartVID value, an adjustable regulator tunes the V_{CC} and V_{CCP} voltage levels to the voltage specified by the SmartVID value.

Intel Agilex devices perform the SmartVID setup in the early stage of the configuration process. The SmartVID process will continue to monitor the V_{CC} and V_{CCP} voltage rails in user mode. The Power Manager monitors the temperature and adjusts the voltage when required. For more information, refer to the *Temperature Compensation* section.

Table 6. SmartVID Regulator Requirements

Specification	Value
Voltage range	0.6 V – 1.0 V
Voltage step	5 – 10 mV
Ramp time	<ul style="list-style-type: none"> • Non-CvP—10 mV/10 ms to 10 mV/20 μs • Configuration via Protocol (CvP)—10 mV/60 μs to 10 mV/20 μs ⁽¹⁾

⁽¹⁾ When the system is required to support the CvP functionality and meet the PCI Express* (PCIe*) link-up timing budget during the initial power up, the minimum ramp time is 10 mV/60 μ s.

Table 7. Supported Voltage Output Format for Intel Agilex Devices with the –V and –E Power Options

Voltage Output Format	Operating Modes	
	PMBus Master Mode	PMBus Slave Mode
Linear mode	Yes	No
VID mode	No	No
Direct mode	Yes	Yes, with coefficient $m=1$, $b=0$, and $R=0$

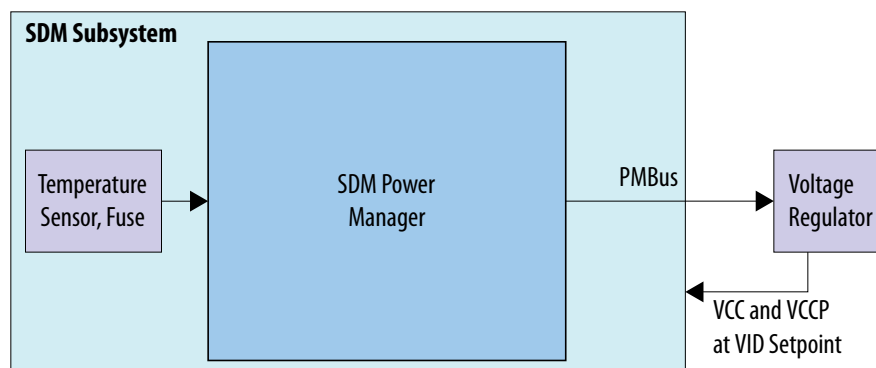
Related Information

Temperature Compensation on page 28

5.1.2. SDM Power Manager

In Intel Agilex devices, the SmartVID feature is managed by the SDM subsystem. The SDM subsystem is powered up after V_{CC} and V_{CCP} voltage levels are powered up to 0.8V. The SDM Power Manager reads the SmartVID programmed value and communicates this value to the external voltage regulator through the PMBus interface.

Figure 9. SDM Power Manager Block Diagram



The SDM Power Manager has the following stages:

- Initial/Shutdown stage
 - Set the external voltage regulator to supply power to V_{CC} and V_{CCP} to the voltage level based on the SmartVID programmed value and the device temperature.
 - Configures the FPGA and switches the FPGA to user mode.
- Monitor stage
 - Monitors temperature and updates V_{CC} and V_{CCP} .

The shutdown stage is triggered during device reconfiguration.

5.1.2.1. PMBus Master Mode

In the PMBus master mode, during the initial stage, the SDM Power Manager sets the external voltage regulator to supply V_{CC} and V_{CCP} voltage levels based on the SmartVID programmed value and the device temperature before it starts to configure the FPGA.

After entering user mode (in the monitor stage), the SDM Power Manager monitors temperature changes and decides if the V_{CC} and V_{CCP} output voltage values need to be updated. If voltages require updating, the SDM Power Manager identifies the voltage value based on the fuse values and the current temperature and sends the desired voltage value to the voltage regulators through the PMBus (PWRMGT_SCL and PWRMGT_SDA).

The PMBus master mode supports the multi-master mode.

Note: The PMBus master mode only supports the 1.8-V single-ended I/O standard.

Figure 10. PMBus Master Mode

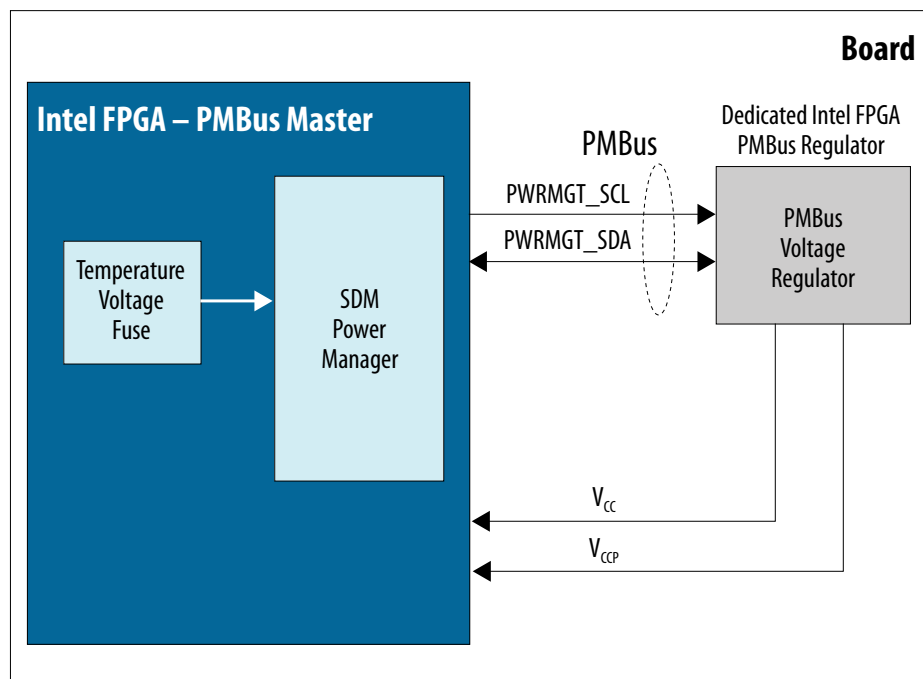


Table 8. Supported Commands for the PMBus Master Mode

Command Name	Command Code	PMBus Transaction Type	Number of Bytes
PAGE ⁽²⁾	00h	Write byte	1
VOOUT_MODE ⁽³⁾	20h	Read byte	1
continued...			

⁽²⁾ This is an optional command. This command is only applicable if you enable the PAGE command parameter. For more information, refer to the Power Management and VID Parameters section.



Command Name	Command Code	PMBus Transaction Type	Number of Bytes
VOUT_COMMAND	21h	Write word	2
READ_VOUT	8Bh	Read word	2
MFR_ADC_CONTROL ⁽⁴⁾	D8h	Write byte	1

5.1.2.2. PMBus Slave Mode

Intel Agilex devices can also be configured in the PMBus slave mode with an external power management controller acting as the PMBus master.

When you configure the Intel Agilex device in the PMBus slave mode, you must connect an additional PWRMGT_ALERT pin while connecting the existing PWRMGT_SCL and PWRMGT_SDA pins. The PWRMGT_ALERT pin is an active low signal.

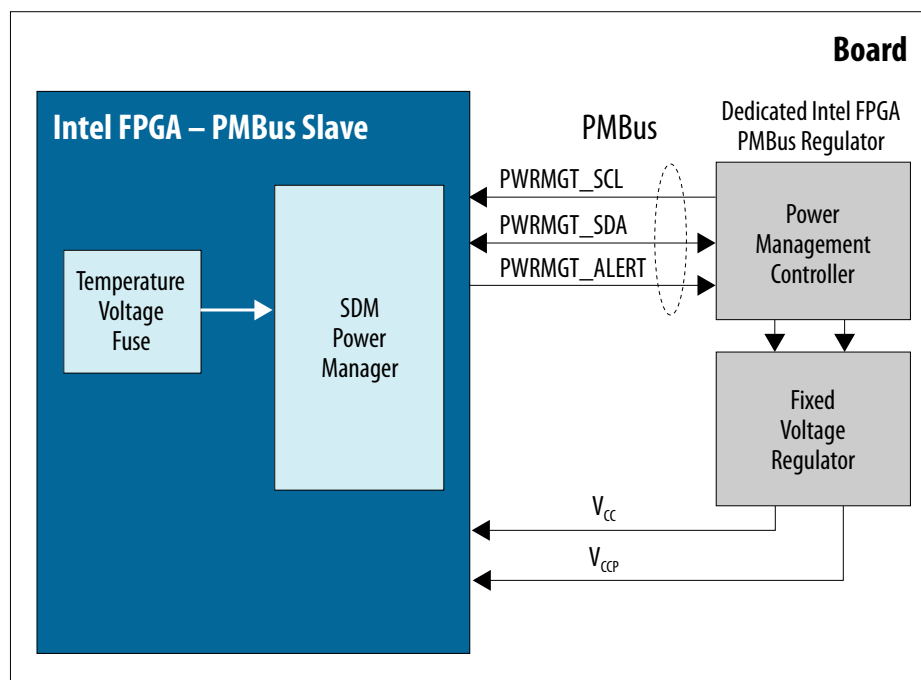
Note: The PMBus slave mode only supports the 1.8-V single-ended I/O standard.

The external PMBus master must poll the state of the PWRMGT_ALERT pin periodically, at an interval not longer than 100ms. When the PWRMGT_ALERT pin is asserted, the external master uses the Alert Response Address (ARA) flow to de-assert the ALERT signal and responds based on the STATUS_BYTE. The external master must also issue the VOUT_COMMAND every 200ms or less to check for a possible change in the target voltage due to temperature compensation.

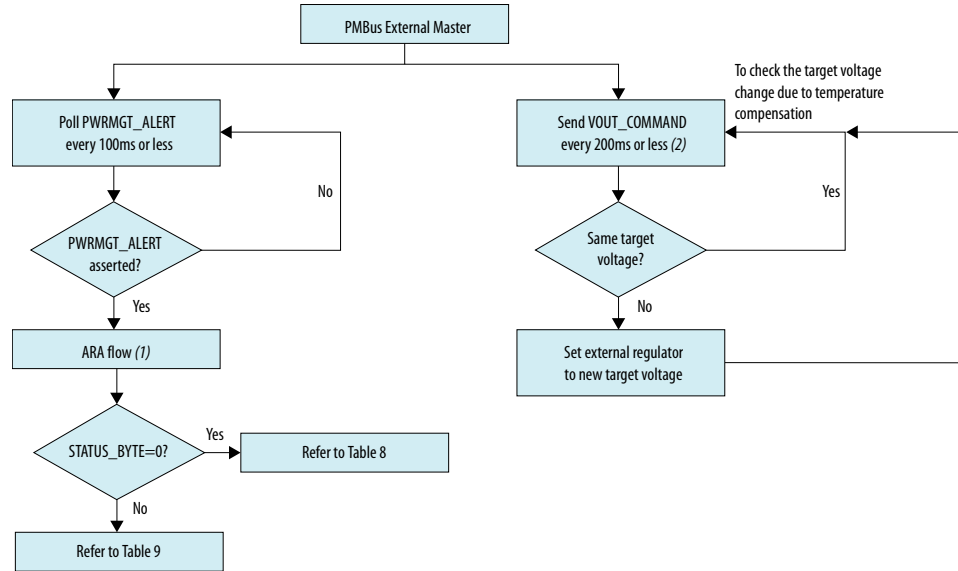
Note: The same VOUT_COMMAND is used for reading the target voltage from the SDM or setting the voltage regulator to the new target voltage. When the Intel Agilex device operates in the PMBus slave mode, the external master sends the VOUT_COMMAND to the SDM to get the target voltage required by the SDM. The external master then sends a VOUT_COMMAND to the voltage regulator to set its voltage.

⁽³⁾ This is an optional command. This command is only applicable if you select the Auto discovery in the voltage output format parameter. For more information, refer to the Power Management and VID Parameters section.

⁽⁴⁾ This command is sent when you set the device type to LTM4677 only.


Figure 11. PMBus Slave Mode

Table 9. Supported Commands for the PMBus Slave Mode

Command Name	Command Code	Default	PMBus Transaction Type	Number of Bytes
CLEAR_FAULTS	03h	—	Send byte	0
VOUT_MODE	20h	40h	Read byte	1
VOUT_COMMAND	21h	—	Read word	2
STATUS_BYTE	78h	00h	Read byte	1

Figure 12. External PMBus Master Software Flow

Notes:

(1) When operating in the slave mode, the master and slave use the alert response address (ARA) flow to assert or de-assert the PWRMGT_ALERT signal.

The following are the details of the ARA flow:

(a) When operating in the slave mode, the slave device uses the ALERT signal to indicate the master device that an update is required.

(b) Upon reception of the ALERT signal, the external master device uses the ARA flow to determine which slave device has asserted the ALERT signal.

(c) The ARA flow is one-byte, broadcast read from the master device to the reserved SMBus Alert Response Address (0x0C).

(d) The slave device that has asserted the ALERT signal responds to this ARA flow with its address.

(e) The slave device de-asserts the ALERT signal after providing its address in step (4). The external master device uses the address provided to communicate with the correct slave device.

(2) For reconfiguration in the user mode, you must ensure:

(a) VOUT_COMMAND is completed before setting nCONFIG = 0. The VOUT_COMMAND is completed once the master device receives two bytes of data following the VOUT_COMMAND.

(b) The VOUT_COMMAND is not issued within 50 ms after setting nCONFIG = 0.

Table 10. Stage Flow for the External PMBus Master when the ALERT Signal is Asserted and STATUS_BYTE=0

Sequence	SDM	PMBus Master	Notes
1	Asserts the ALERT signal	—	—
2	—	Detects the ALERT signal	—
3	—	Initiates the ARA flow	—
4	Responds to the ARA flow and provides its address	—	Only the device which has asserted the ALERT signal in step 1 responds to the ARA flow by providing its address.
5	De-asserts the ALERT signal	—	The ALERT signal is only de-asserted after the SDM responds with its address in the ARA flow.
6	—	Reads the STATUS_BYTE	—
7	Returns STATUS_BYTE=0	—	Indicates the FPGA voltage requires an update.
8	—	Sends CLEAR_FAULTS	—
continued...			



Sequence	SDM	PMBus Master	Notes
9	—	Sends VOUT_COMMAND	The VOUT_COMMAND must be received by the SDM within 200ms after the ALERT signal is asserted. Failure to meet this requirement will cause configuration error. ⁽⁵⁾
10	Receives the VOUT_COMMAND, responds with the target voltage	—	Calculated based on the temperature, the VID fuse and the coefficient for the direct format (you need to specify this input).
11	—	Sets the voltage regulator to the target voltage in step size not greater than 10mV/10ms step	—

Table 11. Stage Flow for the External PMBus Master when the ALERT Signal is Asserted and STATUS_BYTE is not equals to 0

Sequence	SDM	PMBus Master	Notes
1	Asserts the ALERT signal	—	The SDM detects fault and asserts the ALERT signal. ⁽⁶⁾
2	—	Detects the ALERT signal	—
3	—	Initiates the ARA flow	—
4	Responds to the ARA flow and provides its address	—	Only the device which has asserted the ALERT signal in step 1 responds to the ARA flow by providing its address.
5	De-asserts the ALERT signal	—	The ALERT signal is only de-asserted after the SDM responds with its address in the ARA flow.
continued...			

⁽⁵⁾ When there is an error triggered by the SDM because it did not receive the VOUT_COMMAND within the specified time, you must power cycle the device to recover from the error. If you do not power cycle the device to recover from the error, you will not be able to configure the device successfully.

⁽⁶⁾ The following faults can raise the ALERT signal:

- PMBUS_ERR_RD_TOO_MANY_BYTES (Error with the length of the PMBus/I2C message length)
- PMBUS_ERR_WR_TOO_MANY_BYTES (Error with the length of the PMBus/I2C message length)
- PMBUS_ERR_UNSUPPORTED_CMD (VOUT_COMMAND, VOUT_MODE, READ_STATUS, and CLEAR_FAULTS are the only supported commands in the PMBUS Slave Mode)
- PMBUS_ERR_READ_FLAG (Received duplicate command before being able to respond to the first command)
- PMBUS_ERR_INVALID_DATA (Invalid or malformed PMBus/I2C message)

If any of the above errors are detected, the ALERT signal is raised and bit 1 of the status register is set.

Sequence	SDM	PMBus Master	Notes
6	—	Reads the STATUS_BYTE	—
7	Returns the STATUS_BYTE when not equal to 0	—	Indicates that other fault has occurred
8	—	Sends CLEAR_FAULTS	To reset the STATUS_BYTE.
9	—	Reads the STATUS_BYTE	To confirm that STATUS_BYTE=0
10	—	External master to handle the faults	—

The Intel Agilex device in the PMBus slave mode sends the VOUT_COMMAND value in the direct format only. To read the actual voltage value, use the following equation to convert the VOUT_COMMAND value from the Intel Agilex device.

Figure 13. Direct Format Equation

$$X = \frac{1}{m} (Y \times 10^{-R} - b)$$

The equation shows how to convert the direct format value where:

- X, is the calculated, real value in mV;
- m, is the slope coefficient, a 2-byte two's complement integer;
- Y, is the 2-byte two's complement integer received from the Intel Agilex device;
- b, is the offset, a 2-byte two's complement integer;
- R, is the exponent, a 1-byte two's complement integer

The following example shows how an external power management controller retrieves values from the Intel Agilex device. Coefficients used in the VOUT_COMMAND are as follows:

- m = 1
- b = 0
- R = 0

If the external power management controller retrieved a value of 0384h, it is equivalent to the following:

$$X = (1/1) \times (0384h \times 10^{-0} - 0) = 900 \text{ mV} = 0.90 \text{ V}$$

5.1.3. Temperature Compensation

Intel Agilex devices are able to compensate for performance degradation at colder temperatures by raising the voltage. While raising the voltage increases the dynamic power consumption, the increase in dynamic power consumption is countered by lower leakage at cold temperatures, thus enabling total power consumption at cold temperatures to still be lower than at hot temperatures.

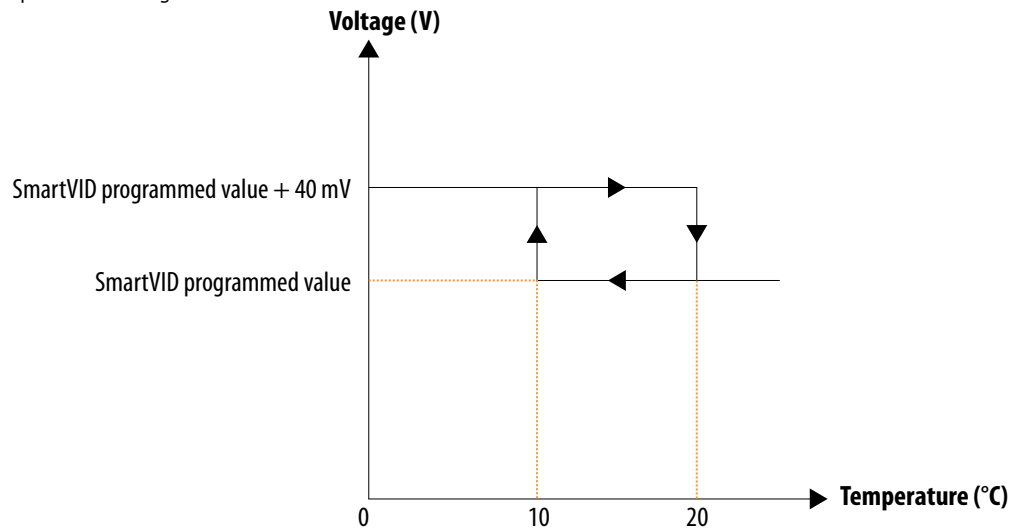


The SmartVID feature supports this dynamic voltage adjustment. The SDM Power Manager checks for temperature changes and updates the new VID value if the temperature crosses the threshold point.

Note: The temperature compensation feature is only supported in the industrial device grade.

Figure 14. Temperature Compensation for SmartVID for Intel Agilex Devices—Preliminary

The SDM monitors the temperature, normally at every 100 ms, and adjusts the voltage by communicating with an external power management system. Adjustment is made by the SDM after the sensor detects the temperature setting is below 10 °C or above 20 °C.



5.1.4. Intel Agilex Power Management and VID Implementation Guide

The Intel Agilex SDM Power Management Firmware manages the SmartVID configuration and enables the FPGA to power up before you can access the FPGA.

5.1.4.1. Intel Agilex Power Management and VID Interface Getting Started

The Intel Agilex Power Management and VID interface is installed as part of the Intel Quartus Prime software.

5.1.4.1.1. Specifying Power Management and VID Parameters and Options

1. Create an Intel Quartus Prime project using the **New Project Wizard** available from the File menu.
2. On the **Assignments** menu, click **Device**.
3. On the **Device** dialog box, click **Device and Pin Options**.
4. On the **Device and Pin Options** dialog box, click **Configuration**.
5. On the **Configuration** page, specify the **VID Operation mode**. There are two modes available—PMBus Master and PMBus Slave.



6. The PMBus modes require these pins—PWMGT_SDA, PWMGT_SCL, and PWRMGT_ALERT. To configure these pins, on the **Configuration** page, click **Configuration Pin Options**. The PWRMGT_ALERT pin is only available and used in the slave mode. For the configuration pin parameters, refer to [Table 12](#) on page 30.
7. On the **Configuration Pin** dialog box, assign the appropriate SDM_IO pin to the power management pins. Click **OK**.
8. On the **Device and Pin Options** dialog box, click **Power Management and VID** to specify the device settings if your device is in the PMBus Master mode. Click **OK**. For the power management and VID parameters, refer to [Table 13](#) on page 31.

This completes the SmartVID setup for the Intel Agilex device.

Configuration Pin Parameters

Table 12. Configuration Pin Parameters

Use the parameter editor to configure these options.

Parameters	Value	Description
Use PWRMGT_SCL output	SDM_IO0	This is a required PMBus interface for the power management when the VID operation mode is the PMBus Master or PMBus Slave mode. Disable this parameter for the non-SmartVID device. Intel recommends using the SDM_IO14 pin for this parameter.
	SDM_IO14	
Use PWRMGT_SDA output	SDM_IO11	This is a required PMBus interface for the power management when the VID operation mode is the PMBus Master or PMBus Slave mode. Disable this parameter for the non-SmartVID device. Intel recommends using the SDM_IO11 pin for this parameter.
	SDM_IO12	
	SDM_IO16	
Use PWRMGT_ALERT output	SDM_IO0	This is a required PMBus interface for the power management that is used only in the PMBus Slave mode. Disable this parameter for the non-SmartVID device. Intel recommends using the SDM_IO12 pin for this parameter.
	SDM_IO12	

Power Management and VID Parameters

You can use the following parameters to configure the Power Management and VID interface if the VID operation is in the PMBus Master mode.

**Table 13. Power Management and VID Parameters**

Parameters	Value	Description
Bus speed mode ⁽⁷⁾	100 KHz	Bus speed mode of PMBus interface when operating in the PMBus Master mode.
	400 KHz	
Slave device type ⁽⁷⁾	ED8401	Supported device types.
	EM21XX	
	EM22XX	
	ISL82XX	
	LTM4677	
	Other	
Device address in PMBus Slave mode ⁽⁸⁾	7-bit hexadecimal value	Device address in the PMBus Slave mode.
Slave device_0 address ⁽⁷⁾	7-bit hexadecimal value	External power regulator address. This parameter must be non-zero when you are using the PMBus Master mode.
Slave device_1 address ⁽⁷⁾	7-bit hexadecimal value	External power regulator address.
Slave device_2 address ⁽⁷⁾	7-bit hexadecimal value	External power regulator address.
Slave device_3 address ⁽⁷⁾	7-bit hexadecimal value	External power regulator address.
Slave device_4 address ⁽⁷⁾	7-bit hexadecimal value	External power regulator address.
Slave device_5 address ⁽⁷⁾	7-bit hexadecimal value	External power regulator address.
Slave device_6 address ⁽⁷⁾	7-bit hexadecimal value	External power regulator address.
Slave device_7 address ⁽⁷⁾	7-bit hexadecimal value	External power regulator address.
Voltage output format ⁽⁷⁾	Auto discovery	<p>The voltage output format when the operation mode is PMBus Master.</p> <p>If the voltage output format is the Auto discovery or Direct format, you must set the following parameters:</p> <ul style="list-style-type: none"> • Direct format coefficient m • Direct format coefficient b • Direct format coefficient R <p>If the voltage regulator is the Linear format, you must set the Linear format N parameter.⁽⁹⁾</p>
	Direct format	
	Linear format	
Direct format coefficient m ⁽⁷⁾	Signed integer: -32768 to 32767	Direct format coefficient m of the slave device type when the operation mode is PMBus Master.
Direct format coefficient b ⁽⁷⁾	Signed integer: -32768 to 32767	Direct format coefficient b of the slave device type when the operation mode is PMBus Master.

continued...⁽⁷⁾ This parameter is used for the PMBus Master mode.⁽⁸⁾ This parameter is used for the PMBus Slave mode.⁽⁹⁾ N is the exponent of a 5-bit two's complement integer.



Parameters	Value	Description
Direct format coefficient R ⁽⁷⁾	Signed integer: -128 to 127	Direct format coefficient R of the slave device type when the operation mode is PMBus Master.
Linear format N ⁽⁷⁾	Signed integer: -16 to 15	Output voltage command when the voltage output format is set to the Linear format.
Translated voltage value unit ⁽⁷⁾	millivolts	Indicates the translated output voltage is in millivolts (mV) or volts (V).
	volts	
Enable PAGE command ⁽⁷⁾	Enable	By enabling the PAGE command, the FPGA PMBus Master mode will use the PAGE command to set all the output channels on registered regulator modules to respond to VOUT_COMMAND.
	Disable	

Intel Agilex Power Management and VID Interface QSF Constraint Guide

You can specify the **Power Management and VID** parameters and options through QSF constraints command.

For the configuration pin parameters, refer to [Table 12](#) on page 30. For the power management and VID parameters, refer to [Table 13](#) on page 31.



Example 1. Specifying the Power Management and VID Parameters through QSF Constraints

```
set_global_assignment -name USE_PWRMGT_SDA SDM_IO11
set_global_assignment -name USE_PWRMGT_SCL SDM_IO14
set_global_assignment -name PWRMGT_SLAVE_DEVICE_TYPE LTM4677
set_global_assignment -name PWRMGT_SLAVE_DEVICE0_ADDRESS41
set_global_assignment -name PWRMGT_SLAVE_DEVICE1_ADDRESS42
set_global_assignment -name PWRMGT_SLAVE_DEVICE2_ADDRESS43
set_global_assignment -name PWRMGT_SLAVE_DEVICE3_ADDRESS44
set_global_assignment -name PWRMGT_SLAVE_DEVICE4_ADDRESS45
set_global_assignment -name PWRMGT_SLAVE_DEVICE5_ADDRESS46
set_global_assignment -name PWRMGT_SLAVE_DEVICE6_ADDRESS47
set_global_assignment -name PWRMGT_SLAVE_DEVICE7_ADDRESS48
set_global_assignment -name VID_OPERATION_MODE "PMBUS MASTER"
set_global_assignment -name PWRMGT_BUS_SPEED_MODE "100 KHZ"
set_global_assignment -name PWRMGT_PAGE_COMMAND_ENABLE ON
set_global_assignment -name PWRMGT_VOLTAGE_OUTPUT_FORMAT "AUTO DISCOVERY"
set_global_assignment -name PWRMGT_TRANSLATED_VOLTAGE_VALUE_UNIT VOLTS
```

5.2. DSP and M20K Power Gating

Intel Agilex devices support power gating for both DSP blocks and M20K memory blocks. By default, the Intel Quartus Prime software automatically configures unused DSP blocks and M20K memory blocks to be power gated.

5.3. Clock Gating

Clock gating can be used to reduce dynamic power consumption. When an application is idle, its clock can be gated temporarily and ungated based on wake-up events. This is done using user logic to enable or disable the programmable clock routing.

You can perform dynamic power reduction by gating the clock signals of any circuitry not used by the design in the Intel Agilex devices. The sector clock gating is done at the multiplexer level.

Clock gating a large portion of your FPGA design could cause significant current change over a short time period when the gated circuitry is enabled or disabled. The maximum current step resulting from this clock gating should be sized such that it does not create noise exceeding the maximum allowed AC noise specification, as



determined by the PDN decoupling design on your PCB. You can control the current step size by dividing a large gated area into smaller sub-regions and staging those regions to enter or exit power gating sequentially.

For more details, refer to the *Clock Gating* section in the *Intel Agilex Clocking and PLL User Guide*.

Related Information

[Intel Agilex Clocking and PLL User Guide](#)

Provides more information about clock gating.

5.4. Power Sense Line

Intel Agilex devices support the power sense line feature. VCCLSENSE and GNDSENSE pins are differential remote sense pins used to monitor the V_{CC} power supply.

You must connect the VCCLSENSE and GNDSENSE pins to the remote sense inputs for the regulator supplying V_{CC} rail that supports the remote voltage sensing feature.

5.5. Power Optimization Techniques in the Intel Quartus Prime Software

The Intel Quartus Prime software offers power-driven compilation to fully optimize device power consumption.

Power-driven compilation focuses on reducing the design's total power consumption in synthesis and place-and-route stages. For detailed information, refer to the *Intel Quartus Prime Pro Edition User Guide: Power Analysis and Optimization*.

Related Information

[Intel Quartus Prime Pro Edition User Guide: Power Analysis and Optimization](#)

6. Document Revision History for the Intel Agilex Power Management User Guide

Document Version	Changes
2020.04.22	<ul style="list-style-type: none"> Added the <i>Guidelines for I/O Pins in GPIO, HPS, and SDM Banks During Power Sequencing</i> section. Added the F-tile and R-tile power rails in the <i>Voltage Rails Group</i> table. Added V_{CCR_CORE} power supply to the <i>Power Supplies Monitored by the POR Circuitry</i> section. Added the <i>Supported Voltage Output Format for Intel Agilex Devices with the -V and -E Power Options</i> table. Updated the table that provides an overview of the local and remote temperature sensors to clarify that the local temperature sensor operates only in user mode. Updated the topic about the temperature sensor channels and locations: <ul style="list-style-type: none"> Updated the description from using "channels" to "locations". Updated the diagram showing the sensor locations. Updated the table listing the sensor locations and equivalent remote TSD pins. Added topic about retrieving the local temperature sensor reading. Updated the voltage monitor design guidelines to add V_{SIGN} and V_{SIGN} pins guideline. Added the E-tile transceiver local temperature sensor design guidelines.
2020.02.06	<ul style="list-style-type: none"> Updated the <i>PMBus Slave Mode</i> section. Added $V_{CC_HSSI_GXE}$, $V_{CCRTPLL_GXE}$, V_{CCR_CORE}, $V_{CCIO_PIO_SDM}$, and V_{CCBAT} power rails to the <i>Voltage Rails Group</i> table. Removed $V_{CCRTPLL_CR3_GXE}$ and V_{CCM_WORD} power rails from the <i>Voltage Rails Group</i> table. Removed the <i>Power Distribution</i> section.
2019.10.04	<ul style="list-style-type: none"> Changed the Early Power Estimator (EPE) tool name to Intel FPGA Power and Thermal Calculator. Added the <i>Intel Agilex Power Management and VID Interface QSF Constraint Guide</i> section. Added ED8401, EM21XX, and EM22XX device selection in the slave device type parameters in the <i>Power Management and VID Parameters</i> table. Updated the power optimization information in the <i>Intel Agilex Power Management Overview</i> section. Updated the <i>Early Power Estimator (EPE)</i> section. Updated the <i>Power Supplies Monitored by the POR Circuitry</i> section to remove the note on powering up V_{CCBAT} when not using the volatile key. Updated the <i>SmartVID Standard Power Devices</i> section to update the voltage value for V_{CC} and V_{CCP} during power up. Updated the V_{CCA_PLL} power rail from Group 2 to Group 3 in the <i>Voltage Rails Group</i> table. Updated the <i>Stage Flow for the External Power Management Controller in the PMBus Slave Mode</i> figure. Changed the voltage and temperature sensors IP support from Temperature Sensor and Voltage Sensor IPs to Mailbox Client and Mailbox Avalon ST IPs. Updated the <i>Local Temperature Sensor</i> topic to add information about the catastrophic trip ($nCATTRIP$) signal. Added reference to the <i>Intel Agilex Design Guideline Training: IBIS AMI Link Simulation, PDN, EMIF Layout Guidelines</i>. Removed the <i>Power Dissipation and Thermal Considerations</i> section.
2019.04.02	Initial release.