1. Introduction

This document illustrates how to setup the DCC demo on the DE10-Standard and the DCC(Data Conversion HSMC Daughter Board) as shown in **Figure 1**. The basic design content is also included. In this demonstration, please refer to the DE10-Standard user manual. For details about the DCC, please refer to the user manual of Data Conversion HSMC daughter card.

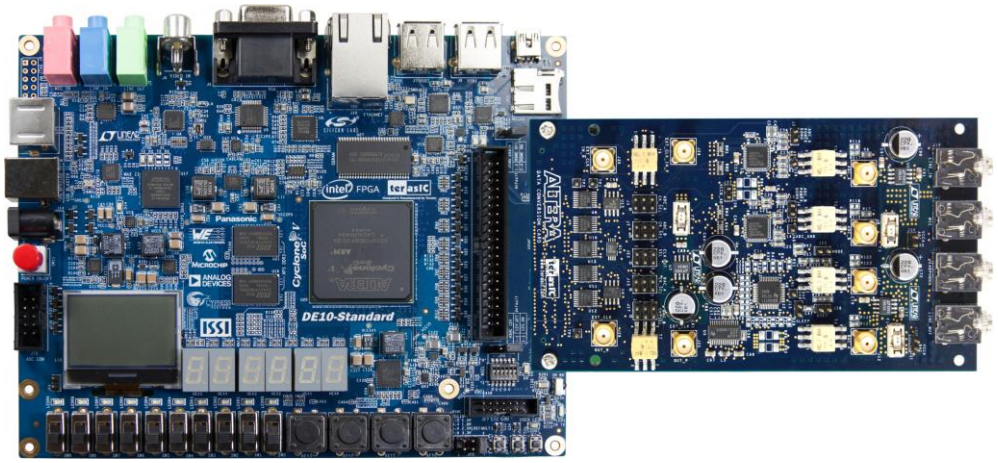

Figure 1 DCC Demo

2. System Requirements

The following items are required to perform this demonstration:

- DE10-Standard and power supply
- DCC(Data Conversion HSMC) daughter card

3. Execute Demonstration

- **Please follow the procedures below to setup the demonstration:**

1. Make sure both Quartus II and USB-Blaster II driver are installed on the host PC.
2. Power off the DE10-Standard board.
3. Connect a mini-USB cable to an UB2 port of the DE10-Standard and the host PC.
4. Connect the Data Conversion HSMC Daughter Board onto the HSMC port(JP2) expansion header of the DE10-Standard.
5. SMA cable to connect ADC_A(J4) with DAC_A(J12) or ADC_B(J8) with DAC_B(J14) depending on which channel you are operating on.
6. Power on the DE10-Standard Board.
7. Open stp1.stp from SignalTap Analyzer

■ Collecting Data using the Signal Tap II Logic Analyzer:

1. Click “Program Device” after Hardware and Device are detected correctly.
2. Click “Autorun Analysis”
3. Observe signals “sine_1” and “sine_10” which output two sine waves where one is running 10 times the frequency of the other.
4. Observe the signal “p_sine” which output the combination of two sine waves, “sine_1” and “sine_10” respectively.
5. Observe the signal “a2d_data” which is the input signal looped back from the A/D generating an attenuated combination of two sine waves. (Note: The A/D converter output is attenuated because of losses in the analog circuitry, transformers, and terminators on the board.)
6. By pressing “KEY0” and “KEY1” will reset the “1 MHz” and 10 MHz” numerically controlled oscillator respectively.
7. By switching the “SW0” on the DE10-Standard board in the “UP” position, it sets the data format in the A/D converter to “binary format”. Leaving the “SW0” in the “DOWN” position, will generate the data format in ‘Twos complement” as shown in **Figure 1**.
8. Choose File -> Create/Update -> Create SignalTap II List File and the Quartus II will generate the filestp1_auto_signaltap_0.txt in the project directory

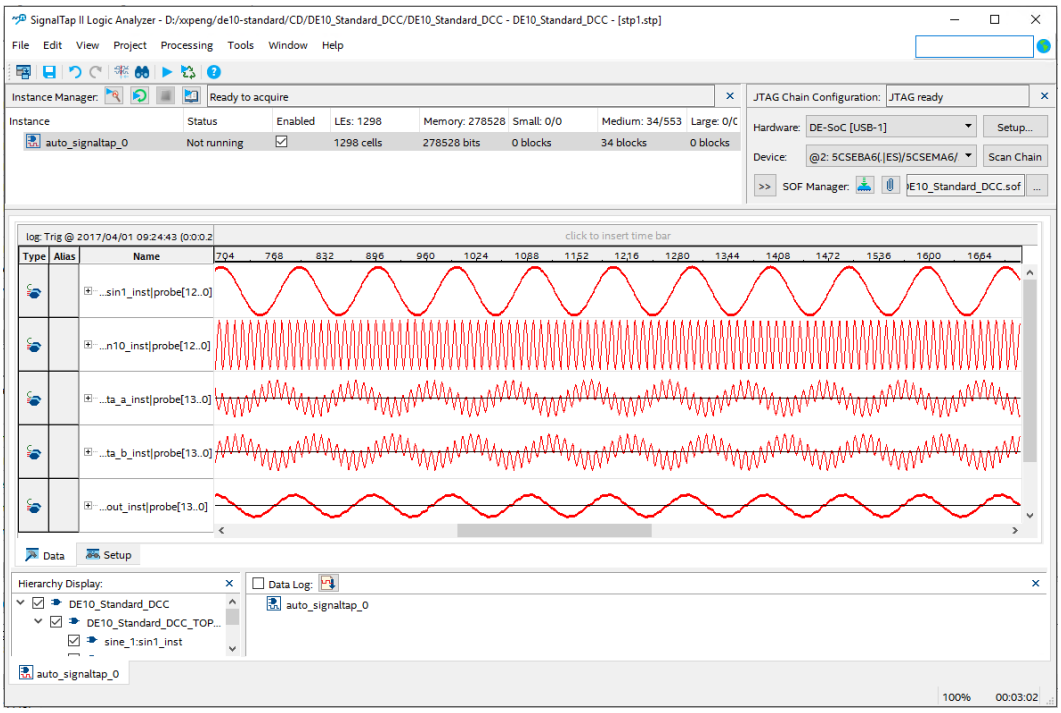

Figure 2 stp1.stp displayed in the SignalTap II Logic Analyzer

■ Configuration Setup and Indicators

User Interface	*Description*
LED[0]	**PLL locked Indicator. Light = Locked**
LED[1]	**ADC DFS (Data Format Select) Indicator**
LED[2]	**ADC DCS (Duty Cycle Stabilizer Select) Indicator**
LED[3]	**ADC Out-of-Range Indicator. Light = Out-of-Range**

LED[4]	**1MHz NCO Output Disable Indicator. Light = Disable**
LED[5]	**10MHz NCO Output Disable Indicator. Light = Disable**
LED[6]	**Channel A or B Indicator. Light = Channel B Select**
LED[7]	**Heartbeat**
SW[0]	**ADC DFS (Data Format Select)**
SW[1]	**ADC DCS (Duty Cycle Stabilizer Select)**
SW[2]	**Channel A or B Select. High selects channel B**
KEY[0]	**1MHz NCO Output Disable**
KEY[1]	**10MHz NCO Output Disable**
KEY[2]	**Not Used**
KEY[3]	**Reset**

4. Project Description

Figure 3 shows the system block diagram of DCC demonstration. The Data Conversion HSMC daughter board reference design contains two sine waves that are generated by two instances of the Altera numerically controlled oscillator (NCO) MegaCore. One of these oscillators is running at 10 times the frequency of the other, but both of them have the same amplitude with each one covering 13 bits of dynamic range. From these blocks, the two sine waves output are converted from two's complement binary to unsigned binary format which then are added together. The combined sine wave signal of 14-bits dynamic range is sent to a 14-bit D/A converter. The analog output of a D/A converter is connected via SMA cable with the analog input of a 14-bit A/D converter. The A/D converter's digital output is looped back to the FPGA device. The A/D is configured by the dip switches to deliver the data in unsigned format. The converted loopback data is captured by an instance of the SignalTap® II logic analyzer in the design for 3 display and analysis. **Figure 1** shows a high-level view of the reference design and how it interacts with the D/A and A/D converters on the Data Conversion HSMC.

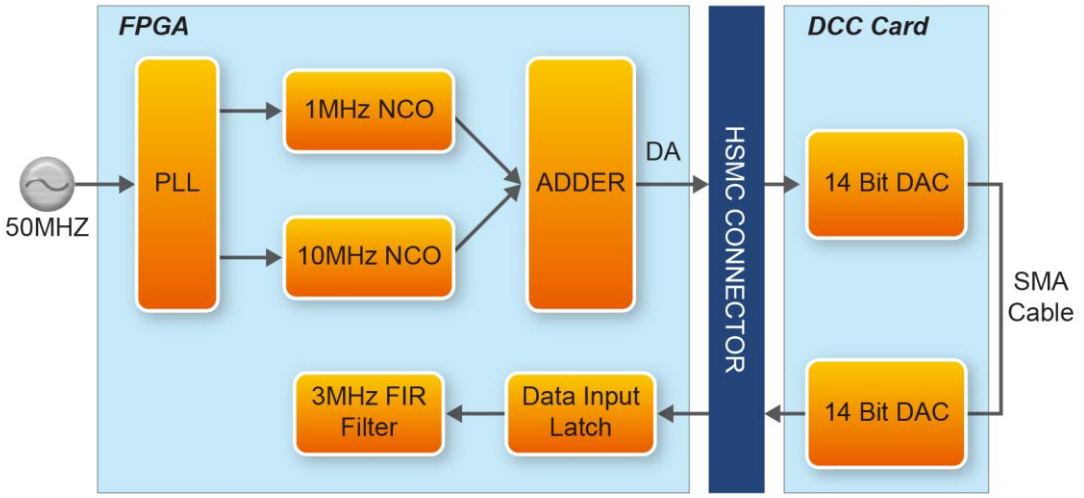

Figure 3 System Block Diagram