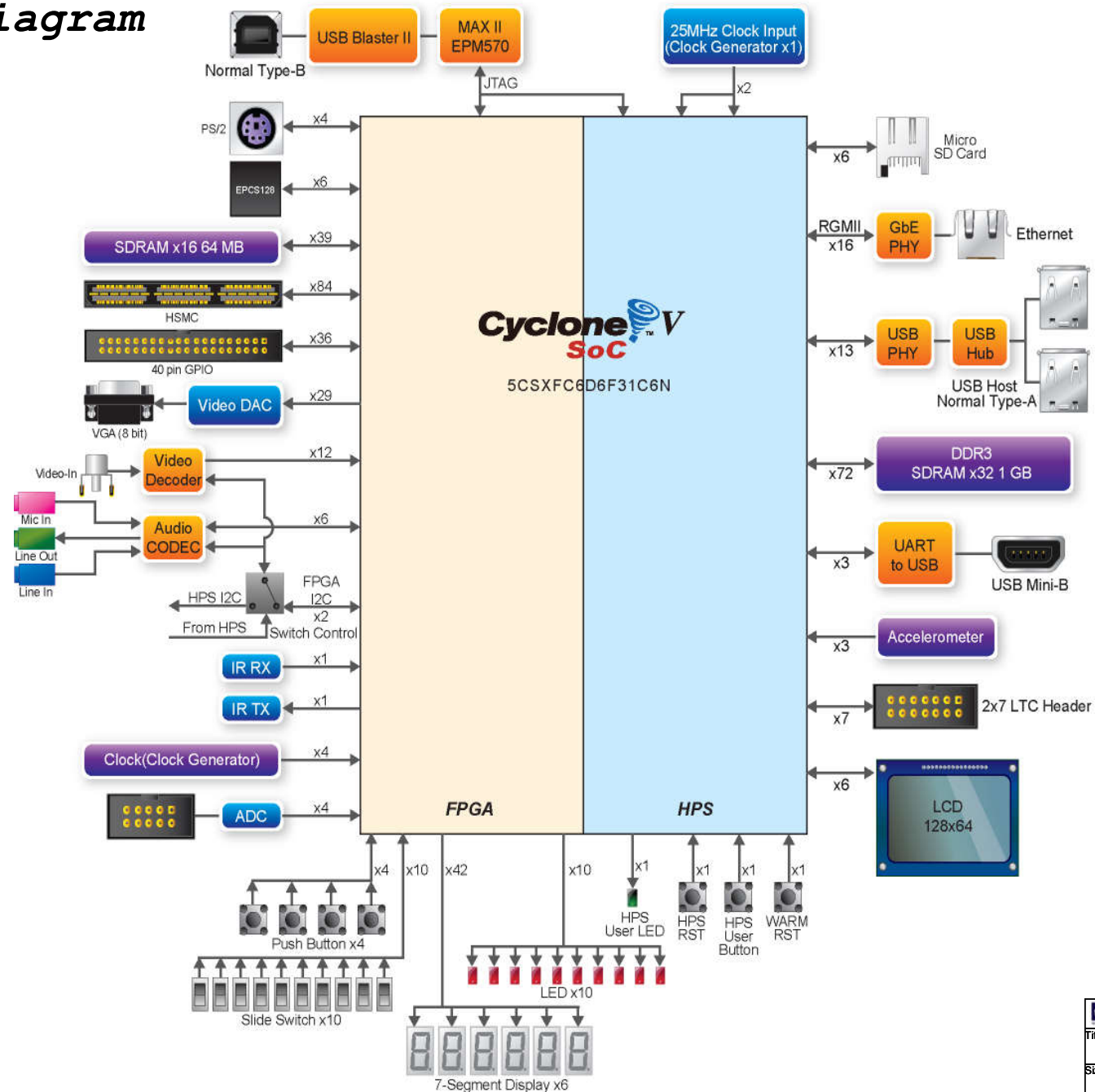
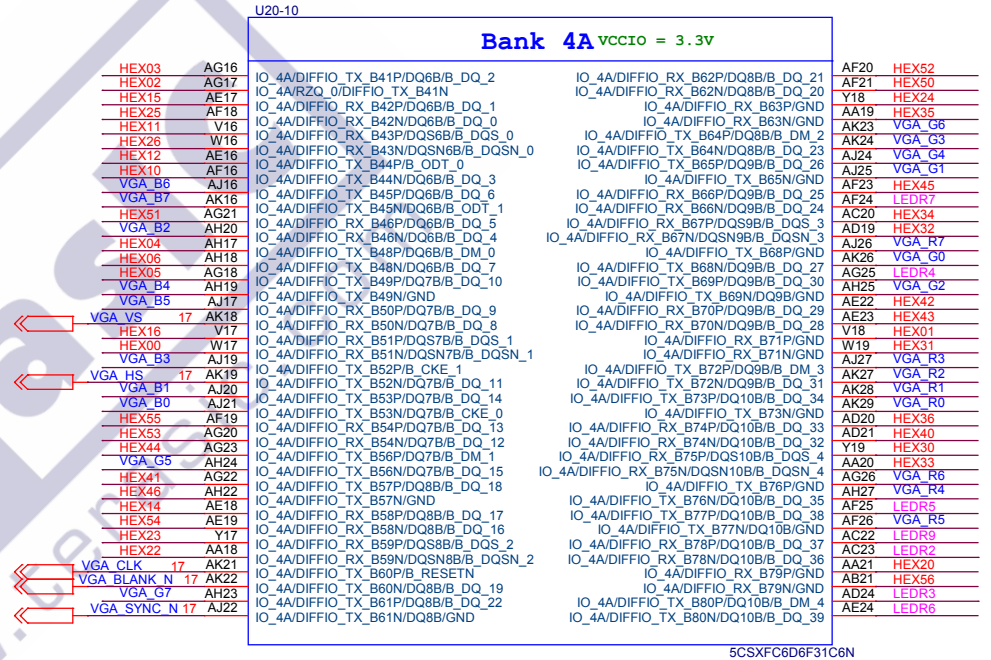
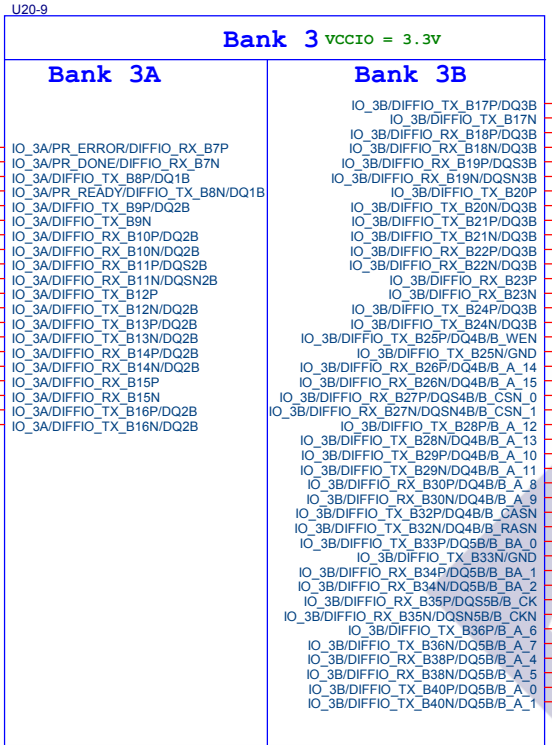
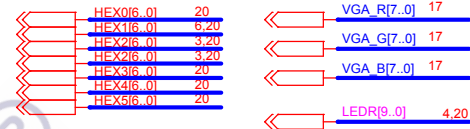


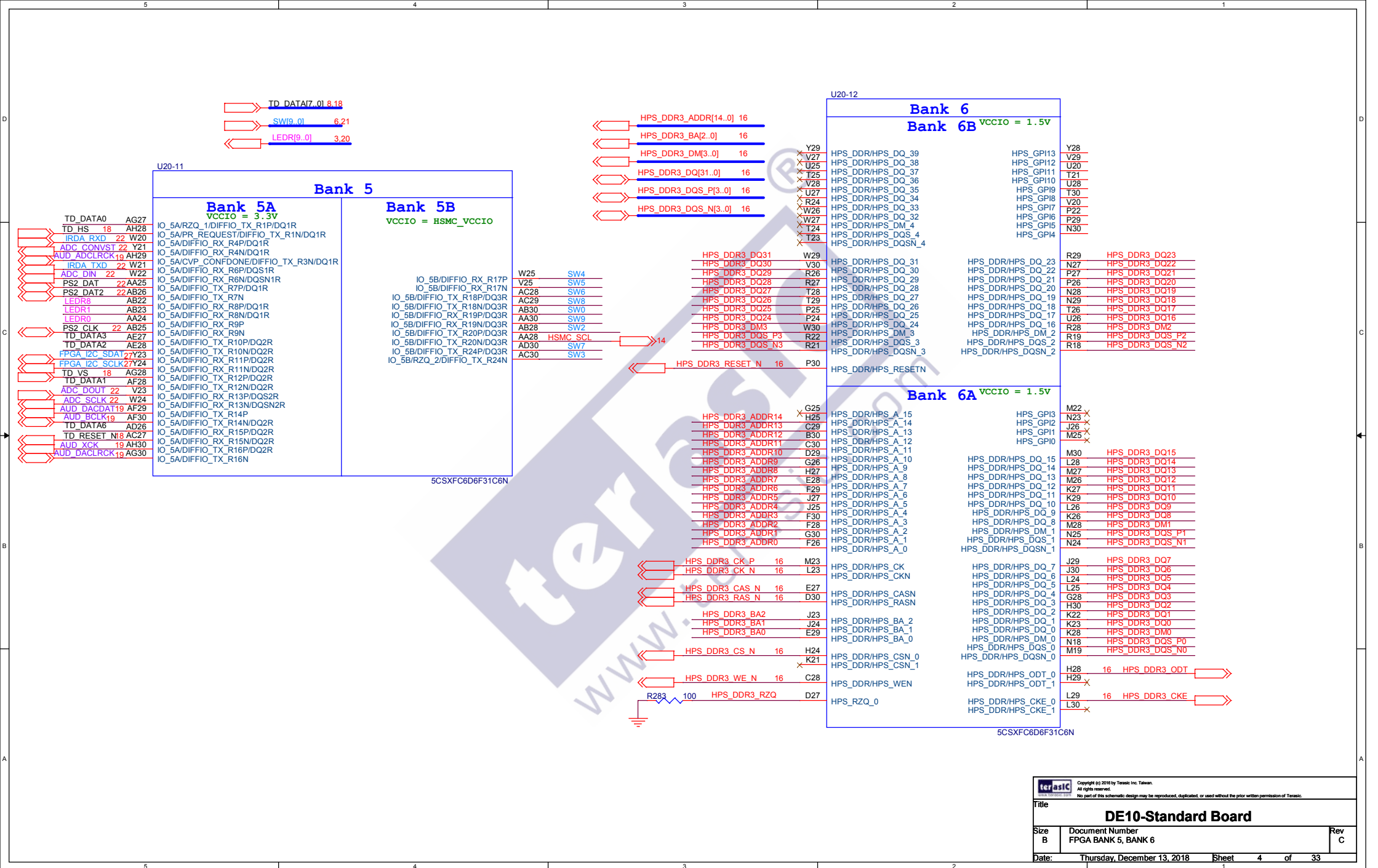
ALTERA Cyclone V SoC Development & Education Board (DE10-Standard)

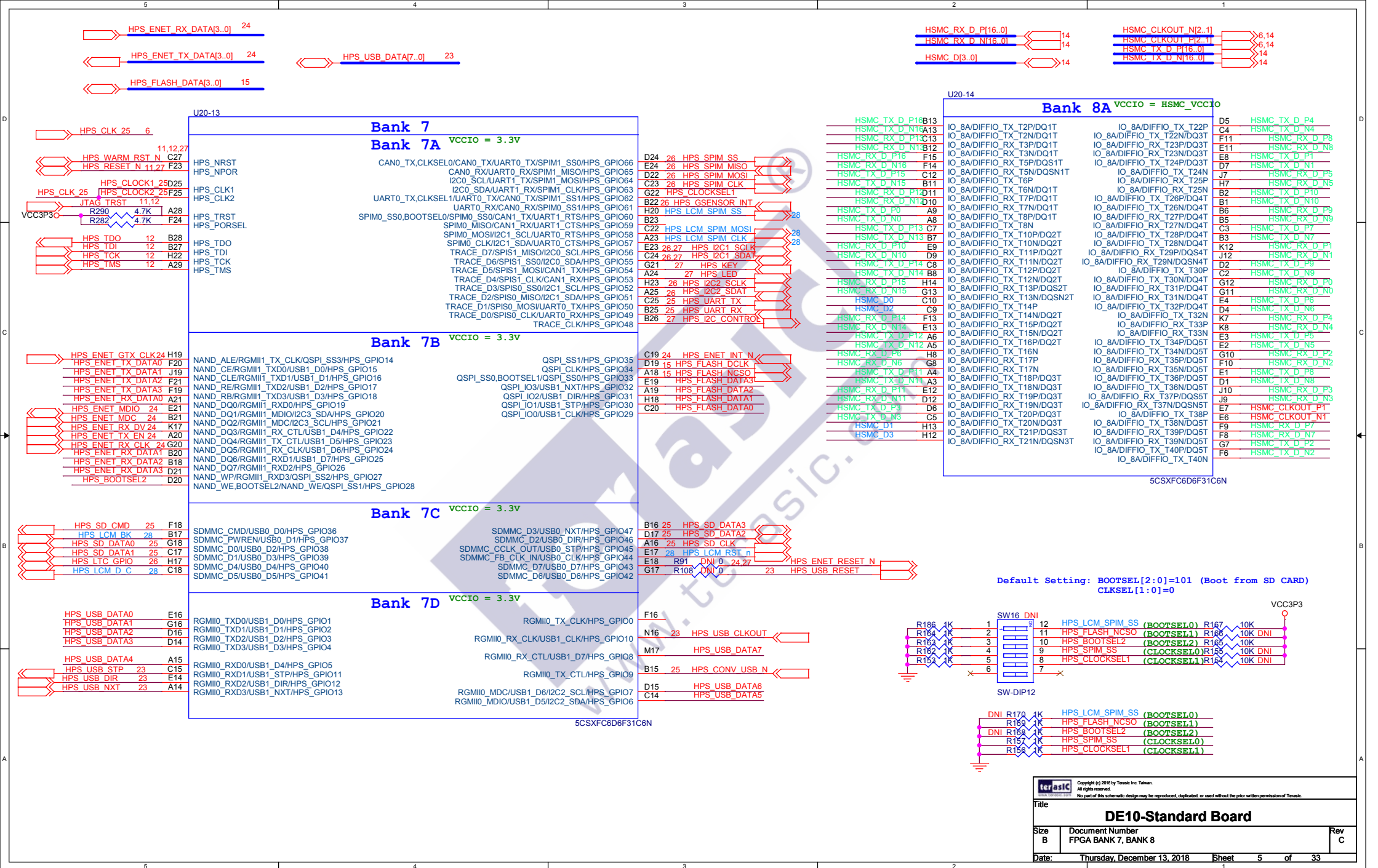
PAGE	CONTENT	PAGE	CONTENT
1	Cover Page	18	ADV7180 Video Decoder
2	Block Diagram	19	Audio CODEC
3	FPGA BANK 3, BANK 4	20	7-Segment Display, LED
4	FPGA BANK 5, BANK 6	21	FPGA BUTTON, Switch
5	FPGA BANK 7, BANK 8	22	ADC, PS2, IR Tx, IR Rx
6	FPGA Clocks, GND	23	2-port USB Host
7	Transceiver	24	1 Gigabit Ethernet
8	FPGA Configuration	25	UART to USB, SD CARD
9	FPGA Decoupling	26	Accelerometer, LTC Connector
10	FPGA Power	27	I2C Multiplexer, HPS BUTTON, HPS LED
11	USB Blaster II	28	LCD
12	JTAG Chain	29	Power - 1.1V
13	GPIO	30	Power - 5V, 3.3V
14	HSMC	31	Power - 9V, 2.5V, 1.5V
15	SDRAM, HPS QSPI Flash	32	Power - 1.2V, 1.8V, DDR3 VREF, DDR3 VTT
16	HPS DDR3 SDRAM	33	Power - VCCIO_HSMC & HSMC_VCCPD
17	ADV7123 VGA		

Block Diagram









U20-2

Clocks

Bank 3B VCCIO = 3.3V

IO_3B/CLK0P,FPLL_BL_FBP/DIFFIO_RX_B31P
IO_3B/CLK0N,FPLL_BL_FBN/DIFFIO_RX_B31N
GPIO0 W15
GPIO2 Y16
IO_3B/CLK1P/DIFFIO_RX_B39P
IO_3B/CLK1N/DIFFIO_RX_B39N

Bank 4A VCCIO = 3.3V

IO_4A/CLK2P/DIFFIO_RX_B47P
IO_4A/CLK2N/DIFFIO_RX_B47N
IO_4A/CLK3P/DIFFIO_RX_B55P
IO_4A/CLK3N/DIFFIO_RX_B55N

Bank 5B VCCIO = HSMC_VCCIO

IO_5B/CLK4P,FPLL_BR_FBP/DIFFIO_RX_R23P/DQ3R
IO_5B/CLK4N,FPLL_BR_FBN/DIFFIO_RX_R23N/DQ3R
IO_5B/CLK5P/DIFFIO_RX_R21P/DQ53R
IO_5B/CLK5N/DIFFIO_RX_R21N/DQ53R

Bank 8A VCCIO = HSMC_VCCIO

IO_8A/CLK6P,FPLL_TL_FBP/DIFFIO_RX_T9P
IO_8A/CLK6N,FPLL_TL_FBN/DIFFIO_RX_T9N
IO_8A/CLK7P/DIFFIO_RX_T1P
IO_8A/CLK7N/DIFFIO_RX_T1N

5CSXFC6D6F31C6N

CLOCK_50 AF14
DRAM_ADDR7 AF15
GPIO0 W15
GPIO2 Y16

CLOCK2_50 AA16
HEX21 AB17
TD_CLK27 18 AC18
HEX13 AD17

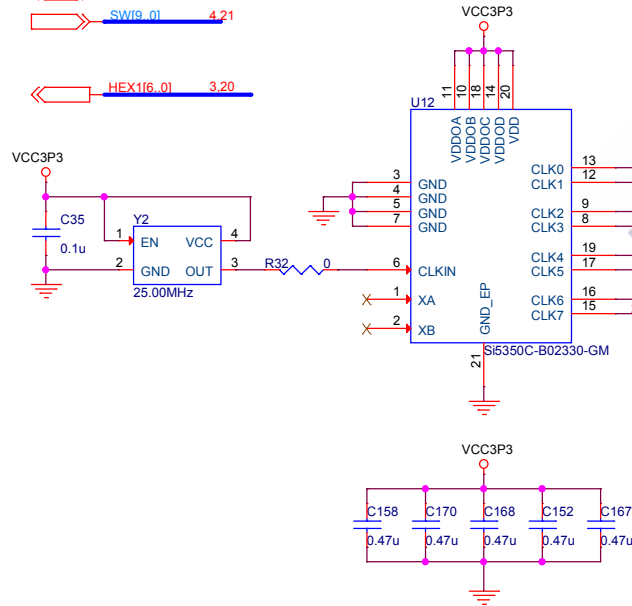
CLOCK3_50 Y26
SW1 Y27
HSMC_CLKIN_P1 AA26
HSMC_CLKIN_N1 AB27

CLOCK4_50 K14
HSMC_CLKIN0 14 J14
HSMC_CLKIN_P2 H15
HSMC_CLKIN_N2 G15

HEX216_01 3.20
DRAM_ADDR[12..0] 3.15

GPIO[35..0] 3.8,13
SW19_01 4.21

HEX116_01 3.20

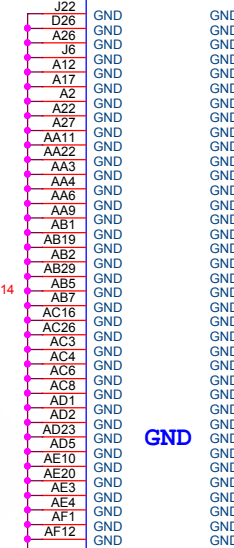


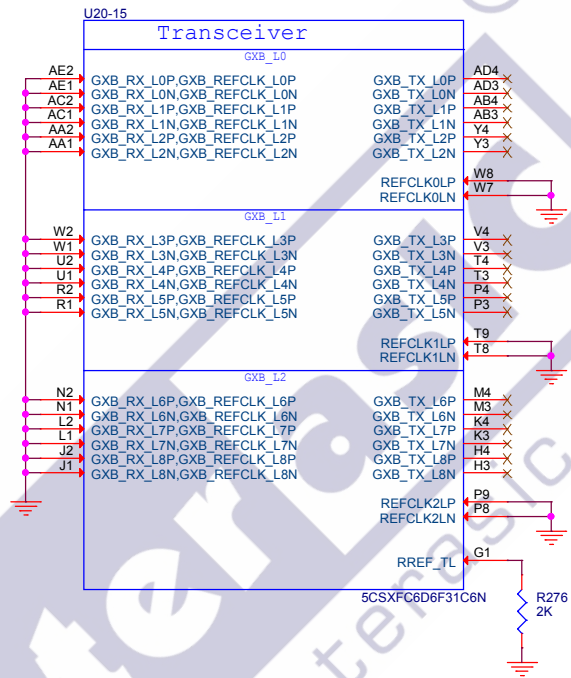
AH12 15 DRAM_CLK
AJ12 15 DRAM_BA1


AE29 HSMC_SDA
AD29 14 HSMC_CLKOUT0

A11 HSMC_CLKOUT_P2
A10 HSMC_CLKOUT_N2

U20-6

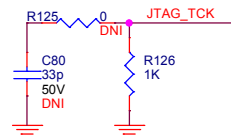




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Title		
DE10-Standard Board		
Size	Document Number	Rev
B	Transceiver	C
Date:	Thursday, December 13, 2018	Sheet 7 of 33

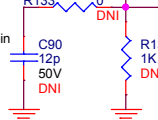
USB Blaster

FPGA TDI	12
JTAG TMS	12
JTAG TCK	12
FPGA TDO	12



Design Note:
Optional termination resistor
for DCLK

CAD Note:
Place near FPGA DCLK pin



JTAG_TCK	AC5
JTAG_TMS	V9
FPGA_TDO	AB9
FPGA_TDI	U8
EPCQ_DCLK	U7
EPCQ_AS_DATA0	AE6
EPCQ_AS_DATA1	AE5
EPCQ_AS_DATA2	AE8
EPCQ_AS_DATA3	AC7
EPCQ_NCS0	AB8
GPIO24	AE9
GPIO26	AE12
GPIO28	AD9
GPIO30	AD11
GPIO22	AF10
GPIO29	AD10
GPIO25	AE11
GPIO32	AC9
GPIO8	AH4
GPIO23	AE7
GPIO12	AG3
GPIO27	AD7

Configuration

Bank 3A VCCIO = 3.3V

TCK
TMS
TDO
TDI
DCLK

Bank 5A VCCIO = 3.3V

IO_5A/INIT_DONE/DIFFIO_RX_R2P
IO_5A/CRC_ERROR/DIFFIO_RX_R2N
IO_5A/DEV_OE/DIFFIO_TX_R5P
IO_5A/NCEO/DIFFIO_TX_R3P/DQ1R
IO_5A/DEV_CLRN/DIFFIO_TX_R5N/DQ1R

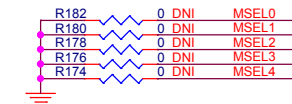
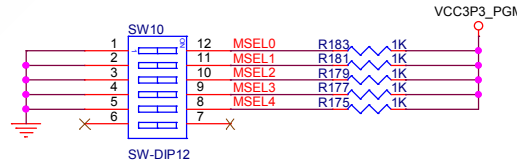
Bank 9A

CONF_DONE
NSTATUS
NCONFIG
NCE

AS_DATA0/ASDO/DATA0
AS_DATA1/DATA1
AS_DATA2/DATA2
AS_DATA3/DATA3
NCS0/DATA4
IO_3A/DATA5/DIFFIO_TX_B2N
IO_3A/DATA6/DIFFIO_RX_B1N/DQ1B
IO_3A/DATA7/DIFFIO_TX_B2P/DQ1B
IO_3A/DATA8/DIFFIO_RX_B1P/DQ1B
IO_3A/DATA9/DIFFIO_TX_B4N/DQ1B
IO_3A/DATA10/DIFFIO_RX_B3N/DQSN1B
IO_3A/DATA11/DIFFIO_TX_B4P
IO_3A/DATA12/DIFFIO_RX_B3P/DQ51B
IO_3A/DATA13/DIFFIO_TX_B6N/DQ1B
IO_3A/DATA14/DIFFIO_RX_B5N/DQ1B
IO_3A/DATA15/DIFFIO_TX_B6P/DQ1B
IO_3A/CLKUSR/DIFFIO_RX_B5P/DQ1B

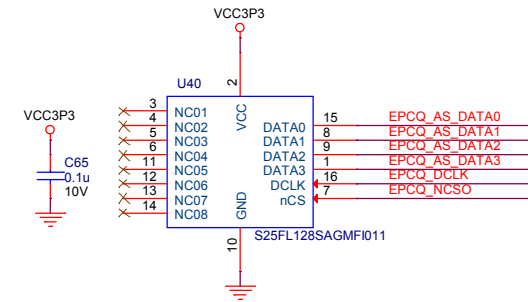
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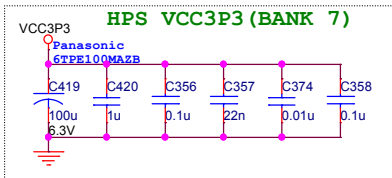
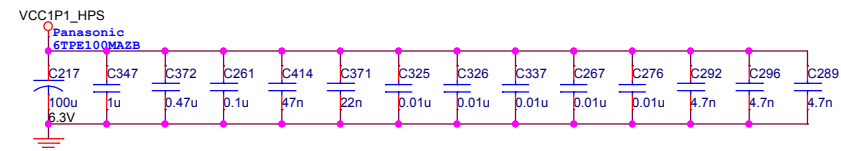
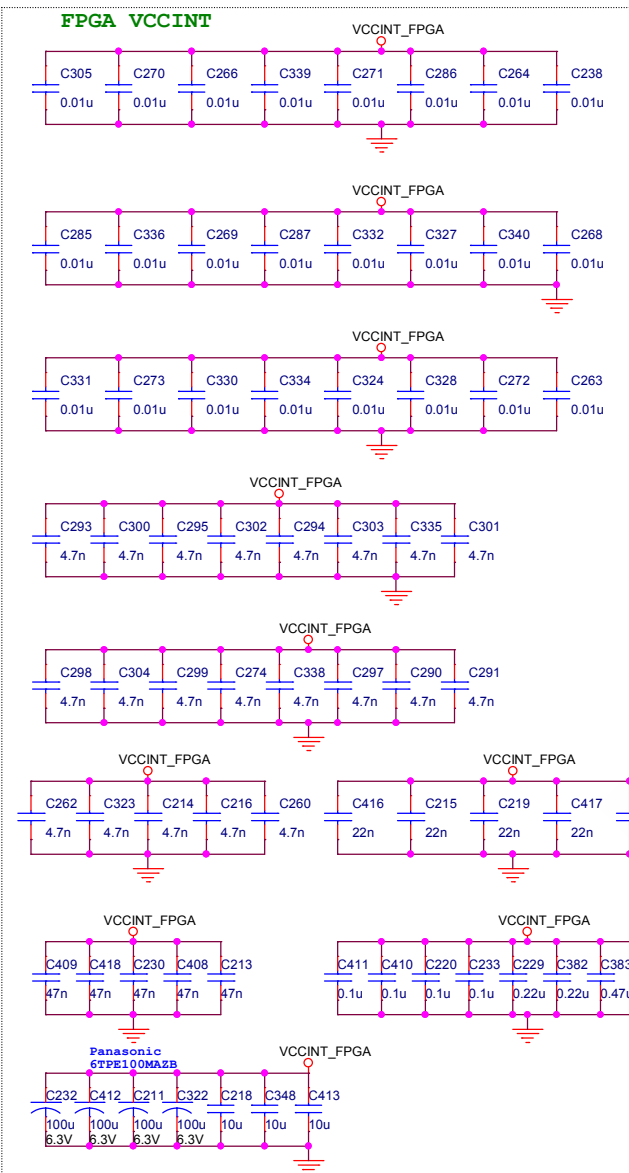
Fix MSEL[4:0]=10010 in AS Fast Mode



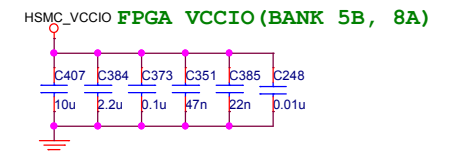
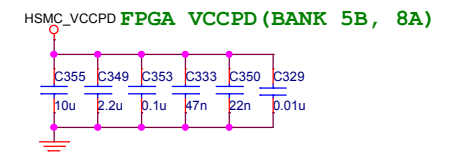
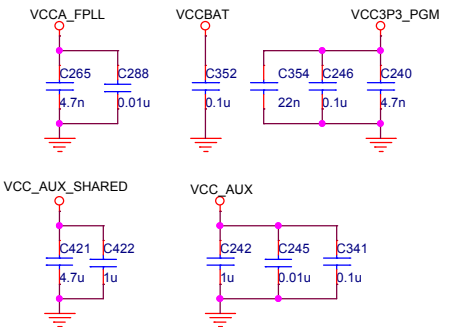
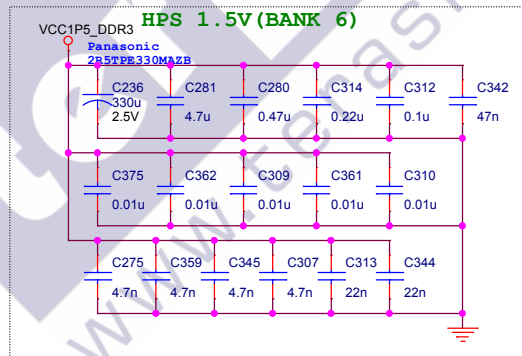
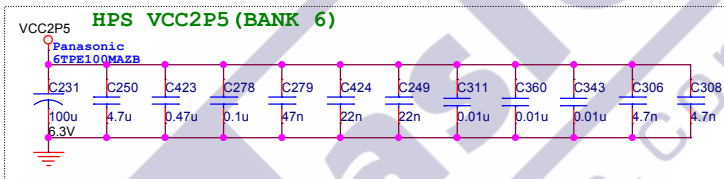
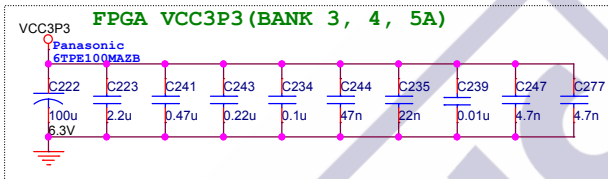
TD_DATA[7..0] 4,18


GPIO[35..0] 3,6,13

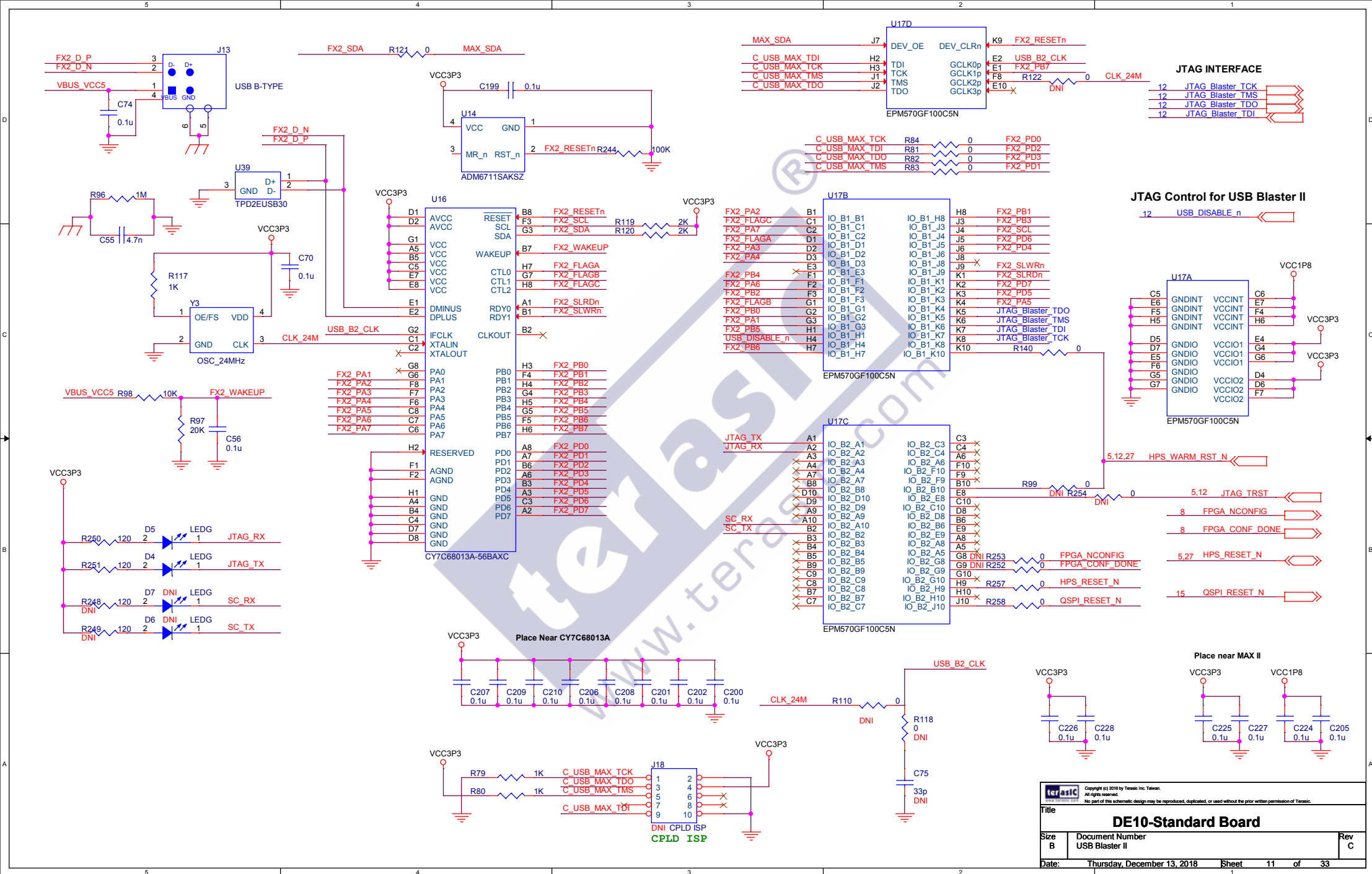


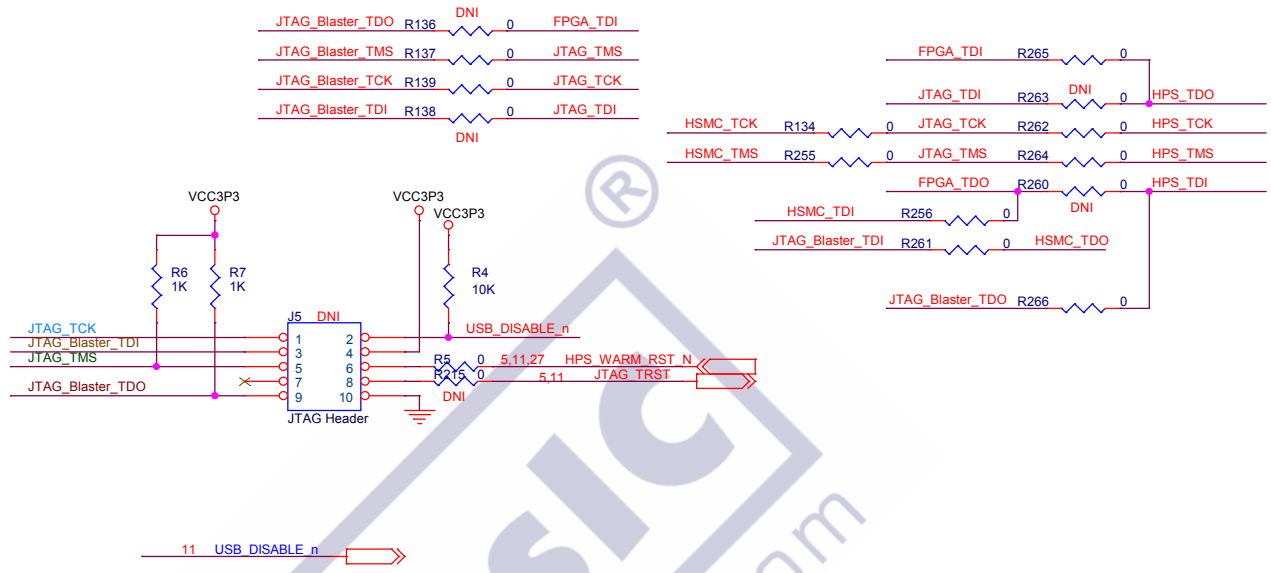
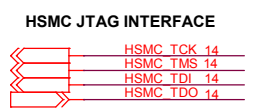
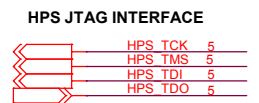
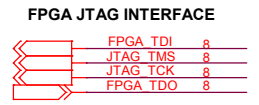
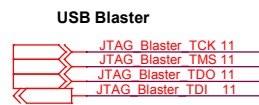


Place C394 close to J20/G23 pin

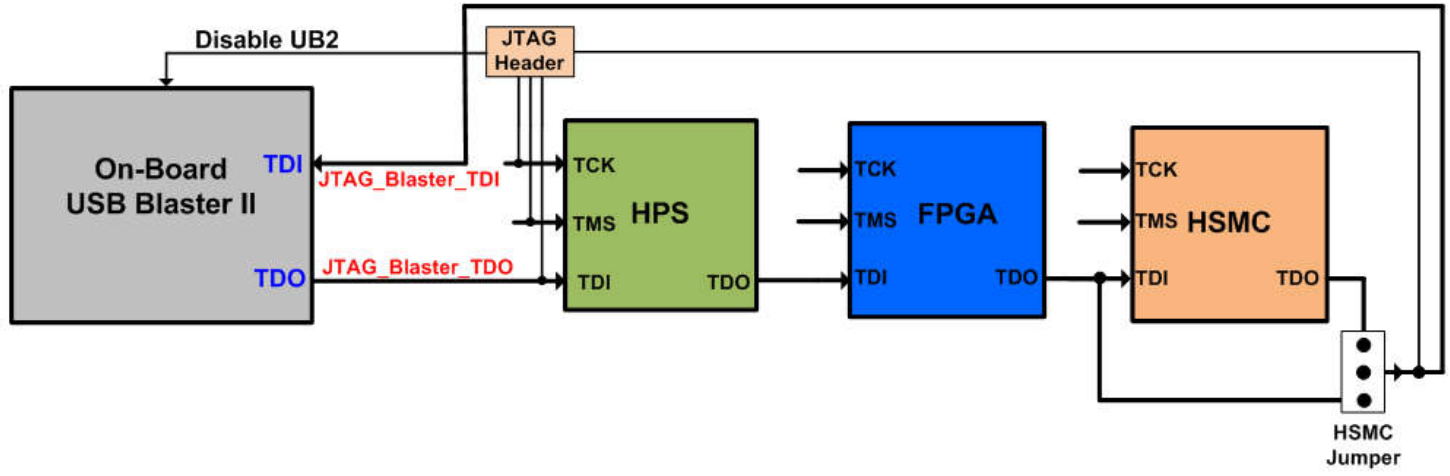


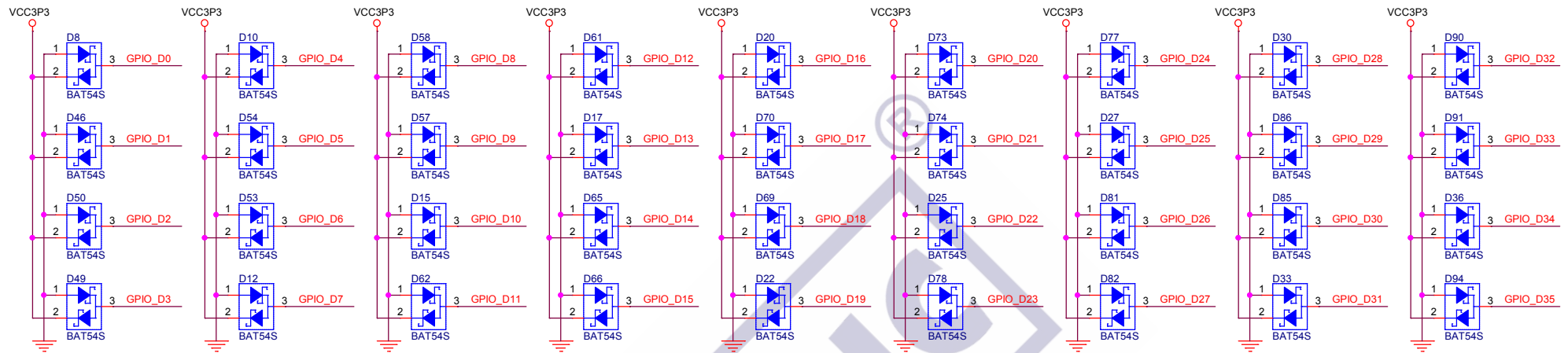
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Size B		Document Number	
Date:		Thursday, December 13, 2018	
		Sheet	9 of 33
		Rev	C





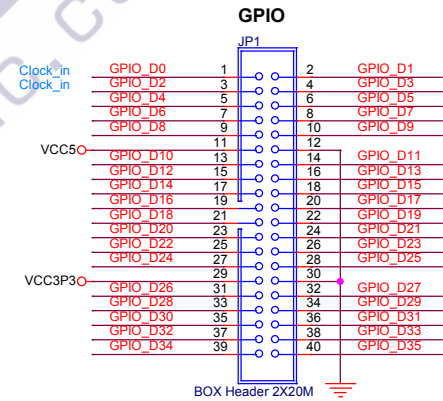
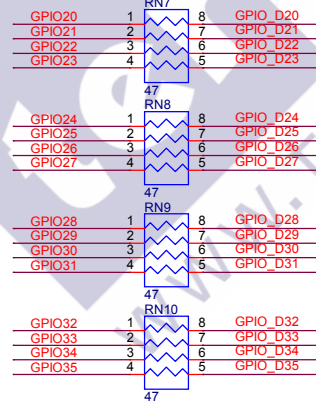
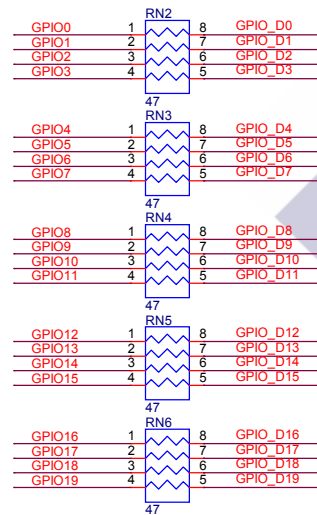
JTAG Chain

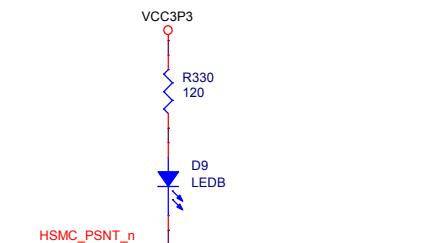
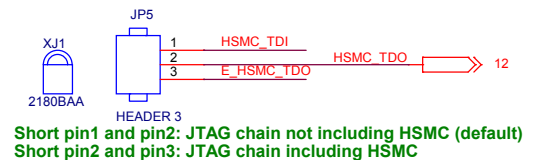
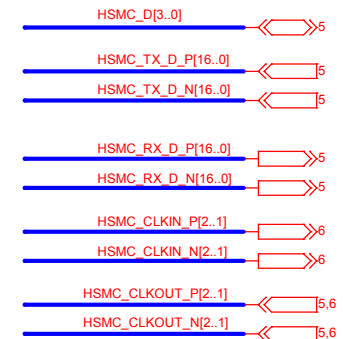


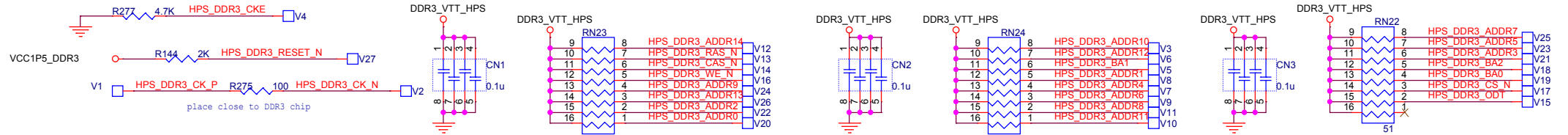


GPIO 0

GPIO[35..0] 3,6,8

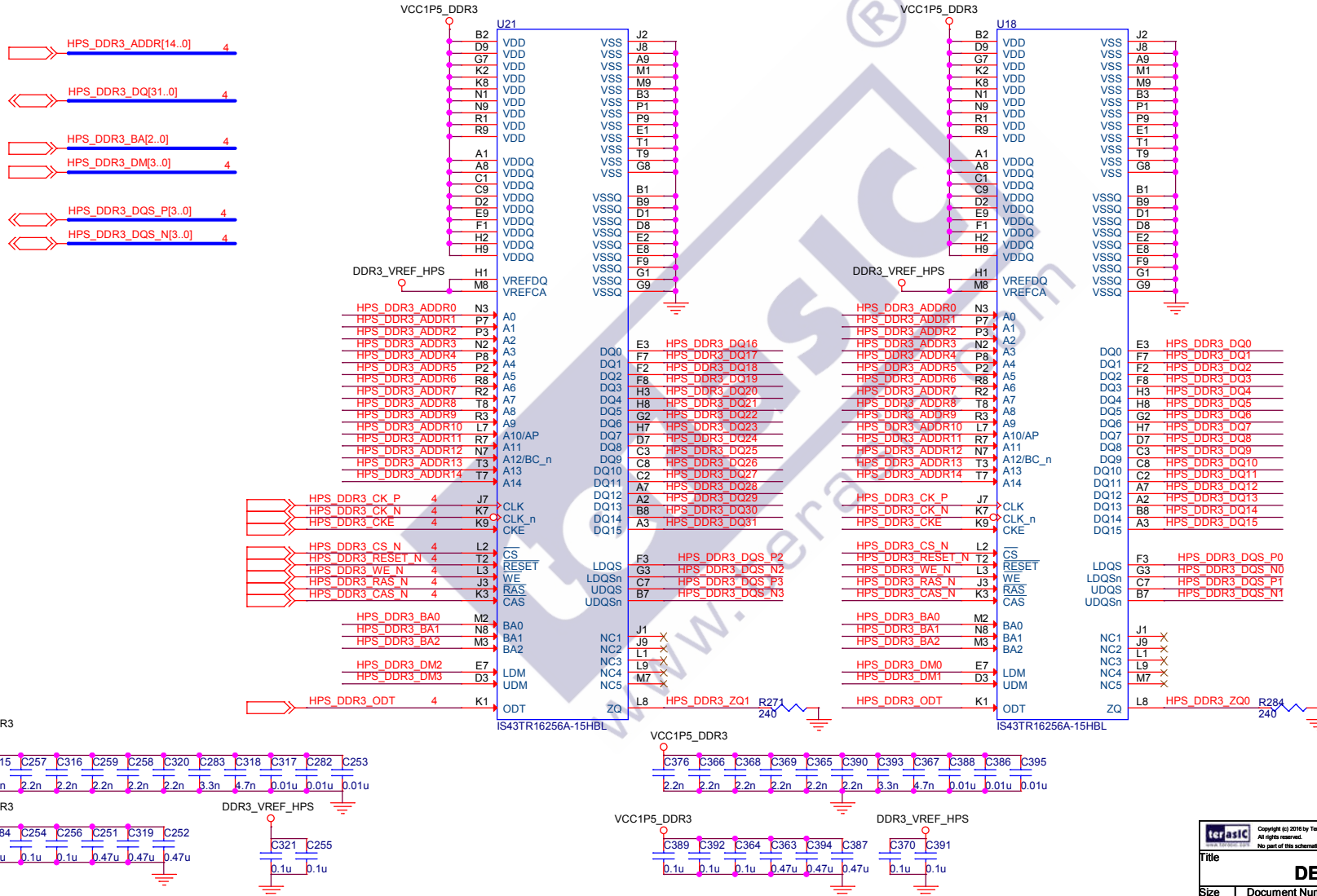


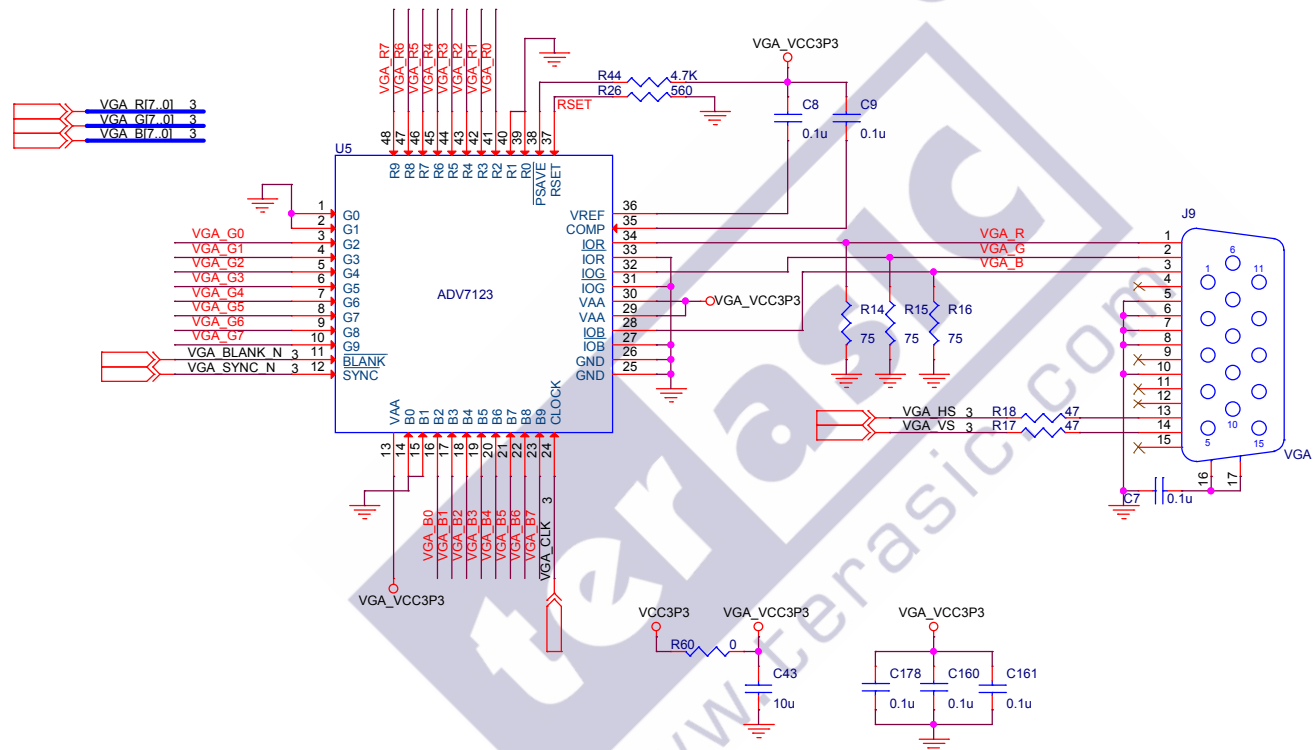


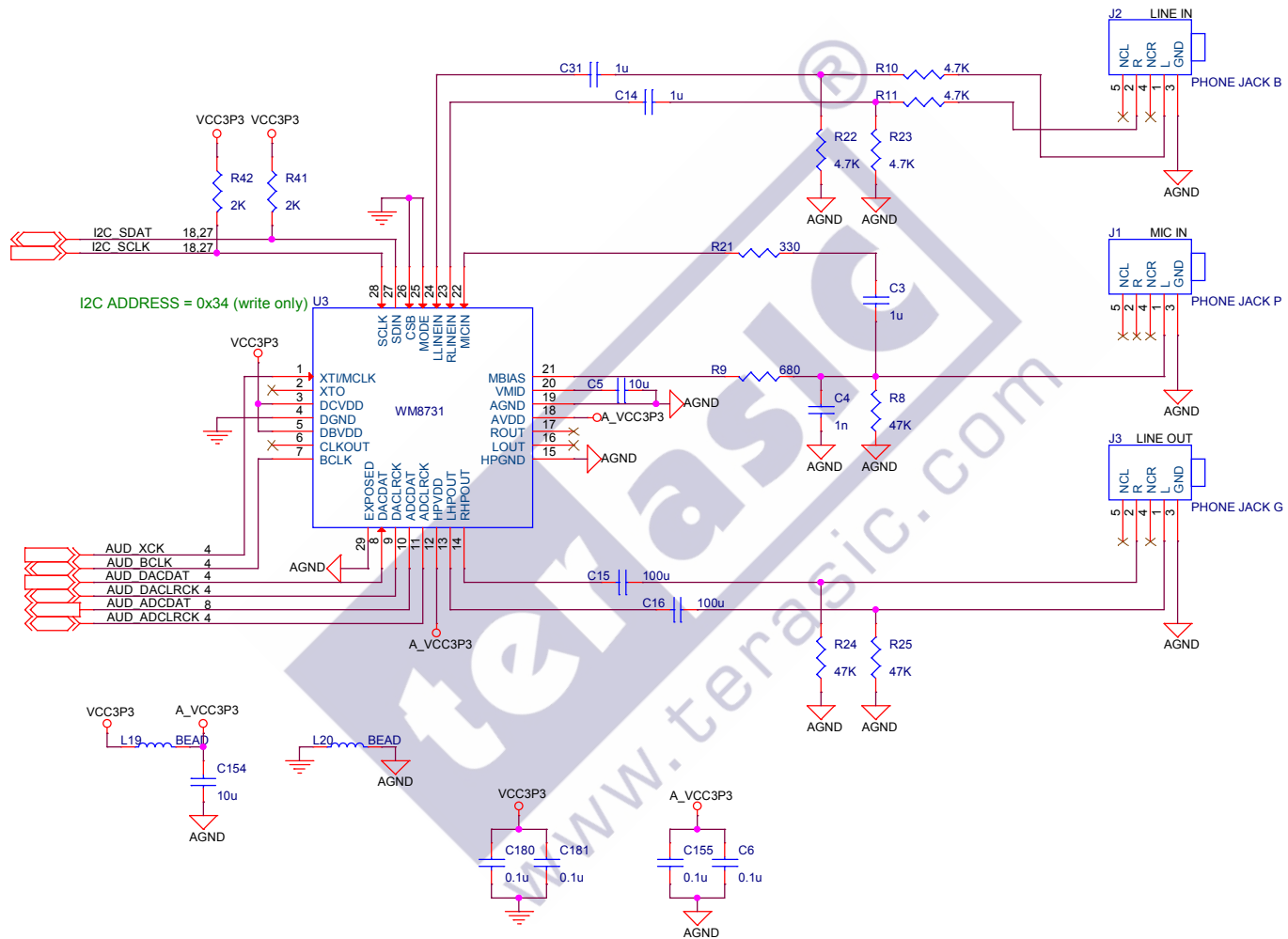


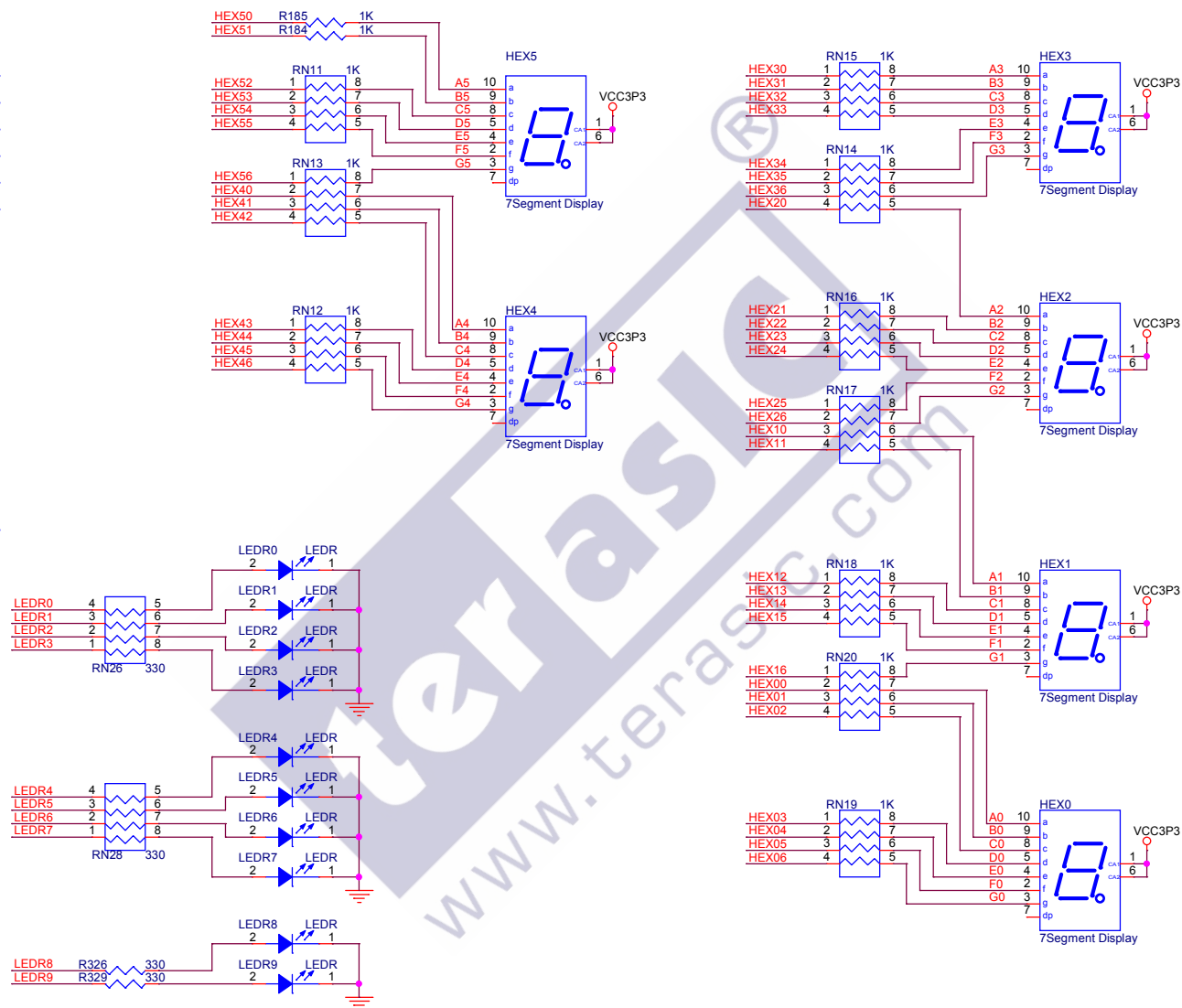
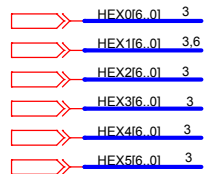
Note: you can only swap the DQ signals within x8 group (e.g. 0-7,8-15,16-23,24-31) on the DDR3 chips

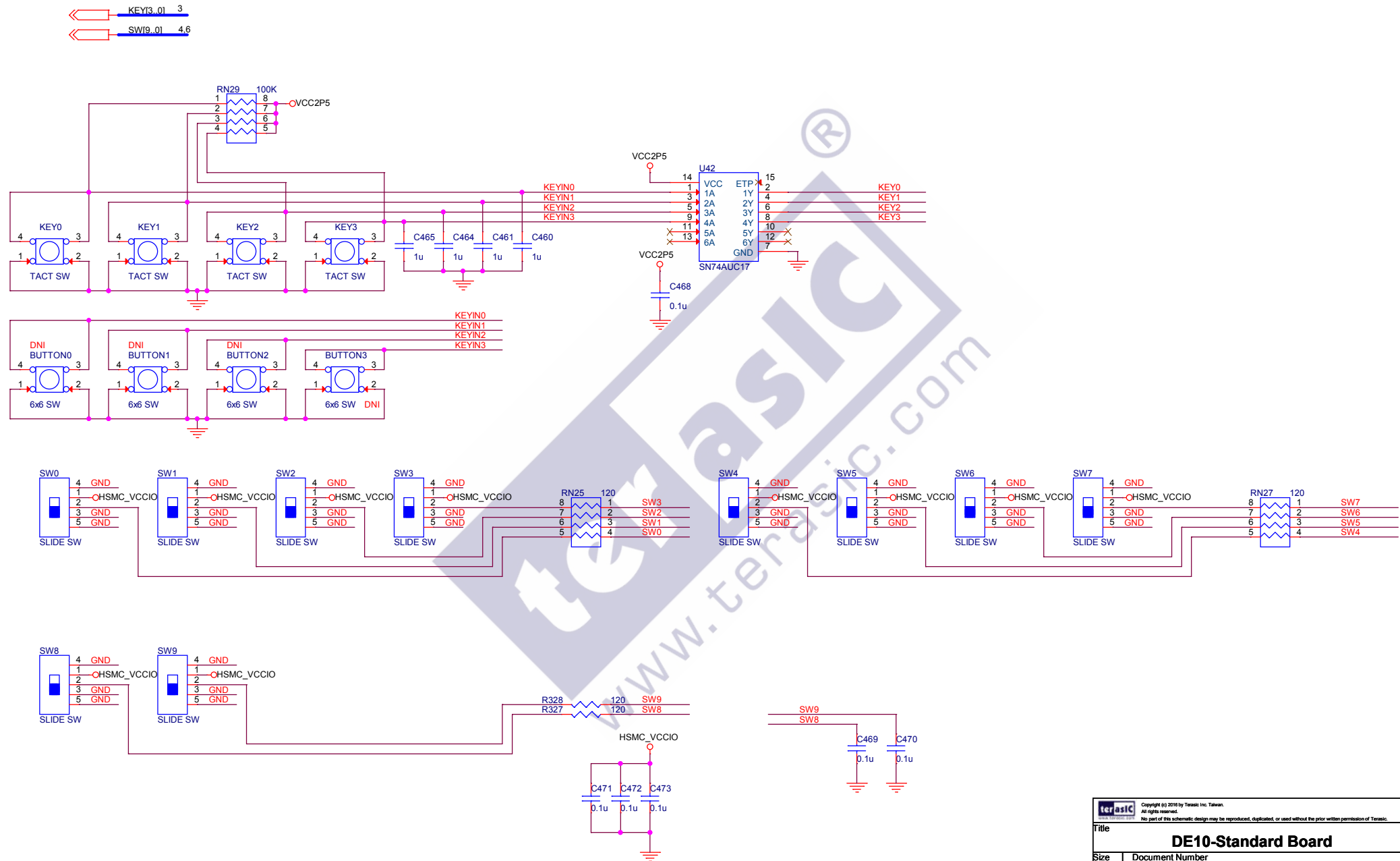
Note: you can swap the signals on the OCT resistor array(include NC pin)

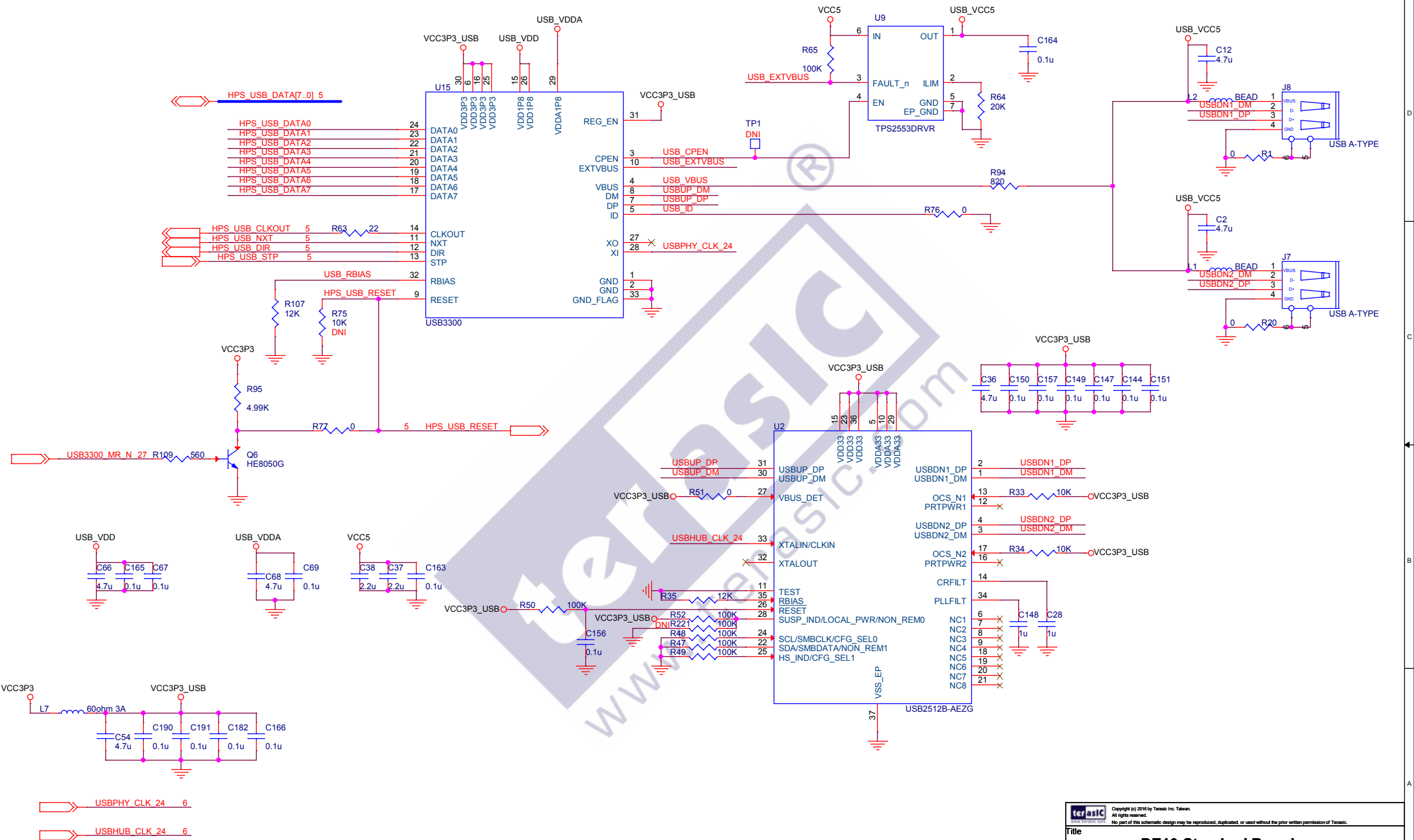


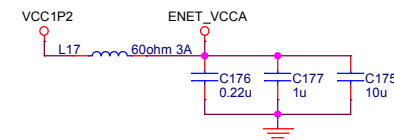
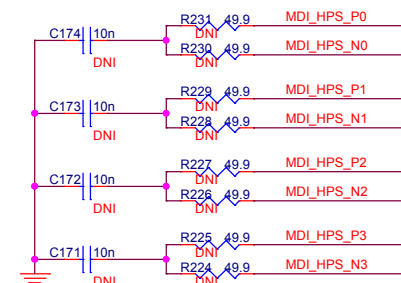
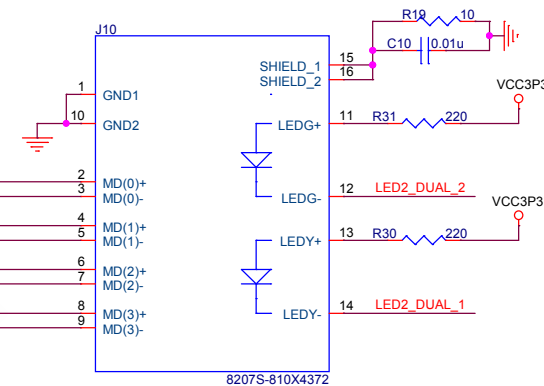
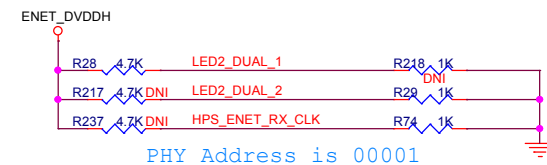
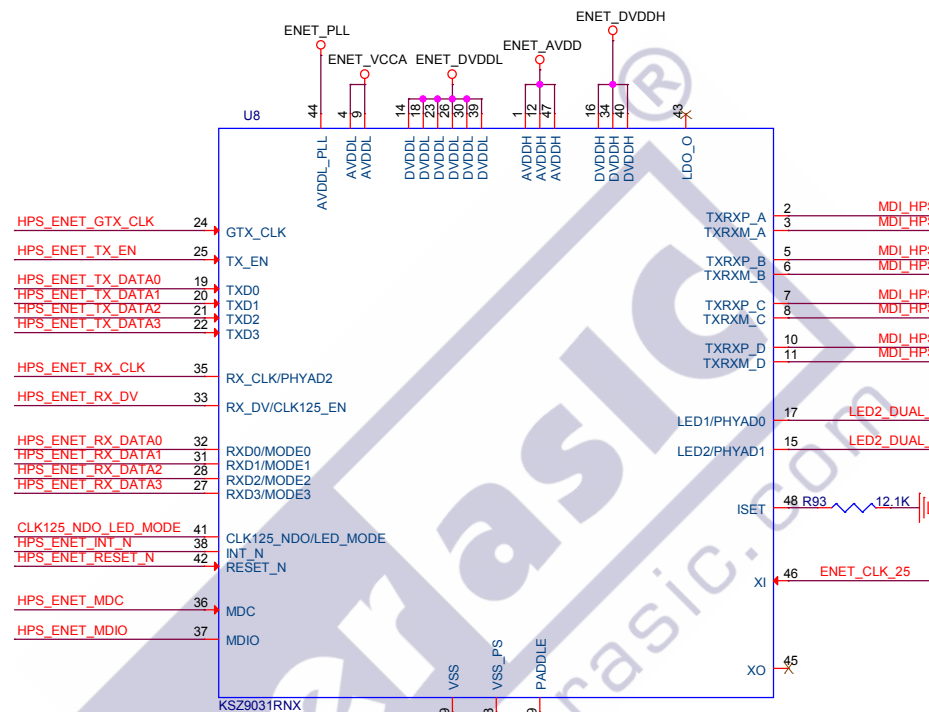
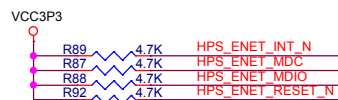
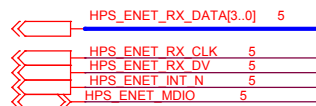










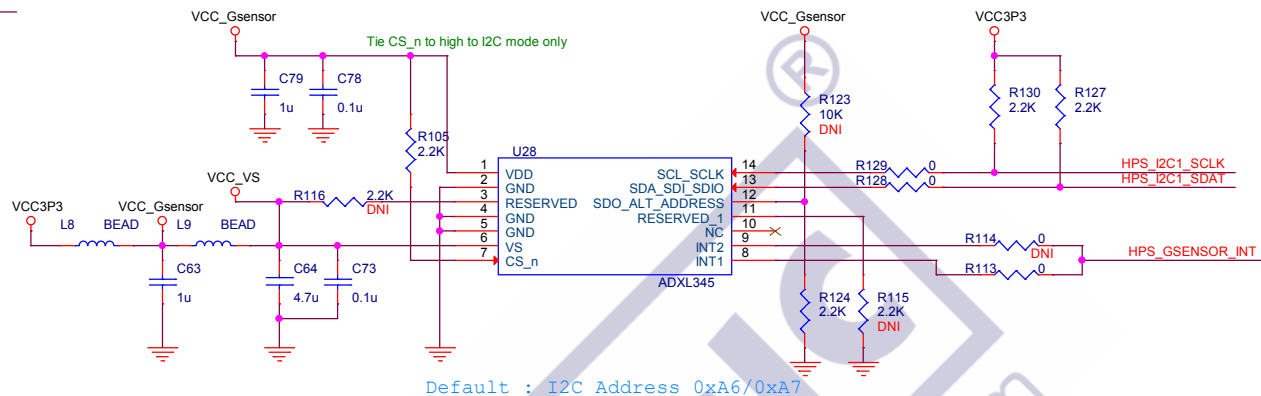


HPS_I2C1_SDAT 5,27

HPS_I2C1_SCLK 5,27

HPS_GSENSOR_INT 5

Digital Accelerometer



LTC 2x7 Connector

HPS_I2C2_SCLK 5

HPS_I2C2_SDAT 5

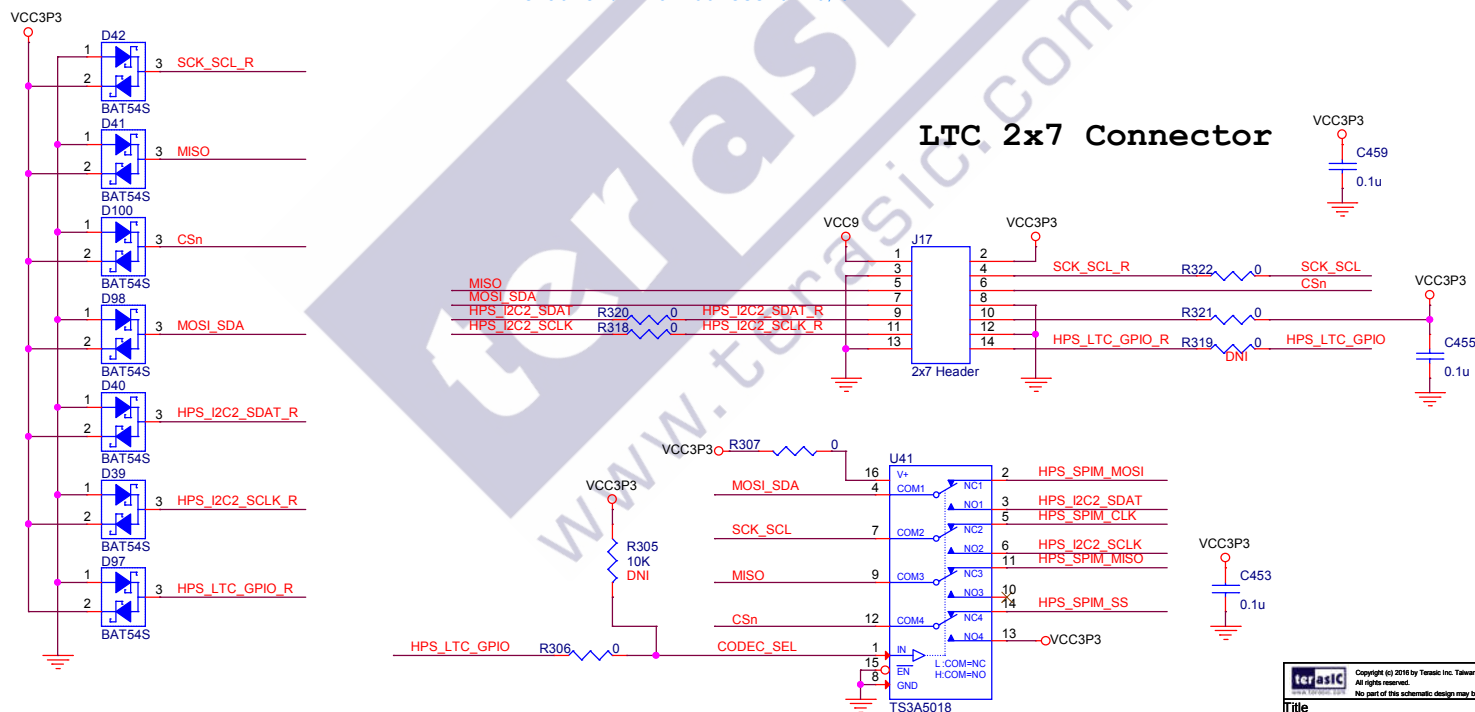
HPS_SPIM_MOSI 5

HPS_SPIM_CLK 5

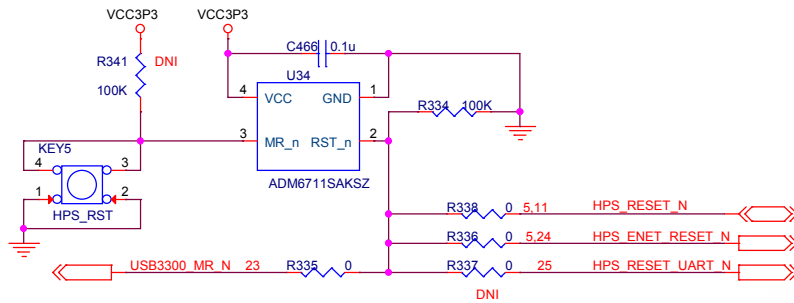
HPS_SPIM_SS 5

HPS_SPIM_MISO 5

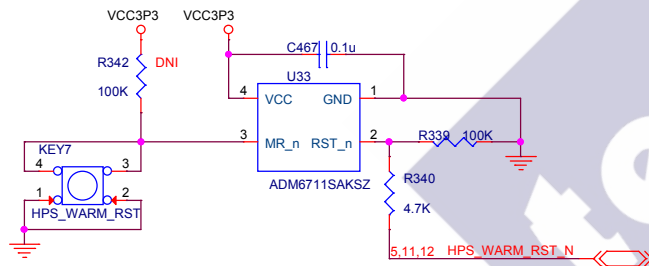
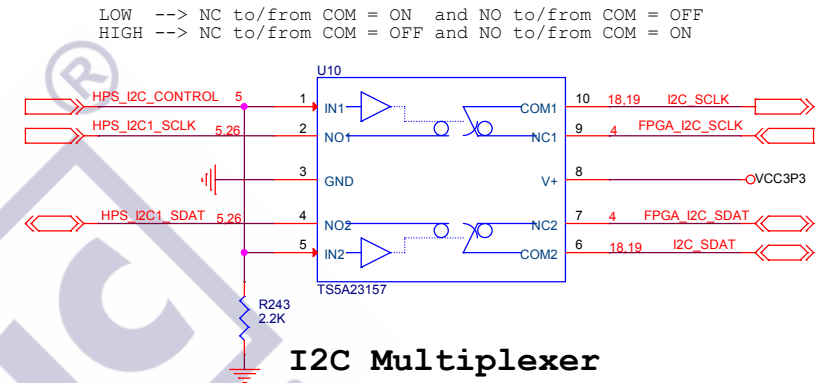
HPS_LTC_GPIO 5



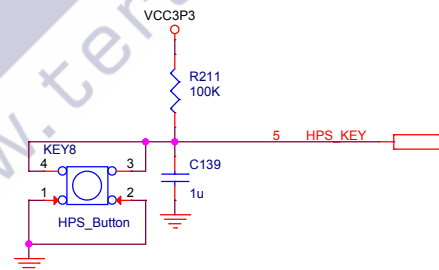
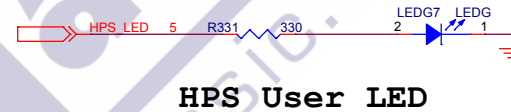
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Title		
DE10-Standard Board		
Size	Document Number	Rev
B	Accelerometer, LTC Connector	C
Date:	Thursday, December 13, 2018	Sheet 26 of 33



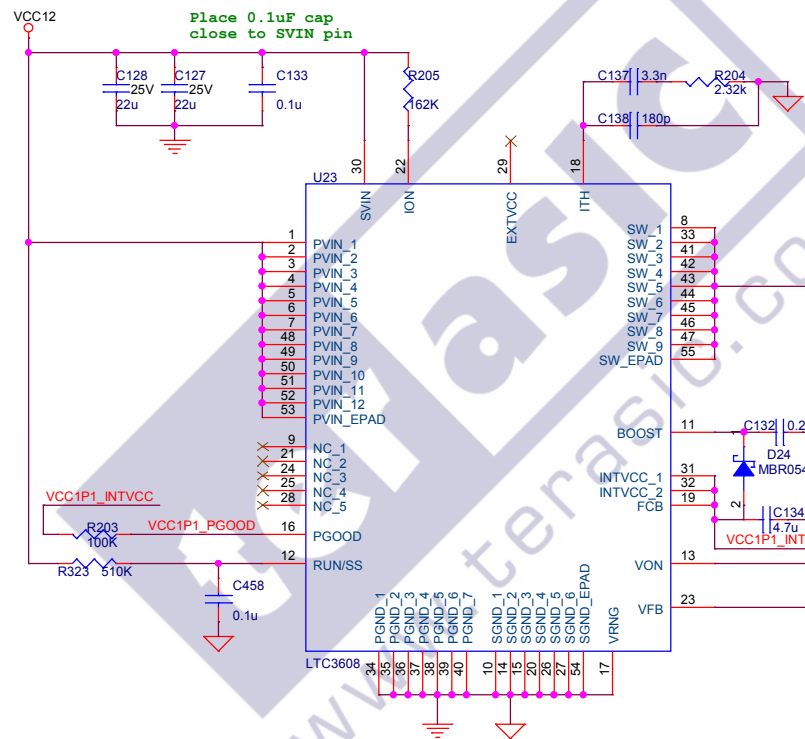
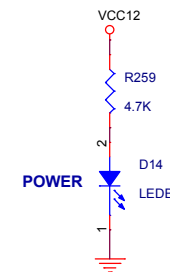
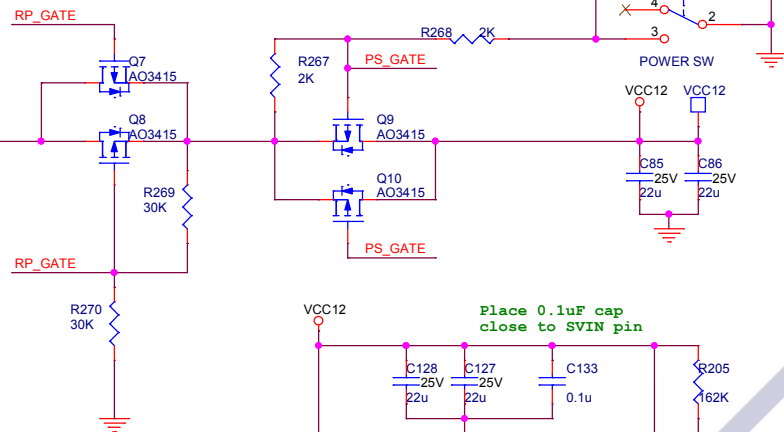
HPS Cold Reset



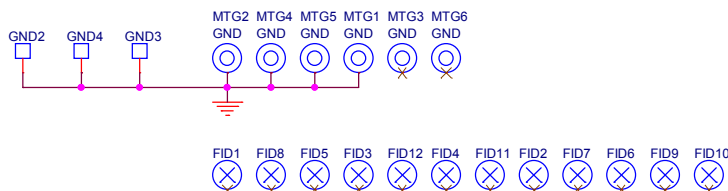
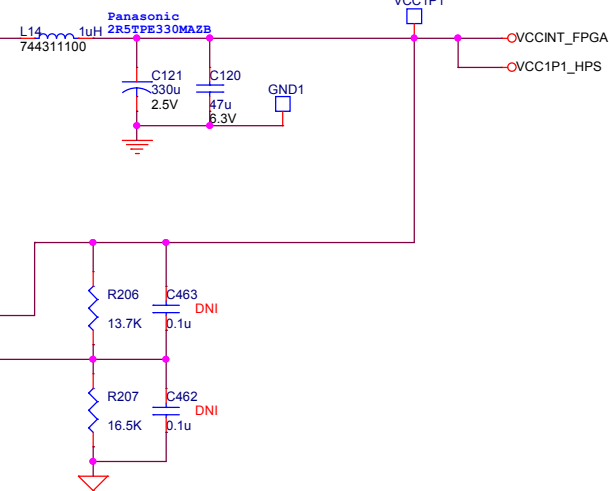
HPS Warm Reset



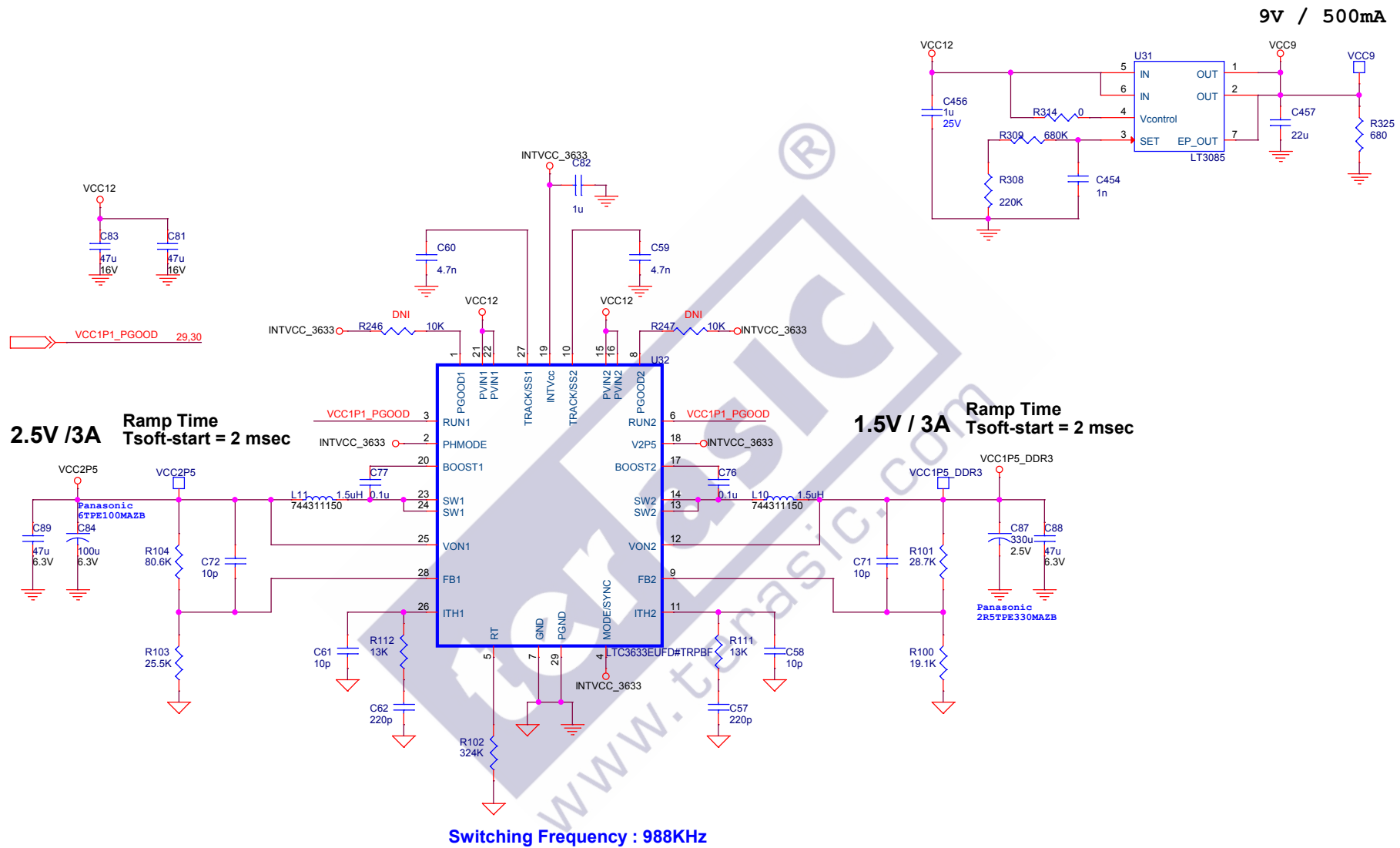
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Title		
DE10-Standard Board		
Size	Document Number	Rev
B	I2C Multiplexer, HPS BUTTON, HPS LED	C
Date:	Thursday, December 13, 2018	Sheet 27 of 33



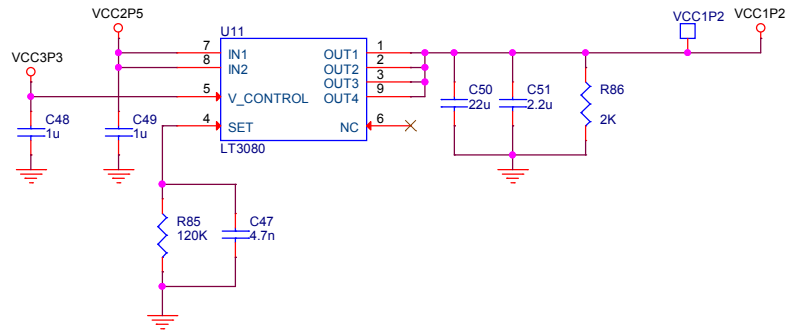
1.1V / 8A
Ramp Time = 190 usec
Switching Frequency : 617KHz



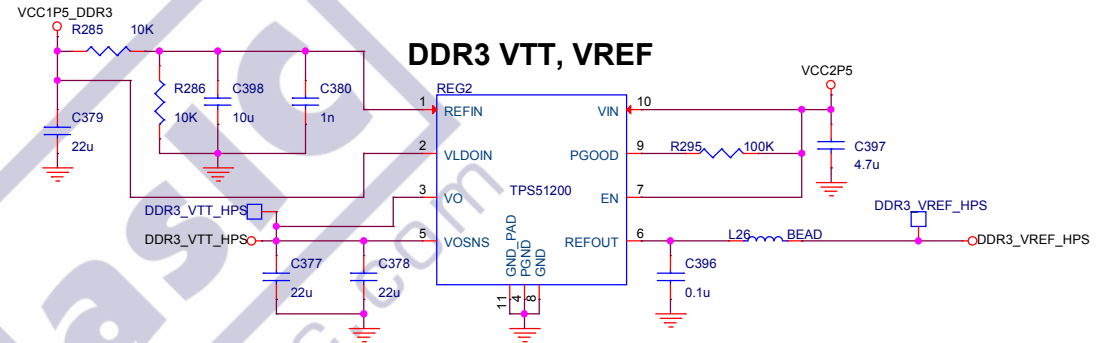
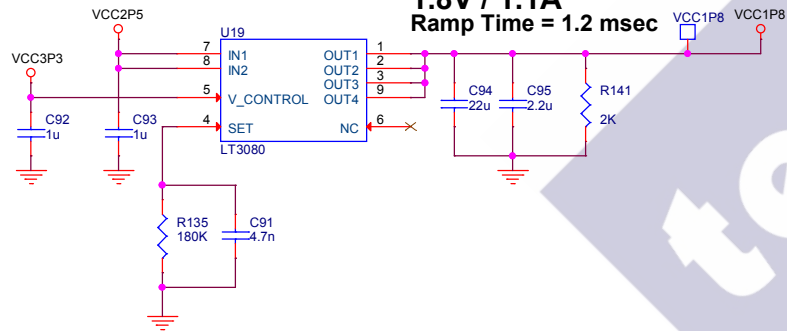
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Title		
DE10-Standard Board		
Size	Document Number	Rev
B	Power - 1.1V	C
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1.2V / 1.1A
Ramp Time = 0.8msec



1.8V / 1.1A
Ramp Time = 1.2 msec



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Size		Document Number	
B		Power - 1.2V, 1.8V, DDR3 VREF, DDR3 VTT	
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