

ALTERA CYCLONE II EP2C70 Development & Education BOARD

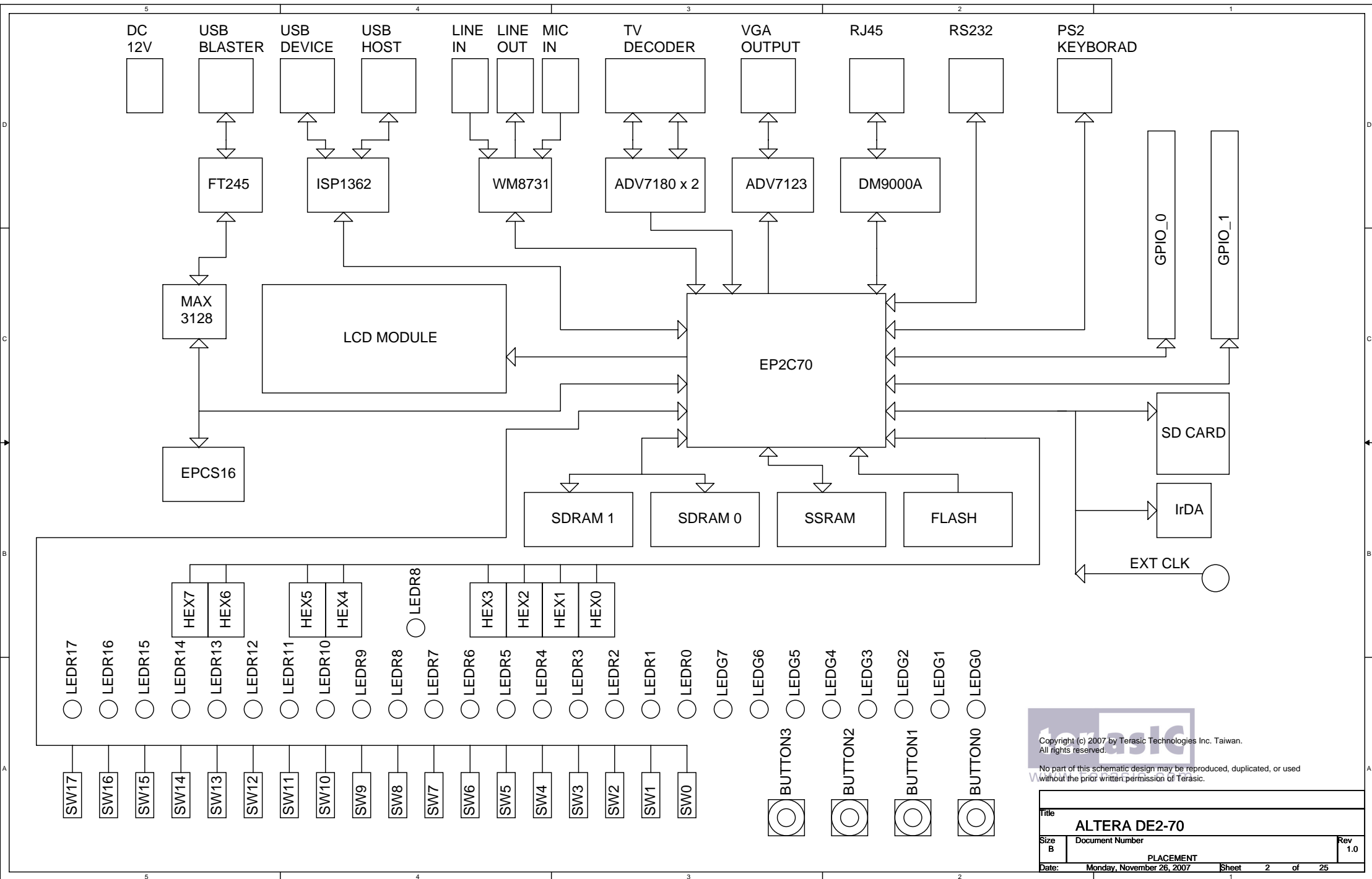
SCHEMATIC	CONTENT	PAGE
TOP	COVER PAGE , TOP	01 ~ 03
MEMORY	SDRAM , SSRAM , FLASH , SD CARD	04 ~ 06
DISPLAY	LCD , LED , 7SEGMENT	07 ~ 08
IN/OUT	CLOCK, IrDA, PS2 , RS232 , BUTTON , SWITCH , CONNECTOR	09 ~ 13
ETHERNET	DM9000A	14 ~ 14
VIDEO	ADV7123, ADV7180	15 ~ 16
AUDIO	WM8731	17 ~ 17
USB DEVICE	ISP1362	18 ~ 18
FPGA	Cyclone II EP2C70 BANK1..BANK8 , POWER , CONFIG	19 ~ 23
POWER	POWER 1.2V, 1.8V, 3.3V, 5V	24 ~ 24
USB BLASTER	USB BLASTER	25 ~ 25

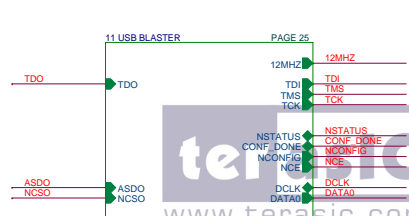
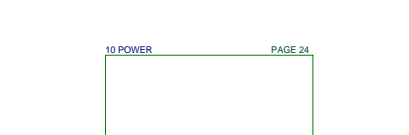
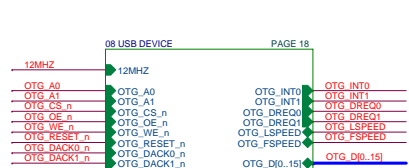
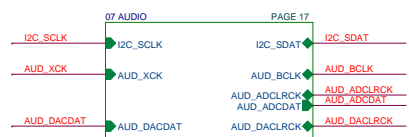
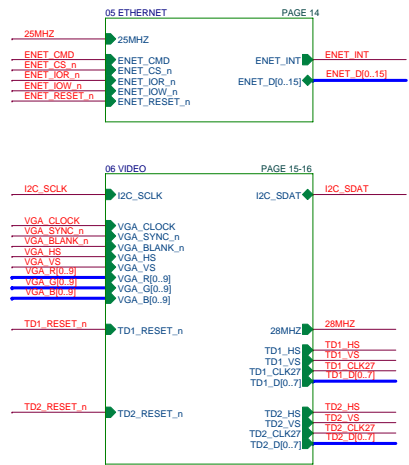
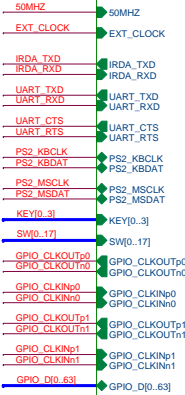
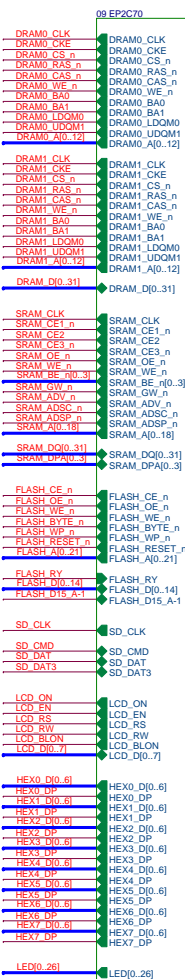
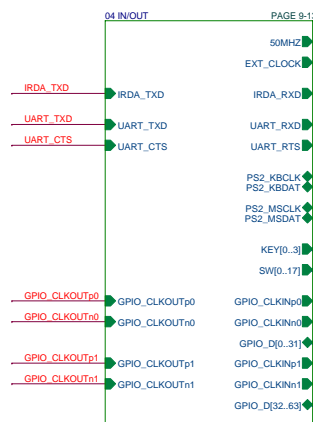
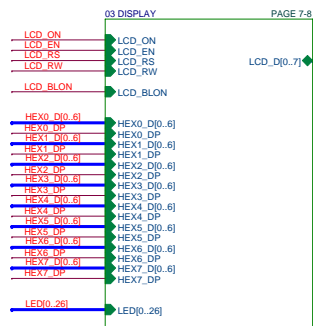
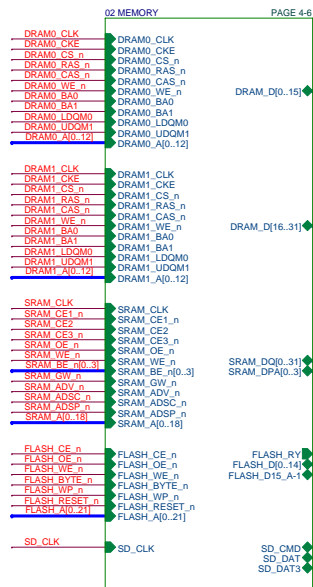


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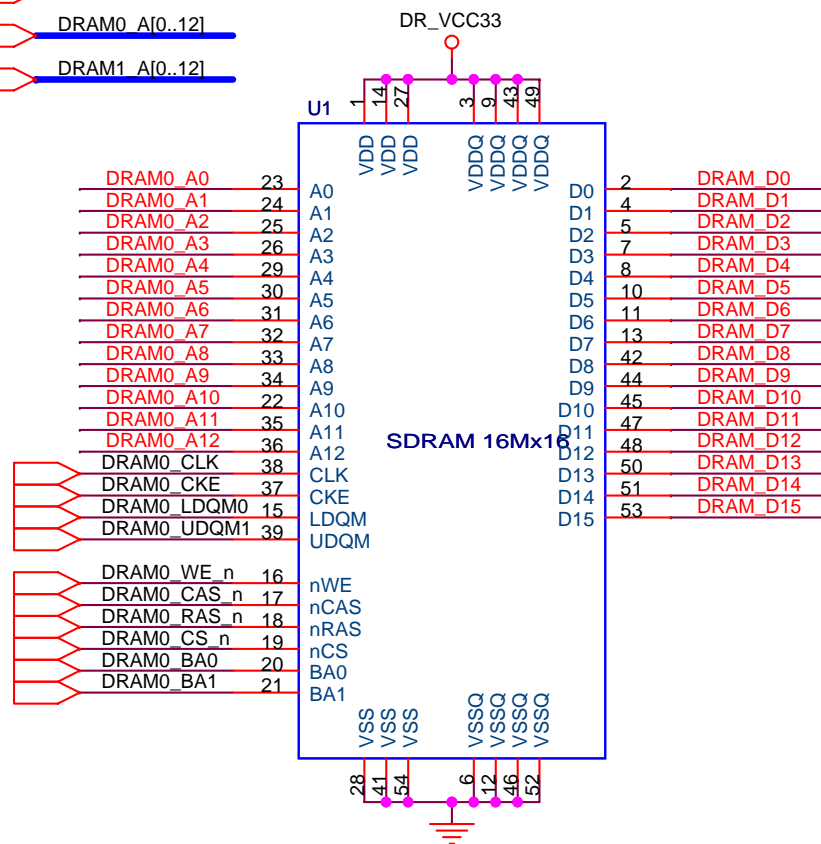
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Title		
ALTERA DE2-70		
Size	Document Number	Rev
B	COVER PAGE	1.0
Date:	Monday, November 26, 2007	Sheet 1 of 25

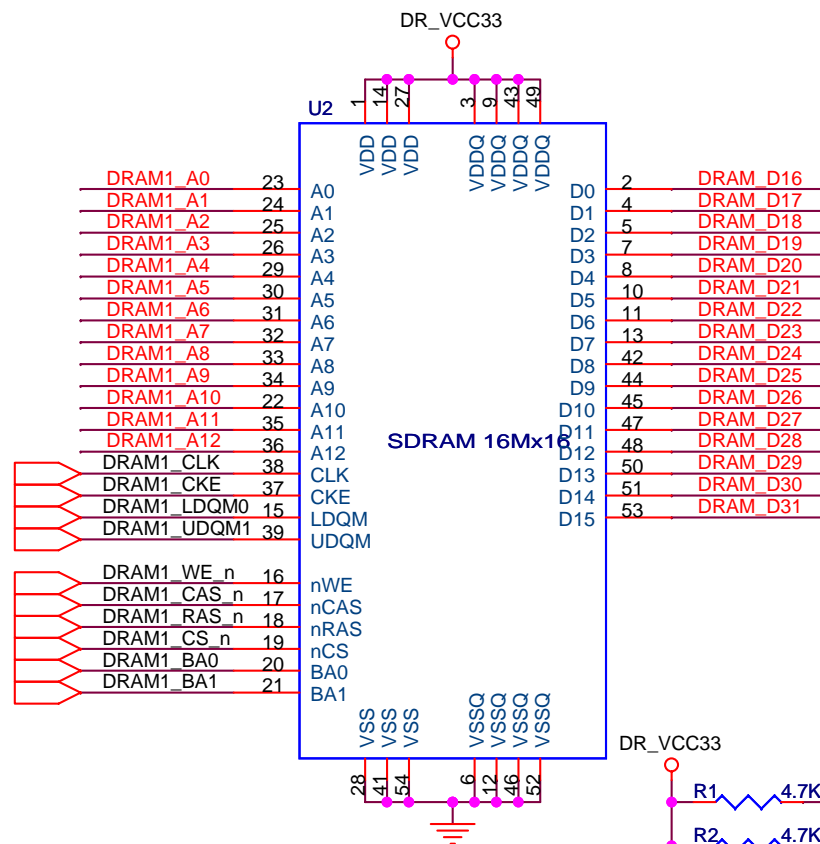




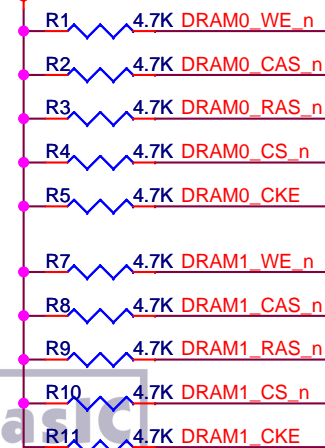
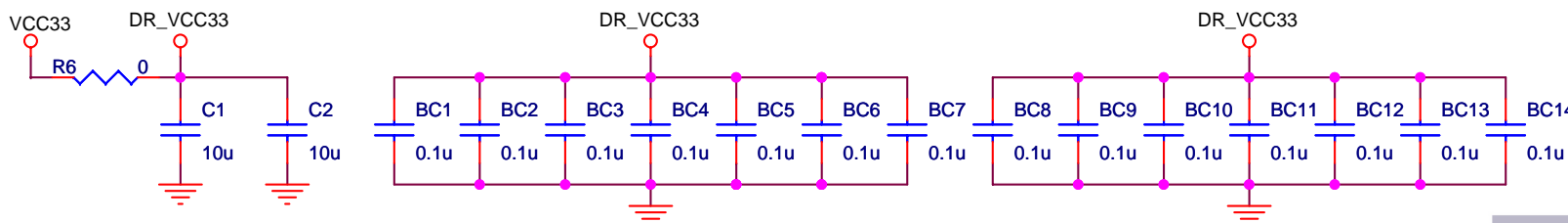
DRAM D[0..31]
 DRAM0 A[0..12]
 DRAM1 A[0..12]



SDRAM0



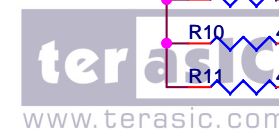
SDRAM1



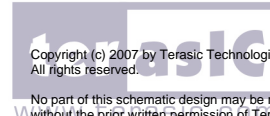
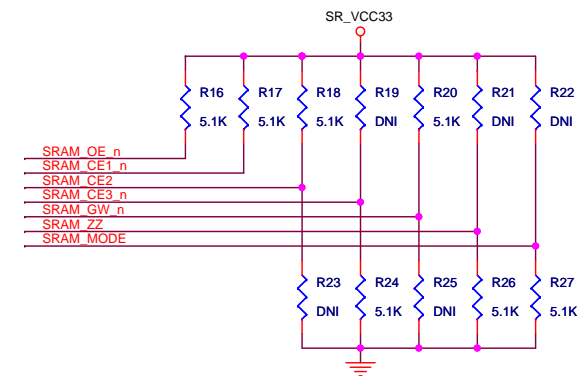
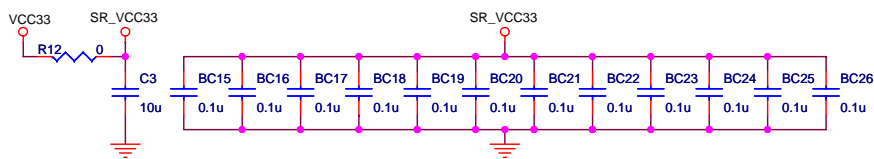
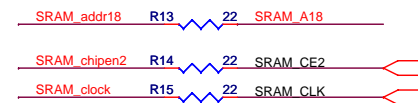
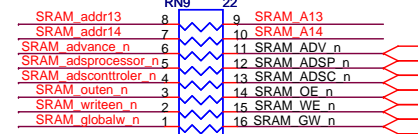
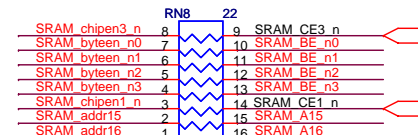
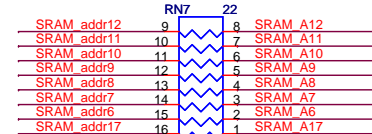
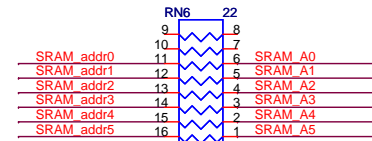
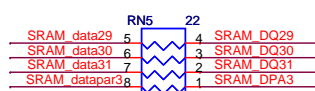
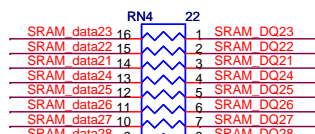
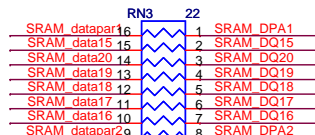
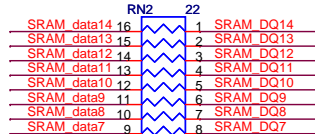
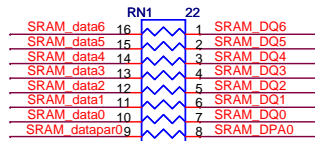
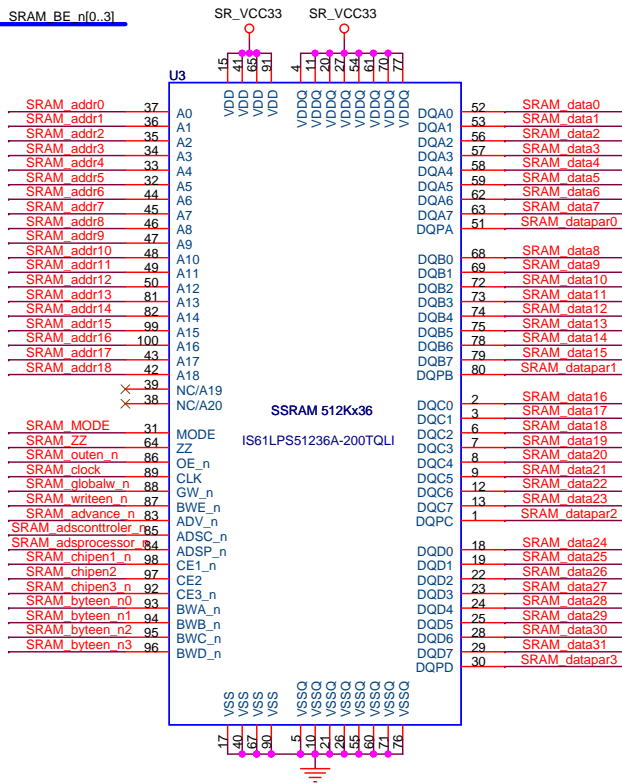
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Title		
ALTERA DE2-70		
Size A	Document Number SDRAM	Rev 1.0
Date:	Monday, November 26, 2007	Sheet 4 of 25



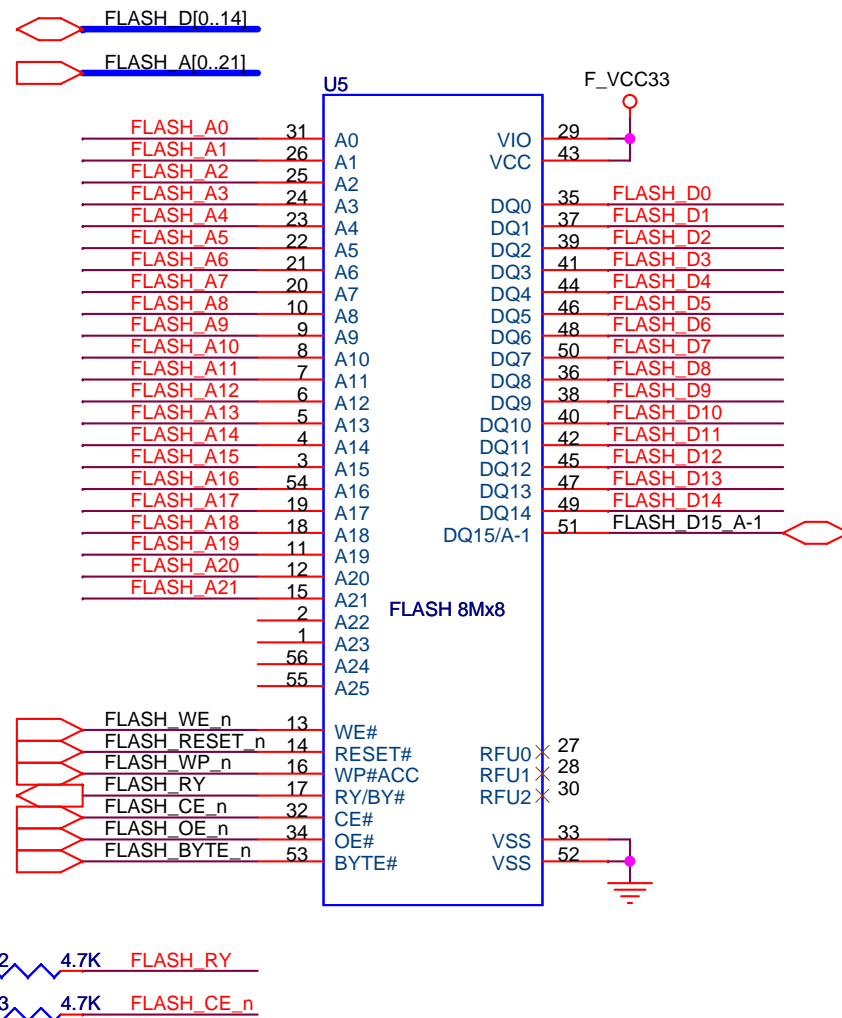
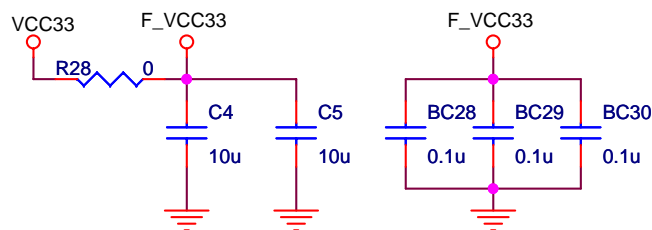
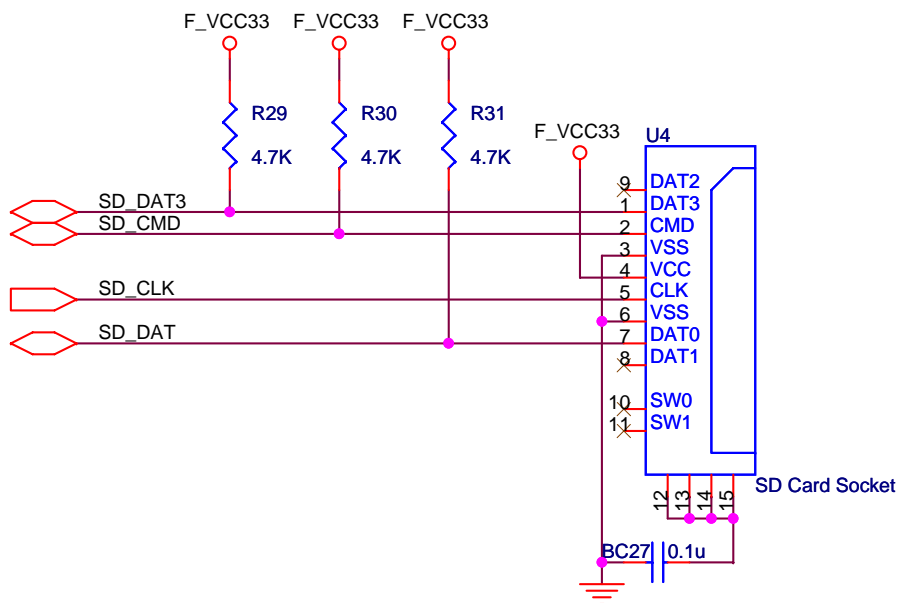
SRAM DQ[0..31]
SRAM DPA[0..3]
SRAM A[0..18]
SRAM BE_n[0..3]



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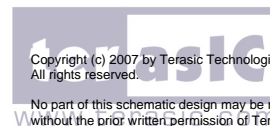
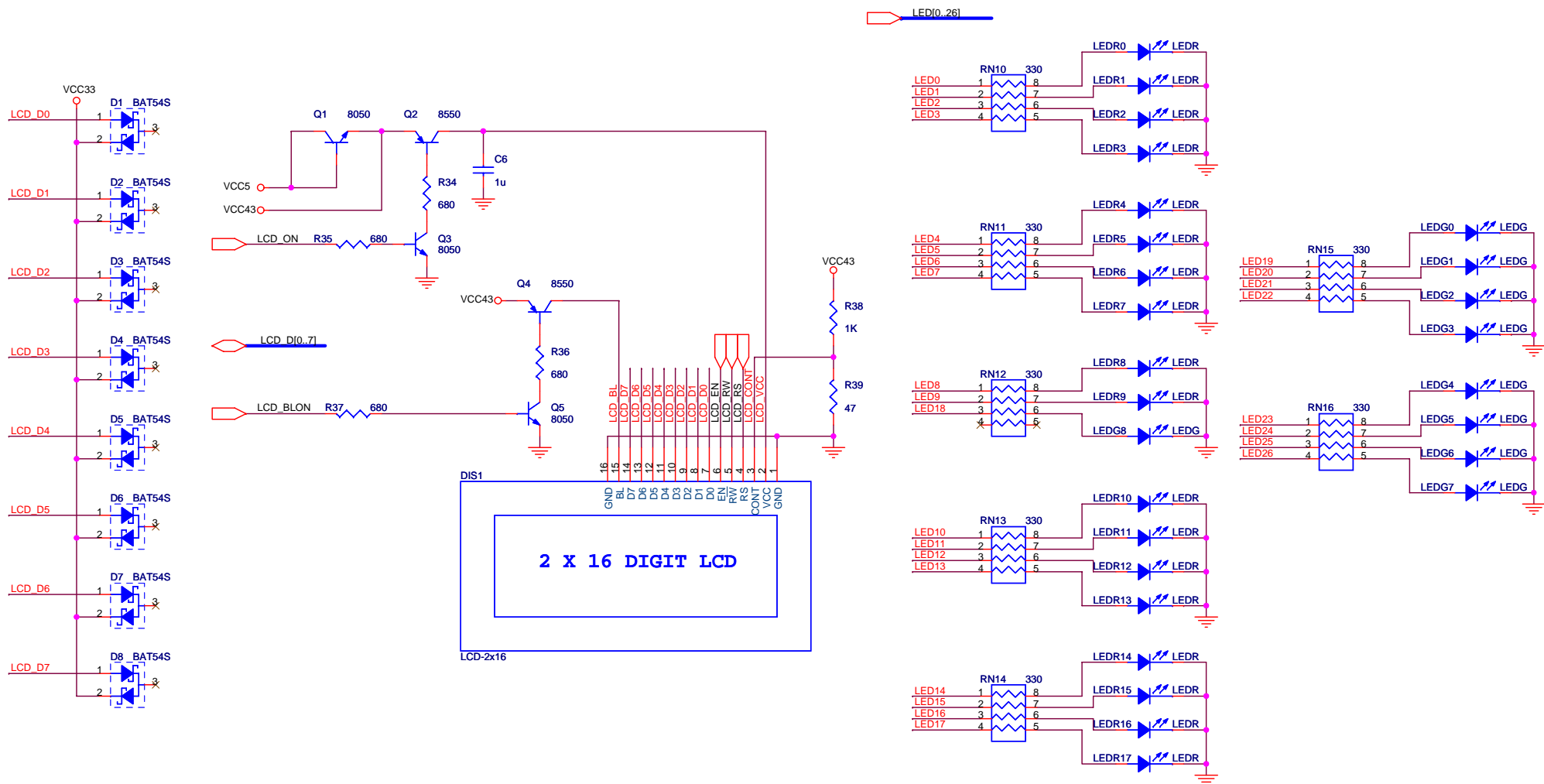
Title		
ALTERA DE2-70		
Size	Document Number	Rev
B	SSRAM	1.0
Date:	Monday, November 26, 2007	Sheet 5 of 25



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Title		
ALTERA DE2-70		
Size A	Document Number FLASH and SD Card	Rev 1.0
Date:	Monday, November 26, 2007	Sheet 6 of 25

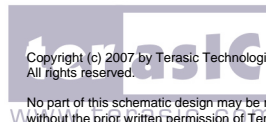
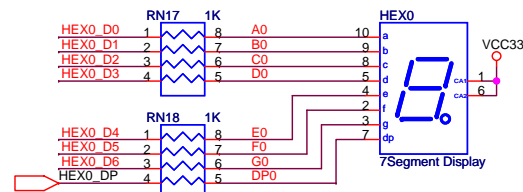
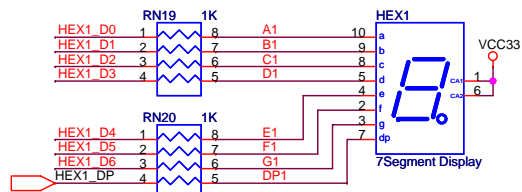
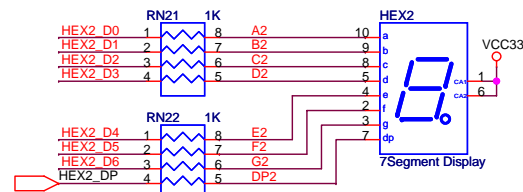
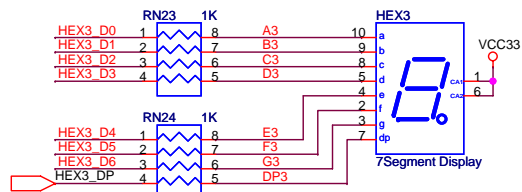
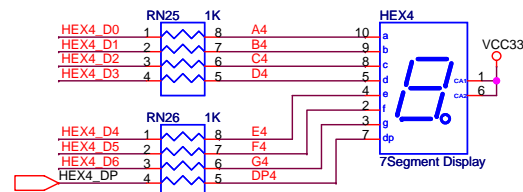
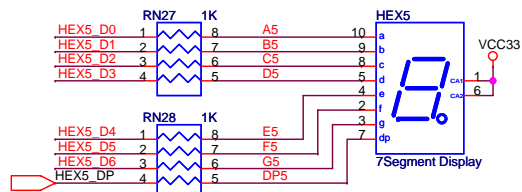
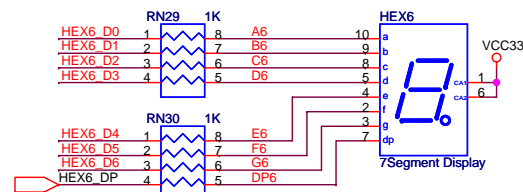
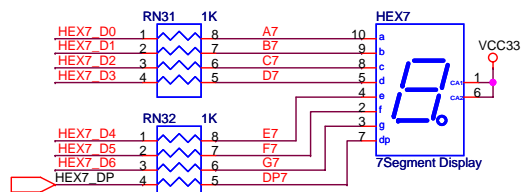


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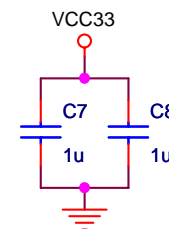
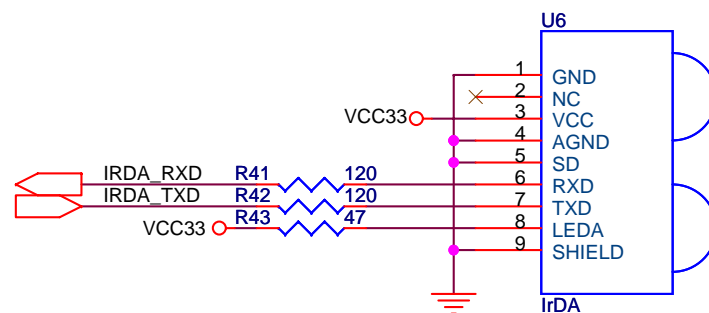
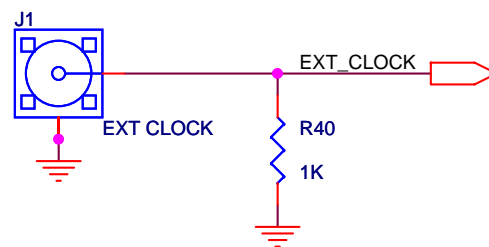
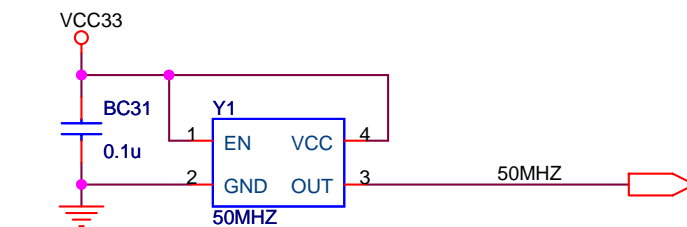
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Title		
ALTERA DE2-70		
Size	Document Number	Rev
B	LCD AND LED	1.0
Date:	Monday, November 26, 2007	Sheet 7 of 25

HEX0_D[0..6]
 HEX1_D[0..6]
 HEX2_D[0..6]
 HEX3_D[0..6]
 HEX4_D[0..6]
 HEX5_D[0..6]
 HEX6_D[0..6]
 HEX7_D[0..6]



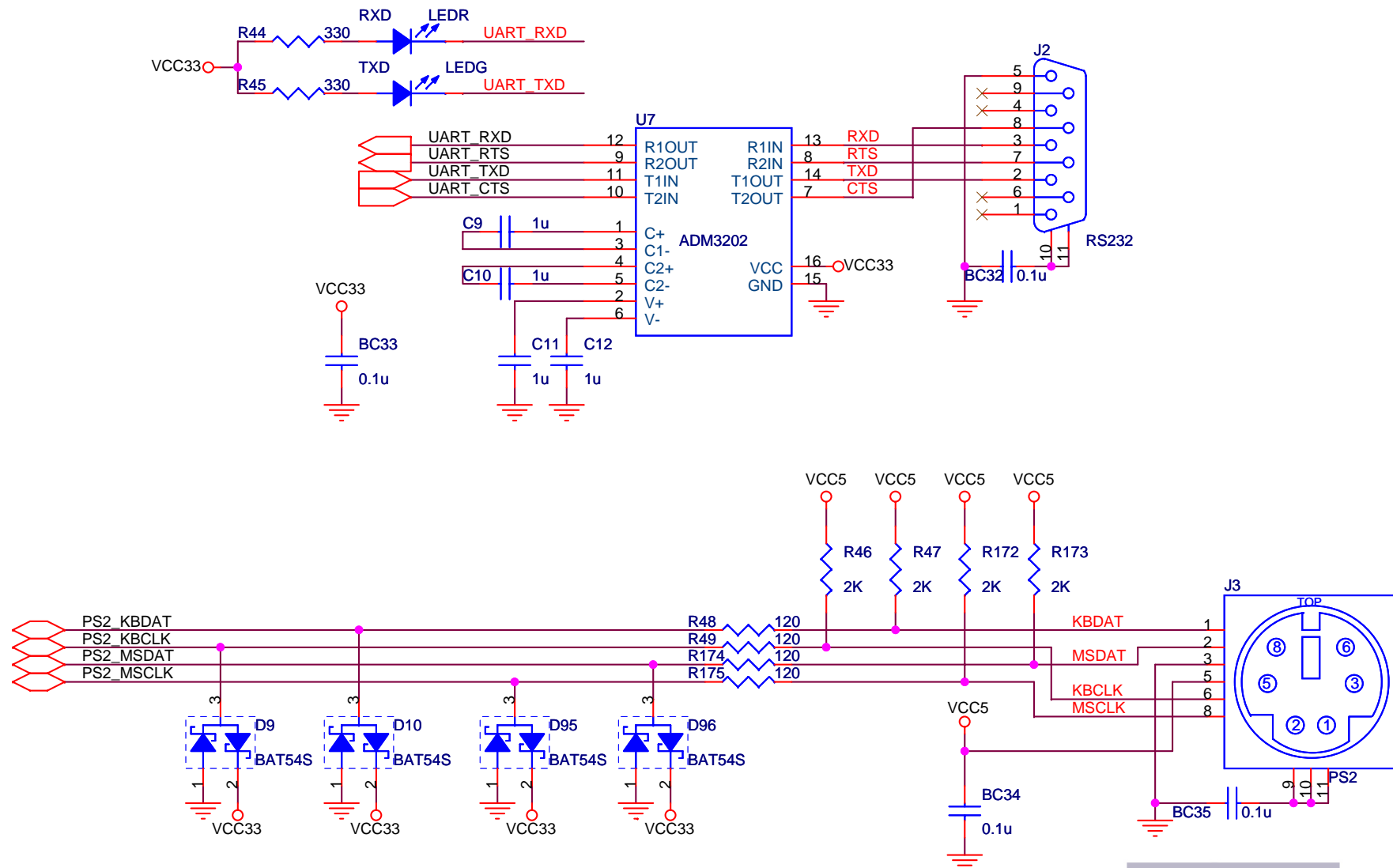
Title			ALTERA DE2-70
Size	Document Number	Rev	
B	7 SEGMENT	1.0	
Date:	Monday, November 26, 2007	Sheet	8 of 25



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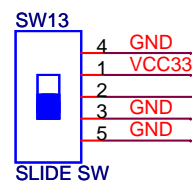
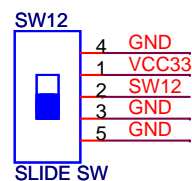
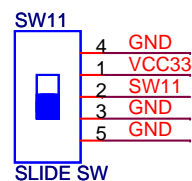
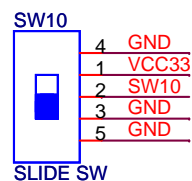
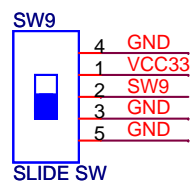
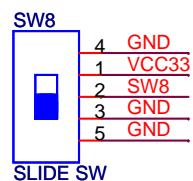
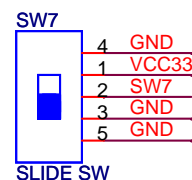
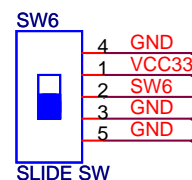
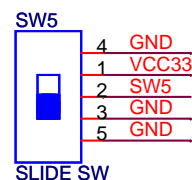
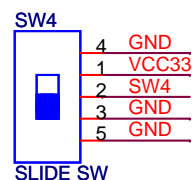
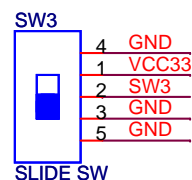
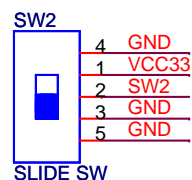
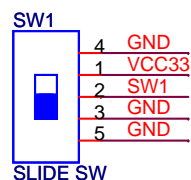
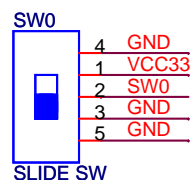
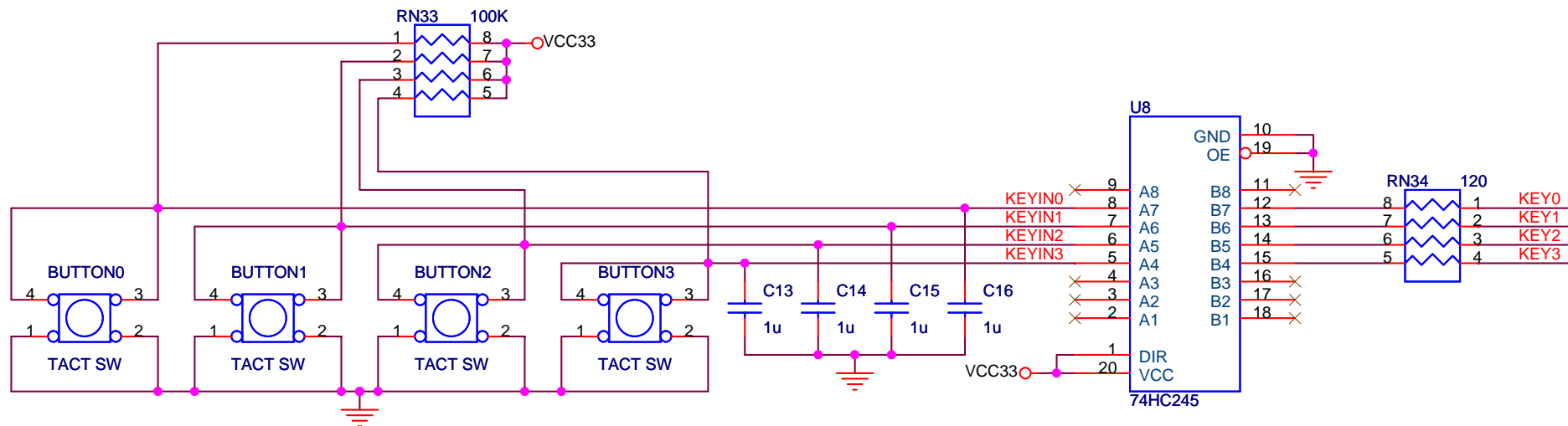
Title		
ALTERA DE2-70		
Size A	Document Number CLOCK and IrDA	Rev 1.0
Date:	Monday, November 26, 2007	Sheet 9 of 25



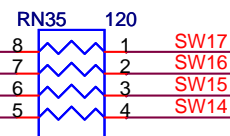
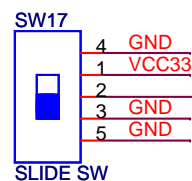
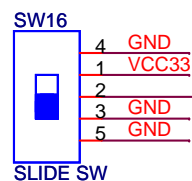
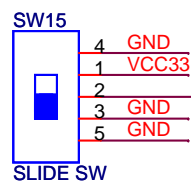
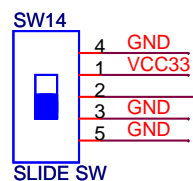
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Title		
ALTERA DE2-70		
Size A	Document Number PS2 AND RS232	Rev 1.0
Date:	Monday, November 26, 2007	Sheet 10 of 25



R50 120 SW13



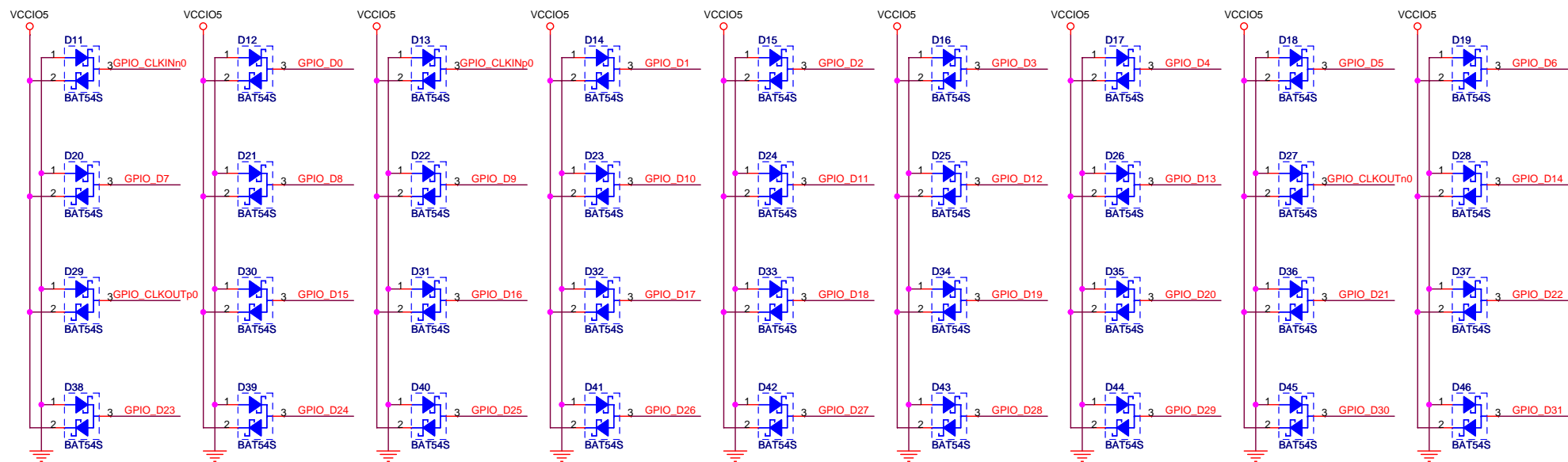
KEY[0..3]
SW[0..17]



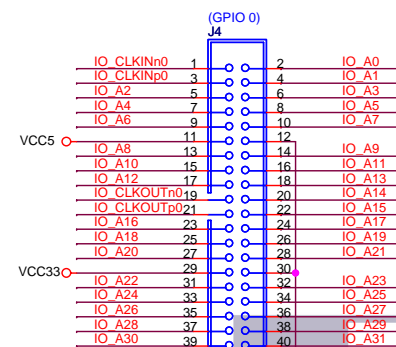
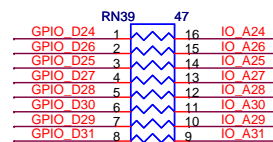
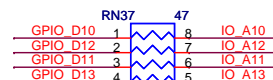
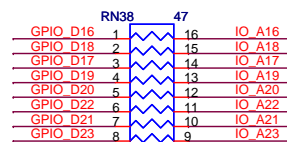
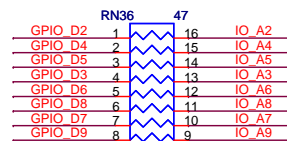
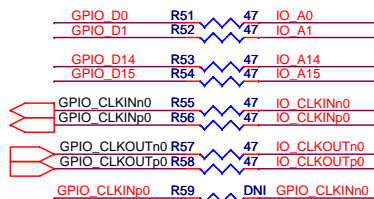
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Title		
ALTERA DE2-70		
Size A	Document Number KEY AND SWITCH	Rev 1.0
Date:	Monday, November 26, 2007	Sheet 11 of 25



GPIO_D10..311



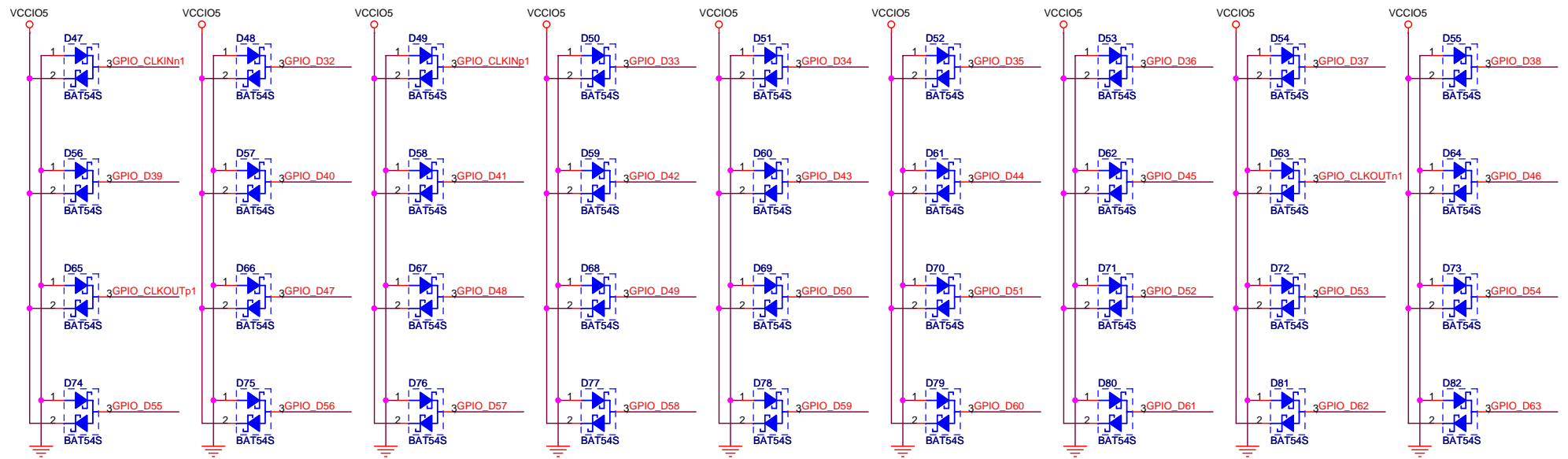
BOX Header 2X20M

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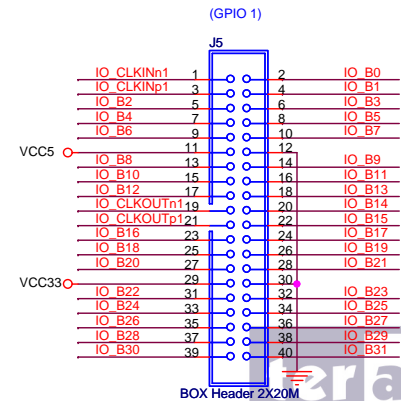
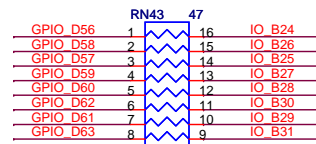
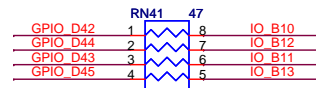
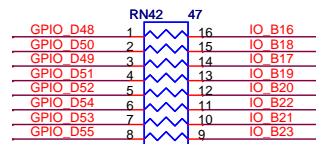
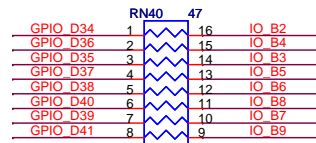
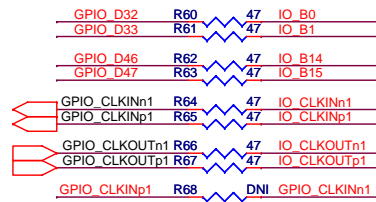
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Title			ALTERA DE2-70
Size	Document Number	Rev	
B	CONNECT A	1.0	
Date:	Monday, November 26, 2007	Sheet	12 of 25



GPIO D[32..63]



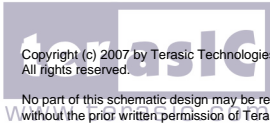
BOX Header 2X20M

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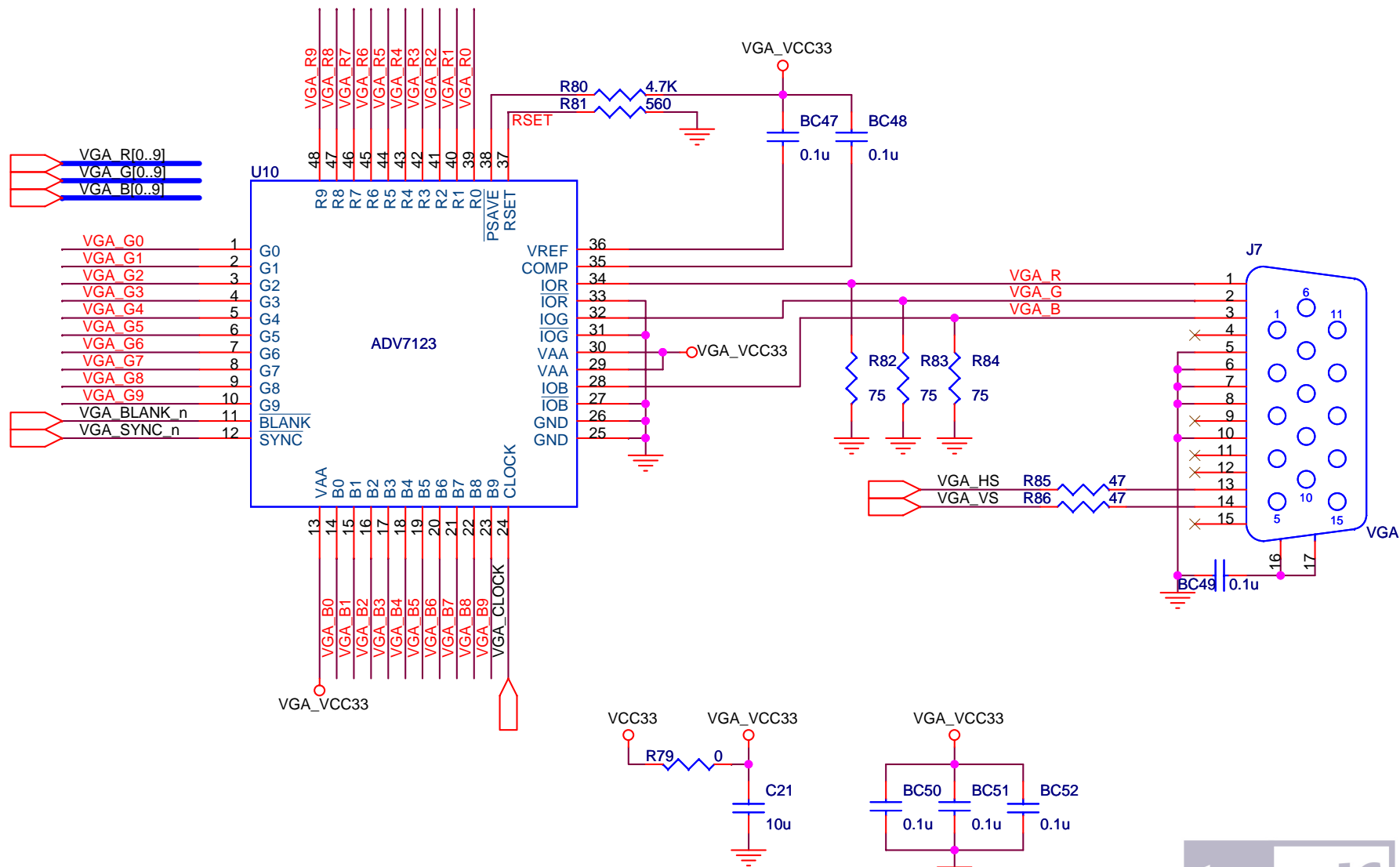
Title			ALTERA DE2-70
Size	Document Number	Rev	1.0
B	CONNECT B		
Date:	Monday, November 26, 2007	Sheet	13 of 25

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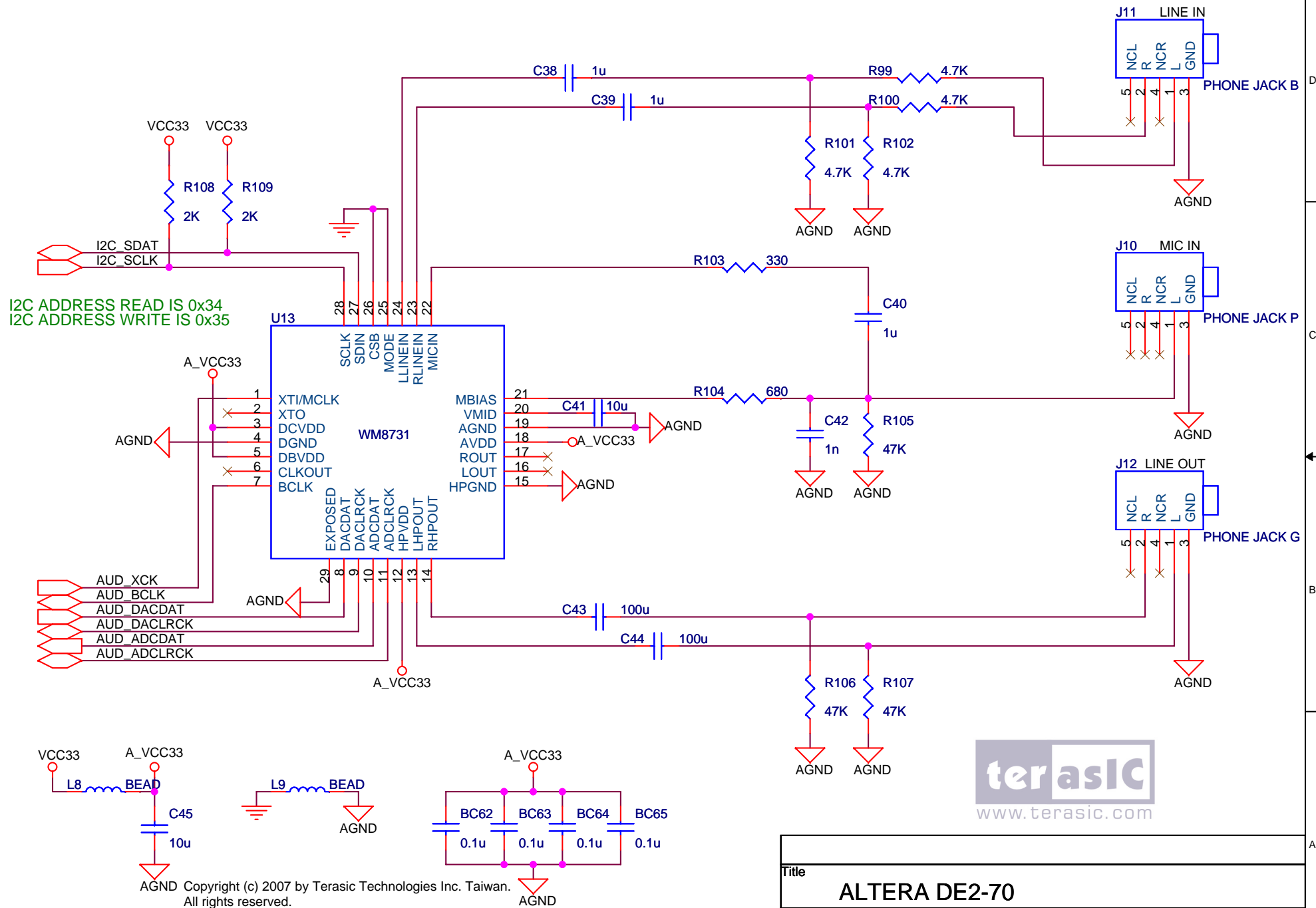
Title			
ALTERA DE2-70			
Size B	Document Number DM9000AE		Rev 1.0
Date:	Monday, November 26, 2007	Sheet	14 of 25



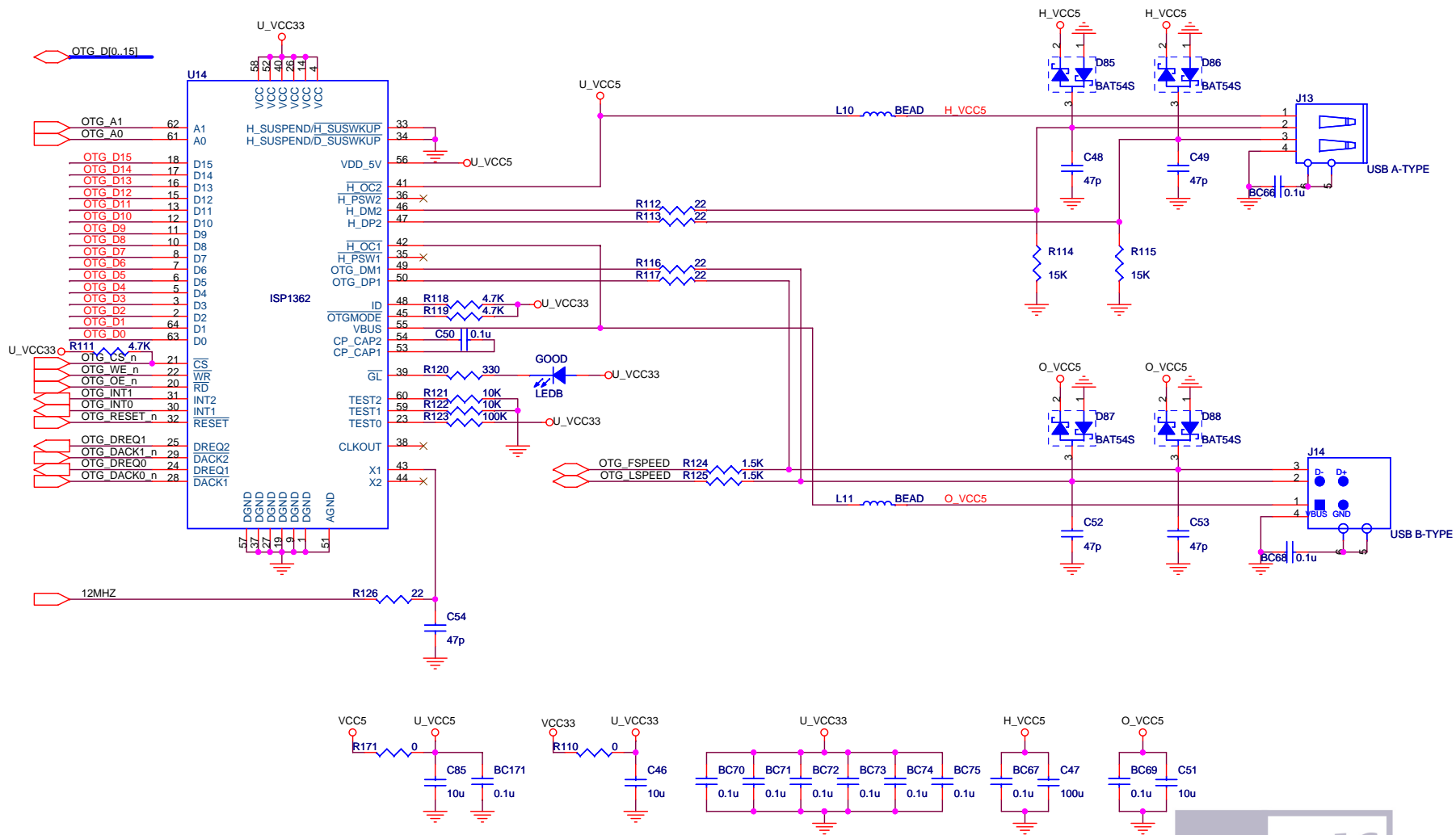
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Title		
ALTERA DE2-70		
Size A	Document Number ADV7123	Rev 1.0
Date:	Monday, November 26, 2007	Sheet 15 of 25



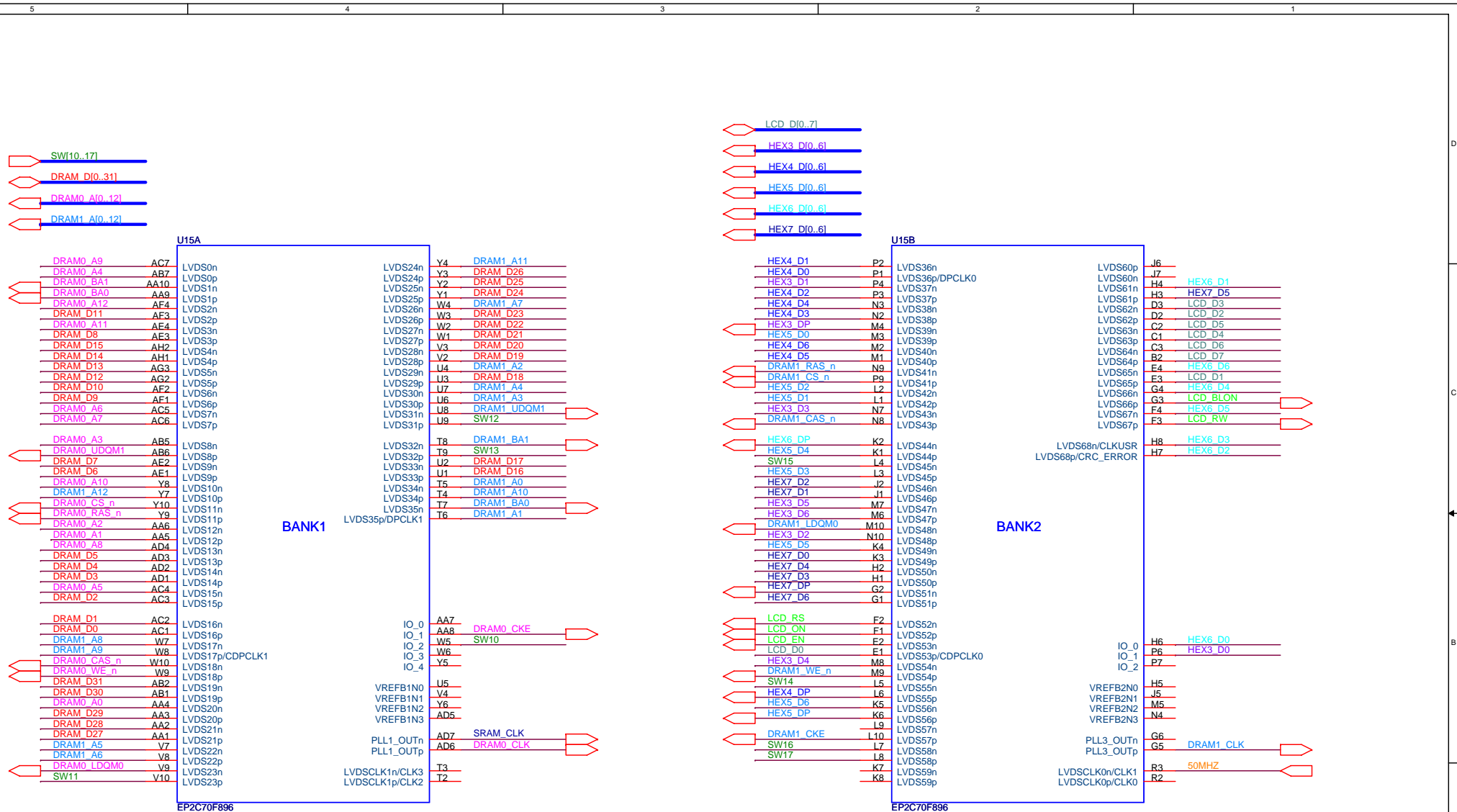
Title		
ALTERA DE2-70		
Size A	Document Number AUDIO	Rev 1.0
Date:	Monday, November 26, 2007	Sheet 17 of 25

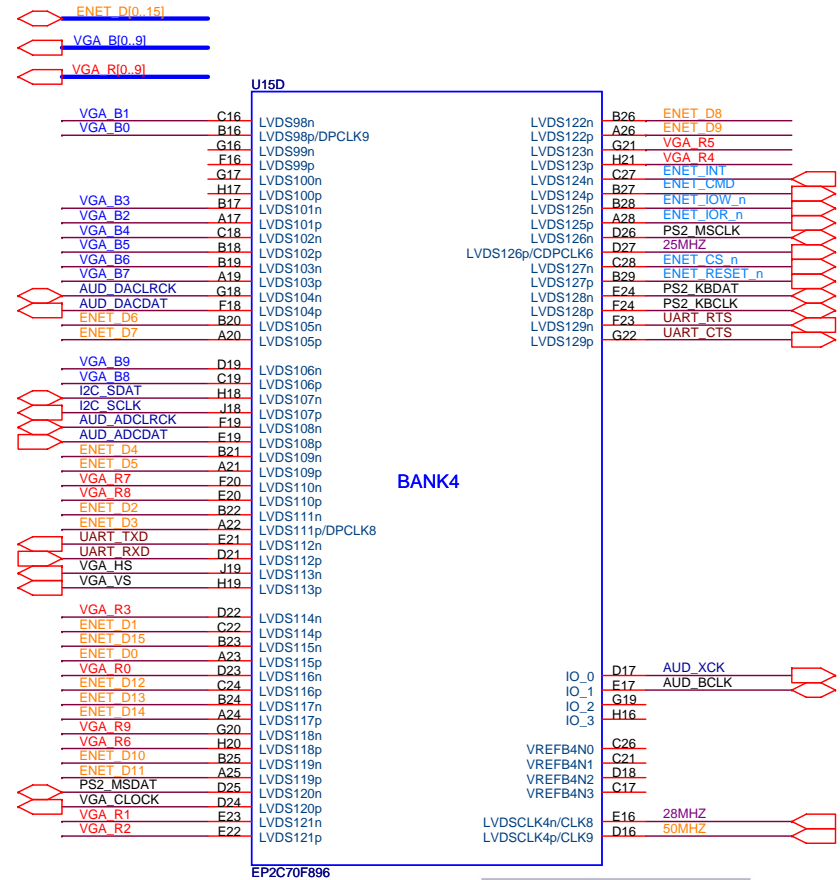
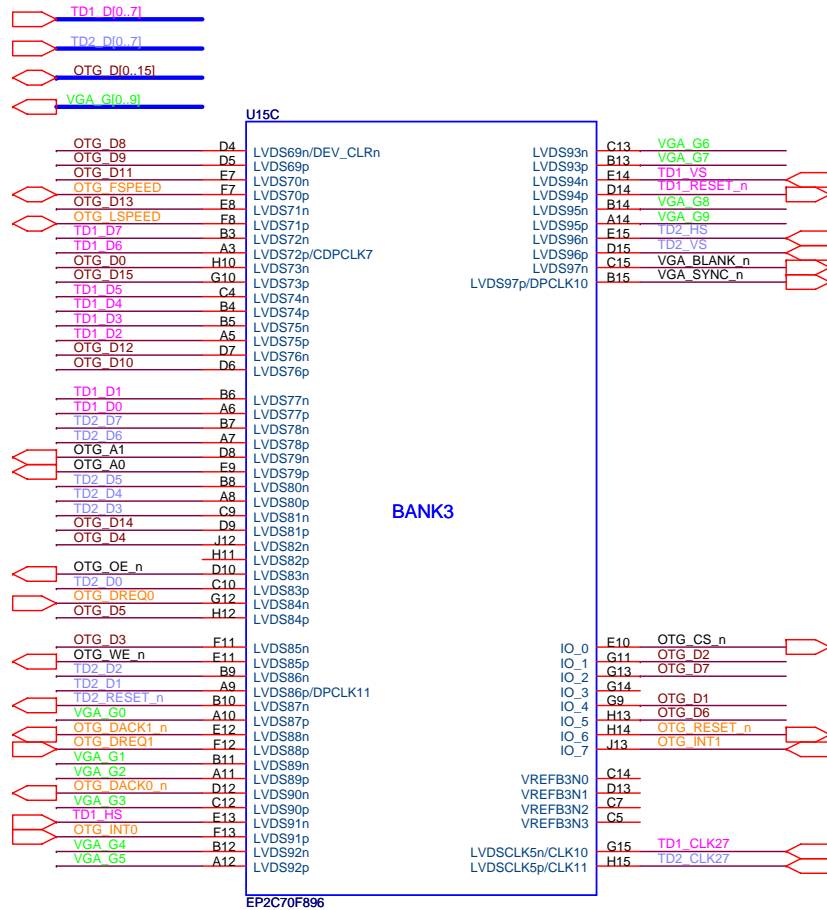


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Title		
ALTERA DE2-70		
Size	Document Number	Rev
B	ISP 1362	1.0
Date:	Monday, November 26, 2007	Sheet 18 of 25

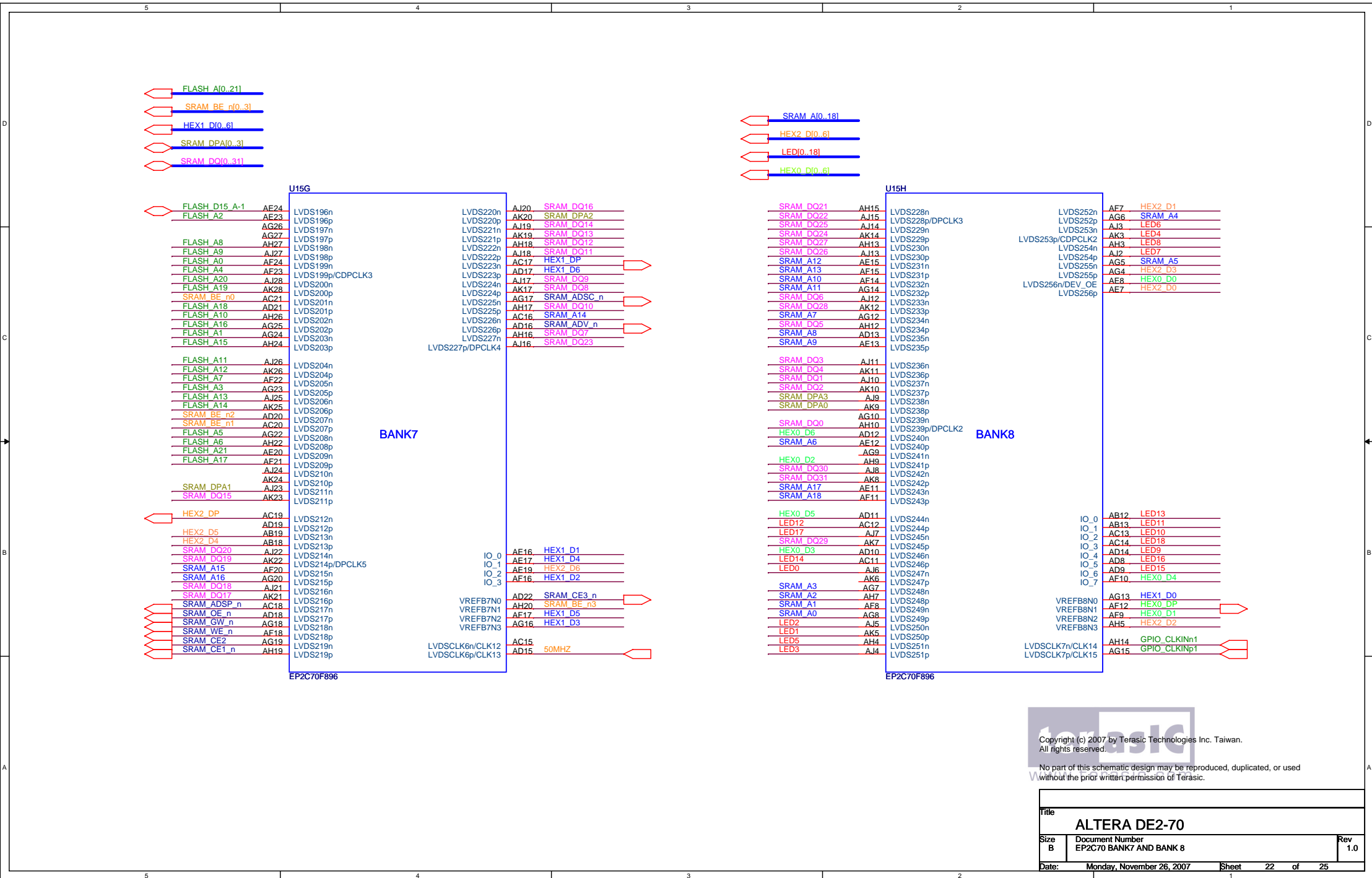




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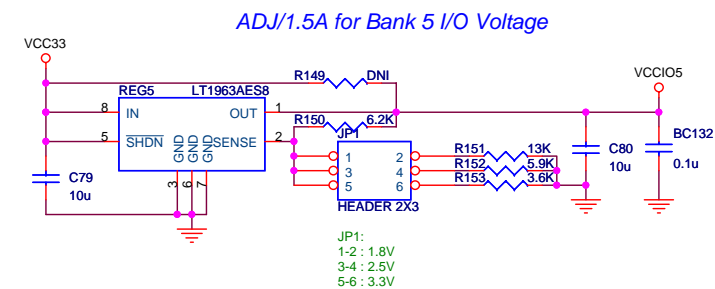
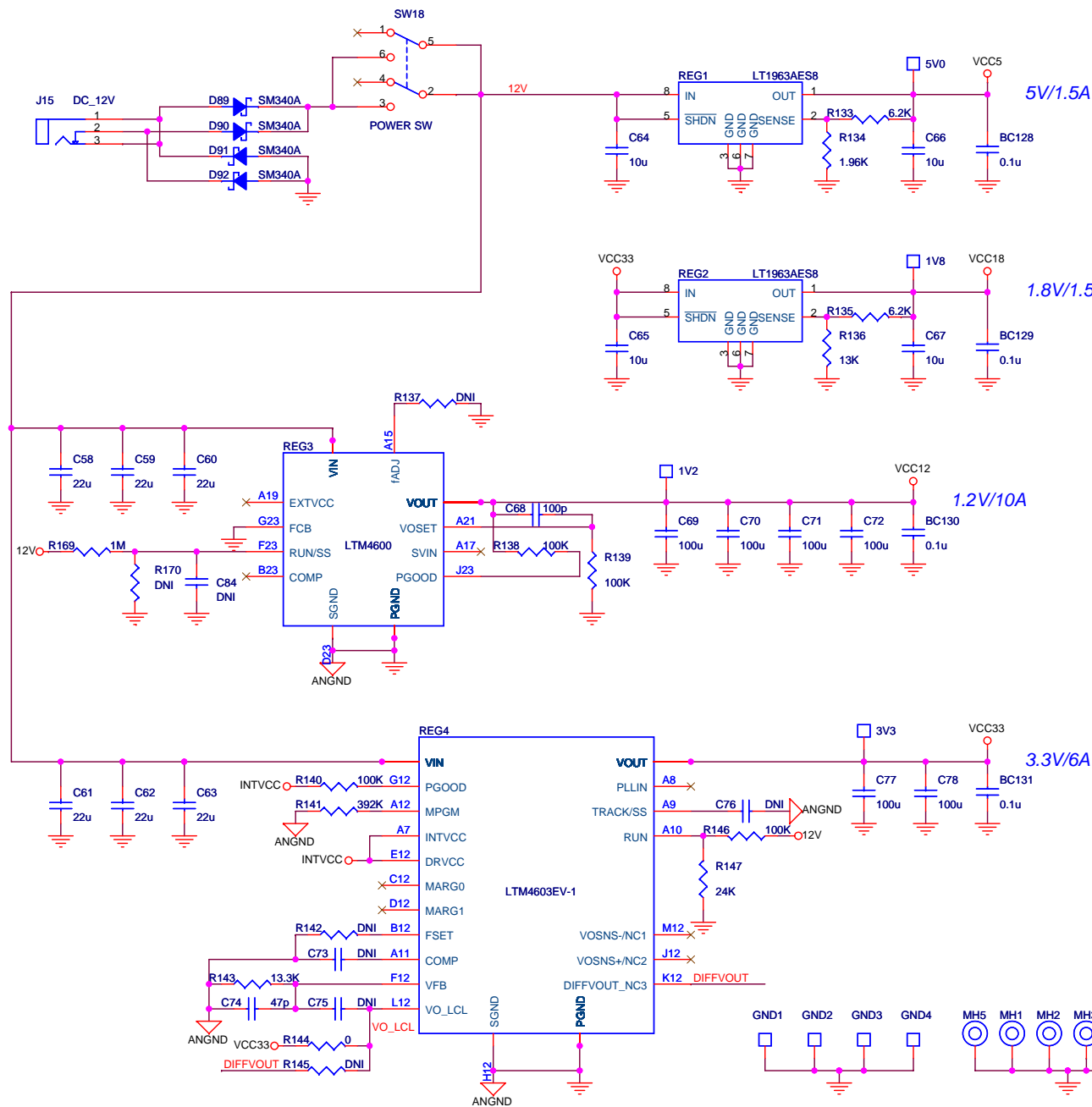
Title		
ALTERA DE2-70		
Size	Document Number	Rev
B	EP2C70 BANK3 AND BANK 4	1.0
Date:	Monday, November 26, 2007	Sheet 20 of 25



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ALTERA DE2-70		
Size	Document Number	Rev
B	EP2C70 BANK7 AND BANK 8	1.0
Date:	Monday, November 26, 2007	Sheet 22 of 25



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Size	Document Number	Rev	
	POWER	1.0	
Date:	Monday, November 26, 2007	Sheet	24 of 25

