











Copyright © 2003-2014 Terasic Technologies Inc. All Rights Reserved.





CHAPTER 1	DE5-NET OPENCL	
1.1 System R	EQUIREMENT	
1.2 OpenCL A	ARCHITECTURE	
CHAPTER 2	OPENCL FOR WINDOWS	5
2.1 Software	E INSTALLATION	5
2.2 OPENCL L	ICENSE INSTALLATION	7
2.3 CONFIGUR	Е	7
2.4 BOARD SE	TUP	9
2.5 OPENCL E	ENVIRONMENT VERIFY AND FLASH CVP	
2.6 COMPILE A	AND TEST OPENCL PROJECT	
CHAPTER 3	OPENCL FOR LINUX	
3.1 SOFTWARE	INSTALLATION	
3.2 OPENCL L	ICENSE INSTALLATION	
3.3 CONFIGUR	Е	
3.4 BOARD SE	TUP	
3.5 OPENCL E	ENVIRONMENT VERIFY AND FLASH CVP	
3.6 COMPILE A	AND TEST OPENCL PROJECT	





Chapter 1



DE5-NET, an unparalleled and powerful platform for high-speed computation, is now officially also an Altera certified board for Altera's Preferred Board Partner Program for OpenCL. It supports both 64-bit Windows and Linux. This document will introduce you how to setup OpenCL development environment for DE5-NET board, and how to compile and execute the example projects for DE5-Net. Note that OpenCL coding instruction is not in the scope of this document, but the user can refer to Altera SDK for OpenCL Programming Guide for more details.

http://www.altera.com/literature/hb/opencl-sdk/aocl_programming_guide.pdf

1.1 System Requirement

The following items are required to set up OpenCL for DE5-NET board:

- Terasic DE5-NET Board with two 2GB DDR3-SODIMM installed
- A Host PC with
 - USB Host Port
 - One PCI Express x8/x16 slot with 12V power pin
 - 32GB memory is recommended, 24GB is minimal
 - 2x3 pin 12V Power for DE5-Net(optional)
- An USB Cable(type A to mini-B)
- 64-bit Windows7 or Linux Installed
- Altera Quartus II 16.0 Installed, licensed is required
- Altera OpenCL 16.0 Installed, license is required
- DE5-Net OpenCL BSP Installed
- Visual Studio 2012 C/C++ installed for Windows7
- GNU development tools for Linux





Note, Altera OpenCL only supports 64-bit OS and x86 architecture.

1.2 OpenCL Architecture

An OpenCL project is composed of both OpenCL Kernel and Host Program as shown in **Figure 1-1**. OpenCL kernel is compiled with Altera OpenCL compiler provided by the Altera OpenCL SDK. The Host Program is compile by Visual Studio C/C++ in Windows or GCC on Linux.



Figure 1-1 Altera OpenCL Architecture





Chapter 2

OpenCL for Windows

This chapter describes how to set up DE5-NET OpenCL development environment on 64-bit Windows, and how to compile and test the OpenCL examples for DE5-Net. For more details about Altera OpenCL started guide, please refer to:

http://www.altera.com/literature/hb/opencl-sdk/aocl_getting_started.pdf

2.1 Software Installation

This section describes where to get the required softwares for OpenCL.

■ Altera Quartus II and OpenCL SDK

Altera Quartus II and OpenCL SDK can be download from the web site:

http://dl.altera.com/opencl

For Quartus II installation, please make sure that the Stratix V device is included.

■ Visual Studio 2012

If developers don't have Visual studio C/C++ 2012, they can use the trial version of Visual Studio 2012 Express. The software can be downloaded from the web site:

http://www.microsoft.com/en-us/download/details.aspx?id=34673





■ DE5-NET OpenCL BSP (Board Support Package)

After Quartus II and OpenCL SDK are installed, please create a "terasic" folder under the folder "D:\altera\16.0\hld\board", as shown in **Figure 2-1**, where assumed Quartus II is installed on the folder "D:\altera \16.0".

🕒 🗢 🔐 < Local Di	sk (D:) → altera → 16.0 → hld → board →	▼ 4 ∱ Se	arch board		× P		
Organize 👻 😭 Oper	Organize ▼ 🙀 Open Include in library ▼ Share with ▼ New folder 🛚 🖽 ▼ 🗍 🔞						
🕮 Recent Places 🔺	Name	Date modified	Туре	Size			
 ✓ □ Libraries ▷ Documents ▷ Music ▷ □ Pictures ▷ □ Videos □ 	 c5soc custom_platform_toolkit dspba_sil_jtag dspba_sil_pcie s5 ref terasic 	2016/10/13 11:08 2016/10/13 11:08 2016/10/13 11:08 2016/10/13 11:08 2016/10/13 11:08 2016/10/13 11:08	File folder File folder File folder File folder File folder File folder				
Computer Second Disk (C:) Cocal Disk (D:) Cocal Disk (D:) terasic File folder	e modified: 2016/10/27 15:48						

Figure 2-1 Create "Terasic" Folder under OpneCL SDK installed folder

Then, download the DE5NET_openCL_BSP_16.0.zip for Altera OpenCL 16.0 from the web: <u>http://cd-de5-net.terasic.com</u>

Decompress DE5NET_openCL_BSP_16.0.zip and copy content into the "terasic" folder, as shown in **Figure 2-2**.

🕒 🗢 📕 🗢 Loca	I Disk	(D:) ▶ altera ▶ 16.0 ▶ hld ▶	board + terasic +	✓ ✓ _↑ Search	terasic			م م							
Organize 🔻 Inclu	de in l	library 🔻 Share with 👻	New folder			:==	•	?							
📃 Recent Places	*	Name	Date modified	Туре	Size										
-		퉬 hardware	2016/10/13 11:10	File folder											
Cibraries		🜗 mmd	2016/10/13 11:10	File folder											
Documents	ents	source	2016/10/27 15:48	File folder											
Music		🌗 test	2016/10/27 14:47	File folder											
Pictures		鷆 windows64	2016/10/20 17:22	File folder											
Videos	5 🗉	-	=	=	=	=	=	=	🔮 board_env.xml	2016/10/20 17:30	XML Document		1 KB		
Nomputer		README.txt	2014/8/13 13:20	Text Document		1 KB									
🏭 Local Disk (C:)															
👝 Local Disk (D:)															
A	-														
7 items															

Figure 2-2 DE5-Net OpenCL BSP Content





2.2 OpenCL License Installation

An OpenCL license is required for Altera OpenCL SDK to compile any OpenCL projects successfully. Developers can purchase the OpenCL license from either Altera or Terasic. Assuming that developers have obtained a license file with the filename "license.dat", and it is saved in the local disk with the file path such as "c:\license.dat". The license can then be set up by creating an environment variable LM_LICENSE_FILE, and set its value as "c:\license.dat". Note that this environment value needs to correspond to the actual "license.dat" file location.

Now, here are the procedures to create the required **LM_LICENSE_FILE** environment variable on Windows 7:

- 1. Open the Start Menu and right click on **Computer**. Select **Properties**.
- 2. Select Advanced system settings.
- 3. In the Advanced tab, select Environment Variables.
- 4. Select New.
- 5. In the popup New User Variable dialog as shown in Figure 2-3, type "LM_LICENSE_FILE" in the Variable name edit box and type "c:\license.dat" in the Variable value edit box.

Edit User Variable	×
Variable name:	LM_LICENSE_FILE
Variable value:	c: \icense.dat
	OK Cancel

Figure 2-3 Setup LM_LICENSE_FILE Environment Variable

2.3 Configure

For Altera OpenCL SDK to be able to find the kit location of DE5-NET correctly, developers need to create an environment variable **AOCL_BOARD_PACKAGE_ROOT**, and set its value as:

 $``\% ALTERAOCLSDKROOT\% \ board\ terasic''$

Also, append "%AOCL_BOARD_PACKAGE_ROOT%\windows64\bin" and "%ALTERAOCLS



DKROOT%/windows64/bin" and "%ALTERAOCLSDKROOT%\host\windows64\bin" and "%A LTERAOCLSDKROOT%\bin" into the **PATH** environment variable so that the OpenCL SD K can find the binary file provided by DE5-NET BSP.

Here are the procedures to create the required **AOCL_BOARD_PACKAGE_ROOT** environment variable on Windows 7:

- 1. Open the Start Menu and right click on **Computer**. Select **Properties**.
- 2. Select Advanced system settings.
- 3. In the Advanced tab, select Environment Variables.
- 4. Select New.
- 5. In the popup New User Variable dialog as shown in Figure 2-4, type "AOCL_BOARD_PACKAGE_ROOT" in the Variable name edit box and type "%ALTERAOCLSDKROOT%\board\terasic" in the Variable value edit box.
- 6. In Command Prompt window, type "aocl install" to install PCI Express driver. Note that users need to have administrator privileges to install the driver.

Edit User Variable	x
Variable name:	AOCL_BOARD_PACKAGE_ROOT
Variable value:	%ALTERAOCLSDKROOT%\board\terasic
	OK Cancel

Figure 2-4 Setup AOCL_BOARD_PACKAGE_ROOT Environment Variable

Here are the procedures to add "%AOCL_BOARD_PACKAGE_ROOT%\windows64\bin" into the **PATH** environment variable on Windows 7:

- 1. Open the Start Menu and right click on **Computer**. Select **Properties**.
- 2. Select Advanced system settings.
- 3. In the Advanced tab, select Environment Variables.
- 4. In the Environment Variables window (as shown below), highlight the **Path** variable in the Systems Variable section and click the **Edit** button as shown in **Figure 2-5**.
- 5. In the Edit dialog, Append "%AOCL_BOARD_PACKAGE_ROOT%\windows64\bin" into the Variable value edit box. Note, each different directory should be separated with a semicolon as shown in **Figure 2-6**.





ronment Variables					
ser variables for Ad	ministrator				
Variable	Value				
PATH	D:\altera\16.0\hld\bin;D:\altera\16.0\hl				
QSYS_ROOTDIR	D:\altera\16.0\quartus\sopc_builder\bin				
QUARTUS_ROO	D:\altera\16.0\quartus				
SOPC_KIT_NIOS2	D:\altera\16.0\nios2eds				
	New Edit Delete				
ystem variables					
ystem variables Variable	Value				
ystem variables Variable ComSpec	Value C:\Windows\system32\cmd.exe				
ystem variables Variable ComSpec FP_NO_HOST_C	Value C:\Windows\system32\cmd.exe NO				
variables Variable ComSpec FP_NO_HOST_C NUMBER_OF_P	Value C:\Windows\system32\cmd.exe NO 4				
variables Variable ComSpec FP_NO_HOST_C NUMBER_OF_P OS	Value C:\Windows\system32\cmd.exe NO 4 Windows_NT				
variables Variable ComSpec FP_NO_HOST_C NUMBER_OF_P OS	Value C:\Windows\system32\cmd.exe NO 4 Windows_NT New Edit Delete				

Figure 2-5 Select "Path" and click "Edit" bottom

Edit User Variable	×
Variable name:	PATH
Variable value:	BOARD_PACKAGE_ROOT%\windows64\bin
	OK Cancel

Figure 2-6 Append "%AOCL_BOARD_PACKAGE_ROOT%\windows64\bin"

2.4 Board Setup

Before testing OpenCL on DE5-NET, please following below procedures to set up DE5-NET board





on your PC as shown in Figure 2-7.

- 1. Make sure your PC is powered off.
- 2. Insert DE5-NET board into PCI Express x8 or x16 slot.
- 3. Connect PC's 12V PCI Express 6-pin power source to the DE5-NET
- 4. Connect PC's USB port to DE5-NET mini USB port using an USB cable.

Note, the usb cable can be removed later if OpenCL code had been programming to the startup configuration flash of DE5-NET by 'aocl flash' command.



Figure 2-7 Setup DE5-NET board on PC

2.5 OpenCL Environment Verify and Flash CvP

This section will show how to make sure the OpenCL environment is setup correctly. Firstly, please open **Command Prompt** windows by click Windows **Start** button, clicking **All Programs**, clicking **Accessories**, and then click **Command Prompt**.

■ Target Board

In Command Prompt window, type "aoc --list-boards" command, and make sure "de5net_a7" is



DE5-Net OpenCL

www.terasic.com October 31, 2016



listed in **Board list** as shown in **Figure 2-8**.



Figure 2-8 'de5net_a7' is listed in Board list

Test 'aocl flash' Command

In Command Prompt window, type "cd D:\altera\16.0\hld\board\terasic\tests\hello_world\bin" to go to hello world OpenCL project folder, then type "aocl flash acl0 hello_world.aocx" to write **hello_world.aocx** OpenCL image onto the startup configuration flash of DE5-NET. Before flash programming, the programmer will ask users which startup configuration image area will be used as shown in **Figure 2-9**. This is because DE5-NET provides two startup configuration image areas, called as Factory Image and User Image. We recommend users to key in '1' to select User Image area.

Administrator: C:\Windows\system32\cmd.exe	
D:\altera\16.0\hld\board\terasic\tests\hello_world\bin>"D:/altera/16.0/quartus"\ bin64\perl\bin\perl "D:\altera\16.0\hld\board\terasic"\windows64\libexec\flash.p l acl0 C:\Users\ADMINI~1\AppData\Local\Temp/2260Commandpm521_1477621684_0_fpga_t emp.bin ====================================	•
Please select the flash page where to store your FPGA configure data: [0] Factory Image Location(Address 0x00040000), SW5.2 = "1" (Right Position) [1] User Image Location(Address 0x020C0000), SW5.2 = "0" (Left Position) Enter a digital number 0 or 1 (Or other values to exit the program) followed by pressing the "Enter" key:	
Flash Programming	
Info: Running Quartus Prime Convert_programming_file Info: Version 16.0.2 Build 222 07/20/2016 SJ Standard Edition Info: Copyright (C) 1991-2016 Altera Corporation. All rights reserved. Info: Your use of Altera Corporation's design tools, logic functions Info: and other software and tools, and its AMPP partner logic Info: functions, and any output files from any of the foregoing Info: (including device programming or simulation files), and any Info: associated documentation or information are expressly subject Info: to the terms and conditions of the Altera Program License Info: Subscription Agreement the Altera Quartus Prime License Agreement	
Info: the Altera MegaCore Function License Agreement, or other	-

Figure 2-9 Select Flash Page





After users select desired flash area, it will take about 20 minutes for flash programming. **Figure 2-10** is the screen shot when flash programming is done successfully.

F80000
Info (209005): Programming status: programming flash memory at byte address 0x0F F90000
Info (209005): Programming status: programming flash memory at byte address 0x0F FA0000
Info (209005): Programming status: programming flash memory at byte address 0x0F
Info (209005): Programming status: programming flash memory at byte address 0x0F
Info (209005): Programming status: programming flash memory at byte address 0x0F
Info (209005): Programming status: programming flash memory at byte address 0x0F
FE0000 Info (209005): Programming status: programming flash memory at byte address 0x0F
FF0000 Info (209011): Successfully performed operation(s)
Info (209061): Ended Programmer operation at Mon Nov 10 18:07:25 2016 Info: Quartus II 64-Bit Programmer was successful. 0 errors, 0 warnings
Info: Peak virtual memory: 2551 megabytes Info: Processing ended: Mon Nov 10 18:07:25 2014
Info: Elapsed time: 00:38:52 Info: Total CPU time (on all processors): 00:00:34
D:\altora\16 (A\bld\board\torasic\tosts\ballo world\bin>
b. diferatio. o difutional diferasic (rests metro_wor futurit)

Figure 2-10 'aocl flash acl0 hello_world.aocx" successfully

To make sure a correct image is used when FPGA boots up, please make sure the dip switch SW5.2 on DE5-NET is changed to the correct location. If a User Image area is selected, the dip switch SW5.2 on the DE5-NET should be moved to **left** position as shown in **Figure 2-11**.



Figure 2-11 Set SW5.2 to Left Position (User Image Page)

After flash programming is done successfully and SW5.2 is set to correct position, developers can power off PC and turn it back on and check whether the **hello_world** OpenCL image, which is CvP enabled, configures the FPGA successfully. In Command Prompt window, type "cd D:\altera\16.0\hld\board\terasic\tests\hello_world\bin" to go to **hello_world\bin** project folder, then type "aocl program acl0 hello_world.aocx" to configure the FPGA with **hello_world.aocx** OpenCL image. If the programming message displays "Program succeed" as shown in **Figure 2-12**, it means





the hello_world OpenCL image is programmed into the flash correctly and CvP works well.



Figure 2-12 'aocl program acl0 hello_world.aocx" use CvP

2.6 Compile and Test OpenCL Project

This section will show how to compile and test OpenCL kernel and OpenCL Host Program for the vector_add project. Developers can use the same procedures to compile and test other OpenCL examples for DE5-NET.

Compile OpenCL Kernel

The utility **aoc** (Altera SDK for OpenCL Kernel Compiler) is used to compile OpenCL kernel. In Command Prompt window, type "*cd D:\altera\16.0\hld\board\terasic\tests\vector_add*" to go to **vector_add** project folder, then type "*aoc device\vector_add.cl -o bin\vector_add.aocx --board de5net-a7*" to compile the OpenCL kernel. It will take about one hour for compiling. When the compilation process is finished, OpenCL image file vector_add.aocx is generated. **Figure 2-13** is the screenshot when OpenCL kernel is compiled. For required parameters to compile vector_add.cl, please refer to the README.txt that is in the same folder as the vectorAdd.cl. For detailed usage of **aoc**, please refer to the **Altera SDK for OpenCL Programming Guide**:

http://www.altera.com/literature/hb/opencl-sdk/aocl_programming_guide.pdf







Figure 2-13 'aoc vector_add.cl" OpenCL kernel compile

Compile Host Program

Visual Studio C/C++ 2012 is used to compile the Host Program. Launch Visual Studio, and select menu item "FILE \rightarrow Open Project...". In the Open Project dialog, go to the folder "D:\altera\16.0\hld\board\terasic\tests\vector_add", and select "vector_add.sln" as shown Figure 2-14.

X 打开项目							
🔾 🗢 📕 « altera	• ▶ 1	6.0 ▶ hld ▶ board ▶ terasic ▶ t	tests ▶ vector_add ▶ ▼	← Search vect	tor_add		Q
Organize 🔻 New	folder				•		2
🧮 Desktop	*	Name	Date modified	Туре	Size		
Downloads		📙 bin	2016/10/28 10:41	File folder			
Recent Places		鷆 device	2016/10/24 14:18	File folder			
🚍 Libraries		퉬 host	2016/10/24 14:18	File folder			
Documents		\mu x64	2016/10/24 16:14	File folder			
J Music	=	🖓 vector_add.sln	2016/5/31 17:00	Microsoft Visual	S	3 KB	
Pictures		🐉 vector_add.vcxproj	2016/10/24 16:14	VC++ Project		9 KB	
Videos							
👰 Computer							
ڏ Local Disk (C:)	-						
F	ile nar	ne: vector add cla		- 新有项目文4	牛(* cln:* dev	* 1/514/	-
	ine riai	vector_add.sin			-(.an, .usv	v, .vev,	
				Open		Cancel	

Figure 2-14 Open vector_add.sln Host Program





After vector_add Host Program project is opened successfully, in Visual Studio IDE select menu item "BUILD→Build Solution" to build host program. When build is successfully, you will see successful message as show in Figure 2-15. The execute file is generate in:

 $``D:\lattera\16.0\hld\board\terasic\tests\vector_add\bin\host.exe''$



Figure 2-15 Message for vector_add Host Program build successfully

Test vector_add project

Firstly, use the compiled OpenCL image file vector_add.aocx to configure the FPGA. In Command Prompt window, type "cd D:\altera\16.0\hld\board\terasic\tests\vector_add\bin" to go to **vector_add** \bin project folder, then type "aocl program acl0 vector_add.aocx" to configure FPGA with the OpenCL Image vector_add.aocx. If configuration is successfully, you will see the successful message as shown in Figure 2-16.



Figure 2-16 "aocl program acl0 vector_add.aocx" configured successfully

In Command Prompt window, execute "host.exe". **Figure 2-17** is the screen shot when the test is successful.





Administrator: C:\Windows\system32\cmd.exe	<u> </u>
D:\altera\16.0\hld\board\terasic\tests\wector_add\bin>aocl program acl0 vector_a dd.aocx aocl program: Running reprogram from D:\altera\16.0\hld\board\terasic/windows64/ libexec Start to program the device acl0 Program succeed.	
D:\altera\16.0\hld\board\terasic\tests\wector_add\bin>_	

Figure 2-17 "vector_add" test successfully





Chapter 3



This chapter describe how to setup DE5-NET OpenCL development environment on 64-bit Linux (Red Hat Enterprise Linux 5.6 or later and CentOS 6.4 or later (with gcc-4.8.0 and libstdc++.so.6.0.18 or later)are recommended), and how to compile and test the OpenCL examples for DE5-Net. For more details about Altera OpenCL, please refer to Altera SDK for OpenCL Getting Started document:

http://www.altera.com/literature/hb/opencl-sdk/aocl_getting_started.pdf

3.1 Software Installation

This section describes how to download and install the required software for OpenCL.

■ Altera Quartus II and OpenCL

Altera Quartus II and OpenCL can be download from the web site:

http://dl.altera.com/opencl/

open the link and select the Linux operation system and the needed version(default the latest) as Figure 3-1 shows.





Altera SDK for OpenCL™	
Release date: May, 2016	Altera [®] SDK
Latest Release: v16.0	for OpenCL
Select release: 16.0 V	
Download Method 🗘 🖲 Akamai DLM3 Download Manager 🟮	O Direct Download
Windows SDK Linux SDK RTE Updates	
Download and install instructions: More 	
Read Altera SDK for OpenCL Getting Started Guide	
Altera SDK for OpenCL (includes Quartus Prime softwar Size: 20.4 GB MD5: 896FC0ACDB7A1A7E9DB4D80273	re and devices) 👔

Figure 3-1 OpenCL Linux version selection

In the OpenCL software download selection form, choose and click the Altera SDK for OpenCL as **Figure 3-2** show.

Windows SDK	Linux SDK RTE Updates
Download and i	nstall instructions: <u>More</u>
Altera SDK fo Size: 20.4 GE	MD5: 896FC0ACDB7A1A7E9DB4D8027354E975
Download	

Figure 3-2 OpenCL Linux version download

Quartus II software uses the built-in USB-Blaster II drivers on Linux to access USB-Blaster II download cable on DE5-Net. but after installed the Quartus II software with built-in drivers, User need to change the port permission for USB-Blaster II via issuing





'gedit /etc/udev/rules.d/51-usbblaster.rules'

to create and add the following lines to the /etc/udev/rules.d/51-usbblaster.rules file.

```
# USB-Blaster
BUS=="usb", SYSFS{idVendor}=="09fb", SYSFS{idProduct}=="6001", MODE="0666"
BUS=="usb", SYSFS{idVendor}=="09fb", SYSFS{idProduct}=="6002", MODE="0666"
BUS=="usb", SYSFS{idVendor}=="09fb", SYSFS{idProduct}=="6003", MODE="0666"
# USB-Blaster II
BUS=="usb", SYSFS{idVendor}=="09fb", SYSFS{idProduct}=="6010", MODE="0666"
BUS=="usb", SYSFS{idVendor}=="09fb", SYSFS{idProduct}=="6810", MODE="0666"
```

Note: You must have system administration (root) privileges to configure the USB-Blaster download cable drivers.

GNU development tools

GNU development tools such as gcc(include g++) and make are required to build the driver and application under Linux. And the gcc version must gcc-4.8.0 or later. User can issue 'yum install gcc ccompat-gcc-c++ make' command to download and install them and their dependencies via internet.

Note: To install the SDK on Linux, you must install it in a directory that you own (that is, a directory that is not a system directory). You must also have sudo or root privileges.

■ DE5-NET openCL BSP (Board Support Package)

After Quartus II and OpenCL SDK are installed, please create a "terasic" folder under the folder "/root/altera/16.0/hld/board", where assumed Quartus II is installed on the folder "/root/altera/16.0".

Then, download the DE5-NET BSP for Altera OpenCL 16.0 from the web:

http://cd-de5-net.terasic.com

Decompress DE5NET_openCL_bsp_16.0.tar.gz and copy content into the "terasic" folder, as shown in Figure 3-3.







Figure 3-3 Copy DE5-Net OpenCL BSPT to terasic Folder

3.2 OpenCL License Installation

An OpenCL license is required to compile the OpenCL projects for Altera OpenCL SDK. Developers can purchase the OpenCL license from either Altera or Terasic. Assuming that developers have obtained a license file with the filename "license.dat", and it is saved in the local disk with the file path such as "/root/altera/16.0/hld/license.dat". The license can then be set up by creating an environment variable LM_LICENSE_FILE, and set its value as "/root/altera/16.0/hld/license.dat".

Note that this environment value needs to correspond to the actual "license.dat" file location.

The next chapter will describe the license environment setting up.

3.3 Configure

If you install the ALTERA FPGA development software and OpenCL SDK on a system that does not contain any .cshrc or Bash Resource file (.bashrc) in your directory, you must set the ALTERAOCLSDKROOT and PATH environment variables manually. And for Altera OpenCL SDK able to find the kit location of DE5-NET correctly, the developers need to create an





environment variable for the DE5-NET board AOCL_BOARD_PACKAGE_ROOT, and set its value as:

"%ALTERAOCLSDKROOT%\board\terasic\de5net"

Alternatively, you can edit the "/etc/profile" **profile** file, and append the environment variables to it. To do this type "*gedit /etc/profile*" *command on Linux Terminal* to open the **profile** file by the **gedit** editor tool, and append the following setting to the **profile** file. Then, save the file and type "*source /etc/profile*" command in Linux Terminal to make the settings make effect.

export **QUARTUS_ROOTDIR**=/root/altera/16.0/quartus export **ALTERAOCLSDKROOT**=/root/altera/16.0/hld export **PATH**=\$PATH:"\$QUARTUS_ROOTDIR"/bin:"\$ALTERAOCLSDKROOT"/linux64/bin:"\$ALTERAOCLSD DKROOT"/bin: "\$AOCL_BOARD_PACKAGE_ROOT"/linux64/bin Export **LD_LIBRARY_PATH**="\$AOCL_BOARD_PACKAGE_ROOT"/linux64/lib:"\$ALTERAOCLSDKROOT" /host/linux64/lib: "\$AOCL_BOARD_PACKAGE_ROOT"/linux64/lib export **AOCL_BOARD_PACKAGE_ROOT**="\$ALTERAOCLSDKROOT"/board/terasic export **QUARTUS_64BIT**=1 export **LM_LICENSE_FILE**=/root/altera/16.0/hld/license.dat

3.4 Board Setup

Before testing OpenCL on DE5-NET, please following the below procedure to setup DE5-NET board on your PC as shown in Figure 3-4.

- 1. Make sure your PC is power off.
- 2. Insert DE5-NET board into PCI Express x8 or x16 slot.
- 3. Connect PC's 12V PCI Express 6-pin power to the DE5-NET source (if there's not, ignore this step)
- 4. Connector PC's USB port to DE5-NET mini USB port using an USB cable.

Note, the usb cable can be removed later if any one of OpenCL code had been programming to the startup configuration flash of DE5-NET by 'aocl flash' command.







Figure 3-4 Setup DE5-NET board on PC

3.5 OpenCL Environment Verify and Flash CvP

This section will show how to make sure the OpenCL environment is setup correctly.

Firstly, please open the Linux system **terminal** window by right click the Mouse on system desktop, then clicking on **Open Terminal**.

■ Target Board

In the Linux terminal, type "*aoc --list-boards*" command, and make sure "de5net_a7" is listed in **Board list** as shown in **Figure 3-5**.



Figure 3-5 'de5net_a7' is listed in Board list





Then type "aocl install" to load the PCIe driver for the DE5-NET as shown in Figure 3-6.

root@localhost:~/altera/16.0/hld/board
<u>F</u> ile <u>E</u> dit <u>V</u> iew <u>T</u> erminal Ta <u>b</u> s <u>H</u> elp
[root@localhost board]# aocl install
aocl install: Running install from /root/altera/16.0/hld/board/terasic/linux64/l
ibexec
Using kernel source files from /usr/src/kernels/2.6.18-238.el5-x86_64
make: Entering directory `/usr/src/kernels/2.6.18-238.el5-x86_64'
<pre>CC [M] /tmp/opencl_driver_ig5451/aclpci_queue.o</pre>
CC [M] /tmp/opencl_driver_ig5451/aclpci.o
<pre>CC [M] /tmp/opencl_driver_ig5451/aclpci_fileio.o</pre>
CC [M] /tmp/opencl_driver_ig5451/aclpci_dma.o
CC [M] /tmp/opencl_driver_ig5451/aclpci_cvp.o
CC [M] /tmp/opencl_driver_ig5451/aclpci_cmd.o
LD [M] /tmp/opencl_driver_ig5451/aclpci_drv.o
Building modules, stage 2.
MODPOST
CC /tmp/opencl_driver_ig5451/aclpci_drv.mod.o
LD [M] /tmp/opencl_driver_ig5451/aclpci_drv.ko
make: Leaving directory _/usr/src/kernels/2.6.18-238.el5-x86_64'
[root@localhost board]#

Figure 3-6 driver installation

Note: if user don't using the recommended Linux system or different version, recompile the driver is needed. You can compile it by typing

"*cd root/altera/16.0/hld/board/terasic/linux64/driver*" (there are source code, makefile and readme.txt)to *locate at the* driver source code directory and type "*./make_all*" to compile and generate the new driver. Before that, user need to install the kernel related development package matched the current kernel (**kernel-devel** package) via issuing '*yum install kernel-devel*' command.

■ Test 'aocl flash' Command

In the terminal, type "*cd /root/altera/16.0/hld/board/terasic/tests/hello_world/bin*" to go to hello world OpenCL project folder, then type "*aocl flash acl0 hello_world.aocx*" to program **hello_world.aocx** OpenCL image onto the startup configuration flash of DE5-NET.

Before flash programming, the programmer will ask users which startup configuration image area will be used as shown in **Figure 3-7**. This is because DE5-NET provides two startup configuration image areas, called as Factory Image and User Image. Typing '1' to select User Image area is recommended.





root@localhost:~/altera/16.0/hld/board/terasic/tests/hello_world/bin File Edit View Terminal Tabs Help [root@localhost bin]# aocl flash acl0 hello world.aocx aocl flash: Running flash from /root/altera/16.0/hld/board/terasic/linux64/libex ec Please select the flash page where to store your FPGA configure data: [0] Factory Image Location(Address 0x00040000), SW5.2 = "1" (Right Position) User Image Location(Address 0x020C0000), SW5.2 = "0" (Left Position) Enter a digital number 0 or 1 (Or other values to exit the program) followed by pressing the "Enter" key: 1 Flash Programming... Info: Info: Running Quartus Prime Convert programming file Info: Version 16.0.0 Build 211 04/27/2016 SJ Standard Edition Info: Copyright (C) 1991-2016 Altera Corporation. All rights reserved. Info: Your use of Altera Corporation's design tools, logic functions Info: and other software and tools, and its AMPP partner logic Info: functions, and any output files from any of the foregoing Info: (including device programming or simulation files), and any Info: associated documentation or information are expressly subject Info: to the terms and conditions of the Altera Program License

Figure 3-7 Select Flash Page

After selecting the desired flash area, it will take about 20 minutes for flash programming. **Figure 3-8** is the screen shot when flash programming is done successfully.

```
Info (209005): Programming status: programming flash memory at byte address 0x0F
FA0000
Info (209005): Programming status: programming flash memory at byte address 0x0F
FB0000
Info (209005): Programming status: programming flash memory at byte address 0x0F
FC0000
Info (209005): Programming status: programming flash memory at byte address 0x0F
FD0000
Info (209005): Programming status: programming flash memory at byte address 0x0F
FE0000
Info (209005): Programming status: programming flash memory at byte address 0x0F
FE0000
Info (209011): Successfully performed operation(s)
Info (209061): Ended Programmer operation at Fri Nov 7 16:38:39 2016
Info: Quartus II 64-Bit Programmer was successful. 0 errors, 0 warnings
   Info: Peak virtual memory: 2681 megabytes
   Info: Processing ended: Fri Nov 7 16:38:39 2014
    Info: Elapsed time: 00:11:22
    Info: Total CPU time (on all processors): 00:02:19
[root@localhost bin]#
```

Figure 3-8 'aocl flash acl0 hello_world.aocx" successfully





To make sure correct image is used when FPGA boot, please make sure the dip switch SW5.2 on DE5-NTE is located at correct location. If User Image area is selected, the dip switch SW5.2 on the DE5-NET should be move to **left** position as shown in **Figure 3-9**.



Figure 3-9 Set SW5.2 to Left Position (User Image Page)

After flash programming is done successfully and SW5.2 is set to correct position, developers can reboot the PC and check whether the **hello_world** OpenCL image, which is CvP enabled, configures the FPGA successfully when DE5-NET is power on. In the Linux terminal, type "*cd* /*root/altera/16.0/hld/board/terasic/tests/hello_world/bin*" to go to hello_world project folder, then type "*aocl program acl0 hello_world.aocx*" to configure the FPGA with **hello_world.aocx** OpenCL image. If the programming message displays "Program succeed" as shown in **Figure 3-10**, it means the **hello_world** OpenCL image is programmed into the flash correctly and CvP works well.



Figure 3-10 'aocl program acl0 hello_world.aocx" use CvP

3.6 Compile and Test OpenCL Project

This section will show how to compile and run the OpenCL kernel and OpenCL Host Program for the vector_add example project. Developers can use the same procedures to compile and test other OpenCL examples (included in the kit) for DE5-NET.





Compile OpenCL Kernel

In the terminal, type "*cd /root/altera/16.0/hld/board/terasic/tests/vector_add*" to go to **vector_add** project folder, then type "*aoc device\vector_add.cl -o bin\vector_add.aocx --board de5net-a7*" to compile the OpenCL kernel. It will takes about one hour for compiling. After that, the OpenCL image file *vector_add.aocx* is generated. **Figure 3-11** is the screen shot when OpenCL kernel is compiled. For required parameters to compile vectorAdd.cl, please refer to the README.txt that is in the same directory.

The utility **aoc** (Altera SDK for OpenCL Kernel Compiler) is used to compile OpenCL kernel. For detailed usage of **aoc**, please refer to the **Altera SDK for OpenCL Programming Guide**:

http://www.altera.com/literature/hb/opencl-sdk/aocl_programming_guide.pdf

Figure 3-11 'aoc vectorAdd.cl" OpenCL kernel compile

Compile Host Program

In the terminal, type "*cd*/*root/altera*/16.0/*hld/board/terasic/tests/vector_add*" and then type "*make*" to compile the host program.

When build is successfully, you will see successful message as show in **Figure 3-12**. The execute file is generate in the same directory which named bin.

26

	r	oot@l	ocalhost	:~/alte	ra/16.	0/hld/board/terasic/tests/vector_add	
<u>F</u> ile	<u>E</u> dit	<u>V</u> iew	Terminal	Ta <u>b</u> s	<u>H</u> elp		
[roo [roo	t@loc t@loc	alhost alhost	vector_ vector_	_add]# _add]#	make 		<u>^</u>
							≡
			minai T		elp		~

Figure 3-12 successful Message for vector_add Host Program build

Test vector_add project

Firstly, In the terminal, type "*cd /root/altera/16.0/hld/board/terasic/tests/vector_add/bin*" to go to the **vector_add** project folder, then type "*aocl program acl0 vector_add.aocx*" to configure FPGA with the OpenCL Image vector_add.aocx.

Then, launch the compiled Host Program to start vector_add execute file for test. In the terminal type "./host". **Figure 3-13** shows the execution is successful.

<pre>root@localhost:~/altera/16.0/hld/board/terasic/tests/vector_add/bin</pre>	X)						
<u>F</u> ile <u>E</u> dit <u>V</u> iew <u>T</u> erminal Ta <u>b</u> s <u>H</u> elp							
<pre>[root@localhost bin]# aocl program acl0 vector_add.aocx</pre>	-						
aocl program: Running reprogram from /root/altera/16.0/hld/board/terasic/linux64							
/libexec							
Start to program the device acl0							
Program succeed.							
[root@localhost bin]# ./host							
Initializing OpenCL							
Platform: Altera SDK for OpenCL							
Using 1 device(s)							
de5net_a7 : Terasic's Preferred Board							
Using AOCX: vector_add.aocx							
Reprogramming device with handle 1							
Launching for device 0 (1000000 elements)							
Time: 8,911 ms							
Kernel time (device 0): 3,449 ms							
Verification: PASS							
[root@localhost bin]# 🗌							
	~						

Figure 3-13 successful Message for "vector_add" test

