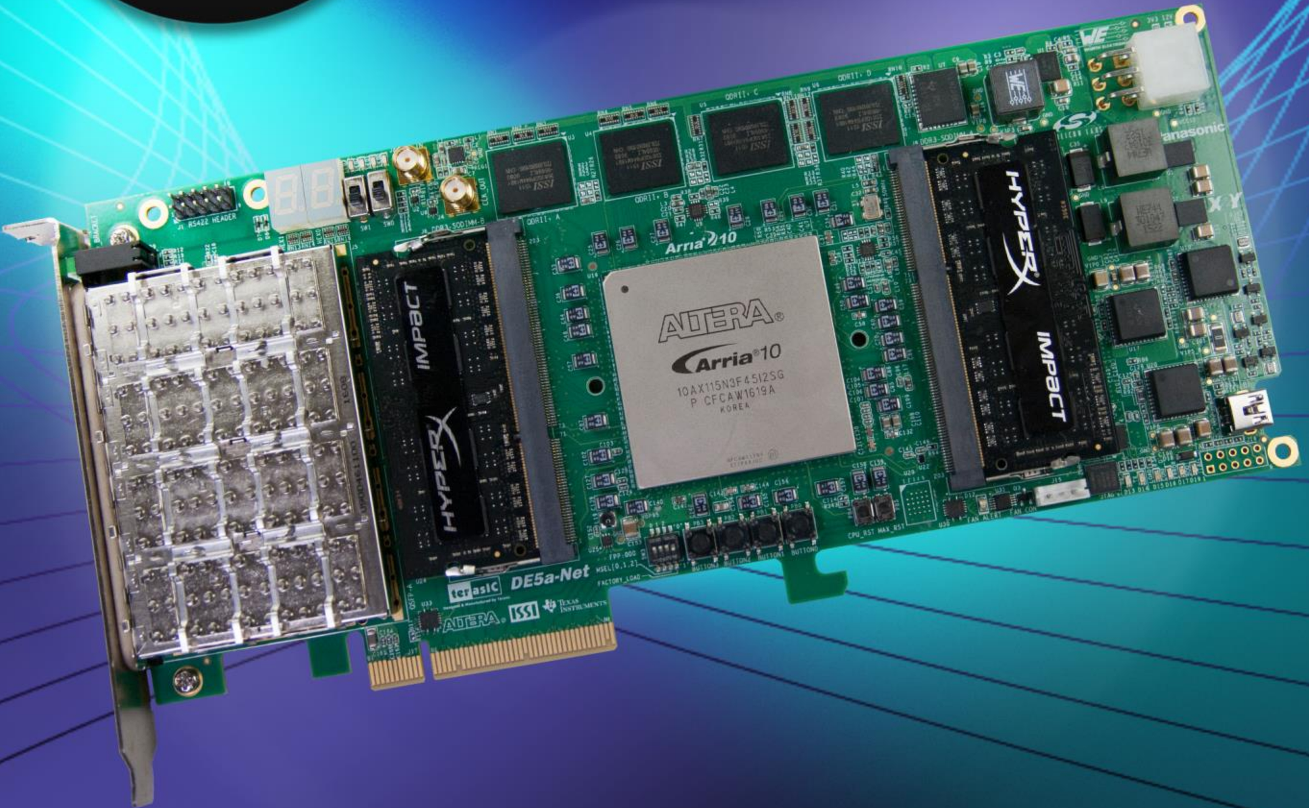
DE5a-Net

OpenCL



Arria 10 GX | Flash | PCI EXPRESS | DDR3 | QDRII+ | QSFP+

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CONTENTS

Chapter 1

DE5a-Net OpenCL

DE5a-Net, an unparalleled and powerful platform for high-speed computation, is now officially also an Intel certified board for Intel's Preferred Board Partner Program for OpenCL. It supports both 64-bit Windows and Linux Operation System. This document will introduce you how to setup OpenCL development environment for DE5a-Net board, and how to compile and execute the example projects for DE5a-Net. Note that OpenCL coding instruction is not introduced in this document, but the user can refer to Intel FPGA SDK for OpenCL Programming Guide for more details.

https://www.altera.com/en_US/pdfs/literature/hb/opencl-sdk/aocl_programming_guide.pdf

1.1 System Requirement

The following items are required to set up OpenCL for DE5a-Net board:

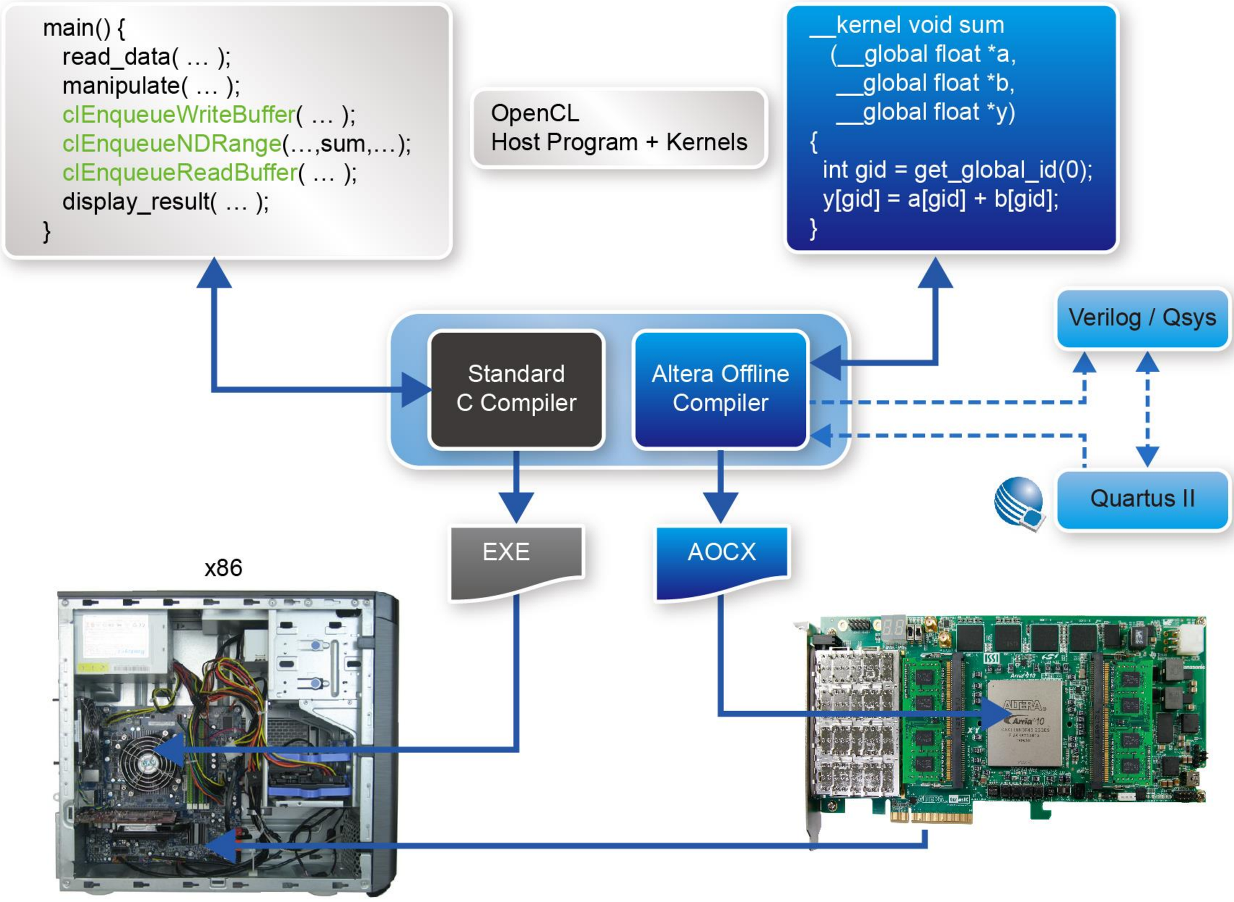
- DE5a-Net Board with two 4GB DDR3-SODIMM installed on two SODIMM port.
- A Host PC with
  - USB Host Port
  - One PCI Express x8/x16 slot with 12V power pin
  - 32GB memory is recommended, 24GB is minimal
  - 2x3 pin 12V Power for DE5a-Net (optional)
- An USB Cable (type A to mini-B)
- 64-bit Windows7/10 or Linux (Redhat 6.5/CentOS 7.0) Installed
- Intel Quartus Prime Pro Edition 17.1.0.240 Installed, **licensed is required**
- Intel FPGA SDK for OpenCL Pro Edition 17.1.0.240 Installed, **license is not required**
- DE5a-Net OpenCL BSP 17.1 Installed
- Visual Studio 2012 C/C++ installed for Windows7/10
- GNU development tools for Linux

Note:

1. Intel FPGA OpenCL only supports 64-bit OS and x86 architecture.
2. We strongly recommend setting the PCIe speed to **Gen3x8** in your PC BIOS for good performance.

1.2 OpenCL Architecture

An OpenCL project is composed of both OpenCL Kernel and Host Program as shown in **Figure 1-1**. OpenCL kernel is compiled with Intel FPGA OpenCL compiler provided by the Altera OpenCL SDK. The Host Program is compiled by Visual Studio C/C++ in Windows or GCC on Linux.



```
main() {
  read_data( … );
  manipulate( … );
  clEnqueueWriteBuffer( … );
  clEnqueueNDRange(…,sum,…);
  clEnqueueReadBuffer( … );
  display_result( … );
}
```

```
__kernel void sum
  (__global float *a,
   __global float *b,
   __global float *y)
{
 int gid = get_global_id(0);
 y[gid] = a[gid] + b[gid];
}
```

Figure 1-1 Intel FPGA OpenCL Architecture

Chapter 2

OpenCL for Windows

This chapter describes how to set up DE5a-Net OpenCL development environment on 64-bit Windows, and how to compile and test the OpenCL examples for DE5a-Net. For more details about Intel FPGA OpenCL started guide, please refer to:

https://www.altera.com/en_US/pdfs/literature/hb/opencl-sdk/aocl_getting_started.pdf

2.1 Software Installation

This section describes where to get the required software for OpenCL.

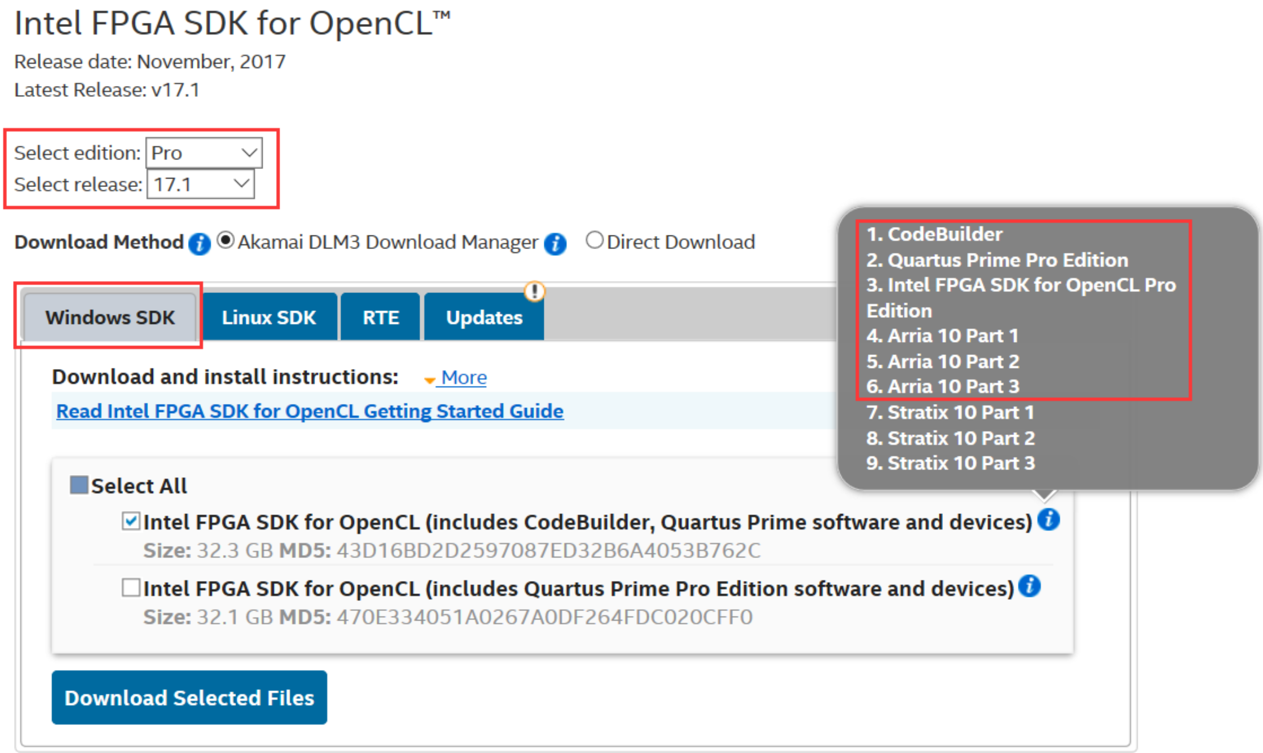
■ Quartus II and OpenCL SDK

Intel Quartus Prime Pro Edition 17.1.0.240 and Intel FPGA SDK for OpenCL Pro Edition 17.1.0.240 can be download from the web site:

http://dl.altera.com/opencl/17.1/?edition=pro

For Quartus II installation, please make sure that the Arria 10 device is included.

Open the link and select the **Windows SDK** table as **Figure 2-1** shows.



Intel FPGA SDK for OpenCL™

Release date: November, 2017
Latest Release: v17.1

Select edition: Pro
Select release: 17.1

Download Method ● Akamai DLM3 Download Manager ○ Direct Download

Download and install instructions: More
Read Intel FPGA SDK for OpenCL Getting Started Guide

1. CodeBuilder
2. Quartus Prime Pro Edition
3. Intel FPGA SDK for OpenCL Pro Edition
4. Arria 10 Part 1
5. Arria 10 Part 2
6. Arria 10 Part 3
7. Stratix 10 Part 1
8. Stratix 10 Part 2
9. Stratix 10 Part 3

Select All

☑ Intel FPGA SDK for OpenCL (includes CodeBuilder, Quartus Prime software and devices)
Size: 32.3 GB **MD5:** 43D16BD2D2597087ED32B6A4053B762C

□ Intel FPGA SDK for OpenCL (includes Quartus Prime Pro Edition software and devices)
Size: 32.1 GB **MD5:** 470E334051A0267A0DF264FDC020CFF0

Figure 2-1 OpenCL Windows SDK Files

■ Visual Studio 2012

If developers don't have Visual Studio C/C++ 2012, they can use the trial version of Visual Studio 2012 Express. The software can be downloaded from the web site:

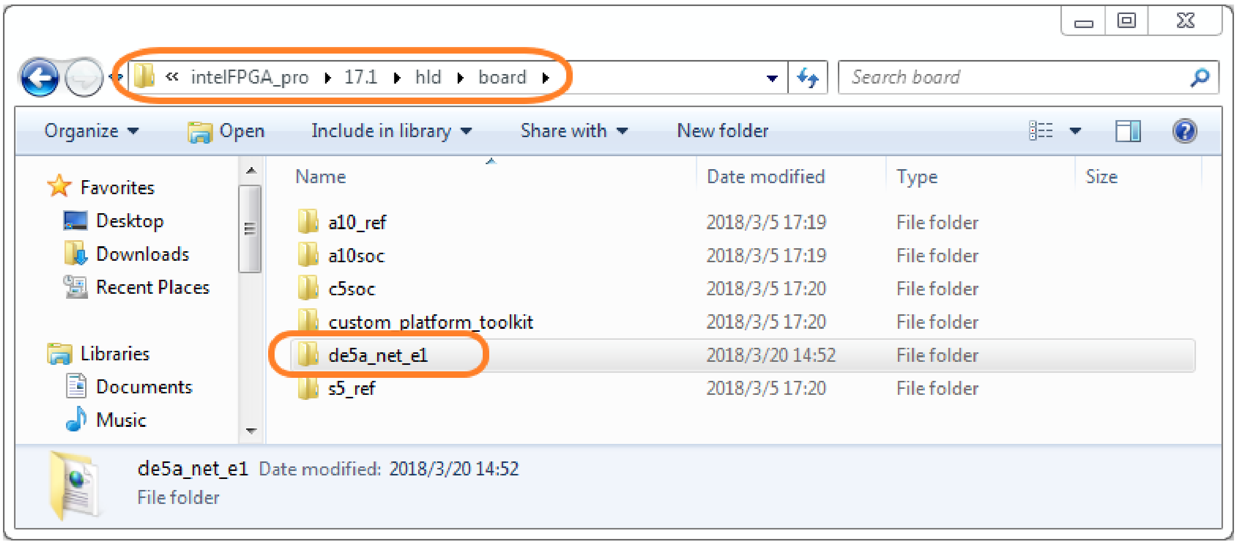
https://www.visualstudio.com/vs/older-downloads/

■ DE5a-Net OpenCL BSP (Board Support Package)

After Quartus II and OpenCL SDK are installed, download the DE5ANET_E1_OpenCL_BSP _17.1.zip DE5a-Net windows BSP from the web site:

http://de5a-net.terasic.com/cd

Then, decompress DE5ANET_E1_OpenCL_BSP_17.1.zip to the "**de5a_net_e1**" folder under the folder "C:\intelFPGA_pro\17.1\hld\board", as shown in **Figure 2-2**, where assumed Quartus II is installed on the folder "C:\ intelFPGA_pro\17.1".



« intelFPGA_pro ▸ 17.1 ▸ hld ▸ board ▸

Name	Date modified	Type	Size
a10_ref	2018/3/5 17:19	File folder	
a10soc	2018/3/5 17:19	File folder	
c5soc	2018/3/5 17:20	File folder	
custom_platform_toolkit	2018/3/5 17:20	File folder	
de5a_net_e1	2018/3/20 14:52	File folder	
s5_ref	2018/3/5 17:20	File folder	

de5a_net_e1 Date modified: 2018/3/20 14:52
File folder

Figure 2-2 DE5a-Net OpenCL BSP Content

For more details about DE5a-Net OpenCL BSP, please refer to the **Table 1**.

Table 1 Windows BSP File

File or Folder	Description
board_env.xml	eXtensible Markup Language (XML) file that describes the Reference Platform to the Intel FPGA SDK for OpenCL.
hardware	Contains the Intel Quartus Prime project templates for the a10gx board variant.
windows64	Contains the MMD library, kernel mode driver, and executable files of the SDK utilities (that is, install, uninstall, flash, program, diagnose) for your 64-bit operating system
tests	Contains some OpenCL Design Examples. The following examples demonstrate how to describe various applications in OpenCL along with their respective host applications, which you can compile and execute on a host with an FPGA board that supports the Intel FPGA SDK for OpenCL.

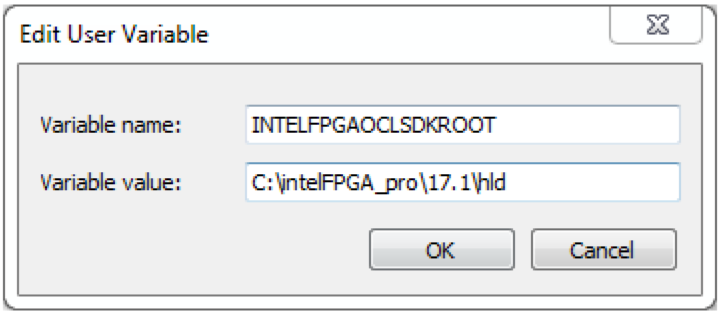
2.2 Environment Configure

Developers need to create and edit some environment variable that Intel FPGA OpenCL SDK can find the kit location of DE5a-Net correctly

Now, here are the procedures to create the required environment variable on Windows 7:

1. Open the **Start** menu and right click on **Computer**. Select **Properties**.
2. Select **Advanced system settings.**
3. In the **Advanced** tab, select **Environment Variables.**
4. Select **New**.
5. In the popup dialog, edit **New User Variable**, type the name in the **Variable name** edit box and type the value in the **Variable value** edit box.

First, edit the environment variable name **ALTERAOCLSDKROOT** to **INTELFPGAOCLSDKROOT**, as shown in **Figure 2-3**.



Variable name: INTELFPGAOCLSDKROOT

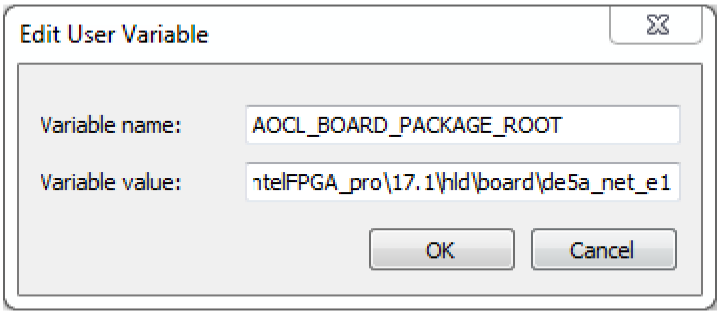
Variable value: C:\intelFPGA_pro\17.1\hld

Figure 2-3 Edit INTELFPGAOCLSDKROOT Environment Variable

Then, create an environment variable **AOCL_BOARD_PACKAGE_ROOT**, and set its value as:

"%INTELFPGAOCLSDKROOT%\board\ de5a_net_e1"

as shown in **Figure 2-4**.



Variable name: AOCL_BOARD_PACKAGE_ROOT

Variable value: ntelFPGA_pro\17.1\hld\board\de5a_net_e1

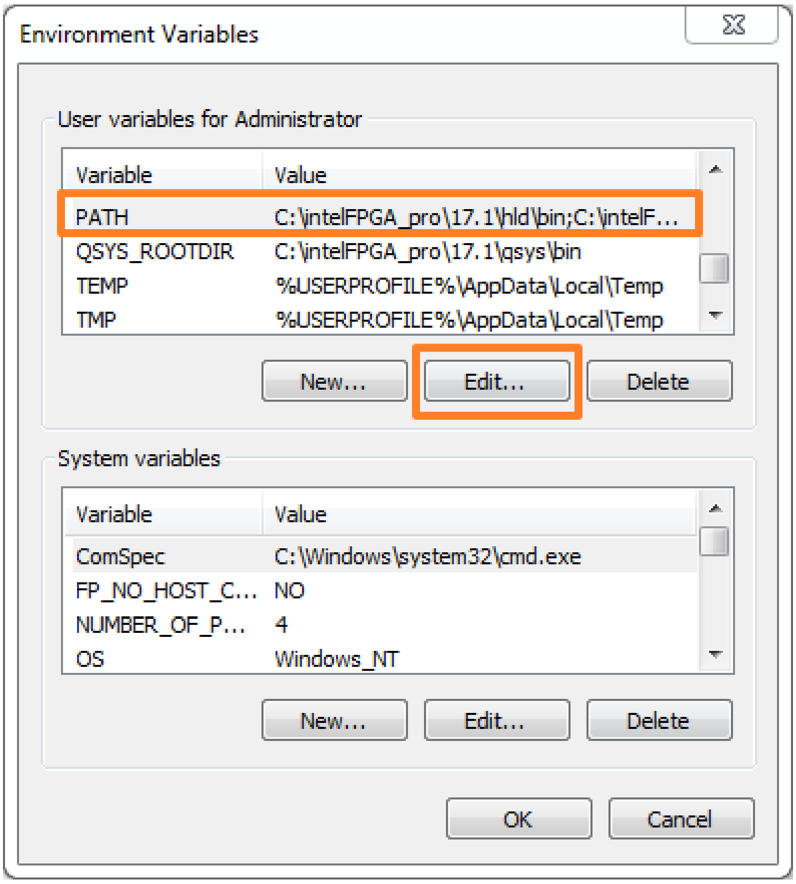
Figure 2-4 Setup AOCL_BOARD_PACKAGE_ROOT Environment Variable

Also, append

"%QUARTUS_ROOTDIR%\bin64 " and

"**%QUARTUS_ROOTDIR%\qsys\bin**" and
"**%INTELFPGAOCLSDKROOT%\bin**" and
"**%INTELFPGAOCLSDKROOT%\windows64\bin**" and
"**%AOCL_BOARD_PACKAGE_ROOT%\windows64\bin**"

into the **PATH** environment variable as shown in **Figure 2-5** and **Figure 2-6**, so the OpenCL SDK can find the binary file provided by OpenCL BSP.



Environment Variables

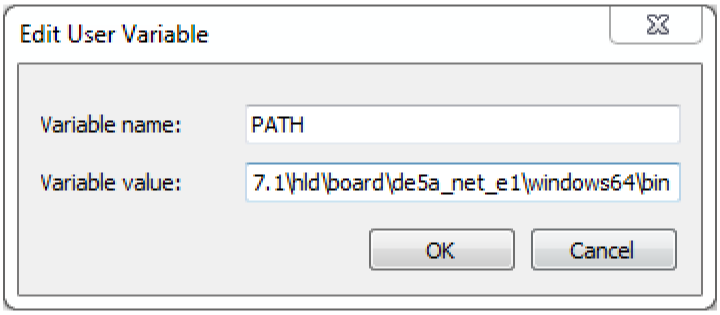
User variables for Administrator

Variable	Value
PATH	C:\intelFPGA_pro\17.1\hld\bin;C:\intelF...
QSYS_ROOTDIR	C:\intelFPGA_pro\17.1\qsys\bin
TEMP	%USERPROFILE%\AppData\Local\Temp
TMP	%USERPROFILE%\AppData\Local\Temp

System variables

Variable	Value
ComSpec	C:\Windows\system32\cmd.exe
FP_NO_HOST_C...	NO
NUMBER_OF_P...	4
OS	Windows_NT

Figure 2-5 Select "Path" and click "Edit" bottom



Edit User Variable

Variable name: PATH

Variable value: 7.1\hld\board\de5a_net_e1\windows64\bin

Figure 2-6 Edit PATH environment variable

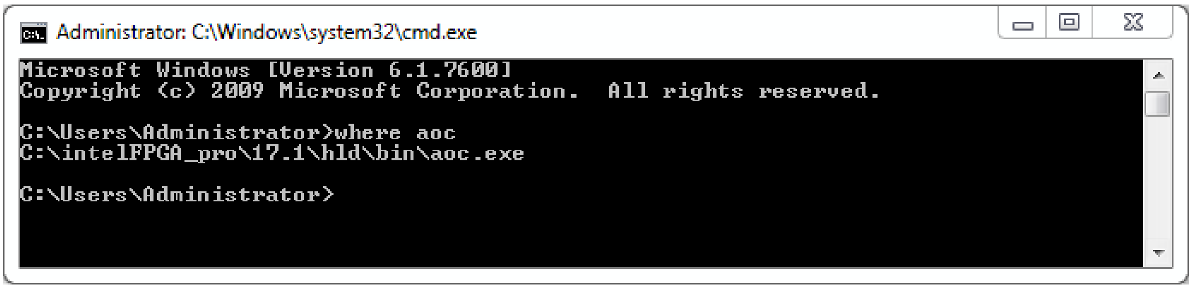
2.3 OpenCL Environment Verify

This section will show how to make sure the OpenCL environment is setup correctly. Firstly, please open **Command Prompt** windows by click Windows **Start** button, clicking **All Programs**, clicking **Accessories**, and then click **Command Prompt**.

Note: In Windows 10 OS, please open Command Prompt windows by click Windows Start button, clicking All Programs, clicking Windows System, and then click Command Prompt.

■ Target AOCL

In **Command Prompt** window, type "**where aoc**" command, and make sure the path of the "**aoc.exe**" is listed as shown in **Figure 2-7**.

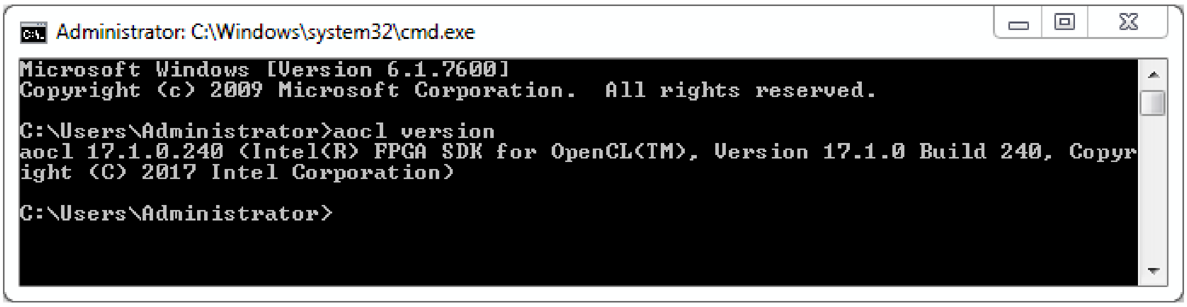


```
Microsoft Windows [Version 6.1.7600]
Copyright (c) 2009 Microsoft Corporation.  All rights reserved.

C:\Users\Administrator>where aoc
C:\intelFPGA_pro\17.1\hld\bin\aoc.exe

C:\Users\Administrator>
```

Figure 2-7 where aoc

■ Target SDK Version

In **Command Prompt** window, type "**aocl version**" command, and make sure the version of the OpenCL SDK is listed as shown in **Figure 2-8**.

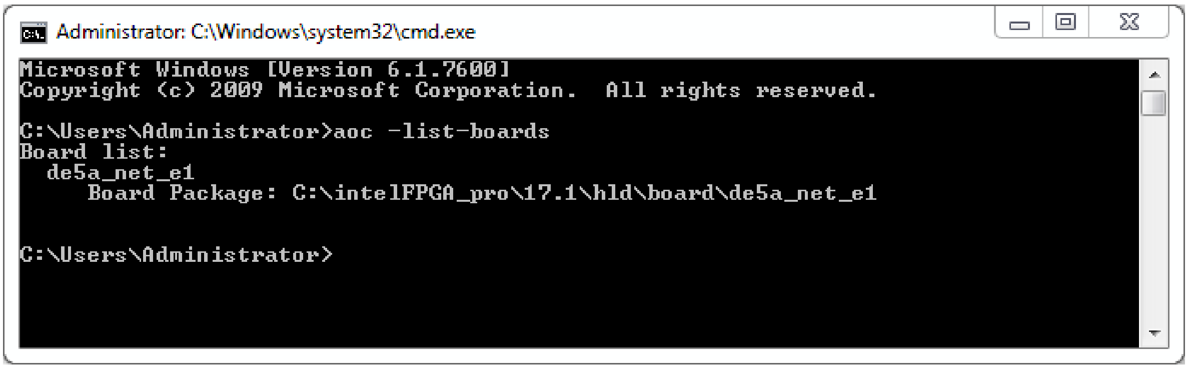


```
Microsoft Windows [Version 6.1.7600]
Copyright (c) 2009 Microsoft Corporation.  All rights reserved.

C:\Users\Administrator>aocl version
aocl 17.1.0.240 (Intel(R) FPGA SDK for OpenCL(TM), Version 17.1.0 Build 240, Copyr
ight (C) 2017 Intel Corporation)

C:\Users\Administrator>
```

Figure 2-8 Version of OpenCL SDK

■ Target Board

In **Command Prompt** window, type "**aoc -list-boards**" command, and make sure "**de5a_net_e1**" is listed in **Board list** as shown in Figure 2-9.



Administrator: C:\Windows\system32\cmd.exe

```
Microsoft Windows [Version 6.1.7600]
Copyright (c) 2009 Microsoft Corporation.  All rights reserved.

C:\Users\Administrator>aoc -list-boards
Board list:
  de5a_net_e1
     Board Package: C:\intelFPGA_pro\17.1\hld\board\de5a_net_e1


C:\Users\Administrator>
```

Figure 2-9 ‘de5a_net_e1’ is listed in Board list

For more information about the **aoc** and **aocl**, refer to the ‘**aoc -h**’ and ‘**aocl help**’ command.

2.4 Initializing the FPGA for using with OpenCL

■ Board Setup

To use the DE5a-Net Arria 10 FPGA Development Kit with the Intel FPGA SDK for OpenCL, you must follow the below procedures to set up DE5a-Net board on your PC as shown in **Figure 2-10.**

1. Make sure your PC is powered off.
2. Insert DE5a-Net board into PCI Express x8 or x16 slot.
3. Connect PC's 12V PCI Express 6-pin power source to the DE5a-Net (if there's not, ignore this step).
4. Connect PC's USB port to DE5a-Net mini USB port using an USB cable.

Note, the USB cable can be removed later if OpenCL code had been programmed to the startup configuration flash of DE5a-Net by '**aocl flash**' command.

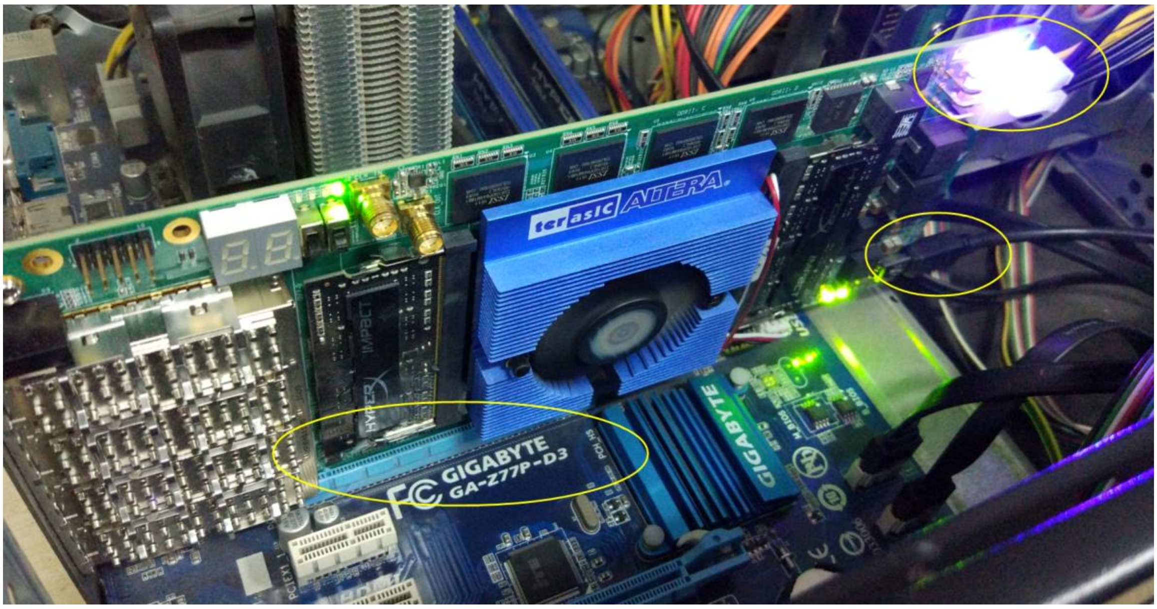
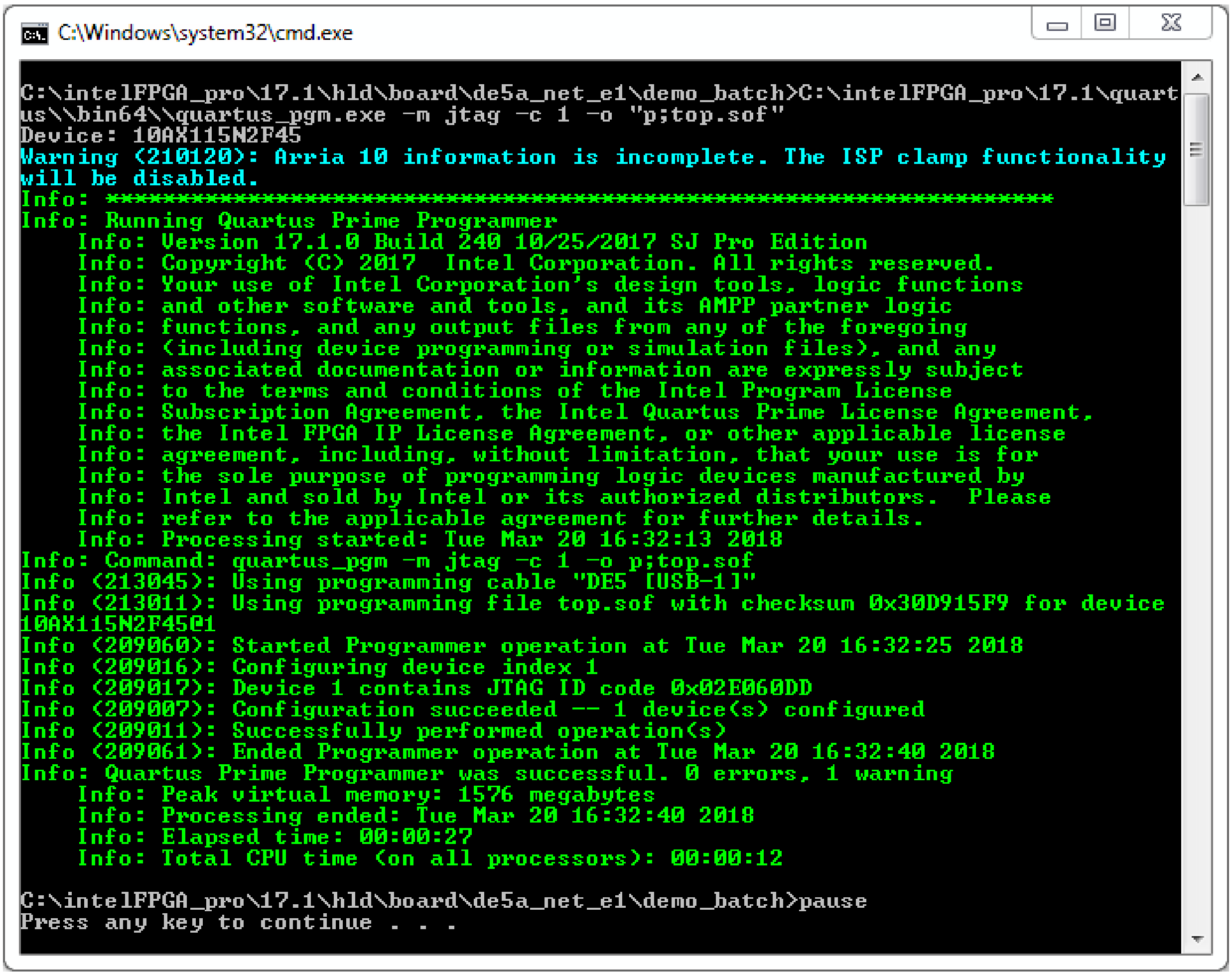


Figure 2-10 Setup DE5a-Net board on PC

■ Bring up the FPGA Board

Before you can use the DE5a-Net Arria 10 FPGA Development Kit with OpenCL, you must initialize the board with an OpenCL image. Without this image, the board host operating system does not recognize the PCIe card and the Intel FPGA OpenCL compiler cannot find the device.

Program the FPGA on your DE5a-Net Arria 10 FPGA Development Kit with the **top.sof** file by running the **test.bat** file in **bringup** folder as shown in Figure 2-11.



```
C:\intelFPGA_pro\17.1\hld\board\de5a_net_e1\demo_batch>C:\intelFPGA_pro\17.1\quart
us\\bin64\\quartus_pgm.exe -m jtag -c 1 -o "p;top.sof"
Device: 10AX115N2F45
Warning (210120): Arria 10 information is incomplete. The ISP clamp functionality
will be disabled.
Info: *******************************************************************
Info: Running Quartus Prime Programmer
    Info: Version 17.1.0 Build 240 10/25/2017 SJ Pro Edition
    Info: Copyright (C) 2017  Intel Corporation. All rights reserved.
    Info: Your use of Intel Corporation's design tools, logic functions
    Info: and other software and tools, and its AMPP partner logic
    Info: functions, and any output files from any of the foregoing
    Info: (including device programming or simulation files), and any
    Info: associated documentation or information are expressly subject
    Info: to the terms and conditions of the Intel Program License
    Info: Subscription Agreement, the Intel Quartus Prime License Agreement,
    Info: the Intel FPGA IP License Agreement, or other applicable license
    Info: agreement, including, without limitation, that your use is for
    Info: the sole purpose of programming logic devices manufactured by
    Info: Intel and sold by Intel or its authorized distributors.  Please
    Info: refer to the applicable agreement for further details.
    Info: Processing started: Tue Mar 20 16:32:13 2018
Info: Command: quartus_pgm -m jtag -c 1 -o p;top.sof
Info (213045): Using programming cable "DE5 [USB-1]"
Info (213011): Using programming file top.sof with checksum 0x30D915F9 for device
10AX115N2F45@1
Info (209060): Started Programmer operation at Tue Mar 20 16:32:25 2018
Info (209016): Configuring device index 1
Info (209017): Device 1 contains JTAG ID code 0x02E060DD
Info (209007): Configuration succeeded -- 1 device(s) configured
Info (209011): Successfully performed operation(s)
Info (209061): Ended Programmer operation at Tue Mar 20 16:32:40 2018
Info: Quartus Prime Programmer was successful. 0 errors, 1 warning
    Info: Peak virtual memory: 1576 megabytes
    Info: Processing ended: Tue Mar 20 16:32:40 2018
    Info: Elapsed time: 00:00:27
    Info: Total CPU time (on all processors): 00:00:12

C:\intelFPGA_pro\17.1\hld\board\de5a_net_e1\demo_batch>pause
Press any key to continue . . .
```

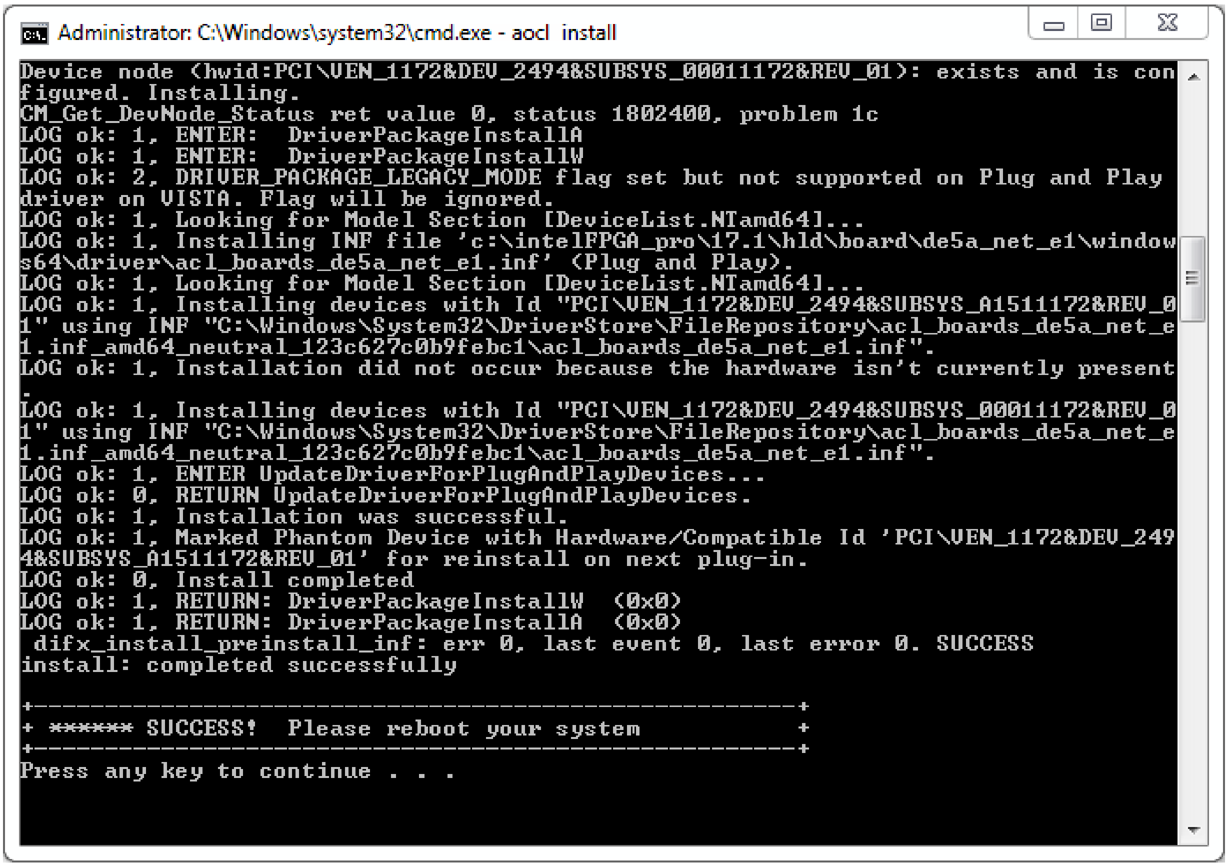
Figure 2-11 Bring up the FPGA board

Perform a soft reboot (sometimes called a warm reboot) of your host system causes your host system to recognize the DE5a-Net Arria 10 FPGA Development Kit PCIe card.

■ Driver Installation

Your system must recognize the card so that the Intel FPGA SDK for OpenCL driver can be loaded. The **install** utility is used install the kernel driver on the host computer. Users of the Intel FPGA SDK for OpenCL only need to install the driver once, after that the driver should be automatically loaded each time the machine reboots.

In **Command Prompt** window, type '**aocl install**' to install the driver as shown in Figure 2-12. Note that users need to have administrator privileges to install the driver.

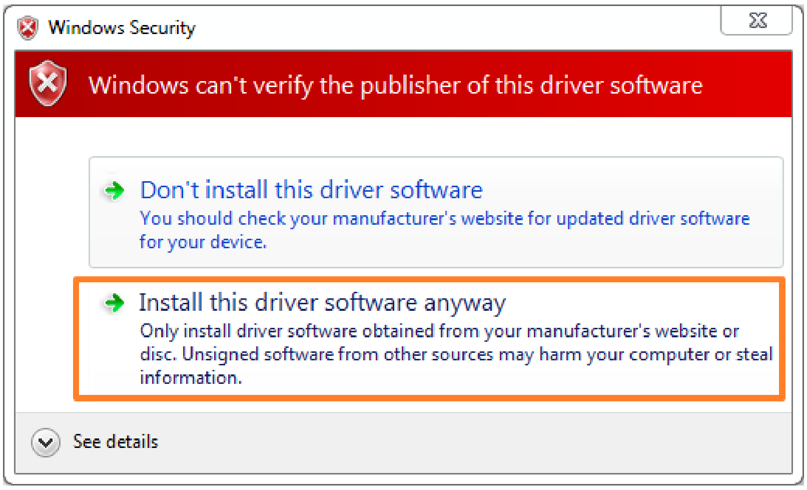


Administrator: C:\Windows\system32\cmd.exe - aocl install

```
Device node (hwid:PCI\VEN_1172&DEV_2494&SUBSYS_00011172&REV_01): exists and is con
figured. Installing.
CM_Get_DevNode_Status ret value 0, status 1802400, problem 1c
LOG ok: 1, ENTER:  DriverPackageInstallA
LOG ok: 1, ENTER:  DriverPackageInstallW
LOG ok: 2, DRIVER_PACKAGE_LEGACY_MODE flag set but not supported on Plug and Play
driver on VISTA. Flag will be ignored.
LOG ok: 1, Looking for Model Section [DeviceList.NTamd64]...
LOG ok: 1, Installing INF file 'c:\intelFPGA_pro\17.1\hld\board\de5a_net_e1\window
s64\driver\acl_boards_de5a_net_e1.inf' (Plug and Play).
LOG ok: 1, Looking for Model Section [DeviceList.NTamd64]...
LOG ok: 1, Installing devices with Id "PCI\VEN_1172&DEV_2494&SUBSYS_A1511172&REV_0
1" using INF "C:\Windows\System32\DriverStore\FileRepository\acl_boards_de5a_net_e
1.inf_amd64_neutral_123c627c0b9febc1\acl_boards_de5a_net_e1.inf".
LOG ok: 1, Installation did not occur because the hardware isn't currently present
.
LOG ok: 1, Installing devices with Id "PCI\VEN_1172&DEV_2494&SUBSYS_00011172&REV_0
1" using INF "C:\Windows\System32\DriverStore\FileRepository\acl_boards_de5a_net_e
1.inf_amd64_neutral_123c627c0b9febc1\acl_boards_de5a_net_e1.inf".
LOG ok: 1, ENTER UpdateDriverForPlugAndPlayDevices...
LOG ok: 0, RETURN UpdateDriverForPlugAndPlayDevices.
LOG ok: 1, Installation was successful.
LOG ok: 1, Marked Phantom Device with Hardware/Compatible Id 'PCI\VEN_1172&DEV_249
4&SUBSYS_A1511172&REV_01' for reinstall on next plug-in.
LOG ok: 0, Install completed
LOG ok: 1, RETURN: DriverPackageInstallW  (0x0)
LOG ok: 1, RETURN: DriverPackageInstallA  (0x0)
 difx_install_preinstall_inf: err 0, last event 0, last error 0. SUCCESS
install: completed successfully

+--------------------------------------------------------+
+ ****** SUCCESS!  Please reboot your system             +
+--------------------------------------------------------+
Press any key to continue . . .
```

Figure 2-12 driver installation

For windows7 x64, If it pops dialog"**Windows Security**"during the installation process, please choose "**Install this driver software anyway**" as shown in **Figure 2-13** and go on.



Windows Security

Windows can't verify the publisher of this driver software

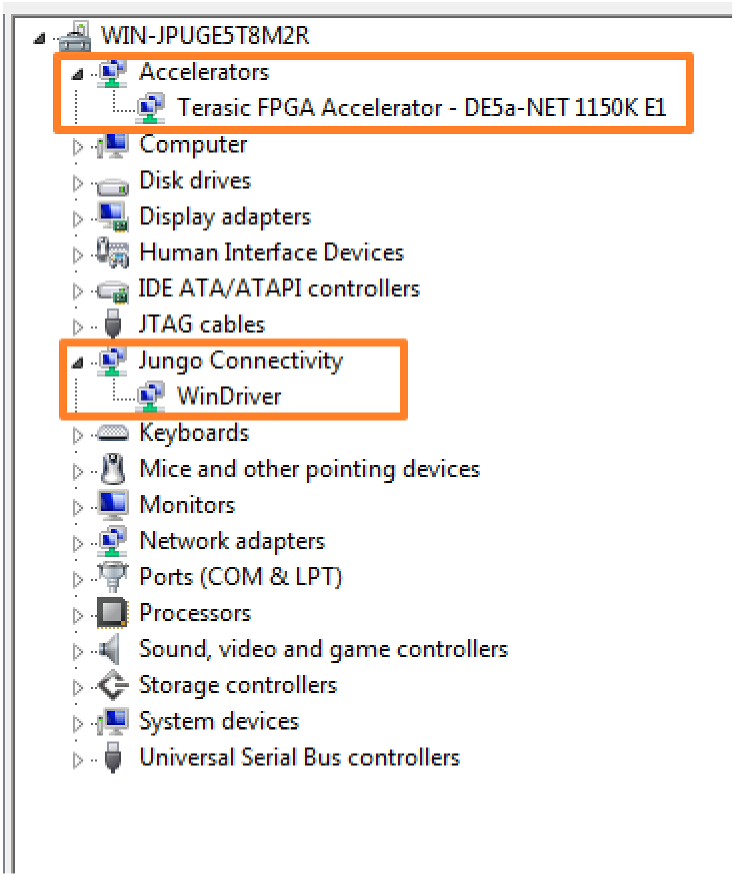
Don't install this driver software
You should check your manufacturer's website for updated driver software for your device.

Install this driver software anyway
Only install driver software obtained from your manufacturer's website or disc. Unsigned software from other sources may harm your computer or steal information.

See details

Figure 2-13 windows security

When the installation is successful, **Jungo WinDriver** and FPGA **Accelerator** board can be found in the PC Device Manage as shown in **Figure 2-14**.



WIN-JPUGE5T8M2R
- Accelerators
  - Terasic FPGA Accelerator - DE5a-NET 1150K E1
- Computer
- Disk drives
- Display adapters
- Human Interface Devices
- IDE ATA/ATAPI controllers
- JTAG cables
- Jungo Connectivity
  - WinDriver
- Keyboards
- Mice and other pointing devices
- Monitors
- Network adapters
- Ports (COM & LPT)
- Processors
- Sound, video and game controllers
- Storage controllers
- System devices
- Universal Serial Bus controllers

Figure 2-14 Driver Installation Success

For **windows10** x64, please refer to the of Chapter 4 **Appendix**.

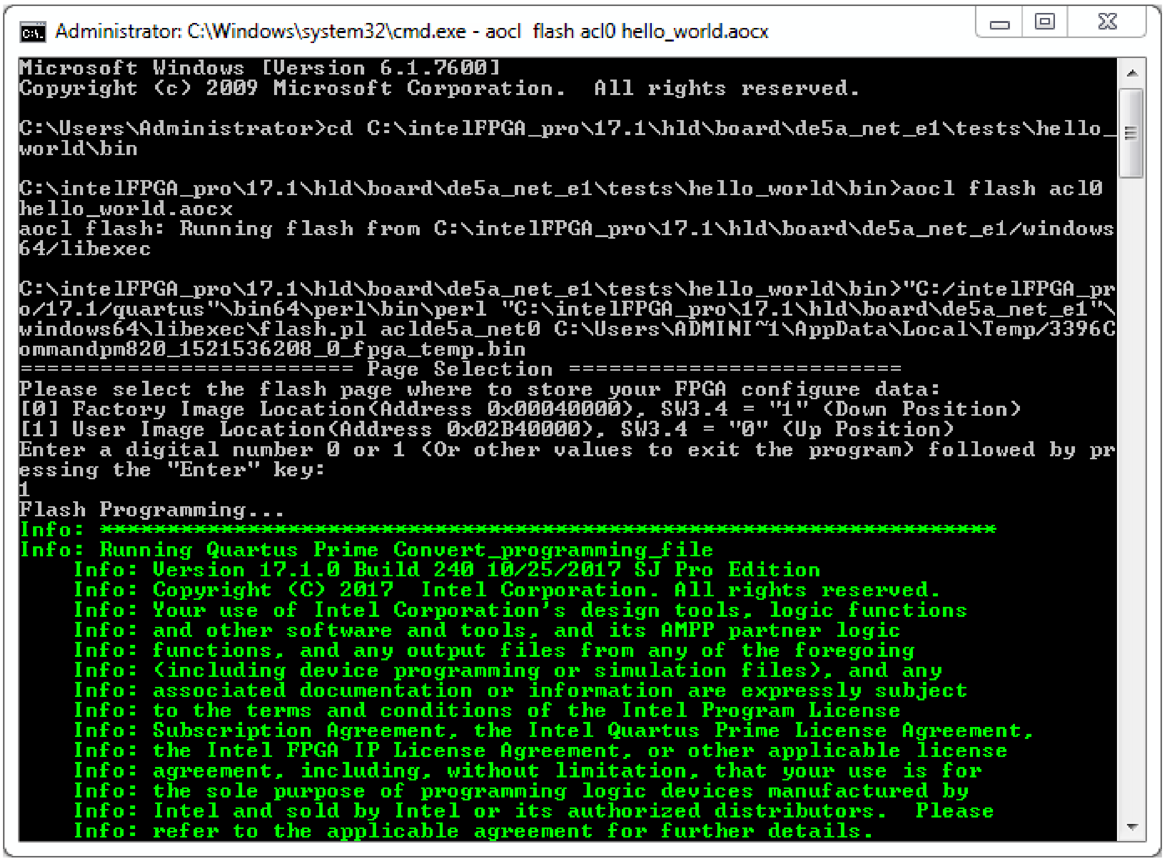
■ ‘aocl flash’ program

The **flash** utility configures the power-on image for the FPGA using the specified **aocx** file. Calling into the MMD library implements the flash utility.

In **Command Prompt** window, type *“cd C:\intelFPGA\17.1\hld\board\de5a_net_e1\tests\hello_world\bin”* to go to hello world OpenCL project folder.

Then type “**aocl flash acl0 hello_world.aocx**” to write **hello_world.aocx** OpenCL image onto the startup configuration flash of DE5a-Net.

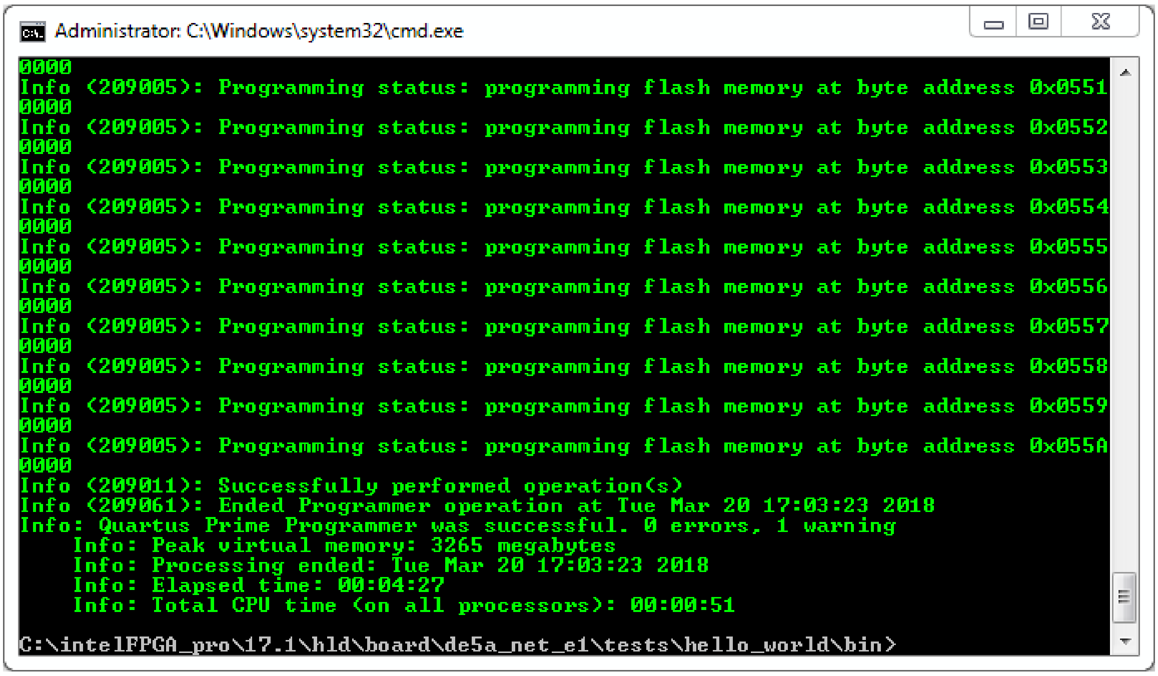
Before flash programming, the programmer will ask users which startup configuration image area will be used as shown in Figure 2-15. This is because DE5a-Net provides two startup configuration image areas, called as Factory Image and User Image. We recommend users to key in ‘1’ to select User Image area.


Administrator: C:\Windows\system32\cmd.exe - aocl flash acl0 hello_world.aocx

```
Microsoft Windows [Version 6.1.7600]
Copyright (c) 2009 Microsoft Corporation.  All rights reserved.

C:\Users\Administrator>cd C:\intelFPGA_pro\17.1\hld\board\de5a_net_e1\tests\hello_
world\bin

C:\intelFPGA_pro\17.1\hld\board\de5a_net_e1\tests\hello_world\bin>aocl flash acl0
hello_world.aocx
aocl flash: Running flash from C:\intelFPGA_pro\17.1\hld\board\de5a_net_e1/windows
64/libexec

C:\intelFPGA_pro\17.1\hld\board\de5a_net_e1\tests\hello_world\bin>"C:/intelFPGA_pr
o/17.1/quartus"\bin64\perl\bin\perl "C:\intelFPGA_pro\17.1\hld\board\de5a_net_e1"\
windows64\libexec\flash.pl acl de5a_net0 C:\Users\ADMINI~1\AppData\Local\Temp/3396C
ommandpm820_1521536208_0_fpga_temp.bin
========================= Page Selection =========================
Please select the flash page where to store your FPGA configure data:
[0] Factory Image Location(Address 0x00040000), SW3.4 = "1" (Down Position)
[1] User Image Location(Address 0x02B40000), SW3.4 = "0" (Up Position)
Enter a digital number 0 or 1 (Or other values to exit the program) followed by pr
essing the "Enter" key:
1
Flash Programming...
Info: *******************************************************************
Info: Running Quartus Prime Convert_programming_file
    Info: Version 17.1.0 Build 240 10/25/2017 SJ Pro Edition
    Info: Copyright (C) 2017  Intel Corporation. All rights reserved.
    Info: Your use of Intel Corporation's design tools, logic functions
    Info: and other software and tools, and its AMPP partner logic
    Info: functions, and any output files from any of the foregoing
    Info: (including device programming or simulation files), and any
    Info: associated documentation or information are expressly subject
    Info: to the terms and conditions of the Intel Program License
    Info: Subscription Agreement, the Intel Quartus Prime License Agreement,
    Info: the Intel FPGA IP License Agreement, or other applicable license
    Info: agreement, including, without limitation, that your use is for
    Info: the sole purpose of programming logic devices manufactured by
    Info: Intel and sold by Intel or its authorized distributors.  Please
    Info: refer to the applicable agreement for further details.
```

Figure 2-15 Select Flash Page

After users select desired flash area, it will take about 8 minutes for flash programming. Figure 2-16 is the screen shot when flash programming is done successfully.



```
0000
Info (209005): Programming status: programming flash memory at byte address 0x0551
0000
Info (209005): Programming status: programming flash memory at byte address 0x0552
0000
Info (209005): Programming status: programming flash memory at byte address 0x0553
0000
Info (209005): Programming status: programming flash memory at byte address 0x0554
0000
Info (209005): Programming status: programming flash memory at byte address 0x0555
0000
Info (209005): Programming status: programming flash memory at byte address 0x0556
0000
Info (209005): Programming status: programming flash memory at byte address 0x0557
0000
Info (209005): Programming status: programming flash memory at byte address 0x0558
0000
Info (209005): Programming status: programming flash memory at byte address 0x0559
0000
Info (209005): Programming status: programming flash memory at byte address 0x055A
0000
Info (209011): Successfully performed operation(s)
Info (209061): Ended Programmer operation at Tue Mar 20 17:03:23 2018
Info: Quartus Prime Programmer was successful. 0 errors, 1 warning
    Info: Peak virtual memory: 3265 megabytes
    Info: Processing ended: Tue Mar 20 17:03:23 2018
    Info: Elapsed time: 00:04:27
    Info: Total CPU time (on all processors): 00:00:51

C:\intelFPGA_pro\17.1\hld\board\de5a_net_e1\tests\hello_world\bin>
```

Figure 2-16 Aocl Flash Successfully

To make sure a correct image is used when FPGA boots up, please make sure the dip switch **SW3.4** on DE5a-Net is changed to the correct location. If a User Image area is selected, the dip switch SW3.4 on the DE5a-Net should be moved to **Up** position as shown in Figure 2-17.

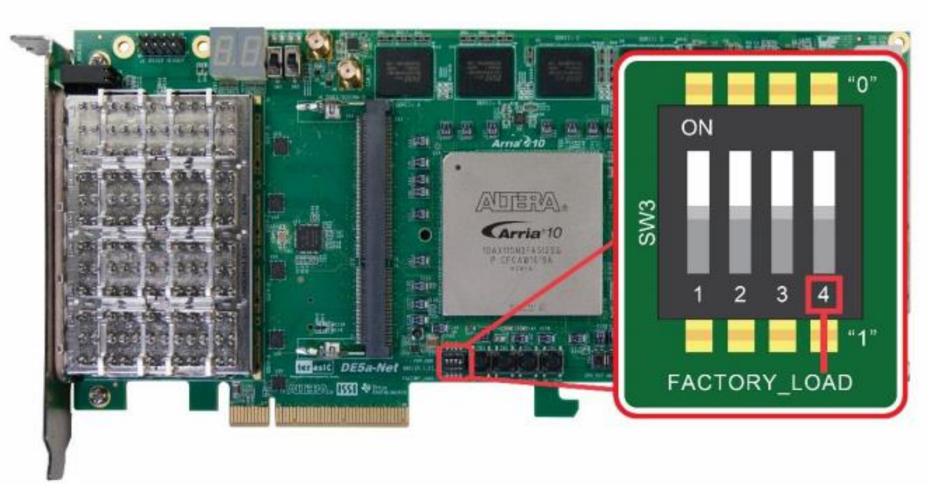


Figure 2-17 Set SW3.4 to Up Position (User Image Page)

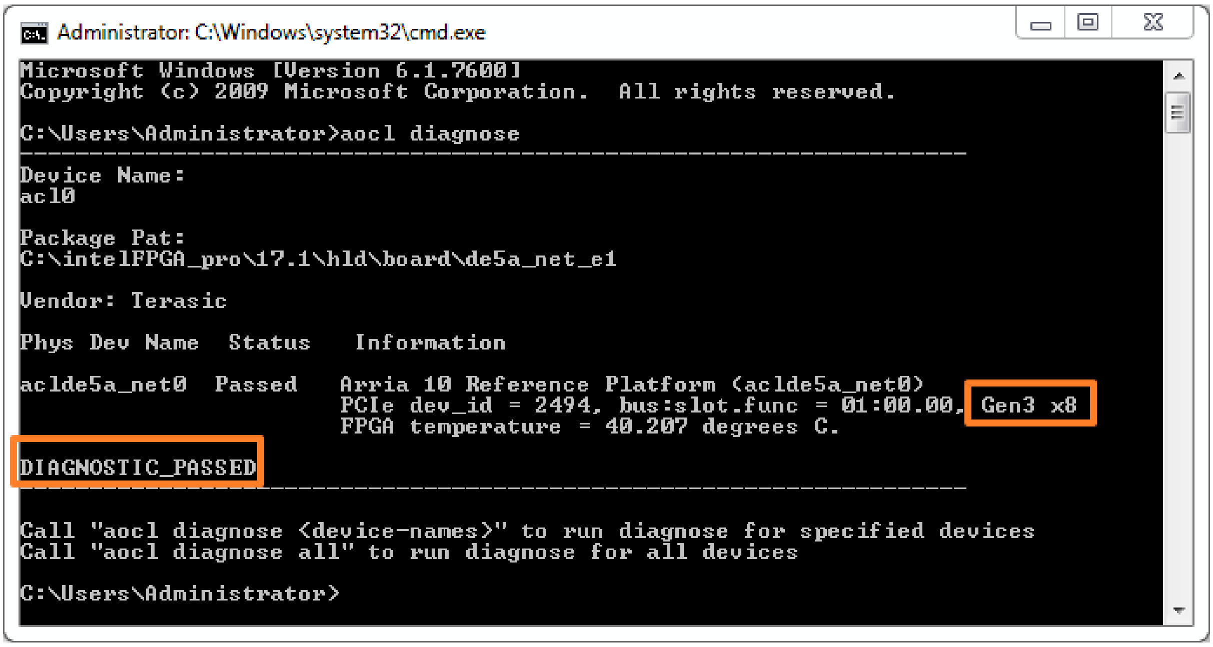
After flash programming is done successfully and SW3.4 is set to correct position, **developers must power off DE5a-Net board, then turn it back on, and restart the PC.**

2.5 OpenCL Runtime Verify

■ Test 'aocl diagnose' Command

The **diagnose** utility reports device information and identifies issues. The diagnose utility first verifies the installation of the kernel driver and returns the overall information of all the devices installed in a host machine.

In **Command Prompt** window, type "**aocl diagnose**" to check if the initialization completed successfully. If successful, the programming message displays "**DIAGNOSTIC_PASSED**" as shown in Figure 2-18.



Administrator: C:\Windows\system32\cmd.exe

```
Microsoft Windows [Version 6.1.7600]
Copyright (c) 2009 Microsoft Corporation.  All rights reserved.

C:\Users\Administrator>aocl diagnose
--------------------------------------------------------------------
Device Name:
acl0

Package Pat:
C:\intelFPGA_pro\17.1\hld\board\de5a_net_e1

Vendor: Terasic

Phys Dev Name  Status   Information

aclde5a_net0  Passed   Arria 10 Reference Platform (aclde5a_net0)
                       PCIe dev_id = 2494, bus:slot.func = 01:00.00, Gen3 x8
                       FPGA temperature = 40.207 degrees C.

DIAGNOSTIC_PASSED
--------------------------------------------------------------------

Call "aocl diagnose <device-names>" to run diagnose for specified devices
Call "aocl diagnose all" to run diagnose for all devices

C:\Users\Administrator>
```

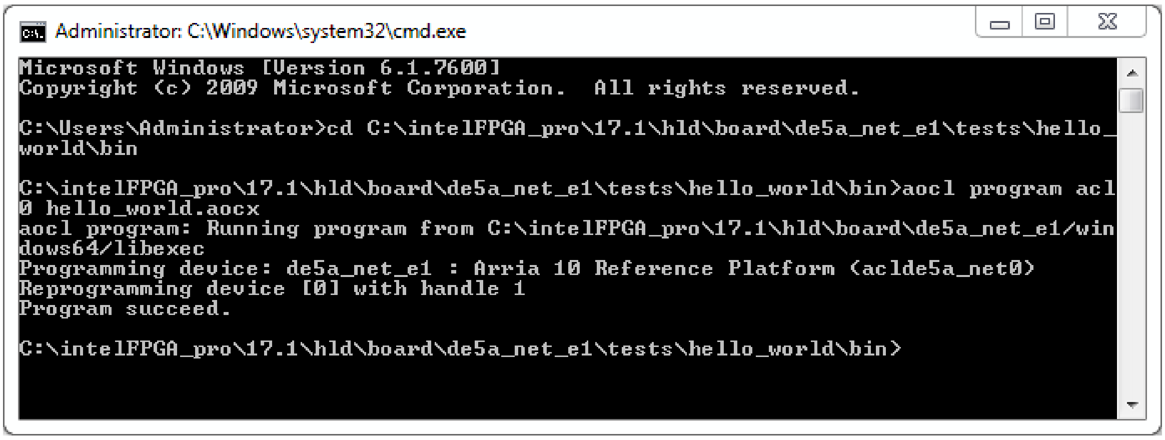
Figure 2-18 "aocl diagnose" Messages

Note: It is strongly recommended that users set the PCIe speed at Gen 3 in the BIOS on the host PC, so that the DE5a-Net negotiates with the host PC at Gen3 as the link speed. If your PC supports PCIe Gen3x8, but it gets incorrect detected information, you can modify the PCIe settings in the BIOS, and reboot.

■ Test 'aocl program' Command

The **program** utility programs the board with the specified **aocx** file. Check whether the **hello_world** OpenCL image configures the FPGA successfully. In **Command Prompt** window, type *"cd C:\intelFPGA_pro\17.1\hld\board\de5a_net_e1\tests\hello_world\bin"* to go to **bin** folder, then type "**aocl program acl0 hello_world.aocx**" to configure the FPGA with **hello_world.aocx**

OpenCL image. If the programming message displays “Program succeed” as shown in **Figure 2-19**, it means the **hello_world** OpenCL image is programmed into the FPGA successfully.



```
Microsoft Windows [Version 6.1.7600]
Copyright (c) 2009 Microsoft Corporation.  All rights reserved.

C:\Users\Administrator>cd C:\intelFPGA_pro\17.1\hld\board\de5a_net_e1\tests\hello_
world\bin

C:\intelFPGA_pro\17.1\hld\board\de5a_net_e1\tests\hello_world\bin>aocl program acl
0 hello_world.aocx
aocl program: Running program from C:\intelFPGA_pro\17.1\hld\board\de5a_net_e1/win
dows64/libexec
Programming device: de5a_net_e1 : Arria 10 Reference Platform (aclde5a_net0)
Reprogramming device [0] with handle 1
Program succeed.

C:\intelFPGA_pro\17.1\hld\board\de5a_net_e1\tests\hello_world\bin>
```

Figure 2-19 Aocl Program Successfully

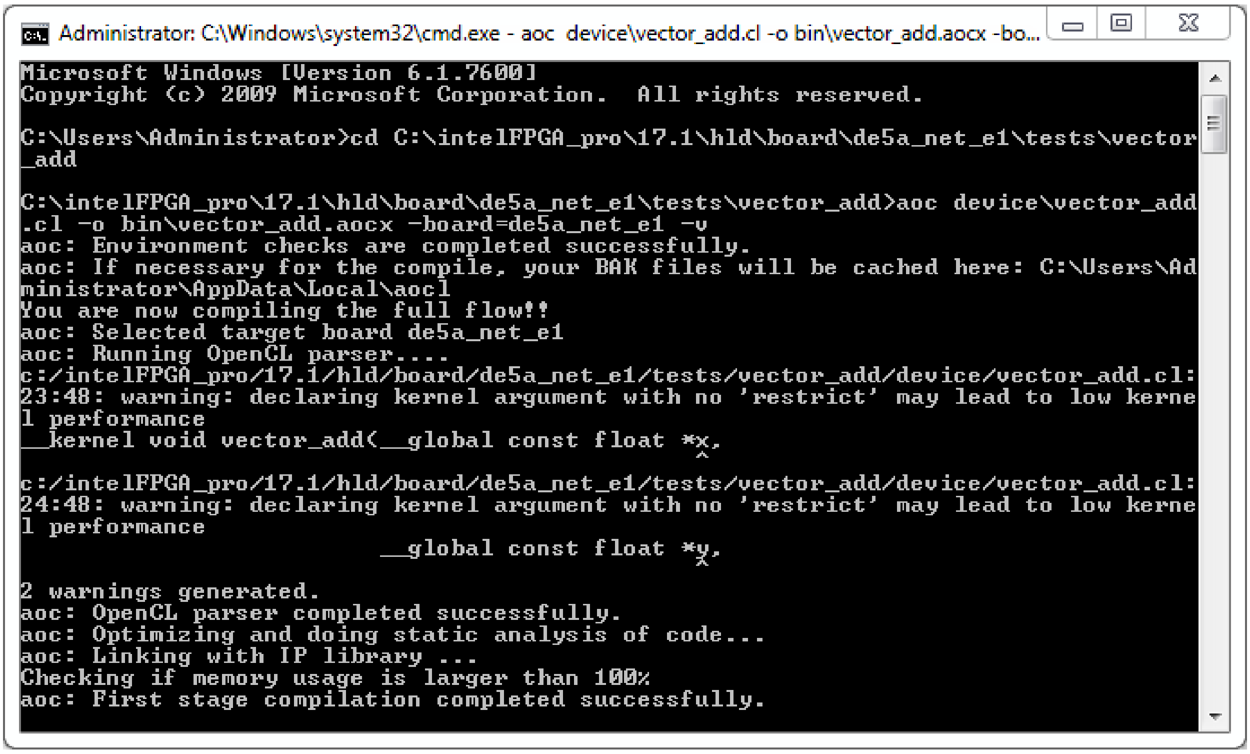
2.6 Compile and Test OpenCL Project

This section will show how to compile and test OpenCL kernel and OpenCL Host Program for the **vector_add** project. Developers can use the same procedures to compile and test other OpenCL examples for DE5a-Net.

■ Compile OpenCL Kernel

The utility **aoc** (Altera SDK for OpenCL Kernel Compiler) is used to compile the OpenCL kernel. In **Command Prompt** window, type *"cd C:\intelFPGA_pro\17.1\hld\board\de5a_net_e1\tests\vector_add"* to go to **vector_add** project folder.
then type "**aoc device\vector_add.cl -o bin\vector_add.aocx -board=de5a_net_e1 -v**" to compile the OpenCL kernel. It will take about one hour for compiling. When the compilation process is finished, OpenCL image file **vector_add.aocx** is generated. **Figure 2-20** is the screenshot when OpenCL kernel is compiling. For required parameters to compile vector_add.cl, please refer to the README.html in the vector_add folder. For detailed usage of **aoc**, please refer to the **Intel FPGA SDK for OpenCL Programming Guide**:

https://www.altera.com/en_US/pdfs/literature/hb/opencl-sdk/aocl_programming_guide.pdf

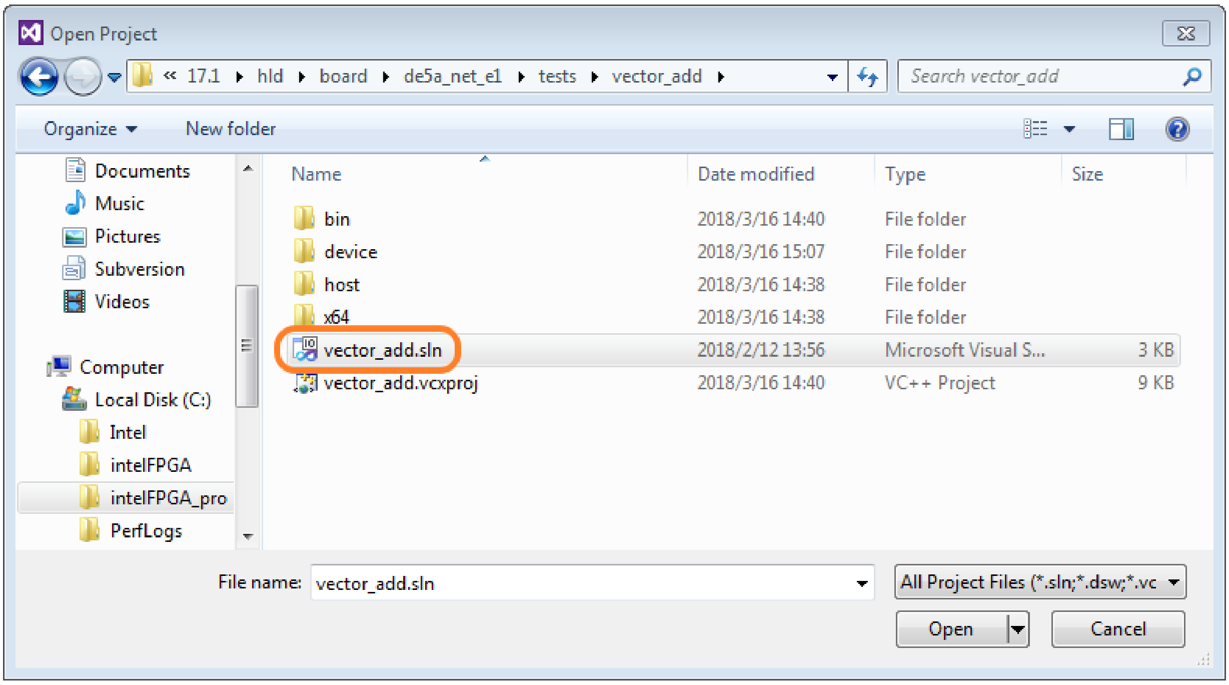

Administrator: C:\Windows\system32\cmd.exe - aoc device\vector_add.cl -o bin\vector_add.aocx -bo...

```
Microsoft Windows [Version 6.1.7600]
Copyright (c) 2009 Microsoft Corporation.  All rights reserved.

C:\Users\Administrator>cd C:\intelFPGA_pro\17.1\hld\board\de5a_net_e1\tests\vector
_add

C:\intelFPGA_pro\17.1\hld\board\de5a_net_e1\tests\vector_add>aoc device\vector_add
.cl -o bin\vector_add.aocx -board=de5a_net_e1 -v
aoc: Environment checks are completed successfully.
aoc: If necessary for the compile, your BAK files will be cached here: C:\Users\Ad
ministrator\AppData\Local\aocl
You are now compiling the full flow!!
aoc: Selected target board de5a_net_e1
aoc: Running OpenCL parser....
c:/intelFPGA_pro/17.1/hld/board/de5a_net_e1/tests/vector_add/device/vector_add.cl:
23:48: warning: declaring kernel argument with no 'restrict' may lead to low kerne
l performance
__kernel void vector_add(__global const float *x,
                                               ^

c:/intelFPGA_pro/17.1/hld/board/de5a_net_e1/tests/vector_add/device/vector_add.cl:
24:48: warning: declaring kernel argument with no 'restrict' may lead to low kerne
l performance
                         __global const float *y,
                                               ^

2 warnings generated.
aoc: OpenCL parser completed successfully.
aoc: Optimizing and doing static analysis of code...
aoc: Linking with IP library ...
Checking if memory usage is larger than 100%
aoc: First stage compilation completed successfully.
```

Figure 2-20 OpenCL Kernel Compile

■ Compile Host Program

Visual Studio C/C++ 2012 is used to compile the Host Program. Launch Visual Studio, and select menu item “FILE→Open Project/Solution…”. In the Open Project dialog, go to the folder *“C:\intelFPGA_pro\17.1\hld\board\de5a_net_e1\tests\vector_add”* , and select **vector_add.sln** as shown **Figure 2-21**.



Name	Date modified	Type	Size
bin	2018/3/16 14:40	File folder	
device	2018/3/16 15:07	File folder	
host	2018/3/16 14:38	File folder	
x64	2018/3/16 14:38	File folder	
vector_add.sln	2018/2/12 13:56	Microsoft Visual S...	3 KB
vector_add.vcxproj	2018/3/16 14:40	VC++ Project	9 KB

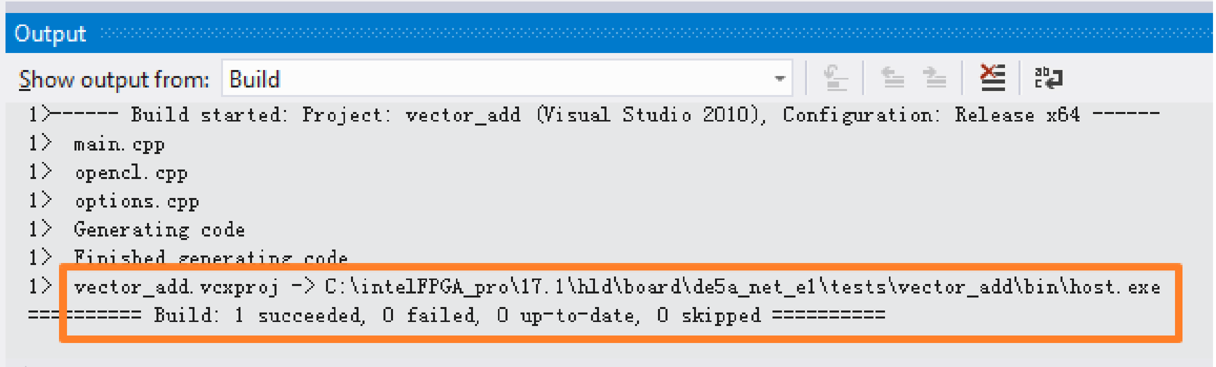
File name: vector_add.sln

All Project Files (*.sln;*.dsw;*.vc

Figure 2-21 Open Host Program

After vector_add Host Program project is opened successfully, in Visual Studio IDE select menu item “BUILD→Build Solution” to build host program. When build process is successful, you will see successful message as show in **Figure 2-22**. The execute file is generate in:

“C:\intelFPGA_pro\17.1\hld\board\de5a_net_e1\tests\vector_add\bin\host.exe”



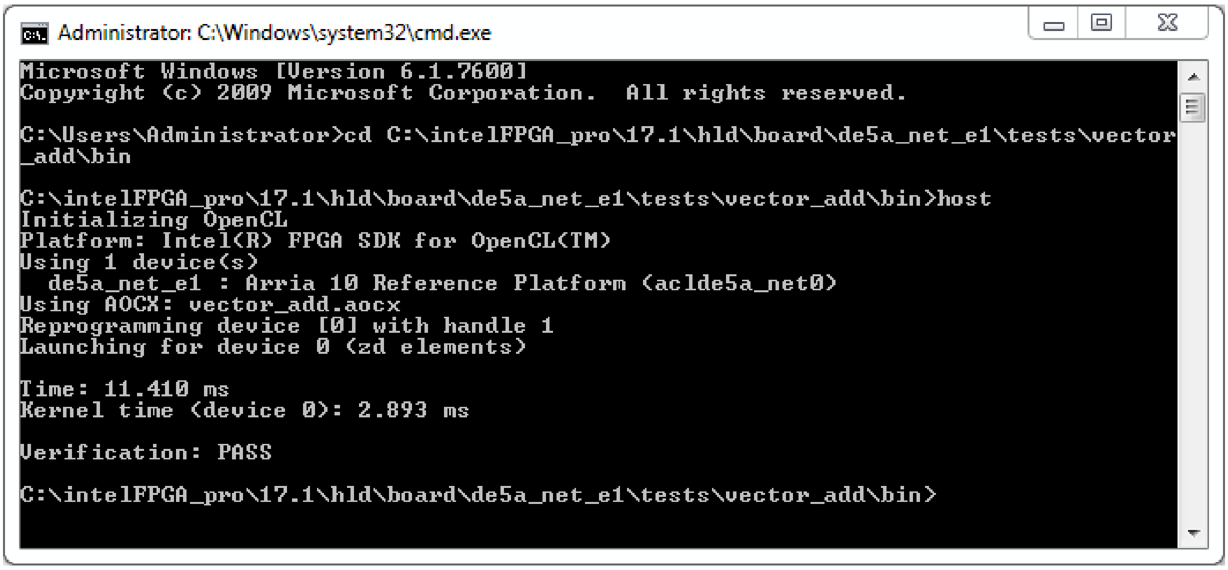
```
1>------ Build started: Project: vector_add (Visual Studio 2010), Configuration: Release x64 ------
1>  main.cpp
1>  opencl.cpp
1>  options.cpp
1>  Generating code
1>  Finished generating code
1>  vector_add.vcxproj -> C:\intelFPGA_pro\17.1\hld\board\de5a_net_e1\tests\vector_add\bin\host.exe
========== Build: 1 succeeded, 0 failed, 0 up-to-date, 0 skipped ==========
```

Figure 2-22 Host Program Build Successfully

■ Test vector_add project

Firstly, In **Command Prompt** window, type *"cd C:\intelFPGA_pro\17.1\hld\board\de5a_net_e1\tests\vector_add\bin"* to go to **vector_add\bin** project folder.

Then, execute "**host.exe**". Figure 2-23 is the screen shot when the test is successful.



Administrator: C:\Windows\system32\cmd.exe

```
Microsoft Windows [Version 6.1.7600]
Copyright (c) 2009 Microsoft Corporation.  All rights reserved.

C:\Users\Administrator>cd C:\intelFPGA_pro\17.1\hld\board\de5a_net_e1\tests\vector
_add\bin

C:\intelFPGA_pro\17.1\hld\board\de5a_net_e1\tests\vector_add\bin>host
Initializing OpenCL
Platform: Intel(R) FPGA SDK for OpenCL(TM)
Using 1 device(s)
  de5a_net_e1 : Arria 10 Reference Platform (acldе5a_net0)
Using AOCX: vector_add.aocx
Reprogramming device [0] with handle 1
Launching for device 0 (zd elements)

Time: 11.410 ms
Kernel time (device 0): 2.893 ms

Verification: PASS

C:\intelFPGA_pro\17.1\hld\board\de5a_net_e1\tests\vector_add\bin>
```

Figure 2-23 Host App Running successfully

Chapter 3

OpenCL for Linux

This chapter describe how to setup DE5a-Net OpenCL development environment on 64-bit Linux (Red Hat Enterprise Linux 6.5/CentOS 7.0 are recommended), and how to compile and test the OpenCL examples for DE5a-Net. For more details about Altera OpenCL, please refer to Intel FPGA SDK for OpenCL Getting Started document:

https://www.altera.com/en_US/pdfs/literature/hb/opencl-sdk/aocl_getting_started.pdf

3.1 Software Installation

This section describes how to download and install the required software for OpenCL.

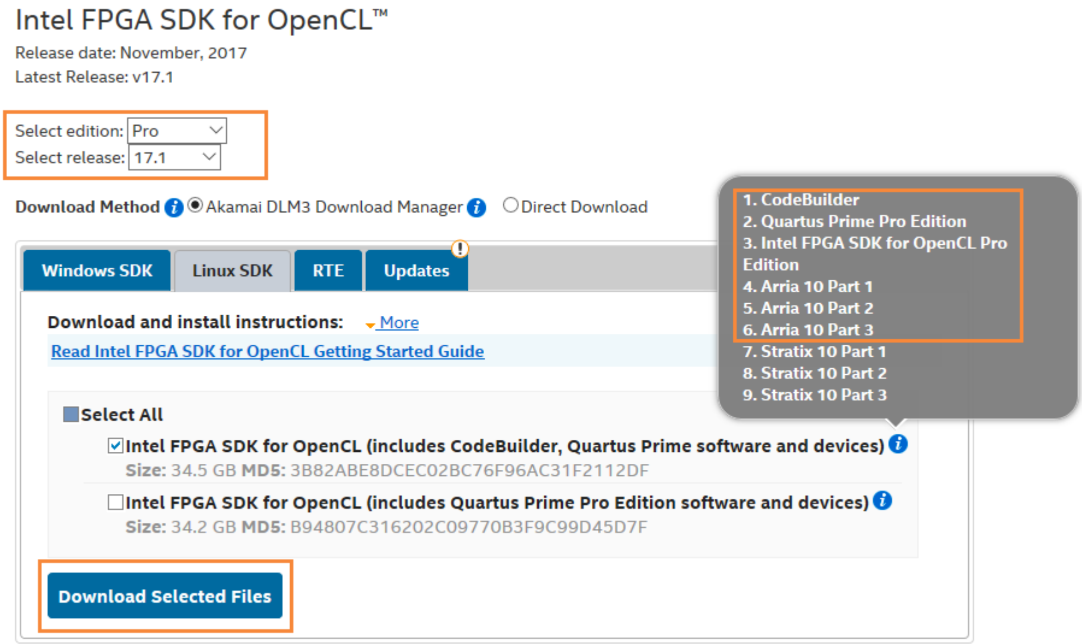
■ Altera Quartus II and OpenCL

Intel Quartus Prime Pro Edition 17.1.0.240 and Intel FPGA SDK for OpenCL 17.1.0.240 can be download from the web site:

http://dl.altera.com/opencl/17.1/?edition=pro

For Quartus II installation, please make sure that the Arria 10 device is included.

Open the link and select the **Linux SDK** as **Figure 3-1** shows.



Intel FPGA SDK for OpenCL™

Release date: November, 2017

Latest Release: v17.1

Select edition: Pro

Select release: 17.1

Download Method ● Akamai DLM3 Download Manager ○ Direct Download

Download and install instructions: More

Read Intel FPGA SDK for OpenCL Getting Started Guide

■ Select All

☑ Intel FPGA SDK for OpenCL (includes CodeBuilder, Quartus Prime software and devices)
Size: 34.5 GB MD5: 3B82ABE8DCEC02BC76F96AC31F2112DF

☐ Intel FPGA SDK for OpenCL (includes Quartus Prime Pro Edition software and devices)
Size: 34.2 GB MD5: B94807C316202C09770B3F9C99D45D7F

Download Selected Files

1. CodeBuilder
2. Quartus Prime Pro Edition
3. Intel FPGA SDK for OpenCL Pro Edition
4. Arria 10 Part 1
5. Arria 10 Part 2
6. Arria 10 Part 3
7. Stratix 10 Part 1
8. Stratix 10 Part 2
9. Stratix 10 Part 3

Figure 3-1 Linux SDK table

Quartus II software uses the built-in USB-Blaster II drivers on Linux to access USB-Blaster II download cable on DE5a-Net. but after installing the Quartus II software with built-in drivers, user need to change the port permission for USB-Blaster II via issuing

‘gedit /etc/udev/rules.d/51-usbblaster.rules’

to create and add the following lines to the **/etc/udev/rules.d/51-usbblaster.rules** file.

```
# USB-Blaster
BUS=="usb", SYSFS{idVendor}=="09fb", SYSFS{idProduct}=="6001", MODE="0666"
BUS=="usb", SYSFS{idVendor}=="09fb", SYSFS{idProduct}=="6002", MODE="0666"
BUS=="usb", SYSFS{idVendor}=="09fb", SYSFS{idProduct}=="6003", MODE="0666"
# USB-Blaster II
BUS=="usb", SYSFS{idVendor}=="09fb", SYSFS{idProduct}=="6010", MODE="0666"
BUS=="usb", SYSFS{idVendor}=="09fb", SYSFS{idProduct}=="6810", MODE="0666"
```

Note: You must have system administration (root) privileges to configure the USB-Blaster download cable drivers.

■ GNU development tools

GNU development tools such as **gcc** (include **g++**) and **make** are required to build the driver and application under Linux. User can issue 'yum install gcc ccompat-gcc-48-c++ make' command to download and install them and their dependencies via internet.

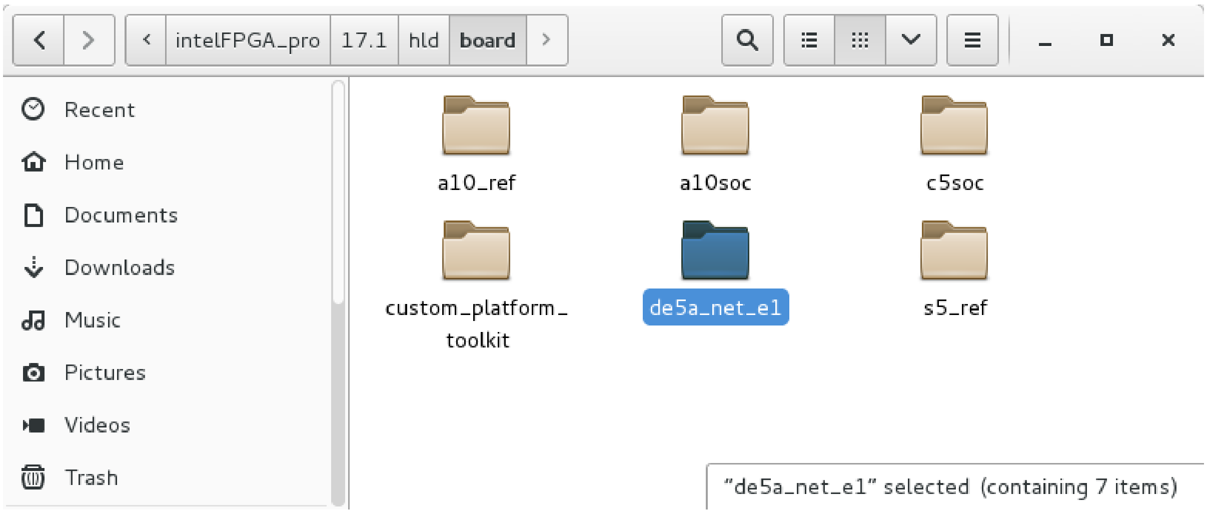
Note: To install the SDK on Linux, you must install it in a directory that you own (that is, a directory that is not a system directory). You must also have sudo or root privileges.

■ DE5a-Net OpenCL BSP (Board Support Package)

After Quartus II and OpenCL SDK are installed, please download the DE5ANET_E1_OpenCL_BSP_17.1.tar.gz DE5a-Net linux BSP from the web site:

http://de5a-net.terasic.com/cd

Then, decompress DE5ANET_E1_OpenCL_BSP_17.1.tar.gz to the "**de5a_net_e1**" folder under the folder "/root/intelFPGA_pro/17.1/hld/board", where assumed Quartus II is installed on the folder "/root/ intelFPGA_pro/17.1", as shown in Figure 3-2.



"de5a_net_e1" selected (containing 7 items)

Figure 3-2 DE5a-Net OpenCL BSP Content

For more details about DE5a-Net OpenCL BSP, please refer to the Table 2.

Table 2 Linux BSP File

File or Folder	Description
board_env.xml	eXtensible Markup Language (XML) file that describes the Reference Platform to the Intel FPGA SDK for OpenCL.
hardware	Contains the Intel Quartus Prime project templates for the a10gx board variant.
Linux64	Contains the MMD library, kernel mode driver, and executable files of the SDK utilities (that is, install, uninstall, flash, program, diagnose) for your 64-bit operating system
tests	Contains some OpenCL Design Examples. The following examples demonstrate how to describe various applications in OpenCL along with their respective host applications, which you can compile and execute on a host with an FPGA board that supports the Intel® FPGA SDK for OpenCL.

3.2 Environment Configure

If you install the Intel FPGA development software and OpenCL SDK on a system that does not contain any .cshrc or Bash Resource file (.bashrc) in your directory, you must set the INTELFPGAOCLSDKROOT and PATH environment variables manually. And the developers need to create an environment variable for the DE5a-Net board **AOCL_BOARD_PACKAGE_ROOT** so that the Intel FPGA OpenCL SDK is able to find the kit location of DE5a-Net correctly, and set its value as:

"$ INTELFPGAOCLSDKROOT "/board/de5a_net_e1”

Alternatively, you can edit the “/etc/profile” **profile** file, and append the environment variables to it. To do this type *“gedit /etc/profile”* command on Linux Terminal to open the **profile** file by the **gedit** editor tool，and append the following setting to the **profile** file. Then, save the file and type “*source /etc/profile”* command in Linux Terminal to make the settings make effect.

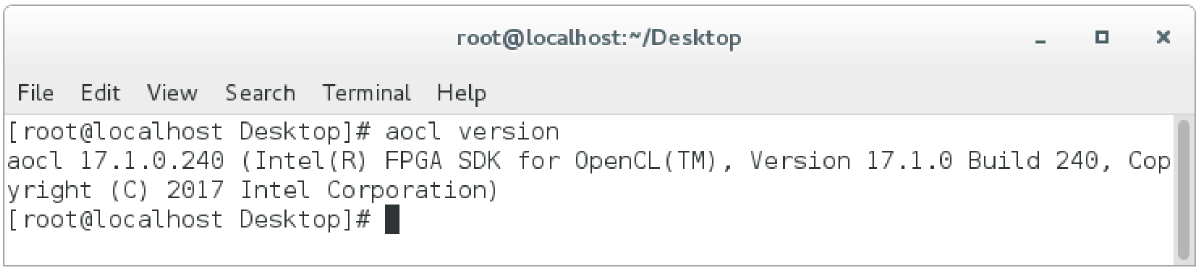
```
export QUARTUS_ROOTDIR=/root/intelFPGA_pro/17.1/quartus
export INTELFPGAOCLSDKROOT=/root/intelFPGA_pro/17.1/hld
export AOCL_BOARD_PACKAGE_ROOT=$INTELFPGAOCLSDKROOT/board/de5a_net_e1
export PATH=$PATH:$QUARTUS_ROOTDIR/bin:$INTELFPGAOCLSDKROOT/linux64/bin:$INTELFPGAOCLSDKROOT/bin:$ INTELFPGAOCLSDKROOT/host/linux64/bin:/root/intelFPGA_pro/17.1/qsys/bin
export LD_LIBRARY_PATH=$AOCL_BOARD_PACKAGE_ROOT/linux64/lib:$ INTELFPGAOCLSDKROOT/host/linux64/lib:$AOCL_BOARD_PACKAGE_ROOT/tests/extlibs/lib
export QUARTUS_64BIT=1
export LM_LICENSE_FILE=/root/intelFPGA_pro/17.1/license.dat
```

3.3 OpenCL Environment Verify

This section will show how to make sure the OpenCL environment is setup correctly. Firstly, please open the Linux system **terminal** window by right click the Mouse on system desktop, then clicking on **Open Terminal**.

■ Target SDK Version

In the Linux terminal, type "**aocl version**" command, and make sure the version of the OpenCL SDK is listed as shown in **Figure 3-3**.

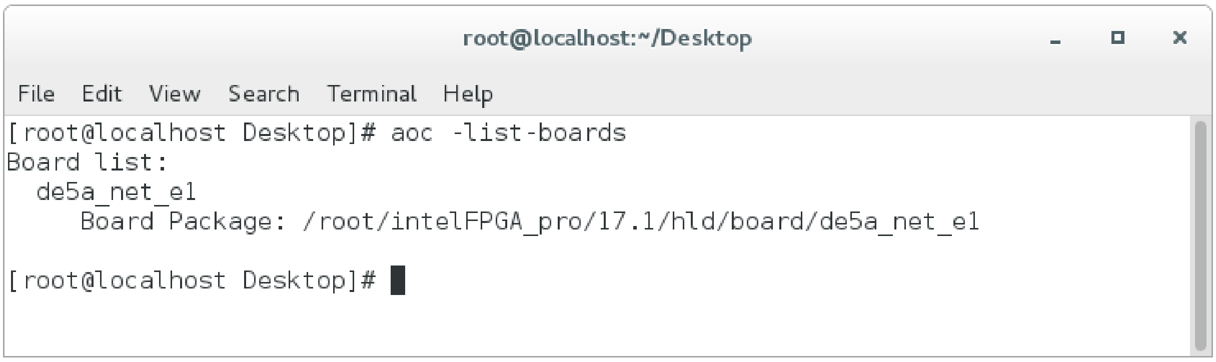


```
[root@localhost Desktop]# aocl version
aocl 17.1.0.240 (Intel(R) FPGA SDK for OpenCL(TM), Version 17.1.0 Build 240, Cop
yright (C) 2017 Intel Corporation)
[root@localhost Desktop]# █
```

Figure 3-3 Version of OpenCL SDK

■ Target Board

In the Linux terminal, type "**aoc -list-boards**" command, and make sure "**de5a_net_e1**" is listed in **Board list** as shown in **Figure 3-4**.



```
[root@localhost Desktop]# aoc -list-boards
Board list:
  de5a_net_e1
     Board Package: /root/intelFPGA_pro/17.1/hld/board/de5a_net_e1

[root@localhost Desktop]# █
```

Figure 3-4 'de5a_net_e1' is Listed in Board List

For more information about the **aoc** and **aocl**, refer to the '**aoc -h**' and '**aocl help**' command.

3.4 Initializing the FPGA for use with OpenCL

■ Board Setup

To use the DE5a-Net Arria 10 FPGA Development Kit with the Intel FPGA SDK for OpenCL, you must follow the below procedures to set up DE5a-Net board on your PC as shown in **Figure 3-5**.

5. Make sure your PC is powered off.
6. Insert DE5a-Net board into PCI Express x8 or x16 slot.
7. Connect PC’s 12V PCI Express 6-pin power source to the DE5a-Net (if there’s not, ignore this step).
8. Connect PC’s USB port to DE5a-Net mini USB port using an USB cable.

Note, the USB cable can be removed later if OpenCL code had been programmed to the startup configuration flash of DE5a-Net by ‘**aocl flash**’ command.

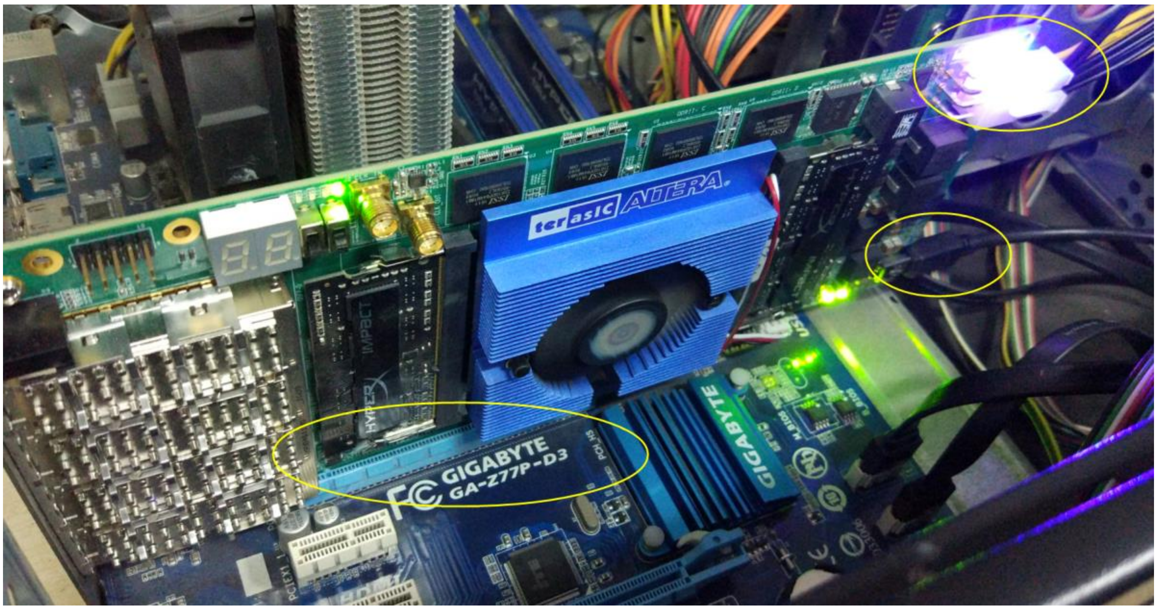
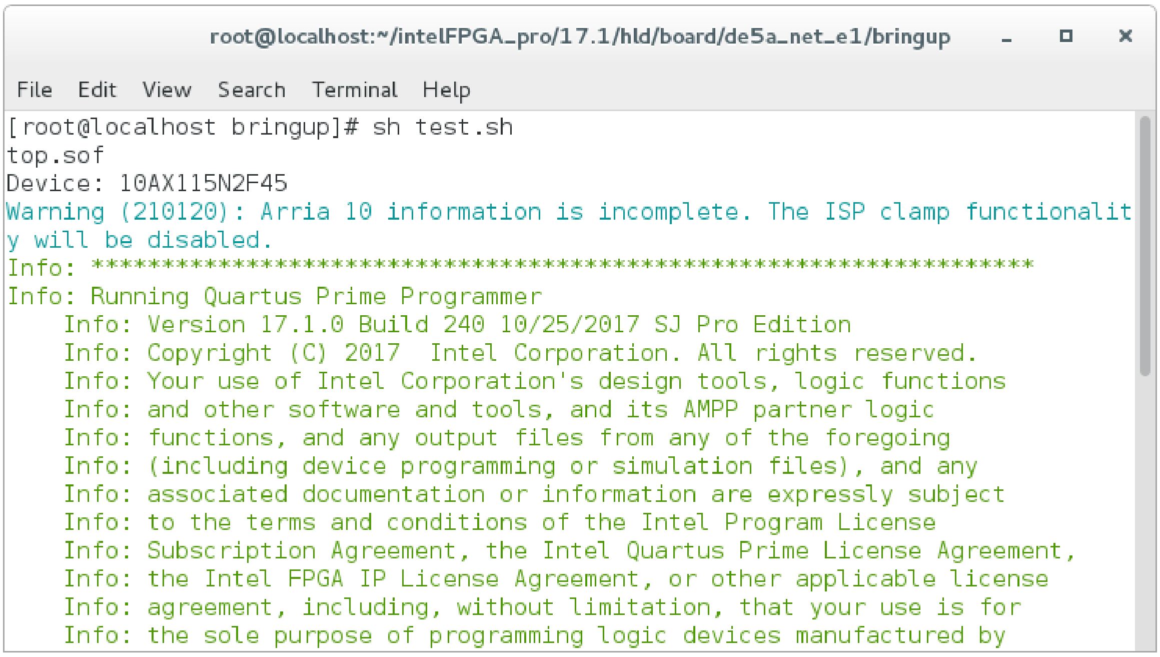


Figure 3-5 Setup DE5a-Net board on PC

■ Bring up the FPGA Board

Before using the DE5a-Net Arria 10 FPGA Development Kit with OpenCL, you must initialize the board with an OpenCL image. Without this image, the board host operating system does not recognize the PCIe card and the Intel FPGA OpenCL compiler cannot find the device.

Program the FPGA on your DE5a-Net Arria 10 FPGA Development Kit with the **top.sof** file by running the **sh test.sh** in **bringup** folder as shown in Figure 3-6.



root@localhost:~/intelFPGA_pro/17.1/hld/board/de5a_net_e1/bringup
File Edit View Search Terminal Help

```
[root@localhost bringup]# sh test.sh
top.sof
Device: 10AX115N2F45
Warning (210120): Arria 10 information is incomplete. The ISP clamp functionalit
y will be disabled.
Info: ******************************************************************
Info: Running Quartus Prime Programmer
    Info: Version 17.1.0 Build 240 10/25/2017 SJ Pro Edition
    Info: Copyright (C) 2017  Intel Corporation. All rights reserved.
    Info: Your use of Intel Corporation's design tools, logic functions
    Info: and other software and tools, and its AMPP partner logic
    Info: functions, and any output files from any of the foregoing
    Info: (including device programming or simulation files), and any
    Info: associated documentation or information are expressly subject
    Info: to the terms and conditions of the Intel Program License
    Info: Subscription Agreement, the Intel Quartus Prime License Agreement,
    Info: the Intel FPGA IP License Agreement, or other applicable license
    Info: agreement, including, without limitation, that your use is for
    Info: the sole purpose of programming logic devices manufactured by
```

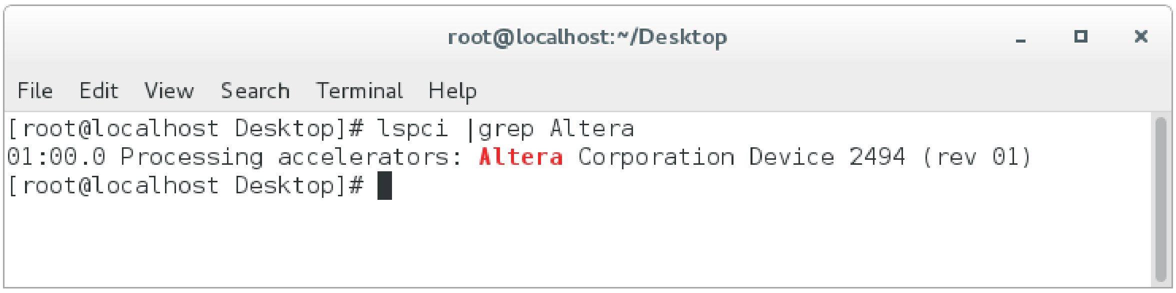
Figure 3-6 Bring up the FPGA Borad

Use the /sbin/reboot command to perform a soft reboot of your host system causes your host system to recognize the DE5a-Net Arria 10 FPGA Development Kit PCIe card.

■ Driver Installation

Your system must recognize the card so that the Intel FPGA SDK for OpenCL driver can be loaded. The **install** utility is used install the kernel driver on the host computer. Users of the Intel FPGA SDK for OpenCL only need to install the driver once, after that the driver should be automatically loaded each time the machine reboots.

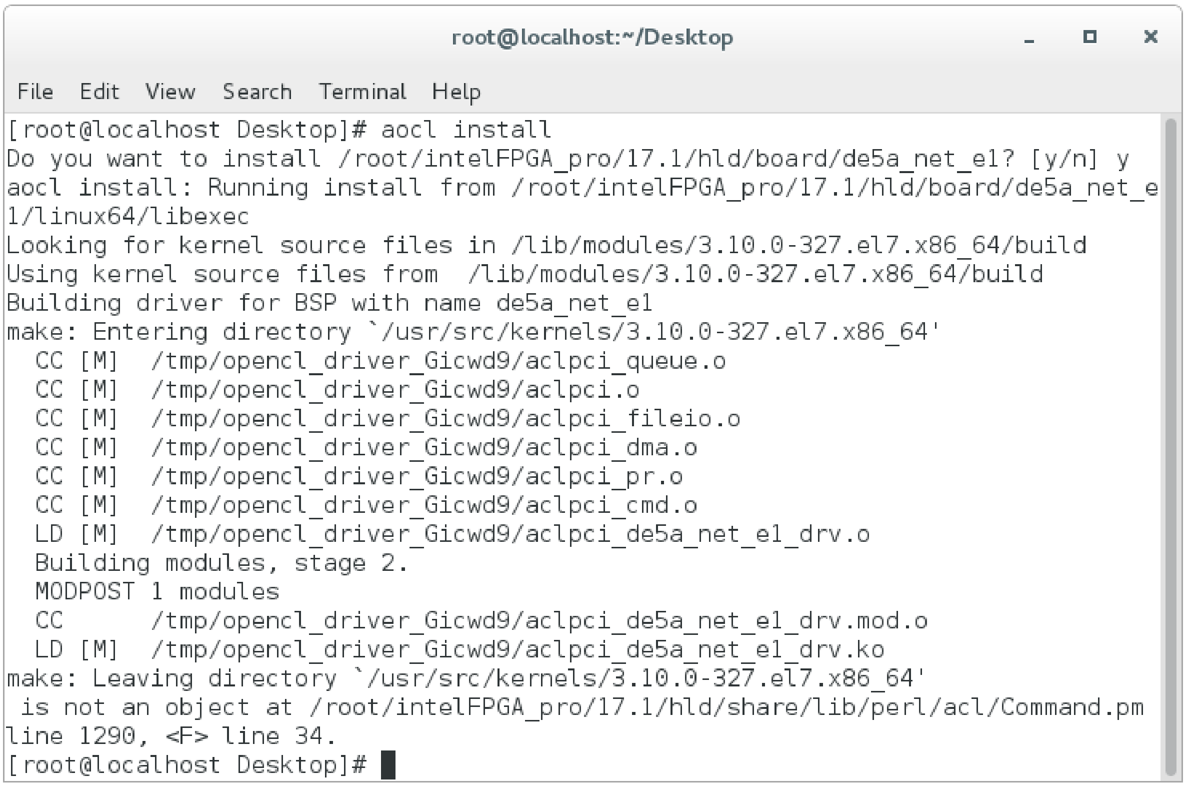
First, in the Linux terminal, type '**lspci |grep Altera**' to make sure the system recognizes the PCIe card as shown in Figure 3-7.



```
[root@localhost Desktop]# lspci |grep Altera
01:00.0 Processing accelerators: Altera Corporation Device 2494 (rev 01)
[root@localhost Desktop]#
```

Figure 3-7 PCIE Message

Type '**aocl install**' to install the driver as shown in Figure 3-8. Note that users need to have root privileges to install the driver.



```
[root@localhost Desktop]# aocl install
Do you want to install /root/intelFPGA_pro/17.1/hld/board/de5a_net_e1? [y/n] y
aocl install: Running install from /root/intelFPGA_pro/17.1/hld/board/de5a_net_e
1/linux64/libexec
Looking for kernel source files in /lib/modules/3.10.0-327.el7.x86_64/build
Using kernel source files from  /lib/modules/3.10.0-327.el7.x86_64/build
Building driver for BSP with name de5a_net_e1
make: Entering directory `/usr/src/kernels/3.10.0-327.el7.x86_64'
  CC [M]  /tmp/opencl_driver_Gicwd9/aclpci_queue.o
  CC [M]  /tmp/opencl_driver_Gicwd9/aclpci.o
  CC [M]  /tmp/opencl_driver_Gicwd9/aclpci_fileio.o
  CC [M]  /tmp/opencl_driver_Gicwd9/aclpci_dma.o
  CC [M]  /tmp/opencl_driver_Gicwd9/aclpci_pr.o
  CC [M]  /tmp/opencl_driver_Gicwd9/aclpci_cmd.o
  LD [M]  /tmp/opencl_driver_Gicwd9/aclpci_de5a_net_e1_drv.o
  Building modules, stage 2.
  MODPOST 1 modules
  CC      /tmp/opencl_driver_Gicwd9/aclpci_de5a_net_e1_drv.mod.o
  LD [M]  /tmp/opencl_driver_Gicwd9/aclpci_de5a_net_e1_drv.ko
make: Leaving directory `/usr/src/kernels/3.10.0-327.el7.x86_64'
 is not an object at /root/intelFPGA_pro/17.1/hld/share/lib/perl/acl/Command.pm
line 1290, <F> line 34.
[root@localhost Desktop]# 
```

Figure 3-8 Driver Installation

Note: if user don't use the recommended Linux system or different version, recompiling the driver is needed. You can compile it by typing *"cd root/intelFPGA_pro/17.1/hld/board/de5a_net_e1/ linux64/driver"* (there are source code, Makefile and README.txt) to locate at the driver source code directory and type *"sh make_all.sh"* to compile and generate the new driver. Before that, user need to install the kernel related development package matched the current kernel (**kernel-devel** package) via issuing '*yum install kernel-devel*' command.

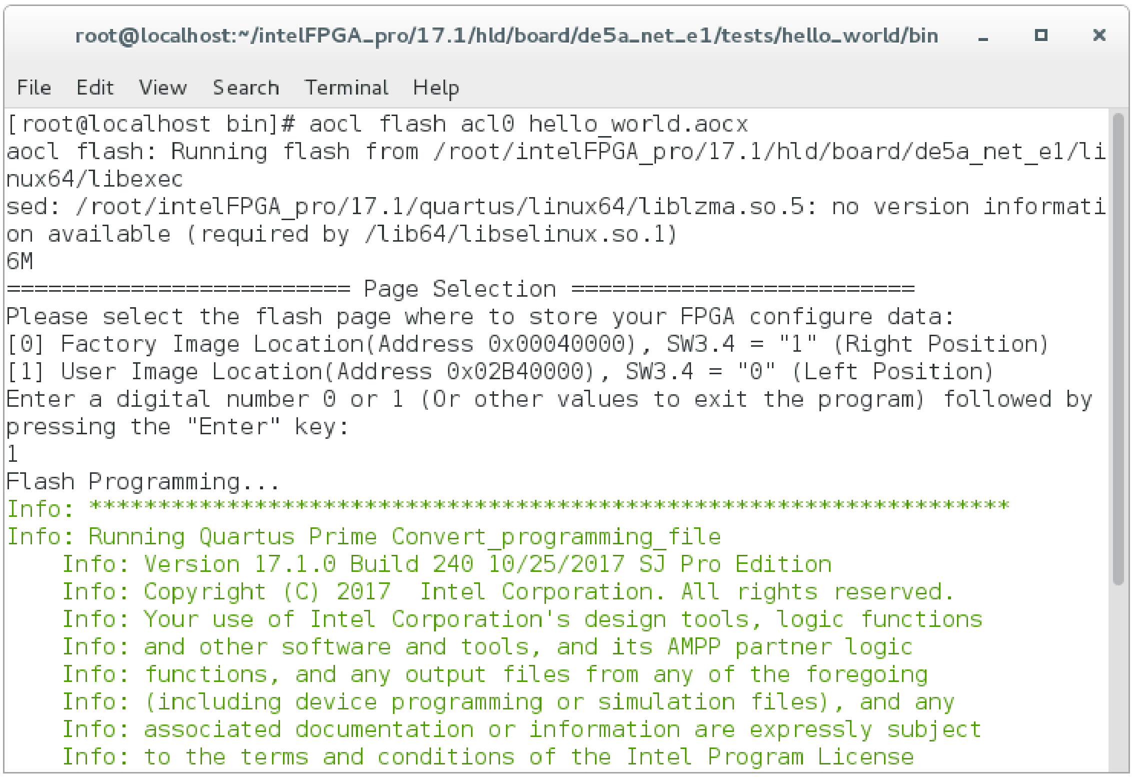
■ 'aocl flash' program

The **flash** utility configures the power-on image for the FPGA using the specified **aocx** file. Calling into the MMD library implements the flash utility.

In the Linux terminal, type *"cd C:\intelFPGA\17.1\hld\board\de5a_net_e1\tests\hello_world\bin"* to go to hello world OpenCL project folder.

Then type "**aocl flash acl0 hello_world.aocx**" to write **hello_world.aocx** OpenCL image onto the startup configuration flash of DE5a-Net.

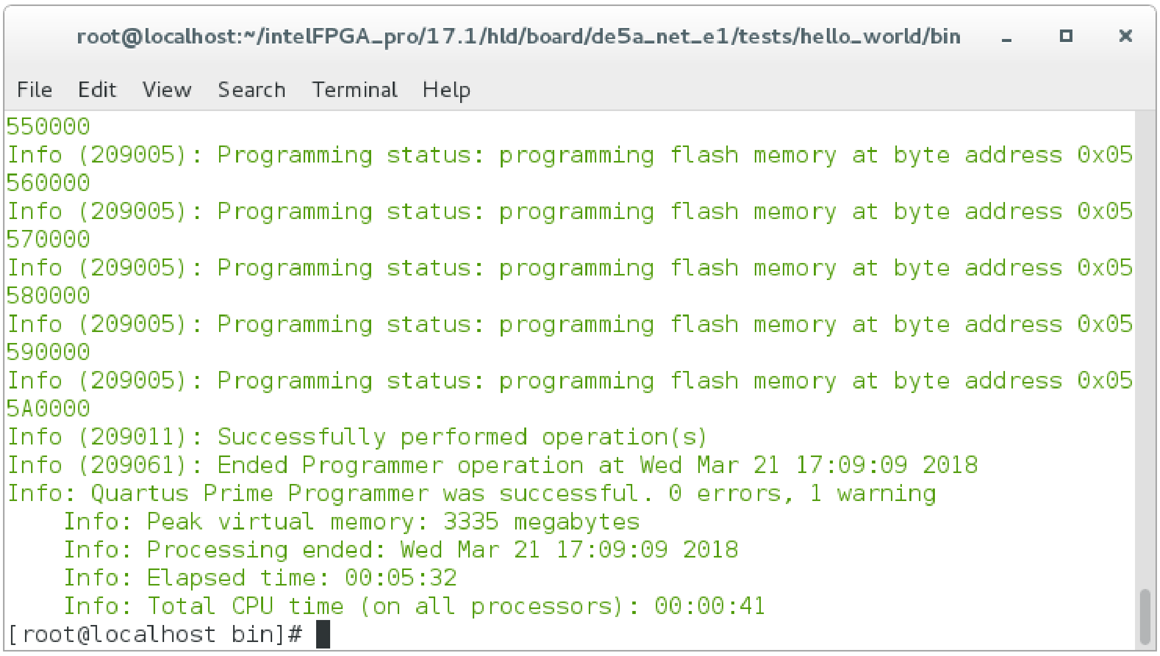
Before flash programming, the programmer will ask users which startup configuration image area will be used as shown in **Figure 3-9**. This is because DE5a-Net provides two startup configuration image areas, called as Factory Image and User Image. We recommend users to key in '1' to select User Image area.


root@localhost:~/intelFPGA_pro/17.1/hld/board/de5a_net_e1/tests/hello_world/bin
File Edit View Search Terminal Help

```
[root@localhost bin]# aocl flash acl0 hello_world.aocx
aocl flash: Running flash from /root/intelFPGA_pro/17.1/hld/board/de5a_net_e1/li
nux64/libexec
sed: /root/intelFPGA_pro/17.1/quartus/linux64/liblzma.so.5: no version informati
on available (required by /lib64/libselinux.so.1)
6M
========================= Page Selection =========================
Please select the flash page where to store your FPGA configure data:
[0] Factory Image Location(Address 0x00040000), SW3.4 = "1" (Right Position)
[1] User Image Location(Address 0x02B40000), SW3.4 = "0" (Left Position)
Enter a digital number 0 or 1 (Or other values to exit the program) followed by
pressing the "Enter" key:
1
Flash Programming...
Info: *******************************************************************
Info: Running Quartus Prime Convert_programming_file
    Info: Version 17.1.0 Build 240 10/25/2017 SJ Pro Edition
    Info: Copyright (C) 2017  Intel Corporation. All rights reserved.
    Info: Your use of Intel Corporation's design tools, logic functions
    Info: and other software and tools, and its AMPP partner logic
    Info: functions, and any output files from any of the foregoing
    Info: (including device programming or simulation files), and any
    Info: associated documentation or information are expressly subject
    Info: to the terms and conditions of the Intel Program License
```

Figure 3-9 Select Flash Page

After users select desired flash area, it will take about 8 minutes for flash programming. Figure 3-10 is the screen shot when flash programming is done successfully.


root@localhost:~/intelFPGA_pro/17.1/hld/board/de5a_net_e1/tests/hello_world/bin
File Edit View Search Terminal Help

```
550000
Info (209005): Programming status: programming flash memory at byte address 0x05
560000
Info (209005): Programming status: programming flash memory at byte address 0x05
570000
Info (209005): Programming status: programming flash memory at byte address 0x05
580000
Info (209005): Programming status: programming flash memory at byte address 0x05
590000
Info (209005): Programming status: programming flash memory at byte address 0x05
5A0000
Info (209011): Successfully performed operation(s)
Info (209061): Ended Programmer operation at Wed Mar 21 17:09:09 2018
Info: Quartus Prime Programmer was successful. 0 errors, 1 warning
    Info: Peak virtual memory: 3335 megabytes
    Info: Processing ended: Wed Mar 21 17:09:09 2018
    Info: Elapsed time: 00:05:32
    Info: Total CPU time (on all processors): 00:00:41
[root@localhost bin]# 
```

Figure 3-10 Aocl Flash Successfully

To make sure a correct image is used when FPGA boots up, please make sure the dip switch **SW3.4** on DE5a-Net is changed to the correct location. If a User Image area is selected, the dip switch SW3.4 on the DE5a-Net should be moved to **Up** position as shown in Figure 3-11.

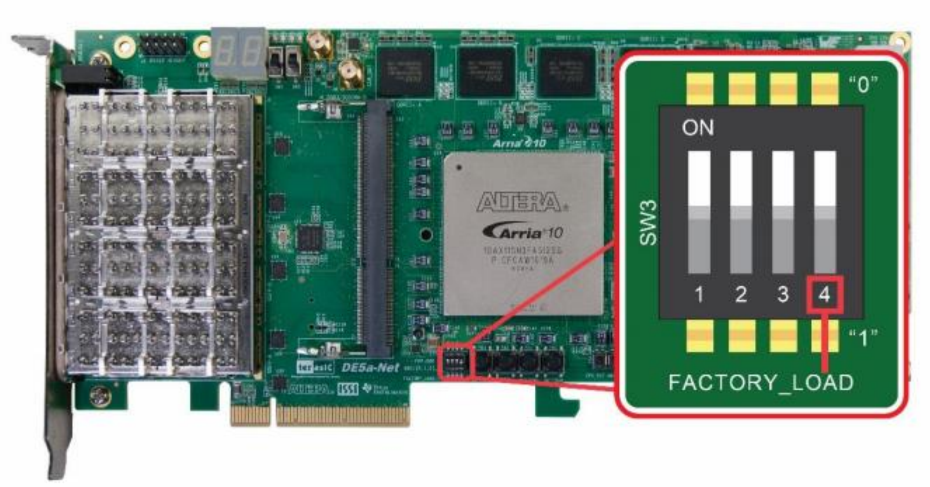


Figure 3-11 Set SW3.4 to Up Position (User Image Page)

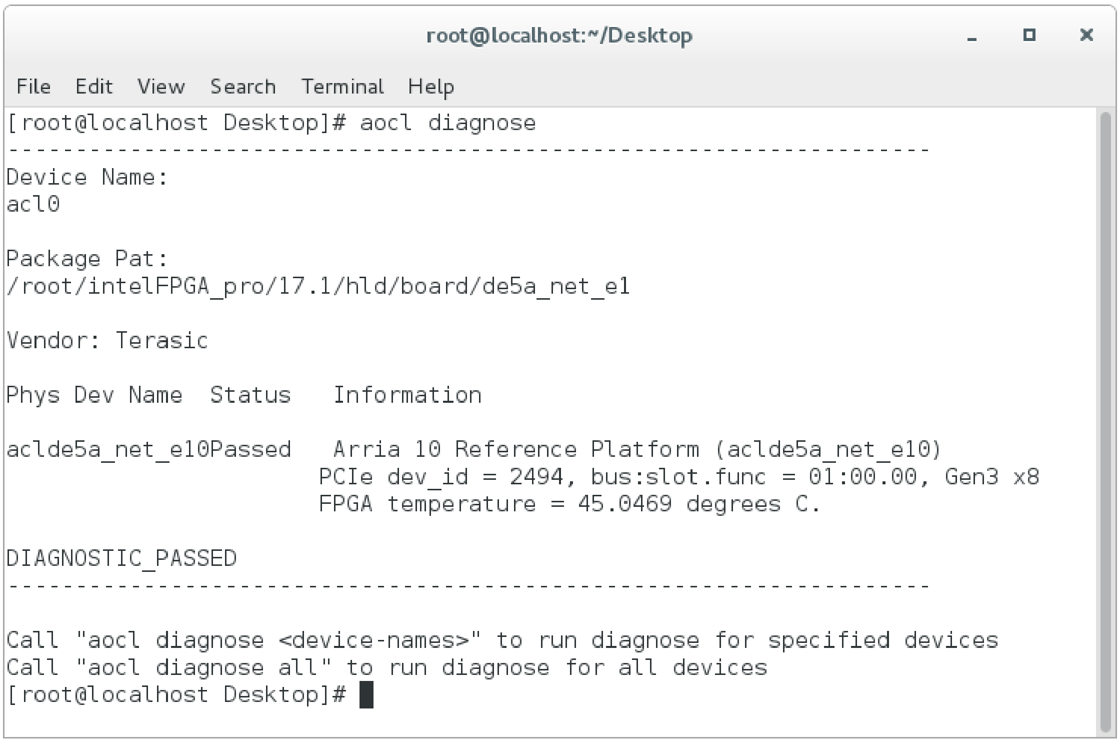
After flash programming is done successfully and SW3.4 is set to correct position, **developers must power off DE5a-Net board, then turn it back on, and restart the PC.**

3.5 OpenCL Runtime Verify

■ Test 'aocl diagnose' Command

The **diagnose** utility reports device information and identifies issues. The diagnose utility first verifies the installation of the kernel driver and returns the overall information of all the devices installed in a host machine.

In the Linux **terminal**, type "**aocl diagnose**" to check if the initialization completed successfully. If successful, the programming message displays "**DIAGNOSTIC_PASSED**" as shown in Figure 3-12.



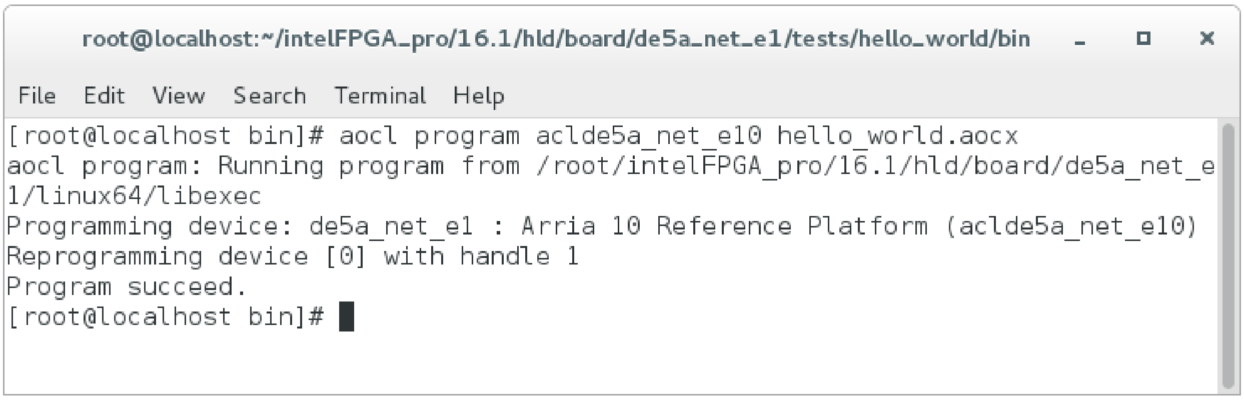
```
[root@localhost Desktop]# aocl diagnose
--------------------------------------------------------------------
Device Name:
acl0

Package Pat:
/root/intelFPGA_pro/17.1/hld/board/de5a_net_e1

Vendor: Terasic

Phys Dev Name  Status   Information

aclde5a_net_e10Passed   Arria 10 Reference Platform (aclde5a_net_e10)
                       PCIe dev_id = 2494, bus:slot.func = 01:00.00, Gen3 x8
                       FPGA temperature = 45.0469 degrees C.

DIAGNOSTIC_PASSED
--------------------------------------------------------------------

Call "aocl diagnose <device-names>" to run diagnose for specified devices
Call "aocl diagnose all" to run diagnose for all devices
[root@localhost Desktop]#
```

Figure 3-12 "aocl diagnose" Messages

Note: It is strongly recommended that users set the PCIe speed at Gen 3 in the BIOS on the host PC, so that DE5a-Net negotiates with the host PC at Gen3 as the link speed. If your PC support PCIe Gen3x8, but it gets incorrect detected information, you can modify the PCIe settings in the BIOS, and reboot.

■ Test ‘aocl program’ Command

The **program** utility programs the board with the specified **aocx** file. Check whether the **hello_world** OpenCL image configures the FPGA successfully. In the Linux **terminal**, type *“cd C:\intelFPGA_pro\17.1\hld\board\de5a_net_e1\tests\hello_world\bin”* to go to **hello_world\bin** project folder, then type “**aocl program acl0 hello_world.aocx**” to configure the FPGA with **hello_world.aocx** OpenCL image. If the programming message displays “Program succeed” as shown in Figure 3-13, it means the **hello_world** OpenCL image is programmed into the FPGA correctly.


root@localhost:~/intelFPGA_pro/16.1/hld/board/de5a_net_e1/tests/hello_world/bin
File Edit View Search Terminal Help

```
[root@localhost bin]# aocl program aclde5a_net_e10 hello_world.aocx
aocl program: Running program from /root/intelFPGA_pro/16.1/hld/board/de5a_net_e
1/linux64/libexec
Programming device: de5a_net_e1 : Arria 10 Reference Platform (aclde5a_net_e10)
Reprogramming device [0] with handle 1
Program succeed.
[root@localhost bin]#
```

Figure 3-13 Aocl Program Successfully

3.6 Compile and Test OpenCL Project

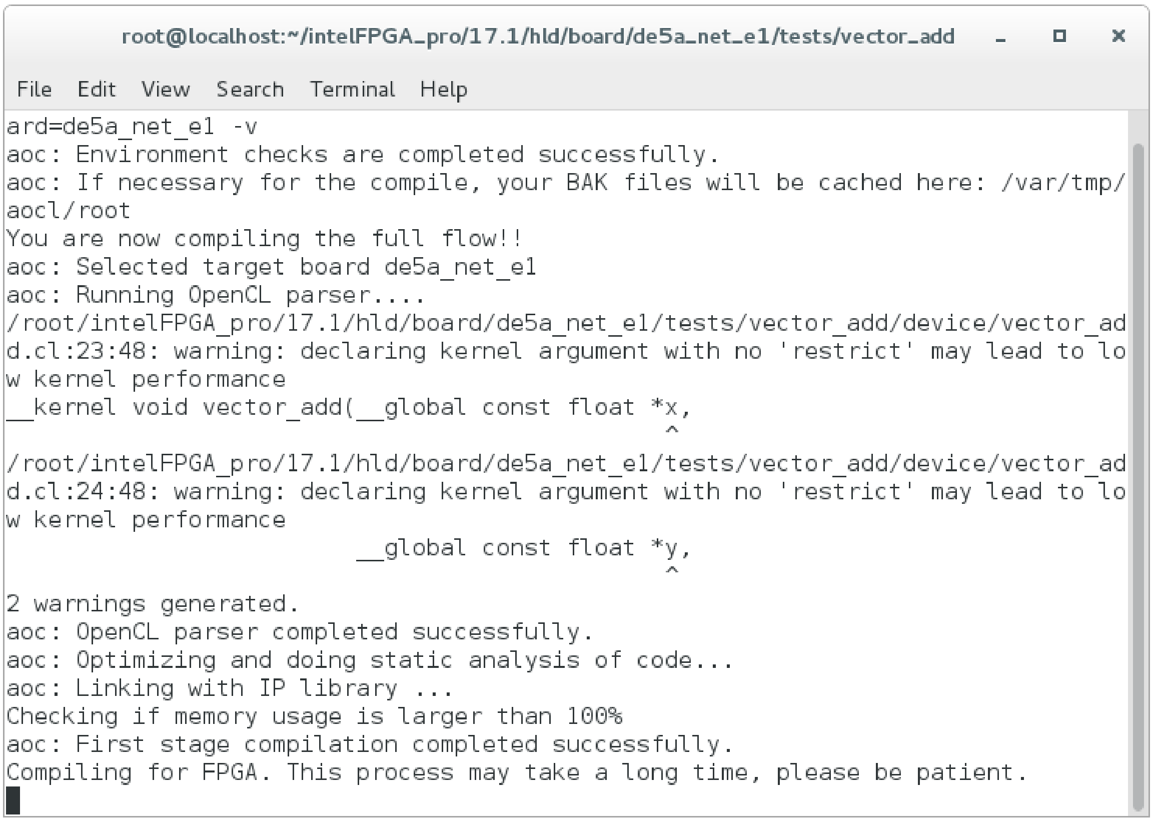
This section will show how to compile and run the OpenCL kernel and OpenCL Host Program for the vector_add example project. Developers can use the same procedures to compile and test other OpenCL examples (included in the kit) for DE5a-Net.

■ Compile OpenCL Kernel

In the **terminal**, type *"cd /root/intelFPGA_pro/17.1/hld/board/de5a_net_e1/tests/vector_add"* to go to **vector_add** project folder, then type **"*aoc device/vector_add.cl -o bin/vector_add.aocx -board=de5a_net_e1 -v*"** to compile the OpenCL kernel. It will take about one hour for compiling. After that, the OpenCL image file **vector_add.aocx** is generated. Figure 3-14 is the screen shot when OpenCL kernel is compiled successfully. For required parameters to compile vector_add.cl, please refer to the README.txt that is in the same directory.

The utility **aoc** (Altera SDK for OpenCL Kernel Compiler) is used to compile OpenCL kernel. For detailed usage of **aoc**, please refer to the **Intel FPGA SDK for OpenCL Programming Guide**:

http://www.altera.com/literature/hb/opencl-sdk/aocl_programming_guide.pdf


root@localhost:~/intelFPGA_pro/17.1/hld/board/de5a_net_e1/tests/vector_add
File Edit View Search Terminal Help

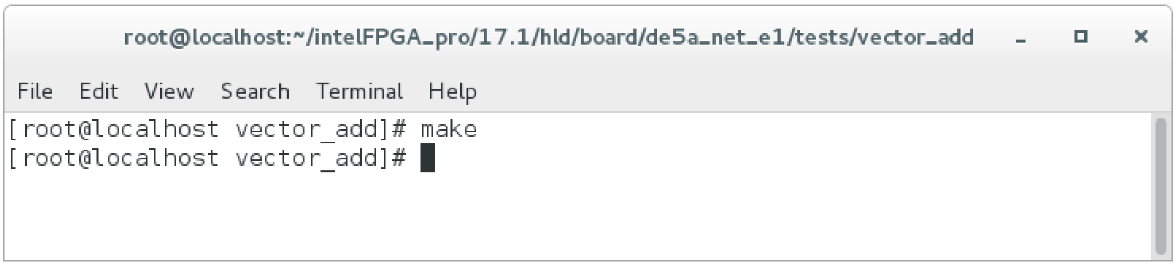
```
ard=de5a_net_e1 -v
aoc: Environment checks are completed successfully.
aoc: If necessary for the compile, your BAK files will be cached here: /var/tmp/
aocl/root
You are now compiling the full flow!!
aoc: Selected target board de5a_net_e1
aoc: Running OpenCL parser....
/root/intelFPGA_pro/17.1/hld/board/de5a_net_e1/tests/vector_add/device/vector_ad
d.cl:23:48: warning: declaring kernel argument with no 'restrict' may lead to lo
w kernel performance
__kernel void vector_add(__global const float *x,
                                               ^
/root/intelFPGA_pro/17.1/hld/board/de5a_net_e1/tests/vector_add/device/vector_ad
d.cl:24:48: warning: declaring kernel argument with no 'restrict' may lead to lo
w kernel performance
                         __global const float *y,
                                               ^
2 warnings generated.
aoc: OpenCL parser completed successfully.
aoc: Optimizing and doing static analysis of code...
aoc: Linking with IP library ...
Checking if memory usage is larger than 100%
aoc: First stage compilation completed successfully.
Compiling for FPGA. This process may take a long time, please be patient.
```

Figure 3-14 OpenCL Kernel Compile Successfully

■ Compile Host Program

In the **terminal**, type *"cd /root/intelFPGA_pro/17.1/hld/board/de5a_net_e1/tests/vector_add"* and then type *"**make**"* to compile the host program.

When build is successfully, you will see successful message as show in **Figure 3-15**. The execute file is generate in the same directory which named bin.


root@localhost:~/intelFPGA_pro/17.1/hld/board/de5a_net_e1/tests/vector_add
File Edit View Search Terminal Help

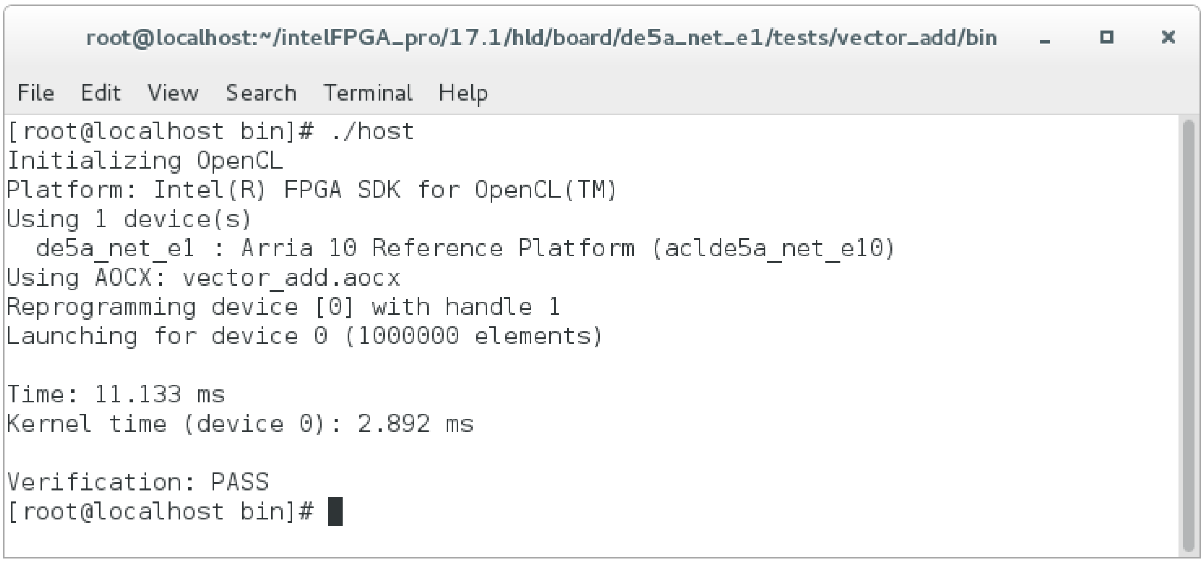
```
[root@localhost vector_add]# make
[root@localhost vector_add]# 
```

Figure 3-15 Host Program Build Successful

■ Test vector_add project

Firstly, In the **terminal**, type *"cd /root/intelFPGA_pro/17.1/hld/board/de5a_net_e1/tests/vector _add/bin"* to go to the **vector_add** project folder, then type "***aocl program acl0 vector_add. aocx***" to configure FPGA with the OpenCL Image vector_add.aocx.

Then, launch the compiled Host Program to start vector_add execute file for test. In the **terminal** type "**./host**". **Figure 3-16** shows the execution is successful.


root@localhost:~/intelFPGA_pro/17.1/hld/board/de5a_net_e1/tests/vector_add/bin
File Edit View Search Terminal Help

```
[root@localhost bin]# ./host
Initializing OpenCL
Platform: Intel(R) FPGA SDK for OpenCL(TM)
Using 1 device(s)
  de5a_net_e1 : Arria 10 Reference Platform (aclde5a_net_e10)
Using AOCX: vector_add.aocx
Reprogramming device [0] with handle 1
Launching for device 0 (1000000 elements)

Time: 11.133 ms
Kernel time (device 0): 2.892 ms

Verification: PASS
[root@localhost bin]# 
```

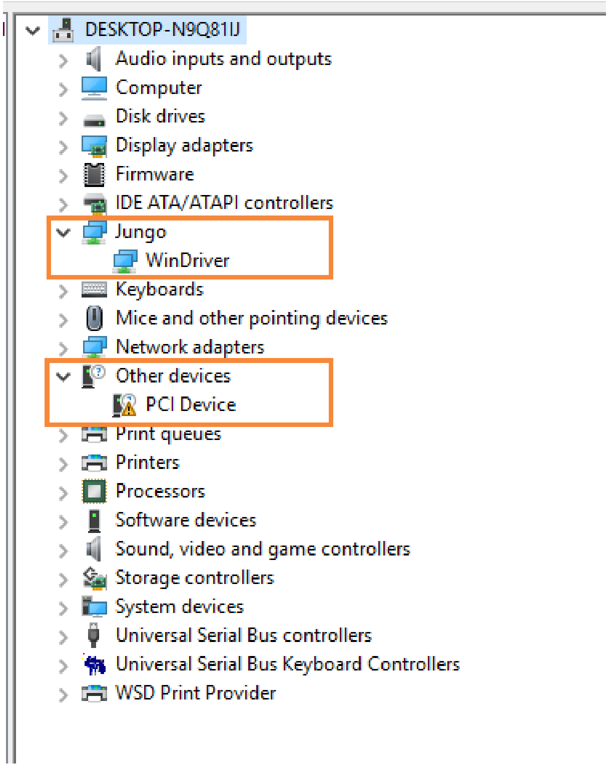
Figure 3-16 Host App Running successfully

Chapter 4

Appendix

Windows10 x64 OpenCL Driver Install

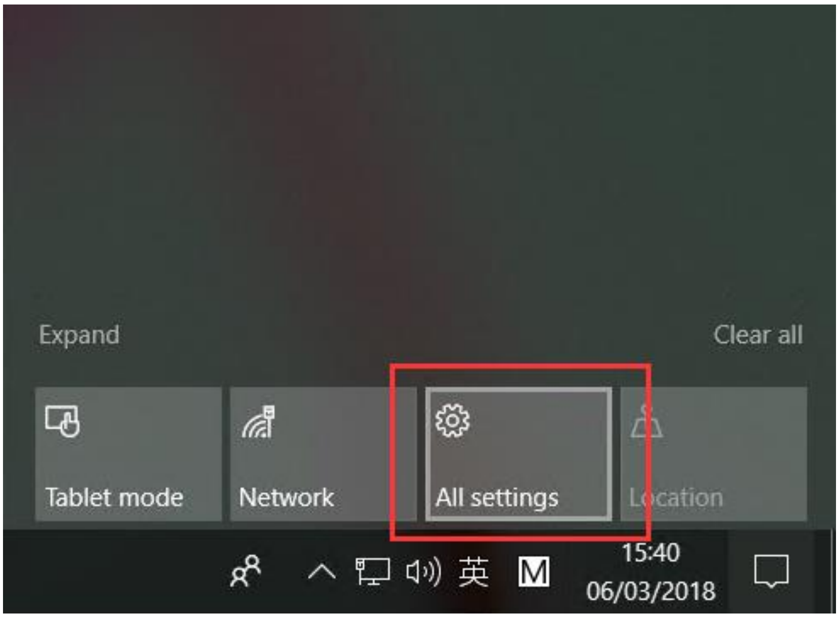
Because the win10 system requires the signature of the .inf file, sometimes, the driver of the PCIE (without signature) fails to be installed after running aocl install.



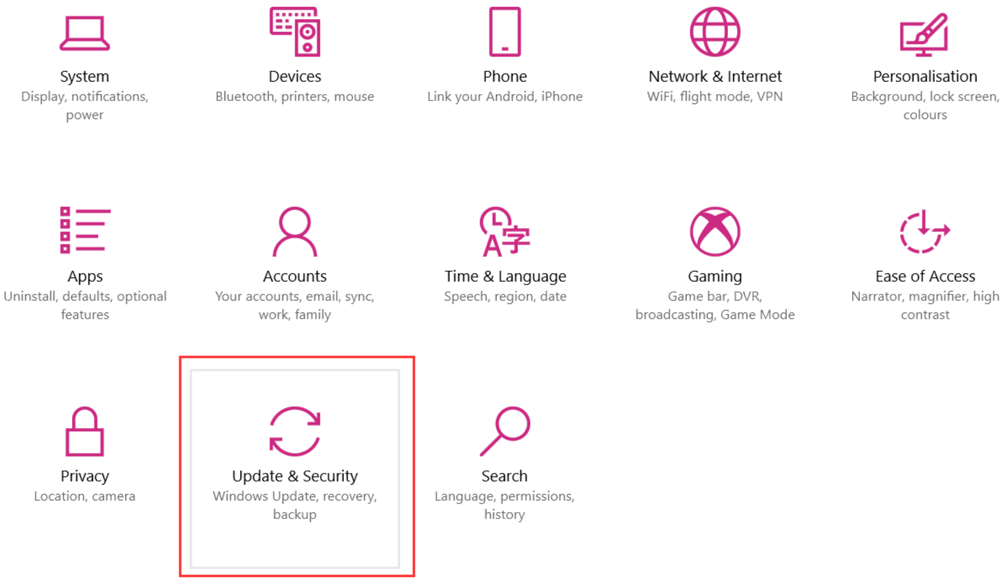
As a solution, it needs to disable the driver signature, and then manually install the PCIe driver. The steps are as following:

A. Disable the driver signature in the Win10 system

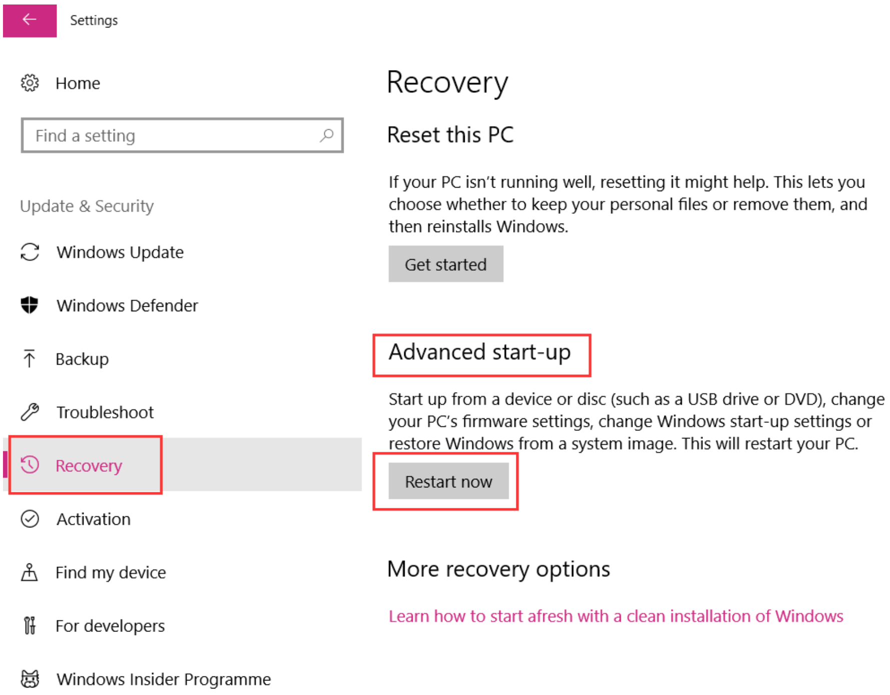
1.Click **Home**，enter “**All settings**”.



2. Access “**Update & Security**”.


System
Display, notifications, power
Devices
Bluetooth, printers, mouse
Phone
Link your Android, iPhone
Network & Internet
WiFi, flight mode, VPN
Personalisation
Background, lock screen, colours
Apps
Uninstall, defaults, optional features
Accounts
Your accounts, email, sync, work, family
Time & Language
Speech, region, date
Gaming
Game bar, DVR, broadcasting, Game Mode
Ease of Access
Narrator, magnifier, high contrast
Privacy
Location, camera
Update & Security
Windows Update, recovery, backup
Search
Language, permissions, history

3.Find **Recovery**. Click “**Restart now**” below “**Advanced start-up**”,restart the PC.



Settings

Home

Find a setting

Update & Security

Windows Update

Windows Defender

Backup

Troubleshoot

Recovery

Activation

Find my device

For developers

Windows Insider Programme

Recovery

Reset this PC

If your PC isn't running well, resetting it might help. This lets you choose whether to keep your personal files or remove them, and then reinstalls Windows.

Get started

Advanced start-up

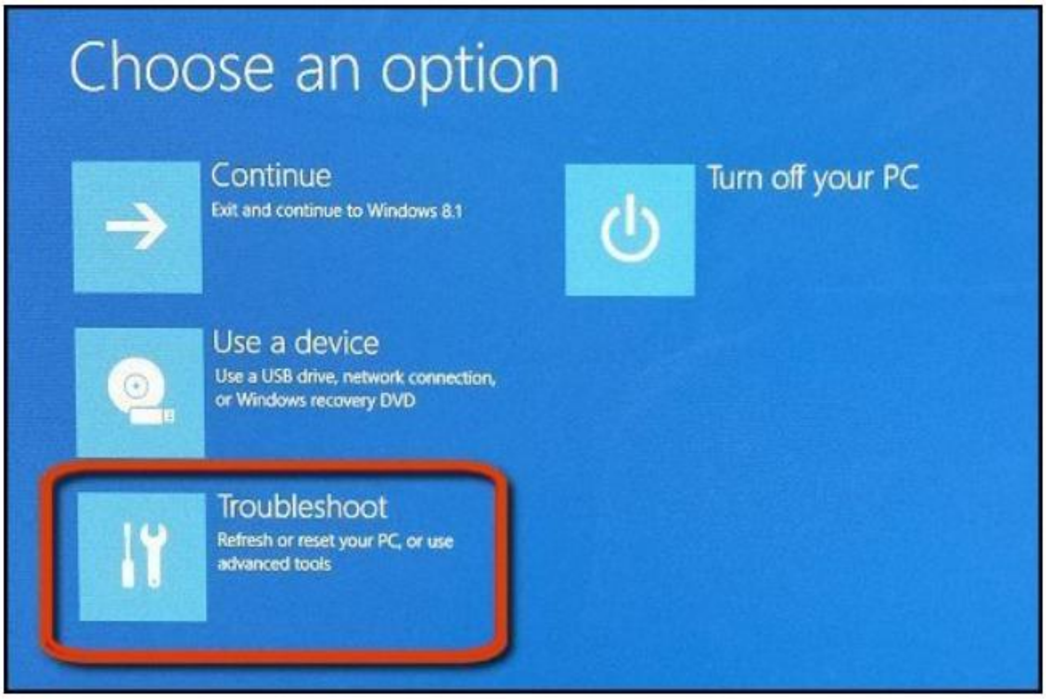
Start up from a device or disc (such as a USB drive or DVD), change your PC's firmware settings, change Windows start-up settings or restore Windows from a system image. This will restart your PC.

Restart now

More recovery options

Learn how to start afresh with a clean installation of Windows

4.After restarting, choose “**Troubleshoot**”.



Choose an option

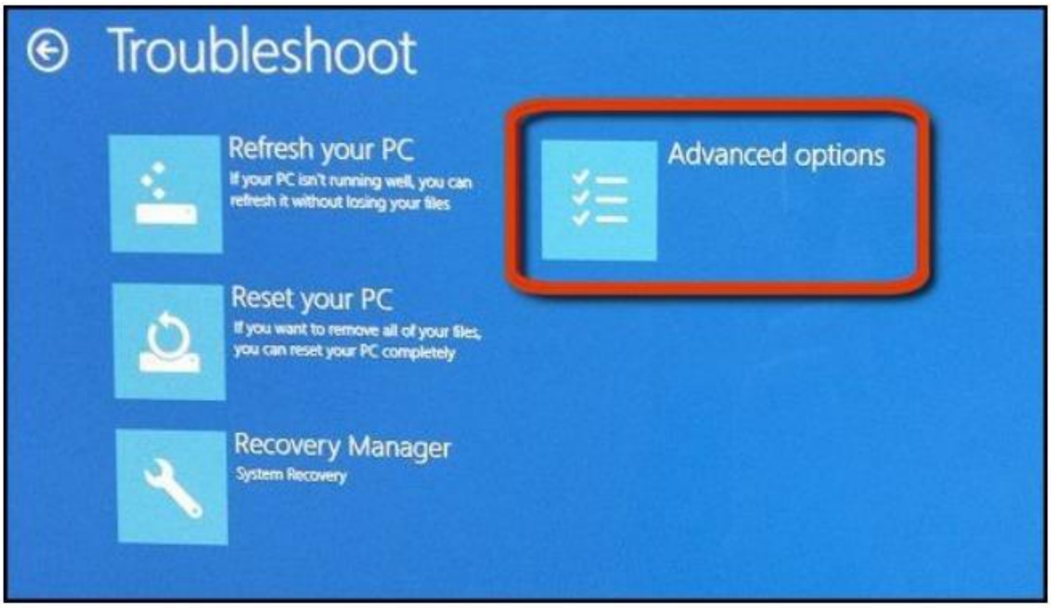
Continue
Exit and continue to Windows 8.1

Turn off your PC

Use a device
Use a USB drive, network connection, or Windows recovery DVD

Troubleshoot
Refresh or reset your PC, or use advanced tools

5.Choose “**Advanced options**”.



Troubleshoot

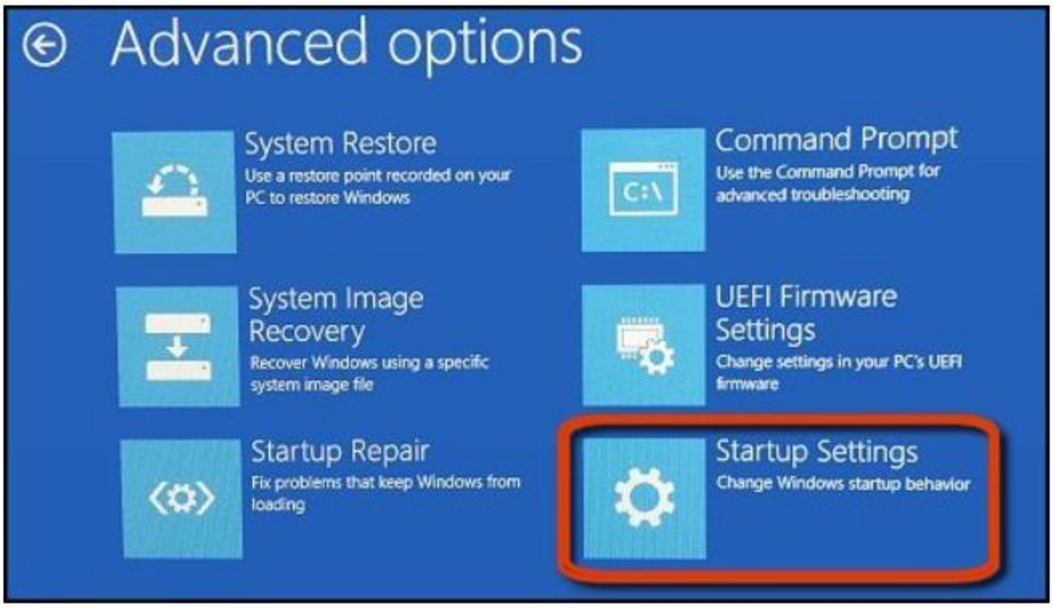
Refresh your PC
If your PC isn't running well, you can refresh it without losing your files

Reset your PC
If you want to remove all of your files, you can reset your PC completely

Recovery Manager
System Recovery

Advanced options

6.Choose "**Start-up Settings**".



Advanced options

System Restore
Use a restore point recorded on your PC to restore Windows

System Image Recovery
Recover Windows using a specific system image file

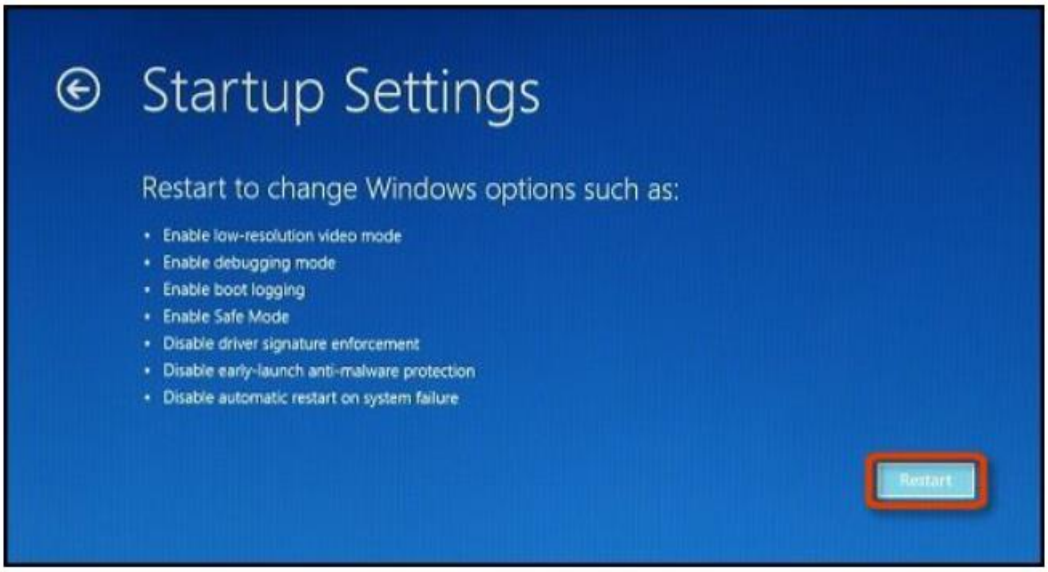
Startup Repair
Fix problems that keep Windows from loading

Command Prompt
Use the Command Prompt for advanced troubleshooting

UEFI Firmware Settings
Change settings in your PC's UEFI firmware

Startup Settings
Change Windows startup behavior

7.Click “**Restart**”.

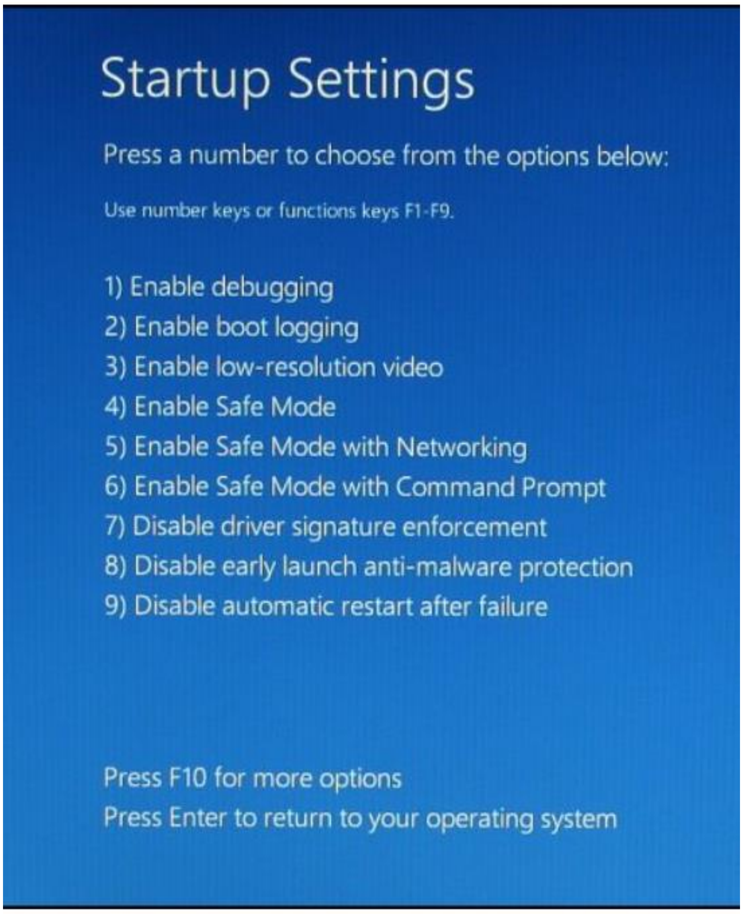


Startup Settings

Restart to change Windows options such as:

- Enable low-resolution video mode
- Enable debugging mode
- Enable boot logging
- Enable Safe Mode
- Disable driver signature enforcement
- Disable early-launch anti-malware protection
- Disable automatic restart on system failure

8.Enter "**F7**" to disable driver signature.



Startup Settings

Press a number to choose from the options below:

Use number keys or functions keys F1-F9.

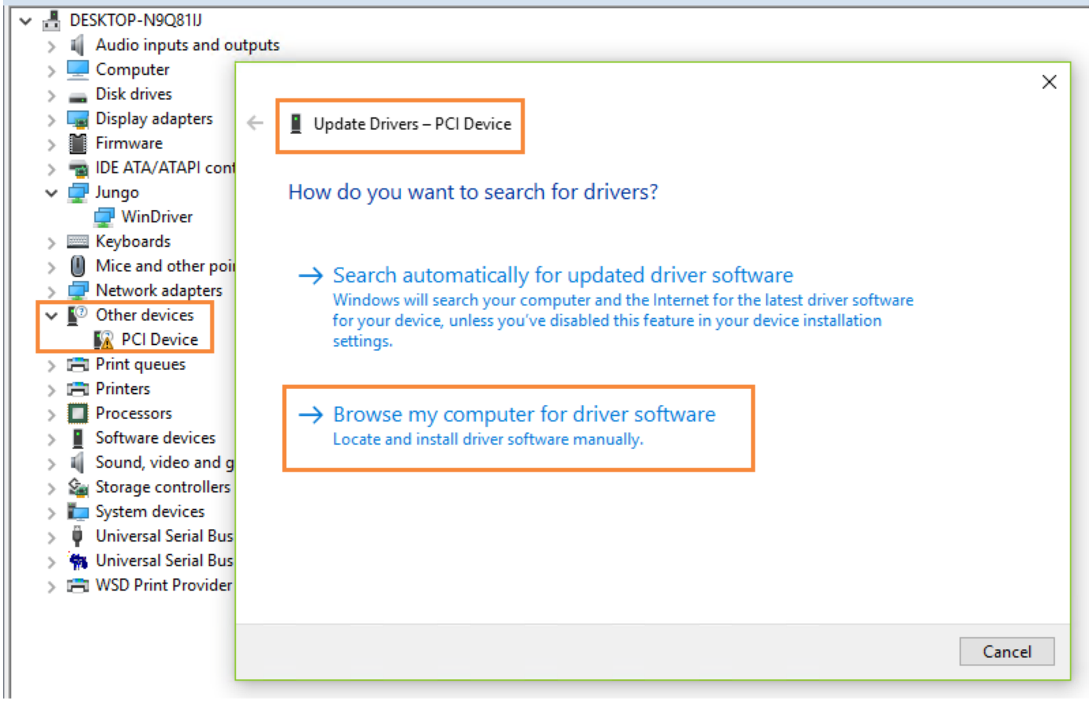
1) Enable debugging
2) Enable boot logging
3) Enable low-resolution video
4) Enable Safe Mode
5) Enable Safe Mode with Networking
6) Enable Safe Mode with Command Prompt
7) Disable driver signature enforcement
8) Disable early launch anti-malware protection
9) Disable automatic restart after failure

Press F10 for more options
Press Enter to return to your operating system

B. Install the PCI driver manually

1. After disable driver signature enforcement and restarting the system. Open the **Device Manager**, you can see a **PCI Device** with a yellow exclamation mark.

Right Click --> Update Drivers - PCI Device --> Browse my computer for driver software

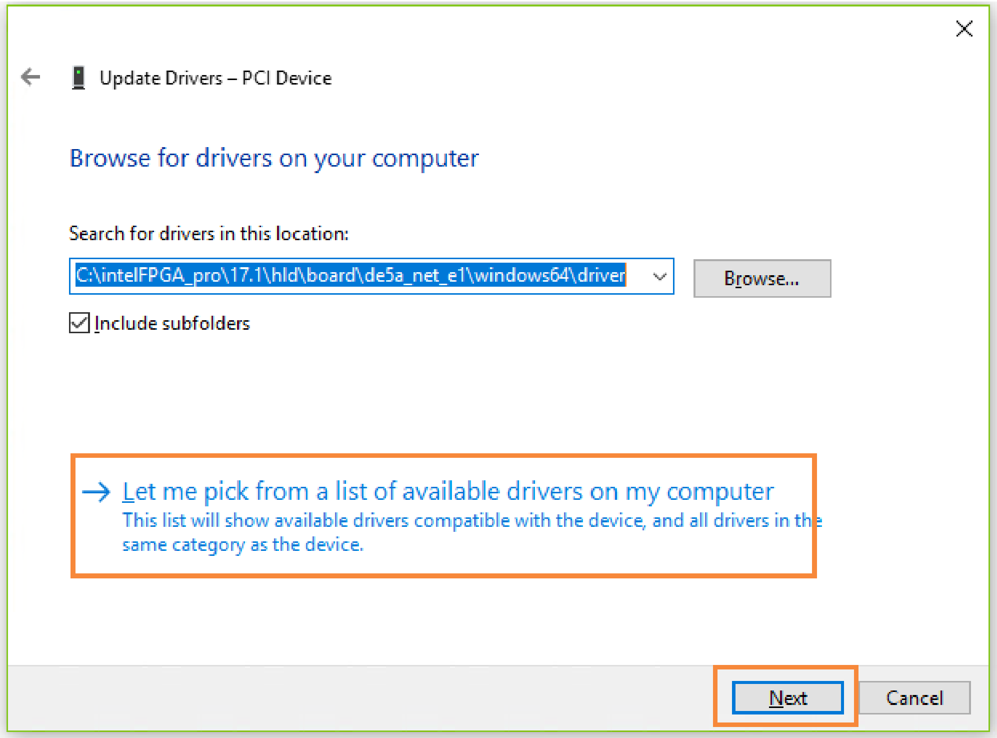


How do you want to search for drivers?

→ Search automatically for updated driver software
Windows will search your computer and the Internet for the latest driver software for your device, unless you've disabled this feature in your device installation settings.

→ Browse my computer for driver software
Locate and install driver software manually.

2.Choose "**Let me pick from a list of available drivers on my computer**", Click "**Next**".



Browse for drivers on your computer

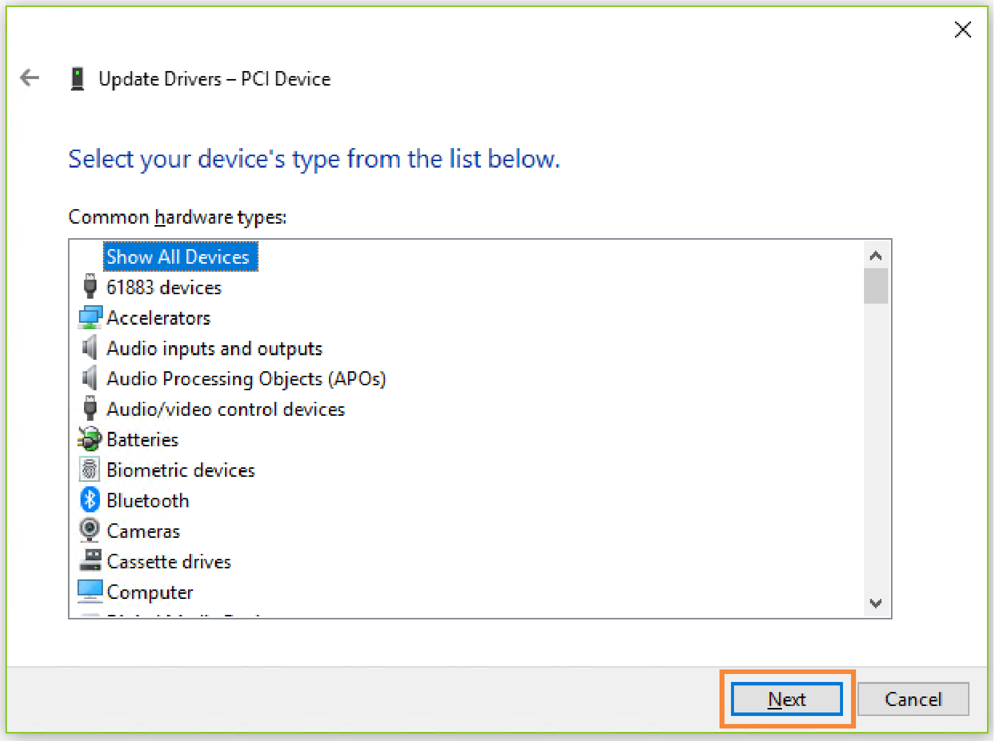
Search for drivers in this location:

C:\intelFPGA_pro\17.1\hld\board\de5a_net_e1\windows64\driver

☑ Include subfolders

→ Let me pick from a list of available drivers on my computer
This list will show available drivers compatible with the device, and all drivers in the same category as the device.

3.Continue choose “**Next**”.



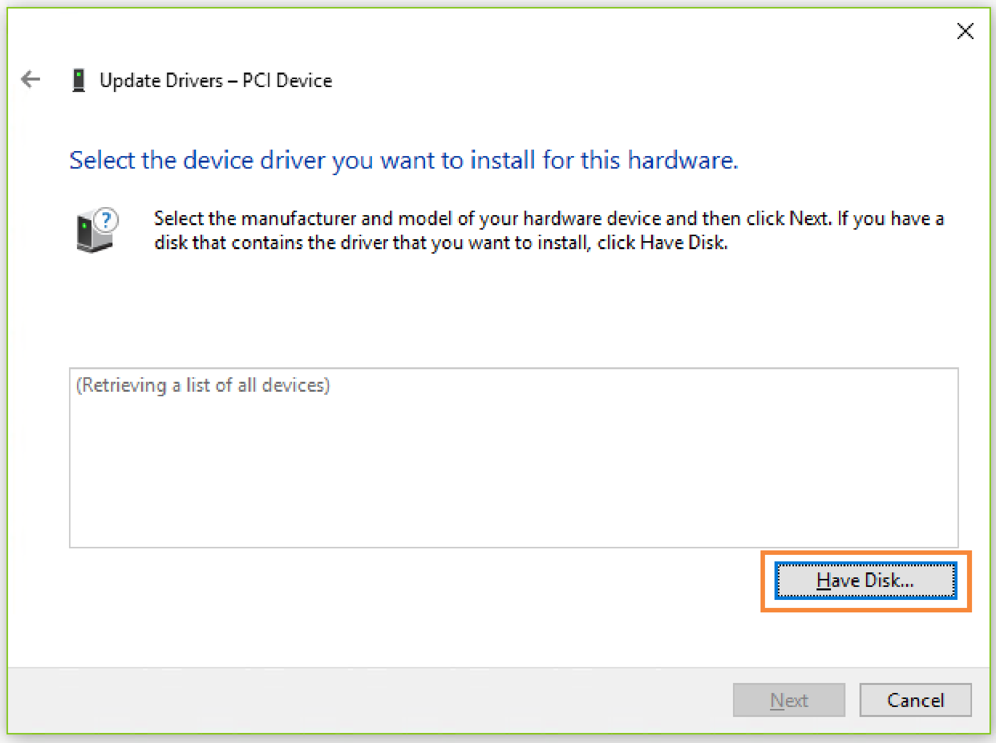
Update Drivers – PCI Device

Select your device's type from the list below.

Common hardware types:

- Show All Devices
- 61883 devices
- Accelerators
- Audio inputs and outputs
- Audio Processing Objects (APOs)
- Audio/video control devices
- Batteries
- Biometric devices
- Bluetooth
- Cameras
- Cassette drives
- Computer

4.Choose “**Have Disk ...**”



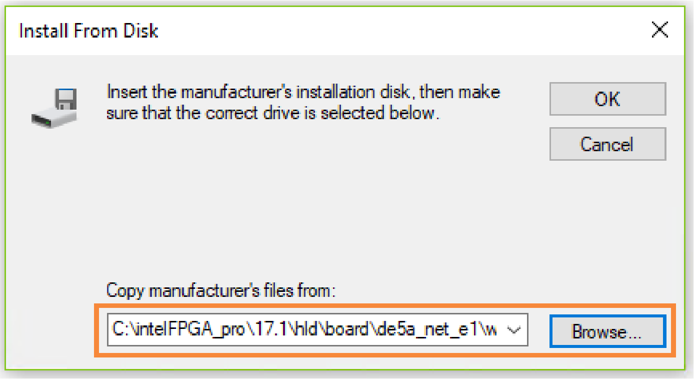
Update Drivers – PCI Device

Select the device driver you want to install for this hardware.

Select the manufacturer and model of your hardware device and then click Next. If you have a disk that contains the driver that you want to install, click Have Disk.

(Retrieving a list of all devices)

5.Click **Browse**， locate BSP to **de5a_net_e1/windows64/driver/ acl_boards_de5a_net_e1.inf**，Click “**OK**”.



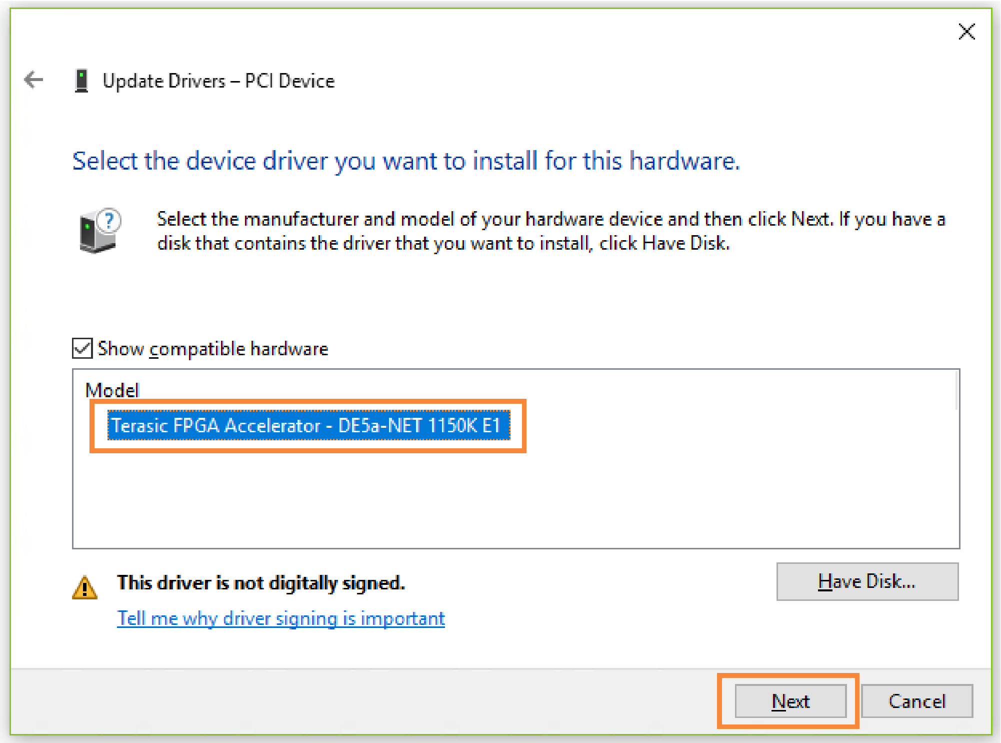
Install From Disk

Insert the manufacturer's installation disk, then make sure that the correct drive is selected below.

Copy manufacturer's files from:

C:\intelFPGA_pro\17.1\hld\board\de5a_net_e1\w

6.Select “**Terasic FPGA Accelerator-DE5a-NET 1150K E1**”, Click "**Next**" to continue the installation.



Update Drivers – PCI Device

Select the device driver you want to install for this hardware.

Select the manufacturer and model of your hardware device and then click Next. If you have a disk that contains the driver that you want to install, click Have Disk.

☑ Show compatible hardware

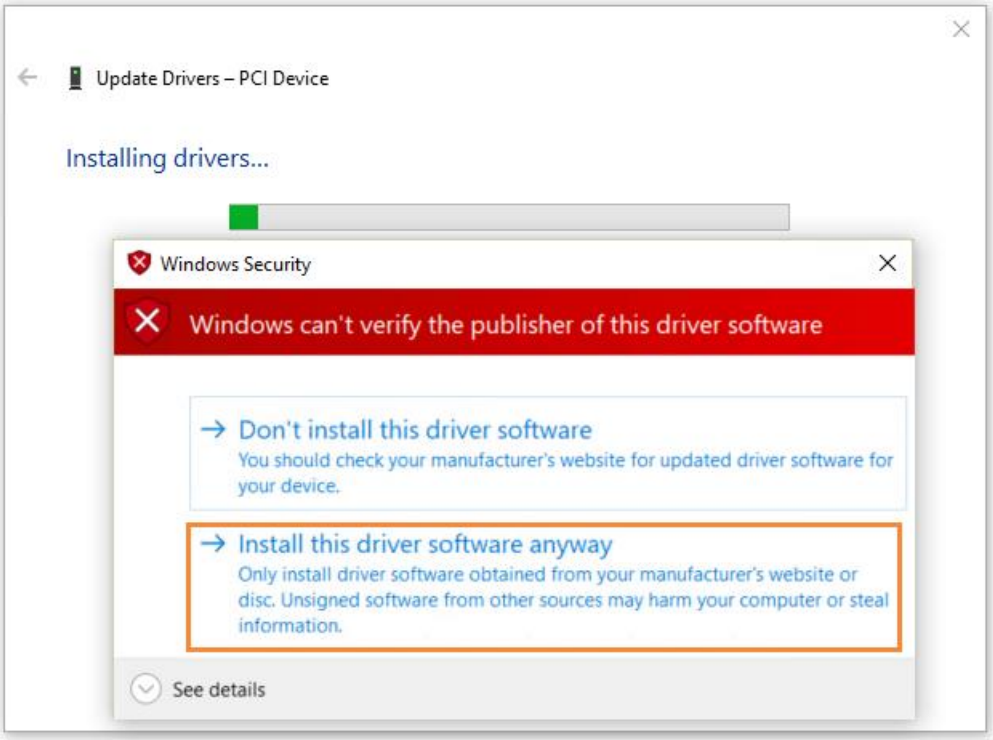
Model

Terasic FPGA Accelerator - DE5a-NET 1150K E1

This driver is not digitally signed.

Tell me why driver signing is important

7.Select “**Install this driver software anyway**” in the pop-up “**Windows Security**” window.



Update Drivers – PCI Device

Installing drivers...

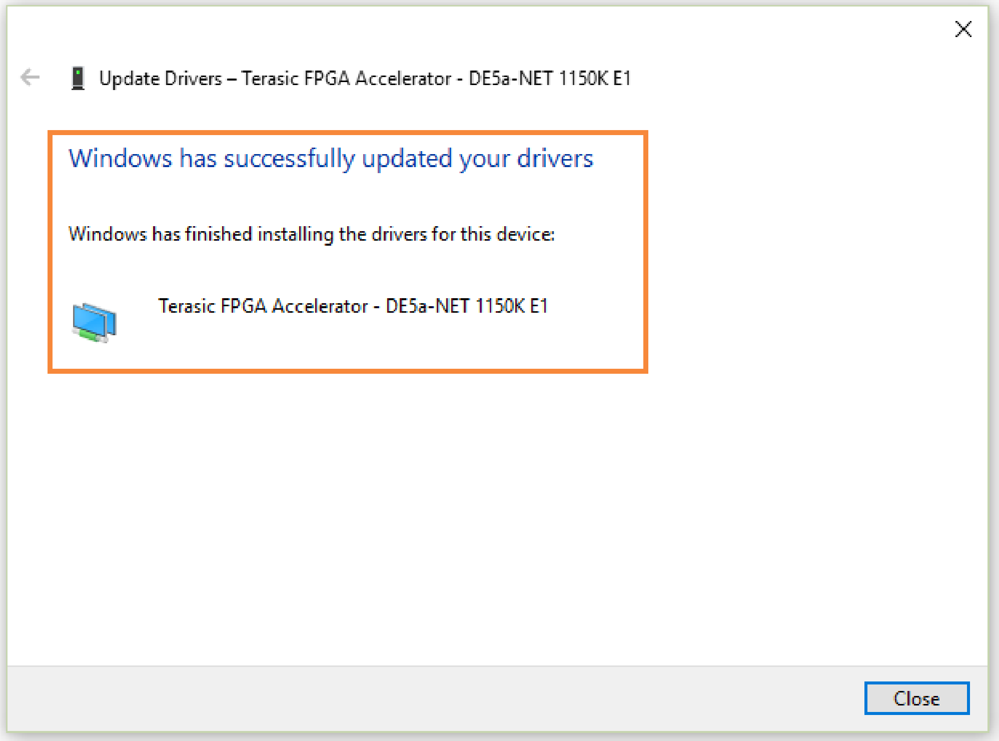
Windows Security

Windows can't verify the publisher of this driver software

→ Don't install this driver software
You should check your manufacturer's website for updated driver software for your device.

→ Install this driver software anyway
Only install driver software obtained from your manufacturer's website or disc. Unsigned software from other sources may harm your computer or steal information.

8.Installation complete.



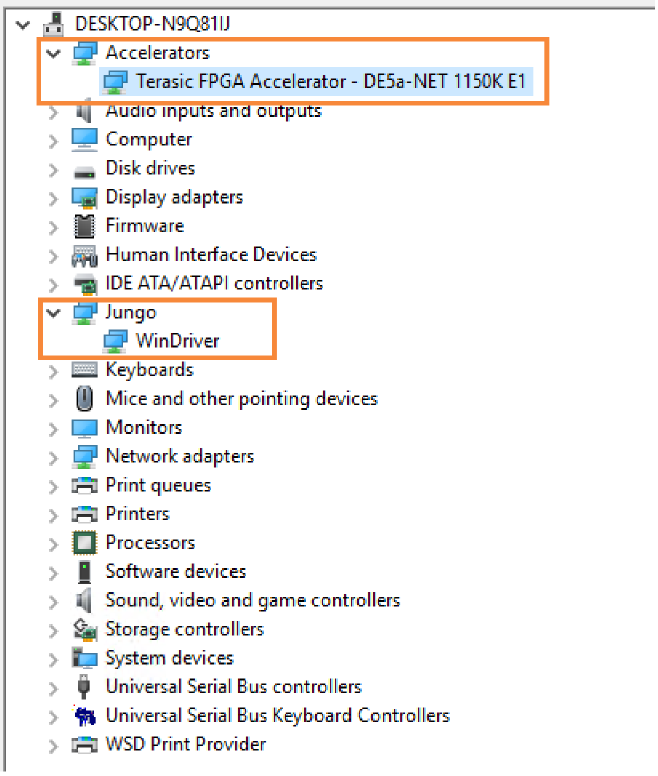
Update Drivers – Terasic FPGA Accelerator - DE5a-NET 1150K E1

Windows has successfully updated your drivers

Windows has finished installing the drivers for this device:

Terasic FPGA Accelerator - DE5a-NET 1150K E1

9.In the device manager, the **Jungo Windriver** and the DE5a-Net PCIE driver are both installed successfully.



DESKTOP-N9Q81IJ
- Accelerators
  - Terasic FPGA Accelerator - DE5a-NET 1150K E1
- Audio inputs and outputs
- Computer
- Disk drives
- Display adapters
- Firmware
- Human Interface Devices
- IDE ATA/ATAPI controllers
- Jungo
  - WinDriver
- Keyboards
- Mice and other pointing devices
- Monitors
- Network adapters
- Print queues
- Printers
- Processors
- Software devices
- Sound, video and game controllers
- Storage controllers
- System devices
- Universal Serial Bus controllers
- Universal Serial Bus Keyboard Controllers
- WSD Print Provider

Revision History

Version	*Change Log*
V1.0	**Initial Version**

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