FLIK Board

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18	FPGA Power	37	Power - 5V
19	FPGA GND	38	Power-Down Discharge
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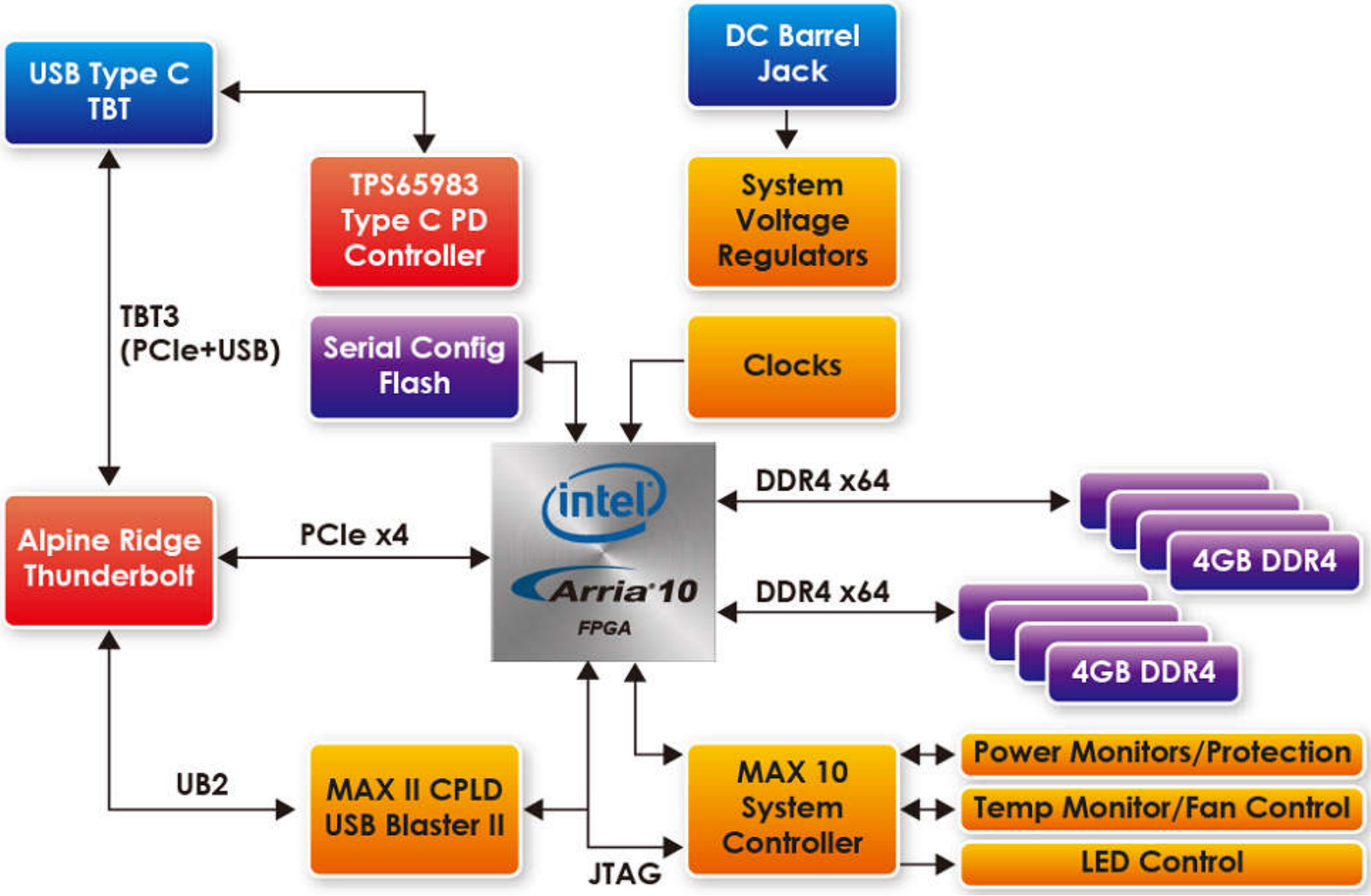
Block Diagram



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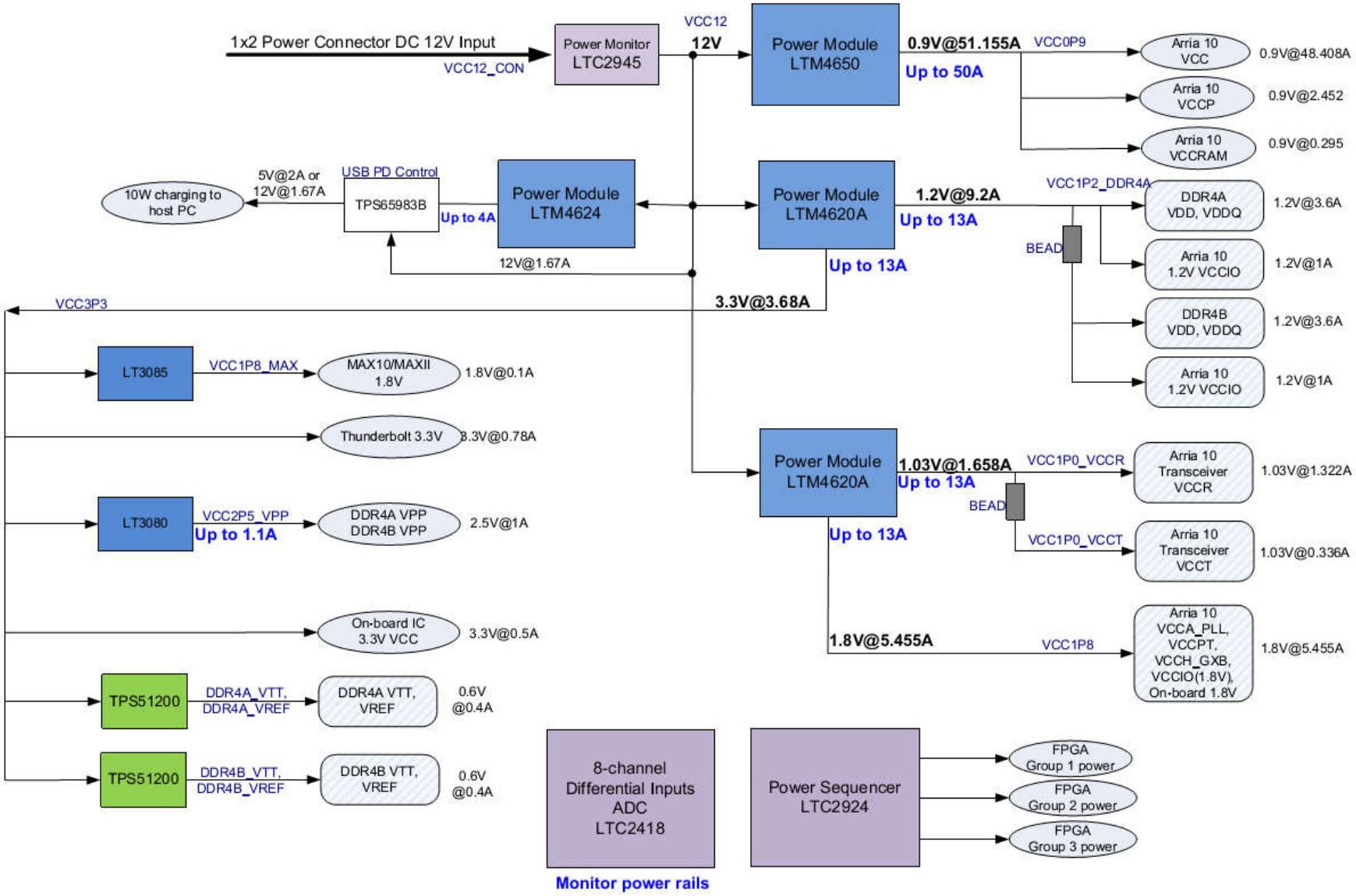
Power Tree



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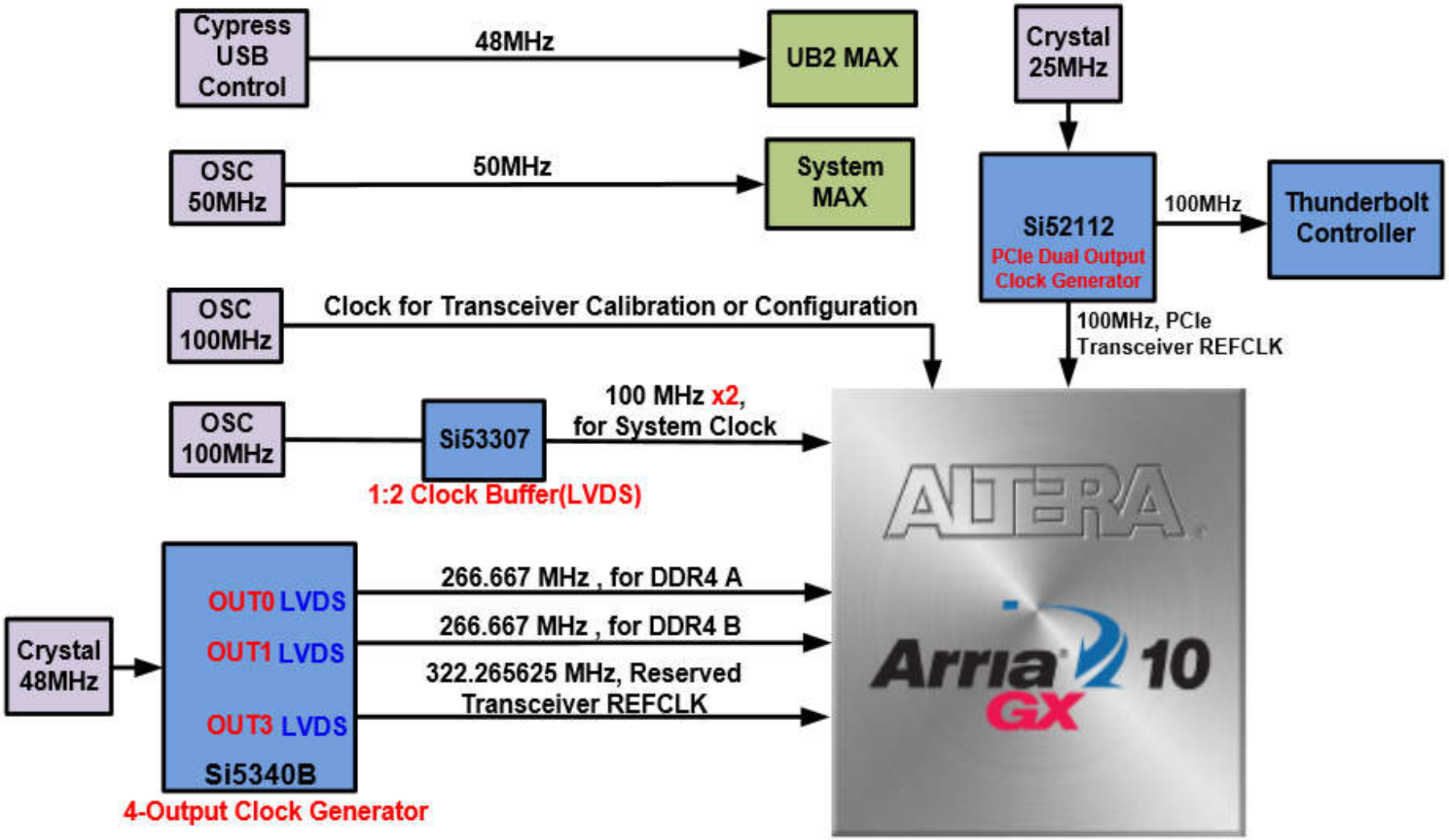
Clock Tree



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Title	FLIK	
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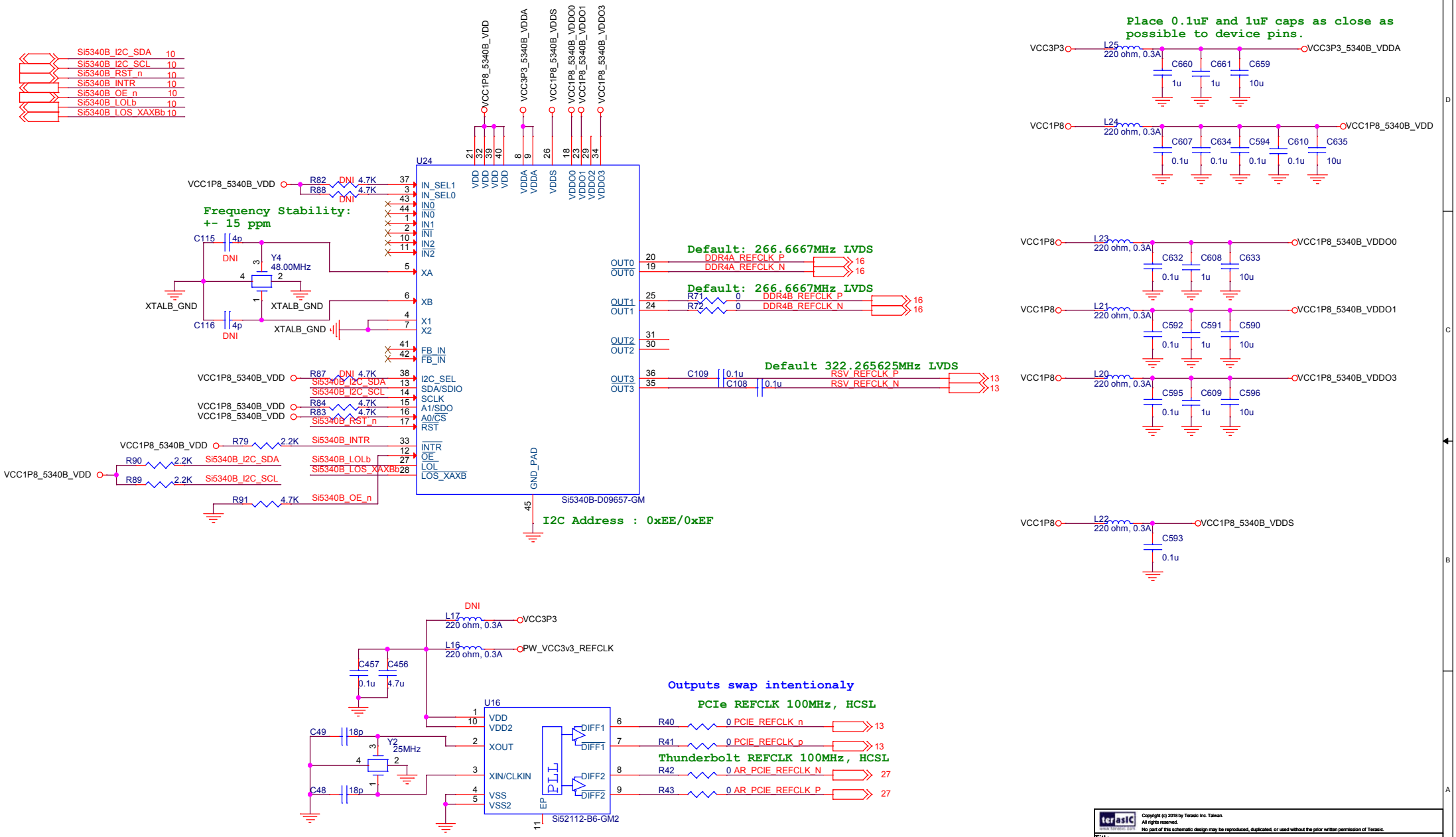

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Title: **FLIK**

Size	Document Number	Rev
B	Programmable Clock Generator	B1

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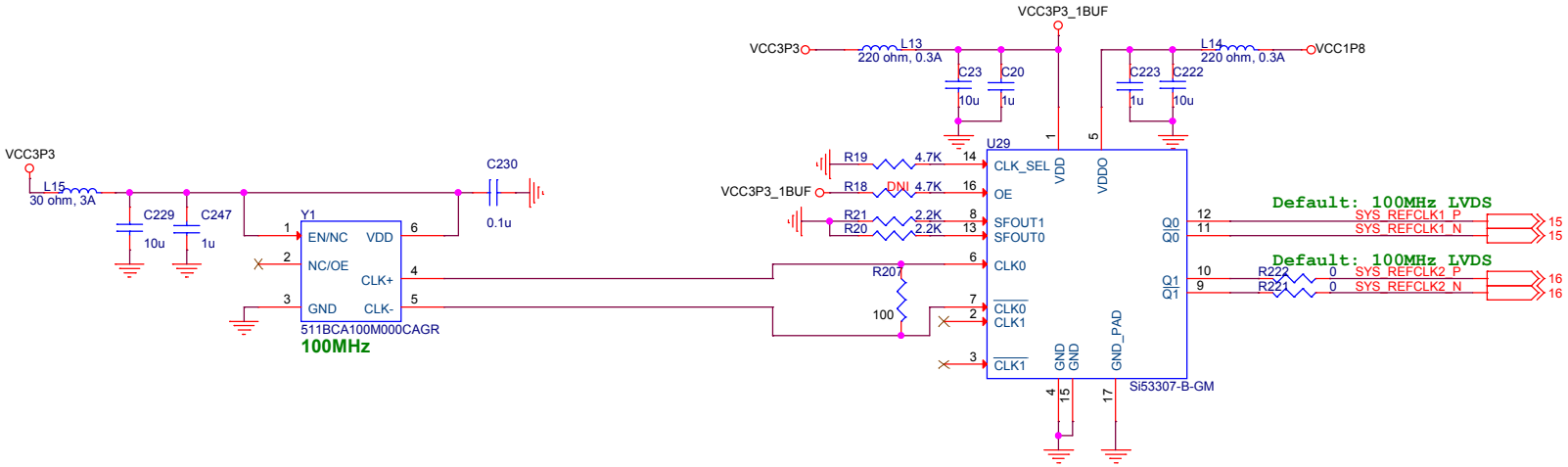
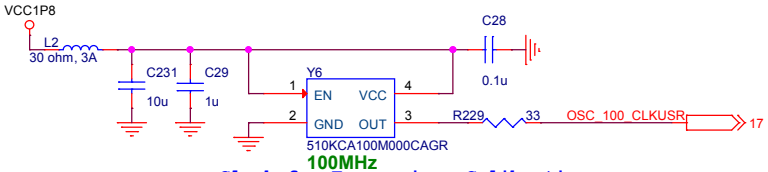
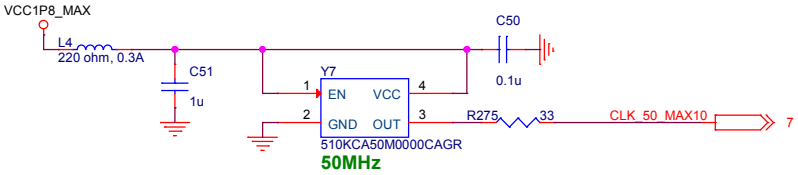




Clock for Transceiver Calibration
or Configuration



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Title
FLIK

Size	Document Number	Rev
B	Clocks from Oscillators	B1

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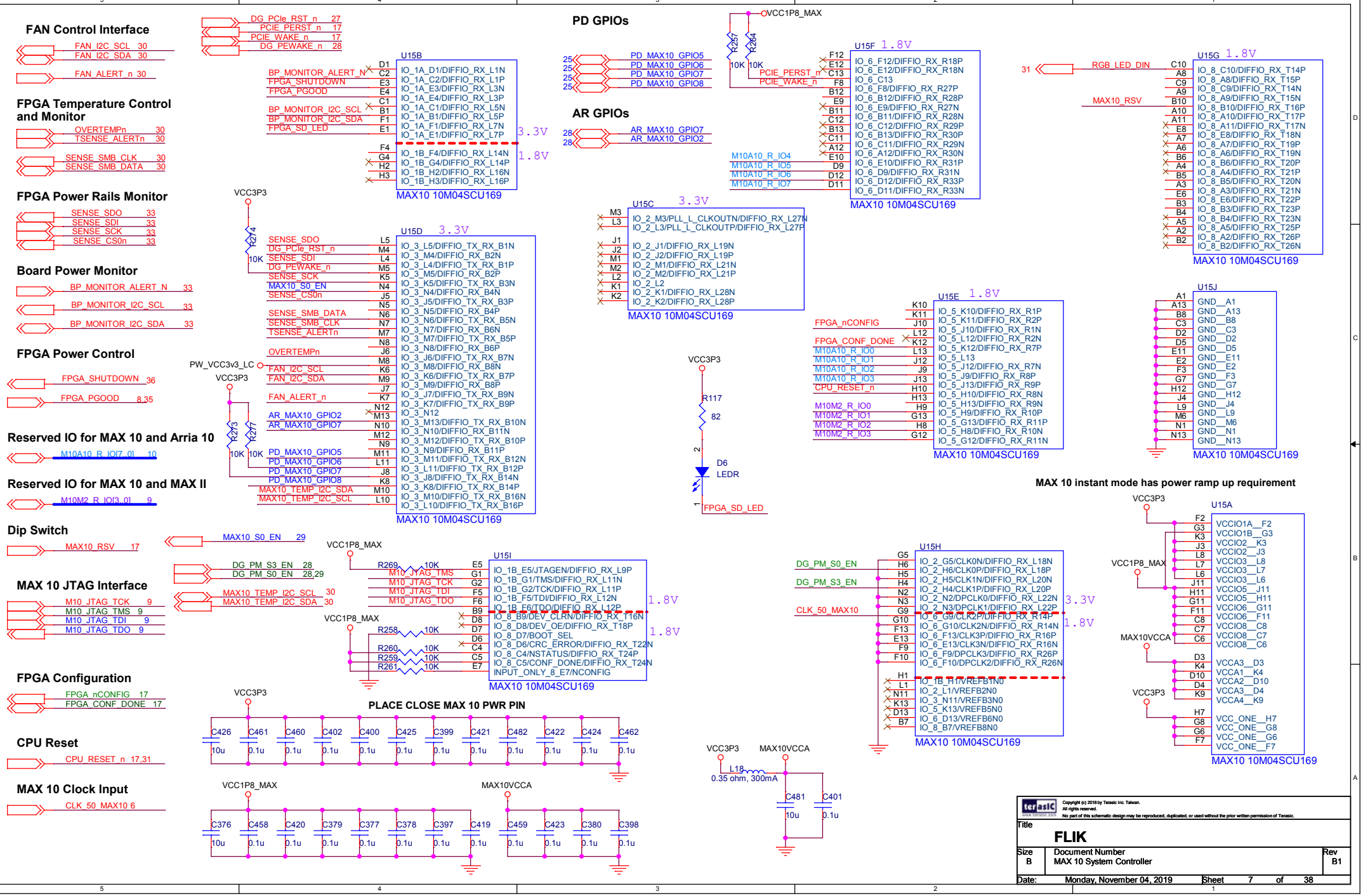
FAN Control Interface
FAN_I2C_SCL 30
FAN_I2C_SDA 30
FAN_ALERT_n 30
FPGA Temperature Control and Monitor
OVERTEMPn 30
TSENSE_ALERTn 30
SENSE_SMB_CLK 30
SENSE_SMB_DATA 30
FPGA Power Rails Monitor
SENSE_SDO 33
SENSE_SDI 33
SENSE_SCK 33
SENSE_CS0n 33
Board Power Monitor
BP_MONITOR_ALERT_N 33
BP_MONITOR_I2C_SCL 33
BP_MONITOR_I2C_SDA 33
FPGA Power Control
FPGA_SHUTDOWN 36
FPGA_PGOOD 8,35
Reserved IO for MAX 10 and Arria 10
M10A10_R_IO[7..0] 10
Reserved IO for MAX 10 and MAX II
M10M2_R_IO[3..0] 9
Dip Switch
MAX10_RSV 17
MAX10_S0_EN 29
MAX 10 JTAG Interface
M10_JTAG_TCK 9
M10_JTAG_TMS 9
M10_JTAG_TDI 9
M10_JTAG_TDO 9
FPGA Configuration
FPGA_nCONFIG 17
FPGA_CONF_DONE 17
CPU Reset
CPU_RESET_n 17,31
MAX 10 Clock Input
CLK_50_MAX10 6
DG_PCIe_RST_n 27
PCIE_PERST_n 17
PCIE_WAKE_n 17
DG_PEWAKE_n 28
U15B
MAX10 10M04SCU169
PD GPIOs
PD_MAX10_GPIO5
PD_MAX10_GPIO6
PD_MAX10_GPIO7
PD_MAX10_GPIO8
AR GPIOs
AR_MAX10_GPIO7
AR_MAX10_GPIO2
VCC1P8_MAX
R257 10K
R264 10K
U15F 1.8V
U15G 1.8V
RGB_LED_DIN
MAX10_RSV
U15C 3.3V
U15D 3.3V
VCC3P3
R214 10K
PW_VCC3v3_LC
R213 10K
R217 10K
R117 82
D6 LEDR
FPGA_SD_LED
U15E 1.8V
FPGA_nCONFIG
FPGA_CONF_DONE
CPU_RESET_n
U15J
MAX 10 instant mode has power ramp up requirement
U15A
U15I
U15H
DG_PM_S3_EN 28
DG_PM_S0_EN 28,29
MAX10_TEMP_I2C_SCL 30
MAX10_TEMP_I2C_SDA 30
R269 10K
R258 10K
R260 10K
R259 10K
R261 10K
DG_PM_S0_EN
DG_PM_S3_EN
CLK_50_MAX10
MAX10VCCA
PLACE CLOSE MAX 10 PWR PIN
C426 10u
C461 0.1u
C460 0.1u
C402 0.1u
C400 0.1u
C425 0.1u
C399 0.1u
C421 0.1u
C482 0.1u
C422 0.1u
C424 0.1u
C462 0.1u
C376 10u
C458 0.1u
C420 0.1u
C379 0.1u
C377 0.1u
C378 0.1u
C397 0.1u
C419 0.1u
C459 0.1u
C423 0.1u
C380 0.1u
C398 0.1u
L18 0.35 ohm, 300mA
C481 10u
C401 0.1u
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Title
FLIK
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MAX 10 System Controller
Rev B1
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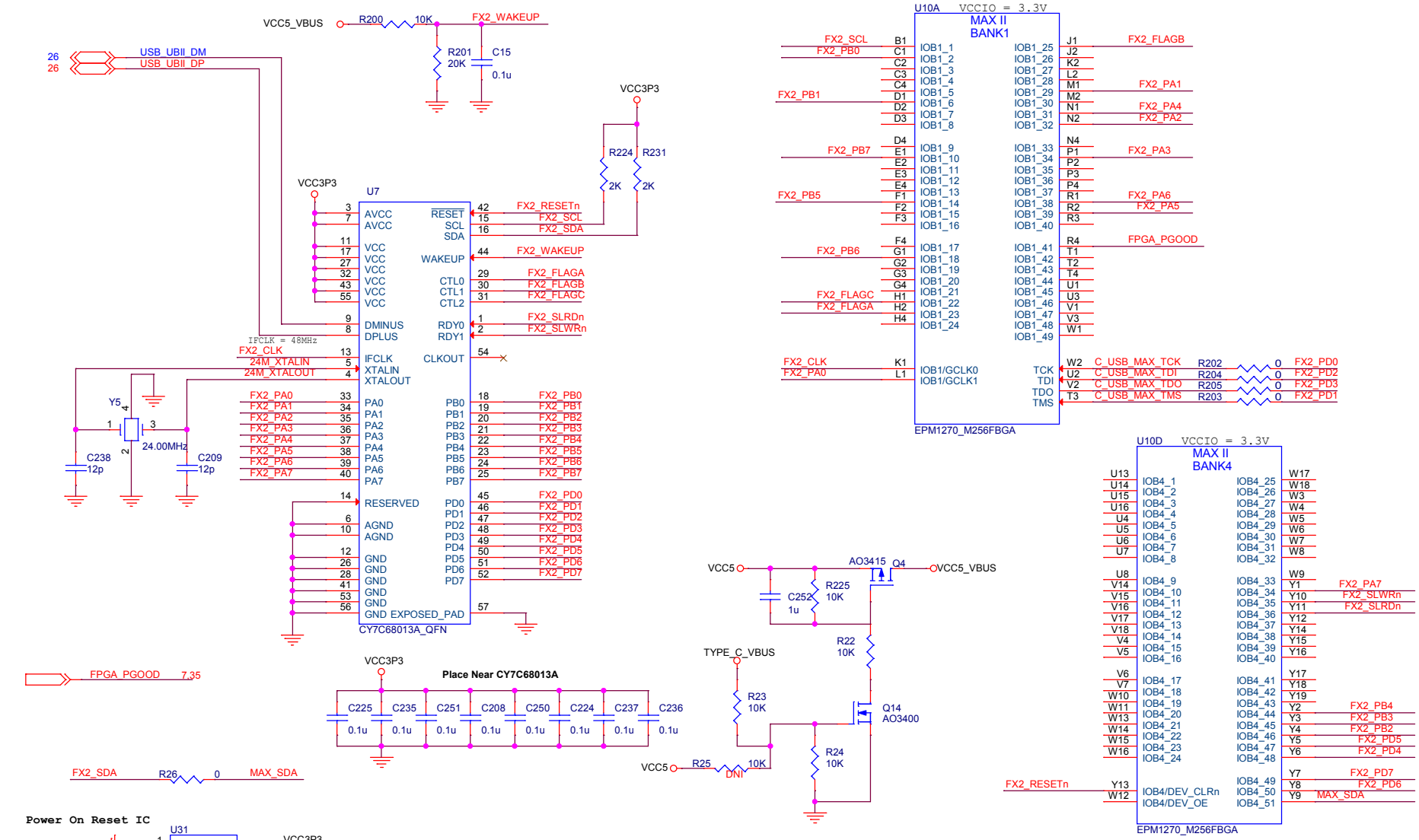
On-Board USB Blaster II - Part 1



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Title
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Size	Document Number	Rev
B	USB Blaster II - 1	B1

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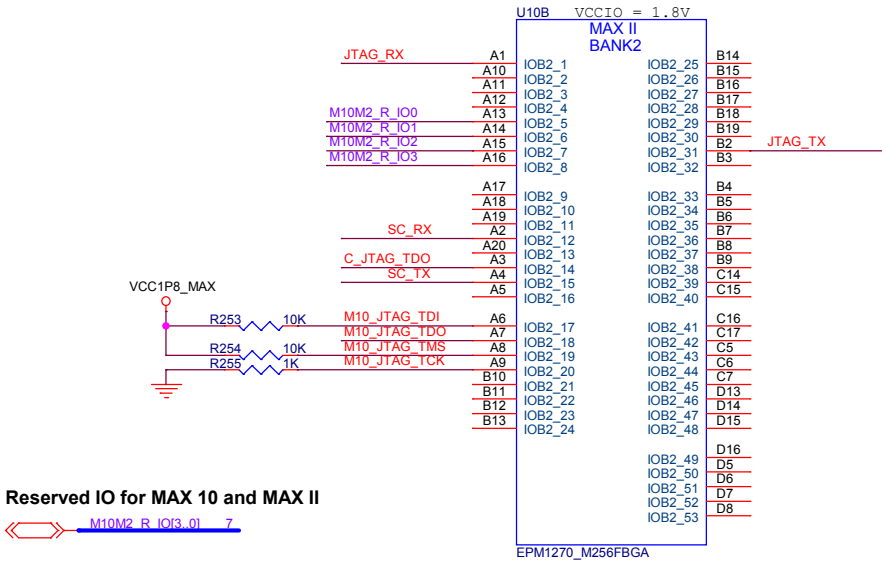
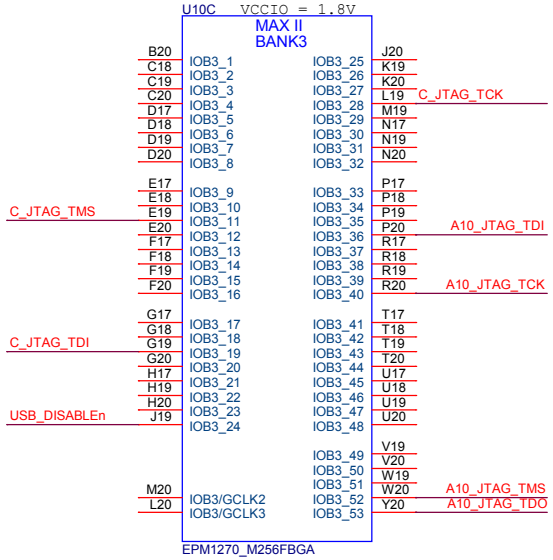
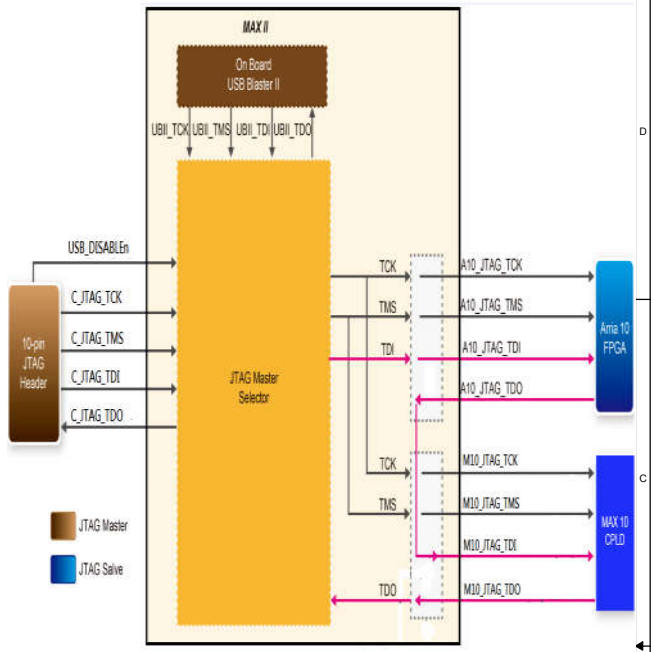
On-Board USB Blaster II - Part 2



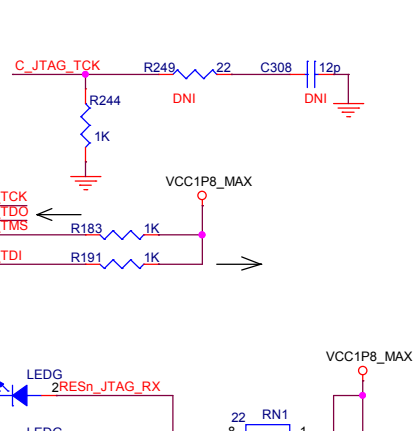


FLIK JTAG Chain



Reserved IO for MAX 10 and MAX II

M10M2_R_IO[3..0] 7

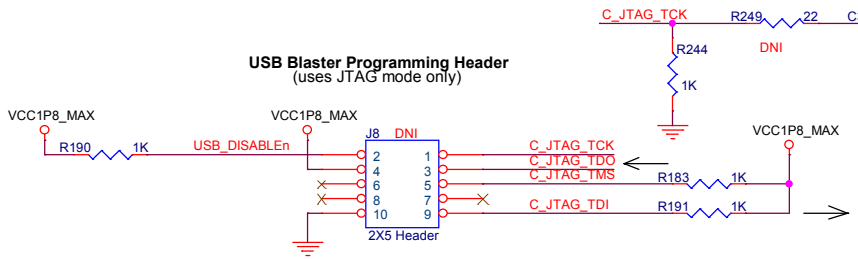


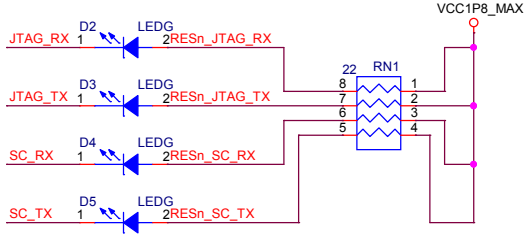
JTAG INTERFACE

A10_JTAG_TCK 17
A10_JTAG_TMS 17
A10_JTAG_TDO 17
A10_JTAG_TDI 17

M10_JTAG_TCK 7
M10_JTAG_TMS 7
M10_JTAG_TDO 7
M10_JTAG_TDI 7

USB Blaster Programming Header
(uses JTAG mode only)





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Reserved IO for MAX 10 and Arria 10

M10A10_R_IO[7..0] 7

USER LEDS

LED[4..1] 15,31

Debug Interface

DEBUG[16..1] 15,31

Si5340B Interface

Si5340B_I2C_SDA 5
Si5340B_I2C_SCL 5
Si5340B_RST_n 5
Si5340B_INTR 5
Si5340B_OE_n 5
Si5340B_LOLb 5
Si5340B_LOS_XAXBb 5

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ARRIA 10 BANK 2I

VCCIO = 1.8V

		AK21	LVDS2I_14P/DQ14/DQ7/20
		AK22	LVDS2I_14N/DQ14/DQ7/21
		AG20	LVDS2I_16P/DQS14/CQ14/DQ7/16
		AG21	LVDS2I_16N/DQSN14/CQN14/DQ7/17
		AH22	LVDS2I_17P/DQ14/DQ7/14
		AG22	LVDS2I_17N/DQ14/DQ7/15
		AF20	LVDS2I_18P/DQ14/DQS7/CQ7/12
		AE20	LVDS2I_18N/DQ14/DQSN7/CQN7/13
AU22	LVDS2I_7P/DQ13/DQ6/34		
AT22	LVDS2I_7N/DQ13/DQ6/35		
AR23	LVDS2I_8P/DQ13/DQ6/32		
AR22	LVDS2I_8N/DQ13/DQ6/33		
AM22	LVDS2I_9P/DQ13/DQ6/30		
AL22	LVDS2I_9N/DQ13/DQ6/31		
AN21	RZQ_2I/LVDS2I_11P/DQ13/DQ6/26		
AN22	LVDS2I_11N/DQ13/DQ6/27		

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ARRIA 10 BANK 2K

VCCIO = 1.8V

N25	LVDS2K_1P/DQ4/DQ2/46				
P25	LVDS2K_1N/DQ4/DQ2/47				
K26	LVDS2K_2P/DQ4/DQ2/44			D23	LED1
L26	LVDS2K_2N/DQ4/DQ2/45		LVDS2K_14P/DQ6/DQ3/20	E23	LED4
L25	LVDS2K_3P/DQ4/DQ2/42		LVDS2K_14N/DQ6/DQ3/21		
M25	LVDS2K_3N/DQ4/DQ2/43				
K25	LVDS2K_4P/DQS4/CQ4/DQ2/40		LVDS2K_16P/DQS6/CQ6/DQ3/16	C25	DEBUG14
L24	LVDS2K_4N/DQSN4/CQN4/DQ2/41		LVDS2K_16N/DQSN6/CQN6/DQ3/17	B24	DEBUG8
M24	LVDS2K_5P/DQ4/DQ2/38		LVDS2K_17P/DQ6/DQ3/14	C22	DEBUG11
N24	LVDS2K_5N/DQ4/DQ2/39		LVDS2K_17N/DQ6/DQ3/15	C21	DEBUG10
J26	LVDS2K_6P/DQ4/DQS2/CQ2/36		LVDS2K_18P/DQ6/DQS3/CQ3/12	B26	DEBUG9
J25	LVDS2K_6N/DQ4/DQSN2/CQN2/37		LVDS2K_18N/DQ6/DQSN3/CQN3/13	C26	DEBUG15
H24	LVDS2K_7P/DQ5/DQ2/34		LVDS2K_19P/DQ7/DQ3/10	A17	DEBUG16
J24	LVDS2K_7N/DQ5/DQ2/35		LVDS2K_19N/DQ7/DQ3/11	A18	
LED3 D25	LVDS2K_8P/DQ5/DQ2/32		LVDS2K_20P/DQ7/DQ3/8	B20	
E25	LVDS2K_8N/DQ5/DQ2/33		LVDS2K_20N/DQ7/DQ3/9	B19	
F24	LVDS2K_9P/DQ5/DQ2/30		LVDS2K_21P/DQ7/DQ3/6	A24	DEBUG4
F23	LVDS2K_9N/DQ5/DQ2/31		LVDS2K_21N/DQ7/DQ3/7	A23	DEBUG3
			LVDS2K_22P/DQS7/CQ7/DQ3/4	A26	DEBUG6
			LVDS2K_22N/DQSN7/CQN7/DQ3/5	A25	DEBUG5
E26	RZQ_2K/LVDS2K_11P/DQ5/DQ2/26		LVDS2K_23P/DQ7/DQ3/2	A22	
F26	LVDS2K_11N/DQ5/DQ2/DQ5/27		LVDS2K_23N/DQ7/DQ3/3	B21	
			LVDS2K_24P/DQ7/DQ3/0	A20	DEBUG2
			LVDS2K_24N/DQ7/DQ3/1	A19	DEBUG1

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ARRIA 10 BANK 2J

VCCIO = 1.8V

AV27	LVDS2J_1P/DQ8/DQ4/46		
AV26	LVDS2J_1N/DQ8/DQ4/47		
AU28	LVDS2J_2P/DQ8/DQ4/44		
AU27	LVDS2J_2N/DQ8/DQ4/45	LVDS2J_14P/DQ10/DQ5/20	AN24
AW28	LVDS2J_3P/DQ8/DQ4/42	LVDS2J_14N/DQ10/DQ5//21	AN23
AV28	LVDS2J_3N/DQ8/DQ4/43		
AW26	LVDS2J_4P/DQS8/CQ8/DQ4/40	LVDS2J_16P/DQS10/CQ10/DQ5/16	AM25
AW25	LVDS2J_4N/DQSN8/CQN8/DQ4/41	LVDS2J_16N/DQSN10/CQN10/DQ5/17	AL25
AW24	LVDS2J_5P/DQ8/DQ4/38	LVDS2J_17P/DQ10/DQ5/14	AL23
AV24	LVDS2J_5N/DQ8/DQ4/39	LVDS2J_17N/DQ10/DQ5/15	AK23
AW23	LVDS2J_6P/DQ8/DQS4/CQ4/36	LVDS2J_18P/DQ10/DQS5/CQ5/12	AL24
AV23	LVDS2J_6N/DQ8/DQSN4/CQN4/37	LVDS2J_18N/DQ10/DQSN5/CQN5/13	AM24
AU26			AJ26
AU25	LVDS2J_7P/DQ9/DQ4/34	LVDS2J_19P/DQ11/DQ5/10	AH25
AT26	LVDS2J_7N/DQ9/DQ4/35	LVDS2J_19N/DQ11/DQ5/11	AH24
AR26	LVDS2J_8P/DQ9/DQ4/32	LVDS2J_20P/DQ11/DQ5/8	AH23
AU24	LVDS2J_8N/DQ9/DQ4/33	LVDS2J_20N/DQ11/DQ5/9	AJ24
AT23	LVDS2J_9P/DQ9/DQ4/30	LVDS2J_21P/DQ11/DQ5/6	AJ23
	LVDS2J_9N/DQ9/DQ4/31	LVDS2J_21N/DQ11/DQ5/7	AK25
		LVDS2J_22P/DQS11/CQ11/DQ5/4	AJ25
		LVDS2J_22N/DQSN11/CQN11/DQ5/5	AG25
AR25	RZQ_2J/LVDS2J_11P/DQ9/DQ4/26	LVDS2J_23P/DQ11/DQ5/2	AF25
AP25	LVDS2J_11N/DQ9/DQ4/27	LVDS2J_23N/DQ11/DQ5/3	AG24
		LVDS2J_24P/DQ11/DQ5/0	AF24
		LVDS2J_24N/DQ11/DQ5/1	

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ARRIA 10 BANK 2L

VCCIO = 1.8V

	LVDS2L_1P/DQ0/DQ0/46				
	LVDS2L_1N/DQ0/DQ0/47				
Si5340B_I2C_SDA M22	LVDS2L_2P/DQ0/DQ0/44		LVDS2L_14P/DQ2/DQ1/20	F19	
Si5340B_I2C_SCL M21	LVDS2L_2N/DQ0/DQ0/45		LVDS2L_14N/DQ2/DQ1/21	G19	
K22	LVDS2L_3P/DQ0/DQ0/42				
Si5340B_RST_n L22	LVDS2L_3N/DQ0/DQ0/43				
Si5340B_INTR N23	LVDS2L_4P/DQS0/CQ0/DQ0/40		LVDS2L_16P/DQS2/CQ2/DQ1/16	E20	
Si5340B_LOLb N22	LVDS2L_4N/DQSN0/CQN0/DQ0/41		LVDS2L_16N/DQSN2/CQN2/DQ1/17	F20	
Si5340B_OE_n K23	LVDS2L_5P/DQ0/DQ0/38		LVDS2L_17P/DQ2/DQ1/14	F18	
Si5340B_LOS_XAXBb L23	LVDS2L_5N/DQ0/DQ0/39		LVDS2L_17N/DQ2/DQ1/15	G17	
M10A10_R_IO4 N20	LVDS2L_6P/DQ0/DQS0/CQ0/36		LVDS2L_18P/DQ2/DQS1/CQ1/12	H18	
M10A10_R_IO5 P20	LVDS2L_6N/DQ0/DQSN0/CQN0/37		LVDS2L_18N/DQ2/DQSN1/CQN1/13	H19	
M10A10_R_IO6 L20					
M10A10_R_IO7 M20					
M10A10_R_IO0 K21	LVDS2L_7P/DQ1/DQ0/34		LVDS2L_19P/DQ3/DQ1/10	E21	
M10A10_R_IO1 K20	LVDS2L_7N/DQ1/DQ0/35		LVDS2L_19N/DQ3/DQ1/11	E22	
M10A10_R_IO2 H23	LVDS2L_8P/DQ1/DQ0/32		LVDS2L_20P/DQ3/DQ1/DQ3/8	D21	
M10A10_R_IO3 J23	LVDS2L_8N/DQ1/DQ0/33		LVDS2L_20N/DQ3/DQ1/9	D20	
J18	LVDS2L_9P/DQ1/DQ0/30		LVDS2L_21P/DQ3/DQ1/6	C17	
J19	LVDS2L_9N/DQ1/DQ0/31		LVDS2L_21N/DQ3/DQ1/7	C18	
			LVDS2L_22P/DQS3/CQ3/DQ1/4	E17	
			LVDS2L_22N/DQSN3/CQN3/DQ1/5	F17	
H22	RZQ_2L/LVDS2L_11P/DQ1/DQ0/26		LVDS2L_23P/DQ3/DQ1/2	C19	
H21	LVDS2L_11N/DQ1/DQ0/27		LVDS2L_23N/DQ3/DQ1/3	D19	
			LVDS2L_24P/DQ3/DQ1/0	D18	
			LVDS2L_24N/DQ3/DQ1/1	E18	

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Title: FLIK

Size	Document Number	Rev
B	FPGA Bank 2I, 2J, 2K, 2L	B1

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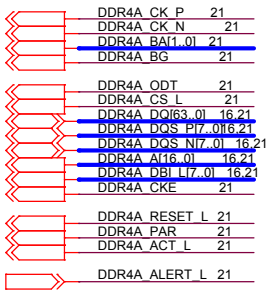
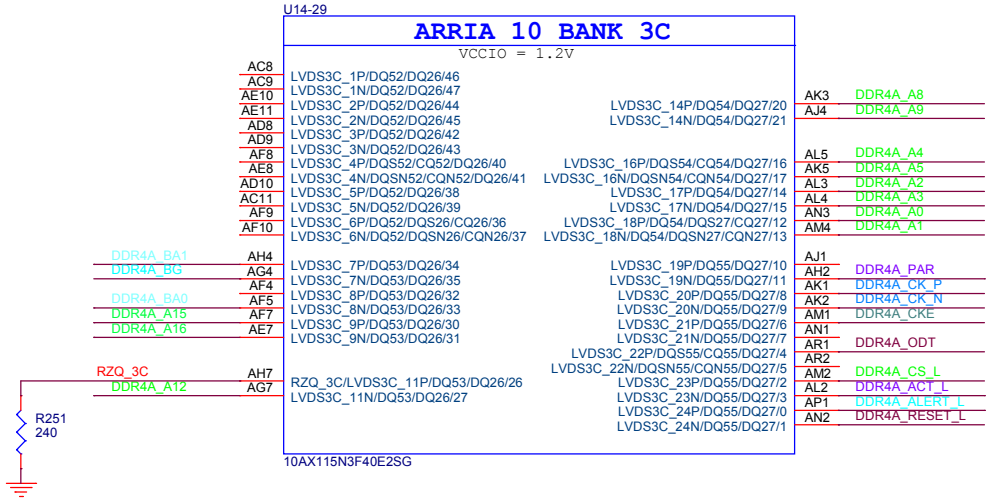
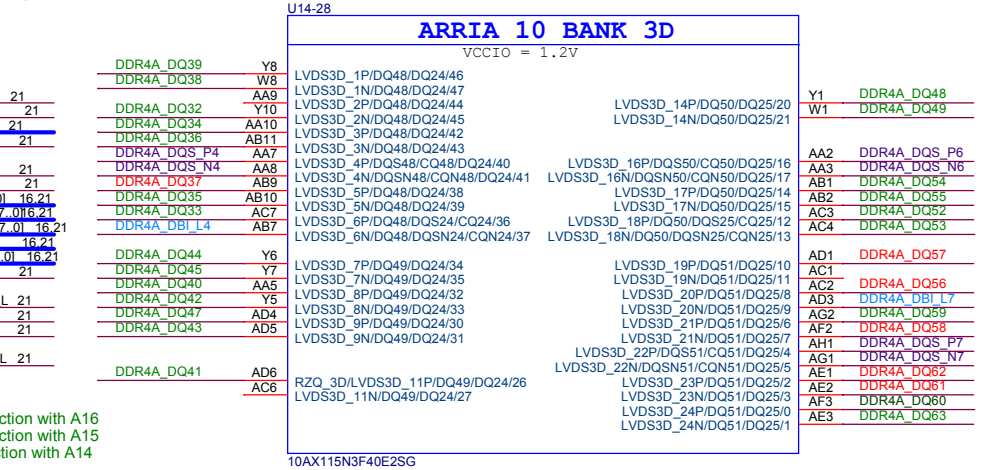
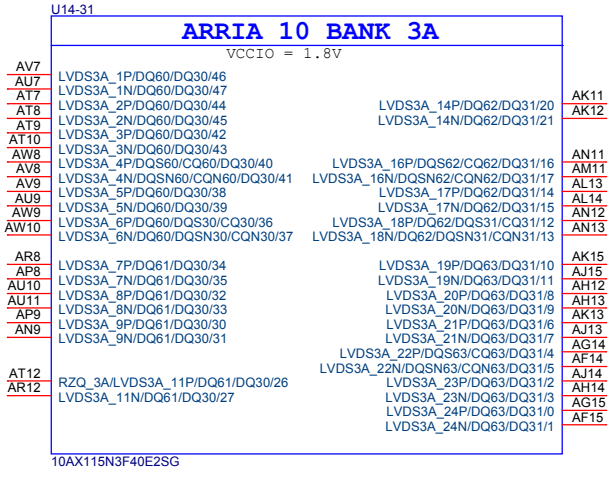
DDR4 SDRAM - A

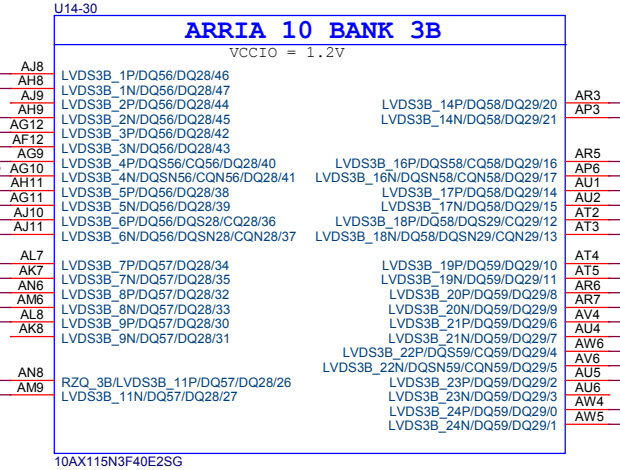


RAS_n is a multiplexed function with A16
CAS_n is a multiplexed function with A15
WE_n is a multiplexed function with A14









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Title: **FLIK**

Size	Document Number	Rev
B	FPGA Bank 3A, 3B, 3C, 3D	B1

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DDR4 SDRAM - B

DDR4B_CK_P 22
DDR4B_CK_N 22
DDR4B_BA[1..0] 22
DDR4B_BG 22

DDR4B_ODT 22
DDR4B_CS_L 22
DDR4B_DQ[63..0] 16,22
DDR4B_DQS_P[7..0] 16,22
DDR4B_DQS_N[7..0] 16,22
DDR4B_A[16..0] 16,22
DDR4B_DBI_L[7..0] 16,22
DDR4B_CKE 22

DDR4B_RESET_L 22
DDR4B_PAR 22
DDR4B_ACT_L 22

DDR4B_ALERT_L 22

RAS_n is a multiplexed function with A16
CAS_n is a multiplexed function with A15
WE_n is a multiplexed function with A14

U14-27 ARRIA 10 BANK 3E

VCCIO = 1.2V

DDR4B_DQ29	M1	LVDS3E_1P/DQ44/DQ22/46			
DDR4B_DQ31	M2	LVDS3E_1N/DQ44/DQ22/47			
DDR4B_DQ25	N3	LVDS3E_2P/DQ44/DQ22/44	LVDS3E_14P/DQ46/DQ23/20	T2	DDR4B_DQ8
DDR4B_DBI_L3	N4	LVDS3E_2N/DQ44/DQ22/45	LVDS3E_14N/DQ46/DQ23/21	T3	
DDR4B_DQ26	R2	LVDS3E_3P/DQ44/DQ22/42			
DDR4B_DQ30	R3	LVDS3E_3N/DQ44/DQ22/43			
DDR4B_DQS_P3	N1	LVDS3E_4P/DQS44/CQ44/DQ22/40	LVDS3E_16P/DQS46/CQ46/DQ23/16	V1	DDR4B_DQS_P1
DDR4B_DQS_N3	N2	LVDS3E_4N/DQSN44/CQN44/DQ22/41	LVDS3E_16N/DQSN46/CQN46/DQ23/17	V2	DDR4B_DQS_N1
DDR4B_DQ27	P1	LVDS3E_5P/DQ44/DQ22/38	LVDS3E_17P/DQ46/DQ23/14	W3	DDR4B_DQ14
DDR4B_DQ28	R1	LVDS3E_5N/DQ44/DQ22/39	LVDS3E_17N/DQ46/DQ23/15	W4	DDR4B_DQ15
DDR4B_DQ24	P3	LVDS3E_6P/DQ44/DQS22/CQ22/36	LVDS3E_18P/DQ46/DQS23/CQ23/12	V3	DDR4B_DQ13
	P4	LVDS3E_6N/DQ44/DQSN22/CQN22/37	LVDS3E_18N/DQ46/DQSN23/CQN23/13	V4	DDR4B_DQ11
DDR4B_DQ22	P5	LVDS3E_7P/DQ45/DQ22/34	LVDS3E_19P/DQ47/DQ23/10	U9	DDR4B_DQ0
DDR4B_DQ20	P6	LVDS3E_7N/DQ45/DQ22/35	LVDS3E_19N/DQ47/DQ23/11	U10	DDR4B_DQ2
DDR4B_DQ16	R5	LVDS3E_8P/DQ45/DQ22/32	LVDS3E_20P/DQ47/DQ23/8	V8	DDR4B_DQ6
DDR4B_DQ18	T5	LVDS3E_8N/DQ45/DQ22/33	LVDS3E_20N/DQ47/DQ23/9	V9	DDR4B_DBI_L0
DDR4B_DQ23	T7	LVDS3E_9P/DQ45/DQ22/30	LVDS3E_21P/DQ47/DQ23/6	T8	DDR4B_DQ3
DDR4B_DQ19	U7	LVDS3E_9N/DQ45/DQ22/31	LVDS3E_21N/DQ47/DQ23/7	T9	DDR4B_DQ1
			LVDS3E_22P/DQS47/CQ47/DQ23/4	W9	DDR4B_DQS_P0
			LVDS3E_22N/DQSN47/CQN47/DQ23/5	W10	DDR4B_DQS_N0
DDR4B_DQ17	V6			U11	
	V7	RZQ_3E/LVDS3E_11P/DQ45/DQ22/26	LVDS3E_23P/DQ47/DQ23/2	V11	DDR4B_DQ4
		LVDS3E_11N/DQ45/DQ22/27	LVDS3E_23N/DQ47/DQ23/3	R6	DDR4B_DQ5
			LVDS3E_24P/DQ47/DQ23/0	R7	DDR4B_DQ7
			LVDS3E_24N/DQ47/DQ23/1		

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U14-25 ARRIA 10 BANK 3G

VCCIO = 1.2V

DDR4B_DQ36	E8	LVDS3G_1P/DQ36/DQ18/46			
DDR4B_DQ35	F8	LVDS3G_1N/DQ36/DQ18/47			
	B7	LVDS3G_2P/DQ36/DQ18/44	LVDS3G_14P/DQ38/DQ19/20	F9	DDR4B_DQ48
DDR4B_DQ32	C7	LVDS3G_2N/DQ36/DQ18/45	LVDS3G_14N/DQ38/DQ19/21	G9	DDR4B_DQ49
DDR4B_DQ34	C8	LVDS3G_3P/DQ36/DQ18/42			
DDR4B_DQ39	D8	LVDS3G_3N/DQ36/DQ18/43			
DDR4B_DQS_P4	B6	LVDS3G_4P/DQS36/CQ36/DQ18/40	LVDS3G_16P/DQS38/CQ38/DQ19/16	G5	DDR4B_DQS_P6
DDR4B_DQS_N4	C6	LVDS3G_4N/DQSN36/CQN36/DQ18/41	LVDS3G_16N/DQSN38/CQN38/DQ19/17	G6	DDR4B_DQS_N6
DDR4B_DQ37	A5	LVDS3G_5P/DQ36/DQ18/38	LVDS3G_17P/DQ38/DQ19/14	G7	DDR4B_DQ55
DDR4B_DQ38	B5	LVDS3G_5N/DQ36/DQ18/39	LVDS3G_17N/DQ38/DQ19/15	H7	DDR4B_DQ54
DDR4B_DQ33	A4	LVDS3G_6P/DQ36/DQS18/CQ18/36	LVDS3G_18P/DQ38/DQS19/CQ19/12	H6	DDR4B_DQ51
DDR4B_DBI_L4	B4	LVDS3G_6N/DQ36/DQSN18/CQN18/37	LVDS3G_18N/DQ38/DQSN19/CQN19/13	J6	DDR4B_DQ53
DDR4B_DQ43	C3	LVDS3G_7P/DQ37/DQ18/34	LVDS3G_19P/DQ39/DQ19/10	K10	DDR4B_DQ58
DDR4B_DQ44	C4	LVDS3G_7N/DQ37/DQ18/35	LVDS3G_19N/DQ39/DQ19/11	L10	DDR4B_DQ56
DDR4B_DQ40	C2	LVDS3G_8P/DQ37/DQ18/32	LVDS3G_20P/DQ39/DQ19/8	J11	DDR4B_DQ61
DDR4B_DQ42	D3	LVDS3G_8N/DQ37/DQ18/33	LVDS3G_20N/DQ39/DQ19/9	K11	DDR4B_DBI_L7
DDR4B_DQ46	E7	LVDS3G_9P/DQ37/DQ18/30	LVDS3G_21P/DQ39/DQ19/6	M12	DDR4B_DQ57
	F7	LVDS3G_9N/DQ37/DQ18/31	LVDS3G_21N/DQ39/DQ19/7	N13	DDR4B_DQ59
			LVDS3G_22P/DQS39/CQ39/DQ19/4	M10	DDR4B_DQS_P7
			LVDS3G_22N/DQSN39/CQN39/DQ19/5	N11	DDR4B_DQS_N7
DDR4B_DQ41	D6			J9	DDR4B_DQ60
DDR4B_DQ47	E6	RZQ_3G/LVDS3G_11P/DQ37/DQ18/26	LVDS3G_23P/DQ39/DQ19/2	J10	
		LVDS3G_11N/DQ37/DQ18/27	LVDS3G_23N/DQ39/DQ19/3	M11	DDR4B_DQ62
			LVDS3G_24P/DQ39/DQ19/0	N12	DDR4B_DQ63
			LVDS3G_24N/DQ39/DQ19/1		

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U14-26 ARRIA 10 BANK 3F

VCCIO = 1.2V

	F4	LVDS3F_1P/DQ40/DQ20/46			
	G4	LVDS3F_1N/DQ40/DQ20/47			
	C1	LVDS3F_2P/DQ40/DQ20/44	LVDS3F_14P/DQ42/DQ21/20	K5	DDR4B_A8
	D1	LVDS3F_2N/DQ40/DQ20/45	LVDS3F_14N/DQ42/DQ21/21	K6	DDR4B_A9
	E1	LVDS3F_3P/DQ40/DQ20/42			
	E2	LVDS3F_3N/DQ40/DQ20/43			
	E3	LVDS3F_4P/DQS40/CQ40/DQ20/40	LVDS3F_16P/DQS42/CQ42/DQ21/16	M6	DDR4B_A4
	F3	LVDS3F_4N/DQSN40/CQN40/DQ20/41	LVDS3F_16N/DQSN42/CQN42/DQ21/17	M7	DDR4B_A5
	F2	LVDS3F_5P/DQ40/DQ20/38	LVDS3F_17P/DQ42/DQ21/14	L4	DDR4B_A2
	G2	LVDS3F_5N/DQ40/DQ20/39	LVDS3F_17N/DQ42/DQ21/15	M4	DDR4B_A3
	G1	LVDS3F_6P/DQ40/DQS20/CQ20/36	LVDS3F_18P/DQ42/DQS21/CQ21/12	L5	DDR4B_A0
	H2	LVDS3F_6N/DQ40/DQSN20/CQN20/37	LVDS3F_18N/DQ42/DQSN21/CQN21/13	M5	DDR4B_A1
DDR4B_BA1	J4	LVDS3F_7P/DQ41/DQ20/34	LVDS3F_19P/DQ43/DQ21/10	N9	
DDR4B_BG	J5	LVDS3F_7N/DQ41/DQ20/35	LVDS3F_19N/DQ43/DQ21/11	P10	DDR4B_PAR
	H1	LVDS3F_8P/DQ41/DQ20/32	LVDS3F_20P/DQ43/DQ21/8	N8	DDR4B_CK_P
DDR4B_BA0	J1	LVDS3F_8N/DQ41/DQ20/33	LVDS3F_20N/DQ43/DQ21/9	M9	DDR4B_CK_N
DDR4B_A15	H3	LVDS3F_9P/DQ41/DQ20/30	LVDS3F_21P/DQ43/DQ21/6	P9	DDR4B_CKE
DDR4B_A16	H4	LVDS3F_9N/DQ41/DQ20/31	LVDS3F_21N/DQ43/DQ21/7	R10	
			LVDS3F_22P/DQS43/CQ43/DQ21/4	P8	DDR4B_ODT
			LVDS3F_22N/DQSN43/CQN43/DQ21/5	R8	
RZQ_3F	L2			P11	DDR4B_CS_L
DDR4B_A12	L3	RZQ_3F/LVDS3F_11P/DQ41/DQ20/26	LVDS3F_23P/DQ43/DQ21/2	R11	DDR4B_ACT_L
		LVDS3F_11N/DQ41/DQ20/27	LVDS3F_23N/DQ43/DQ21/3	L8	DDR4B_ALERT_L
			LVDS3F_24P/DQ43/DQ21/0	L9	DDR4B_RESET_L
			LVDS3F_24N/DQ43/DQ21/1		

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U14-24 ARRIA 10 BANK 3H

VCCIO = 1.8V

	P14	LVDS3H_1P/DQ32/DQ16/46			
	P15	LVDS3H_1N/DQ32/DQ16/47			
	M14	LVDS3H_2P/DQ32/DQ16/44	LVDS3H_14P/DQ34/DQ17/20	D11	
	N14	LVDS3H_2N/DQ32/DQ16/45	LVDS3H_14N/DQ34/DQ17/21	E11	
	J13	LVDS3H_3P/DQ32/DQ16/42			
	J14	LVDS3H_3N/DQ32/DQ16/43			
	L14	LVDS3H_4P/DQS32/CQ32/DQ16/40	LVDS3H_16P/DQS34/CQ34/DQ17/16	F10	
	L15	LVDS3H_4N/DQSN32/CQN32/DQ16/41	LVDS3H_16N/DQSN34/CQN34/DQ17/17	G10	
	L12	LVDS3H_5P/DQ32/DQ16/38	LVDS3H_17P/DQ34/DQ17/14	D10	
	L13	LVDS3H_5N/DQ32/DQ16/39	LVDS3H_17N/DQ34/DQ17/15	E10	
	K12	LVDS3H_6P/DQ32/DQS16/CQ16/36	LVDS3H_18P/DQ34/DQS17/CQ17/12	G11	
	K13	LVDS3H_6N/DQ32/DQSN16/CQN16/37	LVDS3H_18N/DQ34/DQSN17/CQN17/13	H11	
	G14	LVDS3H_7P/DQ33/DQ16/34	LVDS3H_19P/DQ35/DQ17/10	A10	
	H14	LVDS3H_7N/DQ33/DQ16/35	LVDS3H_19N/DQ35/DQ17/11	B10	
	C14	LVDS3H_8P/DQ33/DQ16/32	LVDS3H_20P/DQ35/DQ17/8	A9	
	D14	LVDS3H_8N/DQ33/DQ16/33	LVDS3H_20N/DQ35/DQ17/9	B9	
	C13	LVDS3H_9P/DQ33/DQ16/30	LVDS3H_21P/DQ35/DQ17/6	B11	
	D13	LVDS3H_9N/DQ33/DQ16/31	LVDS3H_21N/DQ35/DQ17/7	B12	
			LVDS3H_22P/DQS35/CQ35/DQ17/4	A12	
			LVDS3H_22N/DQSN35/CQN35/DQ17/5	A13	
	H12			A7	
	H13	RZQ_3H/LVDS3H_11P/DQ33/DQ16/26	LVDS3H_23P/DQ35/DQ17/2	A8	
		LVDS3H_11N/DQ33/DQ16/27	LVDS3H_23N/DQ35/DQ17/3	C9	
			LVDS3H_24P/DQ35/DQ17/0	D9	
			LVDS3H_24N/DQ35/DQ17/1		

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Title: FLIK

Size	Document Number	Rev
B	FPGA Bank 3E, 3F, 3G, 3H	B1

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PCIe Transceiver

PCIE_TX_p[3..0]
PCIE_TX_n[3..0]
PCIE_RX_p[3..0] 37
PCIE_RX_n[3..0] 37
PCIE_REFCLK_p 5
PCIE_REFCLK_n 5

Reserved Reference Clock

RSV_REFCLK_P 5
RSV_REFCLK_N 5

U14-19 ARRIA 10 Transceiver BANK 1C

	AU33	GXBL1C_RX_CH0P,GXBL1C_REFCLK0P	GXBL1C_TX_CH0P	AW33	
	AU32	GXBL1C_RX_CH0N,GXBL1C_REFCLK0N	GXBL1C_TX_CH0N	AW32	
	AT31	GXBL1C_RX_CH1P,GXBL1C_REFCLK1P	GXBL1C_TX_CH1P	AW37	
	AT30	GXBL1C_RX_CH1N,GXBL1C_REFCLK1N	GXBL1C_TX_CH1N	AW36	
	AR33	GXBL1C_RX_CH2P,GXBL1C_REFCLK2P	GXBL1C_TX_CH2P	AV35	
	AR32	GXBL1C_RX_CH2N,GXBL1C_REFCLK2N	GXBL1C_TX_CH2N	AV34	
	AP31	GXBL1C_RX_CH3P,GXBL1C_REFCLK3P	GXBL1C_TX_CH3P	AV39	
	AP30	GXBL1C_RX_CH3N,GXBL1C_REFCLK3N	GXBL1C_TX_CH3N	AV38	
PCIE_RX_p0	AN33	GXBL1C_RX_CH4P,GXBL1C_REFCLK4P	GXBL1C_TX_CH4P	AU37	C256 0.22u, C255 0.22u — PCIE_TX_p0
PCIE_RX_n0	AN32	GXBL1C_RX_CH4N,GXBL1C_REFCLK4N	GXBL1C_TX_CH4N	AU36	PCIE_TX_n0
PCIE_RX_p1	AM31	GXBL1C_RX_CH5P,GXBL1C_REFCLK5P	GXBL1C_TX_CH5P	AT35	C280 0.22u, C302 0.22u — PCIE_TX_p1
PCIE_RX_n1	AM30	GXBL1C_RX_CH5N,GXBL1C_REFCLK5N	GXBL1C_TX_CH5N	AT34	PCIE_TX_n1
PCIE_REFCLK_p	AN29	REFCLK_GXBL1C_CHTP			
PCIE_REFCLK_n	AN28	REFCLK_GXBL1C_CHTN			
R237 10K	AR29	REFCLK_GXBL1C_CHBP			
	AR28	REFCLK_GXBL1C_CHBN			

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U14-17 ARRIA 10 Transceiver BANK 1E

AH35	GXBL1E_RX_CH0P,GXBL1E_REFCLK0P	GXBL1E_TX_CH0P	AL37
AH34	GXBL1E_RX_CH0N,GXBL1E_REFCLK0N	GXBL1E_TX_CH0N	AL36
AG33	GXBL1E_RX_CH1P,GXBL1E_REFCLK1P	GXBL1E_TX_CH1P	AK39
AG32	GXBL1E_RX_CH1N,GXBL1E_REFCLK1N	GXBL1E_TX_CH1N	AK38
AF31	GXBL1E_RX_CH2P,GXBL1E_REFCLK2P	GXBL1E_TX_CH2P	AJ37
AF30	GXBL1E_RX_CH2N,GXBL1E_REFCLK2N	GXBL1E_TX_CH2N	AJ36
AF35	GXBL1E_RX_CH3P,GXBL1E_REFCLK3P	GXBL1E_TX_CH3P	AH39
AF34	GXBL1E_RX_CH3N,GXBL1E_REFCLK3N	GXBL1E_TX_CH3N	AH38
AE32	GXBL1E_RX_CH4N,GXBL1E_REFCLK4N	GXBL1E_TX_CH4P	AG37
AE33	GXBL1E_RX_CH4P,GXBL1E_REFCLK4P	GXBL1E_TX_CH4N	AG36
AD30	GXBL1E_RX_CH5N,GXBL1E_REFCLK5N	GXBL1E_TX_CH5P	AF39
AD31	GXBL1E_RX_CH5P,GXBL1E_REFCLK5P	GXBL1E_TX_CH5N	AF38
R256 10K — AE29	REFCLK_GXBL1E_CHTP		
AE28	REFCLK_GXBL1E_CHTN		
RSV_REFCLK_P AG29	REFCLK_GXBL1E_CHBP		
RSV_REFCLK_N AG28	REFCLK_GXBL1E_CHBN		

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U14-18 ARRIA 10 Transceiver BANK 1D

PCIE_RX_p2	AM35	GXBL1D_RX_CH0P,GXBL1D_REFCLK0P	GXBL1D_TX_CH0P	AT39	C270 0.22u, C269 0.22u — PCIE_TX_p2
PCIE_RX_n2	AM34	GXBL1D_RX_CH0N,GXBL1D_REFCLK0N	GXBL1D_TX_CH0N	AT38	PCIE_TX_n2
PCIE_RX_p3	AL33	GXBL1D_RX_CH1P,GXBL1D_REFCLK1P	GXBL1D_TX_CH1P	AR37	C272 0.22u, C271 0.22u — PCIE_TX_p3
PCIE_RX_n3	AL32	GXBL1D_RX_CH1N,GXBL1D_REFCLK1N	GXBL1D_TX_CH1N	AR36	PCIE_TX_n3
	AK31	GXBL1D_RX_CH2P,GXBL1D_REFCLK2P	GXBL1D_TX_CH2P	AP35	
	AK30	GXBL1D_RX_CH2N,GXBL1D_REFCLK2N	GXBL1D_TX_CH2N	AP34	
	AK35	GXBL1D_RX_CH3P,GXBL1D_REFCLK3P	GXBL1D_TX_CH3P	AP39	
	AK34	GXBL1D_RX_CH3N,GXBL1D_REFCLK3N	GXBL1D_TX_CH3N	AP38	
	AJ33	GXBL1D_RX_CH4P,GXBL1D_REFCLK4P	GXBL1D_TX_CH4P	AN37	
	AJ32	GXBL1D_RX_CH4N,GXBL1D_REFCLK4N	GXBL1D_TX_CH4N	AN36	
	AH31	GXBL1D_RX_CH5P,GXBL1D_REFCLK5P	GXBL1D_TX_CH5P	AM39	
	AH30	GXBL1D_RX_CH5N,GXBL1D_REFCLK5N	GXBL1D_TX_CH5N	AM38	
R252 10K	AJ29	REFCLK_GXBL1D_CHTP			
	AJ28	REFCLK_GXBL1D_CHTN			
R248 10K	AL29	REFCLK_GXBL1D_CHBP			
	AL28	REFCLK_GXBL1D_CHBN			

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U14-16 ARRIA 10 Transceiver BANK 1F

AD35	GXBL1F_RX_CH0P,GXBL1F_REFCLK0P	GXBL1F_TX_CH0P	AE37
AD34	GXBL1F_RX_CH0N,GXBL1F_REFCLK0N	GXBL1F_TX_CH0N	AE36
AC33	GXBL1F_RX_CH1P,GXBL1F_REFCLK1P	GXBL1F_TX_CH1P	AD39
AC32	GXBL1F_RX_CH1N,GXBL1F_REFCLK1N	GXBL1F_TX_CH1N	AD38
AB31	GXBL1F_RX_CH2P,GXBL1F_REFCLK2P	GXBL1F_TX_CH2P	AC37
AB30	GXBL1F_RX_CH2N,GXBL1F_REFCLK2N	GXBL1F_TX_CH2N	AC36
AB35	GXBL1F_RX_CH3P,GXBL1F_REFCLK3P	GXBL1F_TX_CH3P	AB39
AB34	GXBL1F_RX_CH3N,GXBL1F_REFCLK3N	GXBL1F_TX_CH3N	AB38
AA33	GXBL1F_RX_CH4P,GXBL1F_REFCLK4P	GXBL1F_TX_CH4P	AA37
AA32	GXBL1F_RX_CH4N,GXBL1F_REFCLK4N	GXBL1F_TX_CH4N	AA36
Y35	GXBL1F_RX_CH5P,GXBL1F_REFCLK5P	GXBL1F_TX_CH5P	Y39
Y34	GXBL1F_RX_CH5N,GXBL1F_REFCLK5N	GXBL1F_TX_CH5N	Y38
R265 10K — AA29	REFCLK_GXBL1F_CHTP		
AA28	REFCLK_GXBL1F_CHTN		
R262 10K — AC29	REFCLK_GXBL1F_CHBP		
AC28	REFCLK_GXBL1F_CHBN		

10AX115N3F40E2SG

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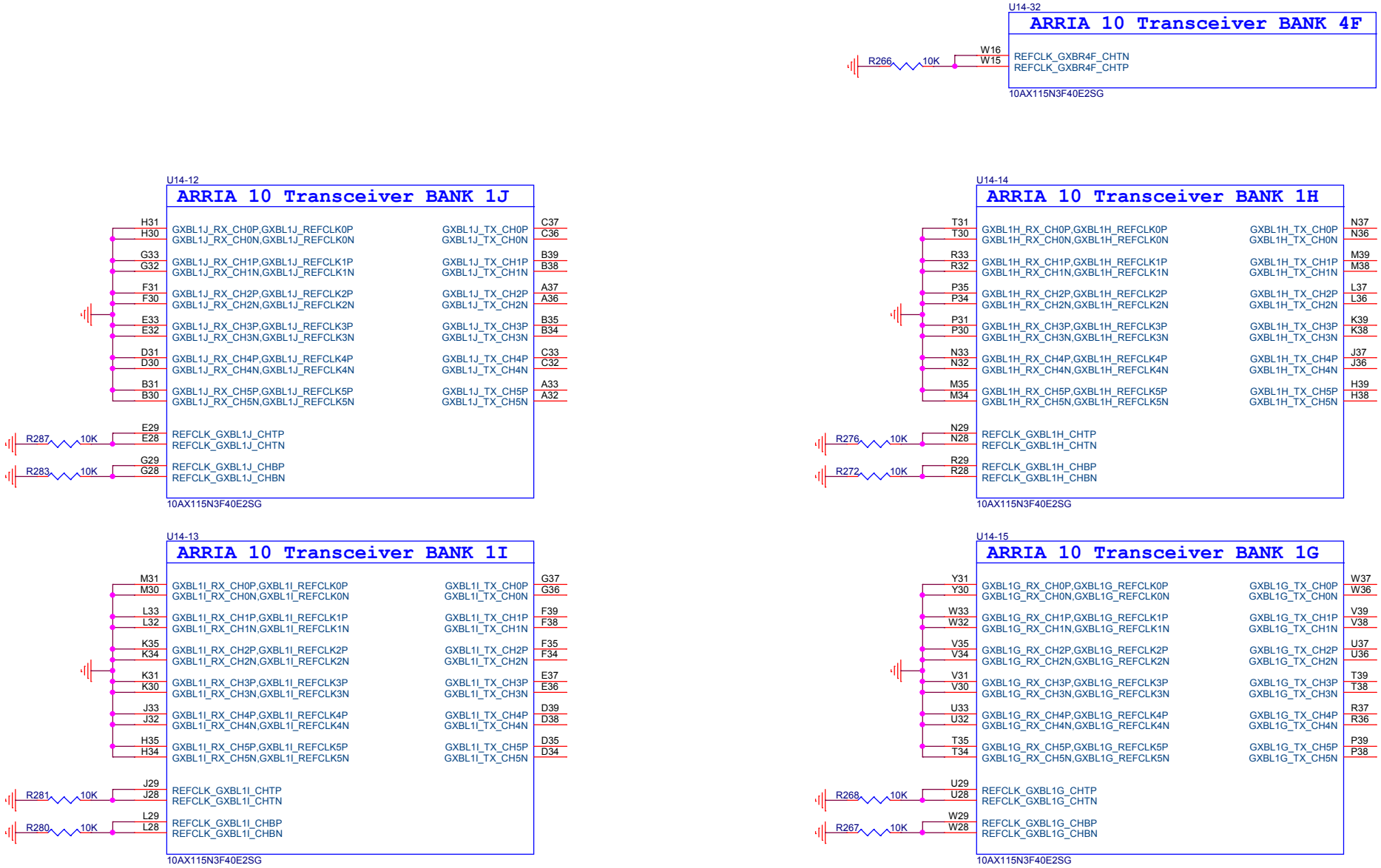
Title: FLIK

Size	Document Number	Rev
B	FPGA GXB 1C, 1D, 1E, 1F	B1

Date: Monday, November 04, 2019 Sheet 13 of 38



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Title
FLIK

Size	Document Number	Rev
B	FPGA GXB 1G, 1H, 1I, 1J, 4F	B1

Date: Monday, November 04, 2019 Sheet 14 of 38

Clock Input

SYS_REFCLK1_P 6
SYS_REFCLK1_N 6

USER LEDS

LED[4..1] 10,31

Debug Interface

DEBUG[16..1] 10,31

U14-2

ARRIA 10 Clock Bank 2

R243 100 DNI

SYS_REFCLK1_P
SYS_REFCLK1_N

IO Standard:
LVDS with on-chip termination

Bank 2A — VCCIO = 1.8V

AT18	CLK_2A_0P/DATA23/LVDS2A_13P/DQ30/DQ15/22	PLL_2A_CLKOUT0P,PLL_2A_CLKOUT0,PLL_2A_FB0/DATA27/LVDS2A_15P/DQ30/DQ15/18	AU19
AR18	CLK_2A_0N/DATA22/LVDS2A_13N/DQ30/DQ15/23	PLL_2A_CLKOUT0N/DATA26/LVDS2A_15N/DQ30/DQ15/19	AT19
AP18	CLK_2A_1P/DATA21/LVDS2A_12P/DQ29/DQ14/24	PLL_2A_CLKOUT1P,PLL_2A_CLKOUT1,PLL_2A_FB1/DATA19/LVDS2A_10P/DQS29/CQ29/DQ14/28	AR16
AN18	CLK_2A_1N/DATA20/LVDS2A_12N/DQ29/DQ14/25	PLL_2A_CLKOUT1N/DATA18/LVDS2A_10N/DQSN29/CQN29/DQ14/29	AP16

Bank 2I — VCCIO = 1.8V

AJ21	CLK_2I_0P/LVDS2I_13P/DQ14/DQ7/22	PLL_2I_CLKOUT0P,PLL_2I_CLKOUT0,PLL_2I_FB0/LVDS2I_15P/DQ14/DQ7/18	AK20
AH21	CLK_2I_0N/LVDS2I_13N/DQ14/DQ7/23	PLL_2I_CLKOUT0N/LVDS2I_15N/DQ14/DQ7/19	AJ20
AM21	CLK_2I_1P/LVDS2I_12P/DQ13/DQ6/24	PLL_2I_CLKOUT1P,PLL_2I_CLKOUT1,PLL_2I_FB1/LVDS2I_10P/DQS13/CQ13/DQ6/28	AR21
AL20	CLK_2I_1N/LVDS2I_12N/DQ13/DQ6/25	PLL_2I_CLKOUT1N/LVDS2I_10N/DQSN13/CQN13/DQ6/29	AP21

Bank 2J — VCCIO = 1.8V

AP26	CLK_2J_0P/LVDS2J_13P/DQ10/DQ5/22	PLL_2J_CLKOUT0P,PLL_2J_CLKOUT0,PLL_2J_FB0/LVDS2J_15P/DQ10/DQ5/18	AL26
AN26	CLK_2J_0N/LVDS2J_13N/DQ10/DQ5/23	PLL_2J_CLKOUT0N/LVDS2J_15N/DQ10/DQ5/19	AK26
AP24	CLK_2J_1P/LVDS2J_12P/DQ9/DQ4/24	PLL_2J_CLKOUT1P,PLL_2J_CLKOUT1,PLL_2J_FB1/LVDS2J_10P/DQS9/CQ9/DQ4/28	AT25
AP23	CLK_2J_1N/LVDS2J_12N/DQ9/DQ4/25	PLL_2J_CLKOUT1N/LVDS2J_10N/DQSN9/CQN9/DQ4/29	AT24

Bank 2K — VCCIO = 1.8V

DEBUG13 C24	CLK_2K_0P/LVDS2K_13P/DQ6/DQ3/22	PLL_2K_CLKOUT0P,PLL_2K_CLKOUT0,PLL_2K_FB0/LVDS2K_15P/DQ6/DQ3/18	B22	DEBUG7
LED2 D24	CLK_2K_0N/LVDS2K_13N/DQ6/DQ3/23	PLL_2K_CLKOUT0N/LVDS2K_15N/DQ6/DQ3/19	C23	DEBUG12
F25	CLK_2K_1P/LVDS2K_12P/DQ5/DQ2/24	PLL_2K_CLKOUT1P,PLL_2K_CLKOUT1,PLL_2K_FB1/LVDS2K_10P/DQS5/CQ5/DQ2/28	G26	
G24	CLK_2K_1N/LVDS2K_12N/DQ5/DQ2/25	PLL_2K_CLKOUT1N/LVDS2K_10N/DQSN5/CQN5/DQ2/29	G25	

Bank 2L — VCCIO = 1.8V

F22	CLK_2L_0P/LVDS2L_13P/DQ2/DQ1/22	PLL_2L_CLKOUT0P,PLL_2L_CLKOUT0,PLL_2L_FB0/LVDS2L_15P/DQ2/DQ1/18	G20
G22	CLK_2L_0N/LVDS2L_13N/DQ2/DQ1/23	PLL_2L_CLKOUT0N/LVDS2L_15N/DQ2/DQ1/19	G21
K18	CLK_2L_1P/LVDS2L_12P/DQ1/DQ0/24	PLL_2L_CLKOUT1P,PLL_2L_CLKOUT1,PLL_2L_FB1/LVDS2L_10P/DQS1/CQ1/DQ0/28	J21
L19	CLK_2L_1N/LVDS2L_12N/DQ1/DQ0/25	PLL_2L_CLKOUT1N/LVDS2L_10N/DQSN1/CQN1/DQ0/29	J20

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Title: **FLIK**

Size	Document Number	Rev
B	FPGA Clock Bank 2	B1

Date: Monday, November 04, 2019 Sheet 15 of 38

DDR4 SDRAM - A

DDR4A_CK_P 11,21
DDR4A_CK_N 11,21
DDR4A_BA[1..0] 11,21
DDR4A_BG 11,21

DDR4A_ODT 11,21
DDR4A_CS_L 11,21
DDR4A_DQ[63..0] 11,21
DDR4A_DQS_P[7..0] 11,21
DDR4A_DQS_N[7..0] 11,21
DDR4A_A[16..0] 11,21
DDR4A_DBI_L[7..0] 11,21
DDR4A_CKE 11,21

DDR4A_RESET_L 11,21
DDR4A_PAR 11,21
DDR4A_ACT_L 11,21

DDR4A_ALERT_L 11,21

RAS_n is a multiplexed function with A16
CAS_n is a multiplexed function with A15
WE_n is a multiplexed function with A14

DDR4 SDRAM - B

DDR4B_CK_P 12,22
DDR4B_CK_N 12,22
DDR4B_BA[1..0] 12,22
DDR4B_BG 12,22

DDR4B_ODT 12,22
DDR4B_CS_L 12,22
DDR4B_DQ[63..0] 12,22
DDR4B_DQS_P[7..0] 12,22
DDR4B_DQS_N[7..0] 12,22
DDR4B_A[16..0] 12,22
DDR4B_DBI_L[7..0] 12,22
DDR4B_CKE 12,22

DDR4B_RESET_L 12,22
DDR4B_PAR 12,22
DDR4B_ACT_L 12,22

DDR4B_ALERT_L 12,22

Clock Input

DDR4A_REFCLK_P 5
DDR4A_REFCLK_N 5

DDR4B_REFCLK_P 5
DDR4B_REFCLK_N 5

Clock Input

SYS_REFCLK2_P 6
SYS_REFCLK2_N 6

U14-3

ARRIA 10 Clock Bank 3

Bank 3A — VCCIO = 1.8V

AM10	CLK_3A_0P/LVDS3A_13P/DQ62/DQ31/22	PLL_3A_CLKOUT0P,PLL_3A_CLKOUT0,PLL_3A_FB0/LVDS3A_15P/DQ62/DQ31/18	AM12
AL10	CLK_3A_0N/LVDS3A_13N/DQ62/DQ31/23	PLL_3A_CLKOUT0N/LVDS3A_15N/DQ62/DQ31/19	AL12
AR11	CLK_3A_1P/LVDS3A_12P/DQ61/DQ30/24	PLL_3A_CLKOUT1P,PLL_3A_CLKOUT1,PLL_3A_FB1/LVDS3A_10P/DQS61/CQ61/DQ30/28	AR10
AP11	CLK_3A_1N/LVDS3A_12N/DQ61/DQ30/25	PLL_3A_CLKOUT1N/LVDS3A_10N/DQSN61/CQN61/DQ30/29	AP10

Bank 3B — VCCIO = 1.2V

DDR4A_DQ13 AN4	CLK_3B_0P/LVDS3B_13P/DQ58/DQ29/22	PLL_3B_CLKOUT0P,PLL_3B_CLKOUT0,PLL_3B_FB0/LVDS3B_15P/DQ58/DQ29/18	AP4	DDR4A_DQ12
DDR4A_DBI_L1 AM5	CLK_3B_0N/LVDS3B_13N/DQ58/DQ29/23	PLL_3B_CLKOUT0N/LVDS3B_15N/DQ58/DQ29/19	AP5	
DDR4A_DQ23 AL9	CLK_3B_1P/LVDS3B_12P/DQ57/DQ28/24	PLL_3B_CLKOUT1P,PLL_3B_CLKOUT1,PLL_3B_FB1/LVDS3B_10P/DQS57/CQ57/DQ28/28	AN7	DDR4A_DQS_P2
DDR4A_DBI_L2 AK10	CLK_3B_1N/LVDS3B_12N/DQ57/DQ28/25	PLL_3B_CLKOUT1N/LVDS3B_10N/DQSN57/CQN57/DQ28/29	AM7	DDR4A_DQS_N2

Bank 3C — VCCIO = 1.2V

DDR4A_A10 AJ5	CLK_3C_0P/LVDS3C_13P/DQ54/DQ27/22	PLL_3C_CLKOUT0P,PLL_3C_CLKOUT0,PLL_3C_FB0/LVDS3C_15P/DQ54/DQ27/18	AK6	DDR4A_A6
DDR4A_A11 AH6	CLK_3C_0N/LVDS3C_13N/DQ54/DQ27/23	PLL_3C_CLKOUT0N/LVDS3C_15N/DQ54/DQ27/19	AJ6	DDR4A_A7
DDR4A_REFCLK_P AG5	CLK_3C_1P/LVDS3C_12P/DQ53/DQ26/24	PLL_3C_CLKOUT1P,PLL_3C_CLKOUT1,PLL_3C_FB1/LVDS3C_10P/DQS53/CQ53/DQ26/28	AJ3	DDR4A_A13
DDR4A_REFCLK_N AG6	CLK_3C_1N/LVDS3C_12N/DQ53/DQ26/25	PLL_3C_CLKOUT1N/LVDS3C_10N/DQSN53/CQN53/DQ26/29	AH3	DDR4A_A14

R250 100 DNI

IO Standard: LVDS with on-chip termination

Bank 3D — VCCIO = 1.2V

DDR4A_DQ51 Y2	CLK_3D_0P/LVDS3D_13P/DQ50/DQ25/22	PLL_3D_CLKOUT0P,PLL_3D_CLKOUT0,PLL_3D_FB0/LVDS3D_15P/DQ50/DQ25/18	AB4	DDR4A_DQ50
DDR4A_DBI_L6 Y3	CLK_3D_0N/LVDS3D_13N/DQ50/DQ25/23	PLL_3D_CLKOUT0N/LVDS3D_15N/DQ50/DQ25/19	AA4	
DDR4A_DQ46 AB5	CLK_3D_1P/LVDS3D_12P/DQ49/DQ24/24	PLL_3D_CLKOUT1P,PLL_3D_CLKOUT1,PLL_3D_FB1/LVDS3D_10P/DQS49/CQ49/DQ24/28	AE5	DDR4A_DQS_P5
DDR4A_DBI_L5 AB6	CLK_3D_1N/LVDS3D_12N/DQ49/DQ24/25	PLL_3D_CLKOUT1N/LVDS3D_10N/DQSN49/CQN49/DQ24/29	AE6	DDR4A_DQS_N5

Bank 3E — VCCIO = 1.2V

DDR4B_DQ9 T4	CLK_3E_0P/LVDS3E_13P/DQ46/DQ23/22	PLL_3E_CLKOUT0P,PLL_3E_CLKOUT0,PLL_3E_FB0/LVDS3E_15P/DQ46/DQ23/18	U1	DDR4B_DQ12
DDR4B_DBI_L1 U4	CLK_3E_0N/LVDS3E_13N/DQ46/DQ23/23	PLL_3E_CLKOUT0N/LVDS3E_15N/DQ46/DQ23/19	U2	DDR4B_DQ10
DDR4B_DQ21 W5	CLK_3E_1P/LVDS3E_12P/DQ45/DQ22/24	PLL_3E_CLKOUT1P,PLL_3E_CLKOUT1,PLL_3E_FB1/LVDS3E_10P/DQS45/CQ45/DQ22/28	U5	DDR4B_DQS_P2
DDR4B_DBI_L2 W6	CLK_3E_1N/LVDS3E_12N/DQ45/DQ22/25	PLL_3E_CLKOUT1N/LVDS3E_10N/DQSN45/CQN45/DQ22/29	U6	DDR4B_DQS_N2

Bank 3F — VCCIO = 1.2V

DDR4B_A10 N6	CLK_3F_0P/LVDS3F_13P/DQ42/DQ21/22	PLL_3F_CLKOUT0P,PLL_3F_CLKOUT0,PLL_3F_FB0/LVDS3F_15P/DQ42/DQ21/18	K7	DDR4B_A6
DDR4B_A11 N7	CLK_3F_0N/LVDS3F_13N/DQ42/DQ21/23	PLL_3F_CLKOUT0N/LVDS3F_15N/DQ42/DQ21/19	L7	DDR4B_A7
DDR4B_REFCLK_P J3	CLK_3F_1P/LVDS3F_12P/DQ41/DQ20/24	PLL_3F_CLKOUT1P,PLL_3F_CLKOUT1,PLL_3F_FB1/LVDS3F_10P/DQS41/CQ41/DQ20/28	K1	DDR4B_A13
DDR4B_REFCLK_N K3	CLK_3F_1N/LVDS3F_12N/DQ41/DQ20/25	PLL_3F_CLKOUT1N/LVDS3F_10N/DQSN41/CQN41/DQ20/29	K2	DDR4B_A14

R279 100 DNI

IO Standard: LVDS with on-chip termination

Bank 3G — VCCIO = 1.2V

DDR4B_DQ50 H8	CLK_3G_0P/LVDS3G_13P/DQ38/DQ19/22	PLL_3G_CLKOUT0P,PLL_3G_CLKOUT0,PLL_3G_FB0/LVDS3G_15P/DQ38/DQ19/18	J8	DDR4B_DQ52
DDR4B_DBI_L6 H9	CLK_3G_0N/LVDS3G_13N/DQ38/DQ19/23	PLL_3G_CLKOUT0N/LVDS3G_15N/DQ38/DQ19/19	K8	
DDR4B_DQ45 E5	CLK_3G_1P/LVDS3G_12P/DQ37/DQ18/24	PLL_3G_CLKOUT1P,PLL_3G_CLKOUT1,PLL_3G_FB1/LVDS3G_10P/DQS37/CQ37/DQ18/28	D4	DDR4B_DQS_P5
DDR4B_DBI_L5 F5	CLK_3G_1N/LVDS3G_12N/DQ37/DQ18/25	PLL_3G_CLKOUT1N/LVDS3G_10N/DQSN37/CQN37/DQ18/29	D5	DDR4B_DQS_N5

Bank 3H — VCCIO = 1.8V

CLK_3H_0P/LVDS3H_13P/DQ34/DQ17/22	PLL_3H_CLKOUT0P,PLL_3H_CLKOUT0,PLL_3H_FB0/LVDS3H_15P/DQ34/DQ17/18	F12
CLK_3H_0N/LVDS3H_13N/DQ34/DQ17/23	PLL_3H_CLKOUT0N/LVDS3H_15N/DQ34/DQ17/19	G12
CLK_3H_1P/LVDS3H_12P/DQ33/DQ16/24	PLL_3H_CLKOUT1P,PLL_3H_CLKOUT1,PLL_3H_FB1/LVDS3H_10P/DQS33/CQ33/DQ16/28	E12
CLK_3H_1N/LVDS3H_12N/DQ33/DQ16/25	PLL_3H_CLKOUT1N/LVDS3H_10N/DQSN33/CQN33/DQ16/29	E13

R290 100 DNI

SYS_REFCLK2_P C11
SYS_REFCLK2_N C12
F13
F14

IO Standard: LVDS with on-chip termination

10AX115N3F40E2SG

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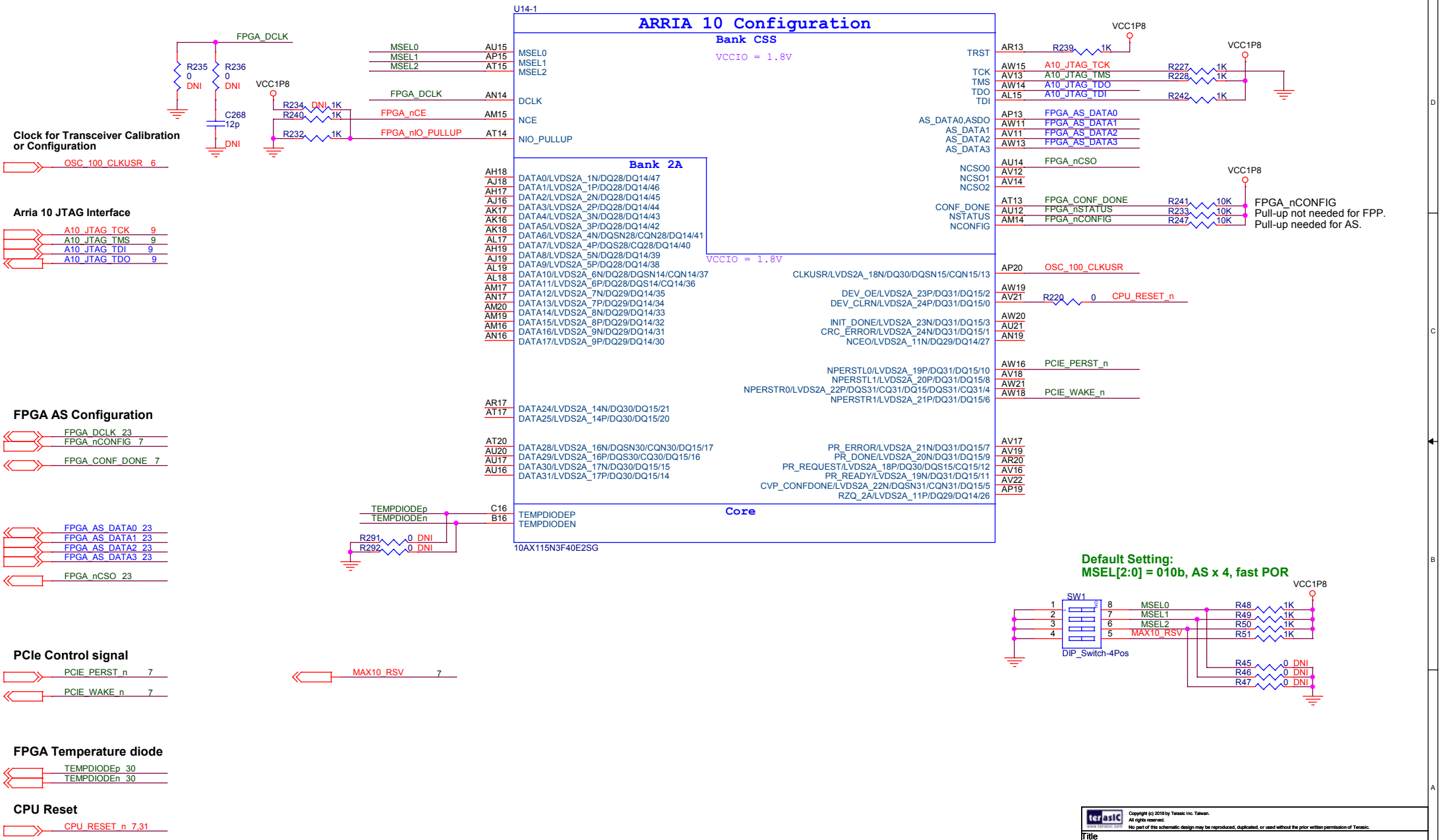
Title: **FLIK**

Size	Document Number	Rev
B	FPGA Clock Bank 3	B1

Date: Monday, November 04, 2019 Sheet 16 of 38



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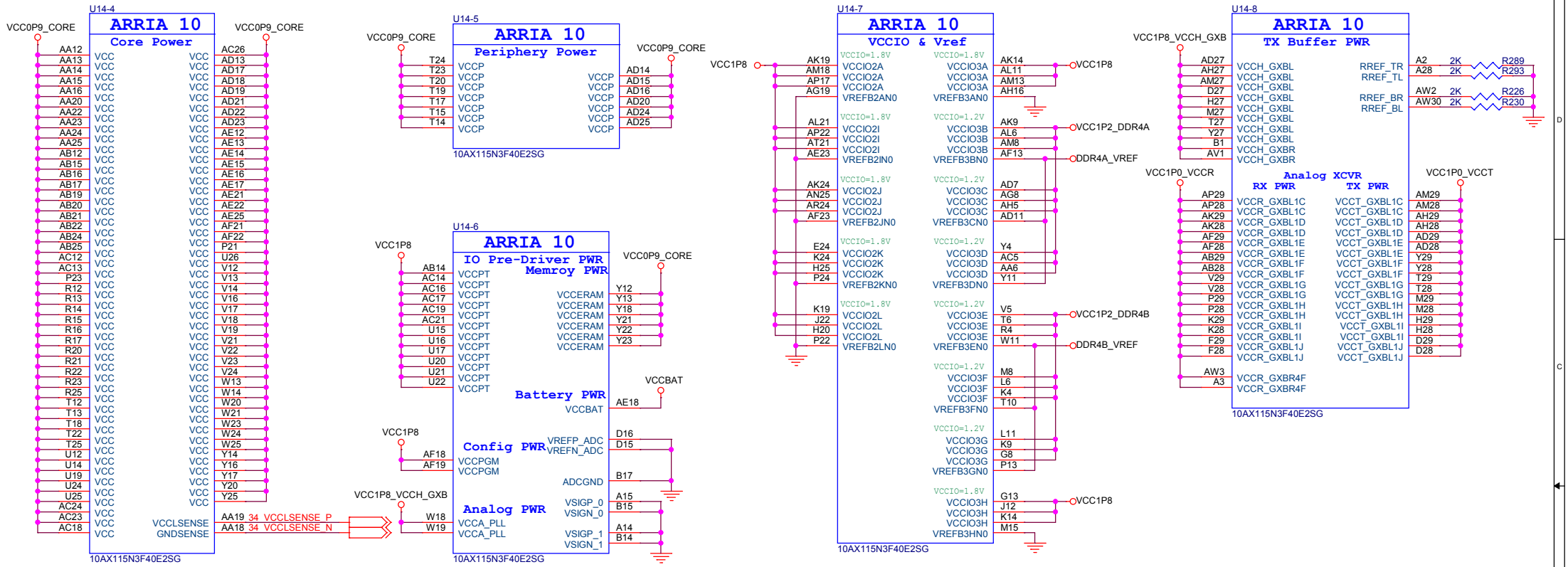
Title: **FLIK**

Size	Document Number	Rev
B	FPGA Configuration	B1

Date: Monday, November 04, 2019 Sheet 17 of 38



VCCLSENSE_P / VCCLSENSE_N sense lines need to be routed as wide traces to its source regulator

Route these connections as differential pair traces and keep them isolated from any other noise source

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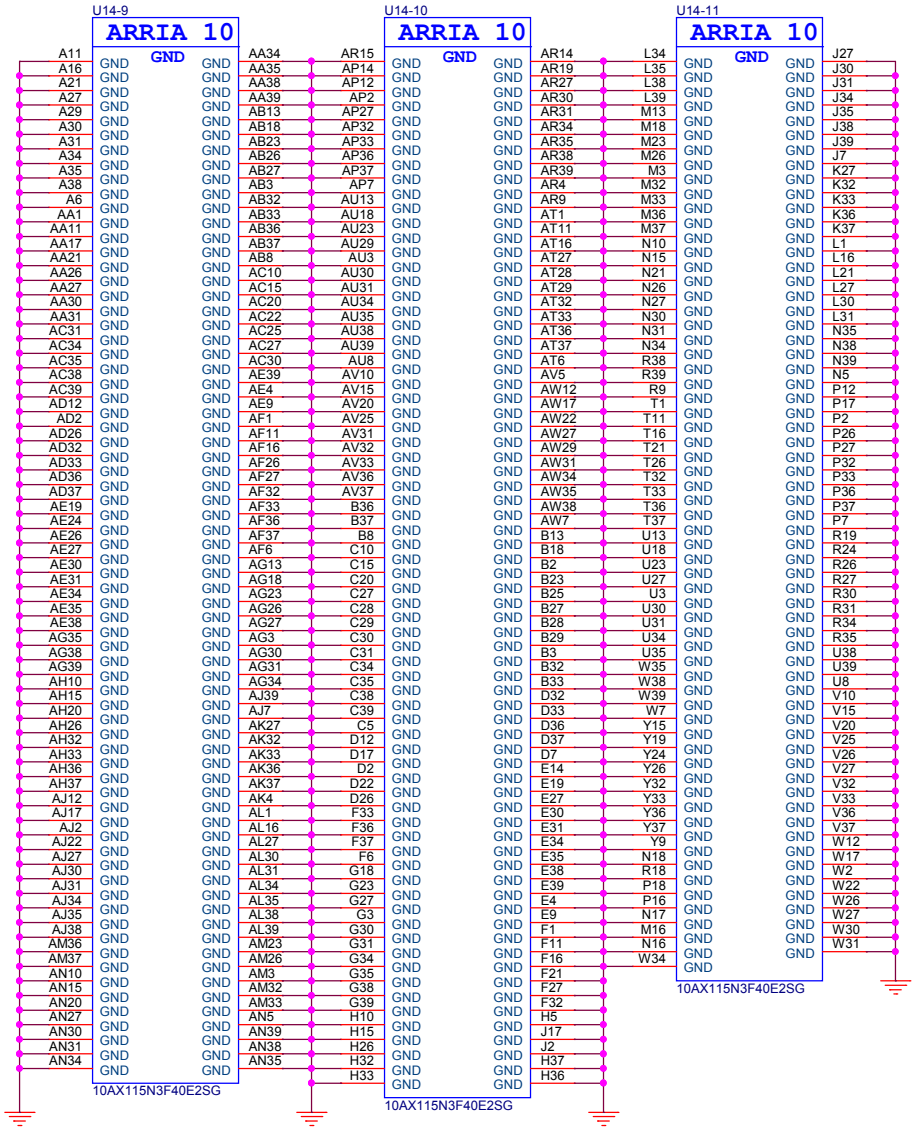
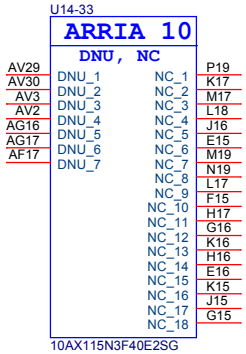
Title	FLIK		
Size B	Document Number FPGA Power		Rev B1
Date: Monday, November 04, 2019	Sheet 18 of 38		





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Title
FLIK

Size	Document Number	Rev
B	FPGA GND	B1

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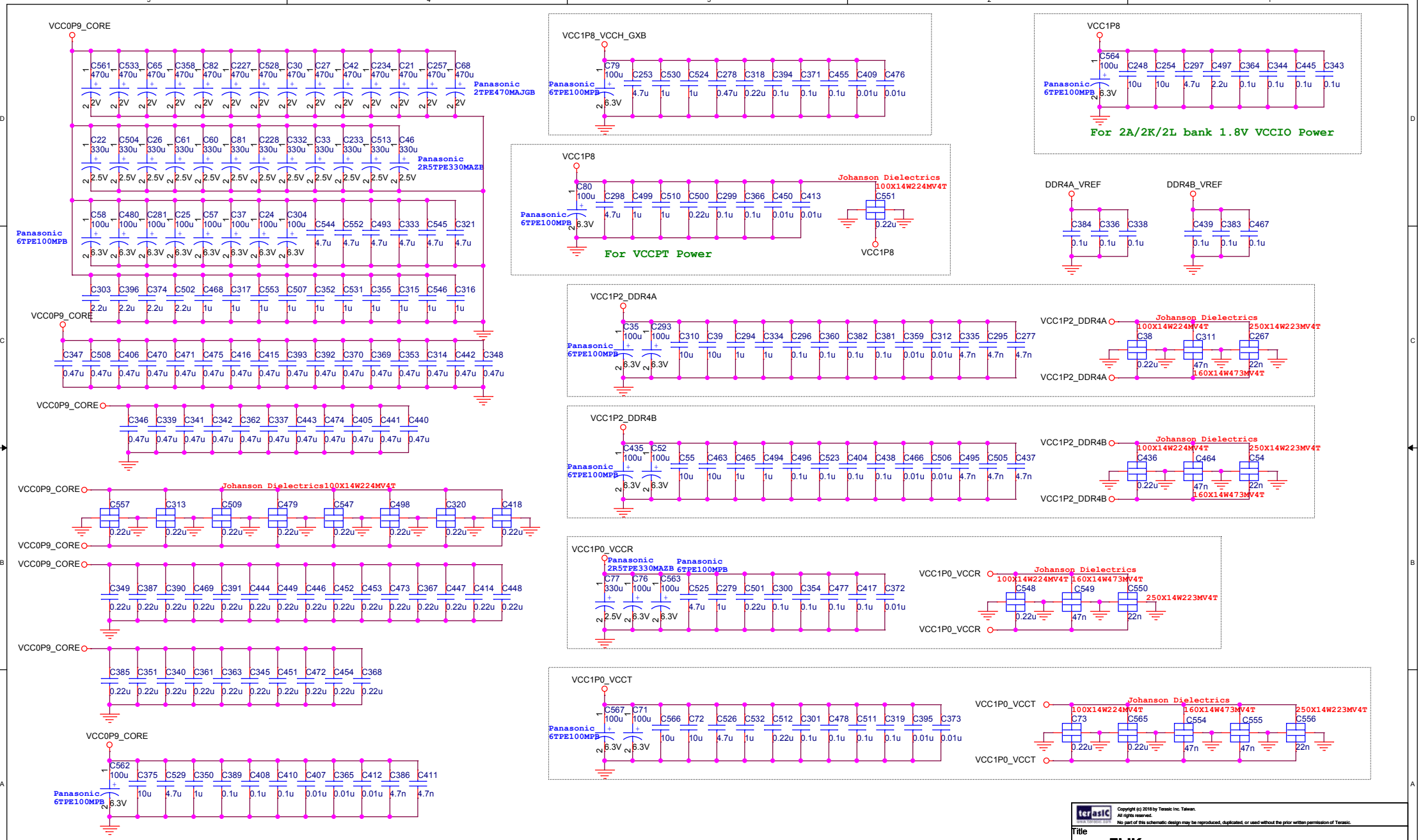
VCC0P9_CORE
C561 470u 2V
C533 470u 2V
C65 470u 2V
C358 470u 2V
C82 470u 2V
C227 470u 2V
C528 470u 2V
C30 470u 2V
C27 470u 2V
C42 470u 2V
C234 470u 2V
C21 470u 2V
C257 470u 2V
C68 470u 2V
Panasonic 2TPE470MAJGB
C22 330u 2.5V
C504 330u 2.5V
C26 330u 2.5V
C61 330u 2.5V
C60 330u 2.5V
C81 330u 2.5V
C228 330u 2.5V
C332 330u 2.5V
C33 330u 2.5V
C233 330u 2.5V
C513 330u 2.5V
C46 330u 2.5V
Panasonic 2R5TPE330MAZB
Panasonic 6TPE100MPB
C58 100u 6.3V
C480 100u 6.3V
C281 100u 6.3V
C25 100u 6.3V
C57 100u 6.3V
C37 100u 6.3V
C24 100u 6.3V
C304 100u 6.3V
C544 4.7u
C552 4.7u
C493 4.7u
C333 4.7u
C545 4.7u
C321 4.7u
C303 2.2u
C396 2.2u
C374 2.2u
C502 2.2u
C468 1u
C317 1u
C553 1u
C507 1u
C352 1u
C531 1u
C355 1u
C315 1u
C546 1u
C316 1u
VCC0P9_CORE
C347 C508 C406 C470 C471 C475 C416 C415 C393 C392 C370 C369 C353 C314 C442 C348 0.47u
VCC0P9_CORE
C346 C339 C341 C342 C362 C337 C443 C474 C405 C441 C440 0.47u
VCC0P9_CORE
Johanson Dielectrics100X14W224MV4T
C557 C313 C509 C479 C547 C498 C320 C418 0.22u
VCC0P9_CORE
VCC0P9_CORE
C349 C387 C390 C469 C391 C444 C449 C446 C452 C453 C473 C367 C447 C414 C448 0.22u
VCC0P9_CORE
C385 C351 C340 C361 C363 C345 C451 C472 C454 C368 0.22u
VCC0P9_CORE
C562 100u 6.3V
Panasonic 6TPE100MPB
C375 10u
C529 4.7u
C350 1u
C389 0.1u
C408 0.1u
C410 0.1u
C407 0.01u
C365 0.01u
C412 0.01u
C386 4.7n
C411 4.7n
VCC1P8_VCCH_GXB
C79 100u 6.3V
Panasonic 6TPE100MPB
C253 4.7u
C530 1u
C524 1u
C278 0.47u
C318 0.22u
C394 0.1u
C371 0.1u
C455 0.1u
C409 0.01u
C476 0.01u
VCC1P8
C80 100u 6.3V
Panasonic 6TPE100MPB
C298 4.7u
C499 1u
C510 1u
C500 0.22u
C299 0.1u
C366 0.1u
C450 0.01u
C413 0.01u
Johanson Dielectrics 100X14W224MV4T
C551 0.22u
VCC1P8
For VCCPT Power
VCC1P8
C564 100u 6.3V
Panasonic 6TPE100MPB
C248 10u
C254 10u
C297 4.7u
C497 2.2u
C364 0.1u
C344 0.1u
C445 0.1u
C343 0.1u
For 2A/2K/2L bank 1.8V VCCIO Power
DDR4A_VREF
C384 C336 C338 0.1u
DDR4B_VREF
C439 C383 C467 0.1u
VCC1P2_DDR4A
C35 100u 6.3V
C293 100u 6.3V
Panasonic 6TPE100MPB
C310 10u
C39 10u
C294 1u
C334 1u
C296 0.1u
C360 0.1u
C382 0.1u
C381 0.1u
C359 0.01u
C312 0.01u
C335 4.7n
C295 4.7n
C277 4.7n
VCC1P2_DDR4A
Johanson Dielectrics
100X14W224MV4T C38 0.22u
C311 47n 160X14W473MV4T
250X14W223MV4T C267 22n
VCC1P2_DDR4A
VCC1P2_DDR4B
C435 100u 6.3V
C52 100u 6.3V
Panasonic 6TPE100MPB
C55 10u
C463 10u
C465 1u
C494 1u
C496 0.1u
C523 0.1u
C404 0.1u
C438 0.1u
C466 0.01u
C506 0.01u
C495 4.7n
C505 4.7n
C437 4.7n
VCC1P2_DDR4B
Johanson Dielectrics
100X14W224MV4T C436 0.22u
C464 47n 160X14W473MV4T
250X14W223MV4T C54 22n
VCC1P2_DDR4B
VCC1P0_VCCR
Panasonic 2R5TPE330MAZB
Panasonic 6TPE100MPB
C77 330u 2.5V
C76 100u 6.3V
C563 100u 6.3V
C525 4.7u
C279 1u
C501 0.22u
C300 0.1u
C354 0.1u
C477 0.1u
C417 0.1u
C372 0.01u
VCC1P0_VCCR
Johanson Dielectrics
100X14W224MV4T C548 0.22u
160X14W473MV4T C549 47n
250X14W223MV4T C550 22n
VCC1P0_VCCR
VCC1P0_VCCT
C567 100u 6.3V
C71 100u 6.3V
Panasonic 6TPE100MPB
C566 10u
C72 10u
C526 4.7u
C532 1u
C512 0.22u
C301 0.1u
C478 0.1u
C511 0.1u
C319 0.1u
C395 0.01u
C373 0.01u
VCC1P0_VCCT
Johanson Dielectrics
100X14W224MV4T C73 0.22u
C565 0.22u
160X14W473MV4T C554 47n
C555 47n
250X14W223MV4T C556 22n
VCC1P0_VCCT
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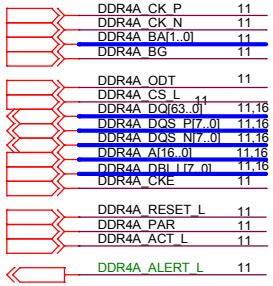
Title
FLIK
Size B
Document Number
FPGA Decoupling
Rev B1
Date: Monday, November 04, 2019
Sheet 20 of 38

DDR4 SDRAM - A



RAS_n is a multiplexed function with A16
CAS_n is a multiplexed function with A15
WE_n is a multiplexed function with A14

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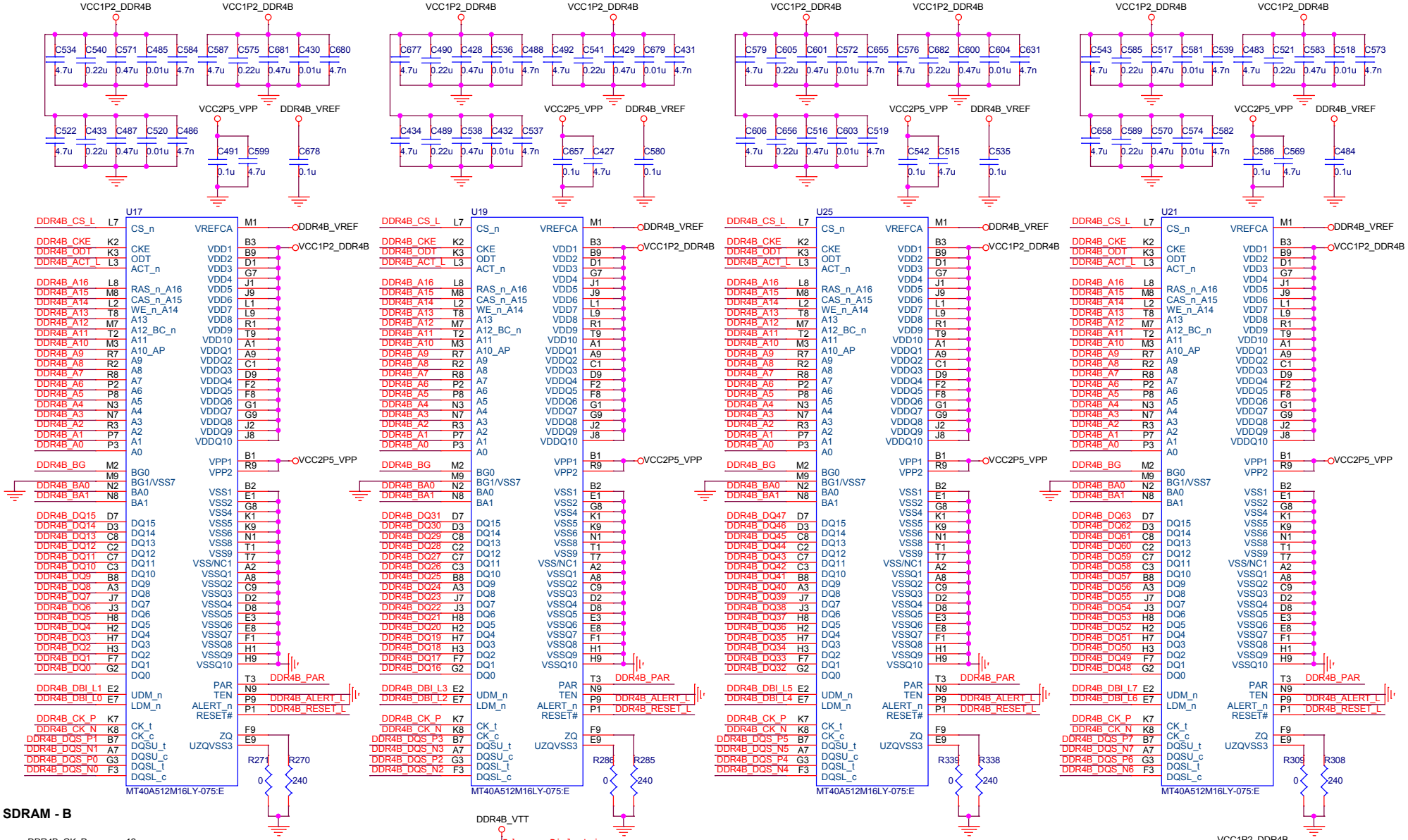
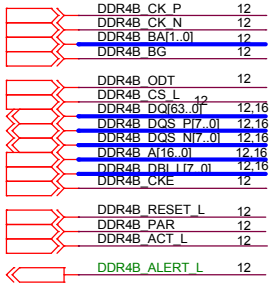
Title: **FLIK**

Size	Document Number	Rev
Custom	DDR4 SDRAM - A	B1

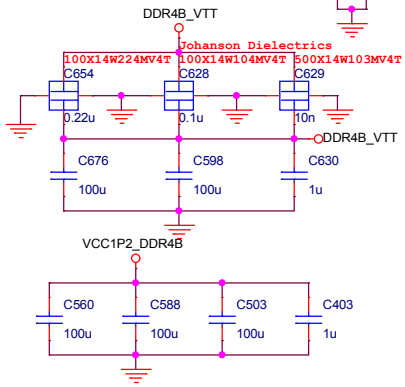
Date: Monday, November 04, 2019 Sheet 21 of 38

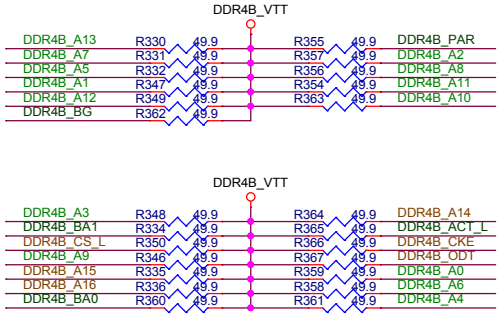


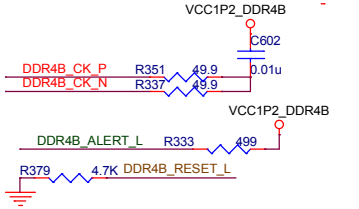
DDR4 SDRAM - B



RAS_n is a multiplexed function with A16
CAS_n is a multiplexed function with A15
WE_n is a multiplexed function with A14







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Title: **FLIK**

Size	Document Number	Rev
Custom	DDR4 SDRAM - B	B1

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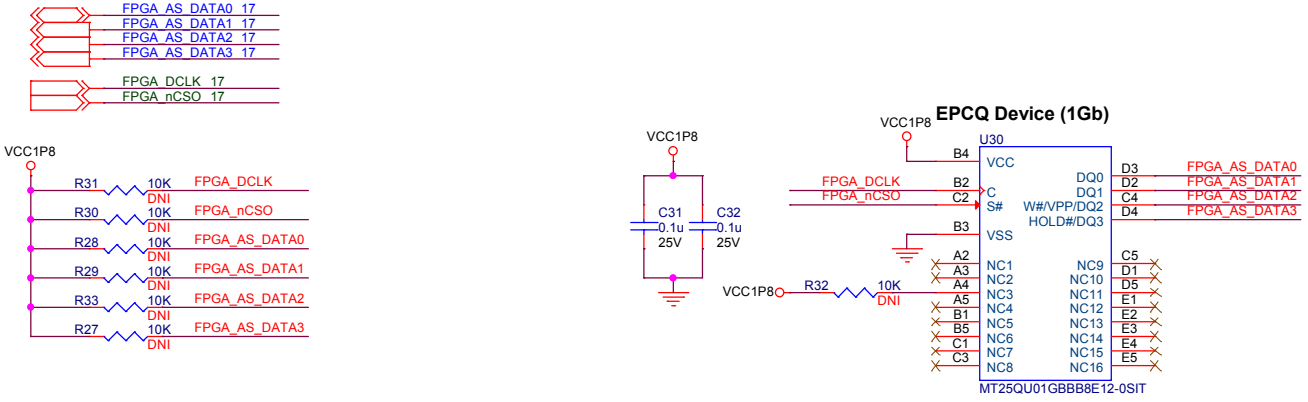
FPGA AS Mode Configuration



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FLIK

Size	Document Number	Rev
B	EPCQ	B1

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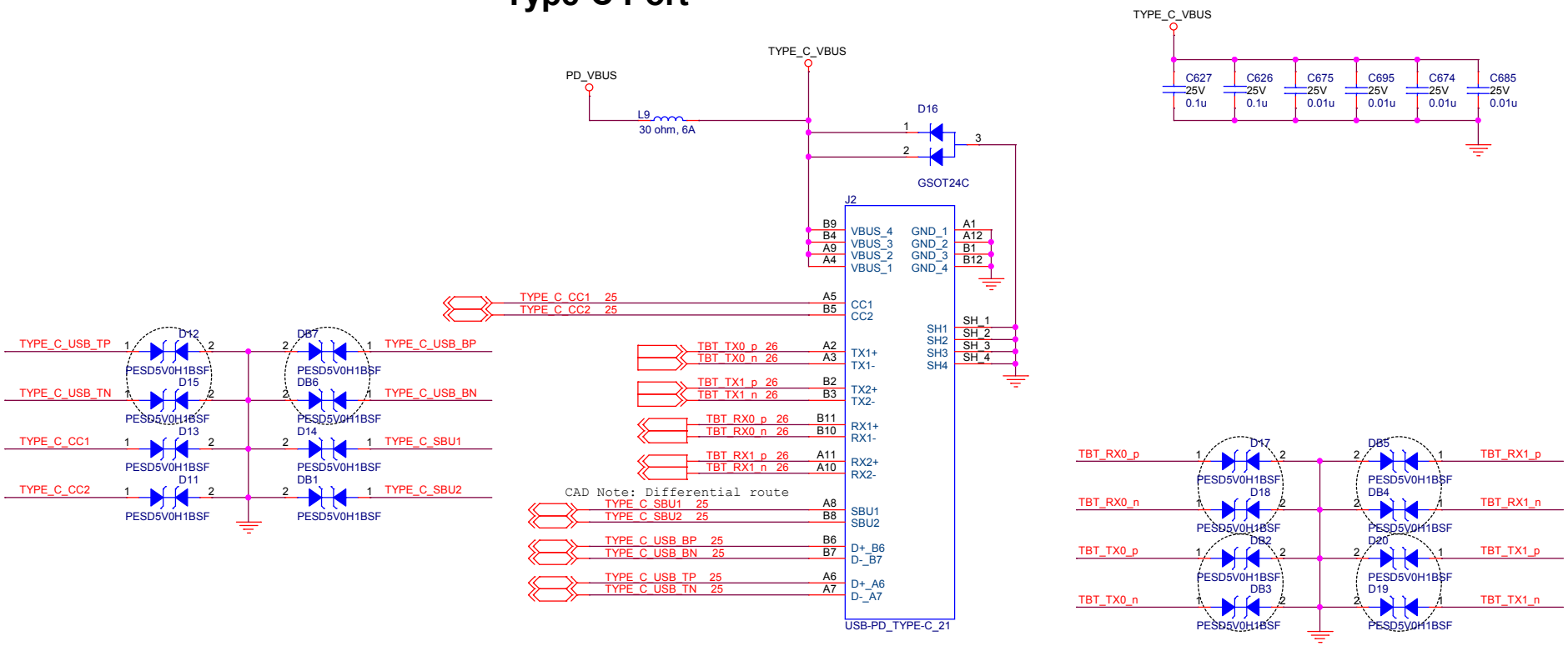
Type-C Port



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Title	FLIK	
Size B	Document Number Type-C Port	Rev B1
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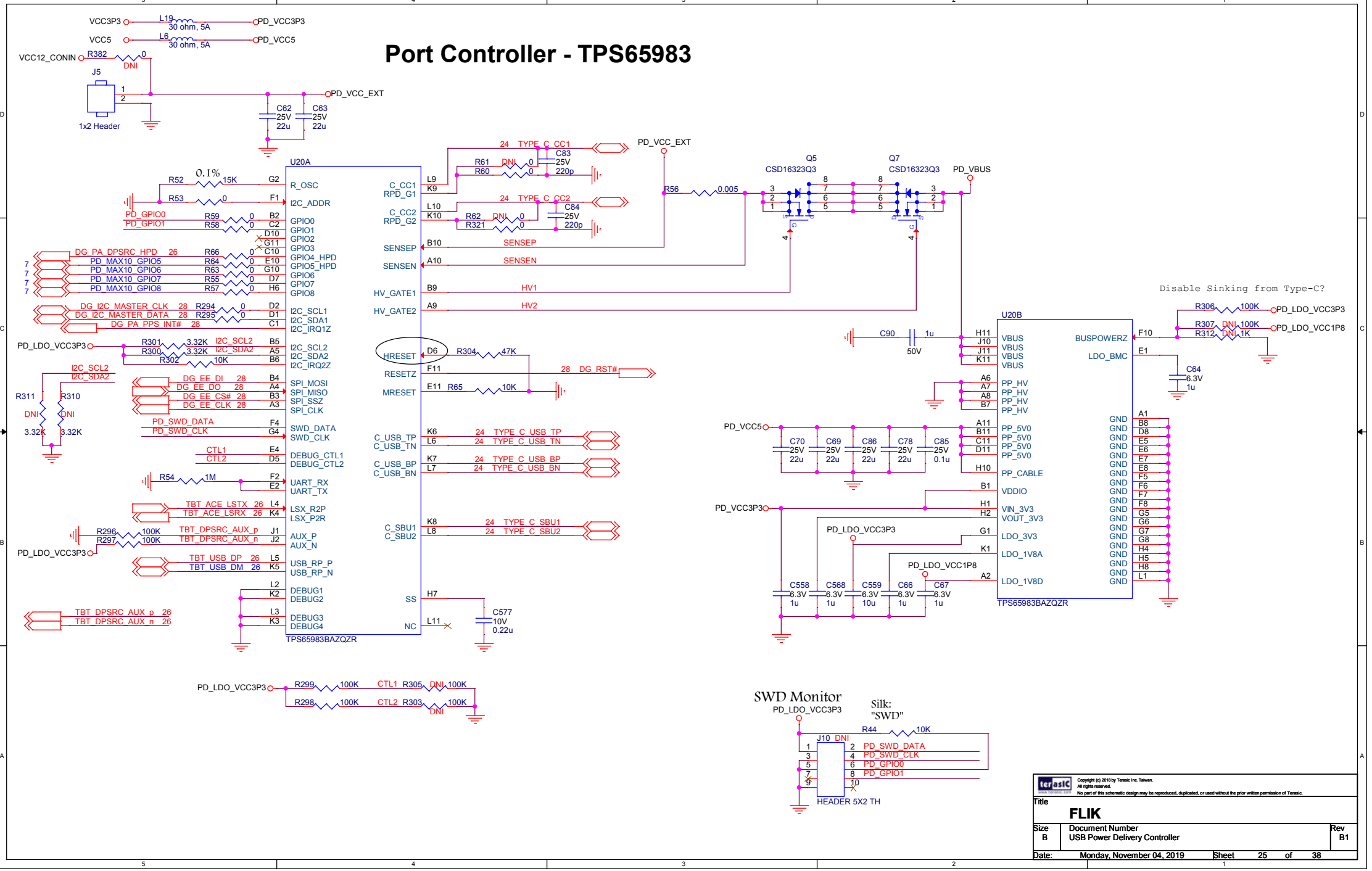
Port Controller - TPS65983



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Title	FLIK	
Size B	Document Number USB Power Delivery Controller	Rev B1
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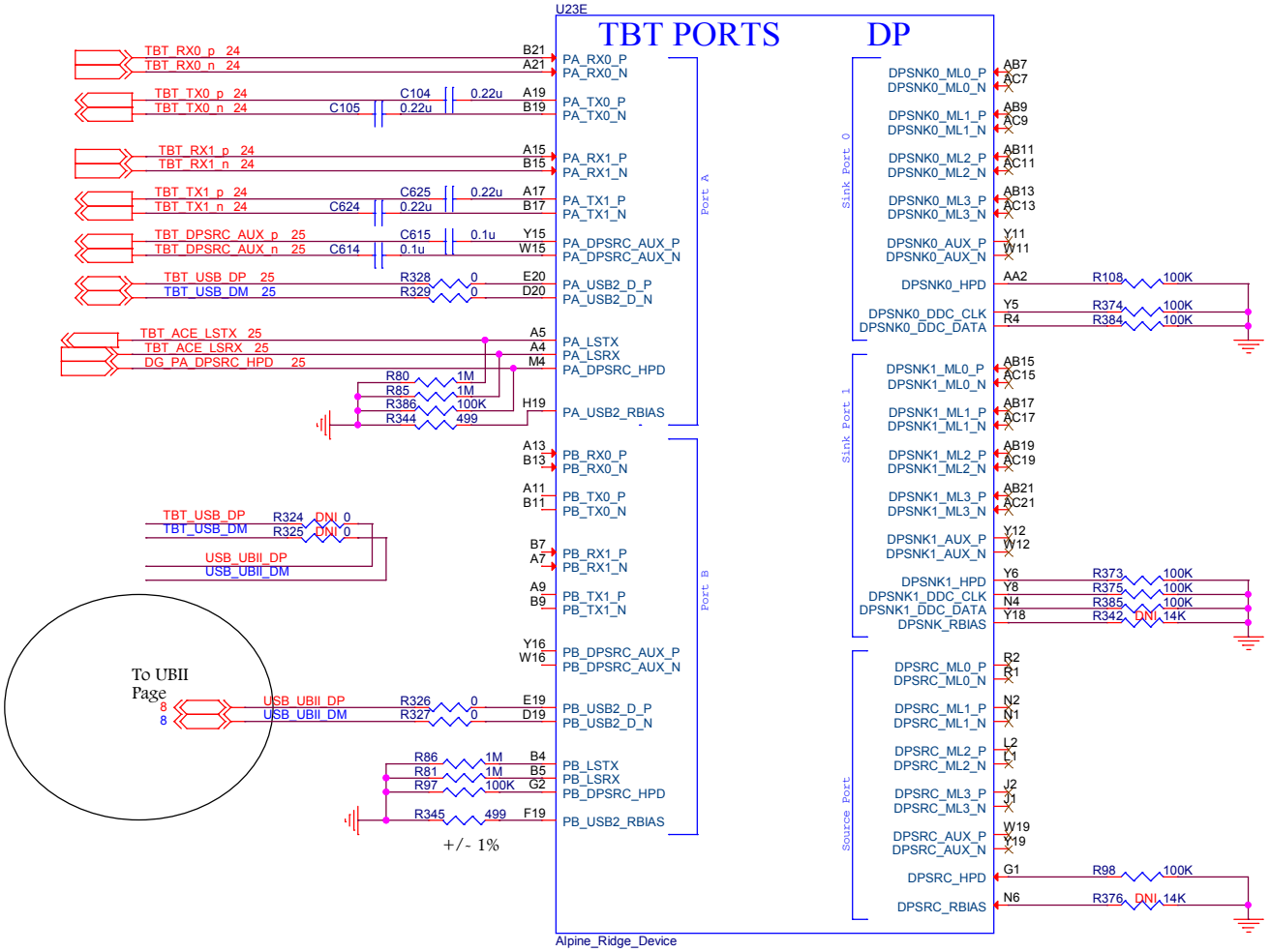
Alpine Ridge 4C - TBT, USB2



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Title
FLIK

Size	Document Number	Rev
B	AR - TBT3 & USB2	B1

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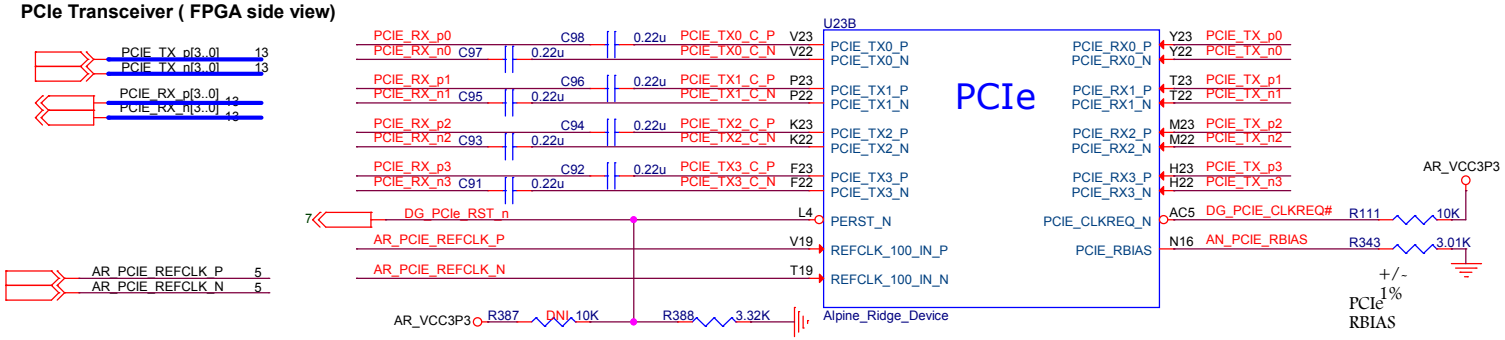
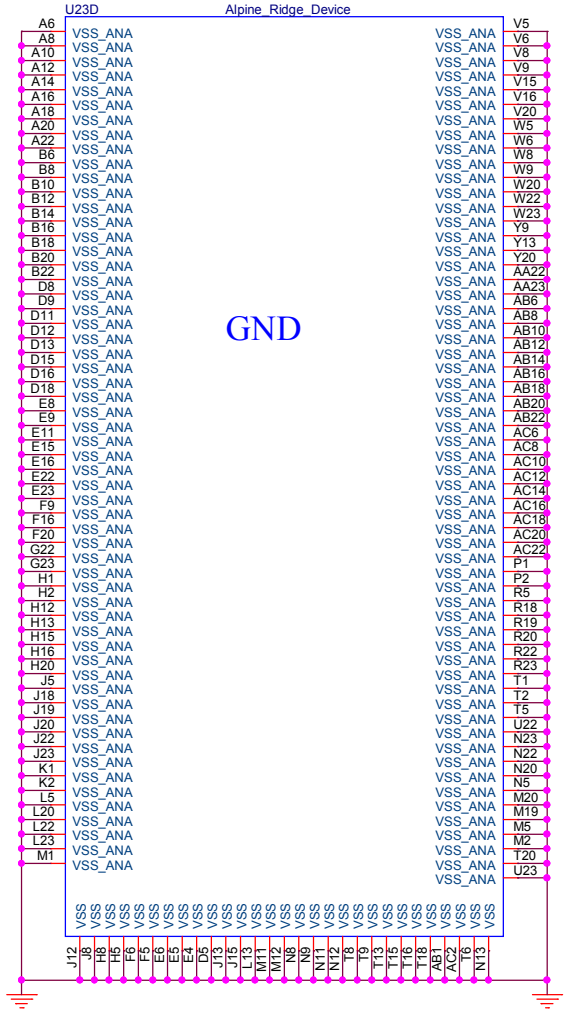
Alpine Ridge 4C - PCIe & GND



Alpine Ridge - GND Symbol



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Title	FLIK	
Size B	Document Number AR - PCIe & GND	Rev B1
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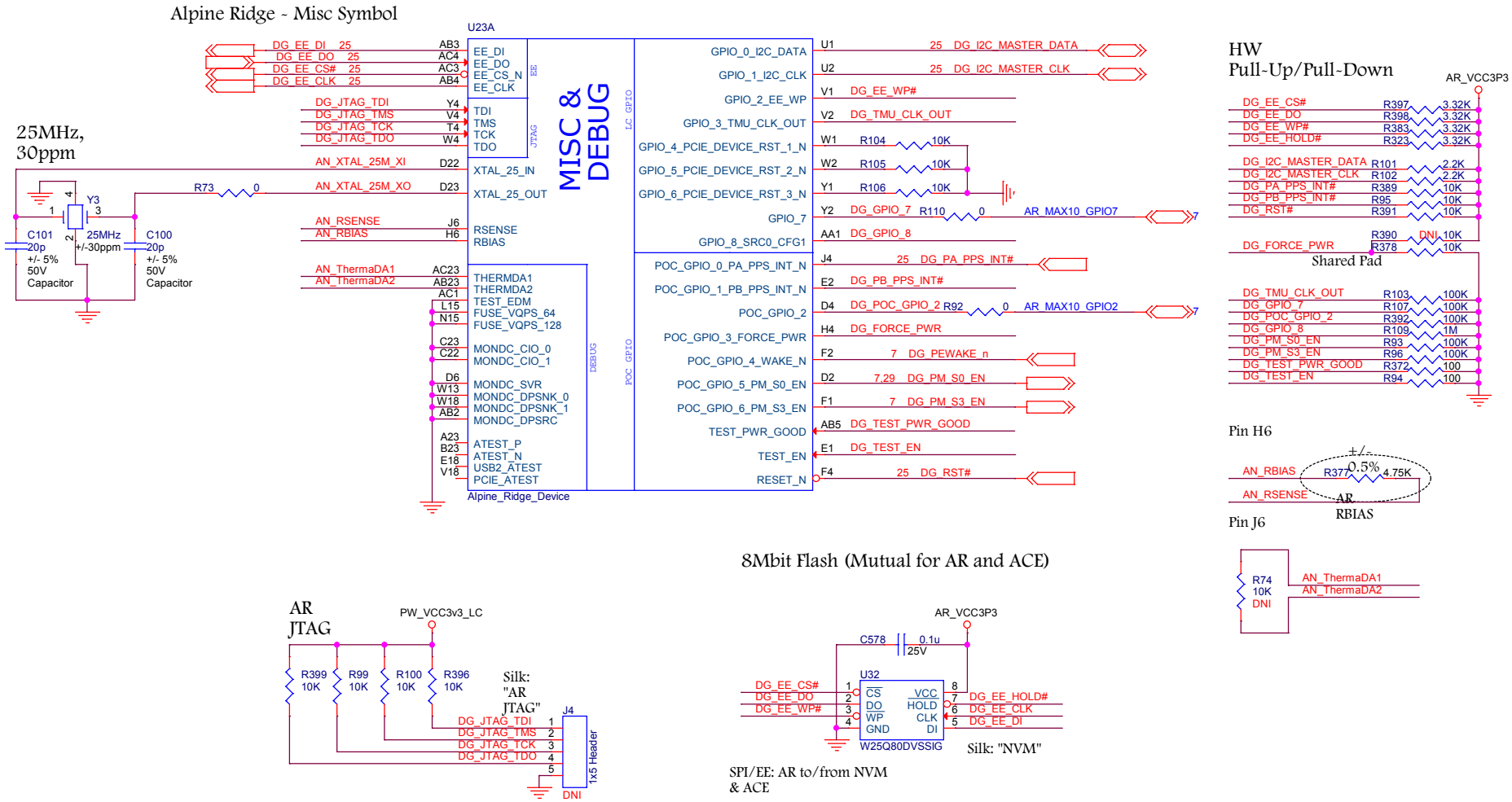
AR - MISC



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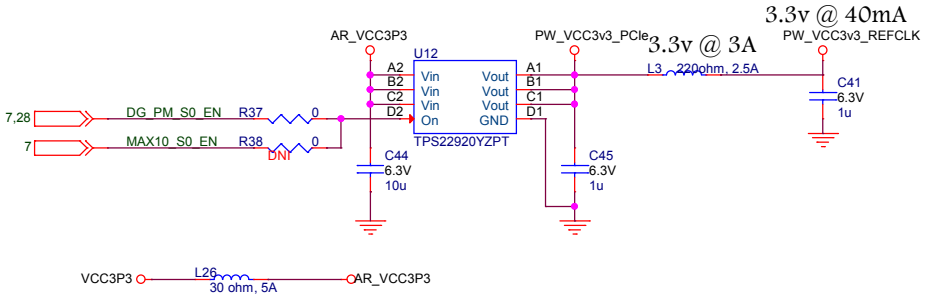
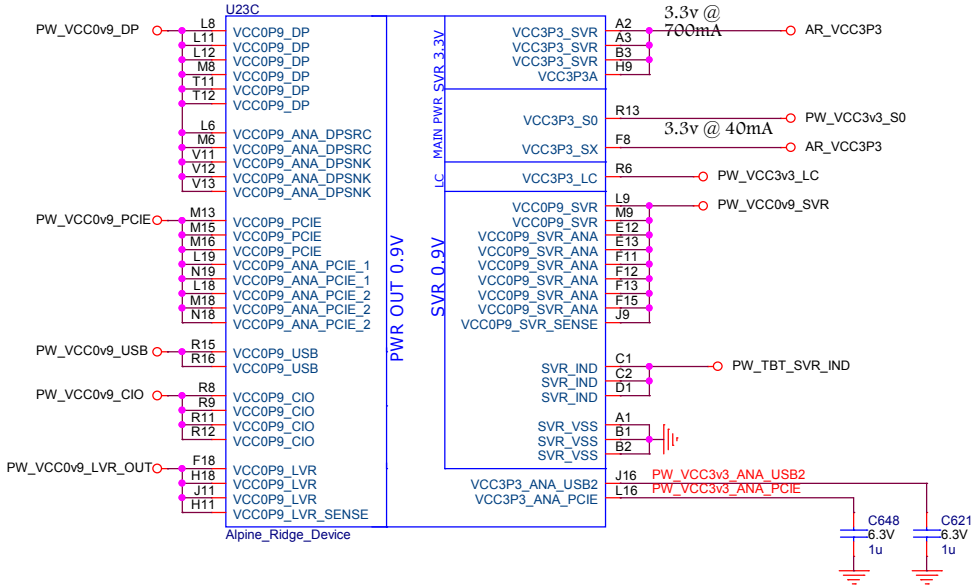
Title	FLIK	
Size B	Document Number AR - MISC	Rev B1
Date: Monday, November 04, 2019	Sheet 28 of 38	

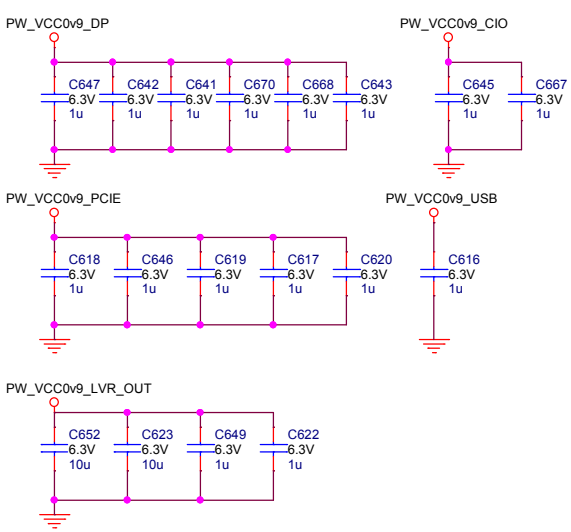
Alpine Ridge 4C - Power Supply

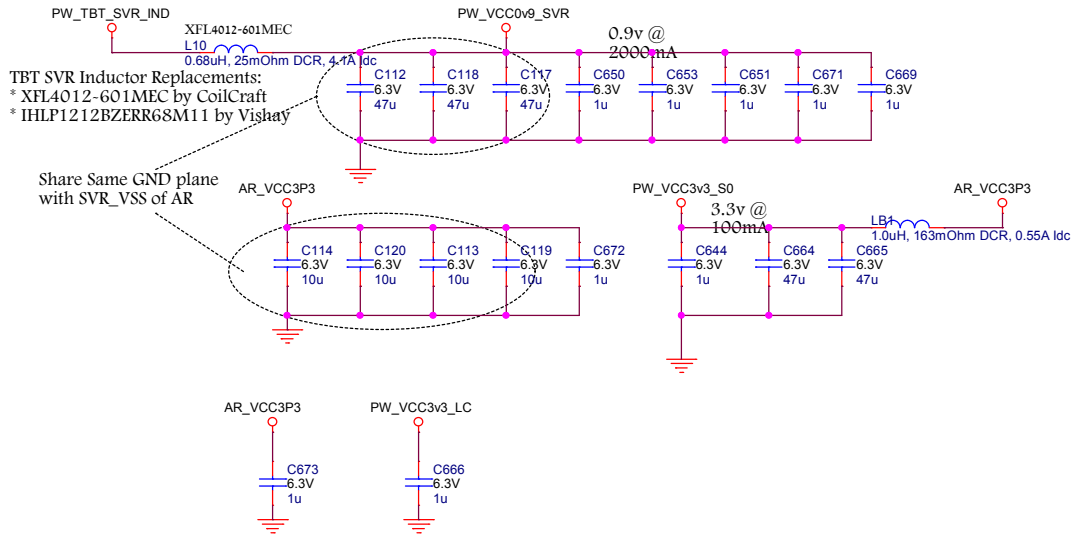


Alpine Ridge - VCC Symbol



Power Supply Decoupling





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Title	FLIK	
Size B	Document Number AR - Power	Rev B1
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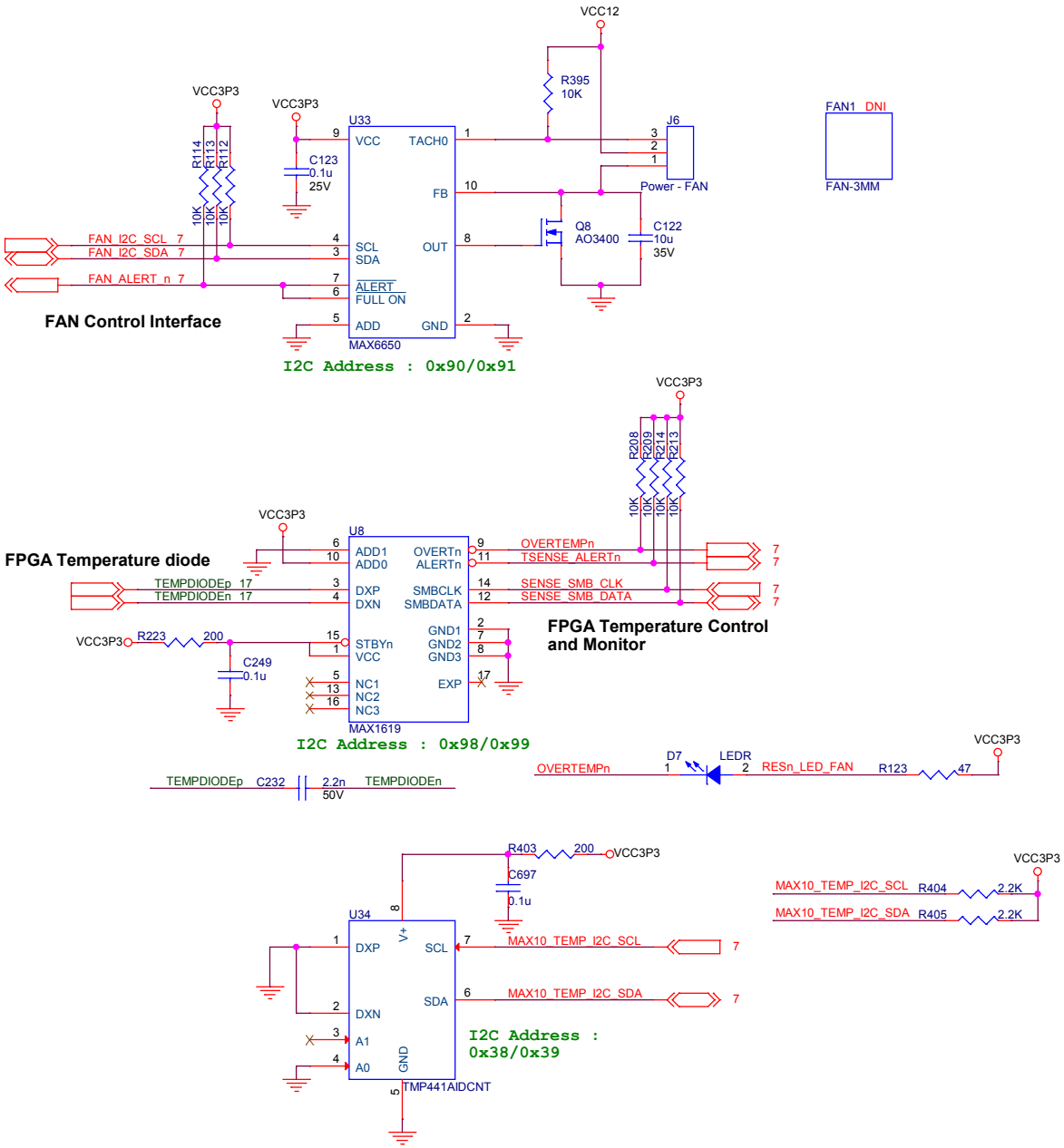

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Title
FLIK

Size	Document Number	Rev
B	FAN Control and Temperature Monitor	B1

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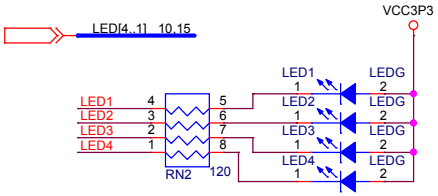
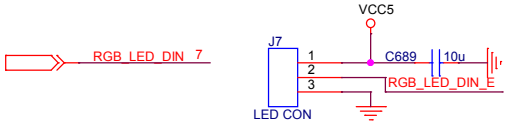
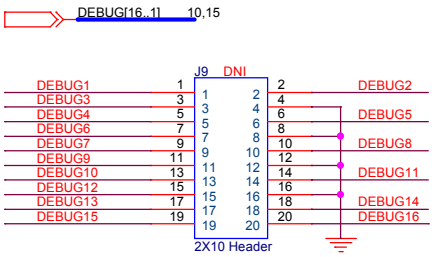
USER LEDS

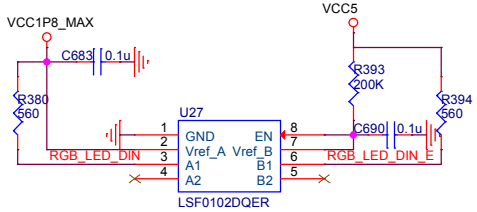


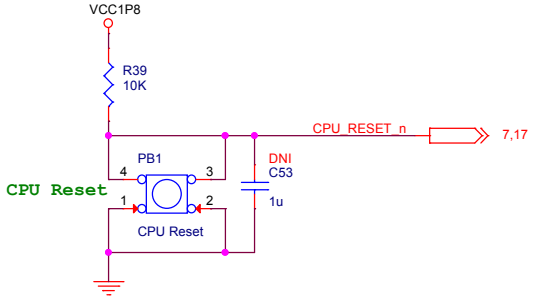
Zip LEDs



Debug Interface







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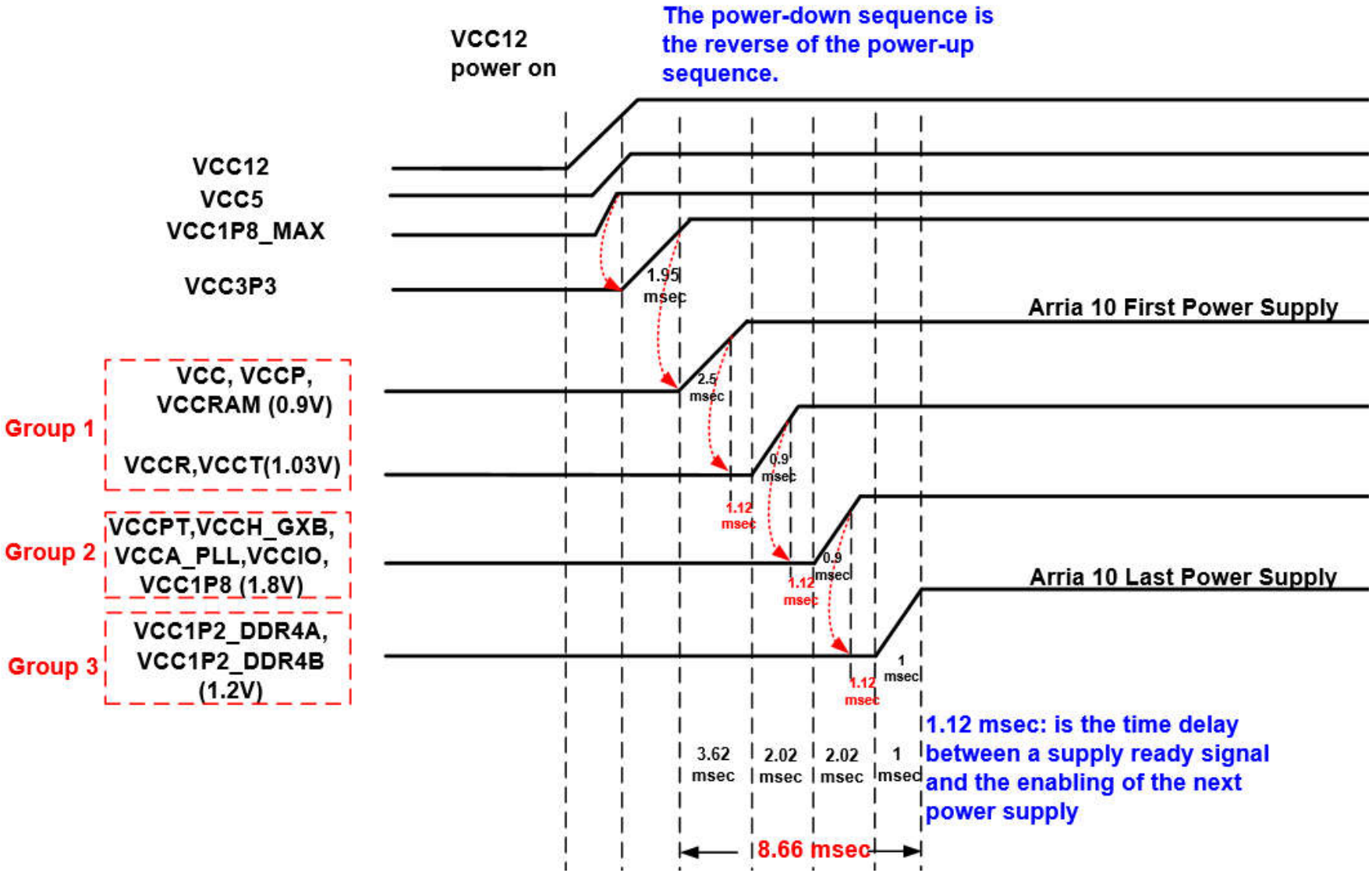
Title	FLIK	
Size B	Document Number Button, Switch, RGBLED, User LED	Rev B1
Date: Monday, November 04, 2019	Sheet 31 of 38	

Arria 10 Power-up Sequence Design Diagram



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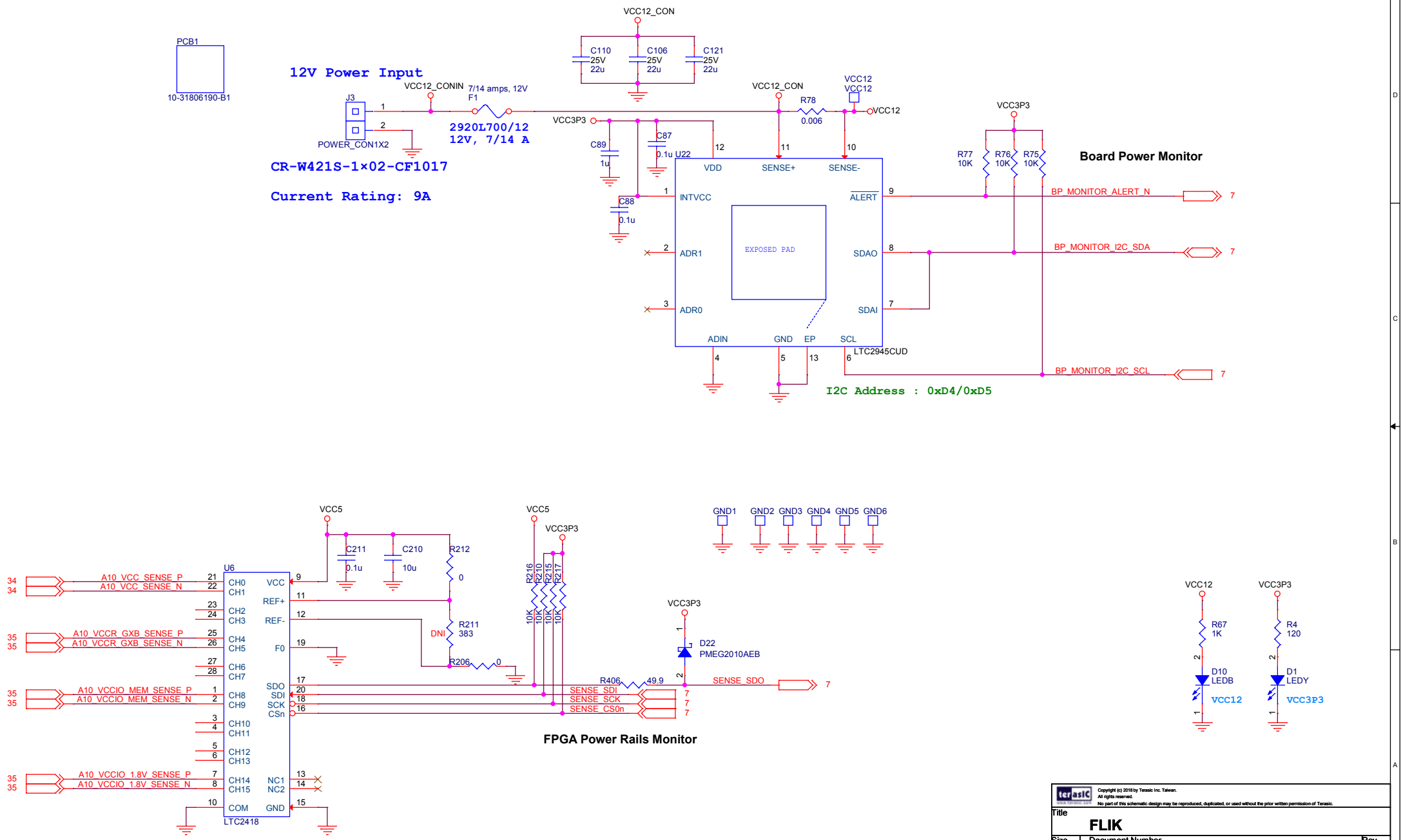
Title	FLIK	
Size B	Document Number Power-up Sequence	Rev B1
Date: Monday, November 04, 2019	Sheet 32 of 38	



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Title: **FLIK**

Size	Document Number	Rev
B	Power - 12 V Power Input and Power Monitor	B1

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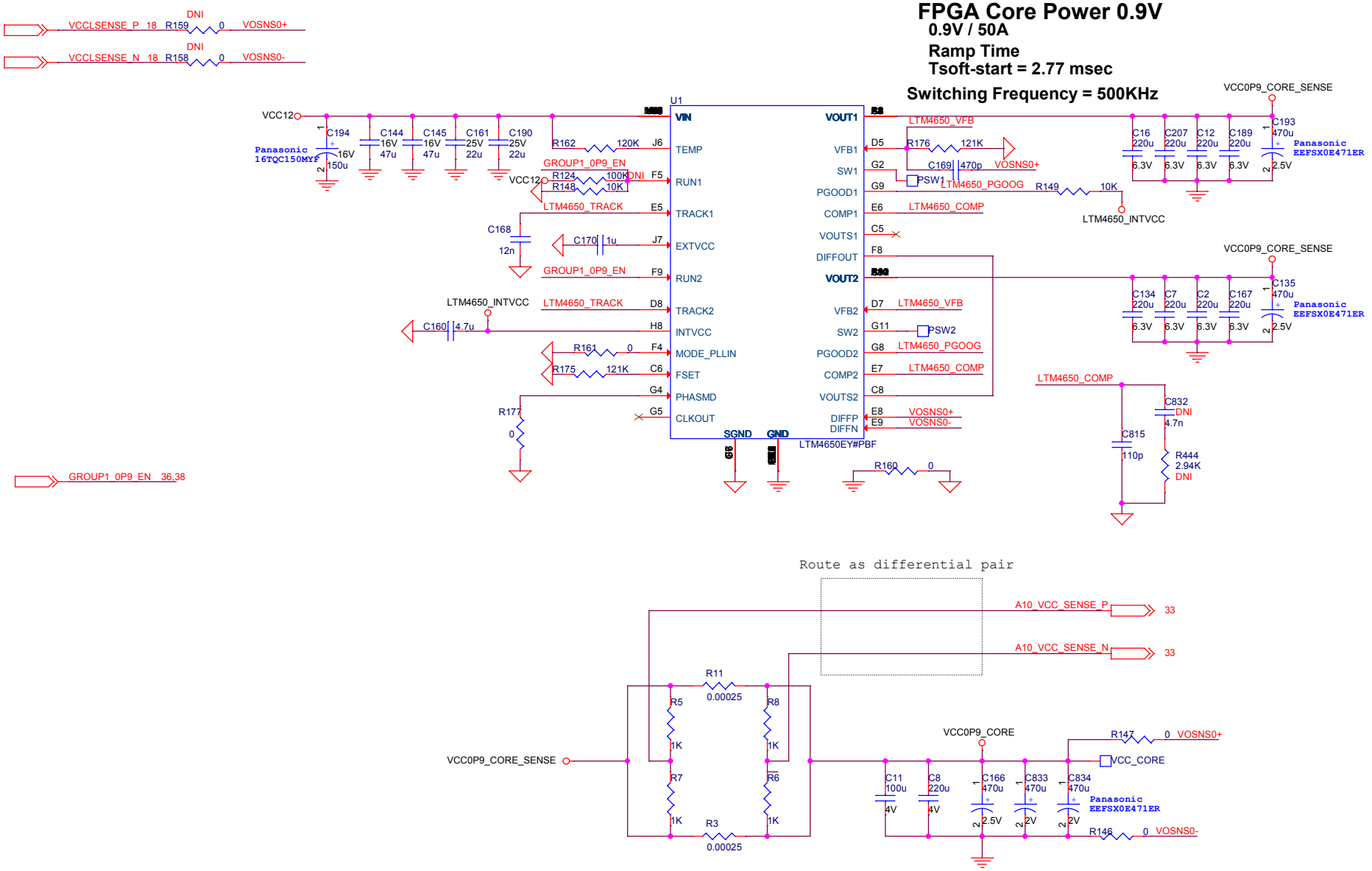
FPGA Core Power 0.9V

0.9V / 50A

Ramp Time

Tsoft-start = 2.77 msec

Switching Frequency = 500KHz



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Title: **FLIK**

Size	Document Number	Rev
B	Power - 0.9V FPGA Core	B1

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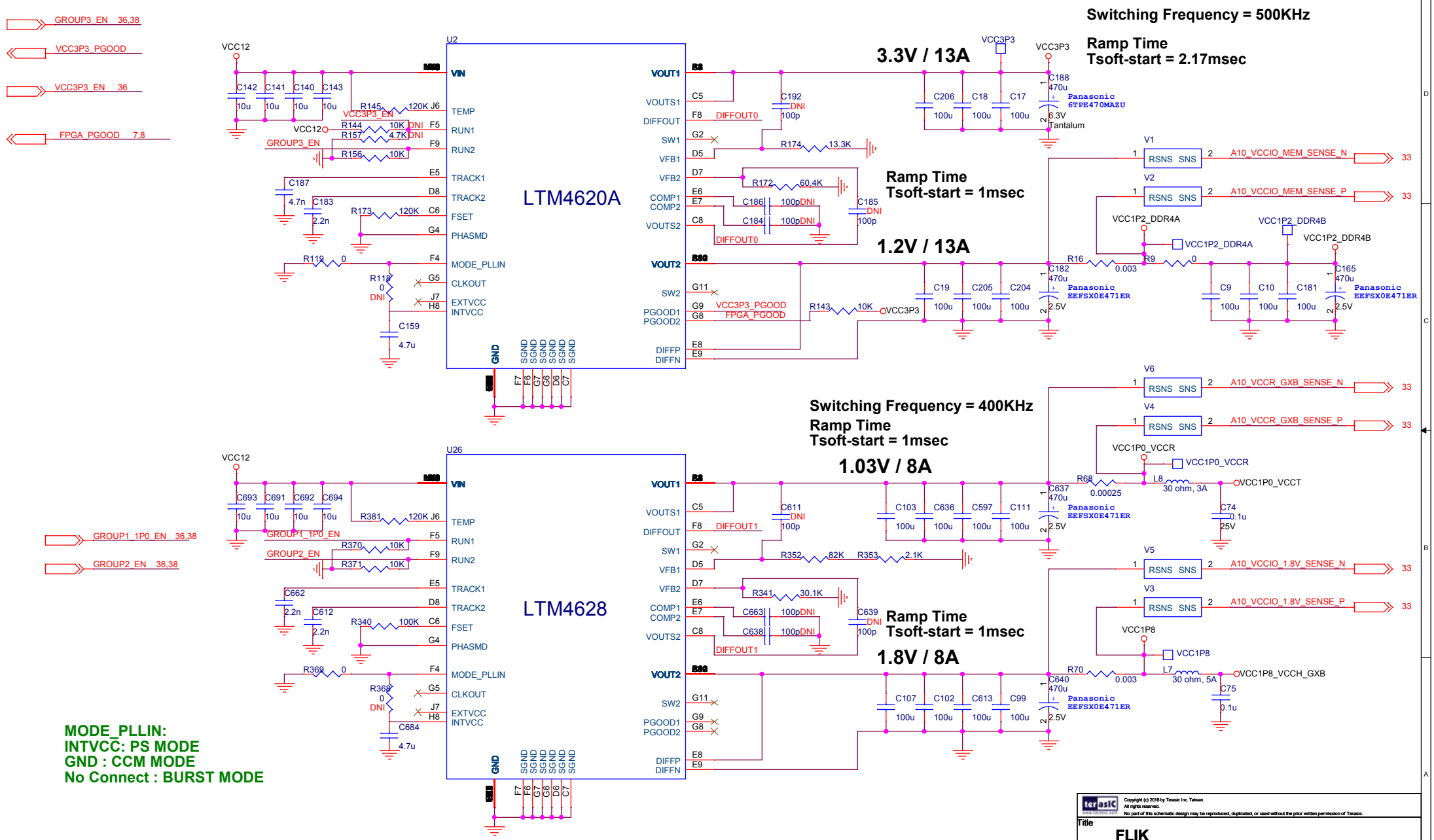

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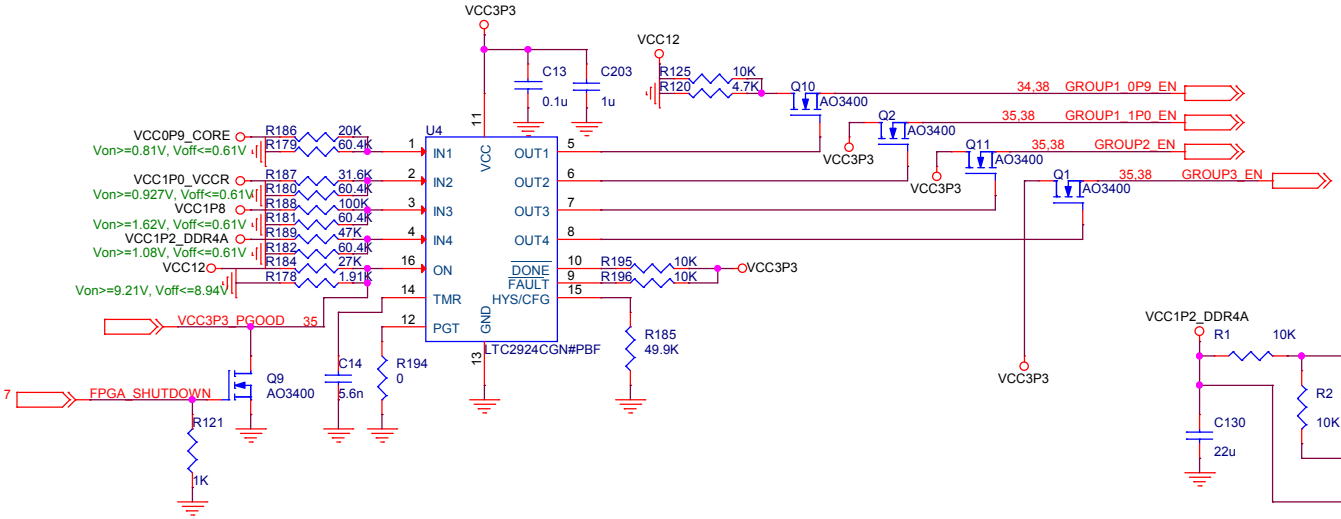
Title
FLIK

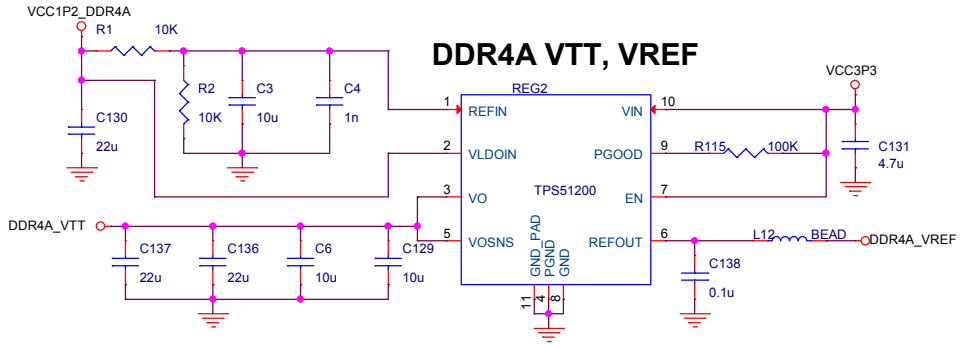
Size	Document Number	Rev
B	Power - 1.03V, 1.2V, 1.8V and 3.3V	B1

Date: Monday, November 04, 2019 Sheet 35 of 38

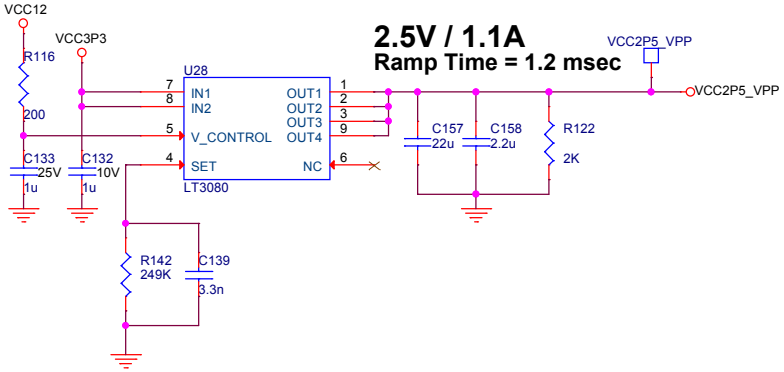
Power up Sequence Control



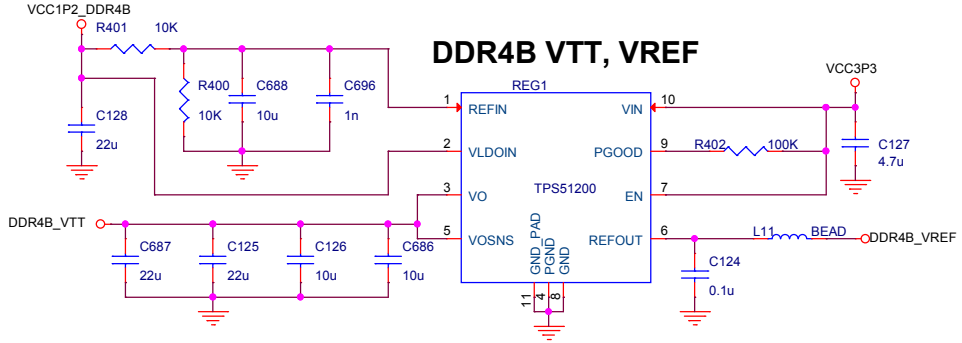
DDR4A VTT, VREF



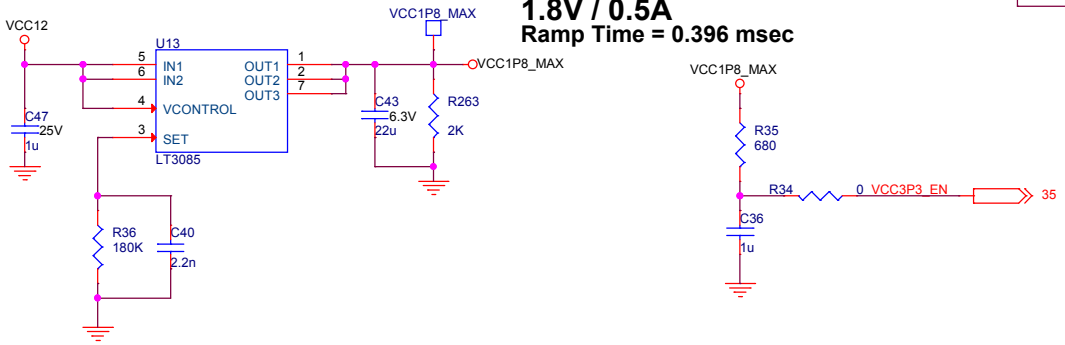
2.5V / 1.1A
Ramp Time = 1.2 msec



DDR4B VTT, VREF



1.8V / 0.5A
Ramp Time = 0.396 msec



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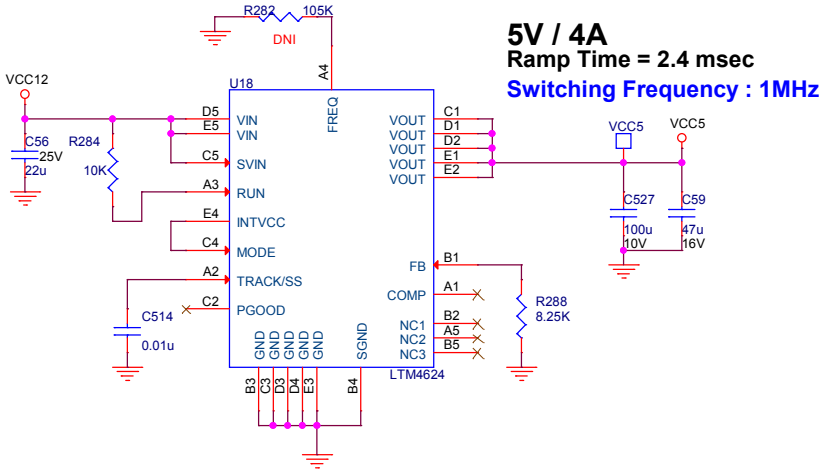
Title	FLIK	
Size B	Document Number Power - 1.8V, 2.5V, DDR4 VTT/VREF and Power Sequence Control	Rev B1
Date: Monday, November 04, 2019	Sheet 36 of 38	



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Title
FLIK

Size	Document Number	Rev
B	Power - 5V	B1

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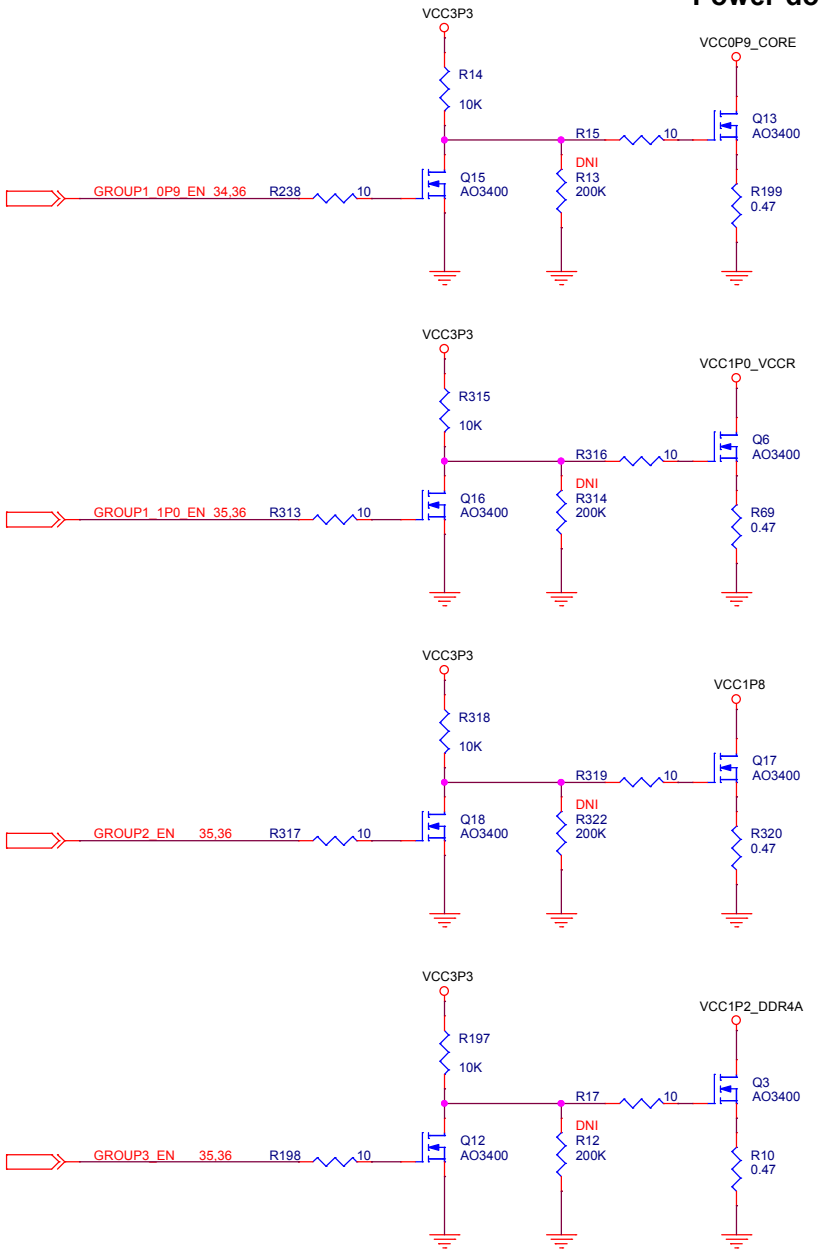
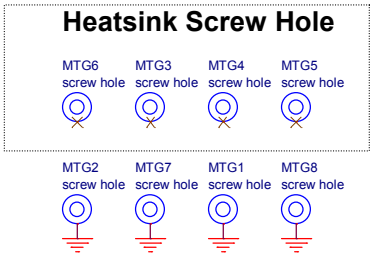
Power-down Fast Discharge



Heatsink Screw Hole



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Title: FLIK

Size	Document Number	Rev
B	Power-Down Discharge	B1

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