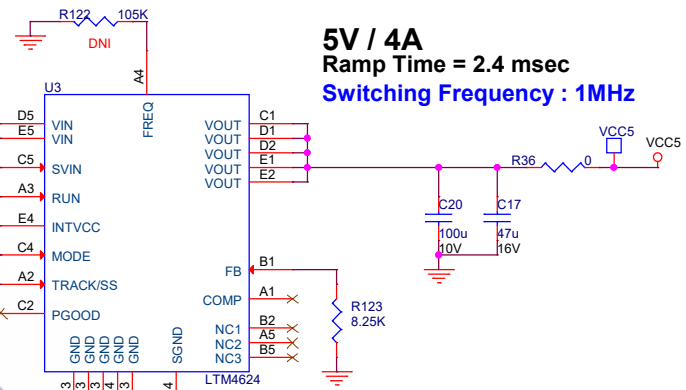
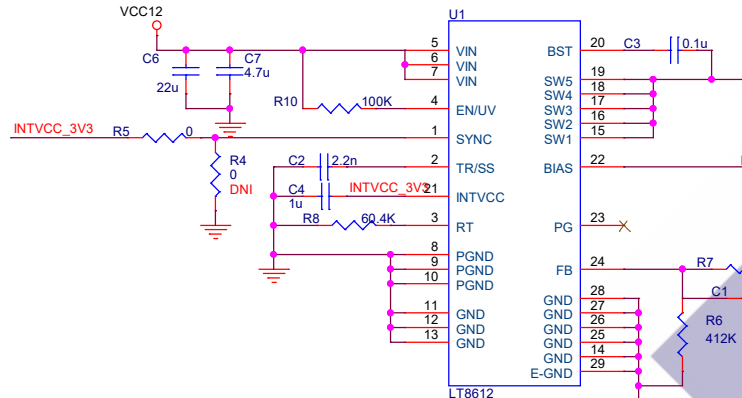


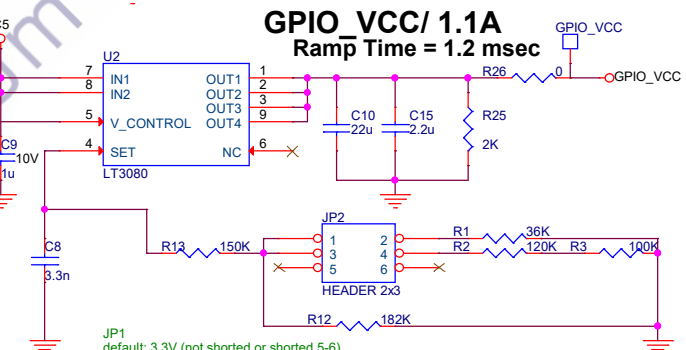
Ramp Time
Tsoft-start = 1.1msec
System 3.3V, 6A
Switching Frequency = 700KHz



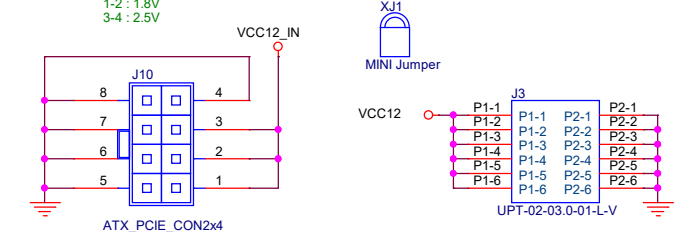
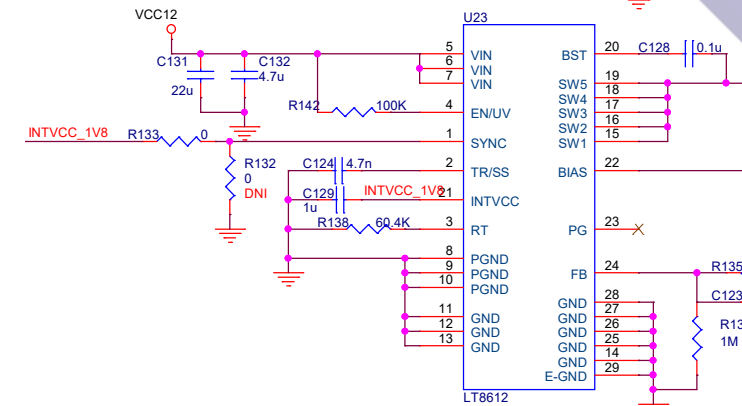
5V / 4A
Ramp Time = 2.4 msec
Switching Frequency : 1MHz



1.8V / 6A
Ramp Time
Tsoft-start = 2.2msec
Switching Frequency = 700KHz

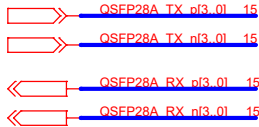


GPIO VCC/ 1.1A
Ramp Time = 1.2 msec

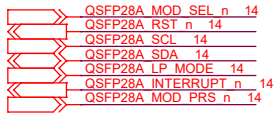


<div> <div>terasic</div> <div>Copyright (c) 2017 by Terasic Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.</div> </div>		
Title		
Apollo Carrier		
Size	Document Number	Rev
B	Power	C0
Date:	Wednesday, September 22, 2021	Sheet 2 of 18

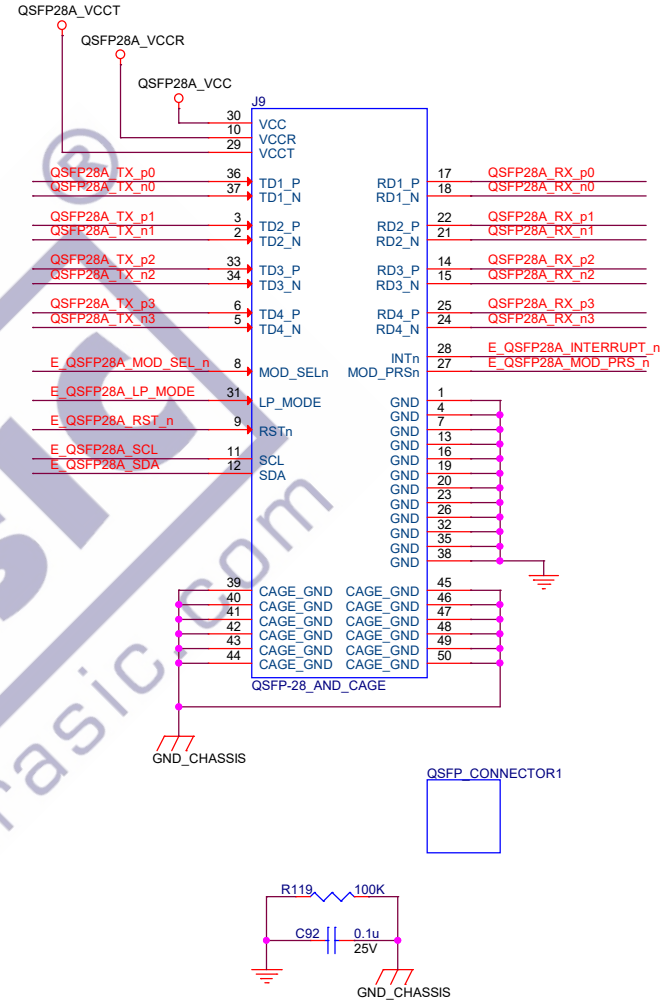
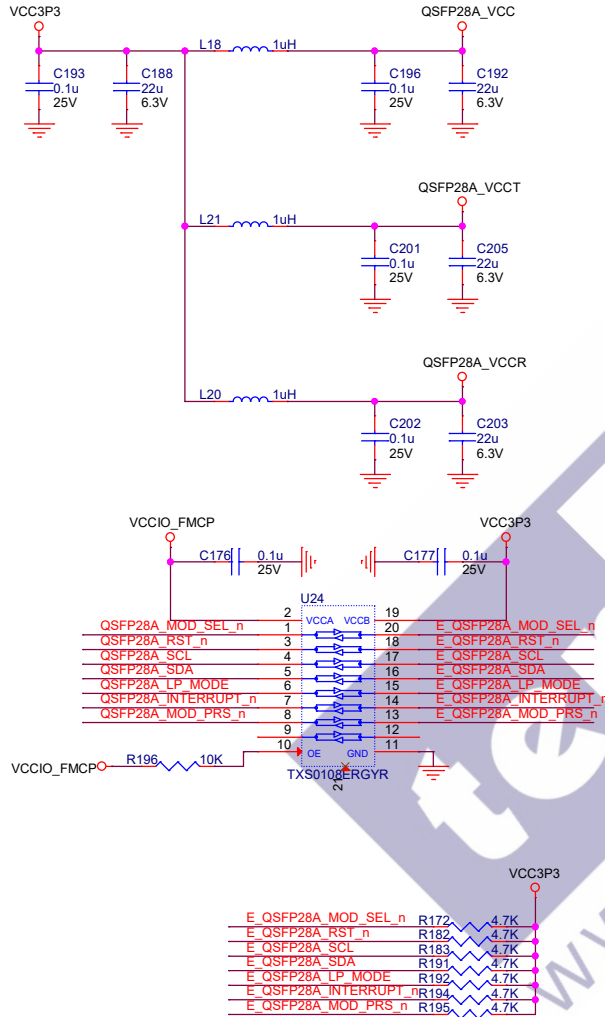
QSFP28 Port A Transceivers



QSFP28A Control Interface



NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.
 NOTE 2: Assuming that the SFP RD 100-ohm termination on the Host Board FPGA device will be implemented via the on-chip termination circuit.
 NOTE 3: DC blocking capacitors are in the module for RX and TX.
 NOTE 4: 1uH inductors should have a DC Resistance of less than 0.1-ohm.



QSFP28 Port B Transceivers

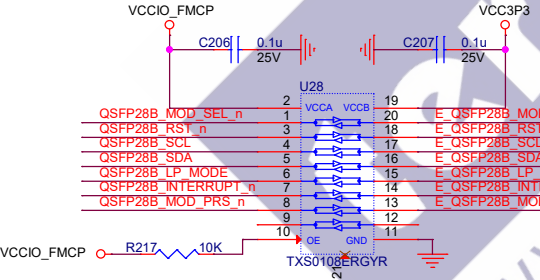
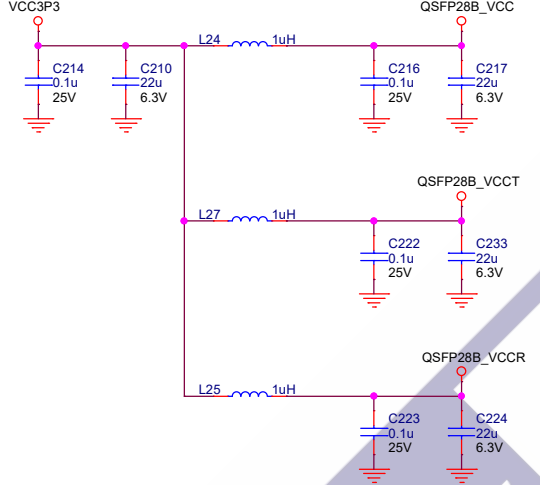
QSFP28B_TX_p[3..0]_15
 QSFP28B_TX_n[3..0]_15

QSFP28B_RX_p[3..0]_15
 QSFP28B_RX_n[3..0]_15

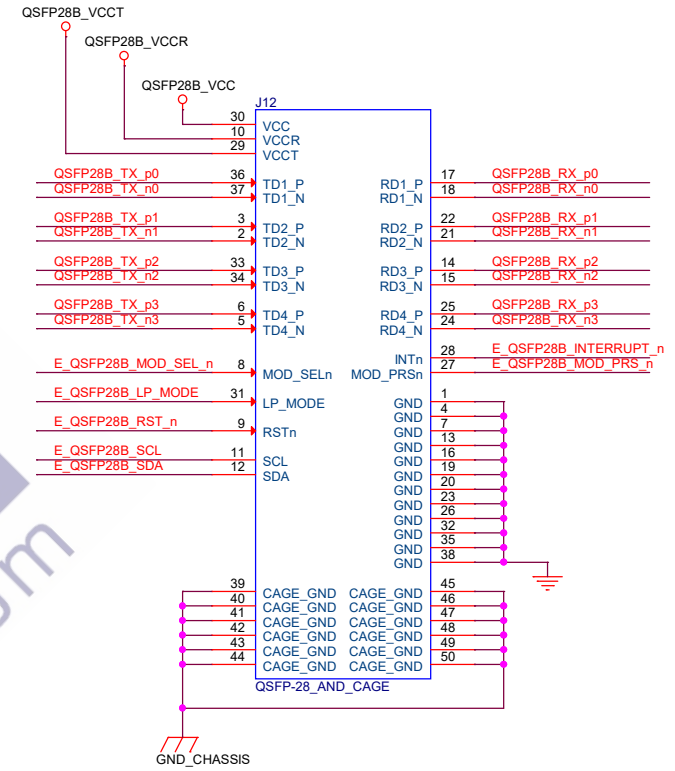
QSFP28B Control Interface

QSFP28B_MOD_SEL_n_14
 QSFP28B_RST_n_14
 QSFP28B_SCL_14
 QSFP28B_SDA_14
 QSFP28B_LP_MODE_14
 QSFP28B_INTERRUPT_n_14
 QSFP28B_MOD_PRS_n_14

NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.
 NOTE 2: Assuming that the SFP RD 100-ohm termination on the Host Board FPGA device will be implemented via the on-chip termination circuit.
 NOTE 3: DC blocking capacitors are in the module for RX and TX.
 NOTE 4: 1uH inductors should have a DC Resistance of less than 0.1-ohm.

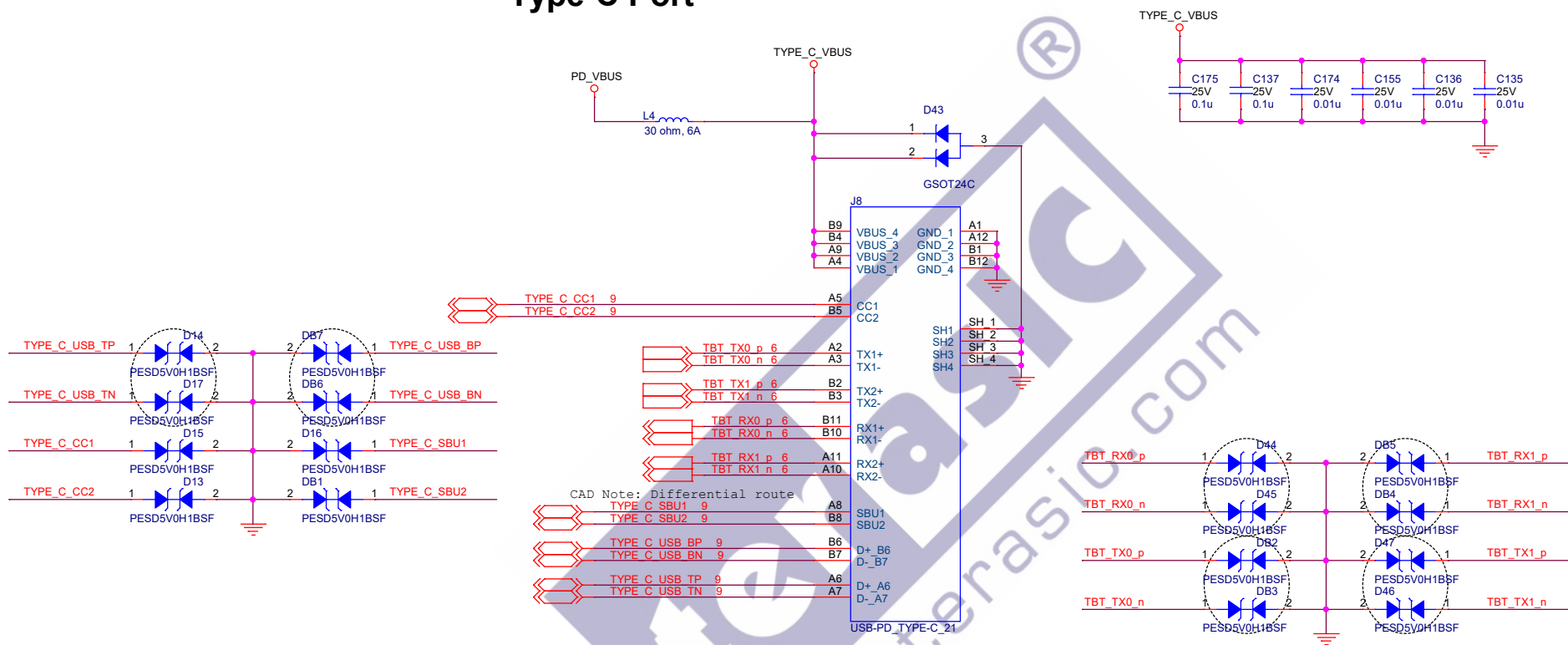


E_QSFP28B_MOD_SEL_n R209 4.7K
 E_QSFP28B_RST_n R210 4.7K
 E_QSFP28B_SCL R211 4.7K
 E_QSFP28B_SDA R213 4.7K
 E_QSFP28B_LP_MODE R214 4.7K
 E_QSFP28B_INTERRUPT_n R215 4.7K
 E_QSFP28B_MOD_PRS_n R218 4.7K

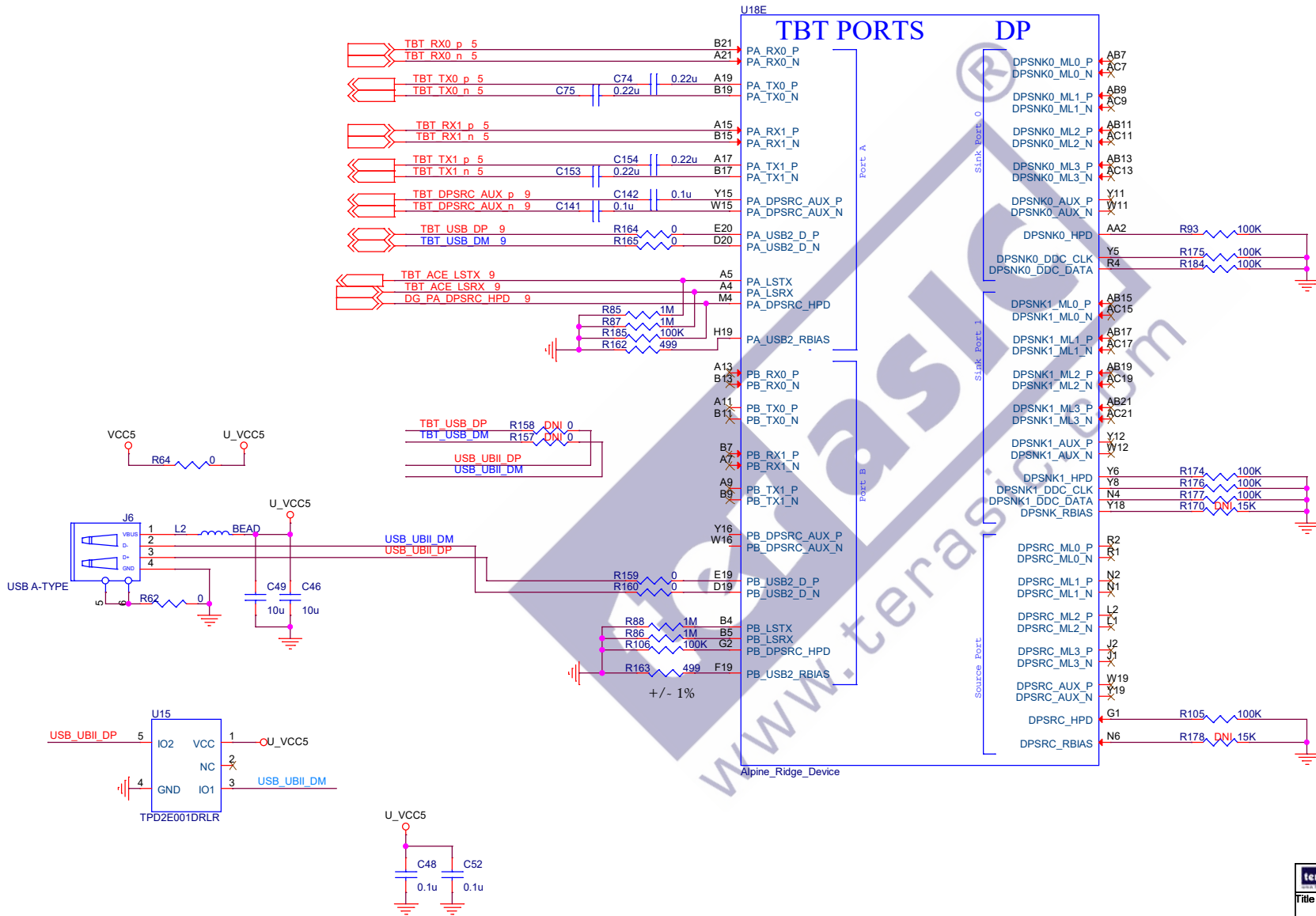


QSFP_CONNECTOR2

Type-C Port

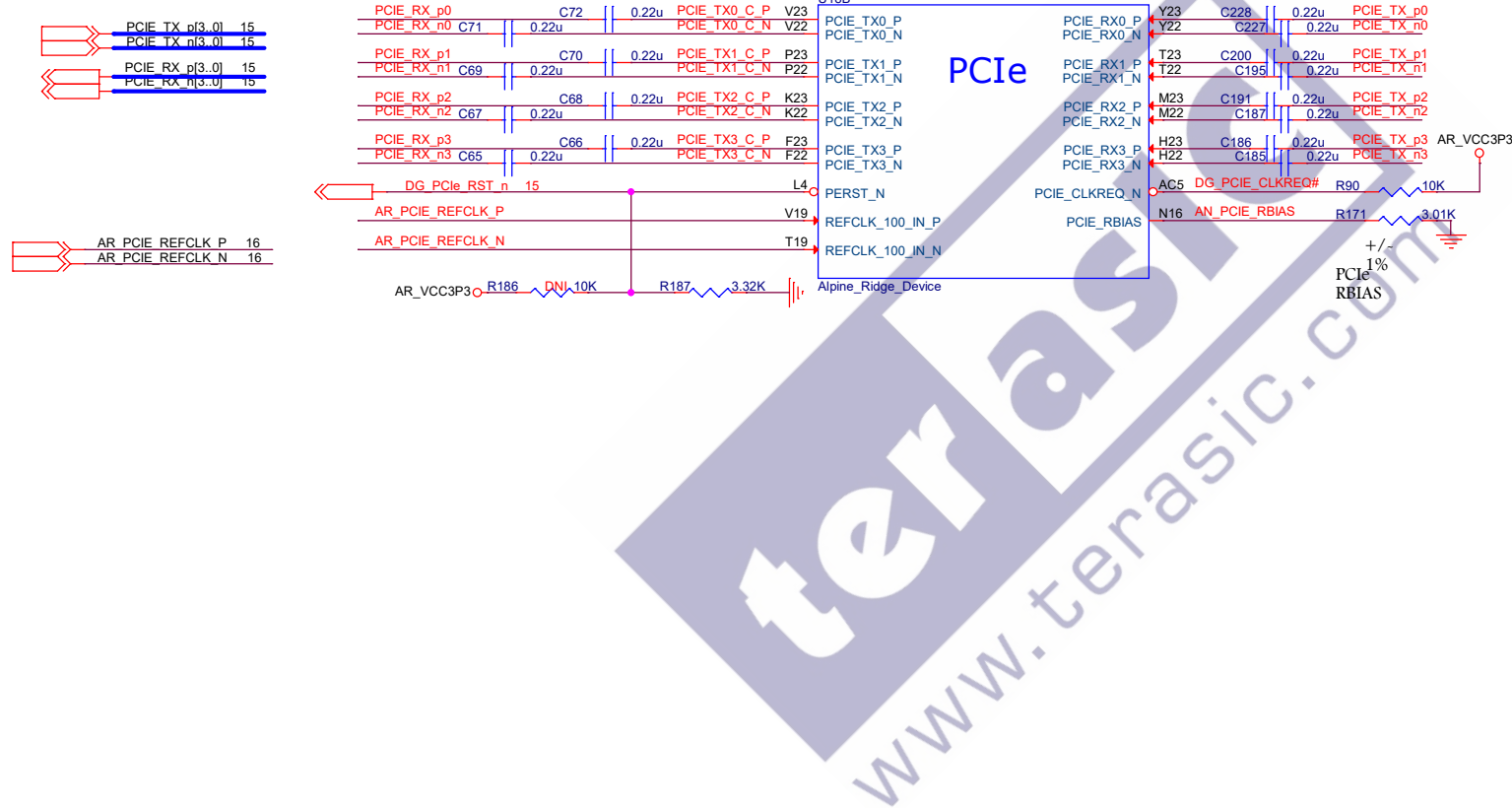


Alpine Ridge 4C - TBT, USB2

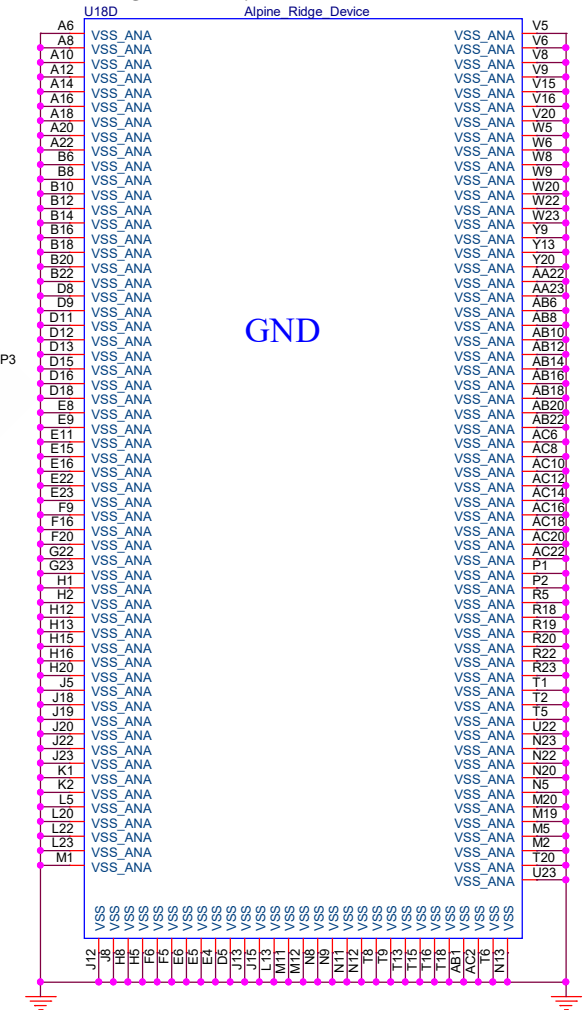


Alpine Ridge 4C - PCIe & GND

PCle Transceiver (FPGA side view)

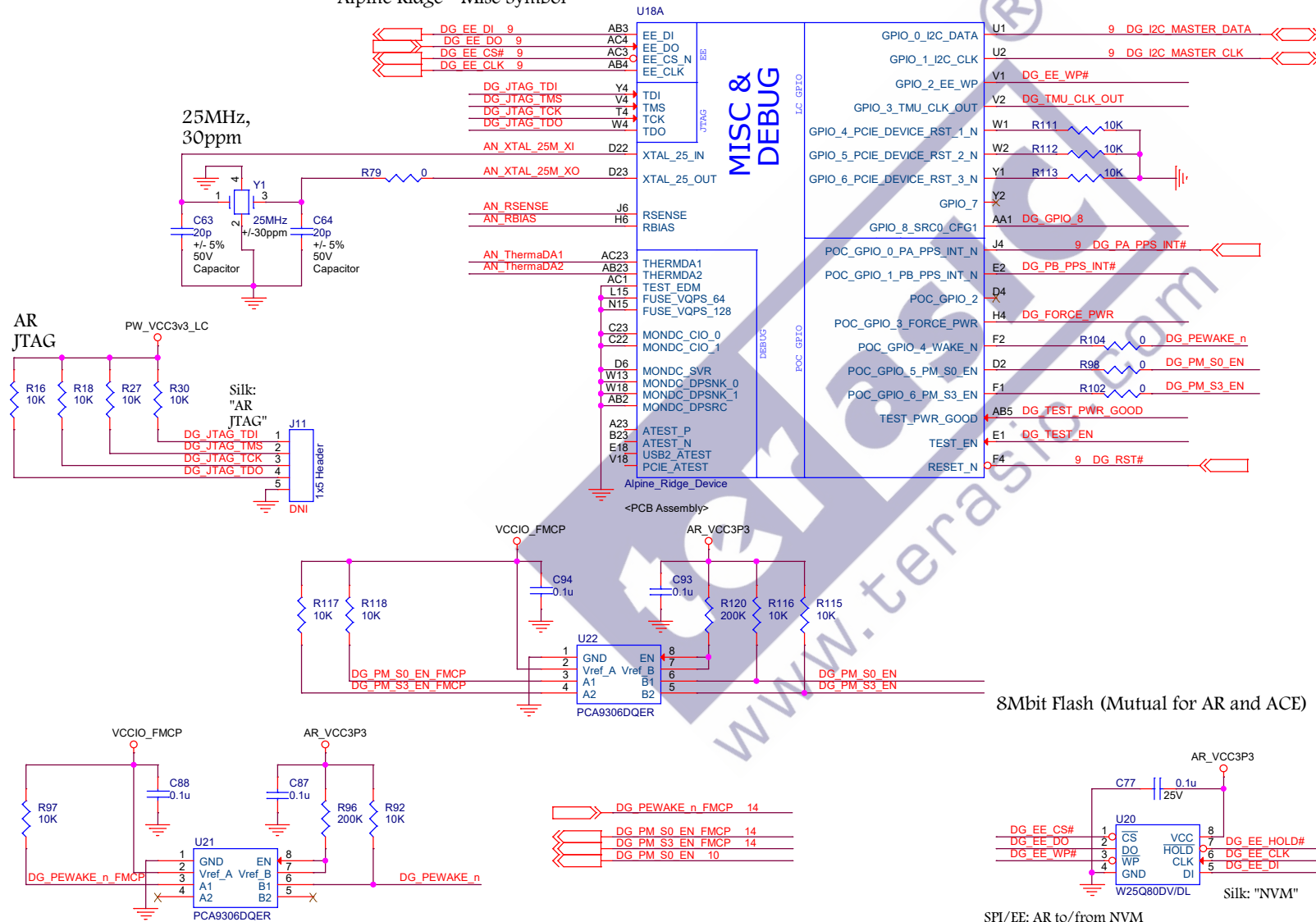


Alpine Ridge ~ GND Symbol

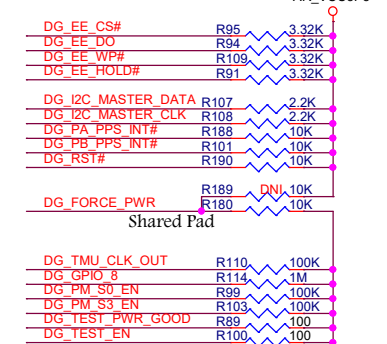


AR - MISC

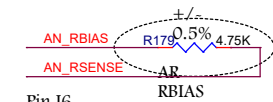
Alpine Ridge - Misc Symbol



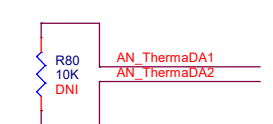
HW Pull-Up/Pull-Down



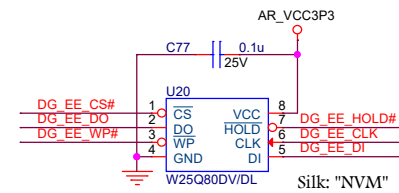
Pin H6



Pin J6



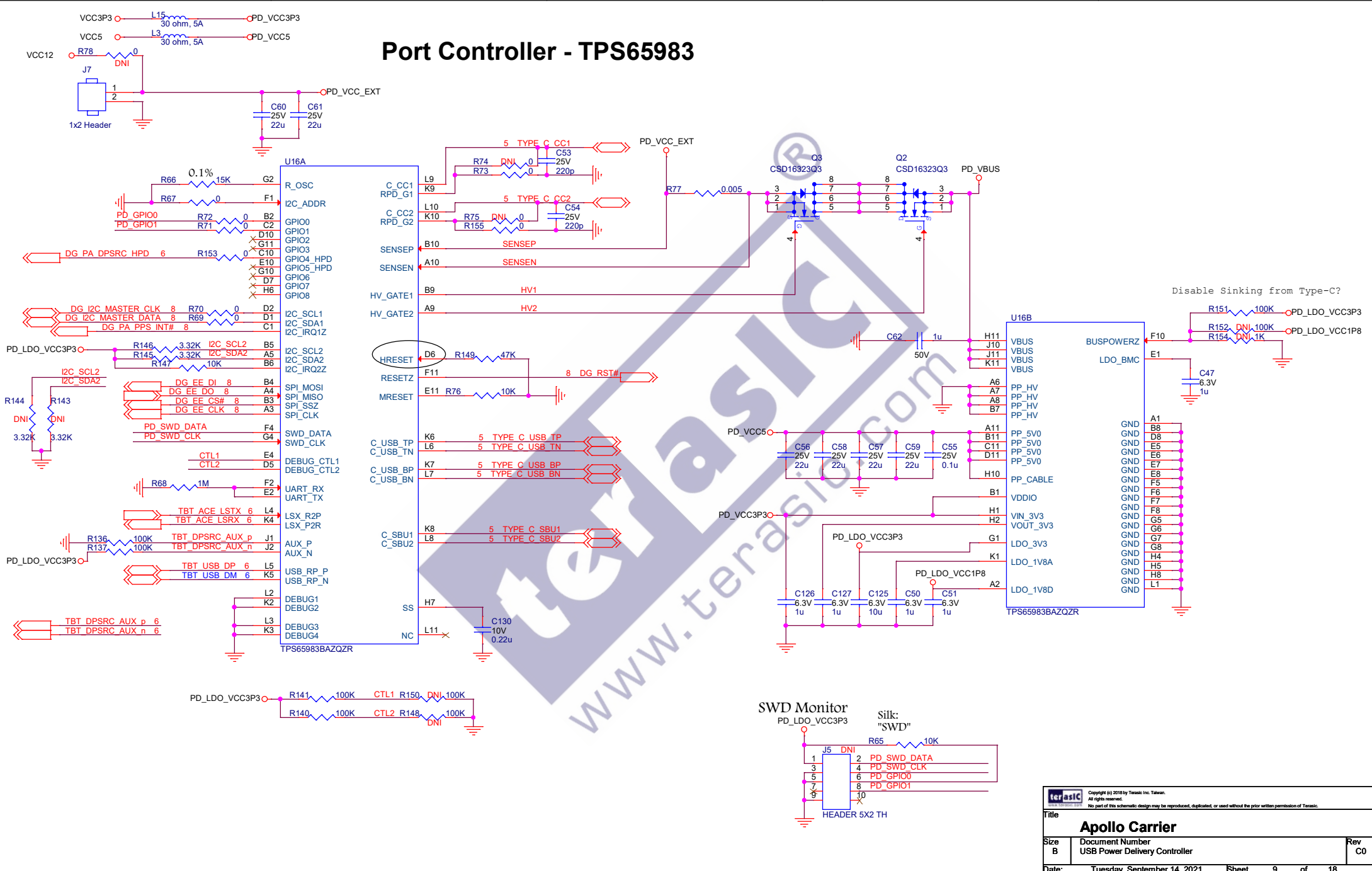
8Mbit Flash (Mutual for AR and ACE)



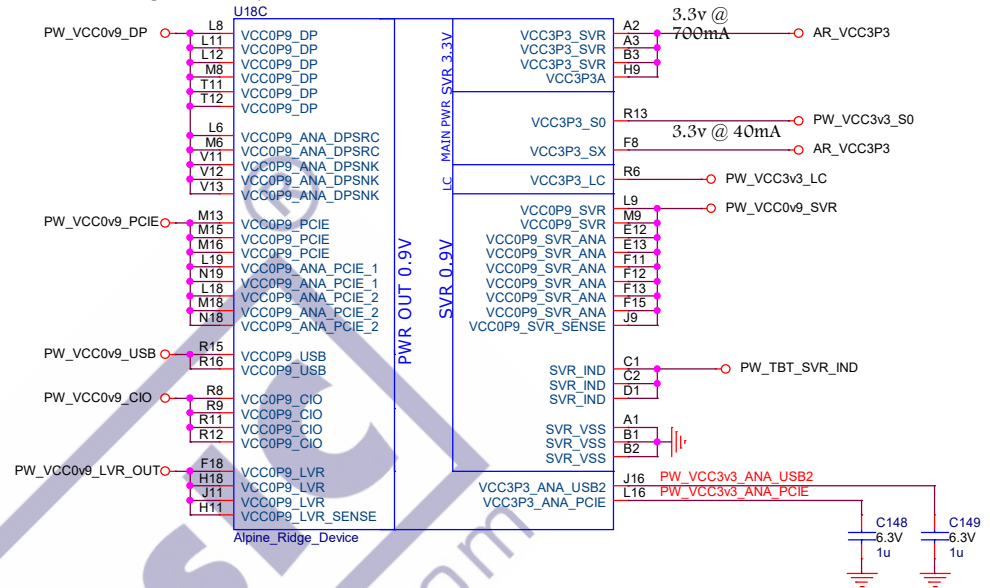
SPI/EE: AR to/from NVM & ACE

Apollo Carrier		
Size B	Document Number AR - MISC	Rev C0
Date:	Tuesday, September 14, 2021	Sheet 8 of 18

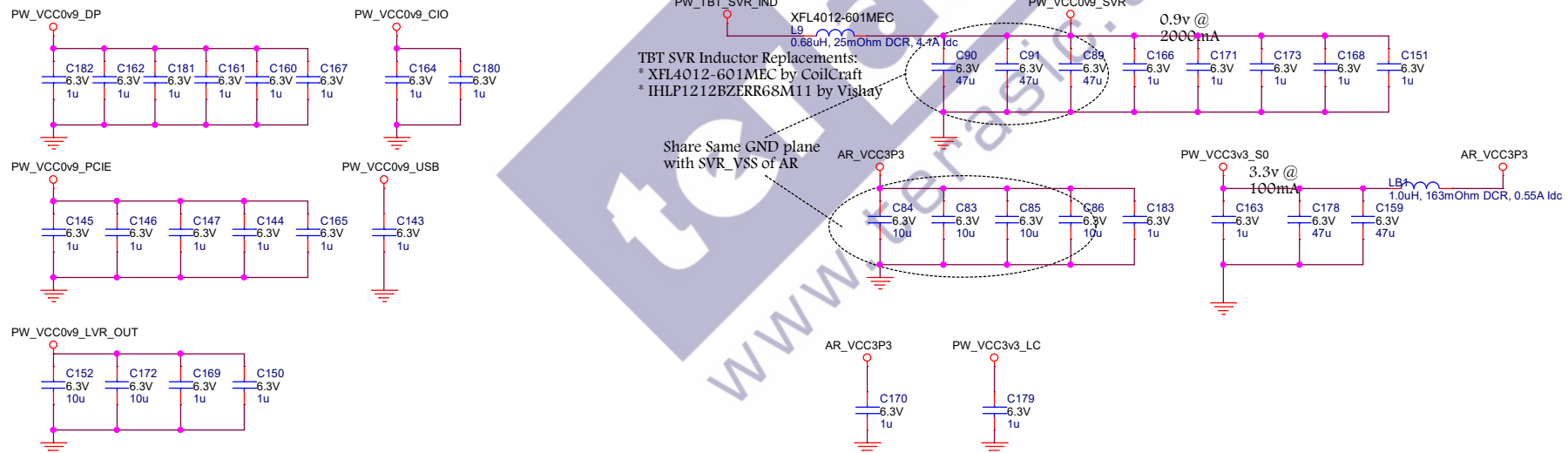
Port Controller - TPS65983

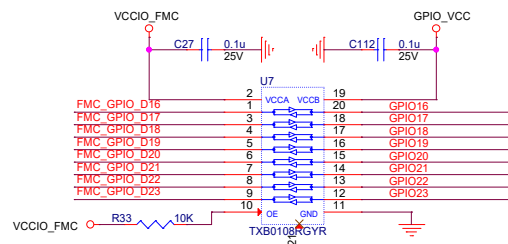
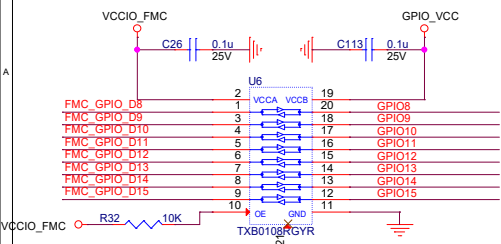
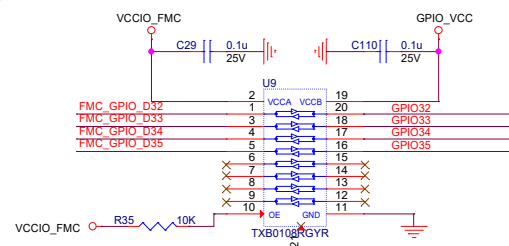
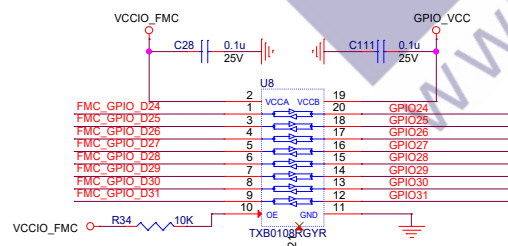
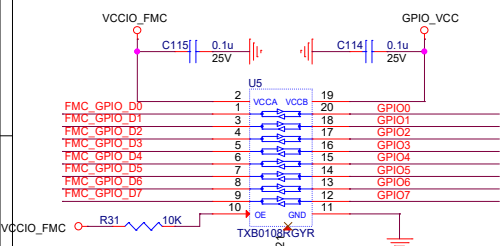
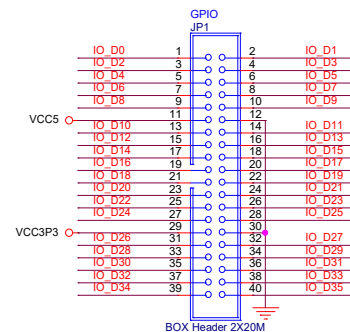
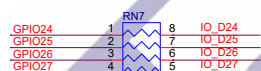
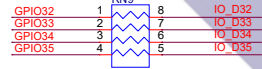
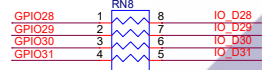
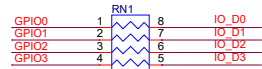
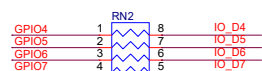
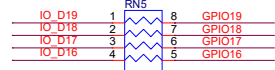
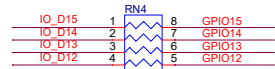
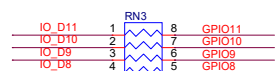
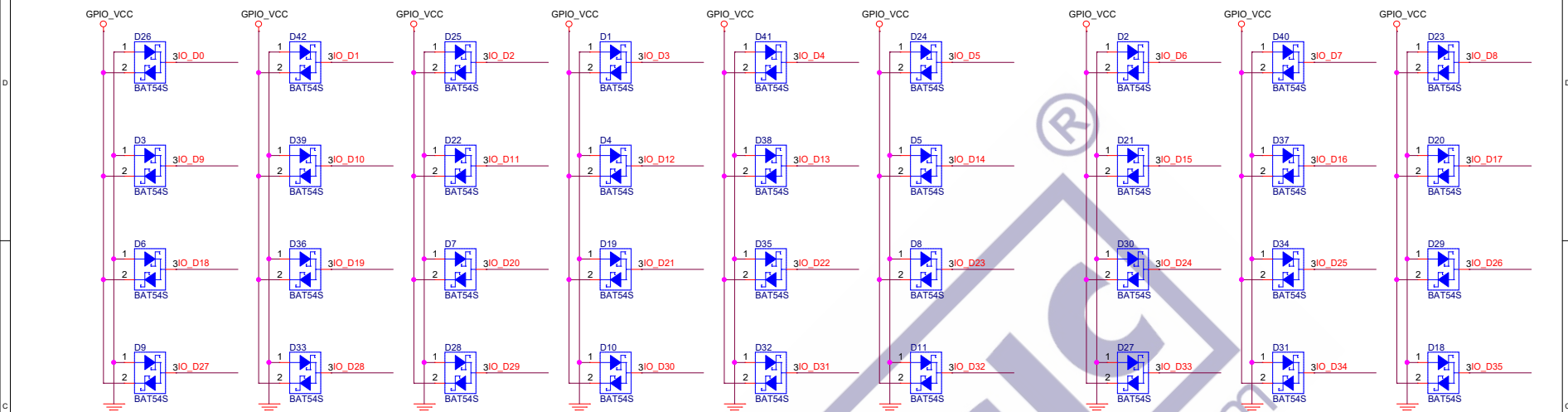


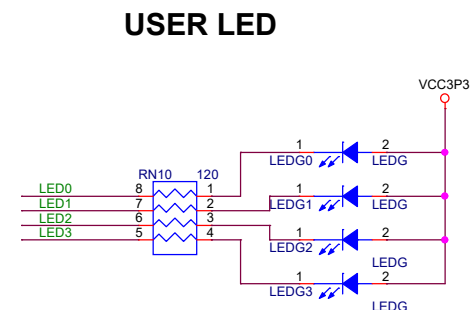
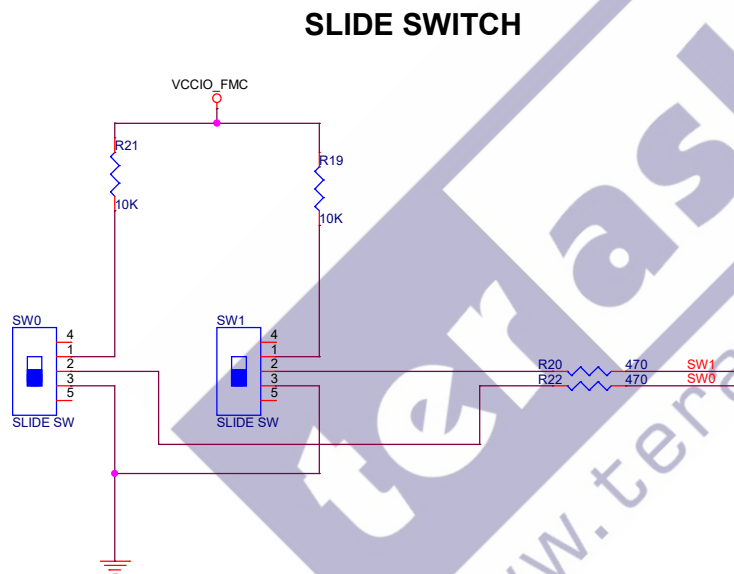
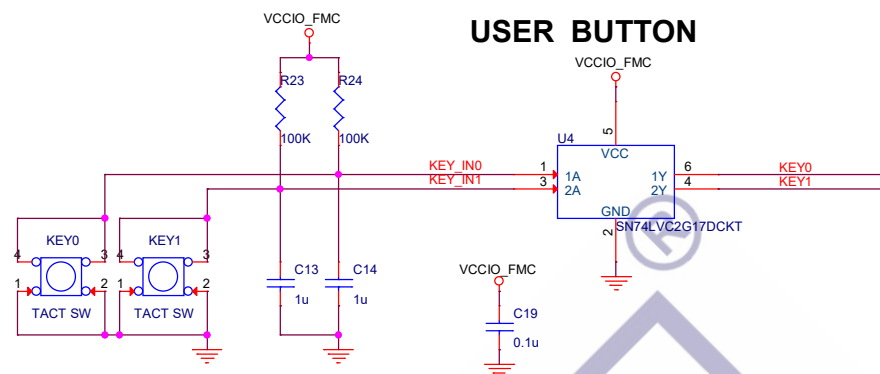
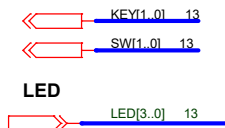
Alpine Ridge ~ VCC Symbol



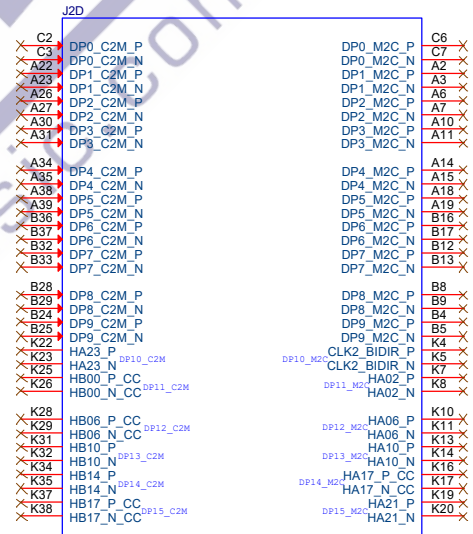
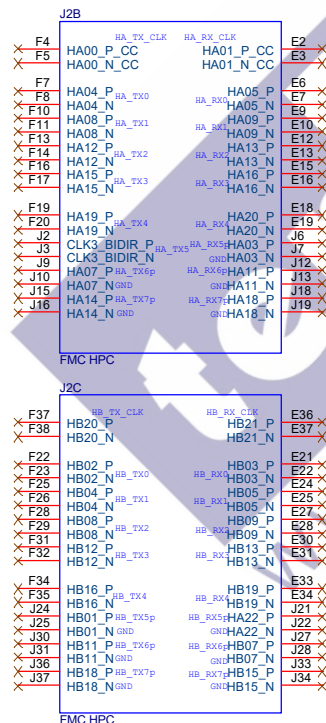
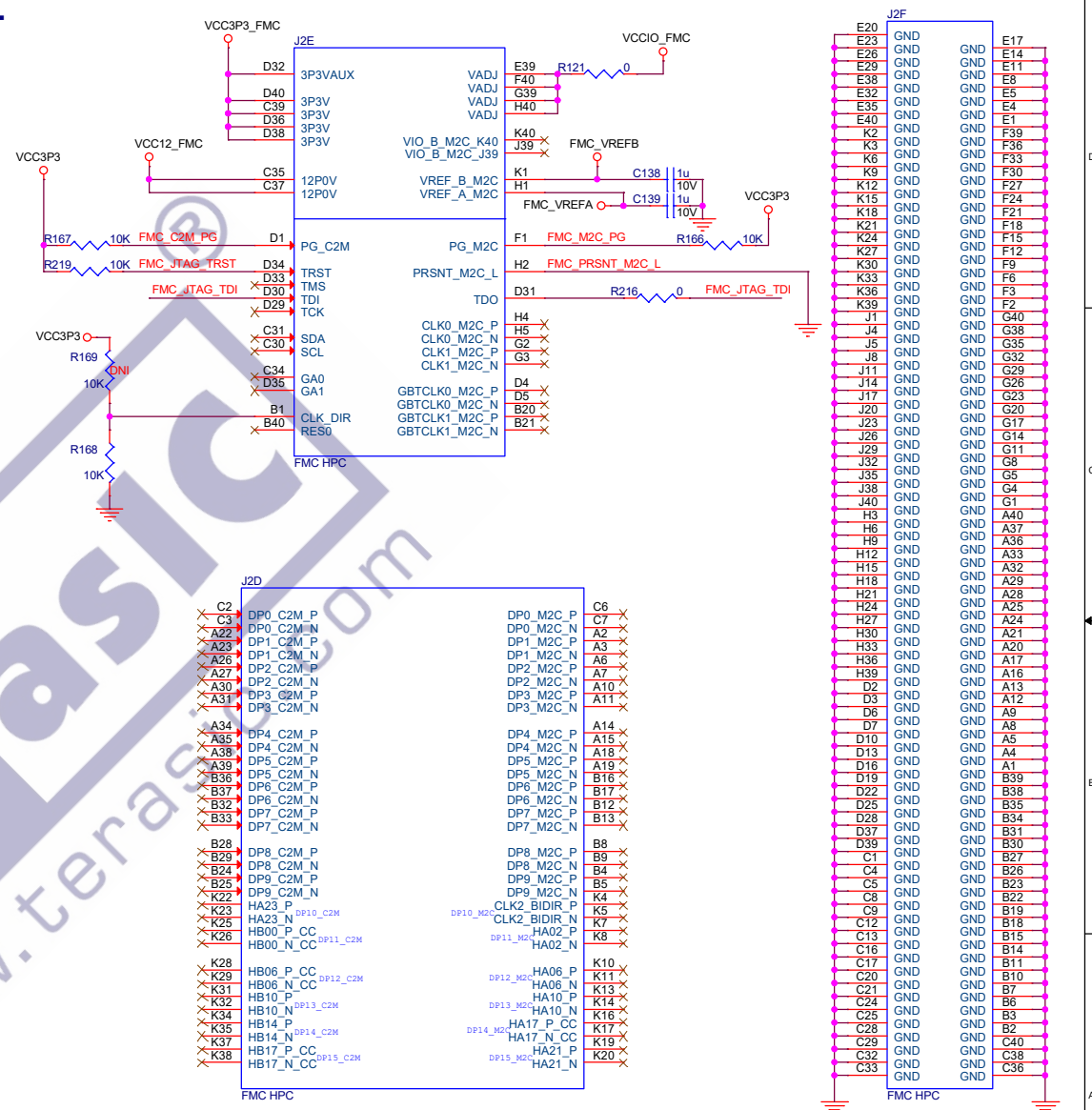
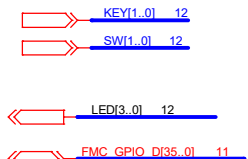
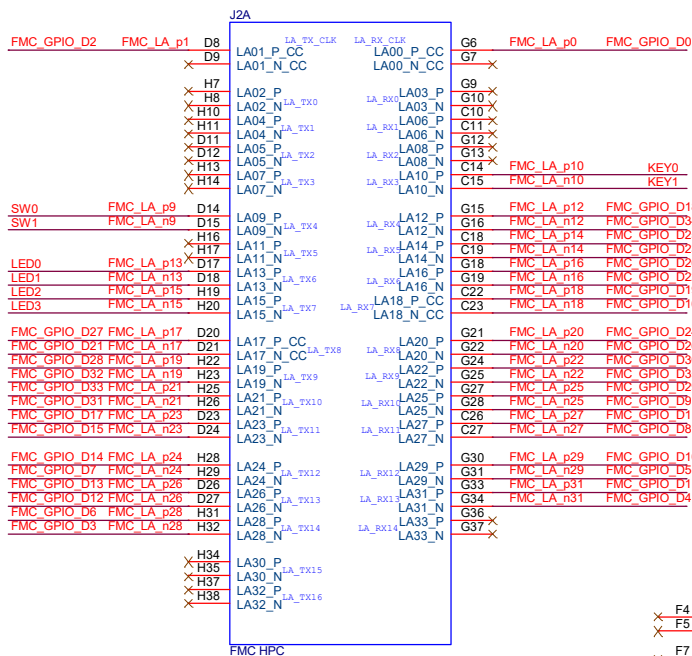
<PCB Assembly>







FMC PORT



FMC+ 1

HDMI TX HPD 17
HDMI TX CEC 17

DG PM S0 EN FMCP 8
DG PM S3 EN FMCP 8
DG PEWAKE n FMCP 8

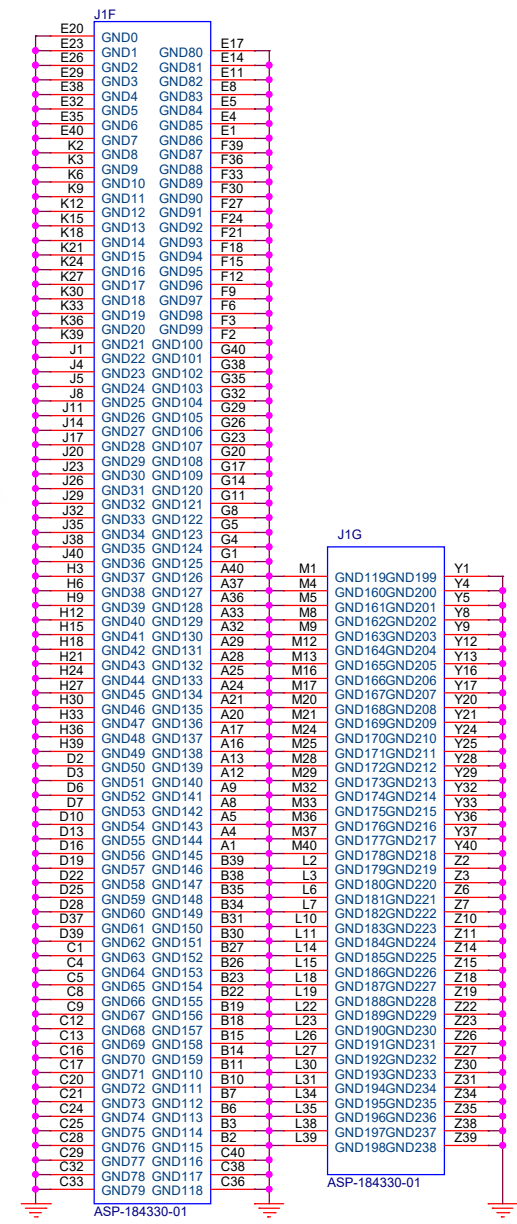
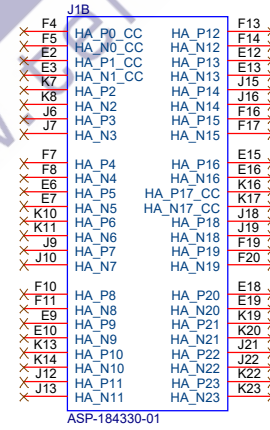
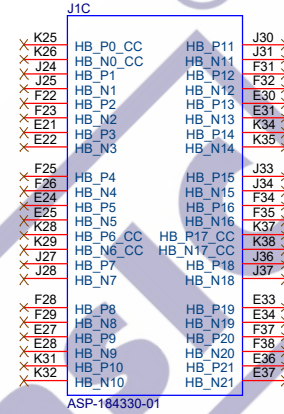
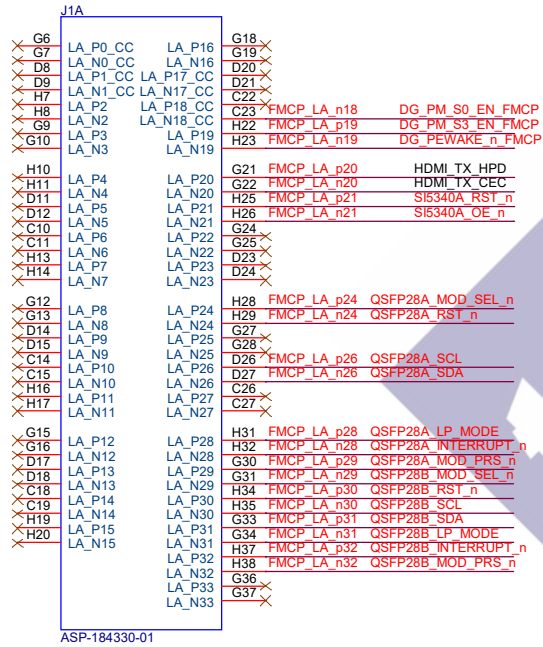
SI5340A RST n 16
SI5340A OE n 16

QSFP28A Control Interface

QSFP28A MOD_SEL n 3
QSFP28A RST n 3
QSFP28A SCL 3
QSFP28A SDA 3
QSFP28A LP_MODE 3
QSFP28A INTERRUPT n 3
QSFP28A MOD_PRS n 3

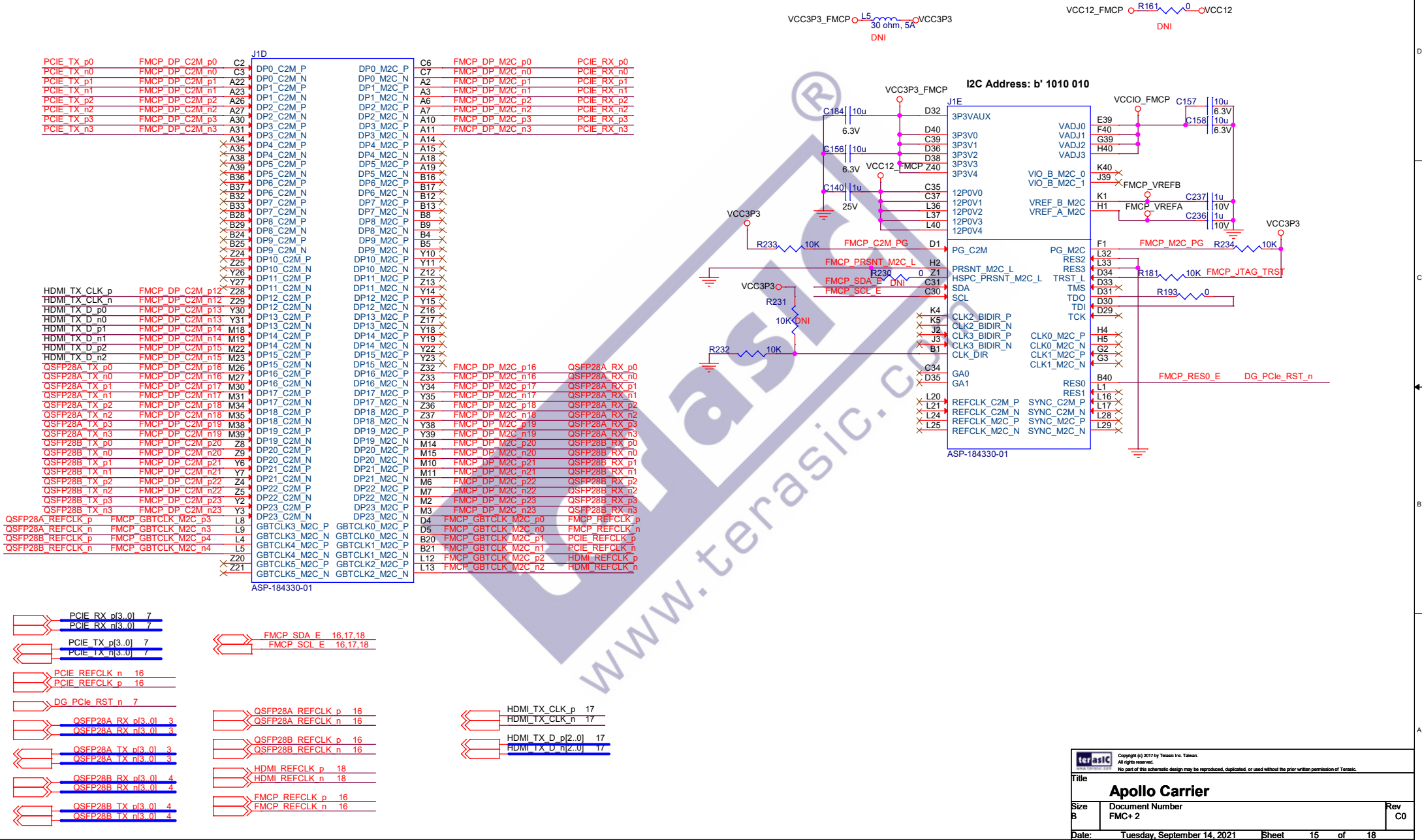
QSFP28B Control Interface

QSFP28B MOD_SEL n 4
QSFP28B RST n 4
QSFP28B SCL 4
QSFP28B SDA 4
QSFP28B LP_MODE 4
QSFP28B INTERRUPT n 4
QSFP28B MOD_PRS n 4

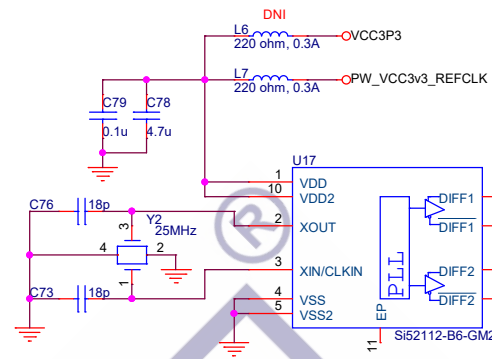
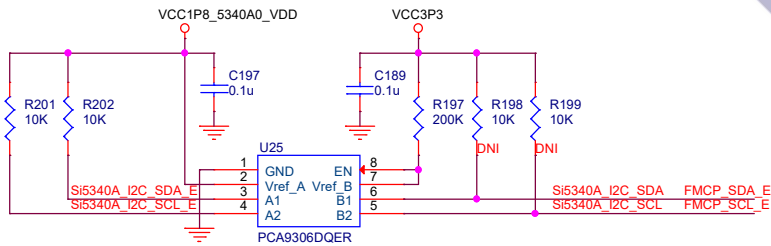
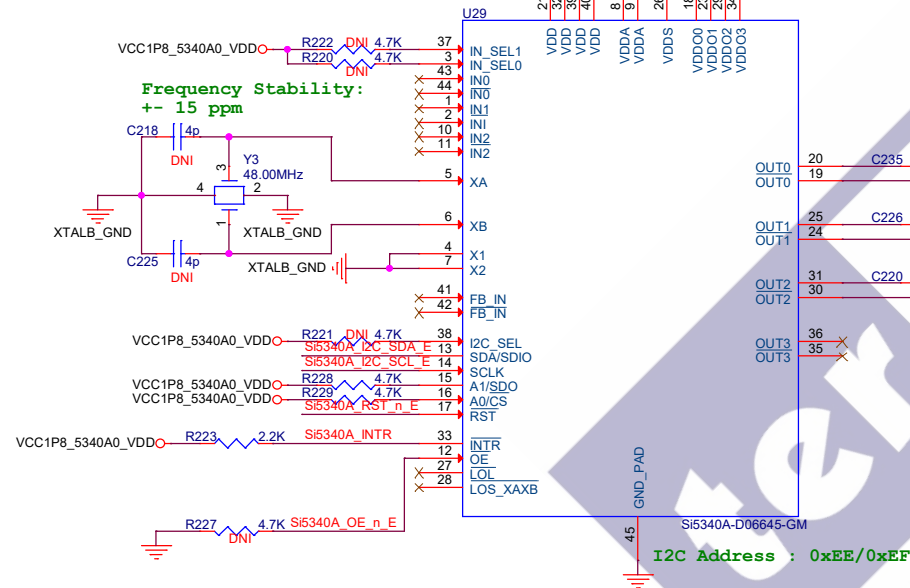


Title		
Apollo Carrier		
Size	Document Number	Rev
B	FMC+1	C0
Date:	Wednesday, September 15, 2021	Sheet 14 of 18

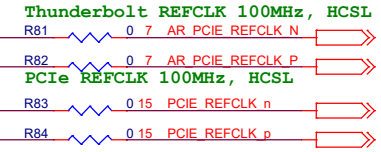
FMC+ 2



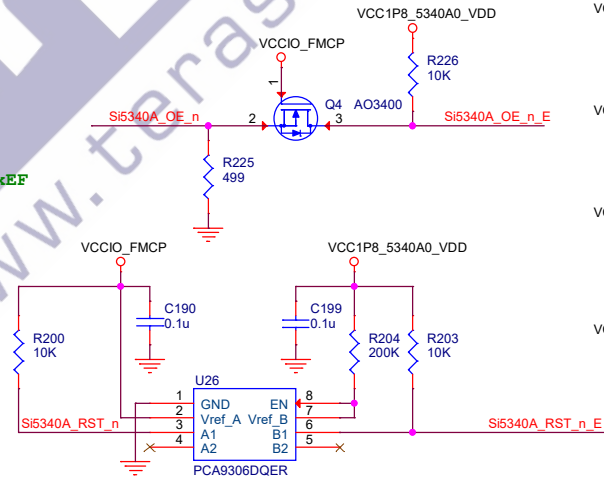
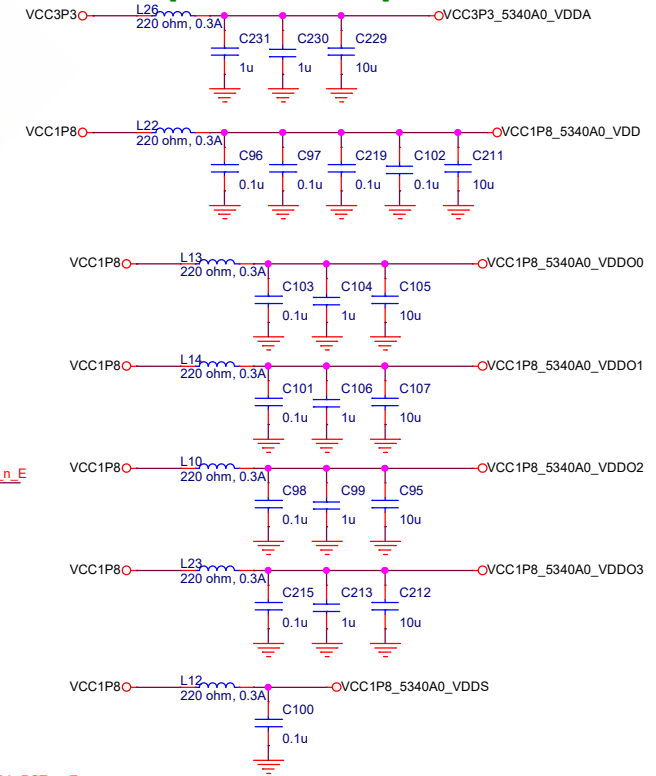
FMCP_SDA_E 15
FMCP_SCL_E 15
SI5340A_RST_n 14
SI5340A_OE_n 14



Outputs swap intentionally

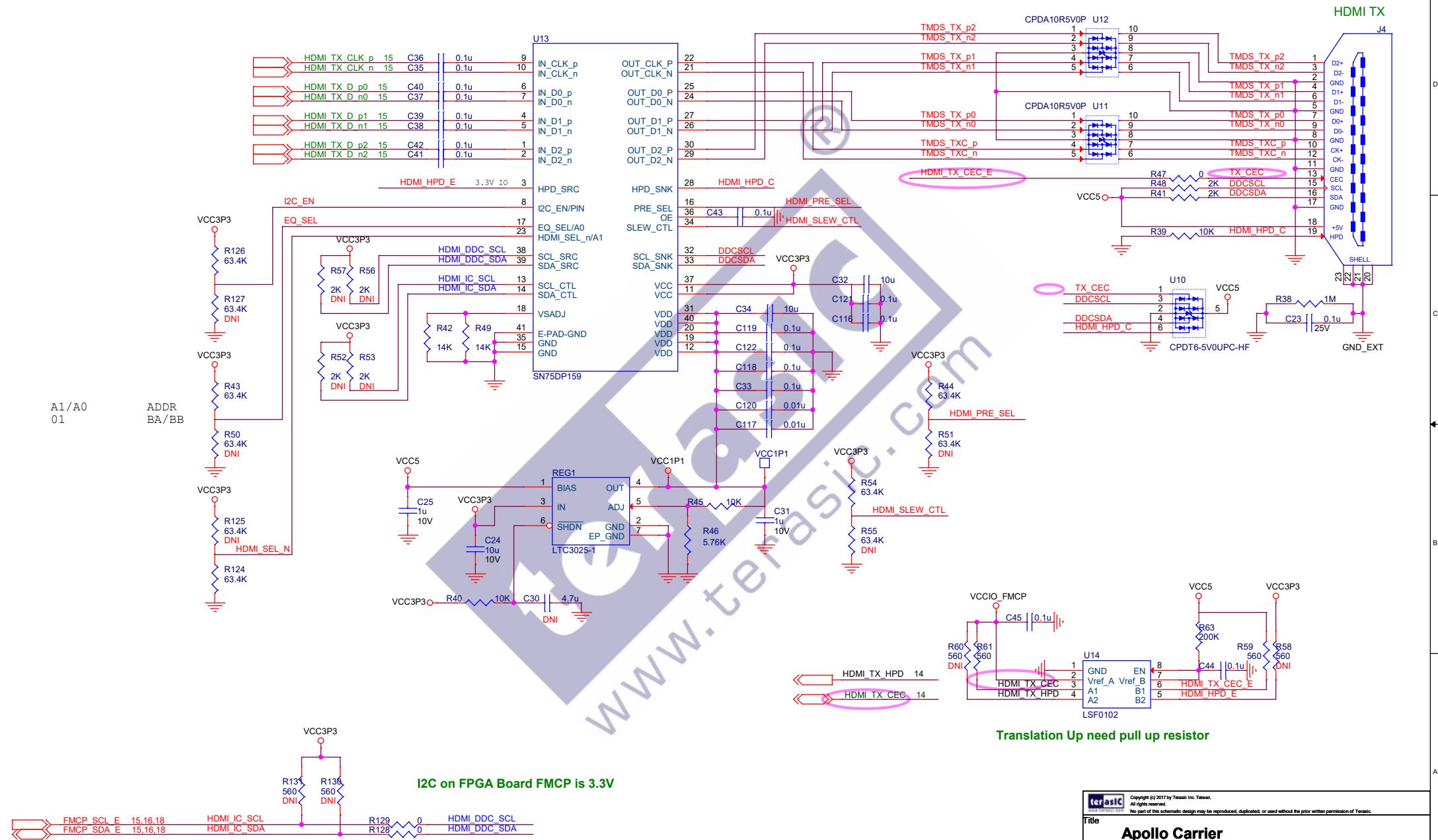


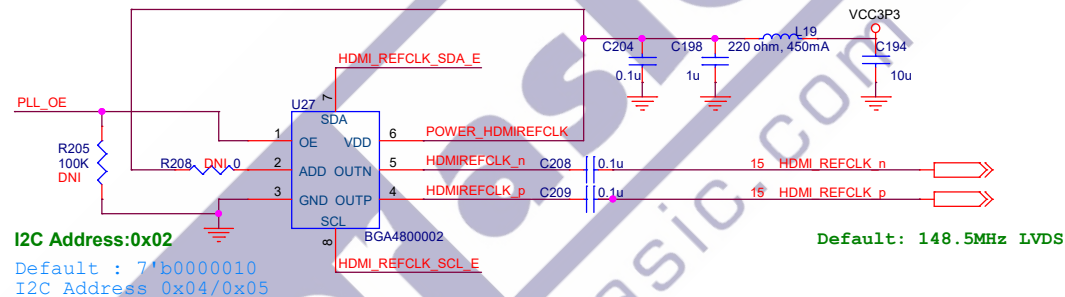
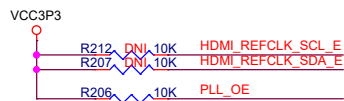
Place 0.1uF and 1uF caps as close as possible to device pins.




<div> <div>terasic</div> <div>Copyright (c) 2017 by Terasic Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.</div> </div>		
Title		
Apollo Carrier		
Size	Document Number	Rev
B	Clock	C0
Date:	Tuesday, September 14, 2021	Sheet 16 of 18

HDMI TX





		Copyright (c) 2017 by Terasic Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.	
Title			
Apollo Carrier			
Size	Document Number		Rev
B	HDMI-Clock		C0
Date:	Wednesday, September 15, 2021	Sheet	18 of 18