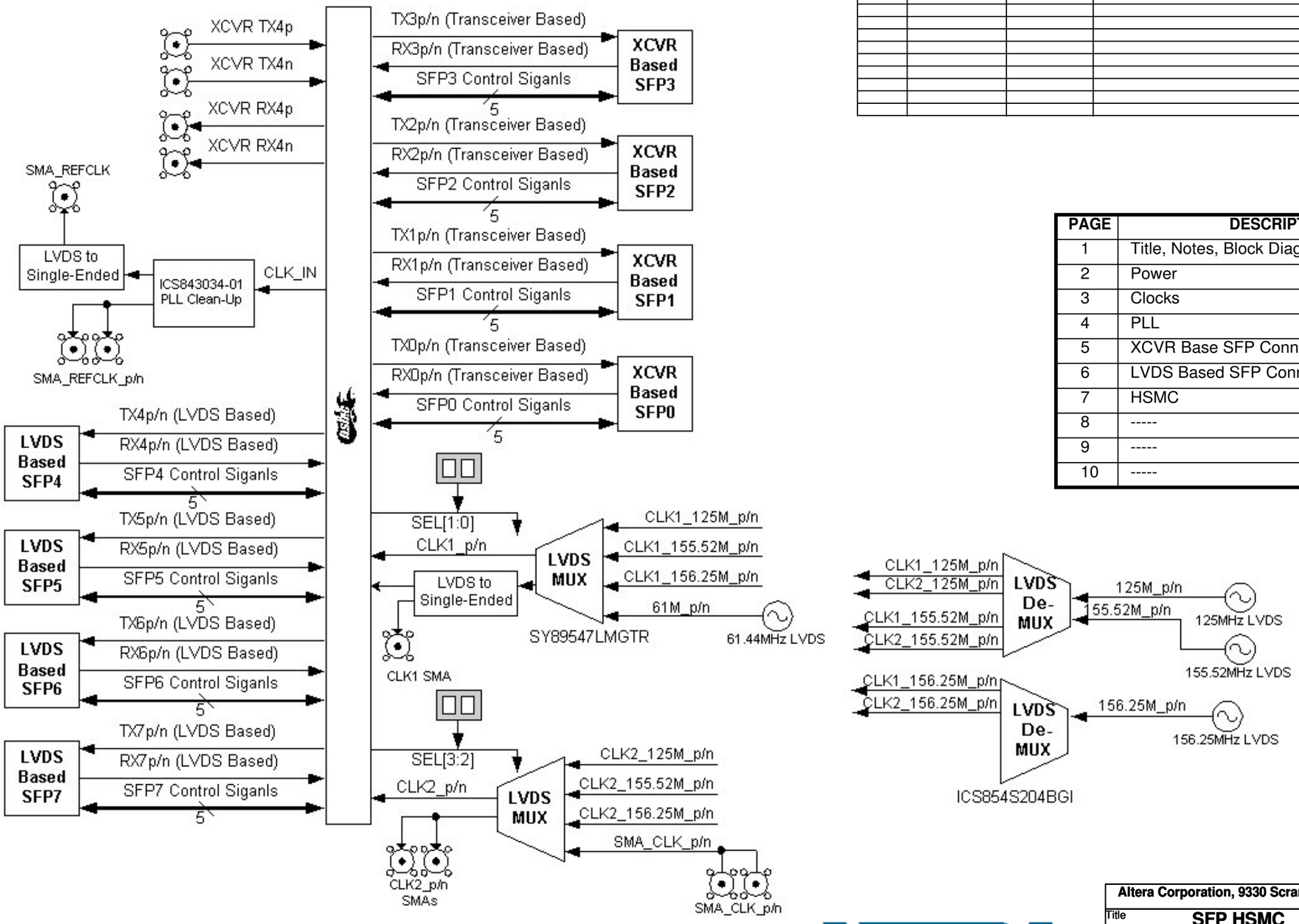
NOTES:

1. Project Drawing Numbers:

Raw PCB	100-0320611-B1
Gerber Files	110-0320611-B1
PCB Design Files	120-0320611-B1
Assembly Drawing	130-0320611-B1
Fab Drawing	140-0320611-B1
Schematic Drawing	150-0320611-B1
PCB Film	160-0320611-B1
Bill of Materials	170-0320611-B1
Schematic Design Files	180-0320611-B1
Functional Specification	210-0320611-B1
PCB Layout Guidelines	220-0320611-B1
Assembly Rework	320-0320611-B1

2. 318 Parts, 23 Library Parts, 220 Nets, 1336 Pins

Small Form-Factor Pluggable (SFP)
High Speed Mezzanine Card (HSMC)



REV	DATE	PAGES	DESCRIPTION
A	08/26/2008	All	Initial
B-0.1	11/19/2008	6-7	Add a resistor divider to create a 1.25V source to DC bias SFP[4:7]_RDp/n signals. Add standoffs and screws.
B-0.2	11/20/2008	6	Add 2 0.1uF capacitors to the 1.25V power.
B-0.3	11/21/2008	5-6	Change SFP connector (P1-P8) footprints from NULL to 20SFP_DUMMY. Change R126 from 100k to 100 and R134 from 61.4k to 61.4.
B-0.4	11/21/2008	5-6	Add dummy mounting holes to SFP connectors.
B1	11/21/2008	ALL	Ref Des renumber.
	12/11/2008	6-7	Change SFP RD pull-up resistors from 1.00k to 10k. Add 2 more screws and standoffs. Modify R51 & R52 values.

GND_SFP **Digital Ground Symbols**

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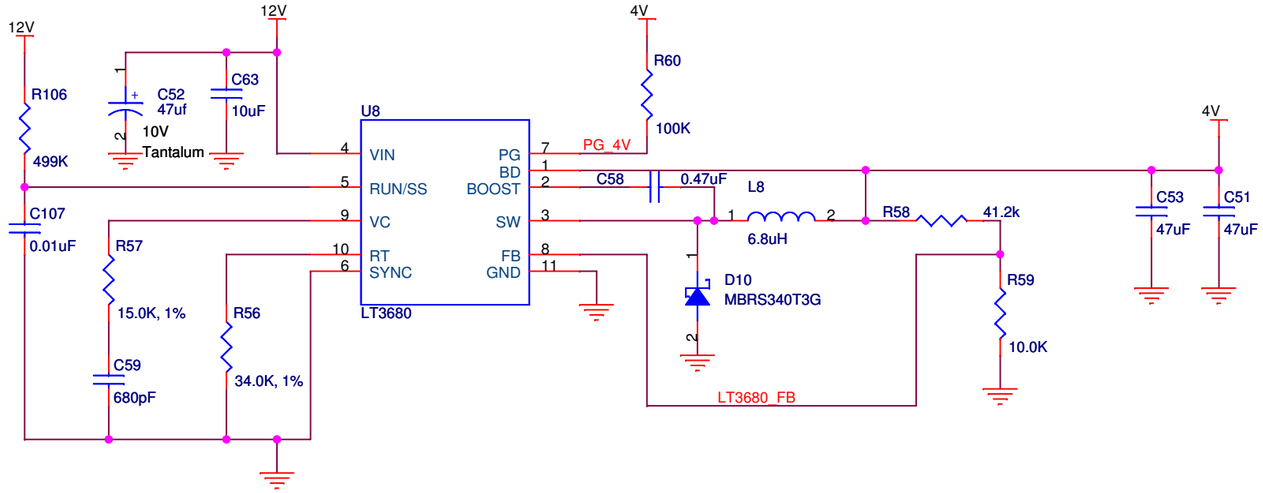
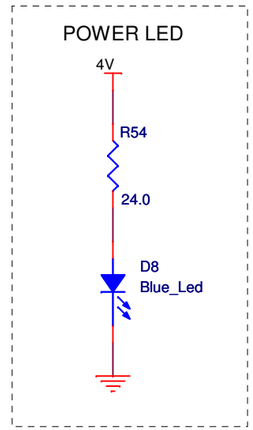
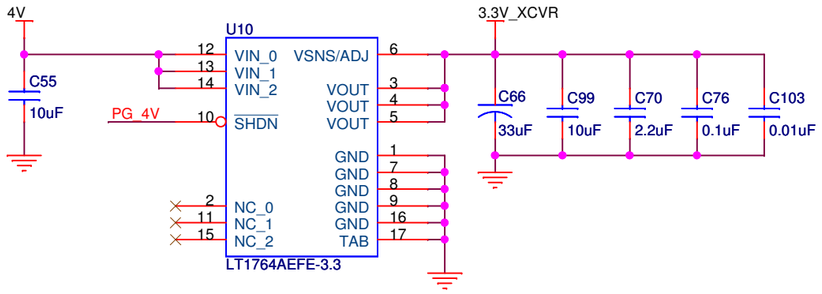
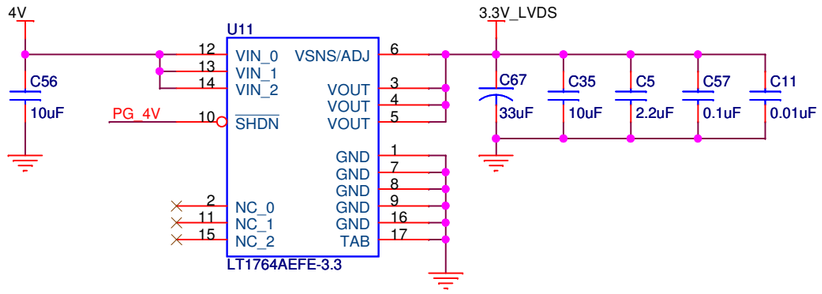
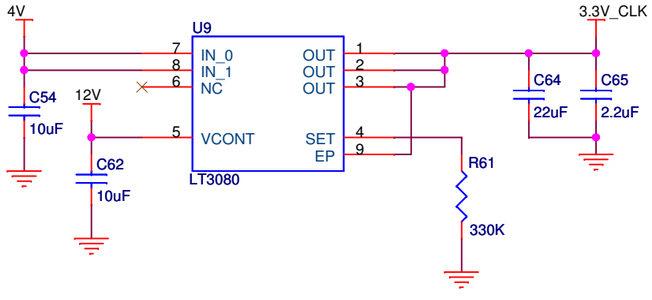
Power











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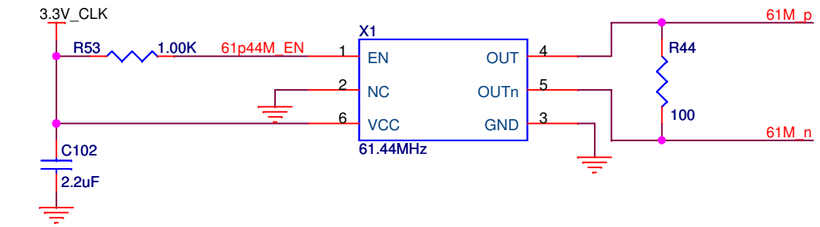
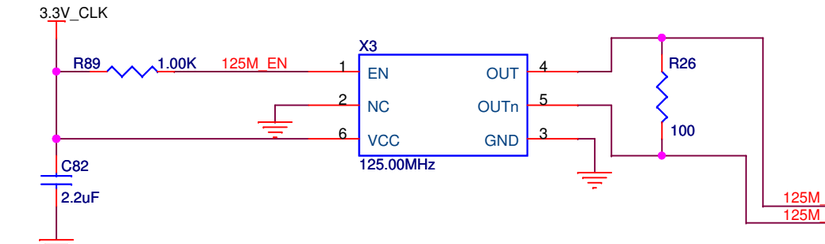
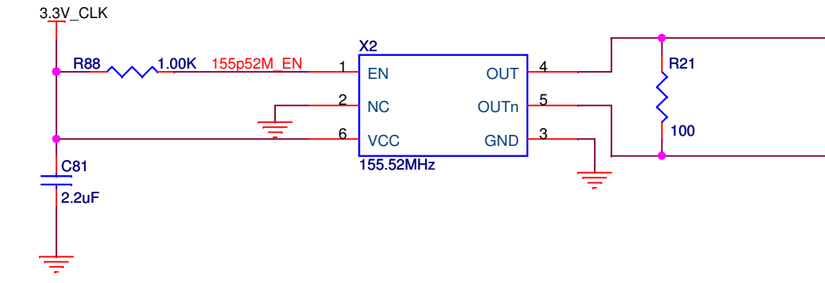
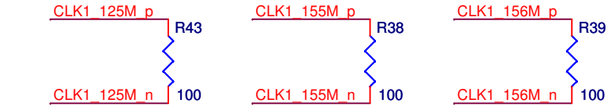
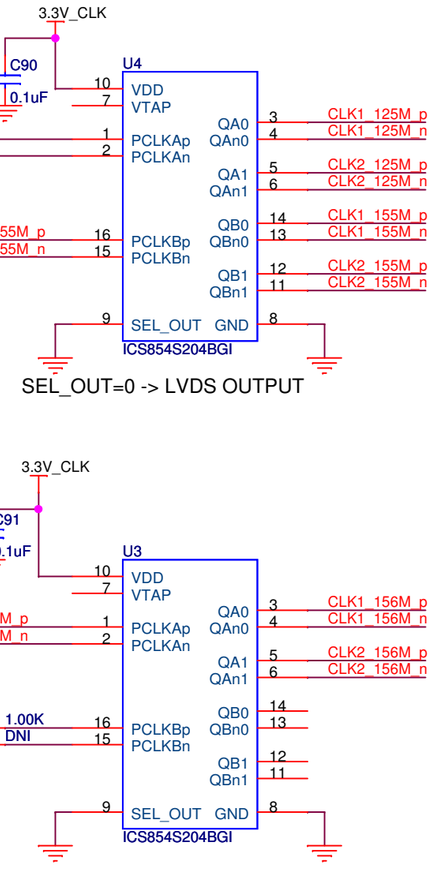
Clocks

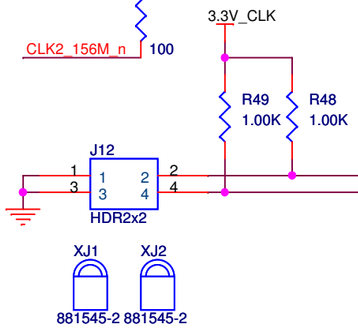


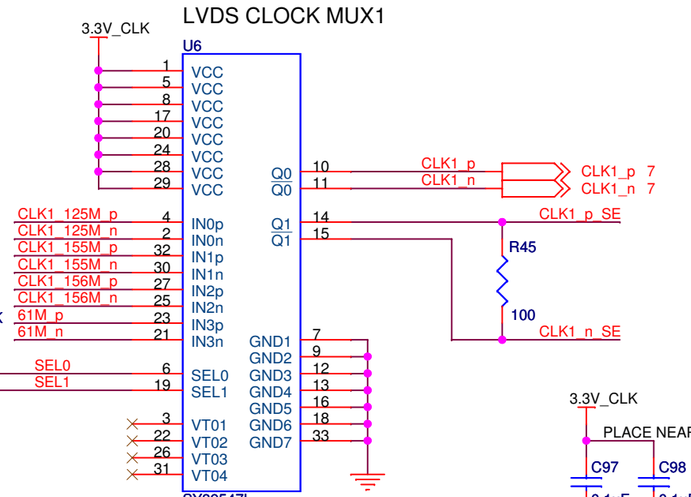


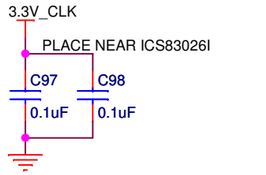


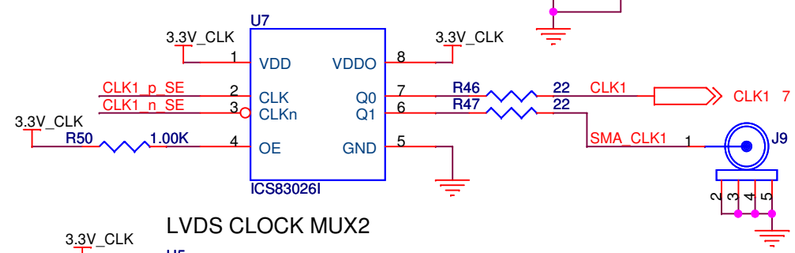


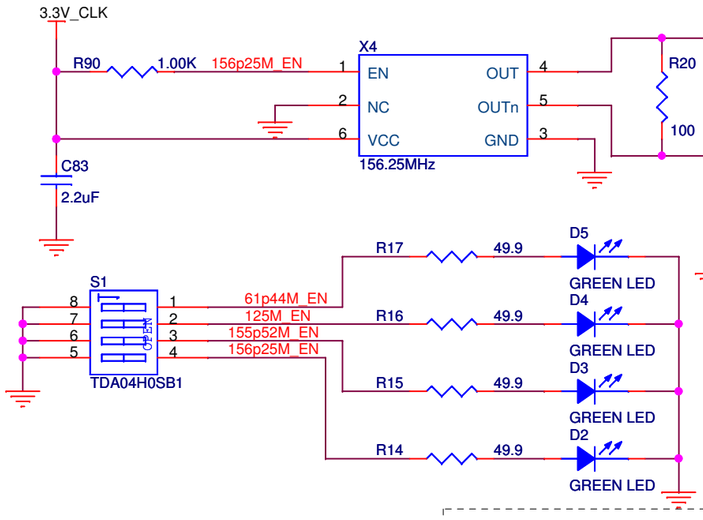


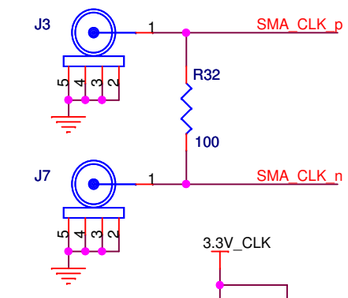


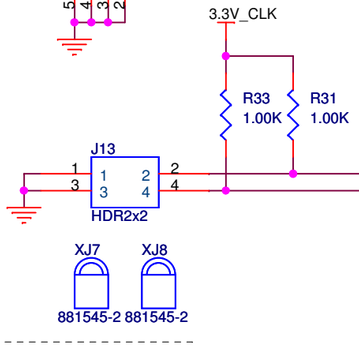


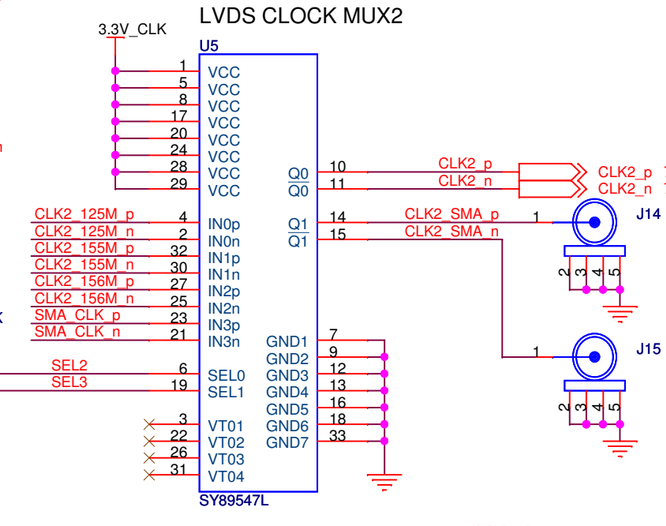


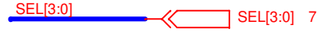


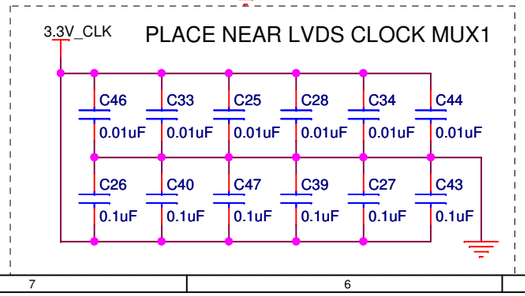


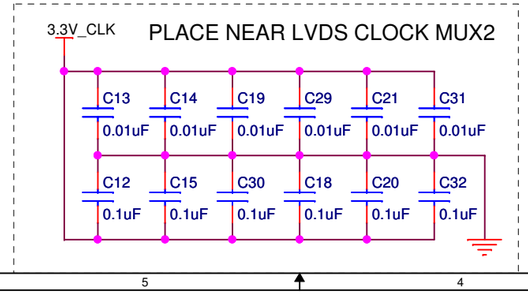












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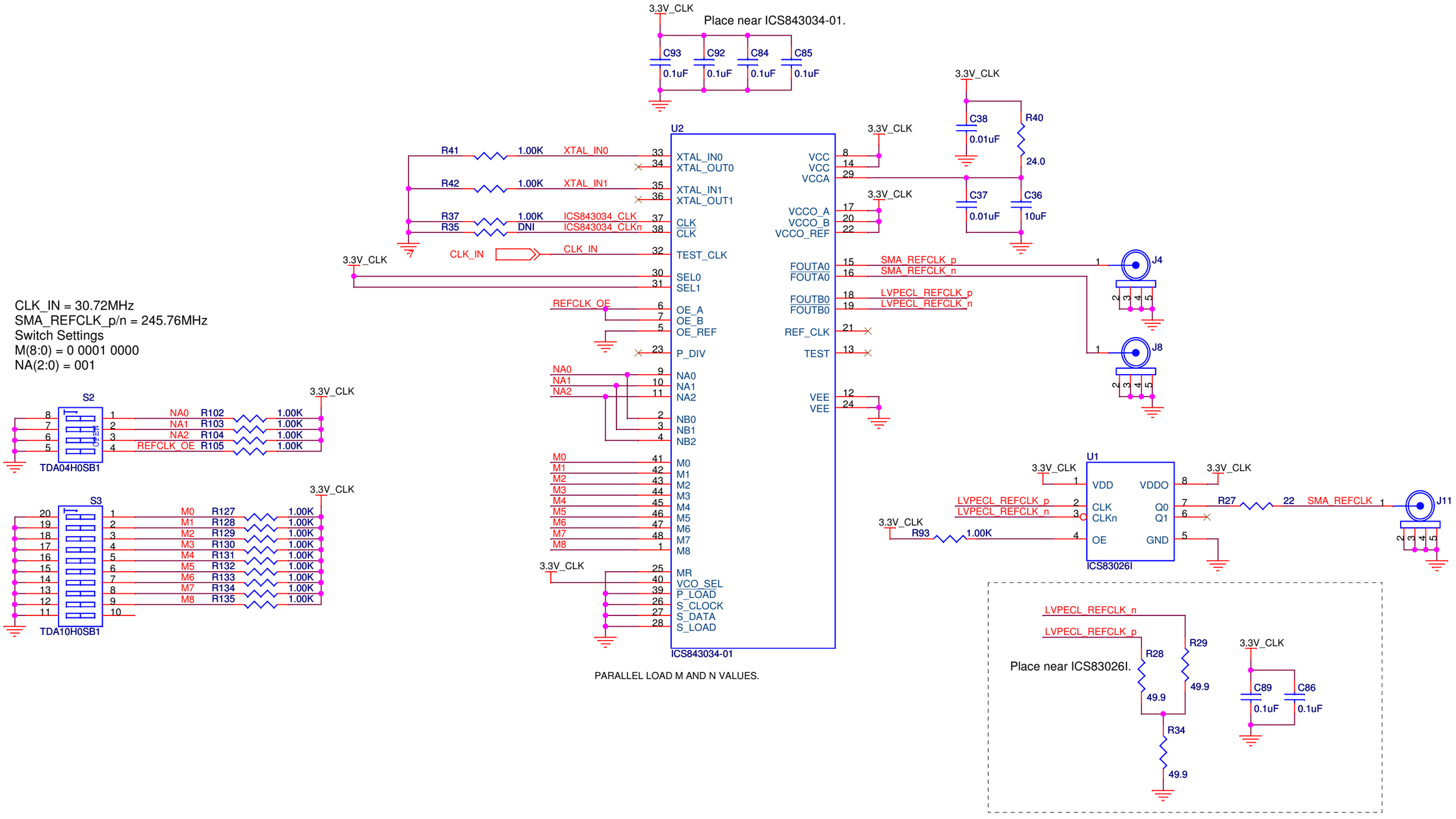
PLL



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Title: SFP HSMC		
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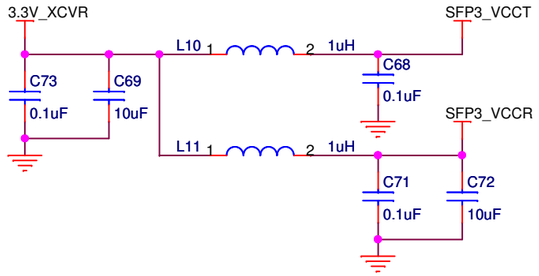
XCVR Based SFP Connectors

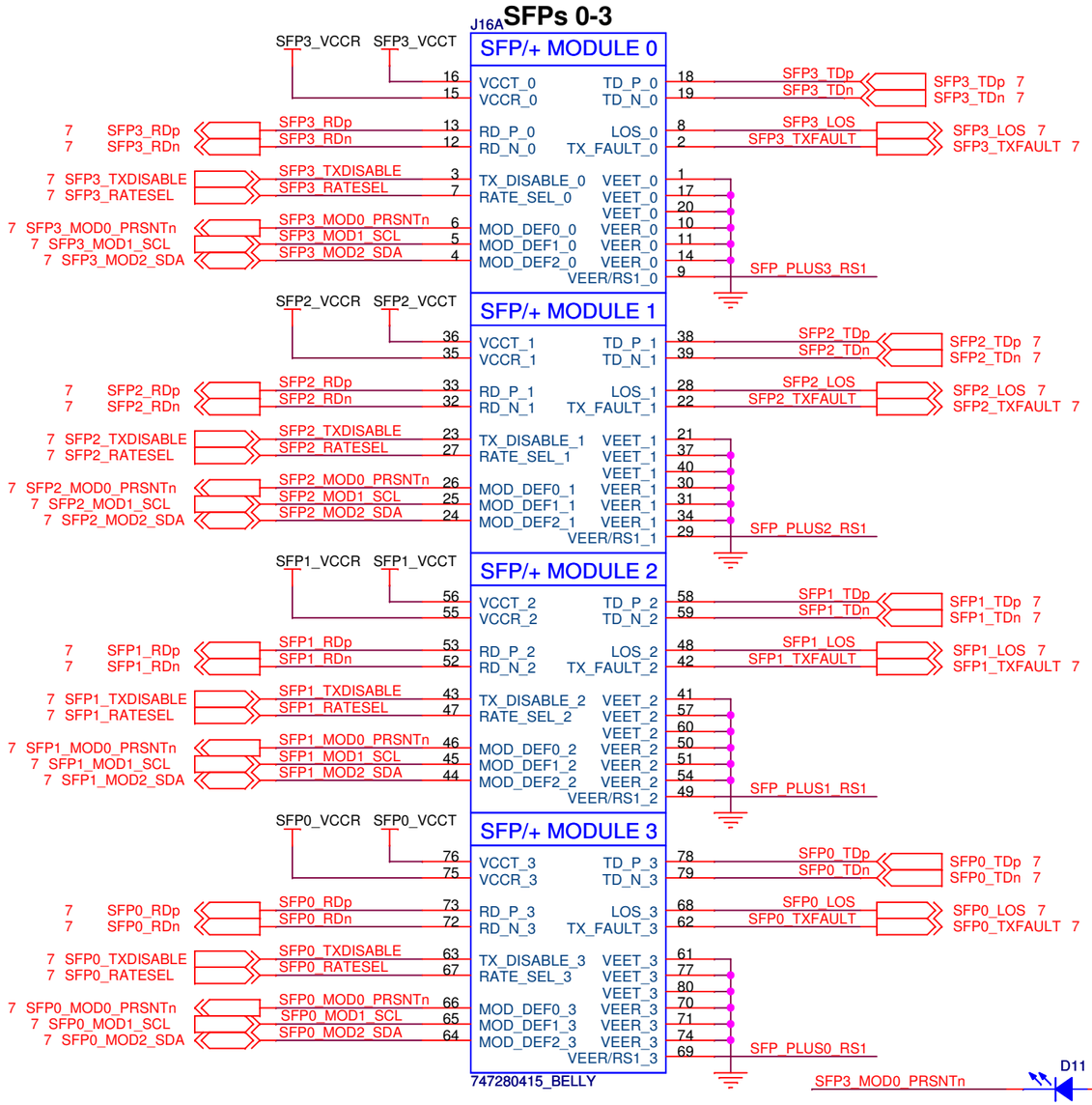
NOTE 1: 1uH ferrite bead should have a DC resistance of less than 1-ohm.

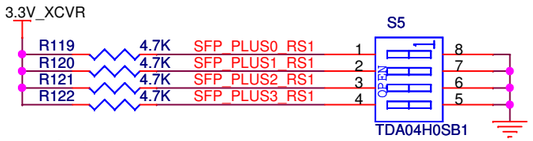
NOTE 2: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.

NOTE 3: Assuming that the SFP RD 100-ohm termination on the Host Board FPGA device will be implemented via the on-chip termination circuit.

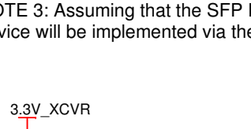
SFPs 0-3

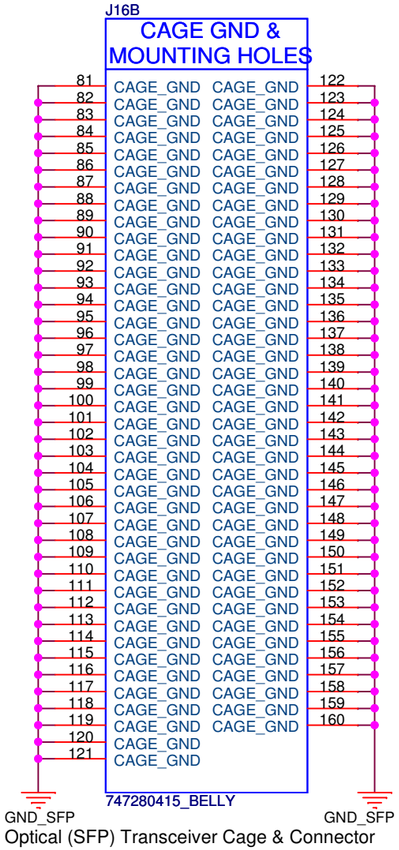




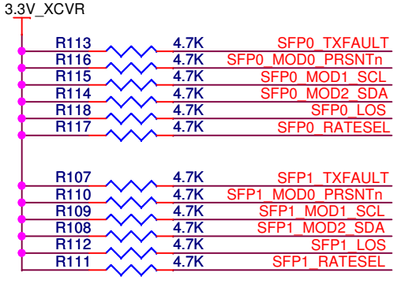


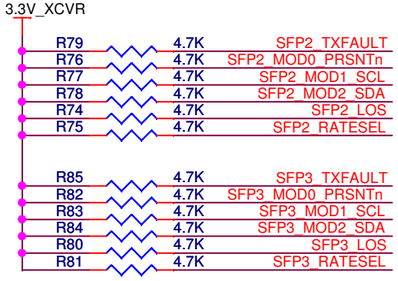
If using SFP this pin must be grounded.
If using SFP+:
0= TX datarates <= 4.25GB/s
1= TX datarates > 4.25GB/s

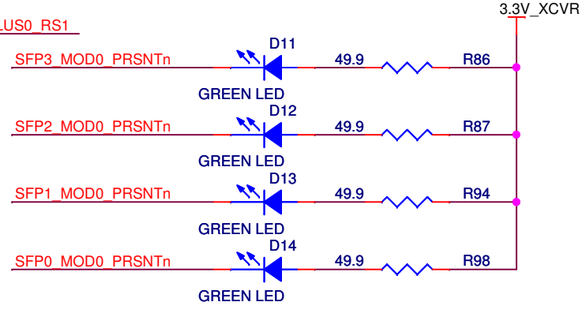




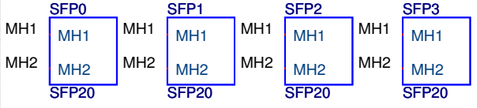
Optical (SFP) Transceiver Cage & Connector







SFP Modules - Signal Connections will be made in the schematic on the connectors.



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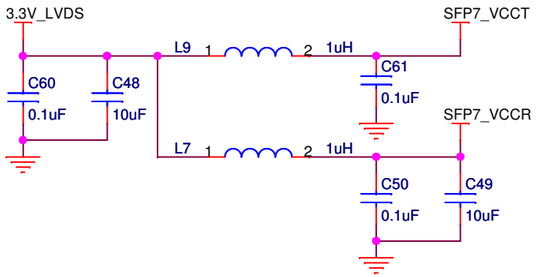
LVDS Based SFP Connectors

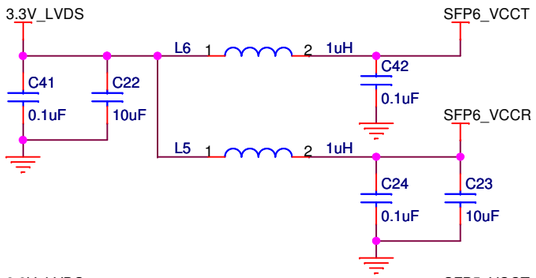
SFPs 4-7

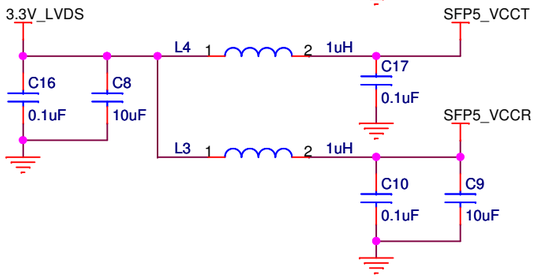
NOTE 1: 1uH ferrite bead should have a DC resistance of less than 1-ohm.

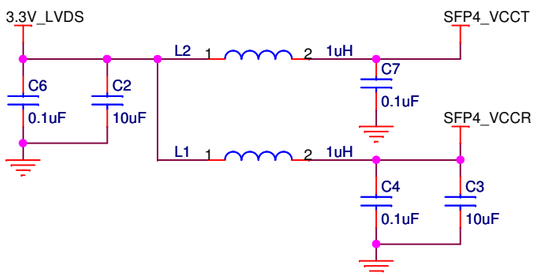
NOTE 2: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.

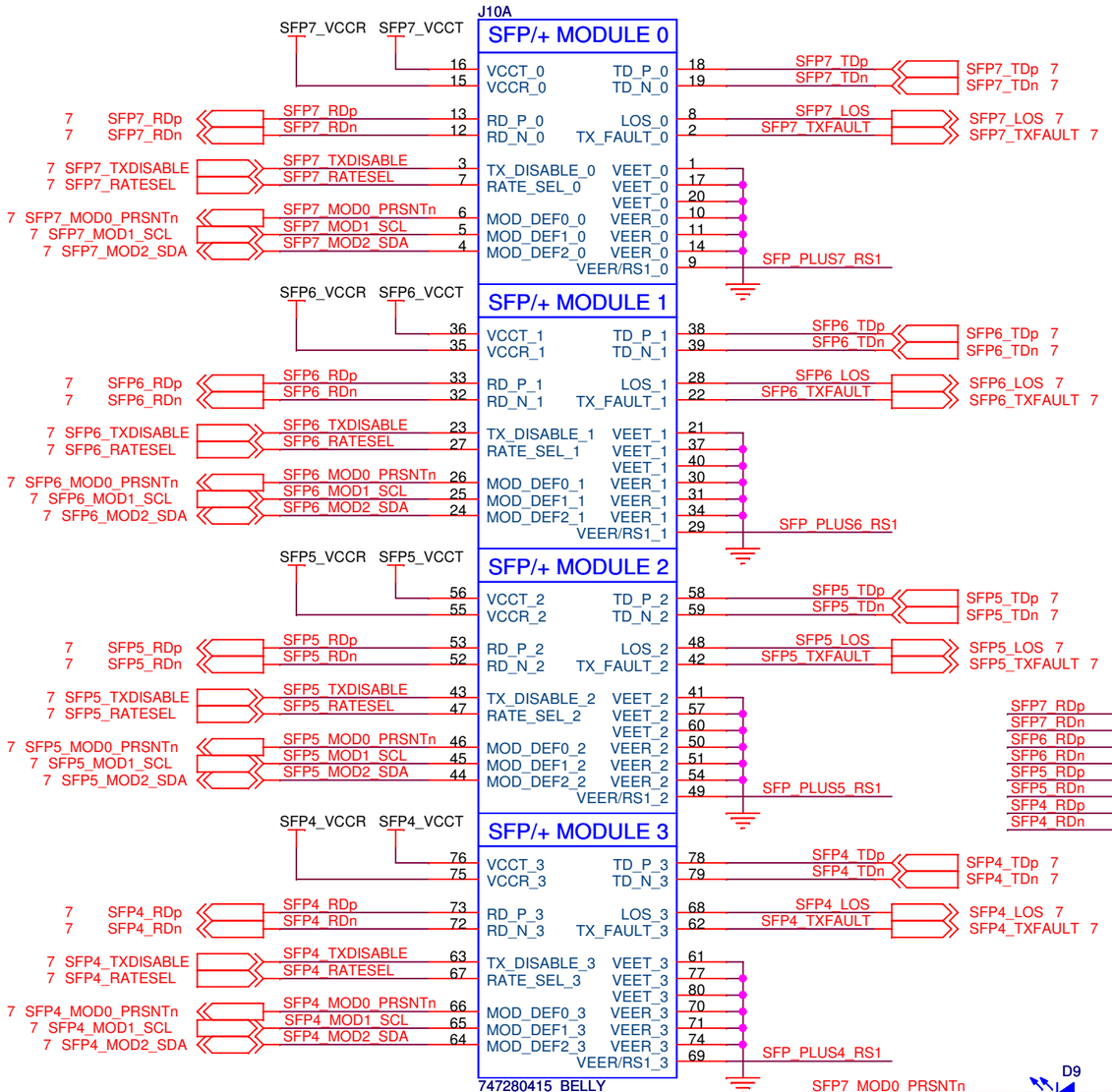
NOTE 3: Assuming that the SFP RD 100-ohm termination on the Host Board FPGA device will be implemented via the on-chip termination circuit.

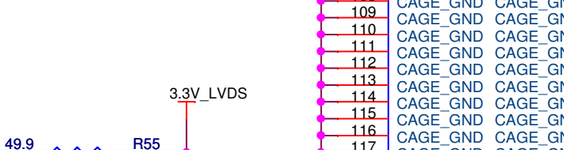












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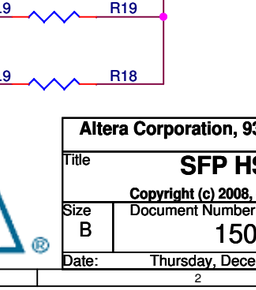
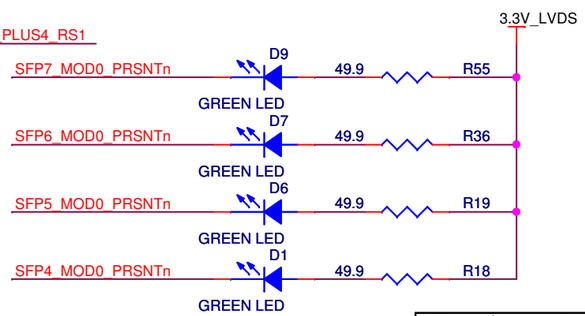
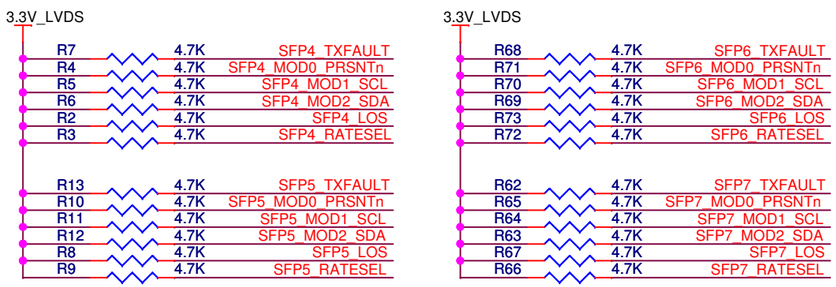


Optical (SFP) Transceiver Cage & Connector





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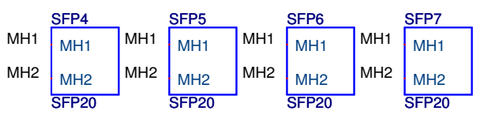

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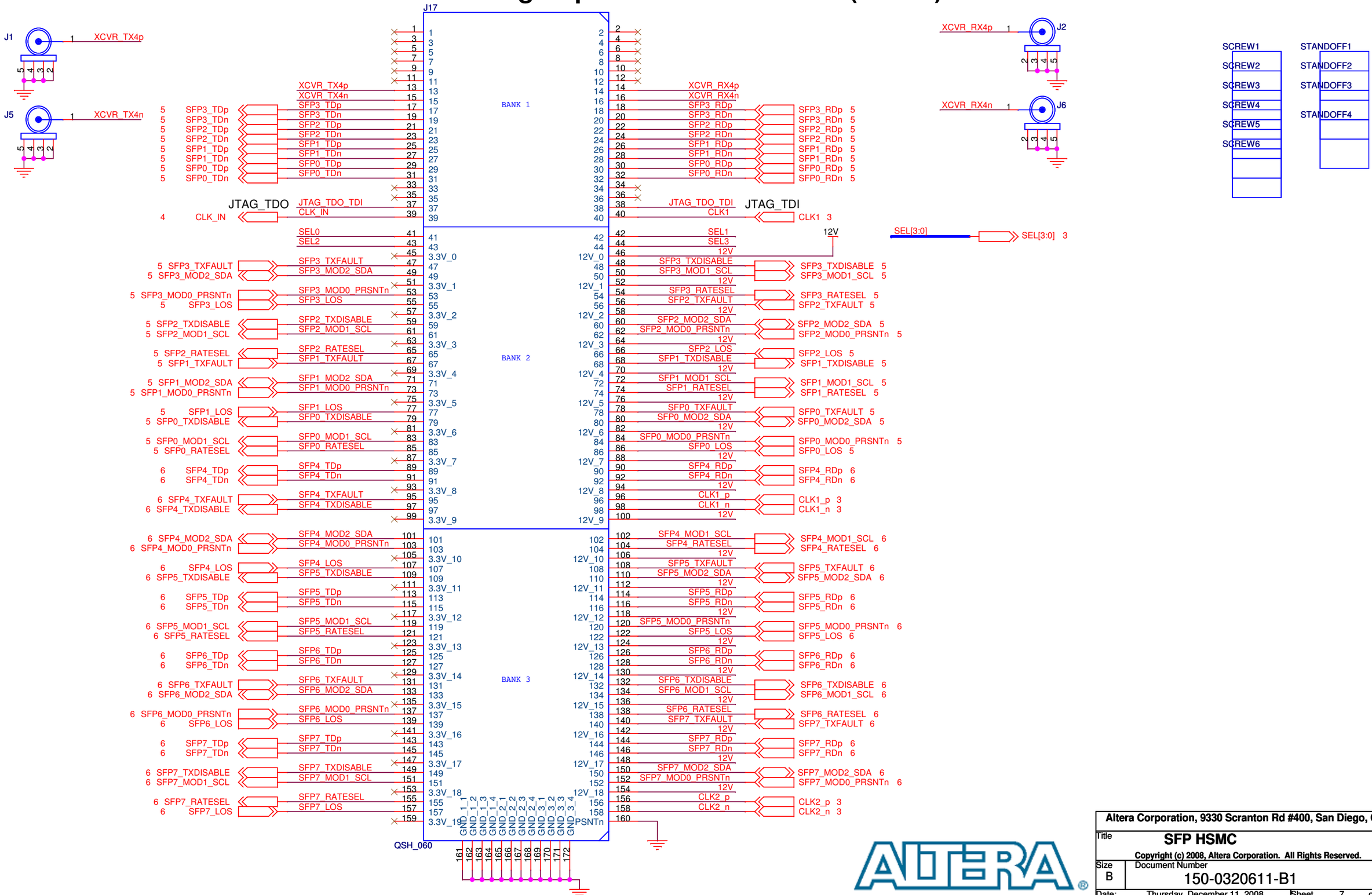
High Speed Mezzanine Card (HSMC)



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