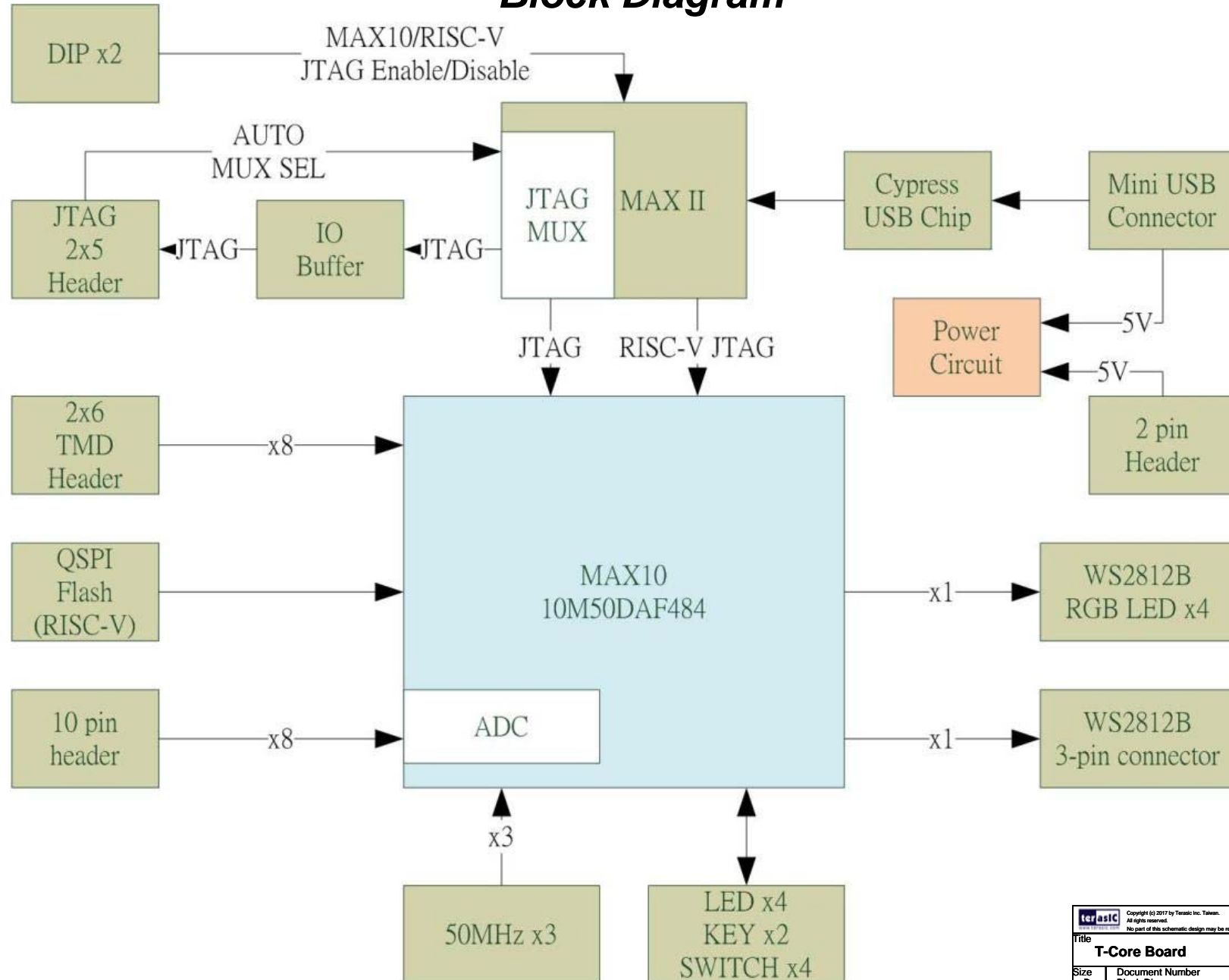


T-Core

MAX10 Development Board

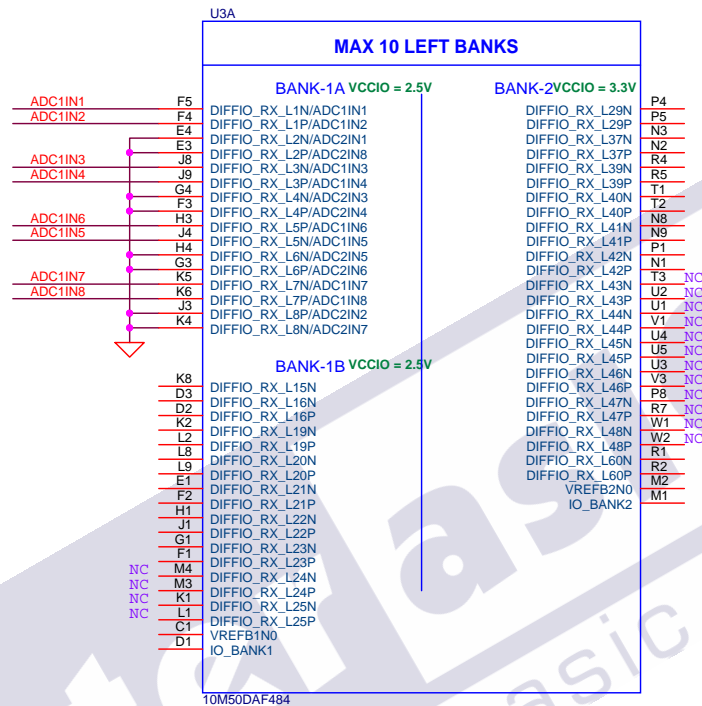
PAGE	CONTENT	PAGE	CONTENT
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4	MAX 10 Bank 3 & 4	22	
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9	MAX10 Power		
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14	Power - 5V, 1.2V		
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Block Diagram

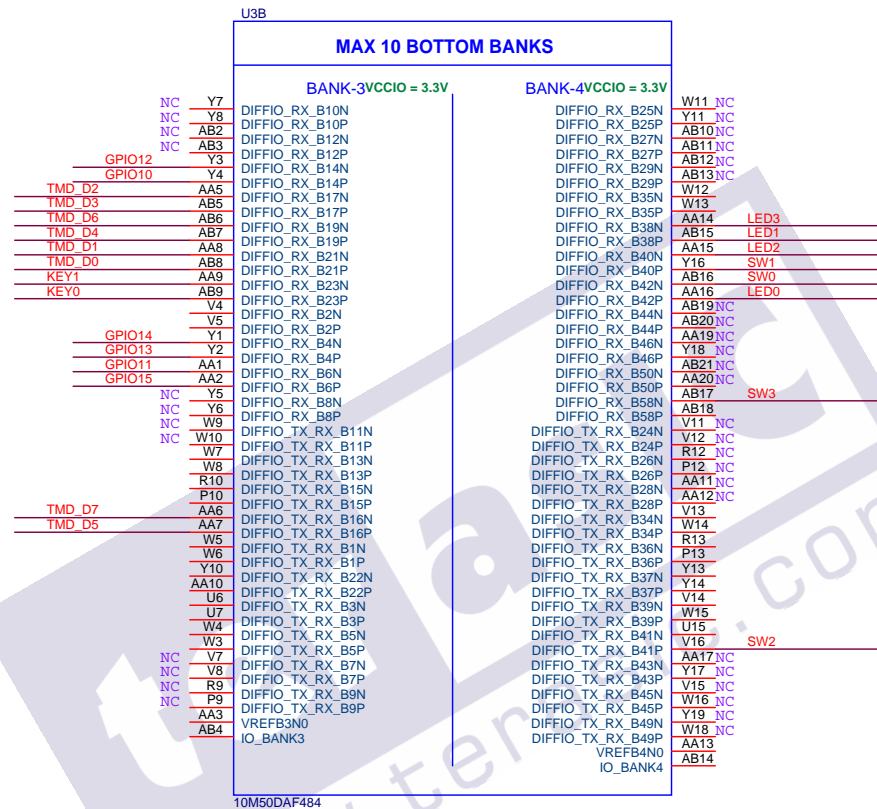
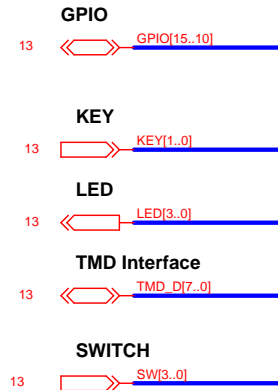


Analog input interface

ADC1IN[8..1]

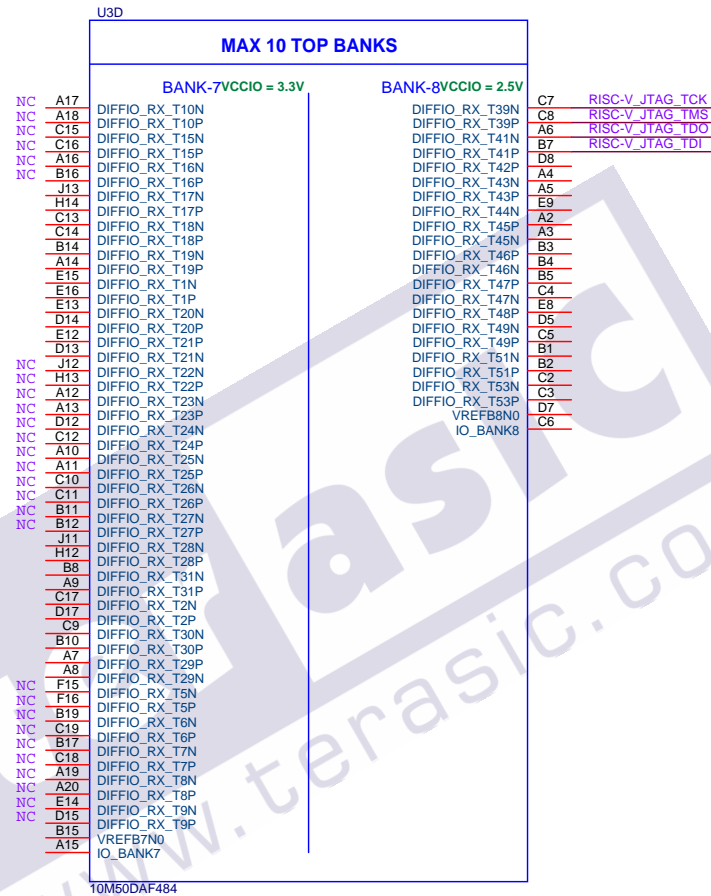


MAX10 Bank 3 & 4

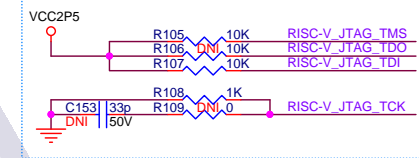


MAX10 Bank 7 & 8

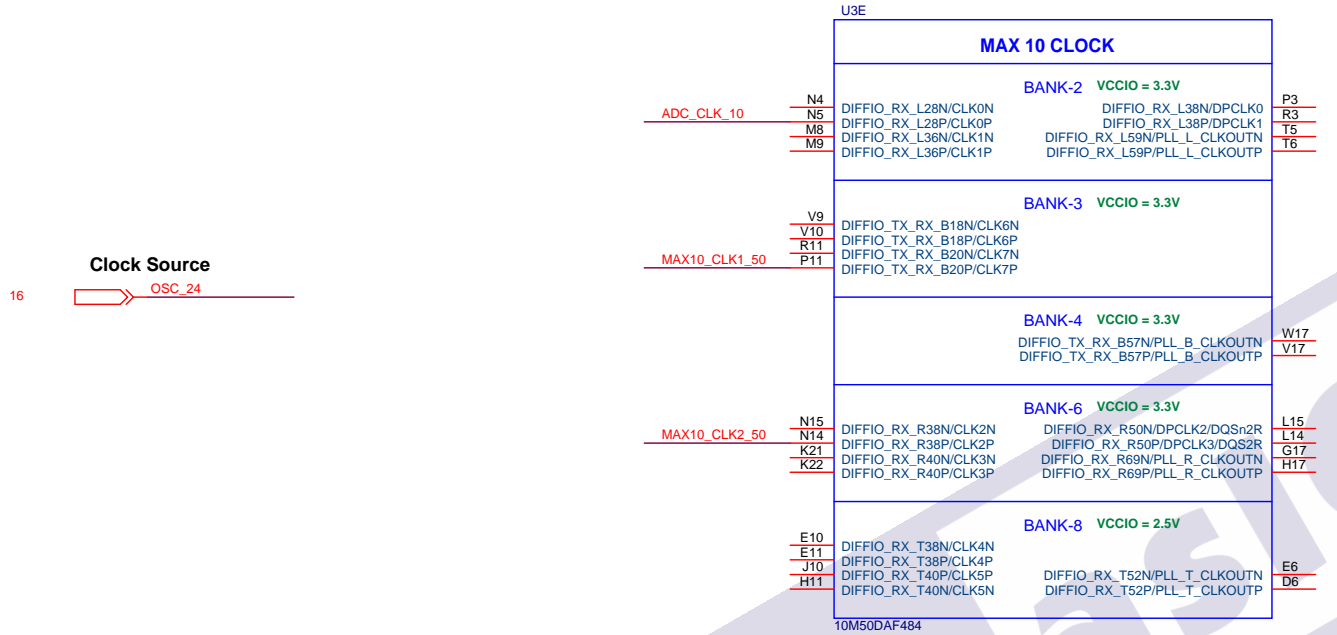
JTAG to RISC-V (2.5V)



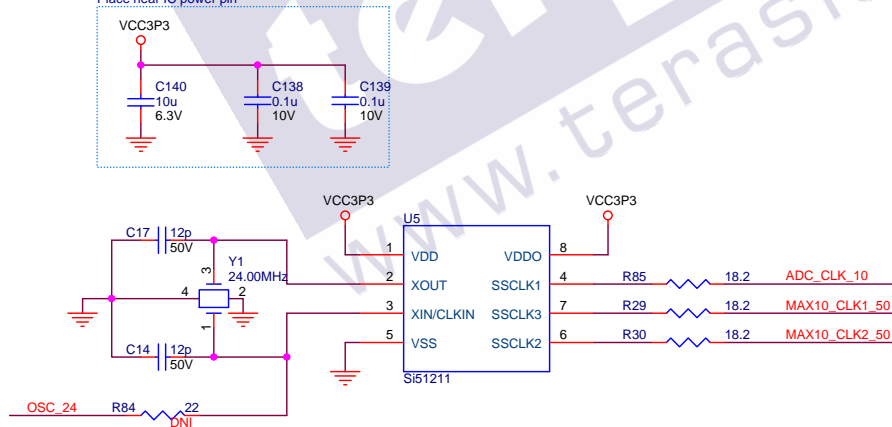
CAD Note:
Place close to MAX10



MAX10 Clock



CAD Note:
Place near IC power pin

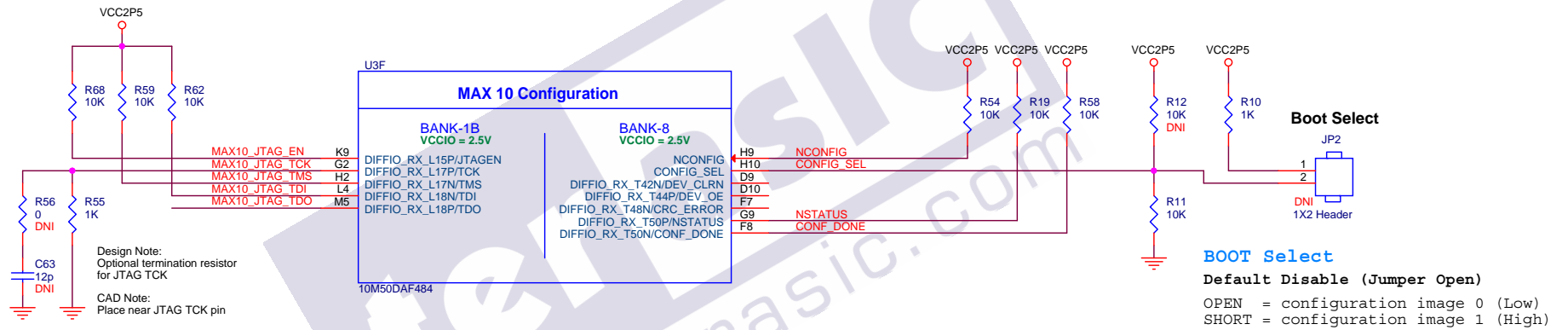
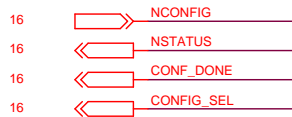


MAX10 Configuration

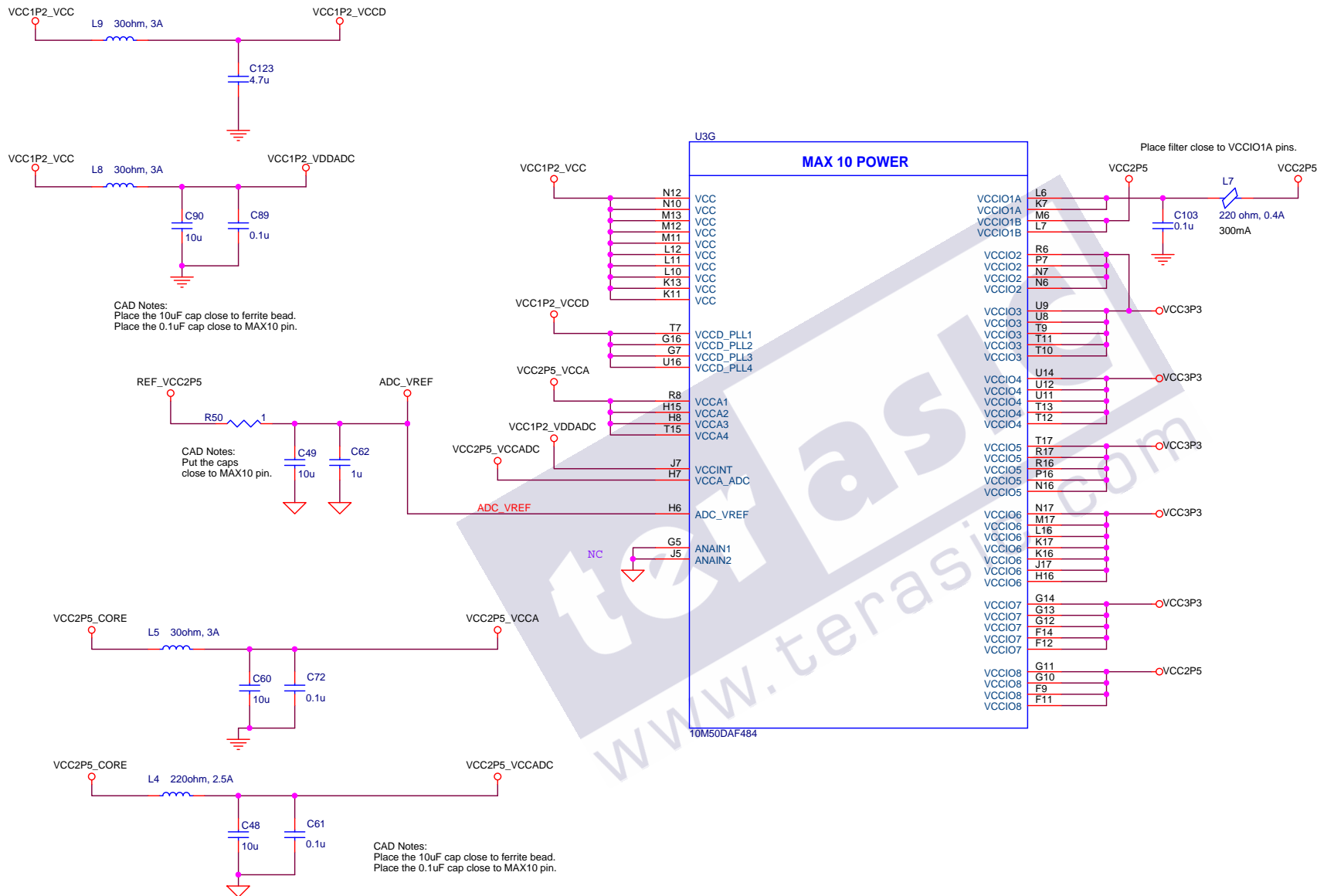
JTAG Interface



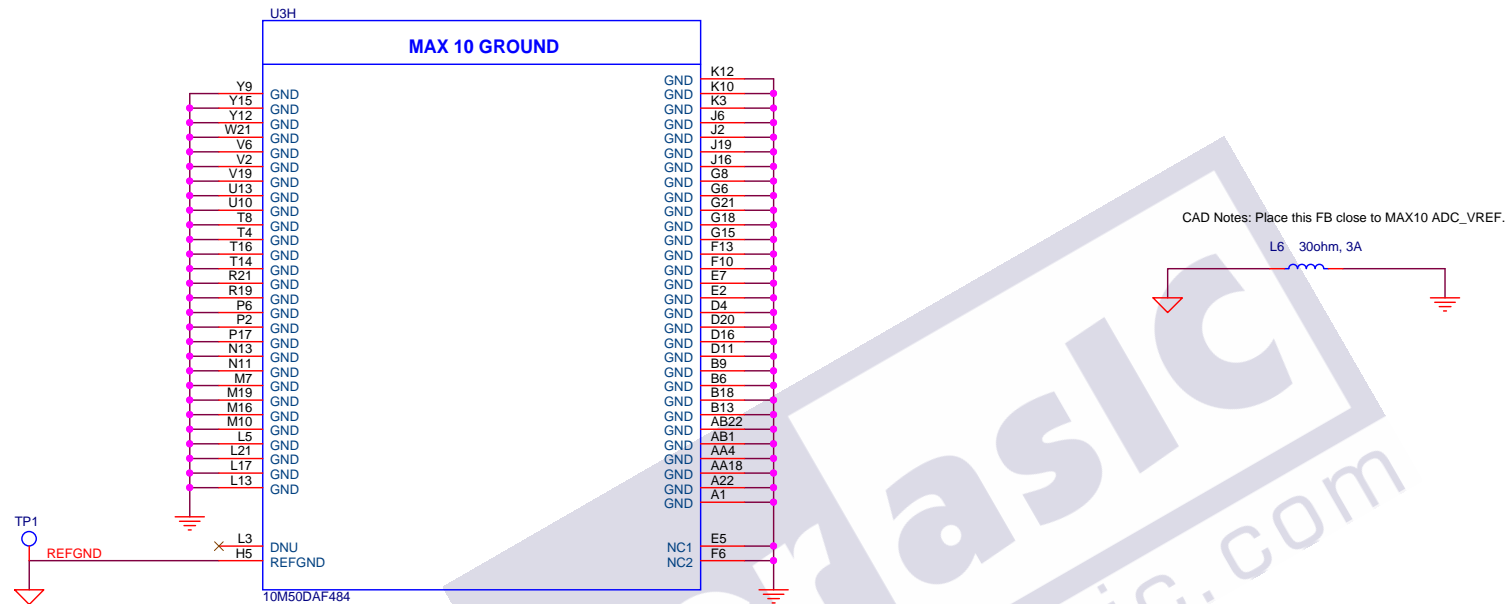
FPGA CONFIG



MAX10 Power

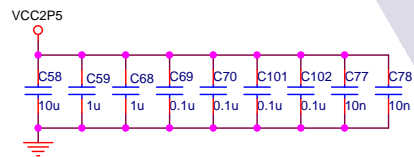
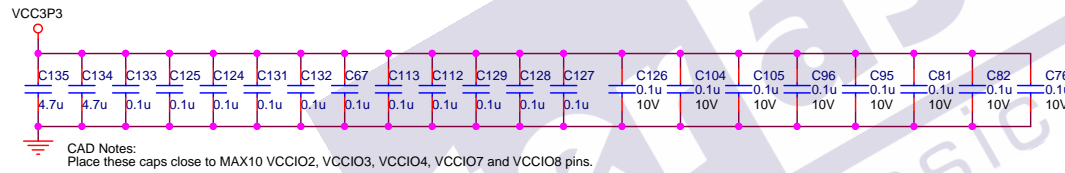
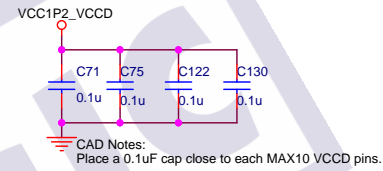
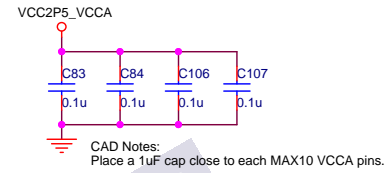
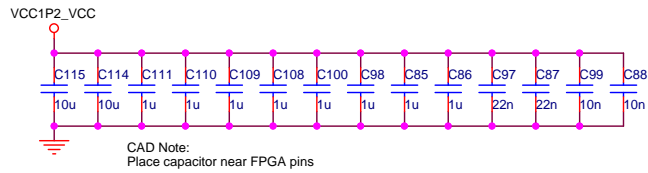


MAX10 Ground



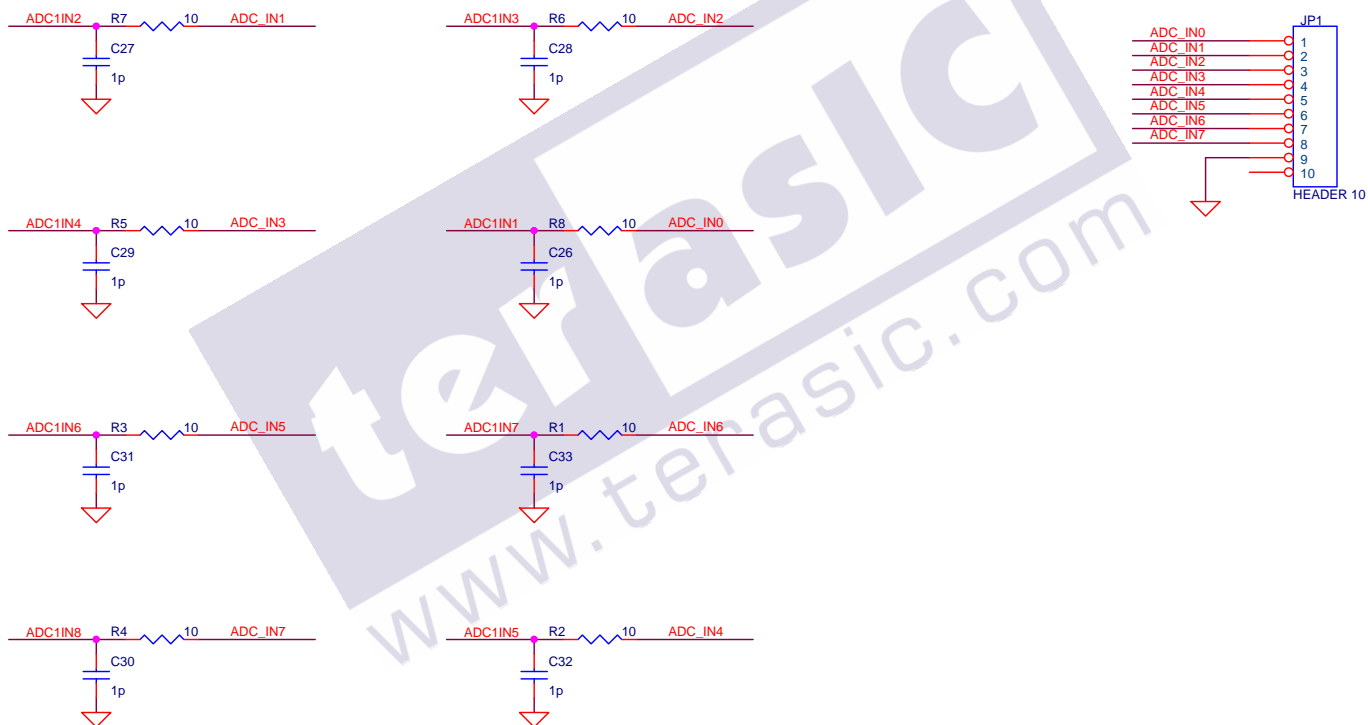
1. Use REFGND as ground reference.
2. Route analog input signal adjacent to AVSSREF as possible.

MAX10 Decoupling

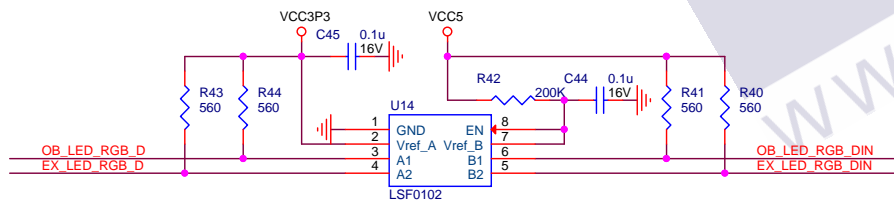
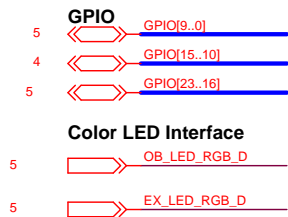
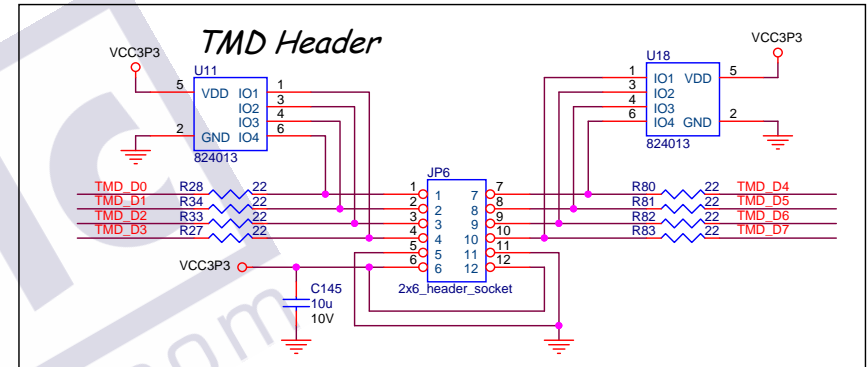
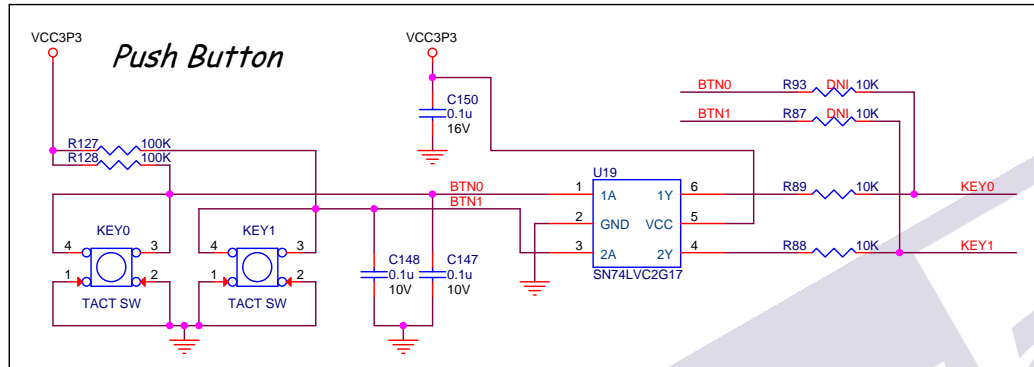
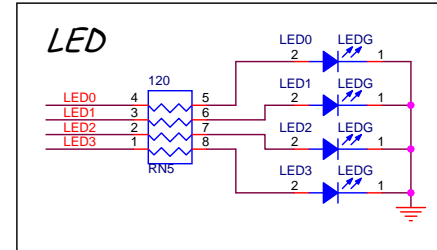
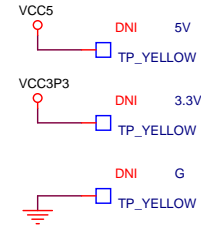
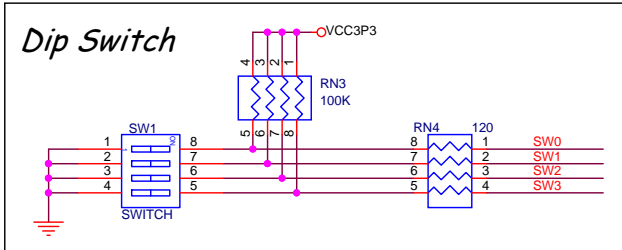
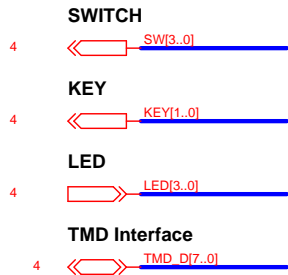


Analog input interface

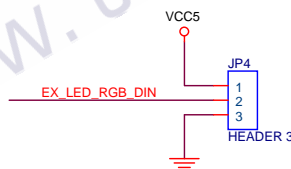
3 ADC1IN[8..1]



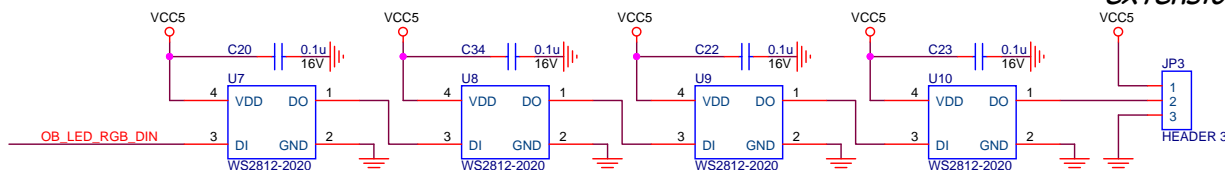
User IO, Button, Switch and LED



External RGB LED Port



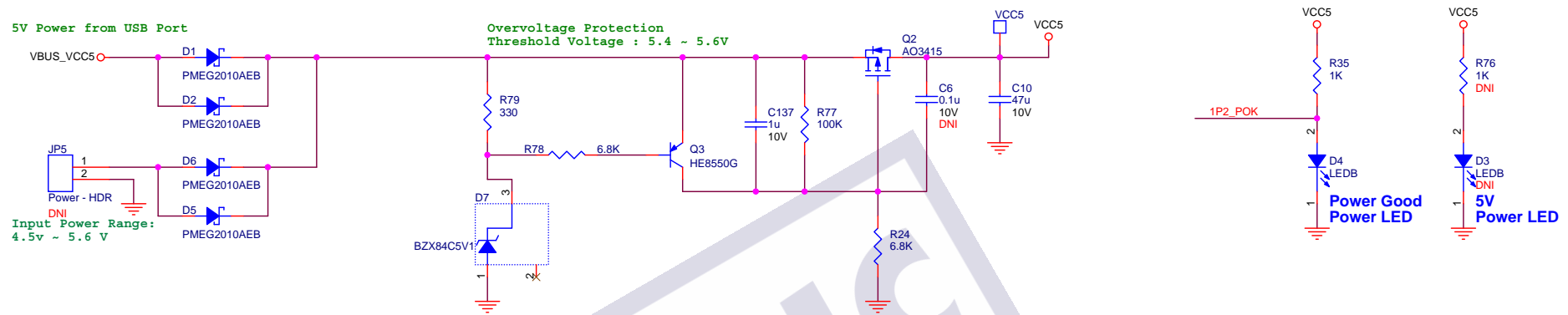
On Board RGB LED extension port



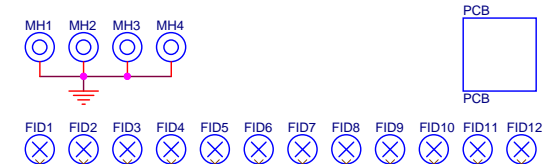
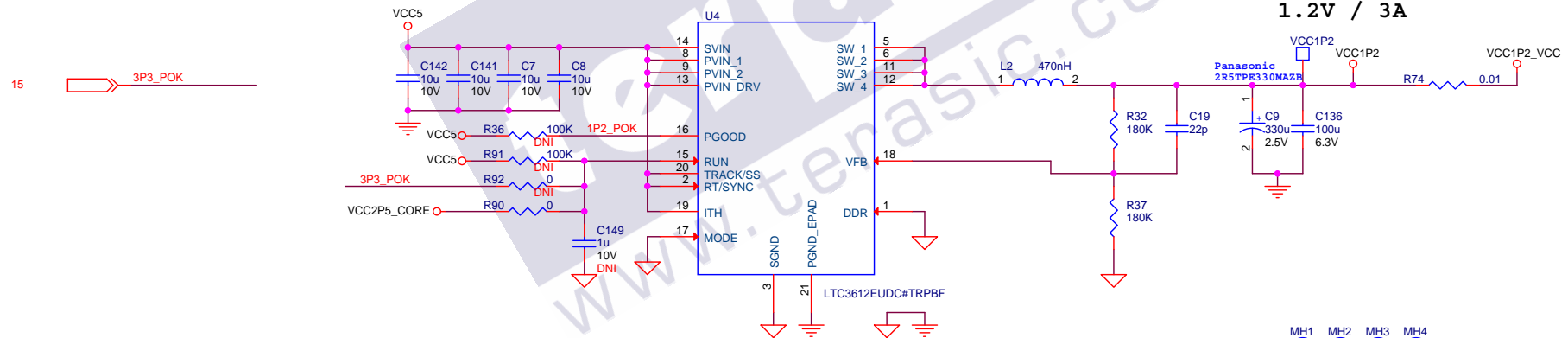
Power - 5V_DCIN / 1.2V


Power up Sequence:

VCC5---> VCC2P5, VCC3P3 ---> VCC1P2_VCC



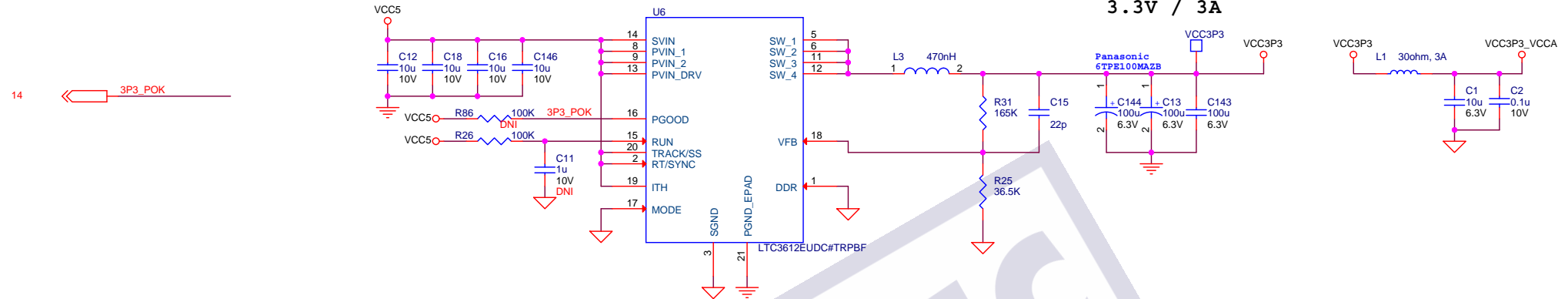
Ramp Time
Tsoft-start = 1 msec
Switching Frequency : 2.25MHz
1.2V / 3A



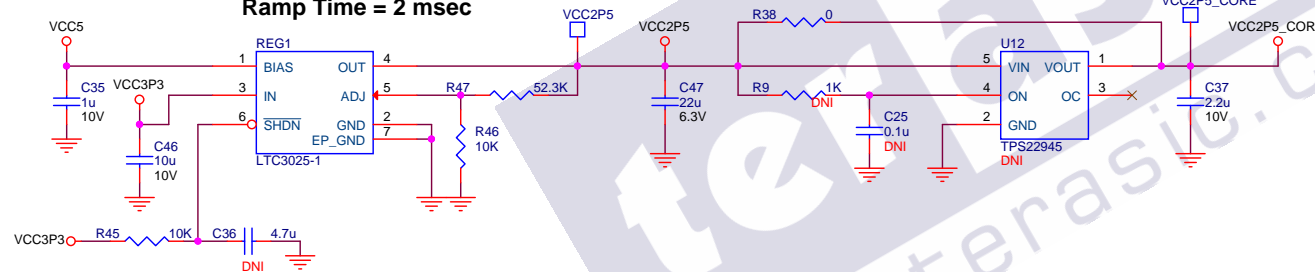
		Copyright (c) 2017 by Terasic Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.	
Title			
T-Core Board			
Size	Document Number		Rev
B	Power - 12V, 5V		A1
Date:	Monday, November 18, 2019	Sheet	14 of 16

Power - 3.3V / 2.5V

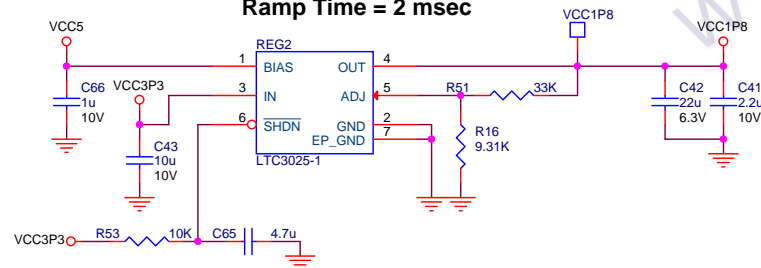
Ramp Time
Tsoft-start = 1 msec
Switching Frequency : 2.25MHz
3.3V / 3A



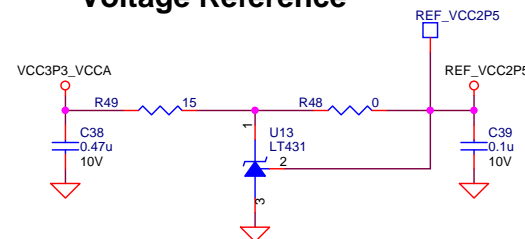
2.5V / 0.5A Ramp Time = 2 msec



1.8V / 0.5A Ramp Time = 2 msec



Voltage Reference



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Title T-Core Board			
Size B	Document Number Power - 1.8V, 2.5V, 3.3V	Rev A1	
Date: Monday, November 18, 2019	Sheet 15	of 16	1