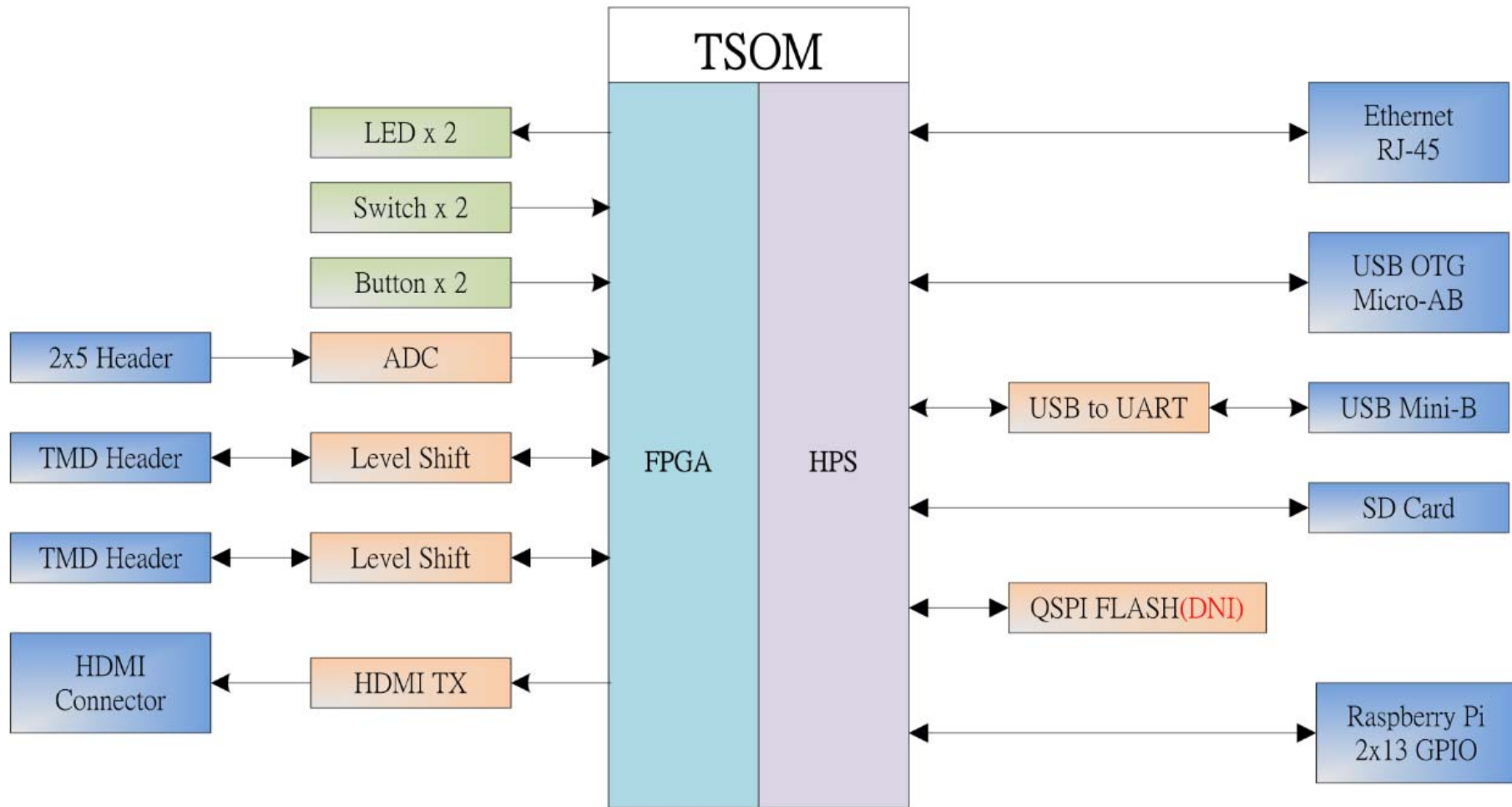
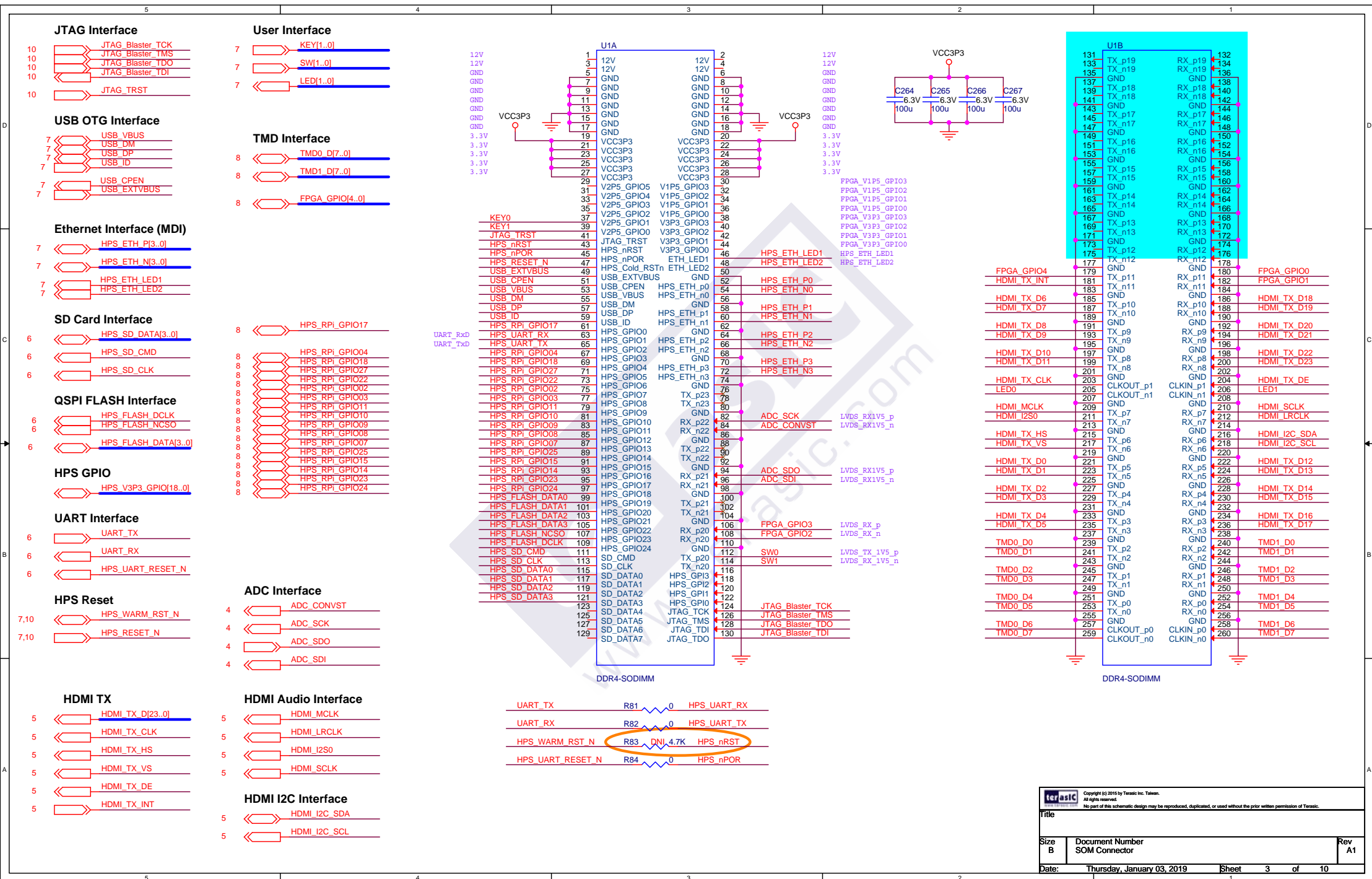
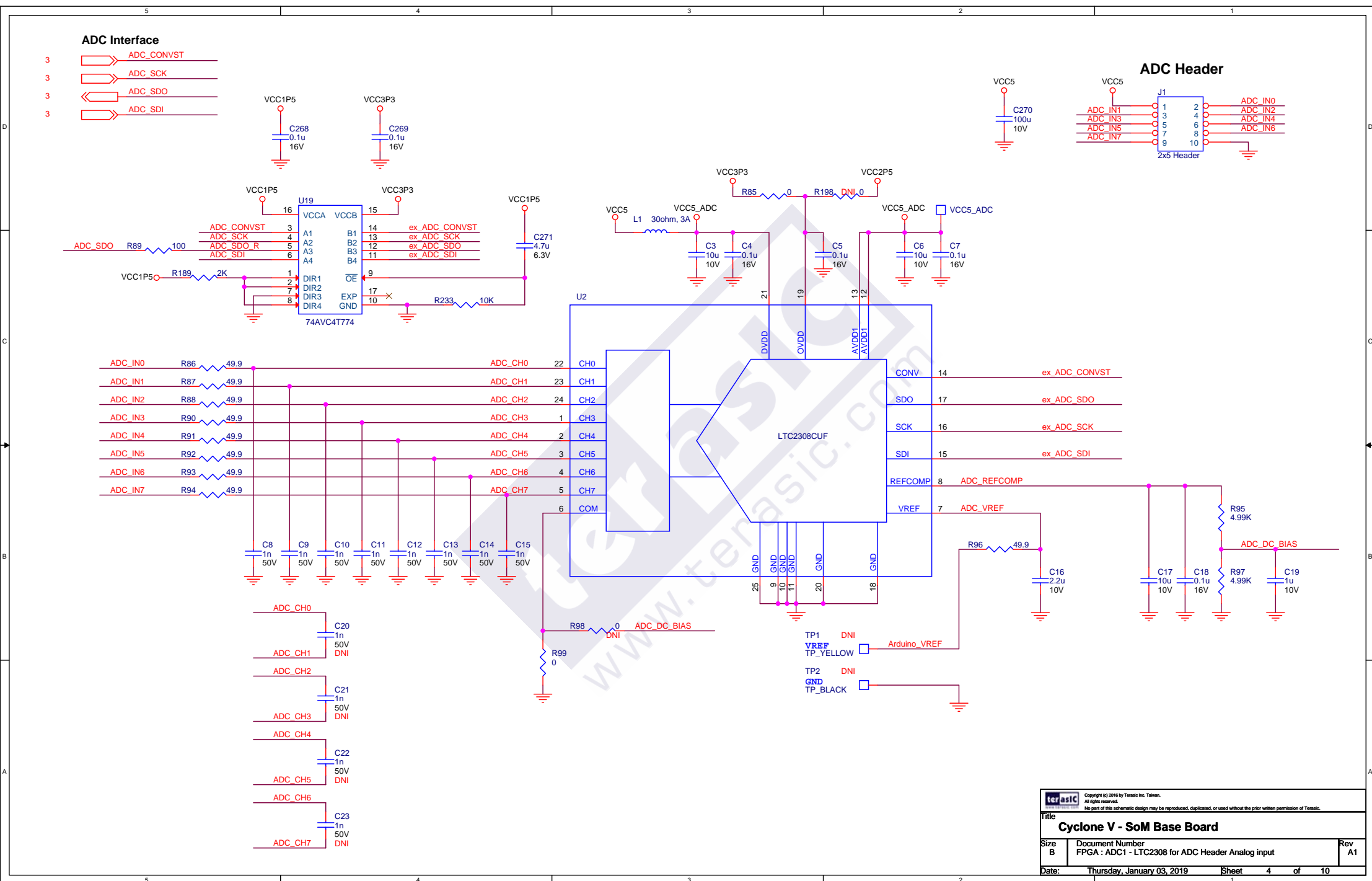


## Cyclone V SoC System on module Base Board

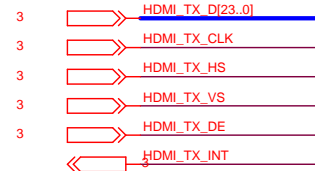
PAGE	CONTENT
01	Cover Page
02	Block Diagram
03	SOM connector
04	FPGA : ADC1 (LTC2308) for 8-channel Analog Expansion Header
05	FPGA : HDMI TX
06	HPS : UART to USB, QSPI Flash & SD CARD
07	FPGA : LED, KEY, SW / HPS : USB-OTG, Ethernet and Reset
08	Expansion IO
09	Power System
10	USB Blaster II
11	
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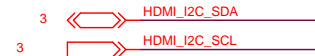
## HDMI TX



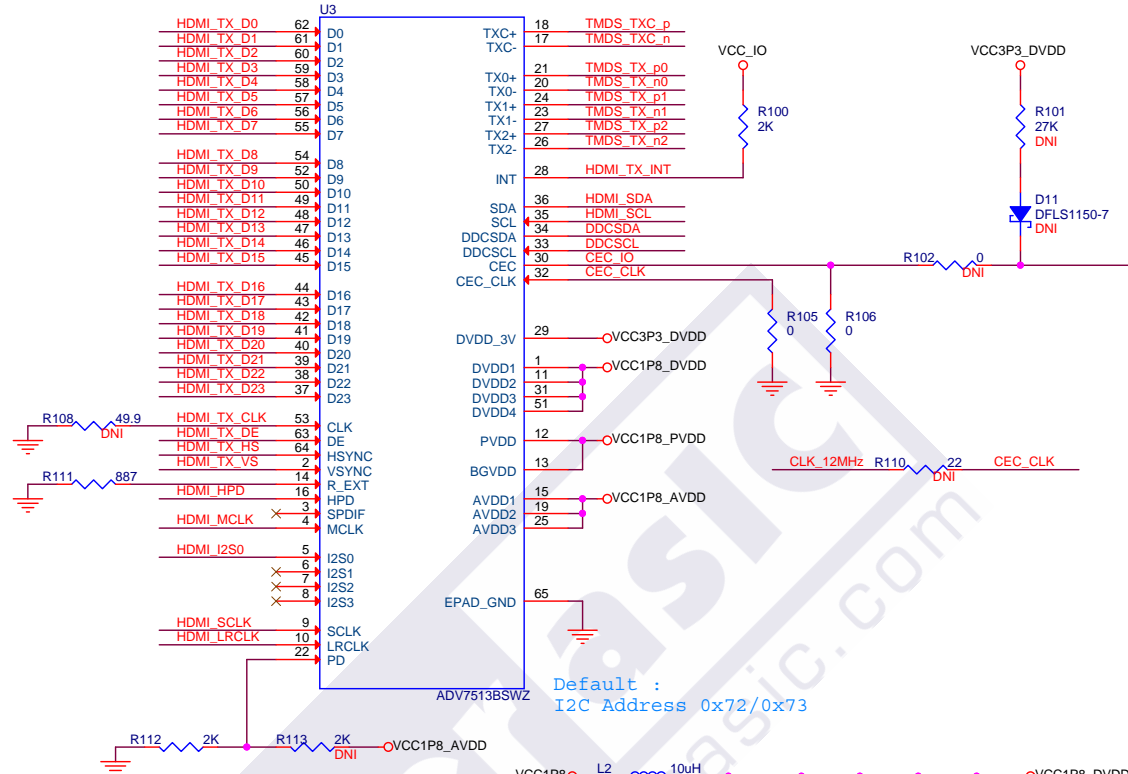
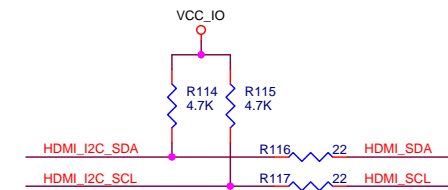
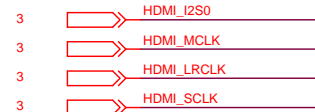
## From MAX



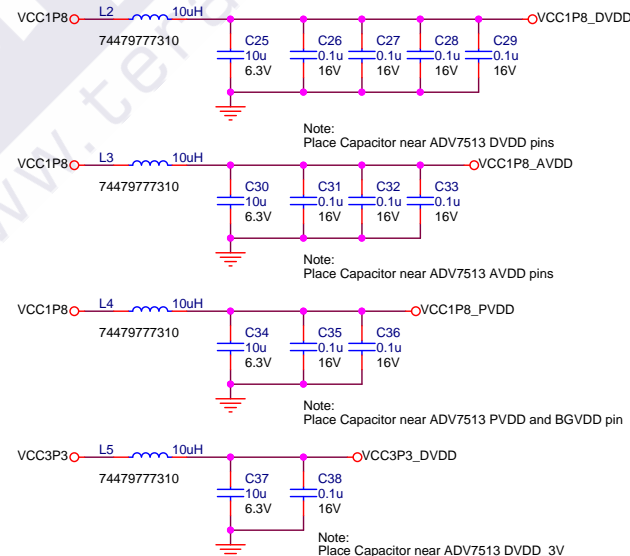
## I2C Interface



## HDMI Audio Interface



Default :  
I2C Address 0x72/0x73



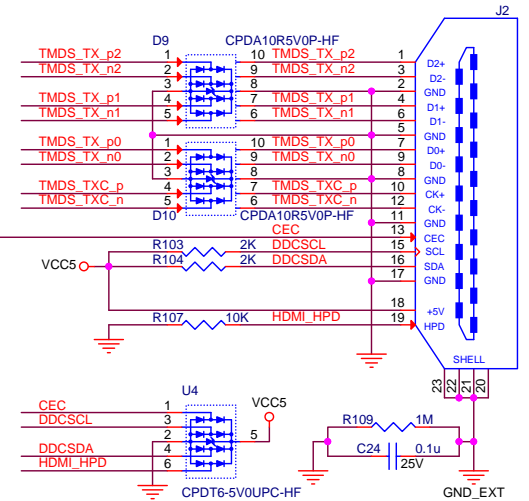
Note:  
Place Capacitor near ADV7513 DVDD pins

Note:  
Place Capacitor near ADV7513 AVDD pins

Note:  
Place Capacitor near ADV7513 PVDD and BGVDD pin

Note:  
Place Capacitor near ADV7513 DVDD\_3V

## HDMI TX



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Title			
Cyclone V - SoM Base Board			
Size	Document Number	Rev	
B	FPGA : HDMI TX	A1	
Date:	Thursday, January 03, 2019	Sheet	5 of 10



## User Interface

### KEY

KEY[1..0]

### SWITCH

SW[1..0]

### LED

LED[1..0]

## HPS Reset

HPS\_WARM\_RST\_N

HPS\_RESET\_N

## USB OTG Interface

USB\_VBUS

USB\_DM

USB\_DP

USB\_ID

USB\_CPEN

USB\_EXTVBUS

## Ethernet Interface (MDI)

HPS\_ETH\_P[3..0]

HPS\_ETH\_N[3..0]

HPS\_ETH\_LED1

HPS\_ETH\_LED2

## User Button

## User LED and Switch

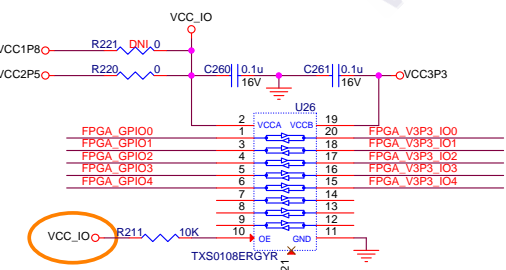
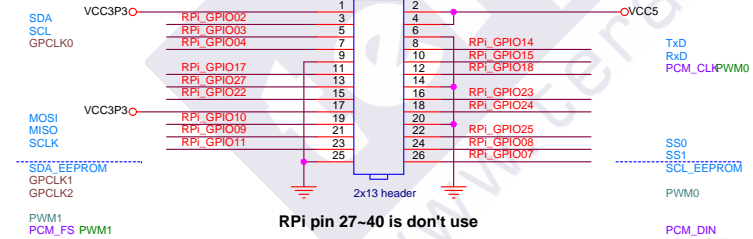
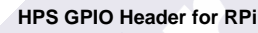
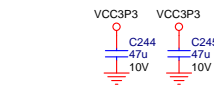
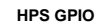
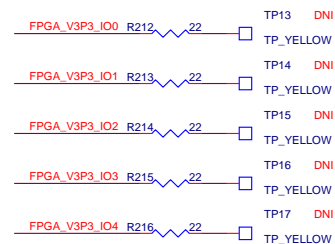
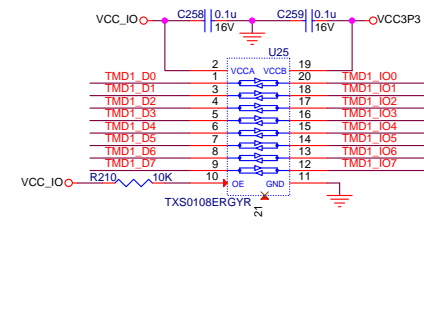
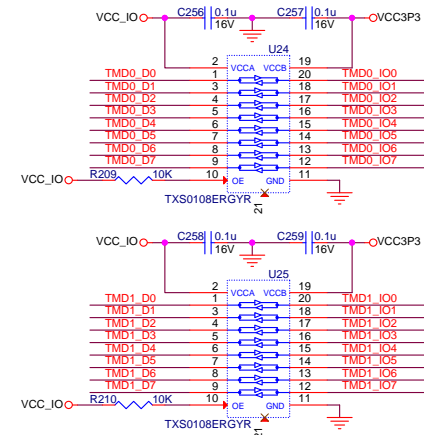
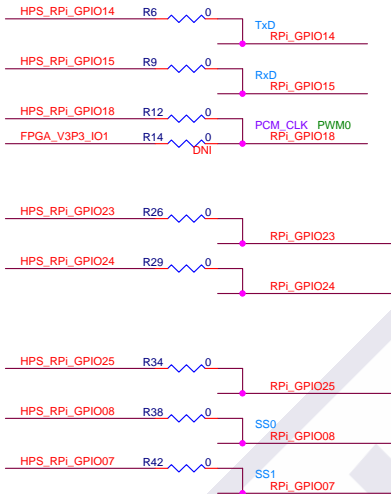
## HPS Reset Button

### Cold Reset

### Warm Reset

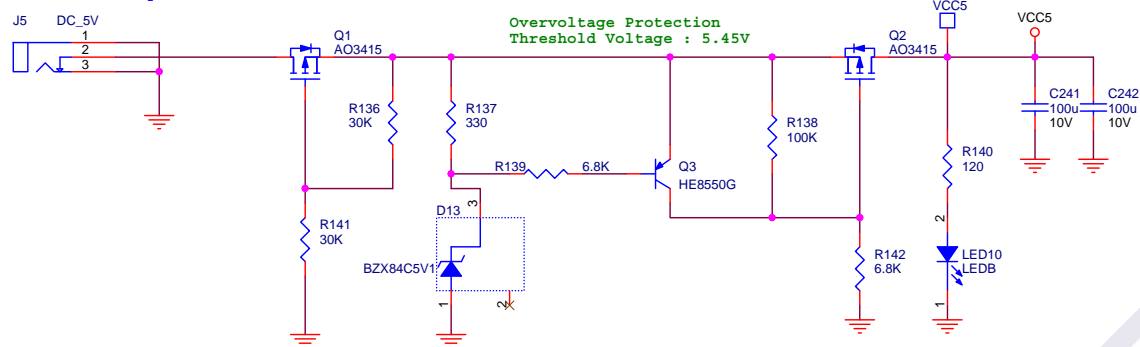
## USB OTG

## Ethernet RJ-45

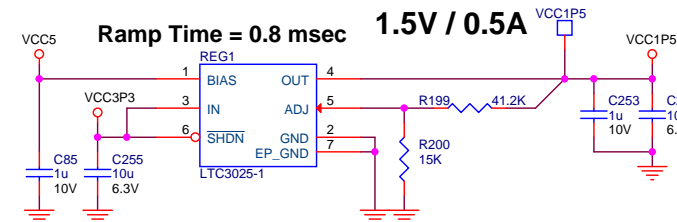




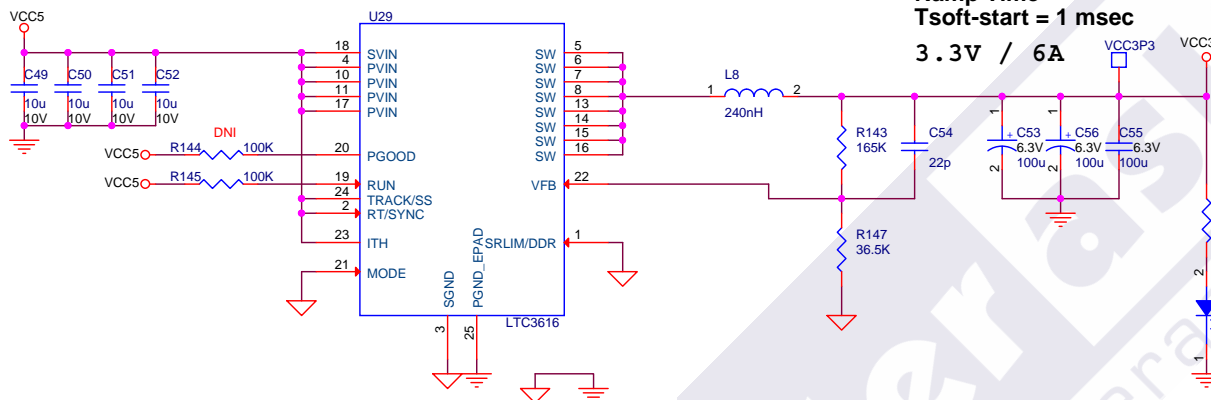
# DC 5V Power Input



# Ramp Time = 0.8 msec 1.5V / 0.5A

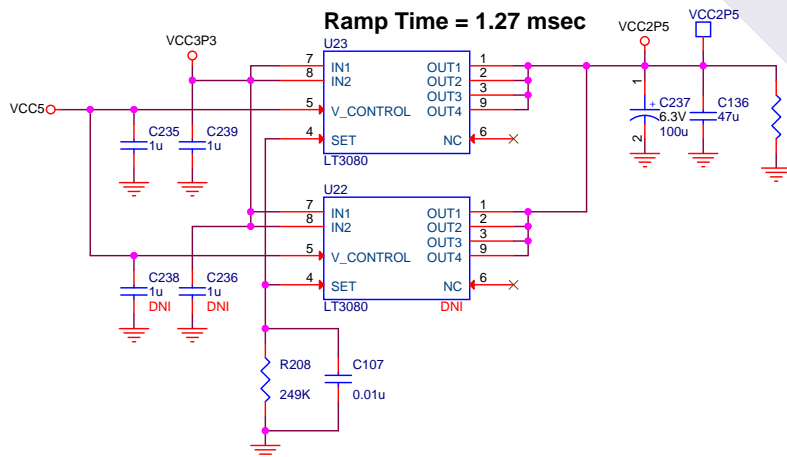


# Ramp Time Tsoft-start = 1 msec 3.3V / 6A



# 2.5V / 2.2A

## Ramp Time = 1.27 msec



# 1.8V / 1.1A

## Ramp Time = 1.2 msec

