

LSF010x 1/2/8 Channel Bidirectional Multi-Voltage Level Translator for Open-Drain and Push-Pull Application

1 Features

- Provides Bidirectional Voltage Translation With No Direction Pin
- Less Than 1.5 ns Max Propagation Delay
- Supports High Speed Translation, Greater Than 100 MHz
- Supports Hot Insertion
- Allow Bidirectional Voltage Level Translation Between
 - 0.95 V ↔ 1.8/2.5/3.3/5 V
 - 1.2 V ↔ 1.8/2.5/3.3/5 V
 - 1.8 V ↔ 2.5/3.3/5 V
 - 2.5 V ↔ 3.3/5 V
 - 3.3 V ↔ 5 V
- Low Standby Current
- 5 V Tolerance I/O Port to Support TTL
- Low Ron Provides Less Signal Distortion
- High-Impedance I/O pins For EN = Low
- Flow-Through Pinout for Ease PCB Trace Routing
- Latch-Up Performance Exceeds 100 mA Per JESD 17
- 40°C to 125°C Operating Temperature Range
- ESD Performance Tested Per JESD 22
 - 2000 V Human-Body Model (A114-B, Class II)
 - 200 V Machine Model (A115-A)
 - 1000 V Charged-Device Model (C101)

2 Applications

- GPIO, MDIO, PMBus, SMBus, SDIO, UART, I²C, and Other Interfaces in Telecom Infrastructure
- Industrial
- Automotive
- Personal Computing

3 Description

The LSF family are bidirectional voltage level translators operational from 0.95 to 4.5 V (Vref_A) and 1.8 to 5.5 V (Vref_B). This allows bidirectional voltage translations between 1 and 5 V without the need for a direction pin in open-drain or push-pull applications. LSF family supports level translation applications with transmission speeds greater than 100 Mbps for open-drain systems using a 30-pF capacitance and 250-Ω pullup resistor.

When the An or Bn port is LOW, the switch is in the ON-state and a low resistance connection exists between the An and Bn ports. The low R_{on} of the switch allows connections to be made with minimal propagation delay and signal distortion. Assuming the higher voltage is on the Bn port when the Bn port is HIGH, the voltage on the An port is limited to the voltage set by Vref_A. When the An port is HIGH, the Bn port is pulled to the drain pullup supply voltage (V_{pu#}) by the pullup resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user without the need for directional control.

The supply voltage (V_{pu#}) for each channel can be individually set up with a pullup resistor. For example, CH1 can be used in up-translation mode (1.2 V ↔ 3.3 V) and CH2 in down-translation mode (2.5 V ↔ 1.8 V).

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|-----------|-------------------|
| LSF0101 | SON (6) | 1.45 mm x 1.00 mm |
| LSF0102 | X2SON (8) | 1.40 mm x 1.00 mm |
| | DSBGA (8) | 1.90 mm x 1.00 mm |
| LSF0108 | VQFN (20) | 4.50 mm x 2.50 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

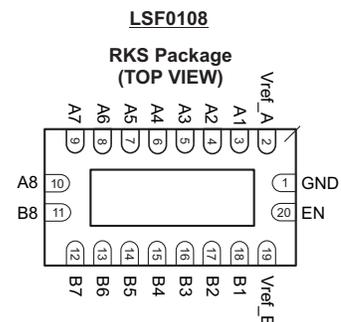
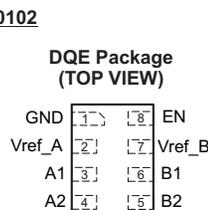
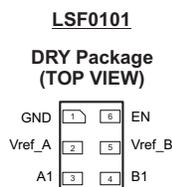


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4 Revision History

| Changes from Revision C (May 2014) to Revision D | Page |
|--|-----------|
| • Changed bidirectional voltage level translation from 1.0 to 0.95 | 1 |
| • Changed YZT package to fix view error. | 1 |
| • Changed YZT package to fix view error. | 3 |
| • Added pin numbers to <i>Pin Functions</i> table | 3 |
| • Added V_{ref_A} footnote. | 13 |

| Changes from Revision B (May 2014) to Revision C | Page |
|---|----------|
| • Changed LSF0108 status from preview to production. | 1 |
| • Updated document title. | 1 |
| • Updated Handling Ratings table. | 4 |

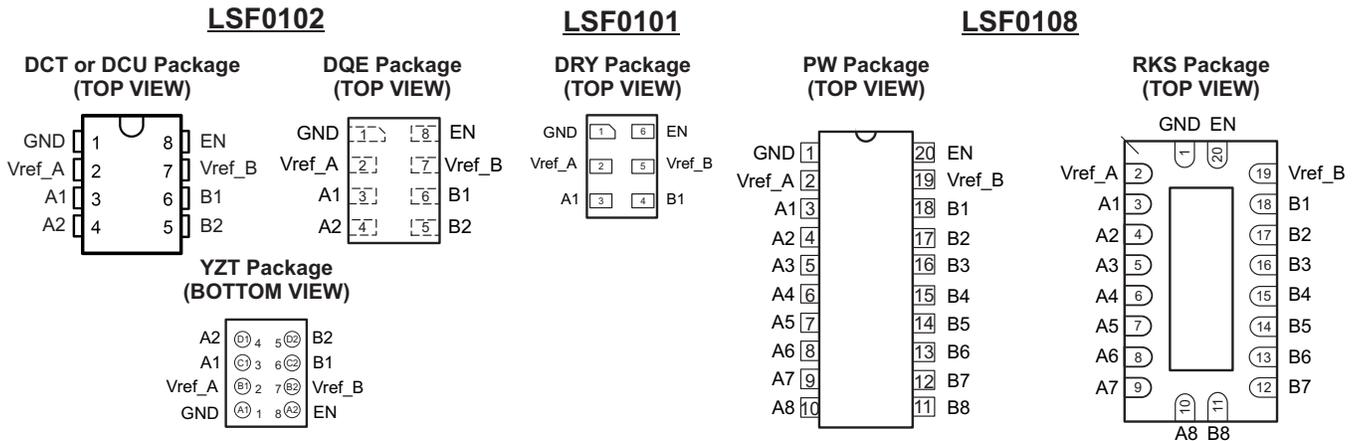
| Changes from Revision A (January 2014) to Revision B | Page |
|--|----------|
| • Added LSF0108 to data sheet. | 1 |

| Changes from Original (December 2013) to Revision A | Page |
|---|----------|
| • Updated part number | 1 |
| • Updated <i>Electrical Characteristics</i> table | 6 |

5 Description (continued)

When EN is HIGH, the translator switch is on, and the An I/O is connected to the Bn I/O, respectively, allowing bidirectional data flow between ports. When EN is LOW, the translator switch is off, and a high-impedance state exists between ports. The EN input circuit is designed to be supplied by Vref_B. To ensure the high-impedance state during power-up or power-down, EN must be LOW.

6 Pin Configuration and Functions



Pin Functions

| NAME | PIN | | | DESCRIPTION |
|--------|------------------------|---------|---------------|---|
| | DCT, DCU, DQE, YZT NO. | DRY NO. | PW or RKS NO. | |
| An | 3, 4 | 3 | 3 to 10 | Data port |
| Bn | 6, 5 | 4 | 18 to 11 | |
| EN | 8 | 6 | 20 | Switch enable input; connect to Vref_B and pullup through a high resistor (200 kΩ). |
| GND | 1 | 1 | 1 | Ground |
| Vref_A | 2 | 2 | 2 | Reference supply voltage; see Application and Implementation . |
| Vref_B | 7 | 5 | 19 | Reference supply voltage; see Application and Implementation . |

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature (unless otherwise noted)

| | | MIN | MAX | UNIT |
|-----------------|--|-------------|-----|------|
| V_I | Input voltage ⁽²⁾ | -0.5 | 7 | V |
| $V_{I/O}$ | Input/output voltage ⁽²⁾ | -0.5 | 7 | V |
| | Continuous channel current | | 128 | mA |
| I_{IK} | Input clamp current | $V_I < 0$ | -50 | mA |
| $R_{\theta JA}$ | Package thermal impedance ⁽³⁾ | DCT package | 220 | °C/W |
| | | DCU package | 227 | |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and input/output negative-voltage ratings may be exceeded if the input and input/output clamp-current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

7.2 Handling Ratings

| | | MIN | MAX | UNIT | |
|-------------|---------------------------|--|-----|------|---|
| T_{stg} | Storage temperature range | -65 | 150 | °C | |
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | 0 | 2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | 0 | 1000 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|-------------------|--------------------------------|-----|-----|------|
| $V_{I/O}$ | Input/output voltage | 0 | 5 | V |
| $V_{ref_A/B/EN}$ | Reference voltage | 0 | 5 | V |
| I_{PASS} | Pass transistor current | | 64 | mA |
| T_A | Operating free-air temperature | -40 | 85 | °C |

7.4 Thermal Information: LSF0101, LSF0108

| THERMAL METRIC ⁽¹⁾ | | LSF0101 | LSF0108 | LSF0108 | UNIT |
|-------------------------------|--|---------|---------|---------|------|
| | | DRY | RKS | PWR | |
| | | 6 PINS | 20 PINS | 20 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 407.0 | 49.3 | 106.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 285.2 | 45.9 | 41.0 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 271.6 | 20.6 | 57.6 | |
| Ψ_{JT} | Junction-to-top characterization parameter | 113.5 | 2.5 | 4.2 | |
| Ψ_{JB} | Junction-to-board characterization parameter | 271.0 | 20.6 | 47.0 | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | 3.4 | n/a | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Thermal Information: LSF0102

| THERMAL METRIC ⁽¹⁾ | | LSF0102 | LSF0102 | LSF0102 | LSF0102 | UNIT |
|-------------------------------|--|---------|---------|---------|---------|------|
| | | DCU | DCT | DQE | YZT | |
| | | 8 PINS | 8 PINS | 8 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 210.1 | 189.6 | 246.5 | 125.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 89.1 | 119.6 | 149.1 | 1.0 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 88.8 | 102.1 | 100.0 | 62.7 | |
| Ψ_{JT} | Junction-to-top characterization parameter | 8.3 | 44.5 | 17.1 | 3.4 | |
| Ψ_{JB} | Junction-to-board characterization parameter | 88.4 | 101.0 | 99.8 | 62.7 | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | n/a | n/a | n/a | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

7.6 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|---|---|--|-----|--------------------|----------|---------------|
| V_{IK} | $I_I = -18 \text{ mA}$, $V_{EN} = 0$ | | | | -1.2 | V |
| I_{IH} | $V_I = 5 \text{ V}$, $V_{EN} = 0$ | | | | 5.0 | μA |
| I_{CC} | $V_{ref_B} = V_{EN} = 5.5 \text{ V}$, $V_{ref_A} = 4.5 \text{ V}$ or 1 V , $I_O = 0$, $V_I = V_{CC}$ or GND | | | 1 | | μA |
| $C_{I(ref_A/B/EN)}$ | $V_I = 3 \text{ V}$ or 0 | | | 11 | | pF |
| $C_{io(off)}$ | $V_O = 3 \text{ V}$ or 0 , $V_{EN} = 0$ | | | 4.0 | 6.0 | pF |
| $C_{io(on)}$ | $V_O = 3 \text{ V}$ or 0 , $V_{EN} = 3 \text{ V}$ | | | 10.5 | 12.5 | pF |
| $r_{on}^{(2)}$ | $V_I = 0$, $I_O = 64 \text{ mA}$ | $V_{ref_A} = 3.3 \text{ V}$; $V_{ref_B} = V_{EN} = 5 \text{ V}$ | | 8.0 | | Ω |
| | | $V_{ref_A} = 1.8 \text{ V}$; $V_{ref_B} = V_{EN} = 5 \text{ V}$ | | 9.0 | | |
| | | $V_{ref_A} = 1.0 \text{ V}$; $V_{ref_B} = V_{EN} = 5 \text{ V}$ | | 10 | | |
| | $V_I = 0$, $I_O = 32 \text{ mA}$ | $V_{ref_A} = 1.8 \text{ V}$; $V_{ref_B} = V_{EN} = 5 \text{ V}$ | | 10 | | Ω |
| | | $V_{ref_A} = 2.5 \text{ V}$; $V_{ref_B} = V_{EN} = 5 \text{ V}$ | | 15 | | |
| | $V_I = 1.8 \text{ V}$, $I_O = 15 \text{ mA}$ | $V_{ref_A} = 3.3 \text{ V}$; $V_{ref_B} = V_{EN} = 5 \text{ V}$ | | 9.0 | | Ω |
| | $V_I = 1.0 \text{ V}$, $I_O = 10 \text{ mA}$ | $V_{ref_A} = 1.8 \text{ V}$; $V_{ref_B} = V_{EN} = 3.3 \text{ V}$ | | 18 | | Ω |
| | $V_I = 0 \text{ V}$, $I_O = 10 \text{ mA}$ | $V_{ref_A} = 1.0 \text{ V}$; $V_{ref_B} = V_{EN} = 3.3 \text{ V}$ | | 20 | | Ω |
| $V_I = 0 \text{ V}$, $I_O = 10 \text{ mA}$ | $V_{ref_A} = 1.0 \text{ V}$; $V_{ref_B} = V_{EN} = 1.8 \text{ V}$ | | 30 | | Ω | |

 (1) All typical values are at $T_A = 25^\circ\text{C}$.

(2) Measured by the voltage drop between the A and B pins at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) pins.

7.7 AC Performance (Translating Down) Switching Characteristics, $V_{GATE} = 3.3 \text{ V}$

 over recommended operating free-air temperature range, $V_{GATE} = 3.3 \text{ V}$, $V_{IH} = 3.3 \text{ V}$, $V_{IL} = 0$, and $V_M = 1.15 \text{ V}$ (unless otherwise noted) (see [Figure 2](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $C_L = 50 \text{ pF}$ | | $C_L = 30 \text{ pF}$ | | $C_L = 15 \text{ pF}$ | | UNIT |
|-----------|--------------|-------------|-----------------------|-----|-----------------------|-----|-----------------------|-----|------|
| | | | TYP | MAX | TYP | MAX | TYP | MAX | |
| t_{PLH} | A or B | B or A | 0.3 | | 0.2 | | 0.1 | | ns |
| t_{PHL} | | | 0.4 | | 0.3 | | 0.2 | | |

7.8 AC Performance (Translating Down) Switching Characteristics, $V_{GATE} = 2.5 \text{ V}$

 over recommended operating free-air temperature range, $V_{GATE} = 2.5 \text{ V}$, $V_{IH} = 2.5 \text{ V}$, $V_{IL} = 0$, and $V_M = 0.75 \text{ V}$ (unless otherwise noted) (see [Figure 2](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $C_L = 50 \text{ pF}$ | | $C_L = 30 \text{ pF}$ | | $C_L = 15 \text{ pF}$ | | UNIT |
|-----------|--------------|-------------|-----------------------|-----|-----------------------|-----|-----------------------|-----|------|
| | | | TYP | MAX | TYP | MAX | TYP | MAX | |
| t_{PLH} | A or B | B or A | 0.4 | | 0.3 | | 0.2 | | ns |
| t_{PHL} | | | 0.5 | | 0.4 | | 0.3 | | |

7.9 AC Performance (Translating Up) Switching Characteristics, $V_{GATE} = 3.3 V$

over recommended operating free-air temperature range, $V_{GATE} = 3.3 V$, $V_{IH} = 2.3 V$, $V_{IL} = 0$, $V_T = 3.3 V$, $V_M = 1.15 V$ and $R_L = 300$ (unless otherwise noted) (see Figure 2)

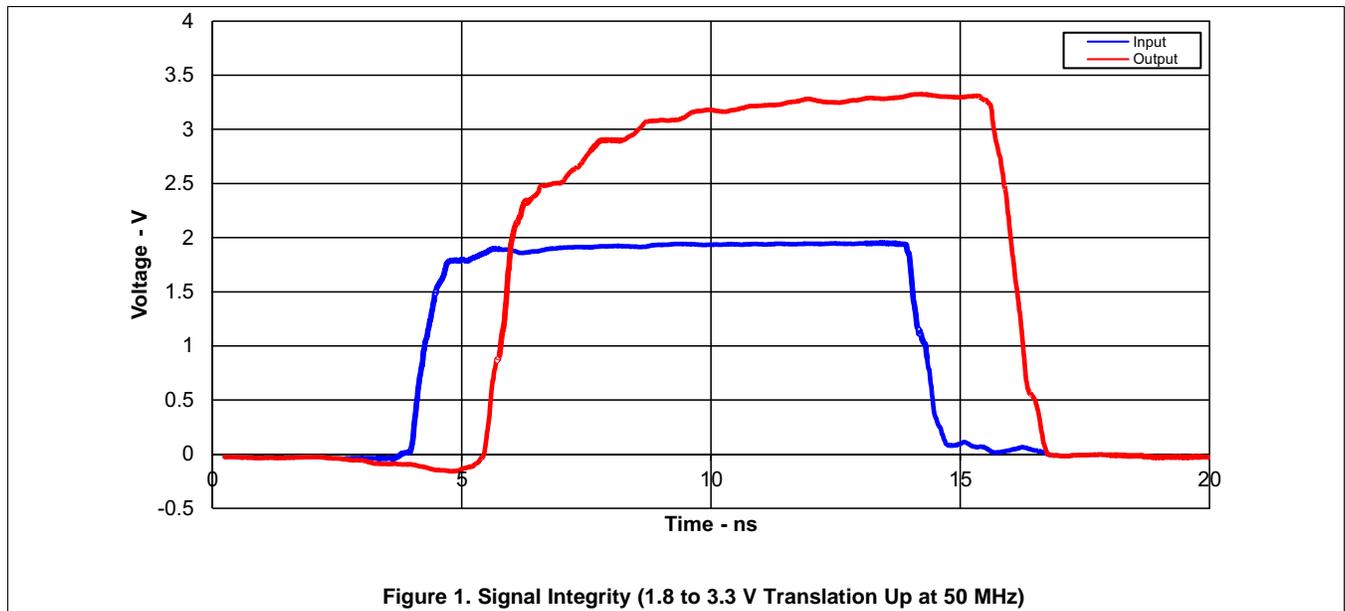
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $C_L = 50 pF$ | | $C_L = 30 pF$ | | $C_L = 15 pF$ | | UNIT |
|-----------|--------------|-------------|---------------|-----|---------------|-----|---------------|-----|------|
| | | | TYP | MAX | TYP | MAX | TYP | MAX | |
| t_{PLH} | A or B | B or A | 0.3 | | 0.2 | | 0.1 | | ns |
| t_{PHL} | | | 0.4 | | 0.3 | | 0.2 | | |

7.10 AC Performance (Translating Up) Switching Characteristics, $V_{GATE} = 2.5 V$

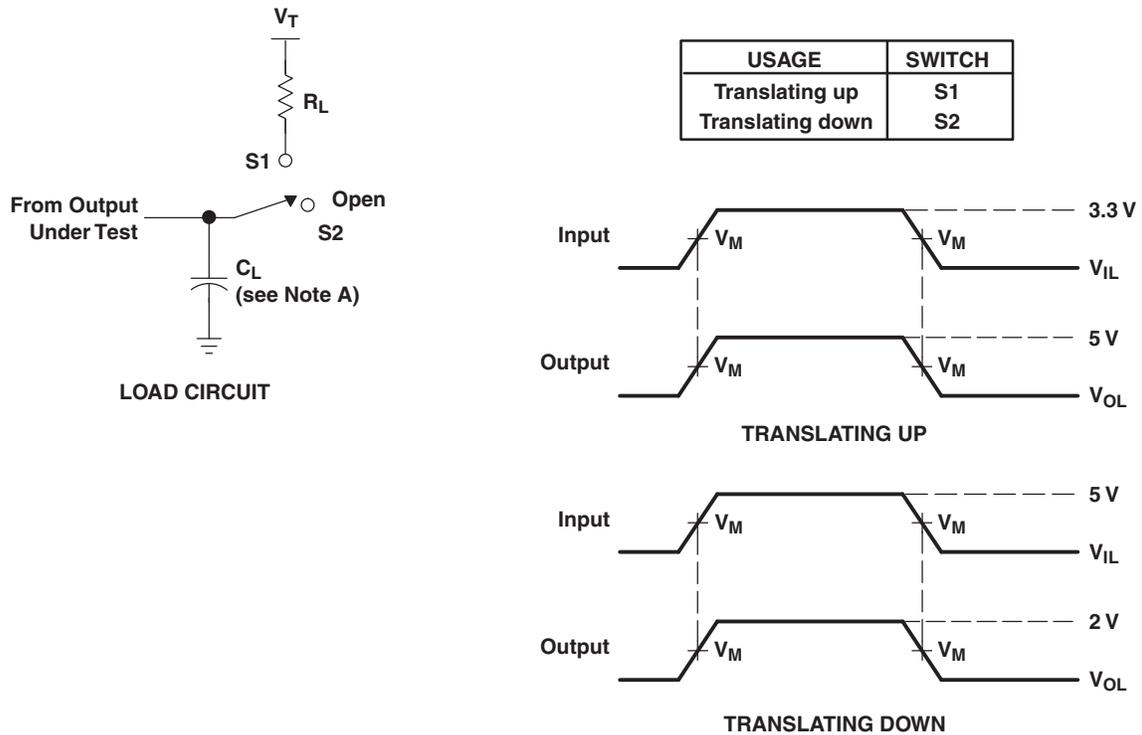
over recommended operating free-air temperature range, $V_{GATE} = 2.5 V$, $V_{IH} = 1.5 V$, $V_{IL} = 0$, $V_T = 2.5 V$, $V_M = 0.75 V$ and $R_L = 300$ (unless otherwise noted) (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $C_L = 50 pF$ | | $C_L = 30 pF$ | | $C_L = 15 pF$ | | UNIT |
|-----------|--------------|-------------|---------------|-----|---------------|-----|---------------|-----|------|
| | | | TYP | MAX | TYP | MAX | TYP | MAX | |
| t_{PLH} | A or B | B or A | 0.4 | | 0.3 | | 0.2 | | ns |
| t_{PHL} | | | 0.5 | | 0.4 | | 0.3 | | |

7.11 Typical Characteristics



8 Parameter Measurement Information



- NOTES:
- C_L includes probe and jig capacitance.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 - The outputs are measured one at a time, with one transition per measurement.

Figure 2. Load Circuit for Outputs

9 Detailed Description

9.1 Overview

The LSF family can be used in level translation applications for interfacing devices or systems operating at different interface voltages with one another. The LSF family is ideal for use in applications where an open-drain driver is connected to the data I/Os. With appropriate pullup resistors and layout, LSF can achieve 100 MHz. The LSF family can also be used in applications where a push-pull driver is connected to the data I/Os.

9.2 Functional Block Diagrams

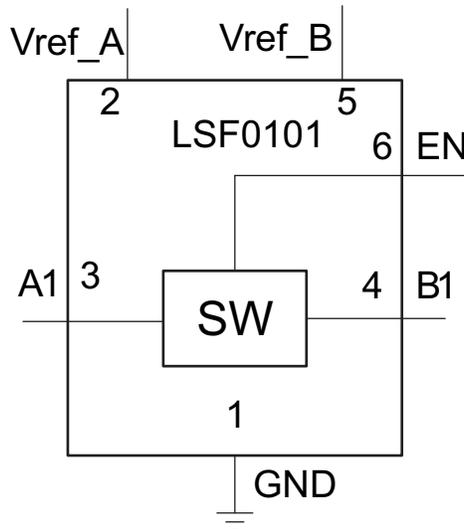


Figure 3. LSF0101 Functional Block Diagram

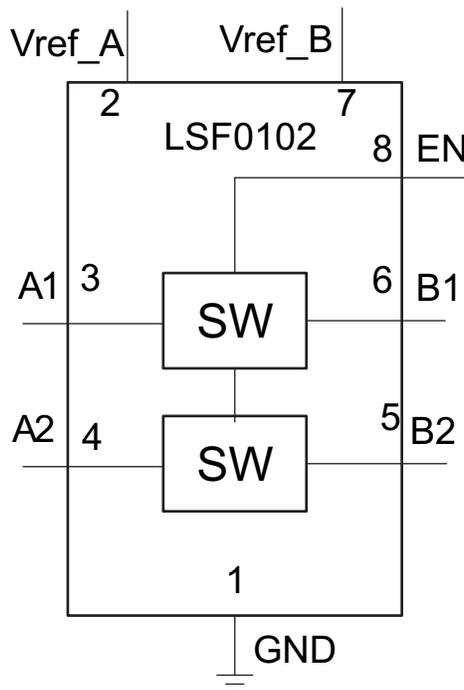
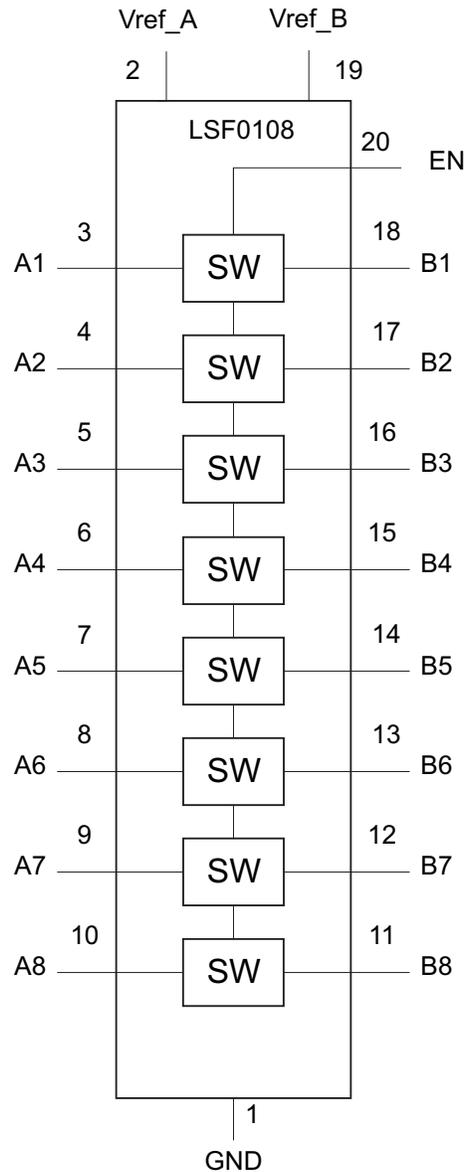


Figure 4. LSF0102 Functional Block Diagram

Functional Block Diagrams (continued)

Figure 5. LSF0108 Functional Block Diagram
9.3 Feature Description

- Supports high speed translation >100 MHz:
 - Allows the LSF family to support more consumer or telecom interfaces (MDIO or SDIO).
- Bidirectional voltage translation without DIR pin:
 - Minimizes system effort to develop voltage translation for bidirectional interface (PMBus, I²C, or SMBus).
- 5 V tolerance on IO port and 125°C support:
 - With 5 V tolerance and 125°C support, the LSF family is flexible and compliant with TTL levels in industrial and telecom applications.
- Channel specific translation:
 - The LSF family is able to set up different voltage translation levels on each channel.

9.4 Device Functional Modes

Table 1. Function Table

| INPUT EN ⁽¹⁾ PIN | FUNCTION |
|-----------------------------|----------|
| H | An = Bn |
| L | H-Z |

- (1) EN is controlled by V_{ref_B} logic levels and should be at least 1 V higher than V_{ref_A} for best translator.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

LSF is able to perform voltage translation for open-drain or push-pull interface. Table 2 provides some consumer/telecom interfaces as reference in regards to the different channel numbers that are supported by the LSF family.

Table 2. Voltage Translator for Consumer/Telecom Interface

| Part Name | Channel Number | Interface |
|-----------|----------------|---|
| LSF0101 | 1 | GPIO |
| LSF0102 | 2 | GPIO, MDIO, SMBus, PMBus, I ² C |
| LSF0108 | 8 | GPIO, MDIO, SDIO, SVID, UART, SMBus, PMBus, I ² C, SPI |

10.2 Typical Application

10.2.1 I²C PMBus, SMBus, GPIO

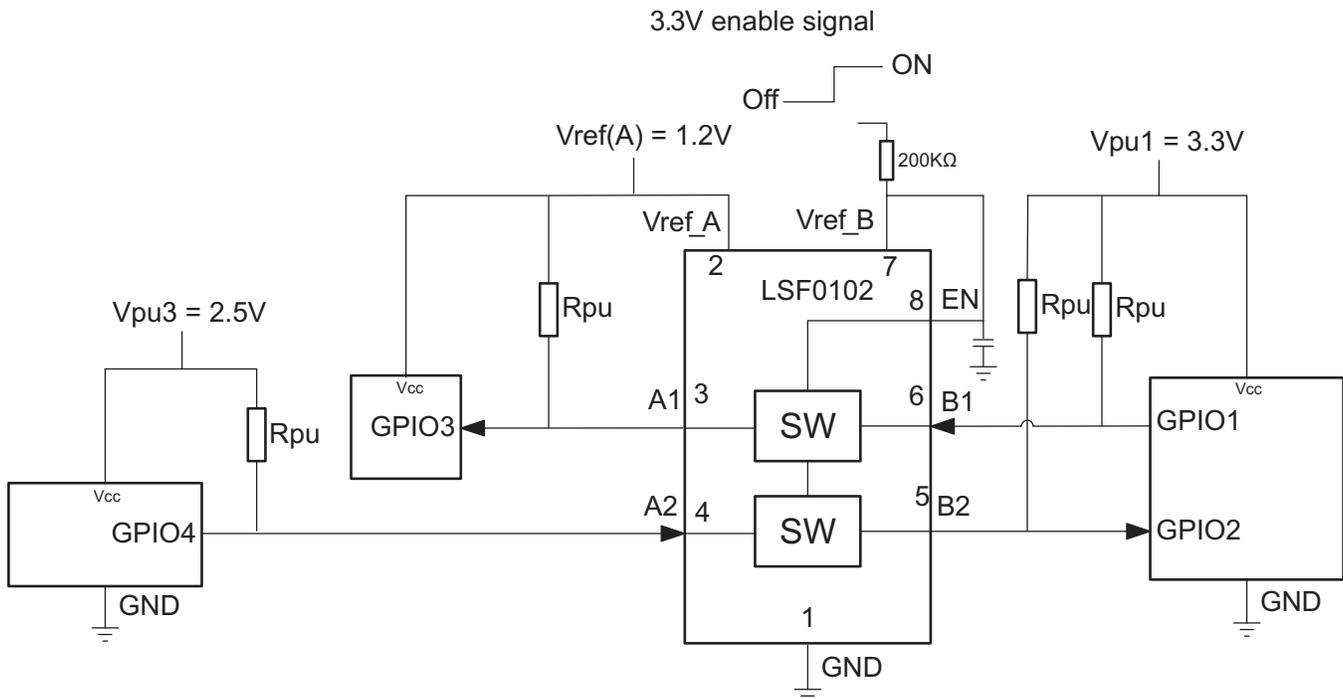


Figure 6. Bidirectional Translation to Multiple Voltage Levels

10.2.1.1 Design Requirements

10.2.1.1.1 Enable, Disable, and Reference Voltage Guidelines

The LSF family has an EN input that is used to disable the device by setting EN LOW, which places all I/Os in the high-impedance state. Since LSF family is switch-type voltage translator, the power consumption is very low. It is recommended to always enable LSF family for bidirectional application (I²C, SMBus, PMBus, or MDIO).

Typical Application (continued)
Table 3. Application Operating Condition

| PARAMETER | | MIN | TYP | MAX | UNIT |
|-----------------------|-------------------------|--------------|-----|--------|------|
| Vref_A ⁽¹⁾ | reference voltage (A) | 0.95 | | 4.5 | V |
| Vref_B | reference voltage (B) | Vref_A + 0.8 | | 5.5 | V |
| V _{I(EN)} | input voltage on EN pin | Vref_A + 0.8 | | 5.5 | V |
| V _{pu} | pullup supply voltage | 0 | | Vref_B | V |

(1) Vref_A have to be the lowest voltage level across all of inputs and outputs.

The 200 kΩ, pullup resistor is required to allow Vref_B to regulate the EN input. A filter capacitor on Vref_B is recommended. Also Vref_B and V_{I(EN)} are recommended to be at 1.0 V higher than Vref_A for best signal integrity.

10.2.1.2 Detailed Design Procedure
10.2.1.2.1 Bidirectional Translation

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to Vref_B and both pins pulled to HIGH side V_{pu} through a pullup resistor (typically 200 kΩ). This allows Vref_B to regulate the EN input. A filter capacitor on Vref_B is recommended. The master output driver can be push-pull or open-drain (pullup resistors may be required) and the slave device output can be push-pull or open-drain (pullup resistors are required to pull the Bn outputs to V_{pu}).

However, if either output is push-pull, data must be unidirectional or the outputs must be tri-state and be controlled by some direction-control mechanism to prevent HIGH-to-LOW contentions in either direction. If both outputs are open-drain, no direction control is needed.

In [Figure 6](#), the reference supply voltage (Vref_A) is connected to the processor core power supply voltage. When Vref_B is connected through a 200 kΩ resistor to a 3.3 V V_{pu} power supply, and Vref_A is set 1.0 V. The output of A3 and B4 has a maximum output voltage equal to Vref_A, and the bidirectional interface (Ch1/2, MDIO) has a maximum output voltage equal to V_{pu}.

10.2.1.2.2 Pullup Resistor Sizing

The pullup resistor value needs to limit the current through the pass transistor when it is in the ON state to about 15 mA. This ensures a pass voltage of 260 to 350 mV. If the current through the pass transistor is higher than 15 mA, the pass voltage also is higher in the ON state. To set the current through each pass transistor at 15 mA, to calculate the pullup resistor value use the following equation:

$$R_{pu} = (V_{pu} - 0.35 \text{ V}) / 0.015 \text{ A} \quad (1)$$

[Table 4](#) summarizes resistor values, reference voltages, and currents at 15, 10, and 3 mA. The resistor value shown in the +10% column (or a larger value) should be used to ensure that the pass voltage of the transistor is 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the LSF family device at 0.175 V, although the 15 mA applies only to current flowing through the LSF family device.

Table 4. Pullup Resistor Values⁽¹⁾⁽²⁾

| V _{DPU} | 15 mA | | 10 mA | | 3 mA | |
|------------------|-------------|-------------------------|-------------|-------------------------|-------------|-------------------------|
| | NOMINAL (Ω) | +10% ⁽³⁾ (Ω) | NOMINAL (Ω) | +10% ⁽³⁾ (Ω) | NOMINAL (Ω) | +10% ⁽³⁾ (Ω) |
| 5 V | 310 | 341 | 465 | 512 | 1550 | 1705 |
| 3.3 V | 197 | 217 | 295 | 325 | 983 | 1082 |
| 2.5 V | 143 | 158 | 215 | 237 | 717 | 788 |
| 1.8 V | 97 | 106 | 145 | 160 | 483 | 532 |
| 1.5 V | 77 | 85 | 115 | 127 | 383 | 422 |
| 1.2 V | 57 | 63 | 85 | 94 | 283 | 312 |

(1) Calculated for V_{OL} = 0.35 V

(2) Assumes output driver V_{OL} = 0.175 V at stated current

(3) +10% to compensate for V_{DD} range and resistor tolerance

10.2.1.2.3 LSF Family Bandwidth

The maximum frequency of the LSF family is dependent on the application. The device can operate at speeds of >100 MHz given the correct conditions. The maximum frequency is dependent upon the loading of the application. The LSF family behaves like a standard switch where the bandwidth of the device is dictated by the on resistance and on capacitance of the device.

Figure 7 shows a bandwidth measurement of the LSF family using a two-port network analyzer.

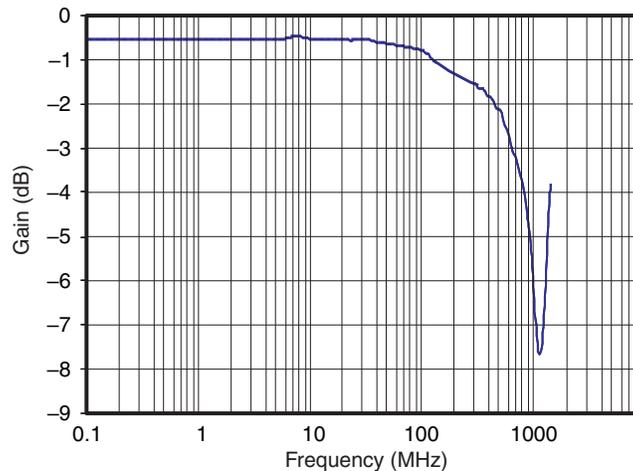


Figure 7. 3-dB Bandwidth

The 3-dB point of the LSF family is ≈ 600 MHz; however, this measurement is an analog type of measurement. For digital applications the signal should not degrade up to the fifth harmonic of the digital signal. The frequency bandwidth should be at least five times the maximum digital clock rate. This component of the signal is very important in determining the overall shape of the digital signal. In the case of the LSF family, a digital clock frequency of greater than 100 MHz can be achieved.

The LSF family does not provide any drive capability. Therefore higher frequency applications will require higher drive strength from the host side. No pullup resistor is needed on the host side (3.3 V) if the LSF family is being driven by standard CMOS totem pole output driver. Ideally, it is best to minimize the trace length from the LSF family on the sink side (1.8 V) to minimize signal degradation.

All fast edges have an infinite spectrum of frequency components; however, there is an inflection (or knee) in the frequency spectrum of fast edges where frequency components higher than f_{knee} are insignificant in determining the shape of the signal.

To calculate the maximum practical frequency component, or the knee frequency (f_{knee}), use the following equations:

$$f_{knee} = 0.5 / RT \text{ (10 – 80\%)} \tag{2}$$

$$f_{knee} = 0.4 / RT \text{ (20 – 80\%)} \tag{3}$$

For signals with rise time characteristics based on 10- to 90-percent thresholds, f_{knee} is equal to 0.5 divided by the rise time of the signal. For signals with rise time characteristics based on 20% to 80% thresholds, which is very common in many of today's device specifications, f_{knee} is equal to 0.4 divided by the rise time of the signal.

Some guidelines to follow that will help maximize the performance of the device:

- Keep trace length to a minimum by placing the LSF family close to the I²C output of the processor.
- The trace length should be less than half the time of flight to reduce ringing and line reflections or non-monotonic behavior in the switching region.
- To reduce overshoots, a pullup resistor can be added on the 1.8 V side; be aware that a slower fall time is to be expected.

10.2.1.3 Application Curve

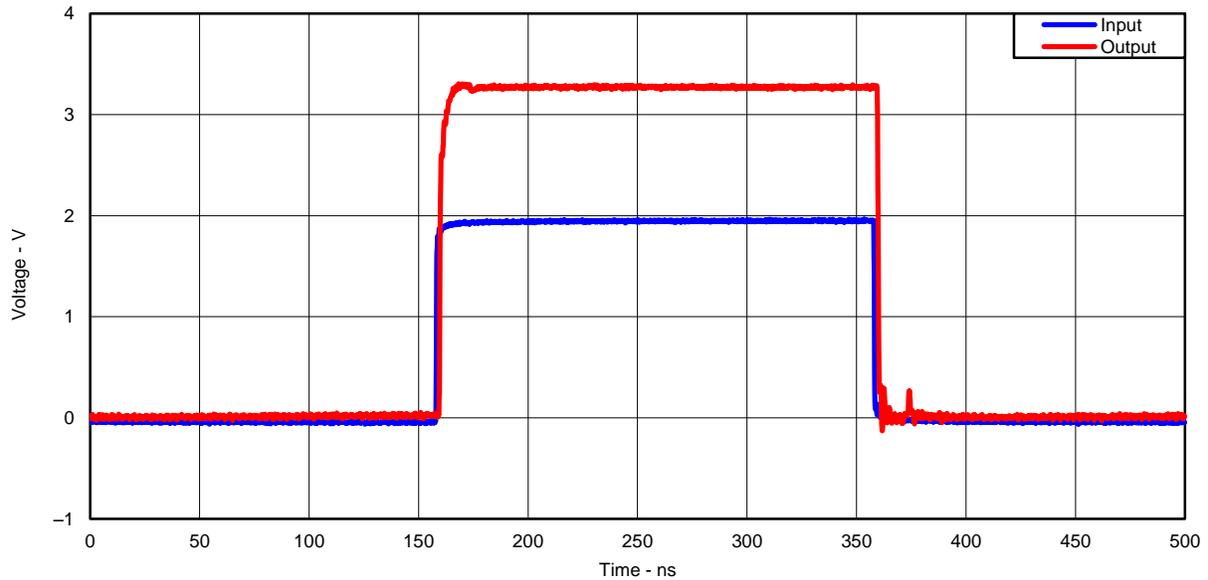


Figure 8. Captured Waveform From Above I²C Set-Up (1.8 to 3.3 V at 2.5 MHz)

10.2.2 MDIO

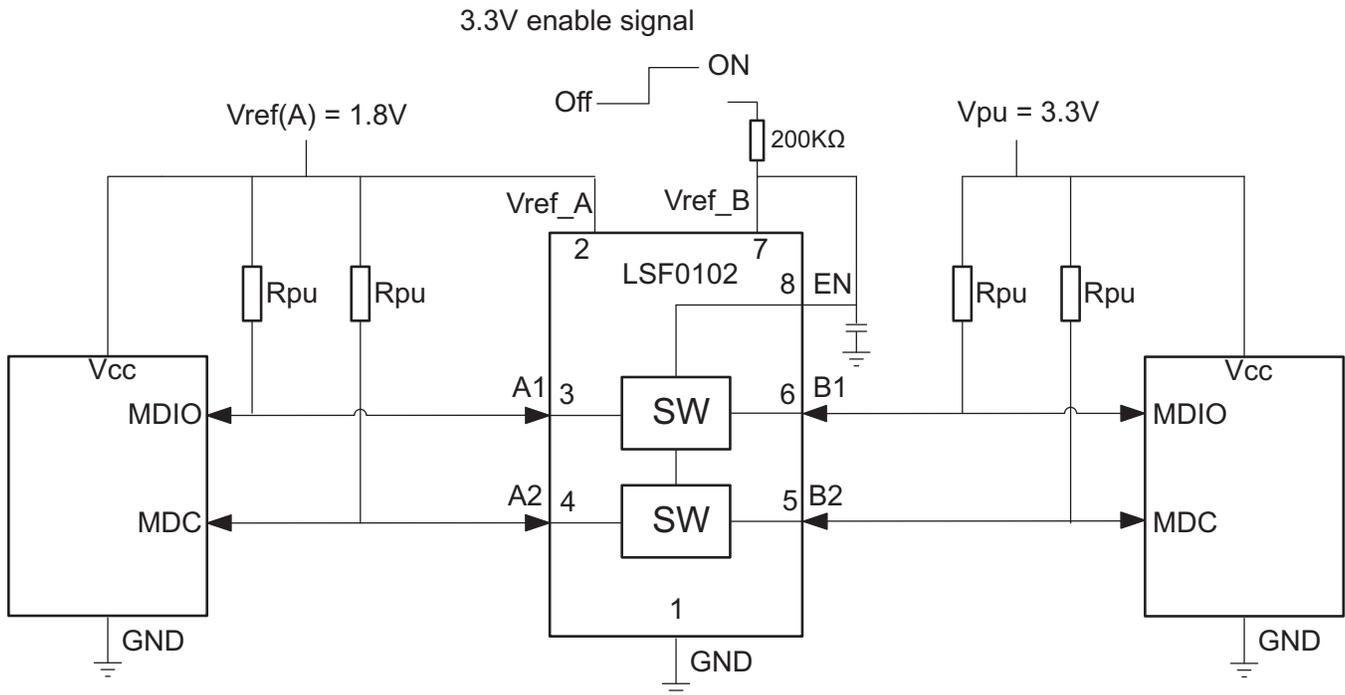


Figure 9. Typical Application Circuit (MDIO/Bidirectional Interface)

10.2.2.1 Design Requirements

Refer to [Design Requirements](#).

10.2.2.2 Detailed Design Procedure

Refer to [Detailed Design Procedure](#).

10.2.2.3 Application Curve

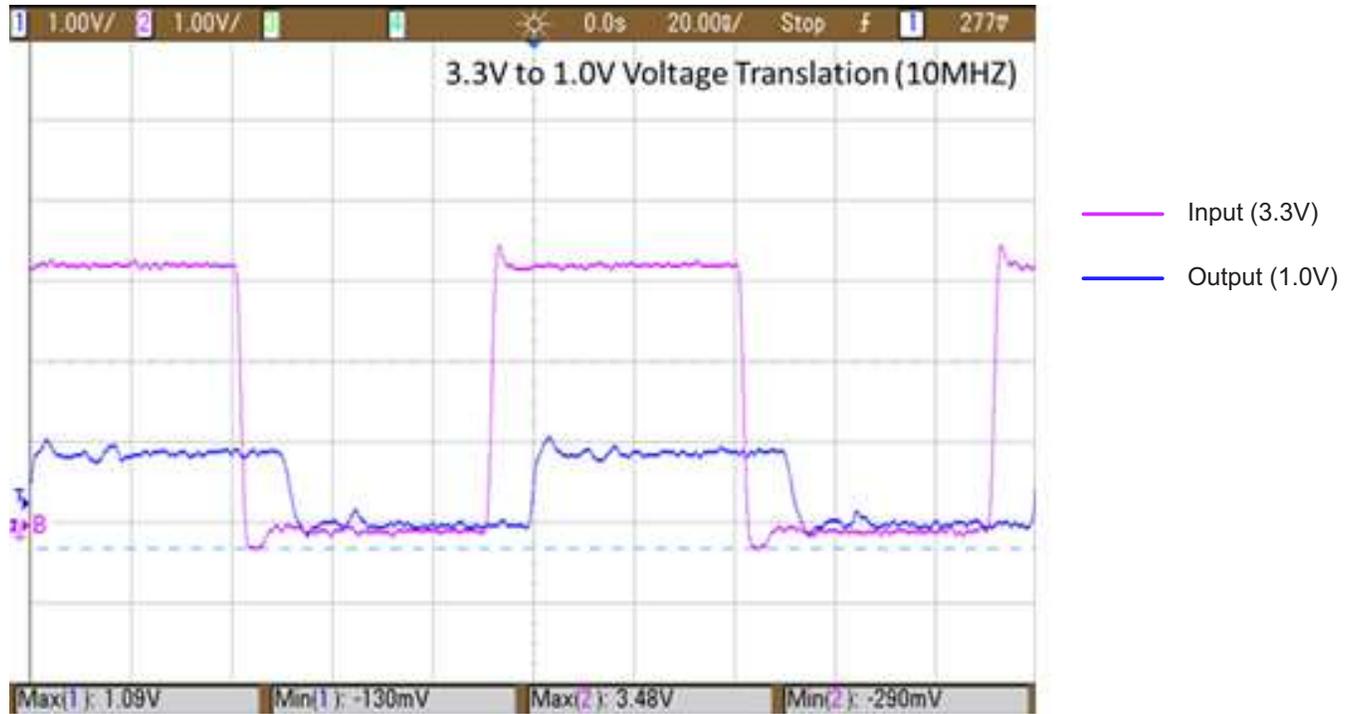
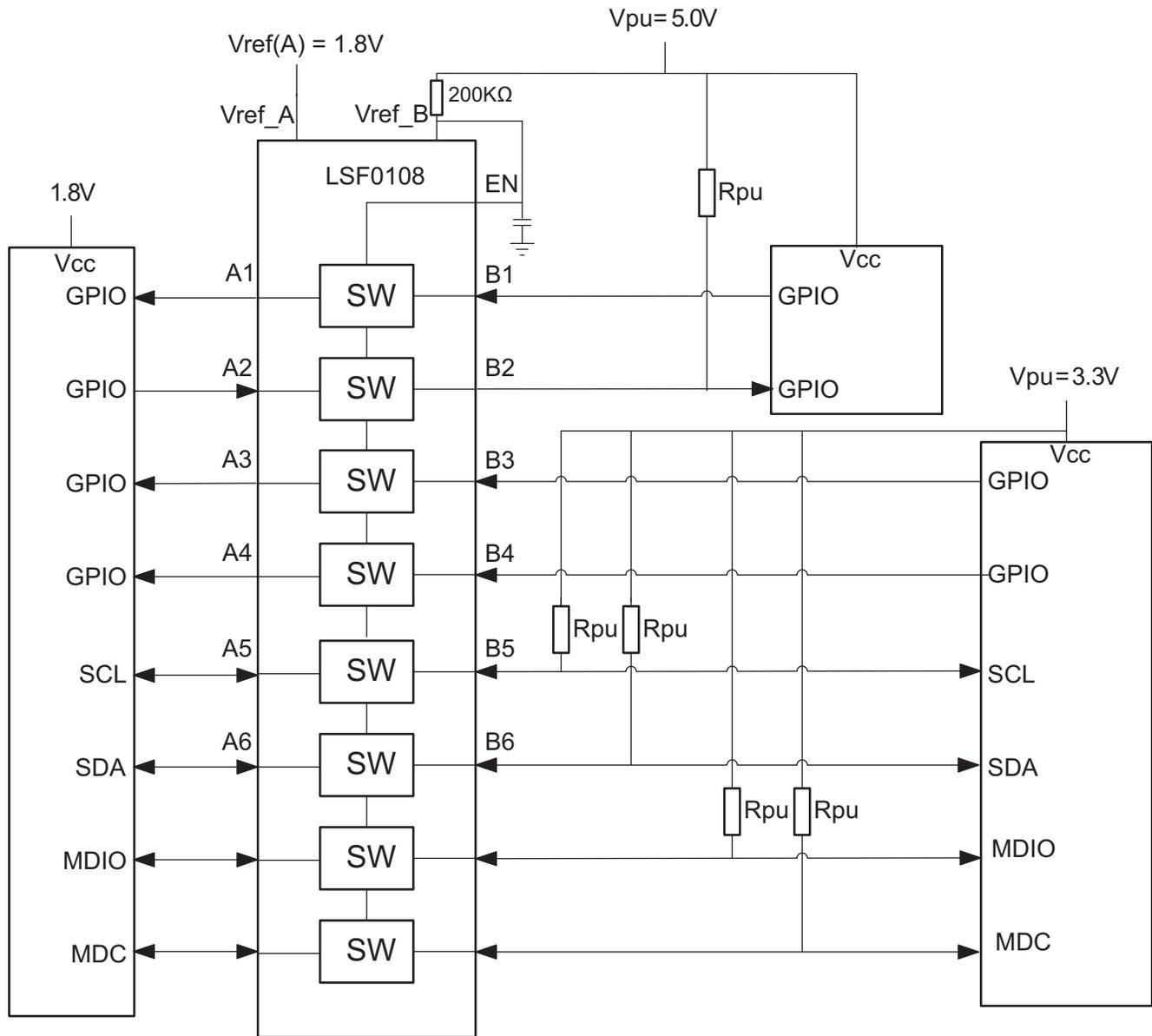


Figure 10. Captured Waveform From Above MDIO Setup

10.2.3 Multiple Voltage Translation in Single Device



10.2.3.1 Design Requirements

Refer to [Design Requirements](#).

10.2.3.2 Detailed Design Procedure

Refer to [Detailed Design Procedure](#).

10.2.3.3 Application Curve

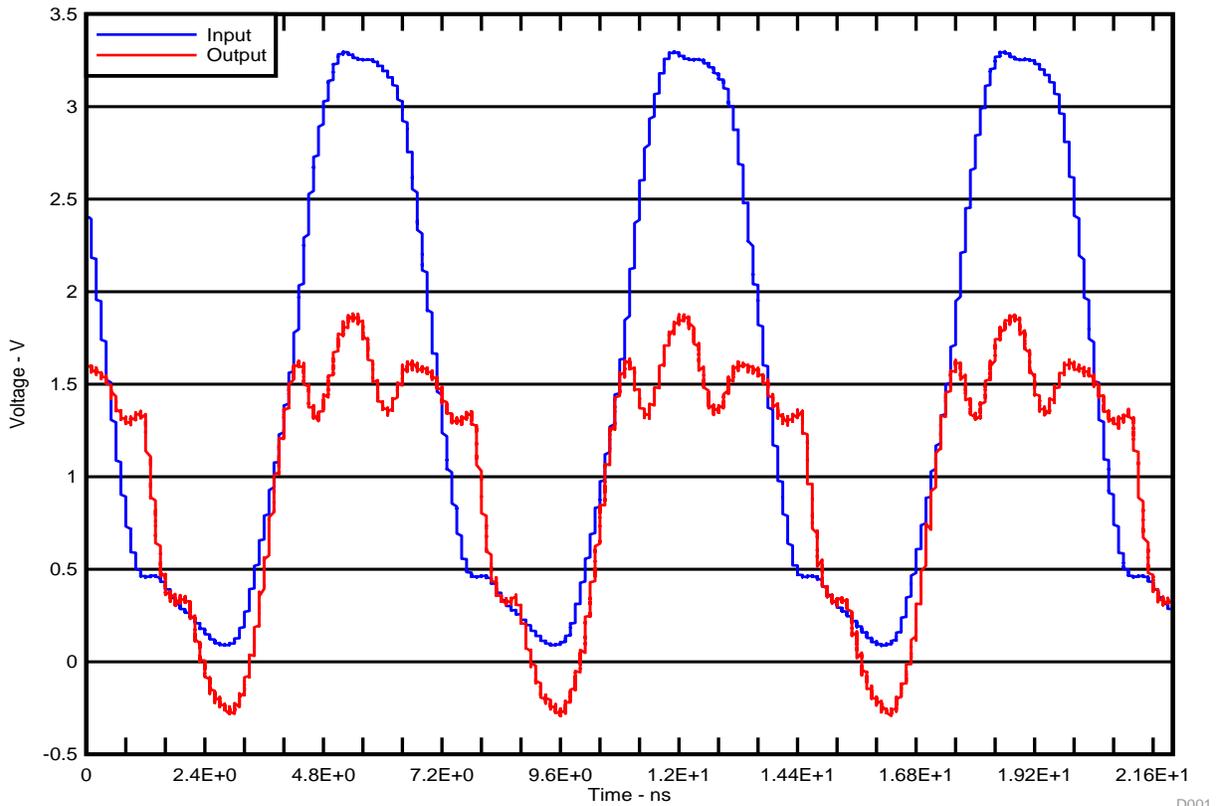


Figure 11. Translation Down (3.3 to 1.8 V) at 150 MHz

D001

11 Power Supply Recommendations

There are no power sequence requirements for the LSF family. For enable and reference voltage guidelines, please refer to the [Enable, Disable, and Reference Voltage Guidelines](#).

12 Layout

12.1 Layout Guidelines

Because the LSF family is a switch-type level translator, the signal integrity is highly related with a pullup resistor and PCB capacitance condition.

- Short signal trace as possible to reduce capacitance and minimize stub from pullup resistor.
- Place LSF close to high voltage side.
- Select the appropriate pullup resistor that applies to translation levels and driving capability of transmitter.

12.2 Layout Example

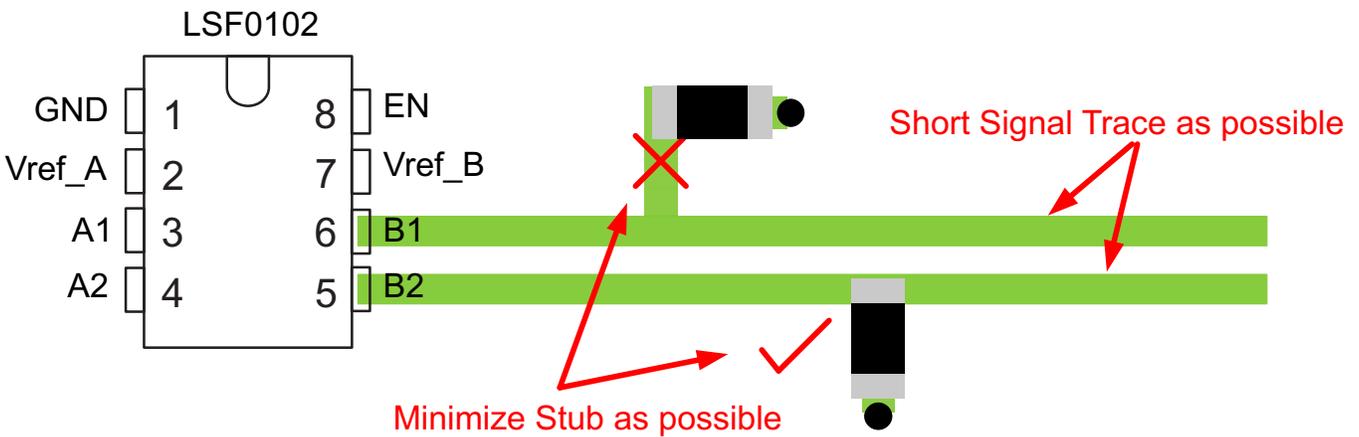


Figure 12. Short Trace Layout

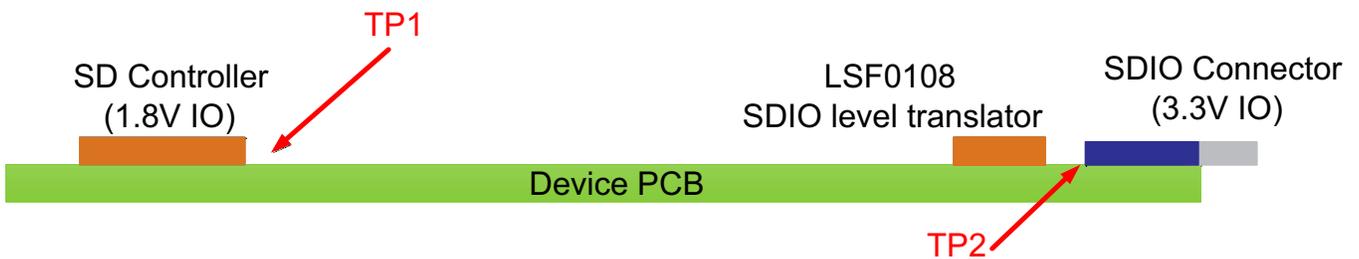
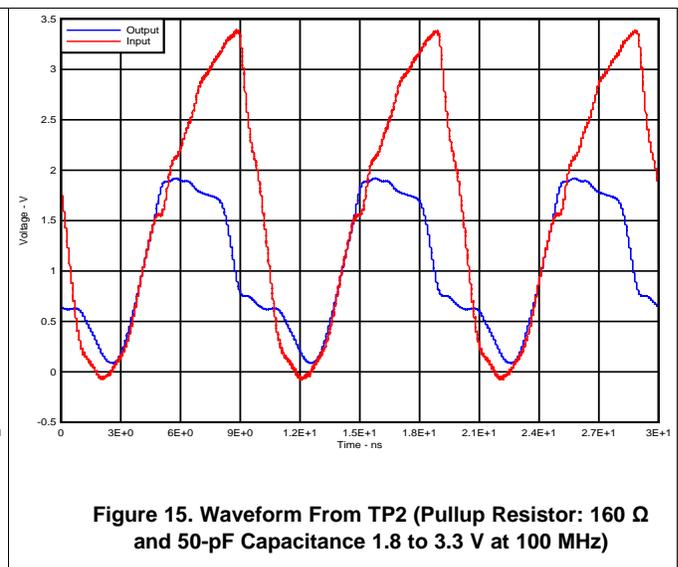
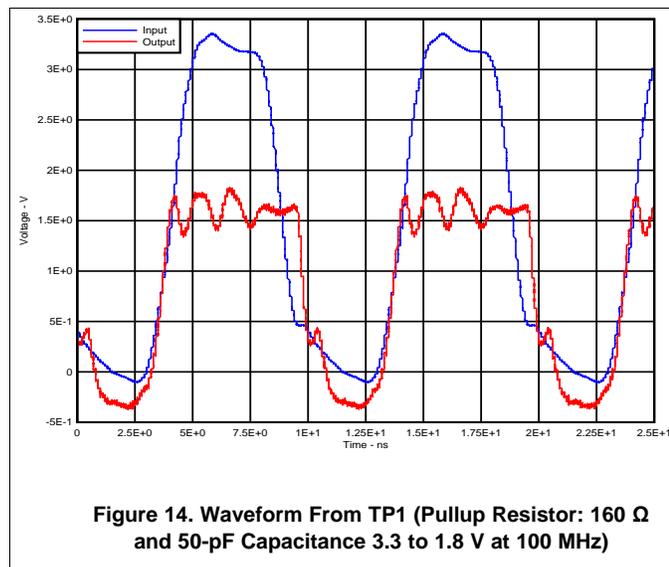


Figure 13. Device Placement

Layout Example (continued)


13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| LSF0101 | Click here |
| LSF0102 | Click here |
| LSF0108 | Click here |

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|--------------------------|-------------------------|
| LSF0101DRYR | ACTIVE | SON | DRY | 6 | 5000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VD | Samples |
| LSF0102DCTR | ACTIVE | SM8 | DCT | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | NG2 Y | Samples |
| LSF0102DCUR | ACTIVE | US8 | DCU | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -40 to 125 | (G2 ~ NG2P ~ NG2S) NY | Samples |
| LSF0102DQER | ACTIVE | X2SON | DQE | 8 | 5000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | RV | Samples |
| LSF0102YZTR | ACTIVE | DSBGA | YZT | 8 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | RV | Samples |
| LSF0108PWR | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LSF0108 | Samples |
| LSF0108RKS | ACTIVE | VQFN | RKS | 20 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LSF0108 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

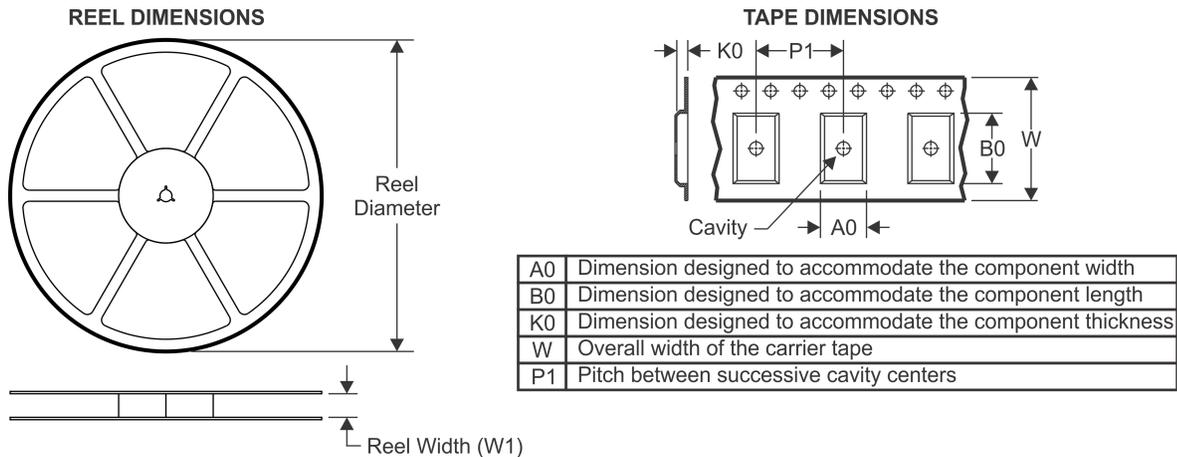
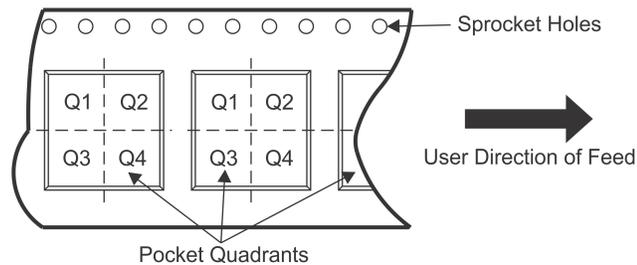
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

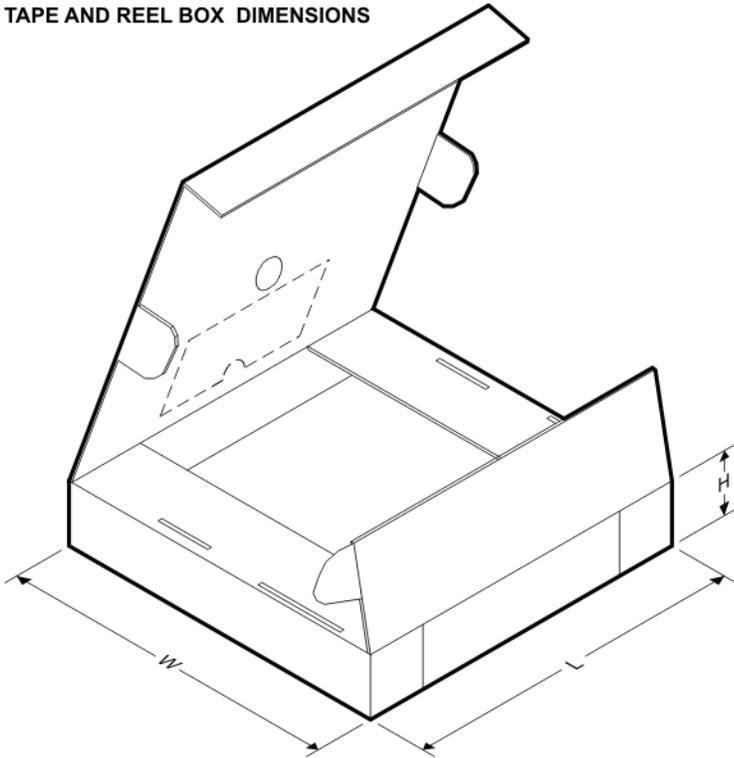
Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LSF0101DRYR | SON | DRY | 6 | 5000 | 180.0 | 9.5 | 1.15 | 1.6 | 0.75 | 4.0 | 8.0 | Q1 |
| LSF0102DCTR | SM8 | DCT | 8 | 3000 | 180.0 | 13.0 | 3.35 | 4.5 | 1.55 | 4.0 | 12.0 | Q3 |
| LSF0102DCUR | US8 | DCU | 8 | 3000 | 180.0 | 8.4 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| LSF0102DCUR | US8 | DCU | 8 | 3000 | 178.0 | 9.5 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| LSF0102DCUR | US8 | DCU | 8 | 3000 | 180.0 | 9.0 | 2.05 | 3.3 | 1.0 | 4.0 | 8.0 | Q3 |
| LSF0102DQER | X2SON | DQE | 8 | 5000 | 180.0 | 9.5 | 1.15 | 1.6 | 0.5 | 4.0 | 8.0 | Q1 |
| LSF0102YZTR | DSBGA | YZT | 8 | 3000 | 180.0 | 8.4 | 1.02 | 2.02 | 0.75 | 4.0 | 8.0 | Q1 |
| LSF0108PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| LSF0108RKSR | VQFN | RKS | 20 | 3000 | 177.8 | 12.4 | 2.73 | 4.85 | 1.03 | 4.0 | 12.0 | Q1 |

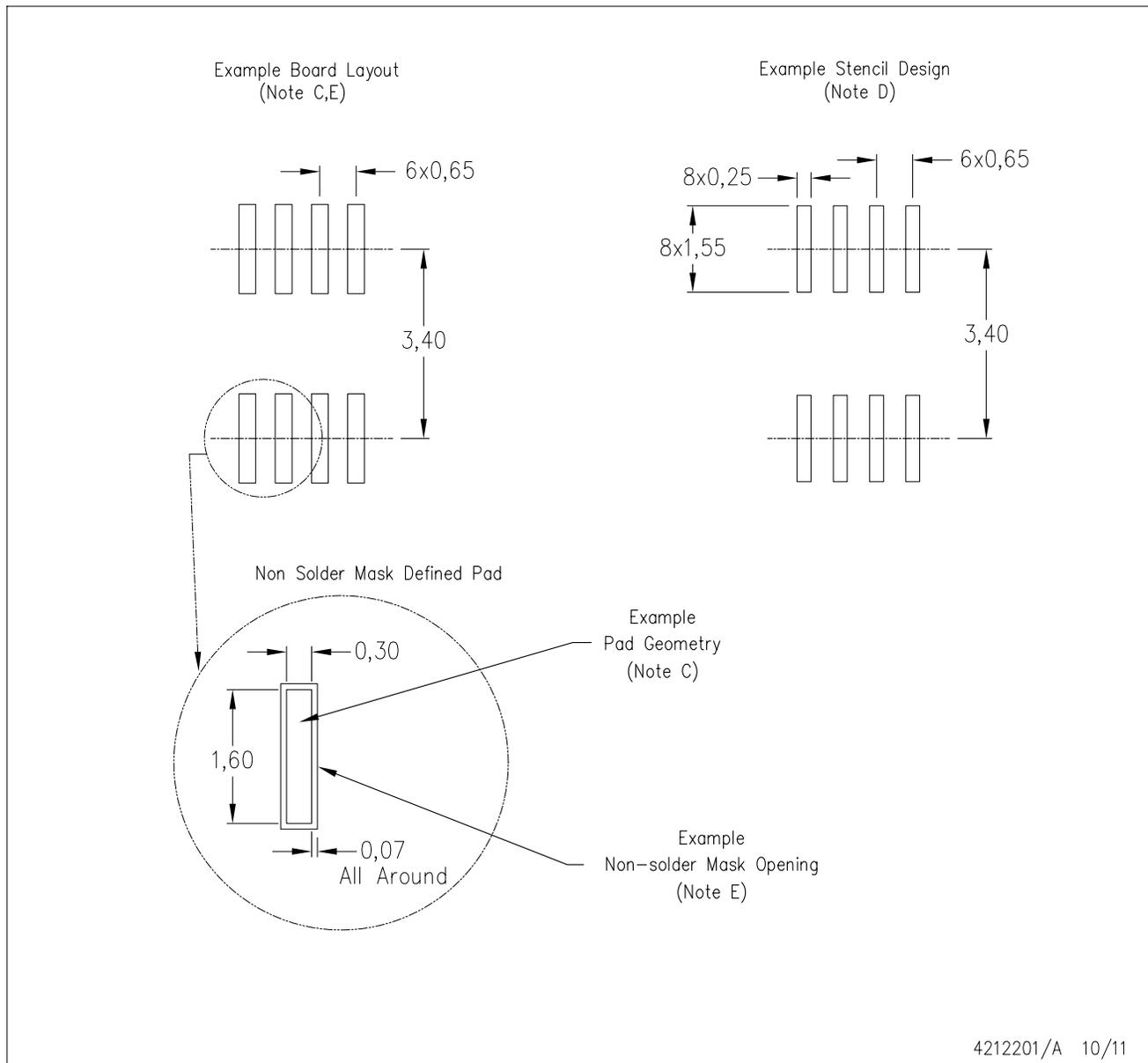
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LSF0101DRYR | SON | DRY | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| LSF0102DCTR | SM8 | DCT | 8 | 3000 | 182.0 | 182.0 | 20.0 |
| LSF0102DCUR | US8 | DCU | 8 | 3000 | 202.0 | 201.0 | 28.0 |
| LSF0102DCUR | US8 | DCU | 8 | 3000 | 202.0 | 201.0 | 28.0 |
| LSF0102DCUR | US8 | DCU | 8 | 3000 | 182.0 | 182.0 | 20.0 |
| LSF0102DQER | X2SON | DQE | 8 | 5000 | 184.0 | 184.0 | 19.0 |
| LSF0102YZTR | DSBGA | YZT | 8 | 3000 | 182.0 | 182.0 | 17.0 |
| LSF0108PWR | TSSOP | PW | 20 | 2000 | 364.0 | 364.0 | 27.0 |
| LSF0108RKSR | VQFN | RKS | 20 | 3000 | 202.0 | 201.0 | 28.0 |

DCT (R-PDSO-G8)

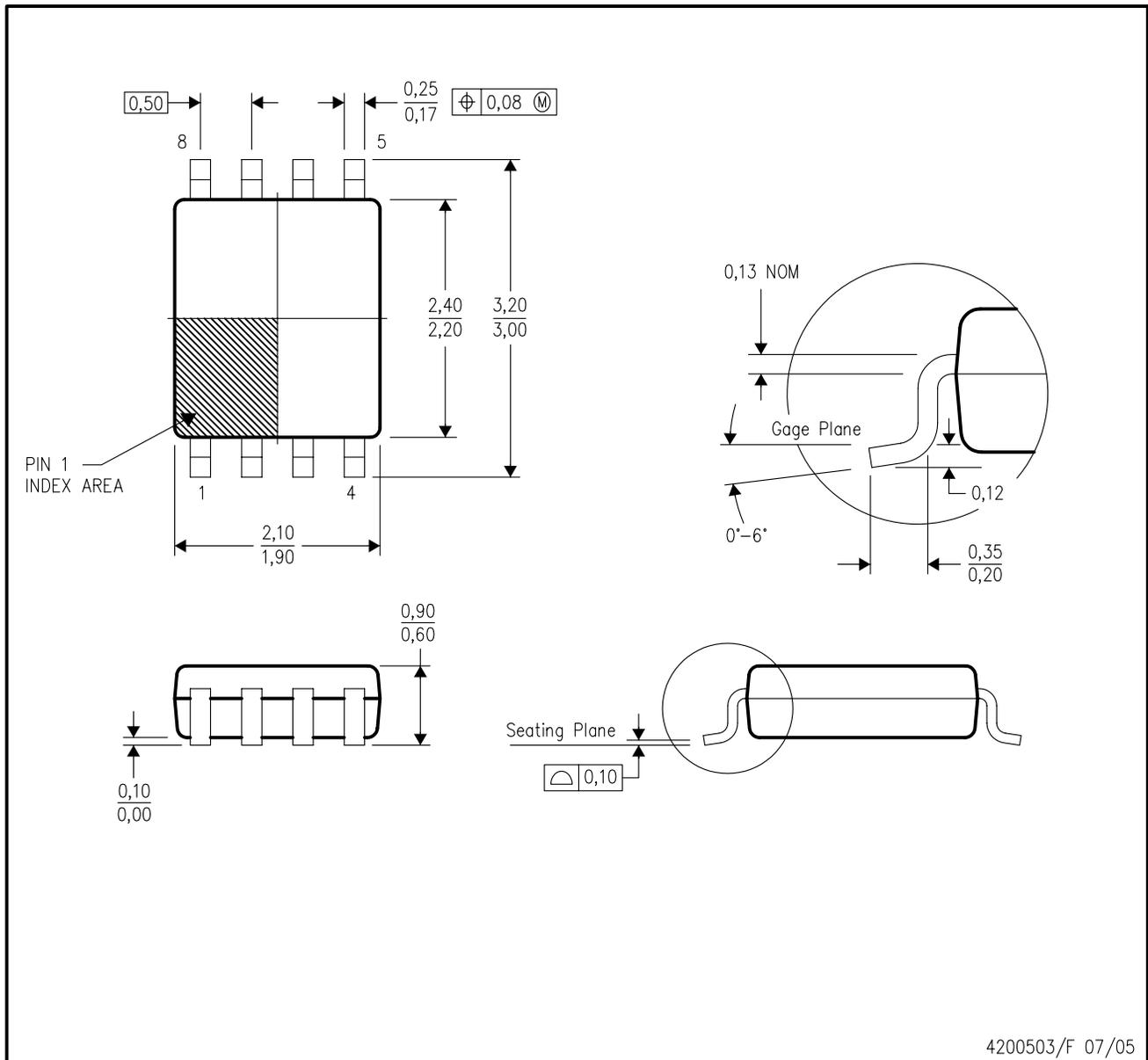
PLASTIC SMALL OUTLINE



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Publication IPC-7351 is recommended for alternate designs.
 D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
 E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DCU (R-PDSO-G8)

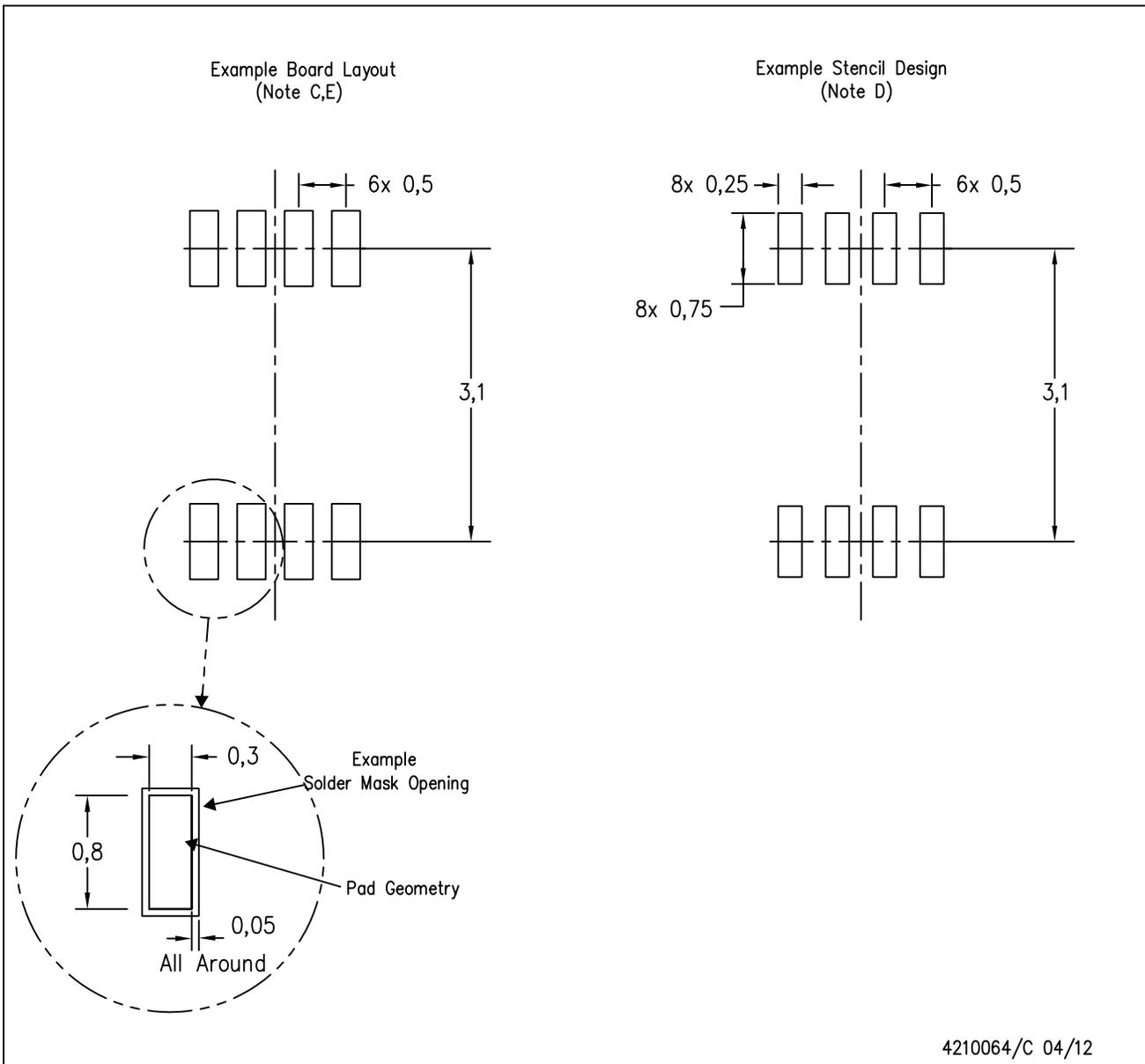
PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-187 variation CA.

DCU (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)

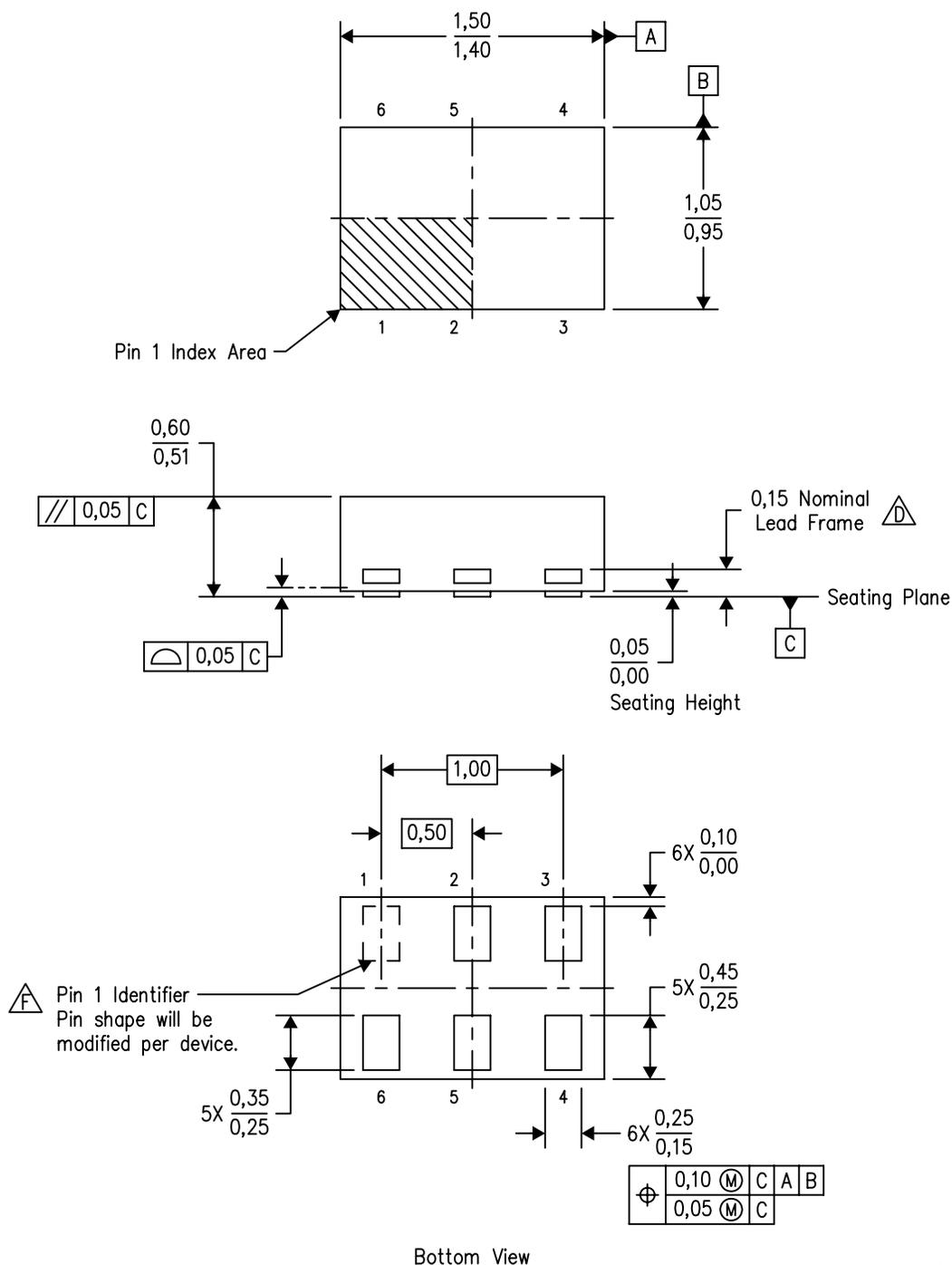


4210064/C 04/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DRY (R-PUSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD

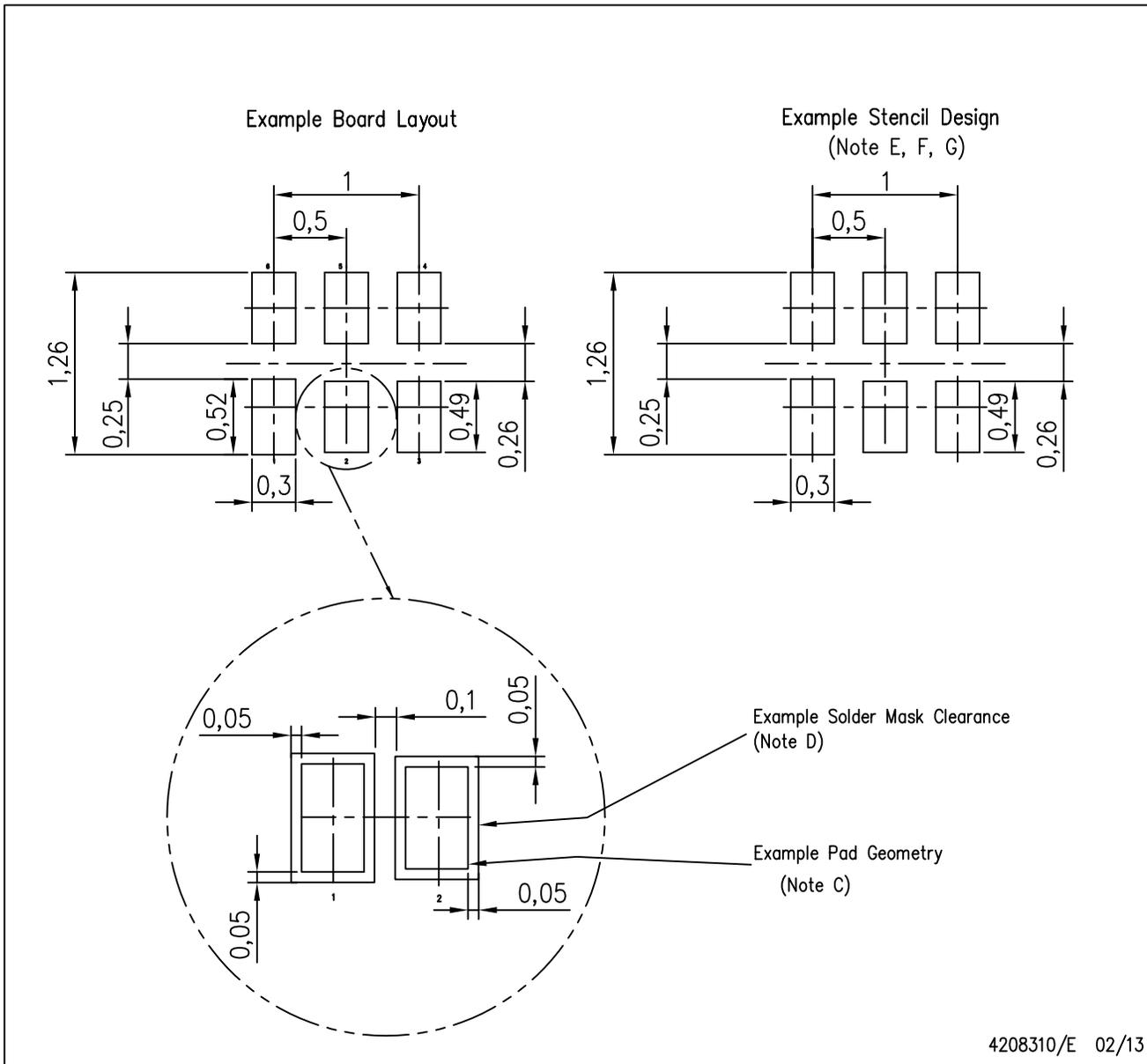


4207181/F 12/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. SON (Small Outline No-Lead) package configuration.
 - $\triangle D$ The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
 - E. This package complies to JEDEC MO-287 variation UFAD.
 - $\triangle F$ See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (R-PUSON-N6)

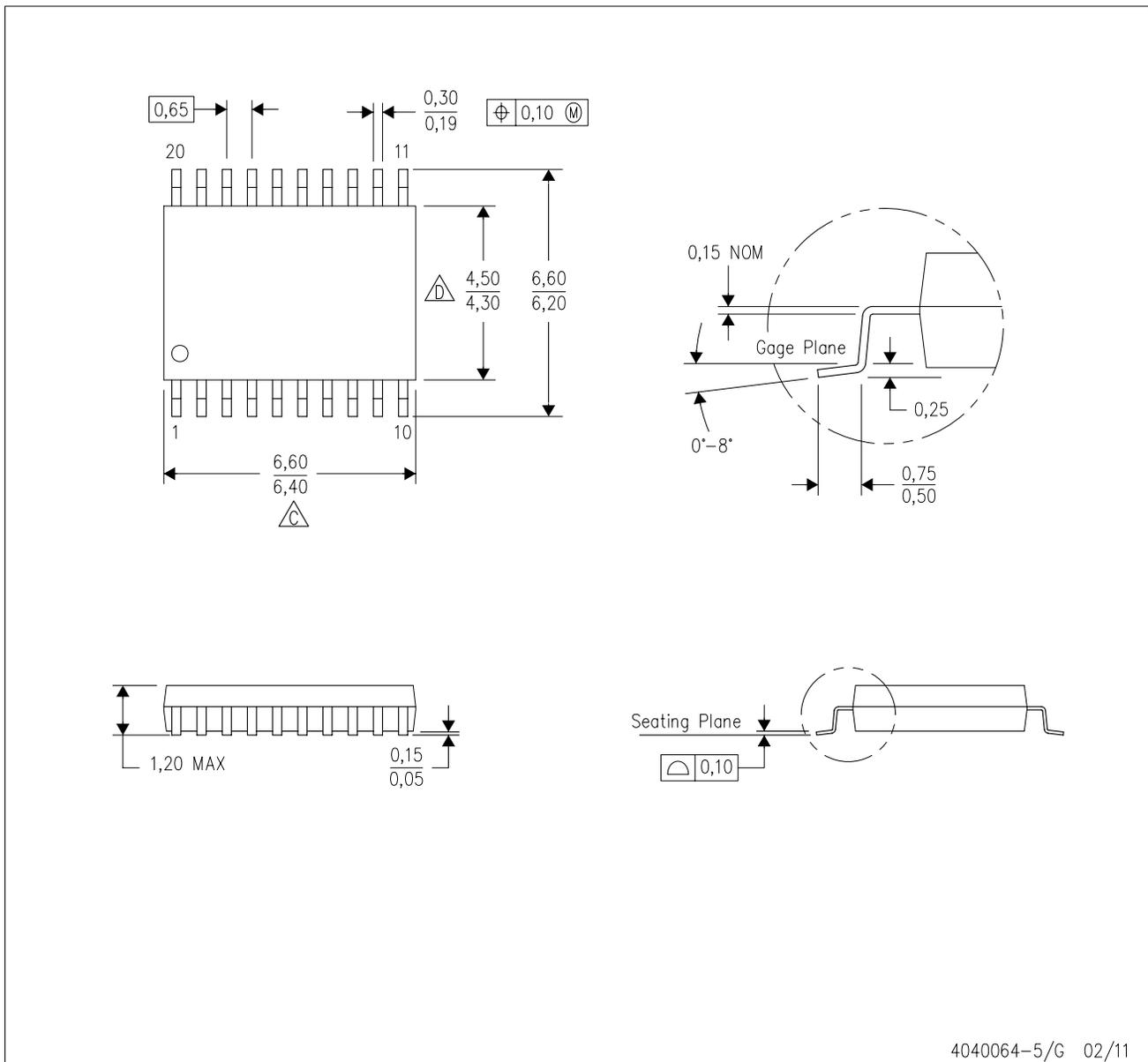
PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

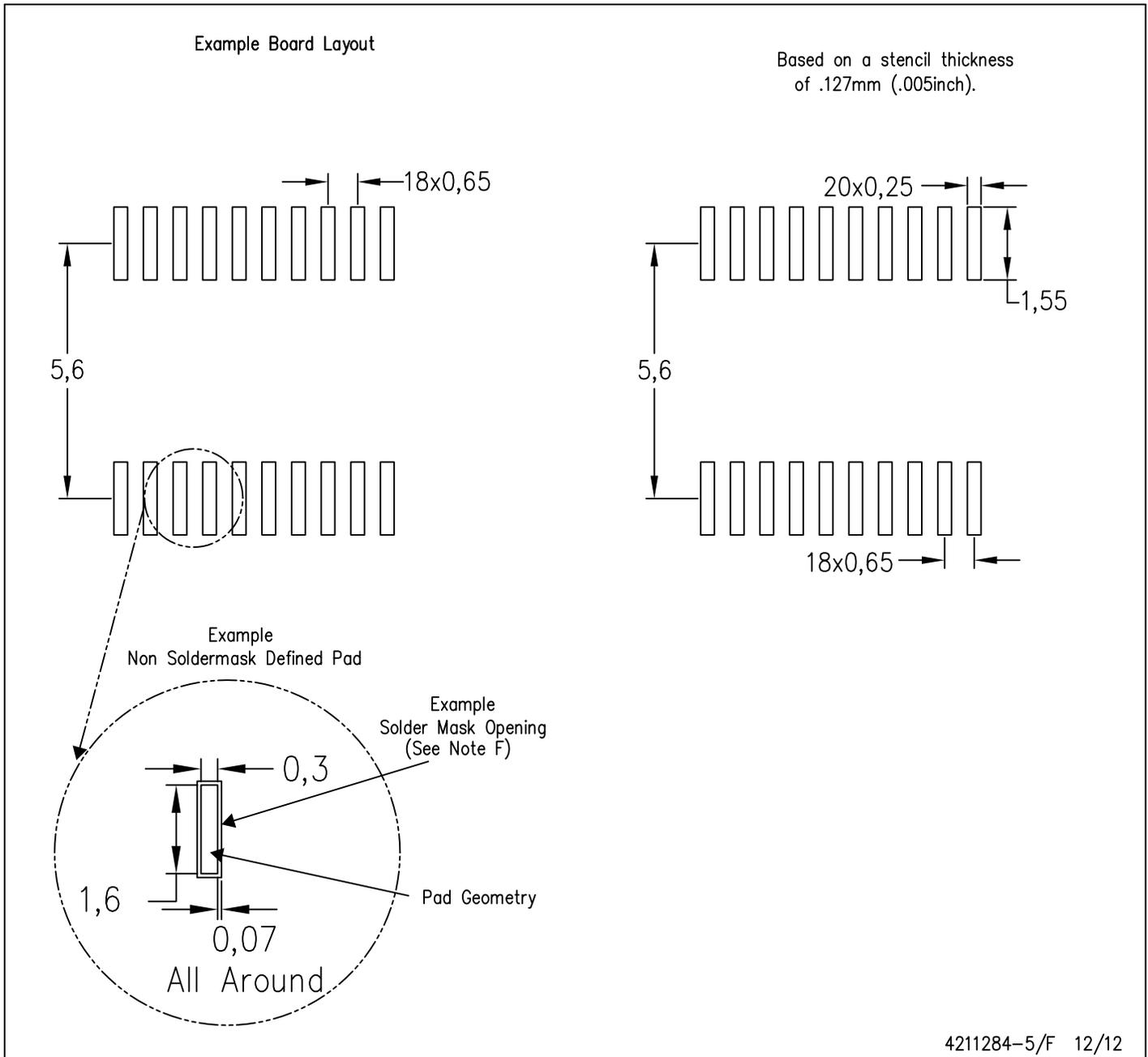


4040064-5/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

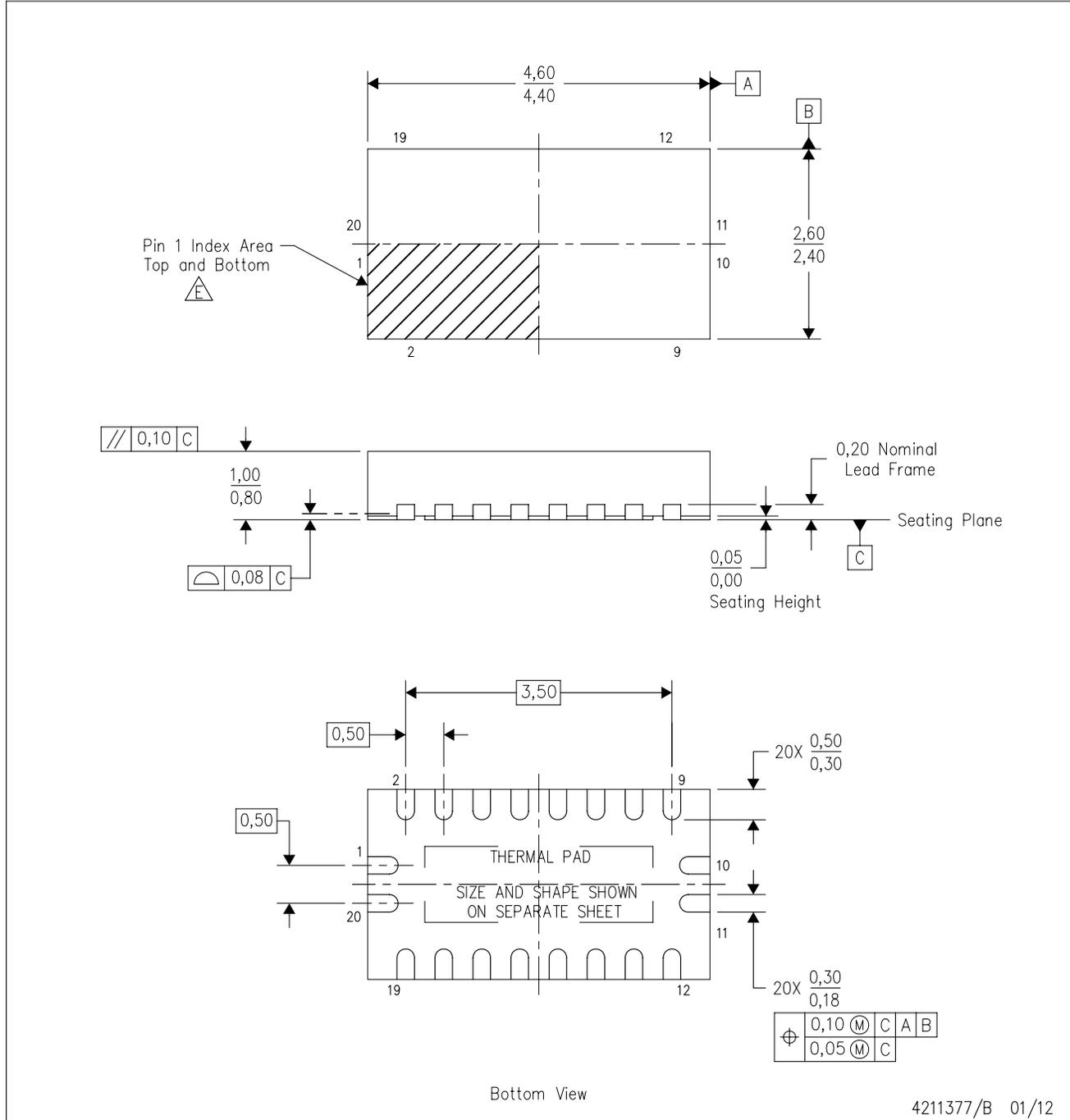
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RKS (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- △ Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

THERMAL PAD MECHANICAL DATA

RKS (R-PVQFN-N20)

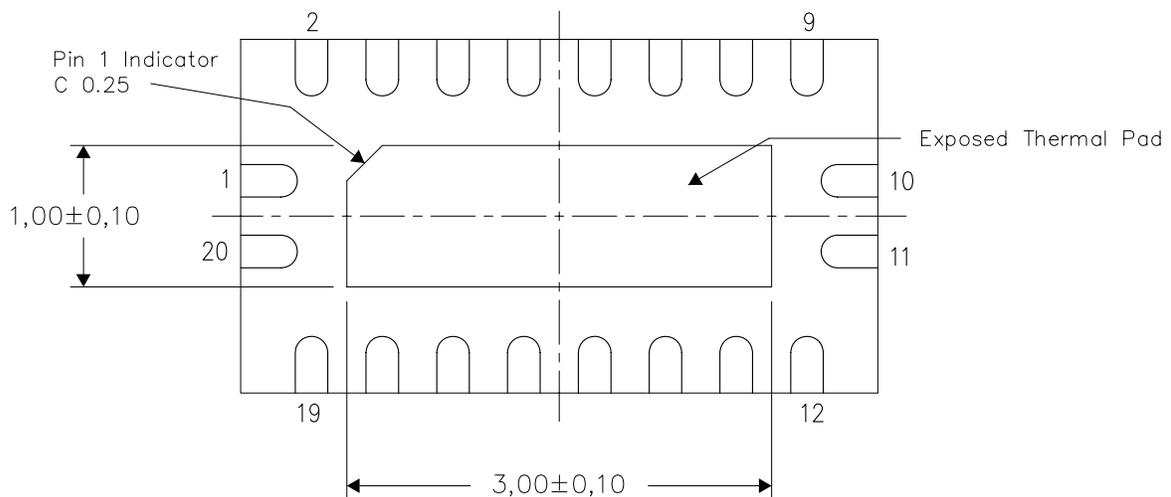
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

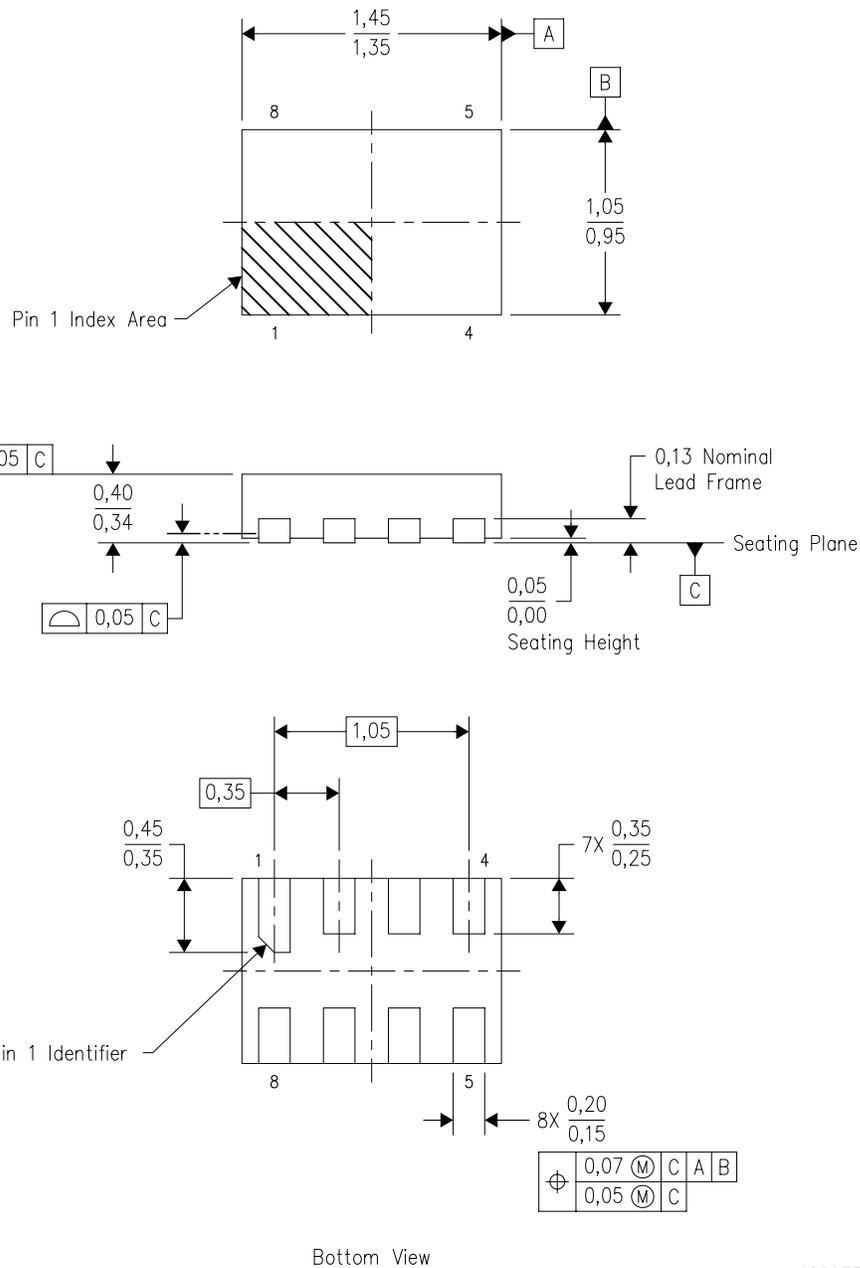
Exposed Thermal Pad Dimensions

4211394/B 01/12

NOTE: All linear dimensions are in millimeters

DQE (R-PX2SON-N8)

PLASTIC SMALL OUTLINE NO-LEAD

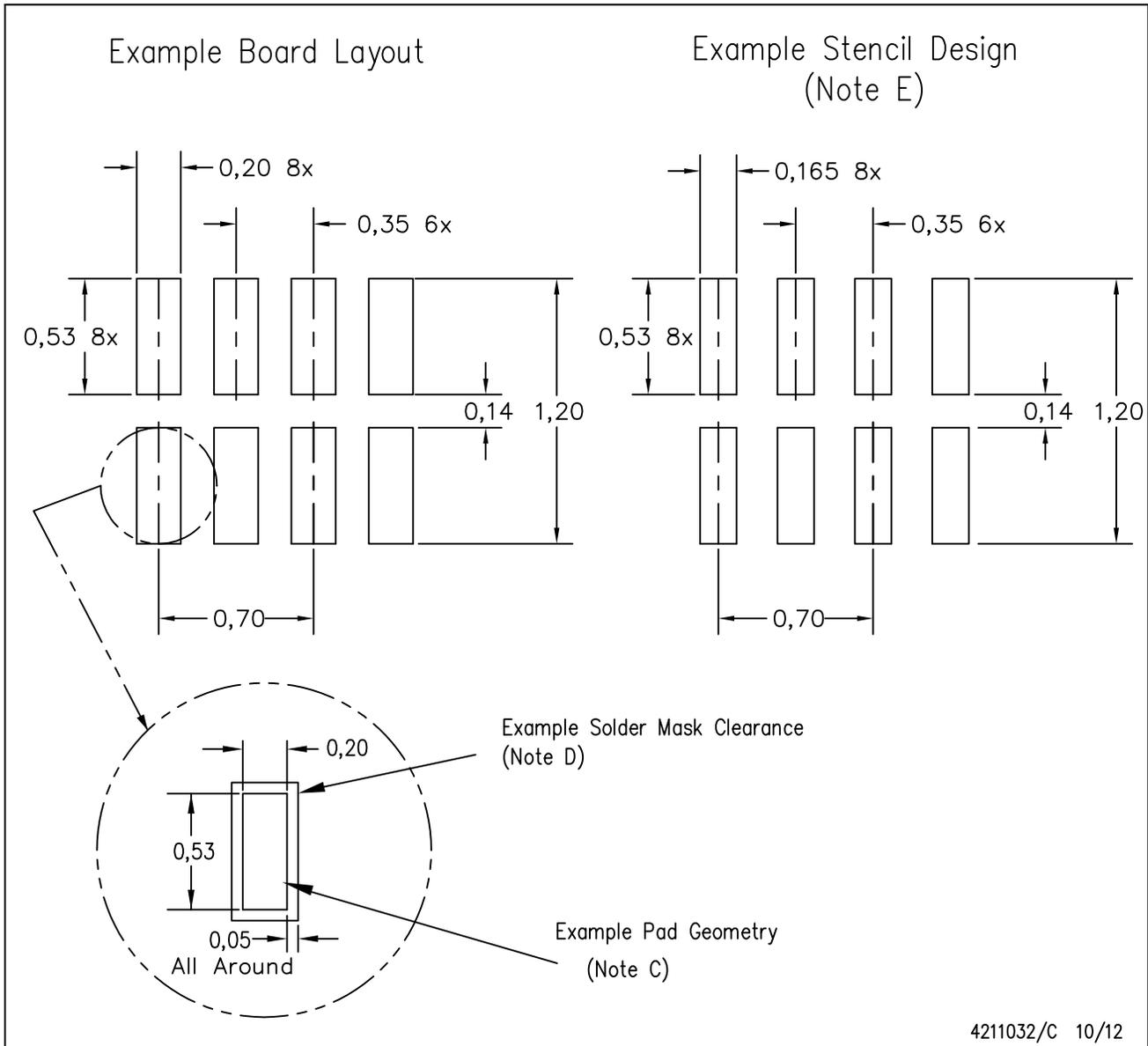


4209779/B 10/2008

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - SON (Small Outline No-Lead) package configuration.
 - This package complies to JEDEC MO-287 variation X2EAF.

DQE (R-PX2SON-N8)

PLASTIC SMALL OUTLINE NO-LEAD

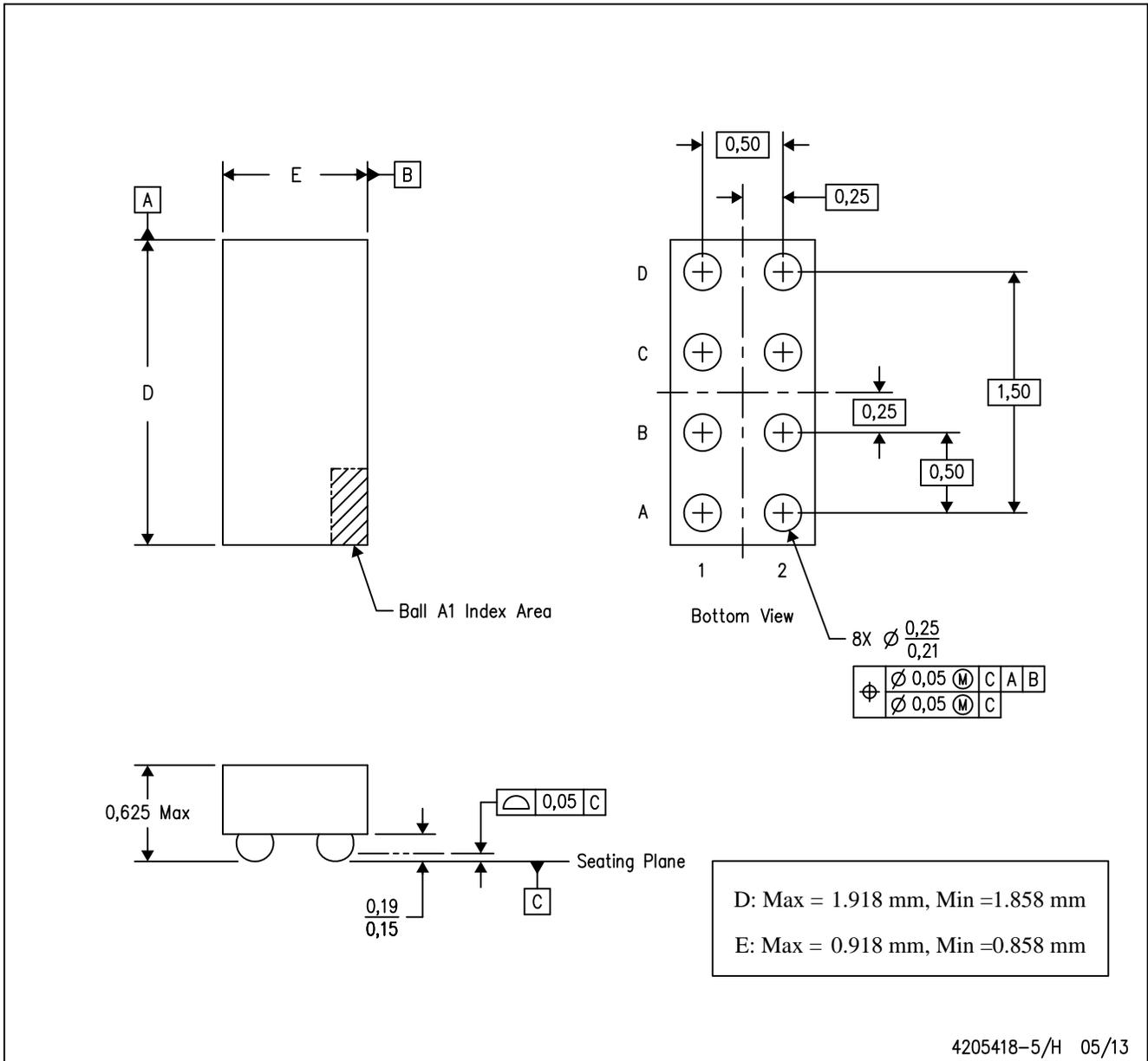


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
 - E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Over-printing land for acceptable area ratio is not viable due to land width and bridging potential. Customer may further reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.
 - H. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
 - I. Component placement force should be minimized to prevent excessive paste block deformation.

MECHANICAL DATA

YZT (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.

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