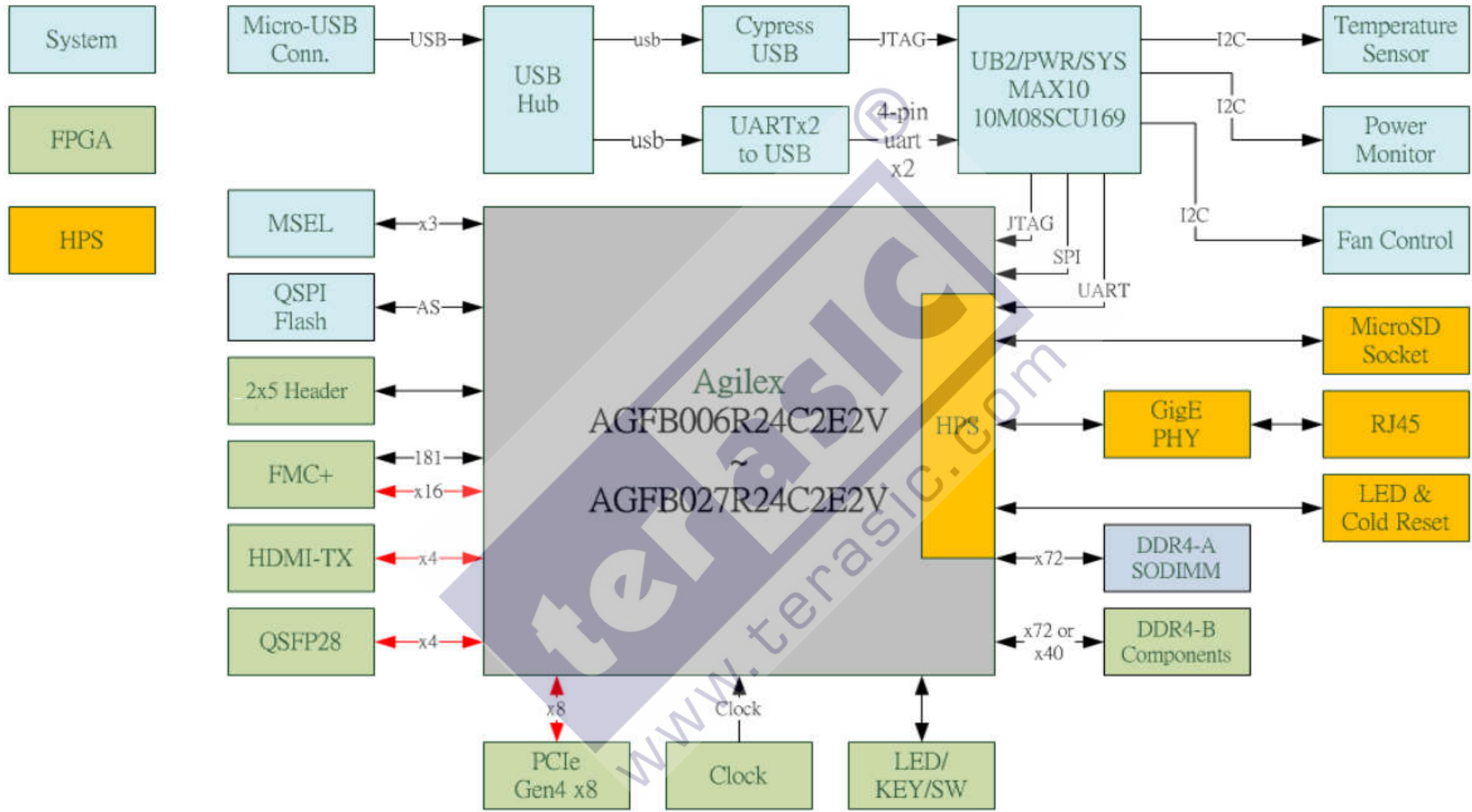
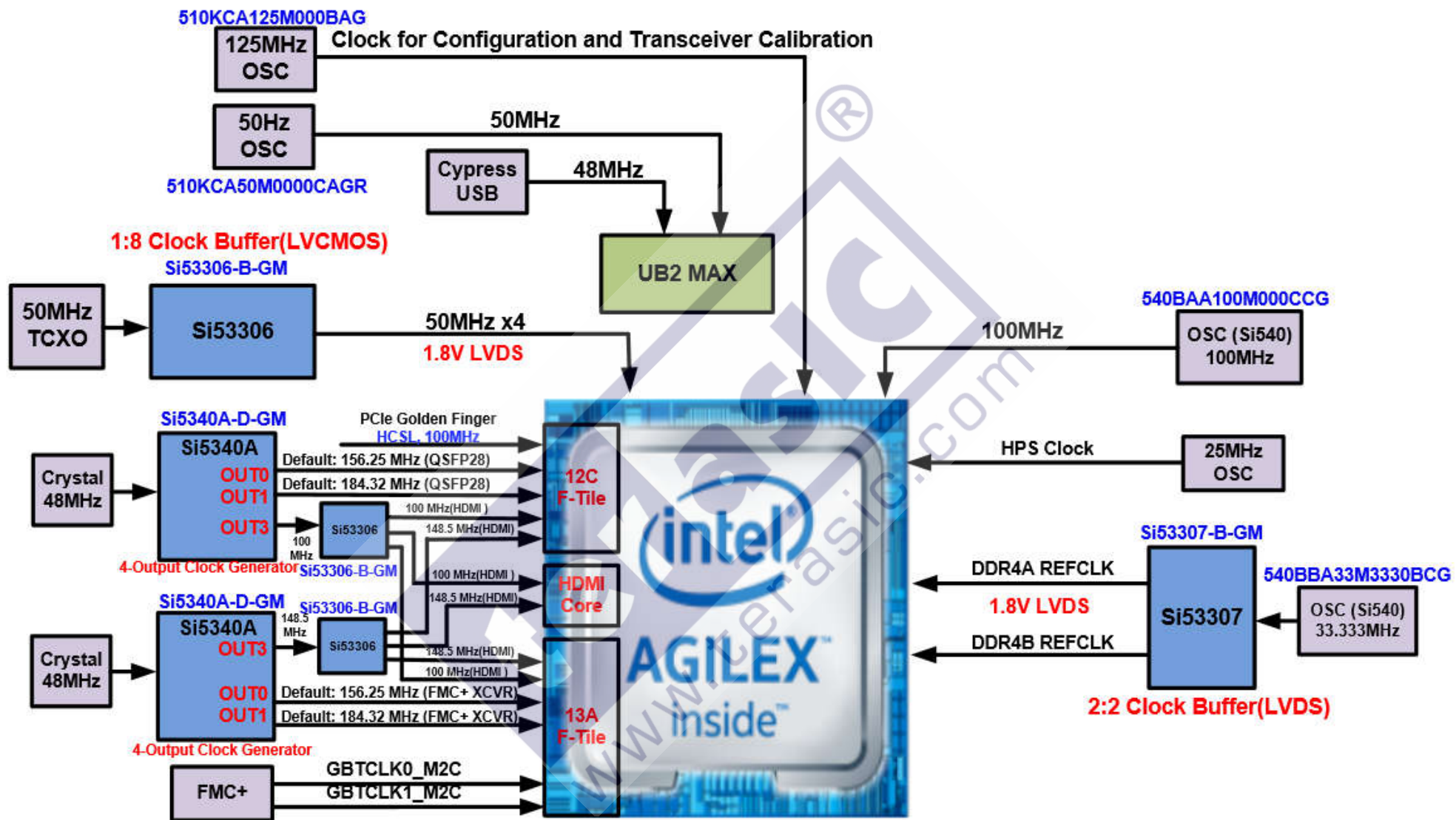


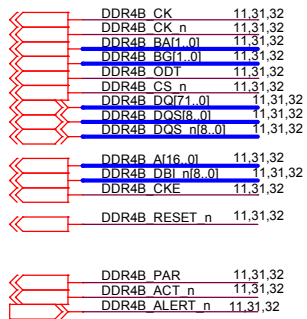
Block Diagram



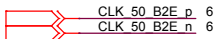
Clock Tree



DDR4 SO-DIMM B



RAS_n is a multiplexed function with A16
CAS_n is a multiplexed function with A15
WE_n is a multiplexed function with A14



DDR4B_DQ51	DA55
DDR4B_DQ53	CY64
DDR4B_DQ55	DC55
DDR4B_DQ49	DD54
	DA53
DDR4B_DBI_n6	CY52
DDR4B_DQS_n6	DC53
DDR4B_DQ56	DD52
DDR4B_DQ50	DA51
DDR4B_DQ54	CY50
DDR4B_DQ48	DC51
DDR4B_DQ52	DD50
	DE53
DDR4B_DQ63	DF52
DDR4B_DQ81	DF52
DDR4B_DQ59	DC51
DDR4B_DQ57	DH50
	DE49
DDR4B_DBI_n7	DF48
DDR4B_DQS_n7	DJ49
DDR4B_DQ57	DH48
DDR4B_DQ56	DE47
DDR4B_DQ60	DF46
DDR4B_DQ62	DJ47
DDR4B_DQ58	DH46
	DA49
DDR4B_DQ45	DA49
DDR4B_DQ47	CY48
DDR4B_DQ43	DC49
DDR4B_DQ41	DD48
	DA47
DDR4B_DBI_n5	CY46
DDR4B_DQS_n5	DC47
DDR4B_DQ55	DD46
DDR4B_DQ42	DA45
DDR4B_DQ44	CY44
DDR4B_DQ40	DC45
DDR4B_DQ46	DD44
	DE45
DDR4B_DQ69	DE45
DDR4B_DQ67	DF44
DDR4B_DQ65	DJ45
DDR4B_DQ71	DH44
	DE43
DDR4B_DBI_n8	DF42
DDR4B_DQS_n8	DJ43
DDR4B_DQ58	DH42
DDR4B_DQ66	DE41
DDR4B_DQ68	DF40
DDR4B_DQ64	DJ41
DDR4B_DQ70	DH40

U35E

IO Bank 2E VCCIO = 1.2V

IO_2E/DIFF_RX_2E1N/95/DQ24
IO_2E/DIFF_RX_2E1P/94/DQ24
IO_2E/DIFF_TX_2E1N/93/DQ24
IO_2E/DIFF_TX_2E1P/92/DQ24
IO_2E/DIFF_RX_2E2N/91/DQ24
IO_2E/DIFF_RX_2E2P/90/DQ24
IO_2E/DIFF_TX_2E2N/89/DQSN24/CQN24
IO_2E/DIFF_TX_2E2P/88/DQSN24/CQ24
IO_2E/DIFF_RX_2E3N/87/DQ24
IO_2E/DIFF_RX_2E3P/86/DQ24
IO_2E/DIFF_TX_2E3N/85/DQ24
IO_2E/DIFF_TX_2E3P/84/DQ24
IO_2E/DIFF_RX_2E4N/83/DQ25
IO_2E/DIFF_RX_2E4P/82/DQ25
IO_2E/DIFF_TX_2E4N/81/DQ25
IO_2E/DIFF_TX_2E4P/80/DQ25
IO_2E/DIFF_RX_2E5N/79/DQ25
IO_2E/DIFF_RX_2E5P/78/DQ25
IO_2E/PLL_2E_T_CLKOUT1N/DIFF_TX_2E5N/77/DQSN25/CQN25
IO_2E/PLL_2E_T_CLKOUT1P,PLL_2E_T_CLKOUT1,PLL_2E_T_FB1/DIFF_TX_2E5P/76/DQSN25/CQ25
IO_2E/DIFF_RX_2E6N/75/DQ25
IO_2E/RZQ_T_2E/DIFF_RX_2E6P/74/DQ25
IO_2E/CLK_T_2E_1N/DIFF_TX_2E6N/73/DQ25
IO_2E/CLK_T_2E_1P/DIFF_TX_2E6P/72/DQ25
IO_2E/CLK_B_2E_0N/DIFF_RX_2E7N/71/DQ26
IO_2E/CLK_T_2E_0P/DIFF_RX_2E7P/70/DQ26
IO_2E/DIFF_TX_2E7N/69/DQ26
IO_2E/DIFF_TX_2E7P/68/DQ26
IO_2E/PLL_2E_T_CLKOUT0N/DIFF_RX_2E8N/67/DQ26
IO_2E/PLL_2E_T_CLKOUT0P,PLL_2E_T_CLKOUT0,PLL_2E_T_FB0/DIFF_RX_2E8P/66/DQ26
IO_2E/DIFF_TX_2E8N/65/DQSN26/CQN26
IO_2E/DIFF_TX_2E8P/64/DQSN26/CQ26
IO_2E/DIFF_RX_2E9N/63/DQ26
IO_2E/DIFF_RX_2E9P/62/DQ26
IO_2E/DIFF_TX_2E9N/61/DQ26
IO_2E/DIFF_TX_2E9P/60/DQ26
IO_2E/DIFF_RX_2E10N/59/DQ27
IO_2E/DIFF_RX_2E10P/58/DQ27
IO_2E/DIFF_TX_2E10N/57/DQ27
IO_2E/DIFF_TX_2E10P/56/DQ27
IO_2E/DIFF_RX_2E11N/55/DQ27
IO_2E/DIFF_RX_2E11P/54/DQ27
IO_2E/DIFF_TX_2E11N/53/DQSN27/CQN27
IO_2E/DIFF_TX_2E11P/52/DQSN27/CQ27
IO_2E/DIFF_RX_2E12N/51/DQ27
IO_2E/DIFF_RX_2E12P/50/DQ27
IO_2E/DIFF_TX_2E12N/49/DQ27
IO_2E/DIFF_TX_2E12P/48/DQ27

TOP BOT

AGFB027R24C2E2VR2

IO_2E/CLK_B_2E_0N/DIFF_RX_2E19N/23/DQ30
IO_2E/CLK_B_2E_0P/DIFF_RX_2E19P/22/DQ30
IO_2E/DIFF_TX_2E19N/21/DQ30
IO_2E/DIFF_TX_2E19P/20/DQ30
IO_2E/PLL_2E_B_CLKOUT0N/DIFF_RX_2E20N/19/DQ30
IO_2E/PLL_2E_B_CLKOUT0P,PLL_2E_B_CLKOUT0,PLL_2E_B_FB0/DIFF_RX_2E20P/18/DQ30
IO_2E/DIFF_TX_2E20N/17/DQSN30/CQN30
IO_2E/DIFF_TX_2E20P/16/DQSN30/CQ30
IO_2E/DIFF_RX_2E21N/15/DQ30
IO_2E/DIFF_RX_2E21P/14/DQ30
IO_2E/DIFF_TX_2E21N/13/DQ30
IO_2E/DIFF_TX_2E21P/12/DQ30
IO_2E/DIFF_RX_2E22N/11/DQ31
IO_2E/DIFF_RX_2E22P/10/DQ31
IO_2E/DIFF_TX_2E22N/9/DQ31
IO_2E/DIFF_TX_2E22P/8/DQ31
IO_2E/DIFF_RX_2E23N/7/DQ31
IO_2E/DIFF_RX_2E23P/6/DQ31
IO_2E/DIFF_TX_2E23N/5/DQSN31/CQN31
IO_2E/DIFF_TX_2E23P/4/DQSN31/CQ31
IO_2E/DIFF_RX_2E24N/3/DQ31
IO_2E/DIFF_RX_2E24P/2/DQ31
IO_2E/DIFF_TX_2E24N/1/DQ31
IO_2E/DIFF_TX_2E24P/1/DQ31

CN53	CLK_50_B2E_n
CM52	CLK_50_B2E_p
CR53	
CT52	
CL51	
CK50	
CN51	
CP50	
CL49	
CK48	
CN49	
CP48	
	CW55
	CV54
	CW53
	CV52
	CR51
	CT50
	CW51
	CV50
	CR49
	CT48
	CW49
	CV48

Copyright (c) 2017 by Terasic Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
A7SK		
Size	Document Number	Rev
B	FPGA Bank 2E	A
Date:	Wednesday, May 10, 2023	Sheet 10 of 52

DDR4B CK	31,32
DDR4B CK_n	31,32
DDR4B BA[1..0]	31,32
DDR4B BG[1..0]	31,32
DDR4B ODT	31,32
DDR4B CS_n	31,32
DDR4B DQ[71..0]	10,31,32
DDR4B DQS[8..0]	10,31,32
DDR4B DQS_n[8..0]	10,31,32
DDR4B A[16..0]	31,32
DDR4B DBI_n[8..0]	10,31,32
DDR4B CKE	31,32
DDR4B RESET_n	31,32

DDR4B PAR	31,32
DDR4B ACT _n	31,32
DDR4B ALERT _n	31,32

DDR4B_REFCLK_p	6
DDR4B_REFCLK_n	6

RAS_n is a multiplexed function with A16
CAS_n is a multiplexed function with A15
WE_n is a multiplexed function with A14



DDR4B_DQ0	DE29
DDR4B_DQ6	DF28
DDR4B_DQ2	DJ29
DDR4B_DQ4	DH28
	DE31
DDR4B_DBI_n0	DF30
DDR4B_DQS_n0	DJ31
DDR4B_DQS0	DH30
DDR4B_DQ7	DE33
DDR4B_DQ3	DF32
DDR4B_DQ5	DJ33
DDR4B_DQ1	DH32

DDR4B_BG0	DA33
DDR4B_BA1	CY32
DDR4B_BA0	DC33
DDR4B_ALERT_n	DD32
DDR4B_A16	DA35
DDR4B_A15	CY34
DDR4B_A14	DC35
DDR4B_A13	DD34
DDR4B_A12	DA37
DDR4B_RZQ	CY36
DDR4B_REFCLK_n	DC37
DDR4B_REFCLK_p	DD36

DDR4B_A11	DE35
DDR4B_A10	DF34
DDR4B_A9	DJ35
DDR4B_A8	DH34
DDR4B_A7	DE37
DDR4B_A6	DF36
DDR4B_A5	DJ37
DDR4B_A4	DH36
DDR4B_A3	DE39
DDR4B_A2	DF38
DDR4B_A1	DJ39
DDR4B_A0	DH38

DDR4B_PAR	DA39
	CY38
DDR4B_CK_n	DC39
DDR4B_CK	DD38
	DA41
DDR4B_CKE	CY40
	DC41
DDR4B_ODT	DD40
DDR4B_ACT_n	DA43
DDR4B_CS_n	CY42
DDR4B_RESET_n	DC43
DDR4B_BG1	DD42

AGFB027R24C2E2VR2

[TOP](#) | [BOT](#)

IO_2F/DIFF_RX_2F1N/95/DQ16
IO_2F/DIFF_RX_2F1P/94/DQ16
IO_2F/DIFF_TX_2F1N/93/DQ16
IO_2F/DIFF_TX_2F1P/92/DQ16
IO_2F/DIFF_RX_2F2N/91/DQ16
IO_2F/DIFF_RX_2F2P/90/DQ16
IO_2F/DIFF_TX_2F2N/89/DQS16/CQN16
IO_2F/DIFF_TX_2F2P/88/DQS16/CQ16
IO_2F/DIFF_RX_2F3N/87/DQ16
IO_2F/DIFF_RX_2F3P/86/DQ16
IO_2F/DIFF_TX_2F3N/85/DQ16
IO_2F/DIFF_TX_2F3P/84/DQ16

IO_2F/DIFF_RX_2F4N/83/DQ17
IO_2F/DIFF_RX_2F4P/82/DQ17
IO_2F/DIFF_TX_2F4N/81/DQ17
IO_2F/DIFF_TX_2F4P/80/DQ17
IO_2F/DIFF_RX_2F5N/79/DQ17
IO_2F/DIFF_RX_2F5P/78/DQ17
IO_2F/PLL_2F_2_CLKOUT1N/DIFF_TX_2F
IO_2F/PLL_2F_2_CLKOUT1P/PLL_2F_2_C
IO_2F/DIFF_RX_2F6N/75/DQ17
IO_2F/RQZ_2F/DIFF_RX_2F6P/74/DQ17
IO_2F/CLK_2F_1N/DIFF_TX_2F6N/73/D
IO_2F/CLK_2F_1P/DIFF_TX_2F6P/72/DQ

IO_2F/CLK_T_2F_0N/DIFF_RX_2F7N17/D
IO_2F/CLK_T_2F_0N/DIFF_RX_2F7P70/D
IO_2F/DIFF_TX_2F7N69/DQ18
IO_2F/DIFF_TX_2F7K68/DQ18
IO_2F/PLL_2F_T_CLKOUT0N/DIFF_RX_2F
IO_2F/PLL_2F_T_CLKOUT0P.PLL_2F_T_C
IO_2F/DIFF_TX_2F8N65/DQSN18/CQ18
IO_2F/DIFF_TX_2F8P64/DQS18/CQ18
IO_2F/DIFF_RX_2F9N63/DQ18
IO_2F/DIFF_RX_2F9P62/DQ18
IO_2F/DIFF_TX_2F9N61/DQ18
IO_2F/DIFF_TX_2F9P60/DQ18

IO_2F/DIFF_RX_2F10N/59/DQ19
IO_2F/DIFF_RX_2F10P/58/DQ19
IO_2F/DIFF_TX_2F10N/57/DQ19
IO_2F/DIFF_TX_2F10P/56/DQ19
IO_2F/DIFF_RX_2F11N/55/DQ19
IO_2F/DIFF_RX_2F11P/54/DQ19
IO_2F/DIFF_TX_2F11N/53/DQSN19/CQN19
IO_2F/DIFF_TX_2F11P/52/DQSN19/CQ19
IO_2F/DIFF_RX_2F12N/51/DQ19
IO_2F/DIFF_RX_2F12P/50/DQ19
IO_2F/DIFF_TX_2F12N/49/DQ19
IO_2F/DIFF_TX_2F12P/48/DQ19

F5N/77/DQSN17/CQN17
CLKOUT1,PLL_2F_T_FB1/DIFF_TX_2F5P/76/DQS1
Q17

Q18
Q18
F8N/67/DQ18
CLKOUT0,PLL_2F_T_FB0/DIFF_RX_2F8P/66/DQ18

9



IO_2F/P
7/CQ17IO_2F/PLL_2F_B_CLKOUT1P,PLL_2F_B_C

IO_2F/PLL_2F_B_CLKOUT0P,PLL_

OP BOT

```

IO_2F/DIFF_RX_2F13N/47/DQ20
IO_2F/DIFF_RX_2F13P/46/DQ20
IO_2F/DIFF_TX_2F13N/45/DQ20
IO_2F/DIFF_TX_2F13P/44/DQ20
IO_2F/DIFF_RX_2F14N/43/DQ20
IO_2F/DIFF_RX_2F14P/42/DQ20
IO_2F/DIFF_TX_2F14N/41/DQ20N2/CQN2
IO_2F/DIFF_TX_2F14P/40/DQ20S2/CQN2
IO_2F/DIFF_RX_2F15N/39/DQ20
IO_2F/DIFF_RX_2F15P/38/DQ20
IO_2F/DIFF_TX_2F15N/37/DQ20
IO_2F/DIFF_TX_2F15P/36/DQ20

```

```

IO_2F/DIFF_RX_2F16N/35/DQ02;
IO_2F/DIFF_RX_2F16P/34/DQ01;
IO_2F/DIFF_TX_2F16N/33/DQ02;
IO_2F/DIFF_TX_2F16P/32/DQ01;
IO_2F/DIFF_RX_2F17N/31/DQ02;
IO_2F/DIFF_RX_2F17P/30/DQ01;
PLL_2F_B_CLKOUT1N/DIFF_TX_2F17N/29/DQS2N1/CQN2;
CLKOUT1_PLL_2F_BF1/DIFF_TX_2F17P/28/DQS2C1/CQN1;
IO_2F/DIFF_RX_2F18N/27/DQ02;
IO_2F/RZQ_B_2F/DIFF_RX_2F18P/26/DQ02;
IO_2F/CLK_B_2F_1N/DIFF_TX_2F18N/25/DQ02;
IO_2F/CLK_B_2F_1P/DIFF_TX_2F18P/24/DQ02;

```

```

IO_2F/CLK_B_2F_0N/DIFF_RX_2F19N/23/DQ22
IO_2F/CLK_B_2F_0N/DIFF_RX_2F19P/22/DQ23
IO_2F/DIFF_TX_2F19N/21/DQ21
IO_2F/DIFF_TX_2F19P/20/DQ20
IO_2F/PLL_2F_B_CLKOUT0N/DIFF_RX_2F20N/19/DQ21
2F_B_CLKOUT0_PLL_2F_B_FBO/DIFF_RX_2F20P/18/DQ20
IO_2F/DIFF_TX_2F20N/17/DQS22/CQN22
IO_2F/DIFF_TX_2F20P/16/DQS22/CQ22
IO_2F/DIFF_RX_2F21N/15/DQ22
IO_2F/DIFF_RX_2F21P/14/DQ21
IO_2F/DIFF_TX_2F21N/13/DQ21
IO_2F/DIFF_TX_2F21P/12/DQ20

```

```

IO_2F/DIFF_RX_2F22N11/DQ23
IO_2F/DIFF_RX_2F22P10/DQ23
IO_2F/DIFF_TX_2F22N9/DQ23
IO_2F/DIFF_TX_2F22P8/DQ23
IO_2F/DIFF_RX_2F23N7/DQ23
IO_2F/DIFF_RX_2F23P6/DQ23
IO_2F/DIFF_TX_2F23N5/DQSN23/CQN23
IO_2F/DIFF_TX_2F23P4/DQSN23/CQN23
IO_2F/DIFF_RX_2F24N3/DQ23
IO_2F/DIFF_RX_2F24P2/DQ23
IO_2F/DIFF_TX_2F24N1/DQ23
IO_2F/DIFF_TX_2F24P/DQ23

```

CR37	DDR4B_DQ12
CT36	DDR4B_DQ10
CW37	DDR4B_DQ14
CV36	DDR4B_DQ8
CR39	
CT38	DDR4B_DBI_n1
CW39	DDR4B_DQS_n1
CV38	DDR4B_DQS1
CR41	DDR4B_DQ15
CT40	DDR4B_DQ9
CW41	DDR4B_DQ13
CV40	DDR4B_DQ11

CL37	DDR4B_DQ34
CK36	DDR4B_DQ38
CN37	DDR4B_DQ32
CP36	DDR4B_DQ36
CL39	
CK38	DDR4B_DBI_n4
CN39	DDR4B_DQS_n4
CP38	DDR4B_DQS4
CL41	DDR4B_DQ35
CK40	DDR4B_DQ37
CN41	DDR4B_DQ39
CP40	DDR4B_DQ33

CR43	DDR4B_DQ23
CT42	DDR4B_DQ20
CW43	DDR4B_DQ18
CV42	DDR4B_DQ16
CR45	
CT44	DDR4B_DBI_n2
CW45	DDR4B_DQS_n2
CV44	DDR4B_DQS2
CR47	DDR4B_DQ21
CT46	DDR4B_DQ22
CW47	DDR4B_DQ19
CV46	DDR4B_DQ17

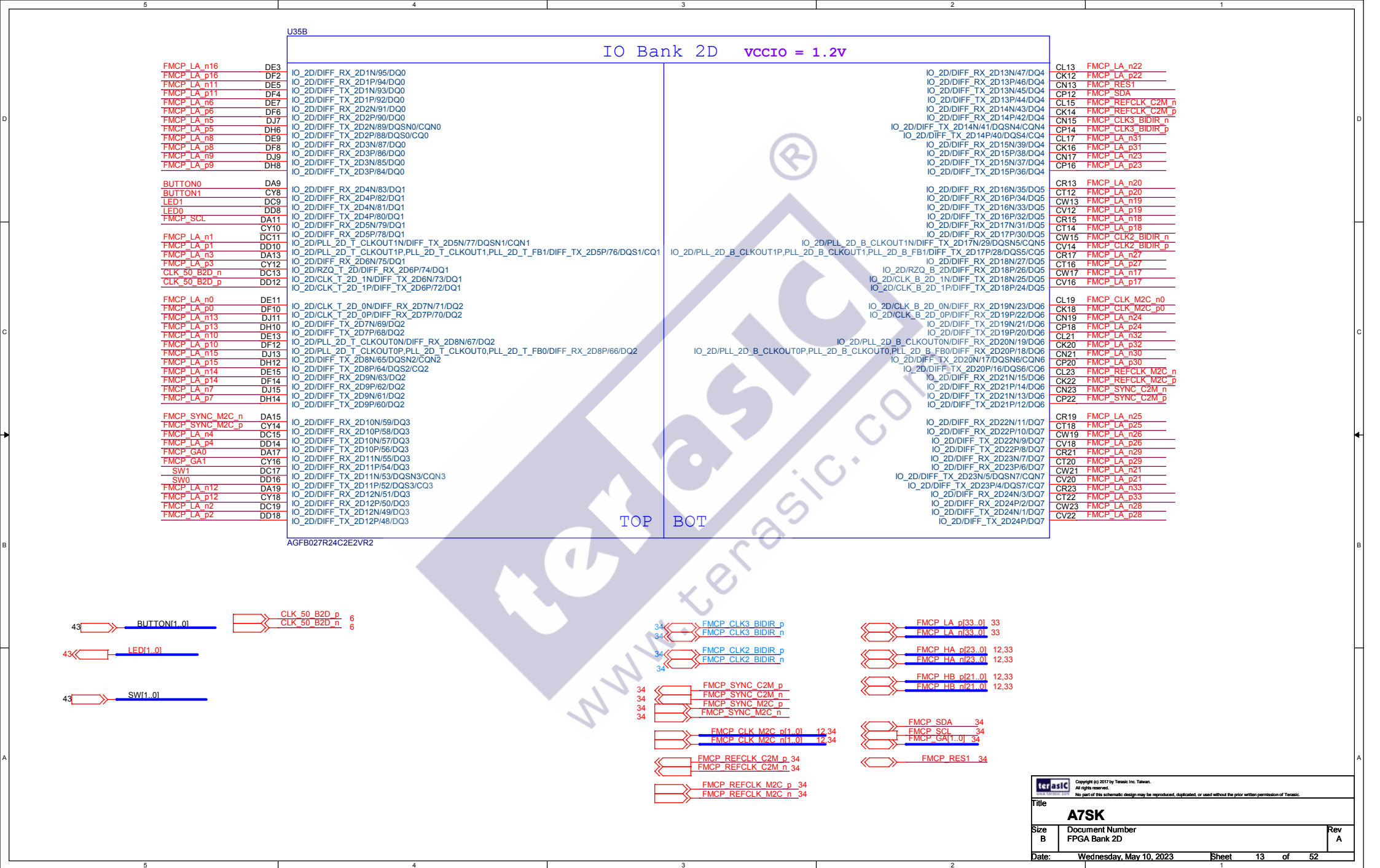
CL43	DDR4B_DQ30
CK42	DDR4B_DQ31
CN43	DDR4B_DQ24
CP42	DDR4B_DQ28
CL45	
CK44	DDR4B_DBI_n3
CN45	DDR4B_DQS_n3
CP44	DDR4B_DQS3
CL47	DDR4B_DQ27
CK46	DDR4B_DQ29
CN47	DDR4B_DQ25
CP46	DDR4B_DQ26

FMCP_CLK_M2C_n1_0 13,34
FMCP_CLK_M2C_n1_0 13,34
FMCP_HA_p23_0 33
FMCP_HA_n23_0 33
FMCP_HB_p21_0 33
FMCP_HB_n21_0 33

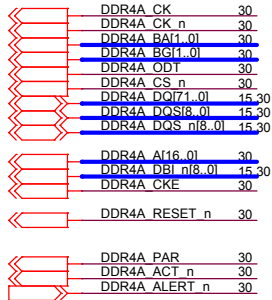
		U35C		IO Bank 2C VCCIO = VCCIO_FMCP_HAB (1.2 or 1.5V)			
FMCP_HA_n7	DE17	IO_2C/DIFF_RX_2C1N/95/DQ8		IO_2C/DIFF_RX_2C13N/47/DQ12	CL25	FMCP_HB_n15	
FMCP_HA_p7	DF16	IO_2C/DIFF_RX_2C1P/94/DQ8		IO_2C/DIFF_RX_2C13P/46/DQ12	CK24	FMCP_HB_p15	
FMCP_HA_n4	DJ17	IO_2C/DIFF_TX_2C1N/93/DQ8		IO_2C/DIFF_TX_2C13N/45/DQ12	CN25	FMCP_HB_n4	
FMCP_HA_p4	DH16	IO_2C/DIFF_TX_2C1P/92/DQ8		IO_2C/DIFF_TX_2C13P/44/DQ12	CP24	FMCP_HB_p4	
FMCP_HA_n9	DE19	IO_2C/DIFF_RX_2C2N/91/DQ8		IO_2C/DIFF_RX_2C14N/43/DQ12	CL27	FMCP_HB_n11	
FMCP_HA_p9	DF18	IO_2C/DIFF_RX_2C2P/90/DQ8		IO_2C/DIFF_RX_2C14P/42/DQ12	CK26	FMCP_HB_p11	
FMCP_HA_n8	DJ19	IO_2C/DIFF_TX_2C2N/89/DQS8/CQN8		IO_2C/DIFF_TX_2C14N/41/DQS8/CQN12	CN27	FMCP_HB_n2	
FMCP_HA_p8	DH18	IO_2C/DIFF_TX_2C2P/88/DQS8/CQ8		IO_2C/DIFF_TX_2C14P/40/DQS12/CQ12	CP26	FMCP_HB_p2	
FMCP_HA_n13	DE21	IO_2C/DIFF_RX_2C3N/87/DQ8		IO_2C/DIFF_RX_2C15N/39/DQ12	CL29	FMCP_HB_n3	
FMCP_HA_p13	DF20	IO_2C/DIFF_RX_2C3P/86/DQ8		IO_2C/DIFF_RX_2C15P/38/DQ12	CK28	FMCP_HB_p3	
FMCP_HA_n6	DJ21	IO_2C/DIFF_TX_2C3N/85/DQ8		IO_2C/DIFF_TX_2C15N/37/DQ12	CN29	FMCP_HB_n5	
FMCP_HA_p6	DH20	IO_2C/DIFF_TX_2C3P/84/DQ8		IO_2C/DIFF_TX_2C15P/36/DQ12	CP28	FMCP_HB_p6	
FMCP_HA_n5	DA21	IO_2C/DIFF_RX_2C4N/83/DQ9		IO_2C/DIFF_RX_2C16N/35/DQ13	CR25	FMCP_HB_n7	
FMCP_HA_p5	CY20	IO_2C/DIFF_RX_2C4P/82/DQ9		IO_2C/DIFF_RX_2C16P/34/DQ13	CT24	FMCP_HB_p7	
FMCP_HA_n2	DC21	IO_2C/DIFF_TX_2C4N/81/DQ9		IO_2C/DIFF_TX_2C16N/33/DQ13	CW25	FMCP_HB_n8	
FMCP_HA_p2	DD20	IO_2C/DIFF_TX_2C4P/80/DQ9		IO_2C/DIFF_TX_2C16P/32/DQ13	CV24	FMCP_HB_p8	
FMCP_HA_n3	DA23	IO_2C/DIFF_RX_2C5N/79/DQ9		IO_2C/DIFF_RX_2C17N/31/DQ13	CR27		
FMCP_HA_p3	CY22	IO_2C/DIFF_RX_2C5P/78/DQ9		IO_2C/DIFF_RX_2C17P/30/DQ13	CT26		
FMCP_HA_n0	DC23	IO_2C/PLL_2C_T_CLKOUT1N/DIFF_TX_2C5N/77/DQSN9/CQN9		IO_2C/PLL_2C_B_CLKOUT1N/DIFF_TX_2C17N/29/DQSN13/CQN13	CW27	FMCP_HB_n0	
FMCP_HA_p0	DD22	IO_2C/PLL_2C_T_CLKOUT1P/PLL_2C_T_CLKOUT1P/PLL_2C_T_FB1/DIFF_TX_2C5P/76/DQSN9/CQ9		IO_2C/PLL_2C_B_CLKOUT1P/PLL_2C_B_CLKOUT1P/PLL_2C_B_FB1/DIFF_TX_2C17P/28/DQSN13/CQ13	CV26	FMCP_HB_p0	
FMCP_HA_n22	DA25	IO_2C/DIFF_RX_2C6N/75/DQ9		IO_2C/DIFF_RX_2C18N/27/DQ13	CR29	FMCP_HB_n5	
FMCP_HA_p22	CY24	IO_2C/RZQ_2C_2C/DIFF_RX_2C6P/74/DQ9		IO_2C/RZQ_2C_2C/DIFF_RX_2C18P/26/DQ13	CT28	FMCP_HB_p5	
FMCP_HA_n17	DC25	IO_2C/CLK_T_2C_1N/DIFF_TX_2C6N/73/DQ9		IO_2C/CLK_B_2C_1N/DIFF_TX_2C18N/25/DQ13	CW29	FMCP_CLK_M2C_n1	
FMCP_HA_p17	DD24	IO_2C/CLK_T_2C_1P/DIFF_TX_2C6P/72/DQ9		IO_2C/CLK_B_2C_1P/DIFF_TX_2C18P/24/DQ13	CV28	FMCP_CLK_M2C_p1	
FMCP_HA_n1	DE23	IO_2C/CLK_T_2C_0N/DIFF_RX_2C7N/71/DQ10		IO_2C/CLK_B_2C_0N/DIFF_RX_2C19N/23/DQ14	CR31	FMCP_HB_n1	
FMCP_HA_p1	DF22	IO_2C/CLK_T_2C_0P/DIFF_RX_2C7P/70/DQ10		IO_2C/CLK_B_2C_0P/DIFF_RX_2C19P/22/DQ14	CT30	FMCP_HB_p1	
FMCP_HA_n10	DJ23	IO_2C/DIFF_TX_2C7N/69/DQ10		IO_2C/DIFF_TX_2C19N/21/DQ14	CW31	FMCP_HB_n10	
FMCP_HA_p10	DH22	IO_2C/DIFF_TX_2C7P/68/DQ10		IO_2C/DIFF_TX_2C19P/20/DQ14	CV30	FMCP_HB_p10	
FMCP_HA_n16	DE25	IO_2C/PLL_2C_T_CLKOUT0N/DIFF_RX_2C8N/67/DQ10		IO_2C/PLL_2C_B_CLKOUT0N/DIFF_RX_2C20N/19/DQ14	CR33	FMCP_HB_n13	
FMCP_HA_p16	DF24	IO_2C/PLL_2C_T_CLKOUT0P/PLL_2C_T_CLKOUT0P/PLL_2C_T_FB0/DIFF_RX_2C8P/66/DQ10		IO_2C/PLL_2C_B_CLKOUT0P/PLL_2C_B_CLKOUT0P/PLL_2C_B_FB0/DIFF_RX_2C20P/18/DQ14	CT32	FMCP_HB_p13	
FMCP_HA_n12	DJ25	IO_2C/DIFF_TX_2C8N/65/DQSN10/CQN10		IO_2C/DIFF_TX_2C20N/17/DQSN14/CQN14	CW33	FMCP_HB_n14	
FMCP_HA_p12	DH24	IO_2C/DIFF_TX_2C8P/64/DQSN10/CQ10		IO_2C/DIFF_TX_2C20P/16/DQSN14/CQ14	CV32	FMCP_HB_p14	
FMCP_HA_n14	DE27	IO_2C/DIFF_RX_2C9N/63/DQ10		IO_2C/DIFF_RX_2C21N/15/DQ14	CR35	FMCP_HB_n21	
FMCP_HA_p14	DF26	IO_2C/DIFF_RX_2C9P/62/DQ10		IO_2C/DIFF_RX_2C21P/14/DQ14	CT34	FMCP_HB_p21	
FMCP_HA_n15	DJ27	IO_2C/DIFF_TX_2C9N/61/DQ10		IO_2C/DIFF_TX_2C21N/13/DQ14	CW35	FMCP_HB_n17	
FMCP_HA_p15	DH26	IO_2C/DIFF_TX_2C9P/60/DQ10		IO_2C/DIFF_TX_2C21P/12/DQ14	CV34	FMCP_HB_p17	
FMCP_HA_n11	DA27	IO_2C/DIFF_RX_2C10N/59/DQ11		IO_2C/DIFF_RX_2C22N/11/DQ15	CL31	FMCP_HB_n9	
FMCP_HA_p11	CY26	IO_2C/DIFF_RX_2C10P/58/DQ11		IO_2C/DIFF_RX_2C22P/10/DQ15	CK30	FMCP_HB_p9	
FMCP_HA_n19	DC27	IO_2C/DIFF_TX_2C10N/57/DQ11		IO_2C/DIFF_TX_2C22N/9/DQ15	CN31	FMCP_HB_n12	
FMCP_HA_p19	DD26	IO_2C/DIFF_TX_2C10P/56/DQ11		IO_2C/DIFF_TX_2C22P/8/DQ15	CP30	FMCP_HB_p12	
FMCP_HA_n20	DA29	IO_2C/DIFF_RX_2C11N/55/DQ11		IO_2C/DIFF_RX_2C23N/7/DQ15	CL33	FMCP_HB_n19	
FMCP_HA_p20	CY28	IO_2C/DIFF_RX_2C11P/54/DQ11		IO_2C/DIFF_RX_2C23P/6/DQ15	CK32	FMCP_HB_p19	
FMCP_HA_n21	DC29	IO_2C/DIFF_TX_2C11N/53/DQSN11/CQN11		IO_2C/DIFF_TX_2C23N/5/DQSN15/CQN15	CN33	FMCP_HB_n16	
FMCP_HA_p21	DD28	IO_2C/DIFF_TX_2C11P/52/DQSN11/CQ11		IO_2C/DIFF_TX_2C23P/4/DQSN15/CQ15	CP32	FMCP_HB_p16	
FMCP_HA_n18	DA31	IO_2C/DIFF_RX_2C12N/51/DQ11		IO_2C/DIFF_RX_2C24N/3/DQ15	CL35	FMCP_HB_n18	
FMCP_HA_p18	CY30	IO_2C/DIFF_RX_2C12P/50/DQ11		IO_2C/DIFF_RX_2C24P/2/DQ15	CK34	FMCP_HB_p18	
FMCP_HA_n23	DC31	IO_2C/DIFF_TX_2C12N/49/DQ11		IO_2C/DIFF_TX_2C24N/1/DQ15	CN35	FMCP_HB_n20	
FMCP_HA_p23	DD30	IO_2C/DIFF_TX_2C12P/48/DQ11		IO_2C/DIFF_TX_2C24P/0/DQ15	CP34	FMCP_HB_p20	

AGFB027R24C2E2V/R2

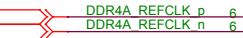
Title		A7SK	
Size	Document Number	Rev	
B	FPGA Bank 2C	A	
Date:	Wednesday, May 10, 2023	Sheet	12 of 52



DDR4 SO-DIMM A



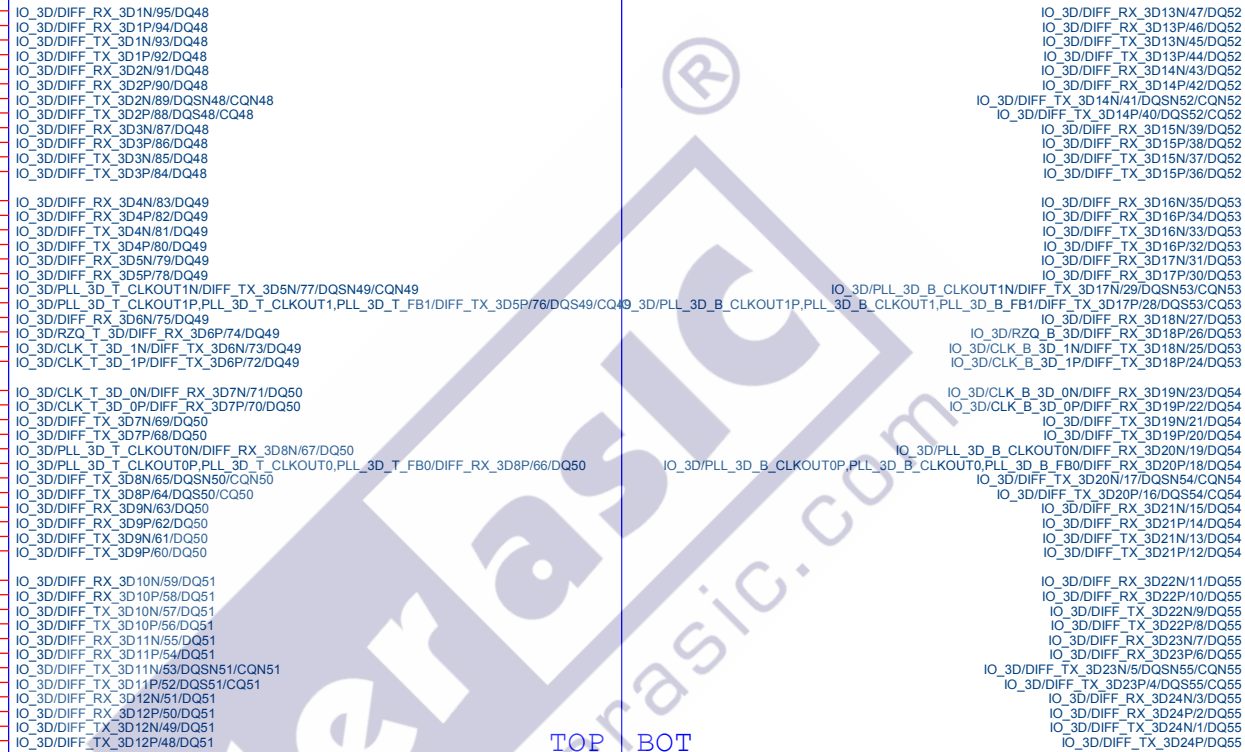
RAS_n is a multiplexed function with A16
CAS_n is a multiplexed function with A15
WE_n is a multiplexed function with A14



DDR4A_DQ4	P2
DDR4A_DQ5	R1
DDR4A_DQ1	M2
DDR4A_DQ0	L1
DDR4A_DBI_n0	P4
DDR4A_DQS_n0	R3
DDR4A_DQS0	M4
DDR4A_DQ6	L3
DDR4A_DQ7	P6
DDR4A_DQ2	R5
DDR4A_DQ3	M6
DDR4A_DQ9	L5
DDR4A_DQ11	K2
DDR4A_DQ10	J1
DDR4A_DQ12	F2
DDR4A_DQ15	G1
DDR4A_DBI_n1	K4
DDR4A_DQS_n1	J3
DDR4A_DQS1	F4
DDR4A_DQ12	G3
DDR4A_DQ8	K6
DDR4A_DQ14	J5
DDR4A_DQ13	F6
DDR4A_DQ23	D6
DDR4A_DQ21	E5
DDR4A_DQ16	B6
DDR4A_DQ17	C5
DDR4A_DBI_n2	D8
DDR4A_DQS_n2	E7
DDR4A_DQS2	B8
DDR4A_DQ18	A7
DDR4A_DQ20	D10
DDR4A_DQ22	E9
DDR4A_DQ19	B10
DDR4A_DQ27	K8
DDR4A_DQ28	J7
DDR4A_DQ25	F8
DDR4A_DQ29	G7
DDR4A_DBI_n3	K10
DDR4A_DQS_n3	J9
DDR4A_DQS3	F10
DDR4A_DQ31	G9
DDR4A_DQ30	K12
DDR4A_DQ24	J11
DDR4A_DQ26	F12
	G11

U35F

IO Bank 3D vccio = 1.2v

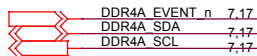
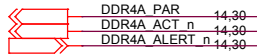
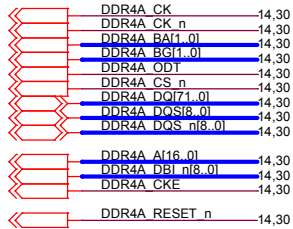


AD2	DDR4A_DQ66
AE1	DDR4A_DQ65
AB2	DDR4A_DQ71
AA1	DDR4A_DQ70
AB4	DDR4A_DBI_n8
AA3	DDR4A_DQS_n8
AB6	DDR4A_DQS_n8
AA5	DDR4A_DQS8
AE7	DDR4A_DQ68
AD6	DDR4A_DQ69
AB8	DDR4A_DQ64
AA7	DDR4A_DQ67
Y2	DDR4A_BG0
W1	DDR4A_BA1
T2	DDR4A_ALERT_n
U1	DDR4A_ALERT_n
Y4	DDR4A_A16
W3	DDR4A_A15
T4	DDR4A_A14
U3	DDR4A_A13
Y6	DDR4A_A12
W5	DDR4A_RZQ
T6	DDR4A_REFCLK_n
U5	DDR4A_REFCLK_p
Y8	DDR4A_A11
W7	DDR4A_A10
T8	DDR4A_A9
U7	DDR4A_A8
Y10	DDR4A_A7
W9	DDR4A_A6
T10	DDR4A_A5
U9	DDR4A_A4
Y12	DDR4A_A3
W11	DDR4A_A2
T12	DDR4A_A1
U11	DDR4A_A0
P8	DDR4A_PAR
R7	DDR4A_CK_n
M8	DDR4A_CK
L7	DDR4A_CK
P10	DDR4A_CKE
R9	DDR4A_CKE
M10	DDR4A_ODT
L9	DDR4A_ODT
P12	DDR4A_ACT_n
R11	DDR4A_CS_n
M12	DDR4A_RESET_n
L11	DDR4A_BG1

AGFB027R24C2E2VR2

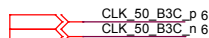
terasic			Copyright (c) 2017 by Terasic Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title					
A7SK					
Size	Document Number				Rev
B	FPGA Bank 3D				A
Date:	Wednesday, May 10, 2023				Sheet 14 of 52

DDR4 SO-DIMM A



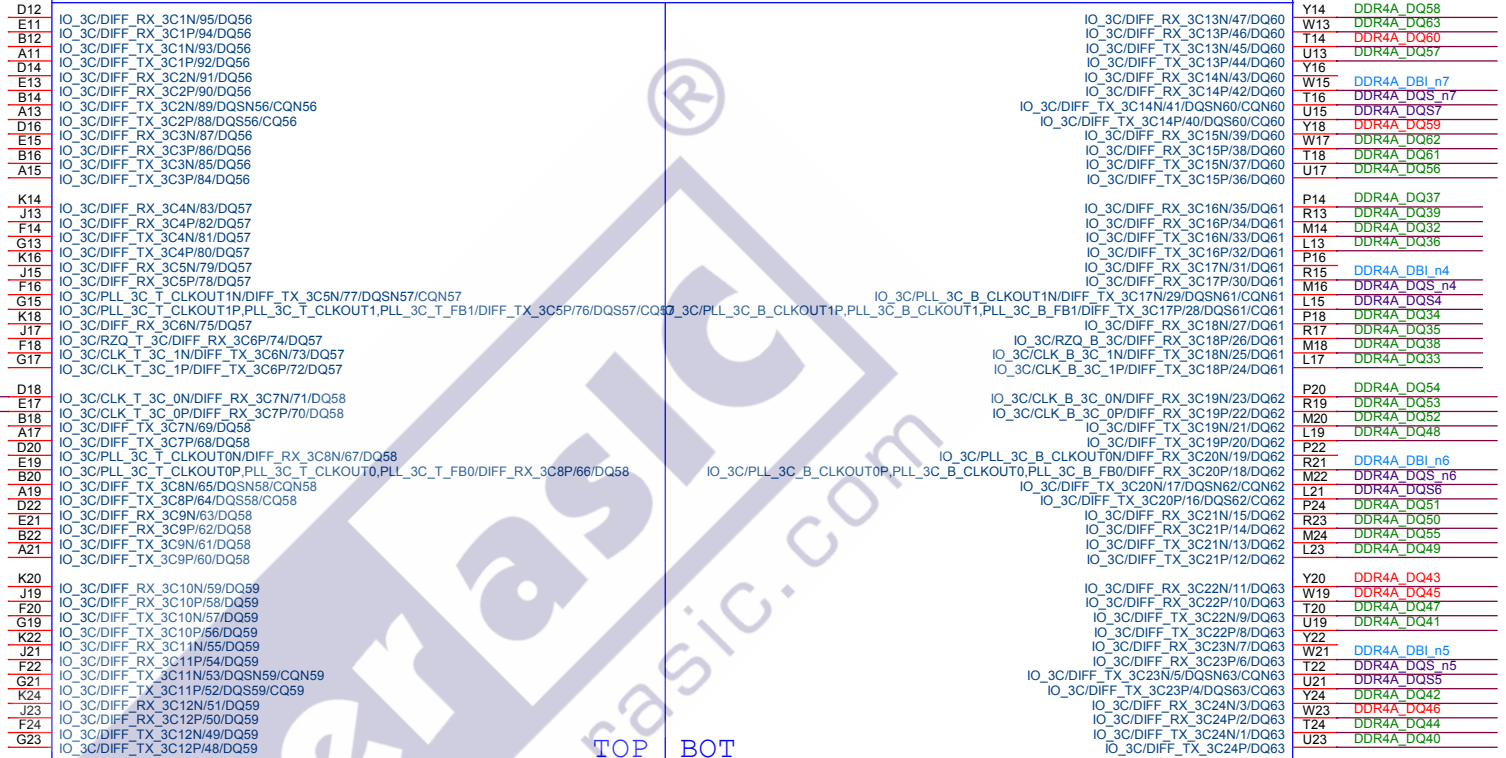
RAS_n is a multiplexed function with A16
CAS_n is a multiplexed function with A15
WE_n is a multiplexed function with A14

CLK_50_B3C_n
CLK_50_B3C_p



U35G

IO Bank 3C vccio = 1.2V



AGFB027R24C2E2V2R

TOP BOT

terasic			Copyright (c) 2017 by Terasic Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title					
A7SK					
Size	Document Number				Rev
B	FPGA Bank 3C				A
Date:	Wednesday, May 10, 2023		Sheet	15	of 52


U35H

IO Bank 3B vccio = 1.2V

K36	IO_3B/DIFF_RX_3B1N/95/DQ80	IO_3B/DIFF_RX_3B13N/47/DQ84	P36
J35	IO_3B/DIFF_RX_3B1P/94/DQ80	IO_3B/DIFF_RX_3B13P/46/DQ84	R35
F36	IO_3B/DIFF_TX_3B1N/93/DQ80	IO_3B/DIFF_TX_3B13N/45/DQ84	M36
G35	IO_3B/DIFF_TX_3B1P/92/DQ80	IO_3B/DIFF_TX_3B13P/44/DQ84	L35
K34	IO_3B/DIFF_RX_3B2N/91/DQ80	IO_3B/DIFF_RX_3B14N/43/DQ84	P34
J33	IO_3B/DIFF_RX_3B2P/90/DQ80	IO_3B/DIFF_RX_3B14P/42/DQ84	R33
F34	IO_3B/DIFF_TX_3B2N/89/DQSN80/CQN80	IO_3B/DIFF_TX_3B14N/41/DQSN84/CQN84	M34
G33	IO_3B/DIFF_TX_3B2P/88/DQSN80/CQ80	IO_3B/DIFF_TX_3B14P/40/DQSN84/CQ84	L33
K32	IO_3B/DIFF_RX_3B3N/87/DQ80	IO_3B/DIFF_RX_3B15N/39/DQ84	P32
J31	IO_3B/DIFF_RX_3B3P/86/DQ80	IO_3B/DIFF_RX_3B15P/38/DQ84	R31
F32	IO_3B/DIFF_TX_3B3N/85/DQ80	IO_3B/DIFF_TX_3B15N/37/DQ84	M32
G31	IO_3B/DIFF_TX_3B3P/84/DQ80	IO_3B/DIFF_TX_3B15P/36/DQ84	L31
D34	IO_3B/DIFF_RX_3B4N/83/DQ81	IO_3B/DIFF_RX_3B16N/35/DQ85	Y36
E33	IO_3B/DIFF_RX_3B4P/82/DQ81	IO_3B/DIFF_RX_3B16P/34/DQ85	W35
B34	IO_3B/DIFF_TX_3B4N/81/DQ81	IO_3B/DIFF_TX_3B16N/33/DQ85	T36
A33	IO_3B/DIFF_TX_3B4P/80/DQ81	IO_3B/DIFF_TX_3B16P/32/DQ85	U35
D32	IO_3B/DIFF_RX_3B5N/79/DQ81	IO_3B/DIFF_RX_3B17N/31/DQ85	Y34
E31	IO_3B/DIFF_RX_3B5P/78/DQ81	IO_3B/DIFF_RX_3B17P/30/DQ85	W33
B32	IO_3B/PLL_3B_T_CLKOUT1N/DIFF_TX_3B5N/77/DQSN81/CQN81	IO_3B/PLL_3B_B_CLKOUT1N/DIFF_TX_3B17N/29/DQSN85/CQN85	T34
A31	IO_3B/PLL_3B_T_CLKOUT1P,PLL_3B_T_CLKOUT1,PLL_3B_T_FB1/DIFF_TX_3B5P/76/DQSN81/CQ81	IO_3B/PLL_3B_B_CLKOUT1P,PLL_3B_B_CLKOUT1,PLL_3B_B_FB1/DIFF_TX_3B17P/28/DQSN85/CQ85	U33
D30	IO_3B/DIFF_RX_3B6N/75/DQ81	IO_3B/DIFF_RX_3B18N/27/DQ85	Y32
E29	IO_3B/RZQ_T_3B/DIFF_RX_3B6P/74/DQ81	IO_3B/RZQ_B_3B/DIFF_RX_3B18P/26/DQ85	W31
B30	IO_3B/CLK_T_3B_1N/DIFF_TX_3B6N/73/DQ81	IO_3B/CLK_B_3B_1N/DIFF_TX_3B18N/25/DQ85	T32
A29	IO_3B/CLK_T_3B_1P/DIFF_TX_3B6P/72/DQ81	IO_3B/CLK_B_3B_1P/DIFF_TX_3B18P/24/DQ85	U31
K30	IO_3B/CLK_T_3B_0N/DIFF_RX_3B7N/71/DQ82	IO_3B/CLK_B_3B_0N/DIFF_RX_3B19N/23/DQ86	P30
J29	IO_3B/CLK_T_3B_0P/DIFF_RX_3B7P/70/DQ82	IO_3B/CLK_B_3B_0P/DIFF_RX_3B19P/22/DQ86	R29
F30	IO_3B/DIFF_TX_3B7N/69/DQ82	IO_3B/DIFF_TX_3B19N/21/DQ86	M30
G29	IO_3B/DIFF_TX_3B7P/68/DQ82	IO_3B/DIFF_TX_3B19P/20/DQ86	L29
K28	IO_3B/PLL_3B_T_CLKOUT0N/DIFF_RX_3B8N/67/DQ82	IO_3B/PLL_3B_B_CLKOUT0N/DIFF_RX_3B20N/19/DQ86	P28
J27	IO_3B/PLL_3B_T_CLKOUT0P,PLL_3B_T_CLKOUT0,PLL_3B_T_FB0/DIFF_RX_3B8P/66/DQ82	IO_3B/PLL_3B_B_CLKOUT0P,PLL_3B_B_CLKOUT0,PLL_3B_B_FB0/DIFF_RX_3B20P/18/DQ86	R27
F28	IO_3B/DIFF_TX_3B8N/65/DQSN82/CQN82	IO_3B/DIFF_TX_3B20N/17/DQSN86/CQN86	M28
G27	IO_3B/DIFF_TX_3B8P/64/DQSN82/CQ82	IO_3B/DIFF_TX_3B20P/16/DQSN86/CQ86	L27
K26	IO_3B/DIFF_RX_3B9N/63/DQ82	IO_3B/DIFF_RX_3B21N/15/DQ86	P26
J25	IO_3B/DIFF_RX_3B9P/62/DQ82	IO_3B/DIFF_RX_3B21P/14/DQ86	R25
F26	IO_3B/DIFF_TX_3B9N/61/DQ82	IO_3B/DIFF_TX_3B21N/13/DQ86	M26
G25	IO_3B/DIFF_TX_3B9P/60/DQ82	IO_3B/DIFF_TX_3B21P/12/DQ86	L25
D28	IO_3B/DIFF_RX_3B10N/59/DQ83	IO_3B/DIFF_RX_3B22N/11/DQ87	Y30
E27	IO_3B/DIFF_RX_3B10P/58/DQ83	IO_3B/DIFF_RX_3B22P/10/DQ87	W29
B28	IO_3B/DIFF_TX_3B10N/57/DQ83	IO_3B/DIFF_TX_3B22N/9/DQ87	T30
A27	IO_3B/DIFF_TX_3B10P/56/DQ83	IO_3B/DIFF_TX_3B22P/8/DQ87	U29
D26	IO_3B/DIFF_RX_3B11N/55/DQ83	IO_3B/DIFF_RX_3B23N/7/DQ87	Y28
E25	IO_3B/DIFF_RX_3B11P/54/DQ83	IO_3B/DIFF_RX_3B23P/6/DQ87	W27
B26	IO_3B/DIFF_TX_3B11N/53/DQSN83/CQN83	IO_3B/DIFF_TX_3B23N/5/DQSN87/CQN87	T26
A25	IO_3B/DIFF_TX_3B11P/52/DQSN83/CQ83	IO_3B/DIFF_TX_3B23P/4/DQSN87/CQ87	U27
D24	IO_3B/DIFF_RX_3B12N/51/DQ83	IO_3B/DIFF_RX_3B24N/3/DQ87	Y26
E23	IO_3B/DIFF_RX_3B12P/50/DQ83	IO_3B/DIFF_RX_3B24P/2/DQ87	W25
B24	IO_3B/DIFF_TX_3B12N/49/DQ83	IO_3B/DIFF_TX_3B24N/1/DQ87	T26
A23	IO_3B/DIFF_TX_3B12P/48/DQ83	IO_3B/DIFF_TX_3B24P/DQ87	U25

AGFB027R24C2E2VR2

TOP BOT

 Copyright (c) 2017 by Terasic Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
A7SK		
Size	Document Number	Rev
B	FPGA Bank 3B	A
Date:	Wednesday, May 10, 2023	Sheet 16 of 52

CLK 50 B3A p 6
CLK 50 B3A n 6

CLK 100 B3A p 6
CLK 100 B3A n 6

DDR4A EVENT n 7
DDR4A SDA 7
DDR4A SCL 7

EXP EN 45

PCIe control signals

PCIE_WAKE n 41
PCIE_SMBDAT 41
PCIE_SMBCLK 41

PCIE_CLKREQ n 41

CPU_RESET n 8,43

2x5 Timing Header

GPIO_P13_01
GPIO_CLK0
GPIO_CLK1

HDMI Clocks

CLK_100 p 4
CLK_100 n 4
CLK_148M5 p 5
CLK_148M5 n 5

INFO_SPI_SCLK	D54	IO_3A/DIFF_RX_3A1N/95/DQ88
INFO_SPI_MOSI	E53	IO_3A/DIFF_RX_3A1P/94/DQ88
DVI_TX_SDA	D52	IO_3A/DIFF_TX_3A1N/83/DQ88
INFO_SPI_MISO	E51	IO_3A/DIFF_TX_3A1P/92/DQ88
GPIO_P13	D50	IO_3A/DIFF_RX_3A2N/91/DQ88
INFO_SPI_CS_n	E49	IO_3A/AVST_READY/DIFF_RX_3A2P/90/DQ88
DVI_TX_SCL	B50	IO_3A/AVST_DATA31/DIFF_TX_3A2P/88/DQ88
CPU_RESET_n	A49	IO_3A/AVST_DATA30/DIFF_TX_3A2P/88/DQ88
DVI_TX_CEC_IN_n	D48	IO_3A/AVST_DATA29/DIFF_RX_3A3N/87/DQ88
QSFP28_LP_MODE	E47	IO_3A/AVST_DATA28/DIFF_RX_3A3P/86/DQ88
DVI_TX_HPD_n	B48	IO_3A/AVST_DATA27/DIFF_TX_3A3N/85/DQ88
HDMI_TX_SCL	A47	IO_3A/AVST_DATA26/DIFF_TX_3A3P/84/DQ88
HDMI_TX_SDA	F50	IO_3A/AVST_DATA25/DIFF_RX_3A4N/83/DQ89
GPIO_CLK1	G49	IO_3A/AVST_DATA24/DIFF_RX_3A4P/82/DQ89
EXP_EN	F48	IO_3A/AVST_DATA23/DIFF_TX_3A4N/81/DQ89
DDR4A_EVENT_n	G47	IO_3A/AVST_DATA22/DIFF_TX_3A4P/80/DQ89
GPIO_P1	K46	IO_3A/AVST_DATA21/DIFF_RX_3A5N/79/DQ89
GPIO_CLK0	J45	IO_3A/AVST_DATA20/DIFF_RX_3A5P/78/DQ89
Si5340A1_I2C_SCL	F46	IO_3A/PLL_3A_T_CLKOUT1N/AVST_DATA19/DIFF_TX_3A5N/77/DQ89
GPIO_P2	G45	IO_3A/PLL_3A_T_CLKOUT1P,PLL_3A_T_CLKOUT1,PLL_3A_T_FB1/AVST_DATA18/DIFF_TX_3A5P/76/DQ89
Si5340A1_I2C_SDA	K44	IO_3A/PLL_3A_B_CLKOUT1N/AVST_DATA17/DIFF_RX_3A6N/75/DQ89
GPIO_P0	J43	IO_3A/RZQ_T_3A/AVST_DATA16/DIFF_RX_3A6P/74/DQ89
CLK_148M5_n	F44	IO_3A/CLK_T_3A_1N/DIFF_TX_3A6N/73/DQ89
CLK_148M5_p	G43	IO_3A/CLK_T_3A_1P/DIFF_TX_3A6P/72/DQ89
CLK_100_n	D46	IO_3A/CLK_T_3A_0N/DIFF_RX_3A7N/71/DQ90
CLK_100_p	E45	IO_3A/CLK_T_3A_0P/DIFF_RX_3A7P/70/DQ90
Si5340A0_I2C_SDA	B46	IO_3A/DIFF_TX_3A7N/69/DQ90
QSFP28_INTERRUPT_n	A45	IO_3A/DIFF_TX_3A7P/68/DQ90
Si5340A0_I2C_SCL	D44	IO_3A/PLL_3A_T_CLKOUT0N/DIFF_RX_3A8N/67/DQ90
Si5340A1_I2C_SCL	E43	IO_3A/PLL_3A_T_CLKOUT0P,PLL_3A_T_CLKOUT0,PLL_3A_T_FB0/DIFF_RX_3A8P/66/DQ90
Si5340A1_OE_n	B44	IO_3A/AVST_CLK/DIFF_TX_3A8N/65/DQ89
DVI_TX_5V	A43	IO_3A/AVST_DATA15/DIFF_TX_3A8P/64/DQ90
QSFP28_SCL	D42	IO_3A/AVST_DATA14/DIFF_RX_3A9N/63/DQ90
DVI_TX_CEC_OUT_n	B42	IO_3A/AVST_DATA13/DIFF_RX_3A9P/62/DQ90
Si5340A0_OE_n	D40	IO_3A/AVST_DATA12/DIFF_TX_3A9N/61/DQ90
QSFP28_SDA	E39	IO_3A/AVST_DATA11/DIFF_TX_3A9P/60/DQ90
Si5340A0_RST_n	B40	IO_3A/AVST_DATA10/DIFF_RX_3A10N/59/DQ91
QSFP28_MOD_PRS_n	A39	IO_3A/AVST_DATA9/DIFF_RX_3A10P/58/DQ91
PCIE_SMBDAT	D38	IO_3A/AVST_DATA8/DIFF_TX_3A10N/57/DQ91
DDR4A_SDA	E37	IO_3A/AVST_DATA7/DIFF_RX_3A11P/56/DQ91
QSFP28_RST_n	B38	IO_3A/AVST_DATA6/DIFF_RX_3A11P/54/DQ91
PCIE_CLKREQ_n	A37	IO_3A/AVST_DATA5/DIFF_TX_3A11N/53/DQ89
PCIE_WAKE_n	D36	IO_3A/AVST_DATA4/DIFF_TX_3A11P/52/DQ89
DDR4A_SCL	E35	IO_3A/AVST_DATA3/DIFF_RX_3A12N/51/DQ91
QSFP28_MOD_SEL_n	B36	IO_3A/AVST_DATA2/DIFF_RX_3A12P/50/DQ91
PCIE_SMBCLK	A35	IO_3A/AVST_DATA1/DIFF_TX_3A12N/49/DQ91
		IO_3A/AVST_DATA0/DIFF_TX_3A12P/48/DQ91

AGFB027R24C2E2VR2

FPGA/System MAX SPI

INFO_SPI_SCLK 8
INFO_SPI_CS_n 8
INFO_SPI_MOSI 8
INFO_SPI_MISO 8

Si5340A0 Interface

Si5340A0_I2C_SDA 4
Si5340A0_I2C_SCL 4
Si5340A0_RST_n 4
Si5340A0_OE_n 4

QSFP28 Control Interface

QSFP28_MOD_SEL_n 40
QSFP28_RST_n 40
QSFP28_SCL 40
QSFP28_SDA 40
QSFP28_LP_MODE 40
QSFP28_INTERRUPT_n 40
QSFP28_MOD_PRS_n 40

Si5340A1 Interface

Si5340A1_I2C_SDA 5
Si5340A1_I2C_SCL 5
Si5340A1_RST_n 5
Si5340A1_OE_n 5

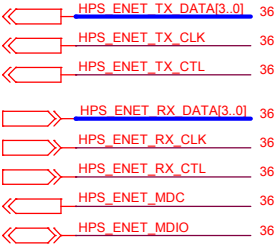
IO Bank 3A vccio = 1.2v

TOP BOT

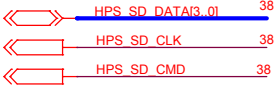
IO_3A/DIFF_RX_3A13N/47/DQ92	Y42
IO_3A/DIFF_RX_3A13P/46/DQ92	W41
IO_3A/DIFF_TX_3A13N/45/DQ92	T42
IO_3A/DIFF_TX_3A13P/44/DQ92	U41
IO_3A/DIFF_RX_3A14N/43/DQ92	Y40
IO_3A/DIFF_RX_3A14P/42/DQ92	W39
IO_3A/DIFF_TX_3A14N/41/DQ89	T40
IO_3A/DIFF_TX_3A14P/40/DQ89	U39
IO_3A/DIFF_RX_3A15N/39/DQ92	Y38
IO_3A/DIFF_RX_3A15P/38/DQ92	W37
IO_3A/DIFF_TX_3A15N/37/DQ92	T38
IO_3A/DIFF_TX_3A15P/36/DQ92	U37
IO_3A/DIFF_RX_3A16N/35/DQ93	M48
IO_3A/DIFF_RX_3A16P/34/DQ93	L47
IO_3A/DIFF_TX_3A16N/33/DQ93	K48
IO_3A/DIFF_TX_3A16P/32/DQ93	J47
IO_3A/DIFF_RX_3A17N/31/DQ93	P46
IO_3A/DIFF_RX_3A17P/30/DQ93	R45
IO_3A/DIFF_TX_3A17N/29/DQ93	M46
IO_3A/DIFF_TX_3A17P/28/DQ93	L45
IO_3A/DIFF_RX_3A18N/27/DQ93	P44
IO_3A/DIFF_RX_3A18P/26/DQ93	R43
IO_3A/CLK_B_3A_1N/DIFF_TX_3A18N/25/DQ93	M44
IO_3A/CLK_B_3A_1P/DIFF_TX_3A18P/24/DQ93	L43
IO_3A/CLK_B_3A_0N/DIFF_RX_3A19N/23/DQ94	P42
IO_3A/CLK_B_3A_0P/DIFF_RX_3A19P/22/DQ94	R41
IO_3A/DIFF_TX_3A19N/21/DQ94	M42
IO_3A/DIFF_TX_3A19P/20/DQ94	L41
IO_3A/PLL_3A_B_CLKOUT0N/DIFF_RX_3A20N/19/DQ94	P40
IO_3A/PLL_3A_B_CLKOUT0P,PLL_3A_B_CLKOUT0,PLL_3A_B_FB0/DIFF_RX_3A20P/18/DQ94	R39
IO_3A/DIFF_TX_3A20N/17/DQ89	M40
IO_3A/DIFF_TX_3A20P/16/DQ89	L39
IO_3A/DIFF_RX_3A21N/15/DQ94	P38
IO_3A/DIFF_RX_3A21P/14/DQ94	R37
IO_3A/DIFF_TX_3A21N/13/DQ94	M38
IO_3A/DIFF_TX_3A21P/12/DQ94	L37
IO_3A/DIFF_RX_3A22N/11/DQ95	K42
IO_3A/DIFF_RX_3A22P/10/DQ95	J41
IO_3A/DIFF_TX_3A22N/9/DQ95	F42
IO_3A/DIFF_TX_3A22P/8/DQ95	G41
IO_3A/DIFF_RX_3A23N/7/DQ95	K40
IO_3A/DIFF_RX_3A23P/6/DQ95	J39
IO_3A/DIFF_TX_3A23N/5/DQ89	F40
IO_3A/DIFF_TX_3A23P/4/DQ89	G39
IO_3A/DIFF_RX_3A24N/3/DQ95	K38
IO_3A/DIFF_RX_3A24P/2/DQ95	J37
IO_3A/DIFF_TX_3A24N/1/DQ95	F38
IO_3A/DIFF_TX_3A24P/0/DQ95	G37

Title		
A7SK		
Size B	Document Number FPGA Bank 3A	Rev A
Date:	Wednesday, May 10, 2023	Sheet 17 of 52

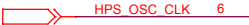
Ethernet PHY Interface (RGMII)



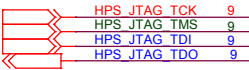
SD Card Interface



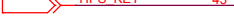
HPS 25MHz Clock



HPS JTAG Interface



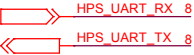
HPS User Button



HPS User LED



UART Interface




FPGA Bank - HPS

U35.J

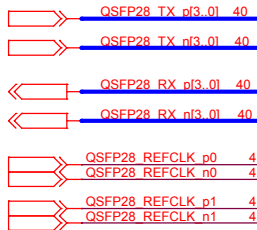
HPS Bank vccio = 1.8v

AC15 HPS_IOA_1/GPIO0_IO0,SPIM0_SS1_N,SPIS0_CLK,UART0_CTS_N,NAND_ADO0,USB0_CLK,SDMMC_CCLK
AL15 HPS_IOA_2/GPIO0_IO1,SPIM1_SS1_N,SPIS0_MOSI,UART0_RTS_N,NAND_ADO1,USB0_STP,SDMMC_CMD
AJ11 HPS_IOA_3/GPIO0_IO2,SPIS0_SS0_N,UART0_TX,I2C1_SDA,NAND_WE_N,USB0_DIR,SDMMC_DATA0
AM16 HPS_IOA_4/GPIO0_IO3,SPIS0_MISO,UART0_RX,I2C1_SCL,NAND_RE_N,USB0_DATA0,SDMMC_DATA1
AH12 HPS_IOA_5/GPIO0_IO4,SPIM0_CLK,UART1_CTS_N,I2C0_SDA,NAND_WP_N,USB0_DATA1,SDMMC_DATA2
AN15 HPS_IOA_6/GPIO0_IO5,SPIM0_MOSI,UART1_RTS_N,I2C0_SCL,NAND_ADO2,USB0_NXT,SDMMC_DATA3
AG13 HPS_IOA_7/GPIO0_IO6,SPIM0_MISO,MDIO2_MDIO,UART1_TX,I2C_EMAC2_SDA,NAND_ADO3,USB0_DATA2,SDMMC_DATA4
AP16 HPS_IOA_8/GPIO0_IO7,SPIM0_SS0_N,MDIO2_MDC,UART1_RX,I2C_EMAC2_SCL,NAND_CLE,USB0_DATA3,SDMMC_DATA5
AF14 HPS_IOA_9/GPIO0_IO8,SPIM1_CLK,SPIS1_CLK,MDIO1_MDIO,I2C_EMAC1_SDA,NAND_ADO4,USB0_DATA4,SDMMC_DATA6
AT16 HPS_IOA_10/GPIO0_IO9,SPIM1_MOSI,SPIS1_MOSI,MDIO1_MDC,I2C_EMAC1_SCL,NAND_ADO5,USB0_DATA5,SDMMC_DATA7
AH10 HPS_IOA_11/GPIO0_IO10,SPIM1_MISO,SPIS1_SS0_N,MDIO0_MDIO,I2C_EMAC0_SDA,NAND_ADO6,USB0_DATA6
AU15 HPS_IOA_12/GPIO0_IO11,SPIM1_SS0_N,SPIS1_MISO,MDIO0_MDC,I2C_EMAC0_SCL,NAND_ADO7,USB0_DATA7
AJ7 HPS_IOA_13/GPIO0_IO12,NAND_ALE,USB1_CLK,EMAC0_TX_CTL
AL13 HPS_IOA_14/GPIO0_IO13,NAND_RB,USB1_STP,EMAC0_TX_CTL
AH8 HPS_IOA_15/GPIO0_IO14,NAND_CE_N,USB1_DIR,EMAC0_RX_CTL
AM14 HPS_IOA_16/GPIO0_IO15,USB1_DATA0,EMAC0_RX_CTL
AD14 HPS_IOA_17/GPIO0_IO16,NAND_ADO8,USB1_DATA1,EMAC0_TXD0
AN13 HPS_IOA_18/GPIO0_IO17,NAND_ADO9,USB1_NXT,EMAC0_TXD1
AG11 HPS_IOA_19/GPIO0_IO18,NAND_ADO10,USB1_DATA2,EMAC0_RXD0
AP14 HPS_IOA_20/GPIO0_IO19,SPIM1_SS1_N,NAND_ADO11,USB1_DATA3,EMAC0_RXD1
AG9 HPS_IOA_21/GPIO0_IO20,SPIM1_CLK,SPIS0_CLK,UART0_CTS_N,I2C1_SDA,NAND_ADO12,USB1_DATA4,EMAC0_TXD2
AF12 HPS_IOA_22/GPIO0_IO21,SPIM1_MOSI,SPIS0_MOSI,UART0_RTS_N,I2C1_SCL,NAND_ADO13,USB1_DATA5,EMAC0_TXD3
AU13 HPS_IOA_23/GPIO0_IO22,SPIM1_MISO,SPIS0_SS0_N,UART0_TX,I2C0_SDA,NAND_ADO14,USB1_DATA6,EMAC0_RXD2
AF10 HPS_IOA_24/GPIO0_IO23,SPIM1_SS0_N,SPIS0_MISO,UART0_RX,I2C0_SCL,NAND_ADO15,USB1_DATA7,EMAC0_RXD3
AU11 HPS_IOB_1/GPIO1_IO0,SPIM1_CLK,UART0_CTS_N,NAND_ADO0,EMAC1_TX_CTL
AF8 HPS_IOB_2/GPIO1_IO1,SPIM1_MOSI,UART0_RTS_N,NAND_ADO1,EMAC1_TX_CTL
AT12 HPS_IOB_3/GPIO1_IO2,SPIM1_MISO,UART0_TX,I2C0_SDA,NAND_WE_N,EMAC1_RX_CTL
AG7 HPS_IOB_4/GPIO1_IO3,SPIM1_SS0_N,UART0_RX,I2C0_SCL,NAND_RE_N,EMAC1_RX_CTL
AP12 HPS_IOB_5/GPIO1_IO4,SPIM1_SS1_N,SPIS1_CLK,UART1_CTS_N,NAND_WP_N,EMAC1_TXD0
AC13 HPS_IOB_6/GPIO1_IO5,SPIS1_MOSI,UART1_RTS_N,NAND_ADO2,EMAC1_TXD1
AN11 HPS_IOB_7/GPIO1_IO6,SPIS1_SS0_N,UART1_TX,I2C1_SDA,NAND_ADO3,EMAC1_RXD0
AD12 HPS_IOB_8/GPIO1_IO7,SPIS1_MISO,UART1_RX,I2C1_SCL,NAND_CLE,EMAC1_RXD1
AM12 HPS_IOB_9/GPIO1_IO8,JTAG_TCK,SPIS0_CLK,MDIO2_MDIO,I2C_EMAC2_SDA,NAND_ADO4,EMAC1_TXD2
AD10 HPS_IOB_10/GPIO1_IO9,JTAG_TMS,SPIS0_MOSI,MDIO2_MDC,I2C_EMAC2_SCL,NAND_ADO5,EMAC1_TXD3
AL11 HPS_IOB_11/GPIO1_IO10,JTAG_TDO,SPIS0_SS0_N,MDIO0_MDIO,I2C_EMAC0_SDA,NAND_ADO6,EMAC1_RXD2
AC11 HPS_IOB_12/GPIO1_IO11,JTAG_TDI,SPIS0_MISO,MDIO0_MDC,I2C_EMAC0_SCL,NAND_ADO7,EMAC1_RXD3
AT10 HPS_IOB_13/GPIO1_IO12,I2C1_SDA,NAND_ALE,SDMMC_DATA0,EMAC2_TX_CTL
AD8 HPS_IOB_14/GPIO1_IO13,I2C1_SCL,NAND_RB,SDMMC_CMD,EMAC2_TX_CTL
AP10 HPS_IOB_15/GPIO1_IO14,UART1_TX,NAND_CE_N,SDMMC_CCLK,EMAC2_RX_CTL
AC9 HPS_IOB_16/GPIO1_IO15,UART1_RX,SDMMC_DATA1,EMAC2_RX_CTL
AM10 HPS_IOB_17/GPIO1_IO16,UART1_CTS_N,NAND_ADO8,SDMMC_DATA2,EMAC2_TXD0
AB10 HPS_IOB_18/GPIO1_IO17,SPIM0_SS1_N,UART1_RTS_N,NAND_ADO9,SDMMC_DATA3,EMAC2_TXD1
AJ13 HPS_IOB_19/GPIO1_IO18,SPIM0_MISO,MDIO1_MDIO,I2C_EMAC1_SDA,NAND_ADO10,SDMMC_DATA4,EMAC2_RXD0
AB14 HPS_IOB_20/GPIO1_IO19,SPIM0_SS0_N,MDIO1_MDC,I2C_EMAC1_SCL,NAND_ADO11,SDMMC_DATA5,EMAC2_RXD1
AH14 HPS_IOB_21/GPIO1_IO20,SPIM0_CLK,SPIS1_CLK,I2C_EMAC2_SDA,NAND_ADO12,SDMMC_DATA6,EMAC2_TXD2
AB12 HPS_IOB_22/GPIO1_IO21,SPIM0_MOSI,SPIS1_MOSI,I2C_EMAC2_SCL,NAND_ADO13,SDMMC_DATA7,EMAC2_TXD3
AJ9 HPS_IOB_23/GPIO1_IO22,SPIM0_MISO,SPIS1_SS0_N,MDIO0_MDIO,I2C_EMAC0_SDA,NAND_ADO14,EMAC2_RXD2
CH50 HPS_IOB_24/GPIO1_IO23,SPIM0_SS0_N,SPIS1_MISO,MDIO0_MDC,I2C_EMAC0_SCL,NAND_ADO15,EMAC2_RXD3
CF50 DNU_5
DNU_6

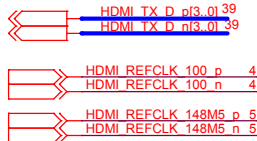
AGFB027R24C2E2VR2

 Copyright (c) 2017 by Terasic Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
A7SK		
Size	Document Number	Rev
B	FPGA Bank HPS	A
Date:	Wednesday, May 10, 2023	Sheet 18 of 52

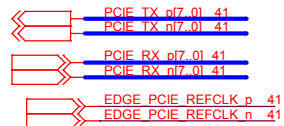
QSFP28 Transceivers



HDMI TX Transceivers



PCIe Transceiver



FPGA Temperature diode

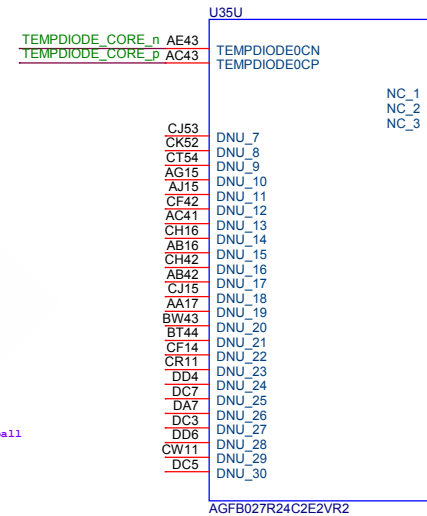


Core

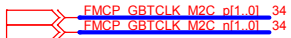
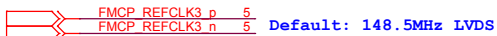
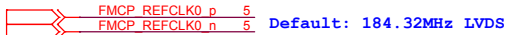
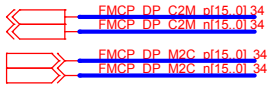


U35K

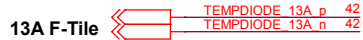
F-TILE Bank 12C



FMC+ Transceiver



FPGA Temperature diode



U35L

F-TILE Bank 13A

FMCP_DP_M2C_n0 AG5
FMCP_DP_M2C_p0 AF4
FMCP_DP_M2C_n1 AH2
FMCP_DP_M2C_p1 AJ1
FMCP_DP_M2C_n2 AM2
FMCP_DP_M2C_p2 AN1
FMCP_DP_M2C_n3 AT2
FMCP_DP_M2C_p3 AU1

FMCP_DP_M2C_n4 AY2
FMCP_DP_M2C_p4 BA1
FMCP_DP_M2C_n5 BD2
FMCP_DP_M2C_p5 BE1
FMCP_DP_M2C_n6 BH2
FMCP_DP_M2C_p6 BJ1
FMCP_DP_M2C_n7 BM2
FMCP_DP_M2C_p7 BN1

FMCP_DP_M2C_n8 BT2
FMCP_DP_M2C_p8 BU1
FMCP_DP_M2C_n9 BY2
FMCP_DP_M2C_p9 CA1
FMCP_DP_M2C_n10 CD2
FMCP_DP_M2C_p10 CE1
FMCP_DP_M2C_n11 CH2
FMCP_DP_M2C_p11 CJ1

FMCP_DP_M2C_n12 CM2
FMCP_DP_M2C_p12 CN1
FMCP_DP_M2C_n13 CR5
FMCP_DP_M2C_p13 CP4
FMCP_DP_M2C_n14 CT2
FMCP_DP_M2C_p14 CU1
FMCP_DP_M2C_n15 CW5
FMCP_DP_M2C_p15 CV4

FMCP_REFCLK3_n BJ7
FMCP_REFCLK3_p BH8

FMCP_REFCLK0_n BU7
FMCP_REFCLK0_p BR7
FMCP_REFCLK1_n BN7
FMCP_REFCLK1_p BP8
FMCP_REFCLK2_n BV8
FMCP_REFCLK2_p BW7
FMCP_GBTCLK_M2C_n0 CD7
FMCP_GBTCLK_M2C_p0 CD8
FMCP_GBTCLK_M2C_n1 CH8
FMCP_GBTCLK_M2C_p1 CJ7

CD10
CF10
CG7
CE7
CG11
CH10
CV10
CN11

FGTR13A_RX_Q0_CH0N
FGTR13A_RX_Q0_CH0P
FGTR13A_RX_Q0_CH1N
FGTR13A_RX_Q0_CH1P
FGTR13A_RX_Q0_CH2N
FGTR13A_RX_Q0_CH2P
FGTR13A_RX_Q0_CH3N
FGTR13A_RX_Q0_CH3P

FGTR13A_RX_Q1_CH0N
FGTR13A_RX_Q1_CH0P
FGTR13A_RX_Q1_CH1N
FGTR13A_RX_Q1_CH1P
FGTR13A_RX_Q1_CH2N
FGTR13A_RX_Q1_CH2P
FGTR13A_RX_Q1_CH3N
FGTR13A_RX_Q1_CH3P

FGTR13A_RX_Q2_CH0N
FGTR13A_RX_Q2_CH0P
FGTR13A_RX_Q2_CH1N
FGTR13A_RX_Q2_CH1P
FGTR13A_RX_Q2_CH2N
FGTR13A_RX_Q2_CH2P
FGTR13A_RX_Q2_CH3N
FGTR13A_RX_Q2_CH3P

FGTR13A_RX_Q3_CH0N
FGTR13A_RX_Q3_CH0P
FGTR13A_RX_Q3_CH1N
FGTR13A_RX_Q3_CH1P
FGTR13A_RX_Q3_CH2N
FGTR13A_RX_Q3_CH2P
FGTR13A_RX_Q3_CH3N
FGTR13A_RX_Q3_CH3P

REFCLK_FGTR13A_Q0_RX_CH0N
REFCLK_FGTR13A_Q0_RX_CH0P
REFCLK_FGTR13A_Q0_RX_CH1N
REFCLK_FGTR13A_Q0_RX_CH1P
REFCLK_FGTR13A_Q1_RX_CH2N
REFCLK_FGTR13A_Q1_RX_CH2P
REFCLK_FGTR13A_Q1_RX_CH3N
REFCLK_FGTR13A_Q1_RX_CH3P
REFCLK_FGTR13A_Q2_RX_CH4N
REFCLK_FGTR13A_Q2_RX_CH4P
REFCLK_FGTR13A_Q2_RX_CH5N
REFCLK_FGTR13A_Q2_RX_CH5P
REFCLK_FGTR13A_Q3_RX_CH6N
REFCLK_FGTR13A_Q3_RX_CH6P
REFCLK_FGTR13A_Q3_RX_CH7N
REFCLK_FGTR13A_Q3_RX_CH7P
REFCLK_FGTR13A_Q2_CH8P
REFCLK_FGTR13A_Q3_CH9P
REFCLK_FGTR13A_Q3_CH9P

ENB_GXF_FHT13A

IO_PLL_REFCLK_13A_GXF

FGTR13A_TX_Q0_CH0N
FGTR13A_TX_Q0_CH0P
FGTR13A_TX_Q0_CH1N
FGTR13A_TX_Q0_CH1P
FGTR13A_TX_Q0_CH2N
FGTR13A_TX_Q0_CH2P
FGTR13A_TX_Q0_CH3N
FGTR13A_TX_Q0_CH3P

FGTR13A_TX_Q1_CH0N
FGTR13A_TX_Q1_CH0P
FGTR13A_TX_Q1_CH1N
FGTR13A_TX_Q1_CH1P
FGTR13A_TX_Q1_CH2N
FGTR13A_TX_Q1_CH2P
FGTR13A_TX_Q1_CH3N
FGTR13A_TX_Q1_CH3P

FGTR13A_TX_Q2_CH0N
FGTR13A_TX_Q2_CH0P
FGTR13A_TX_Q2_CH1N
FGTR13A_TX_Q2_CH1P
FGTR13A_TX_Q2_CH2N
FGTR13A_TX_Q2_CH2P
FGTR13A_TX_Q2_CH3N
FGTR13A_TX_Q2_CH3P

FGTR13A_TX_Q3_CH0N
FGTR13A_TX_Q3_CH0P
FGTR13A_TX_Q3_CH1N
FGTR13A_TX_Q3_CH1P
FGTR13A_TX_Q3_CH2N
FGTR13A_TX_Q3_CH2P
FGTR13A_TX_Q3_CH3N
FGTR13A_TX_Q3_CH3P

RCOMP_N_Q2_CH1_FGT_13A_GXF
RCOMP_P_Q2_CH1_FGT_13A_GXF

I_PIN_PERST_N_13A_GXF

TEMPDIODE4P
TEMPDIODE4N

APROBE_GXF_FGT13A_Q0_CH3
APROBE_GXF_FGT13A_Q2_CH3
APROBE_GXF_FGT13A_Q3_CH3
APROBE2_GXF_FGT13A_Q3_CH3

AL5 FMCP_DP_C2M_n0
AK4 FMCP_DP_C2M_p0
AM8 FMCP_DP_C2M_n1
AN7 FMCP_DP_C2M_p1
AR5 FMCP_DP_C2M_n2
AP4 FMCP_DP_C2M_p2
AT8 FMCP_DP_C2M_n3
AU7 FMCP_DP_C2M_p3

AW5 FMCP_DP_C2M_n4
AV4 FMCP_DP_C2M_p4
AY8 FMCP_DP_C2M_n5
BA7 FMCP_DP_C2M_p5
BC5 FMCP_DP_C2M_n6
BB4 FMCP_DP_C2M_p6
BG5 FMCP_DP_C2M_n7
BF4 FMCP_DP_C2M_p7

BL5 FMCP_DP_C2M_n8
BK4 FMCP_DP_C2M_p8
BR5 FMCP_DP_C2M_n9
BP4 FMCP_DP_C2M_p9
BW5 FMCP_DP_C2M_n10
BV4 FMCP_DP_C2M_p10
CC5 FMCP_DP_C2M_n11
CB4 FMCP_DP_C2M_p11

CG5 FMCP_DP_C2M_n12
CF4 FMCP_DP_C2M_p12
CL5 FMCP_DP_C2M_n13
CK4 FMCP_DP_C2M_p13
CM5 FMCP_DP_C2M_n14
CN7 FMCP_DP_C2M_p14
CT8 FMCP_DP_C2M_n15
CU7 FMCP_DP_C2M_p15

Layout Note: place the resistor under BGA ball

CA7 R402 499 (+/- 0.1%)
BY8

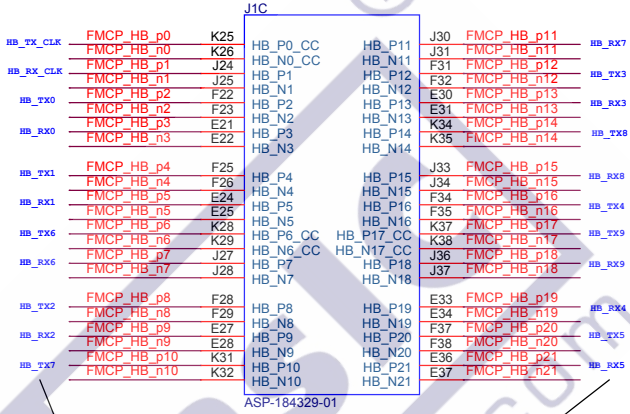
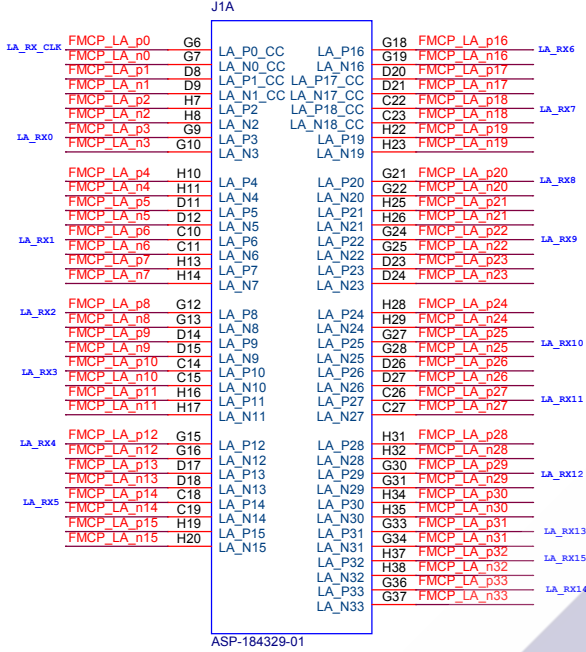
CG13 FMCP_RES0

CB12 TEMPDIODE_13A_p
CA11 TEMPDIODE_13A_n

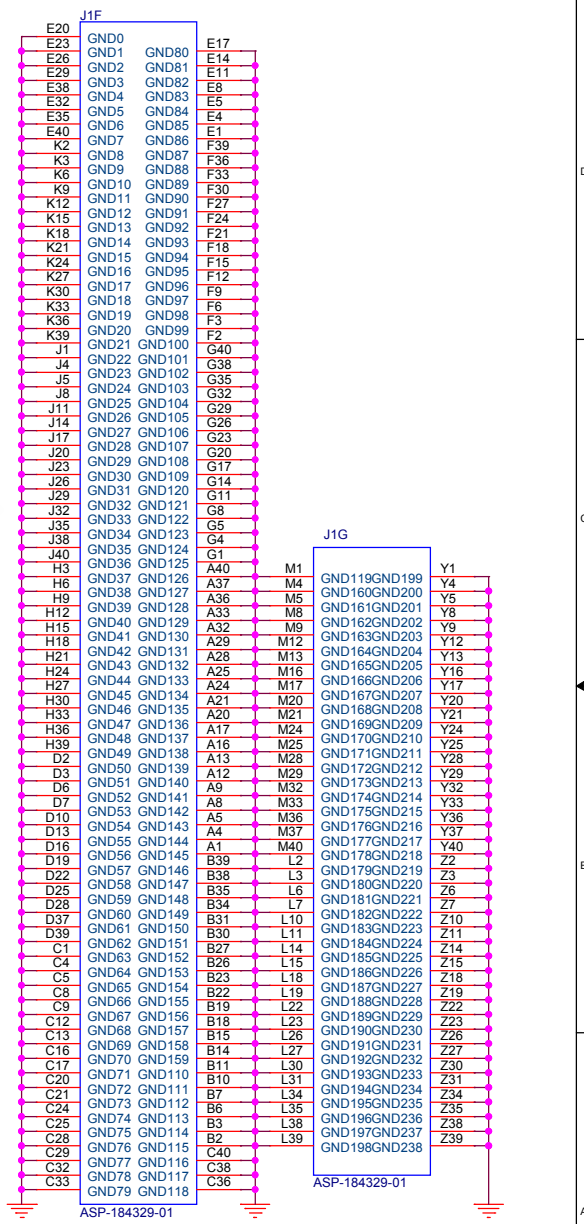
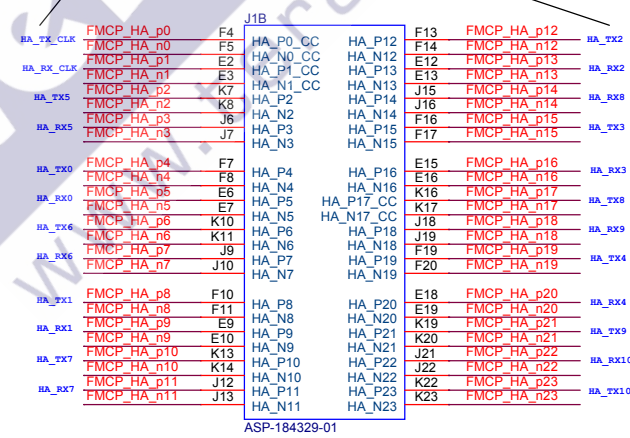
BL7
CB8
CK10
CJ9

FMC+ PORT INTERFACE(HPC)

FMC+ 1



The blue RX and TX affixtures are applied only for True Differential Signaling signals. If you do not use True Differential Signaling signals, you can configure each differential I/O buffer as RX or TX



terasic Copyright (c) 2017 by Terasic Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.

Title: A7SK

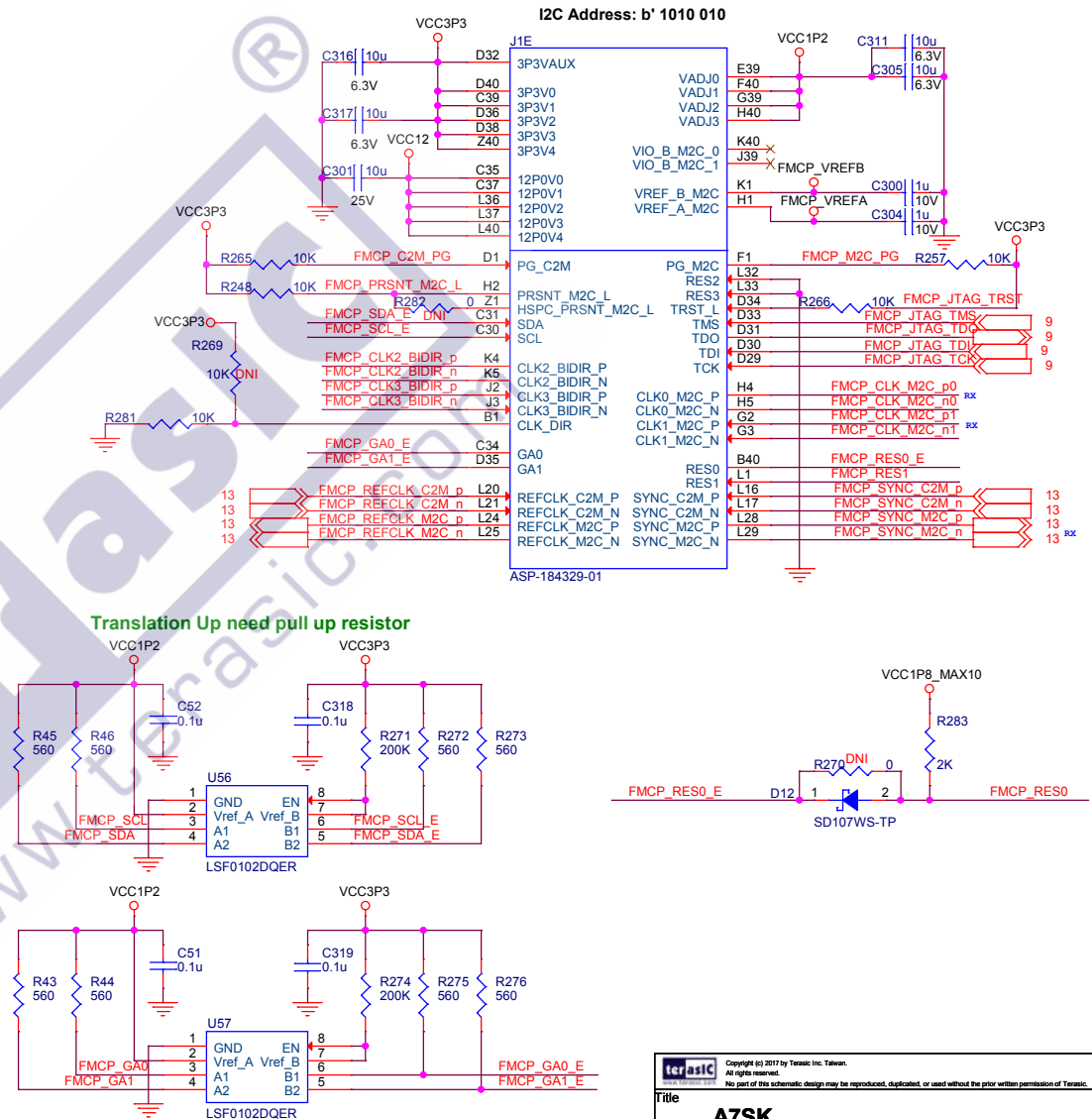
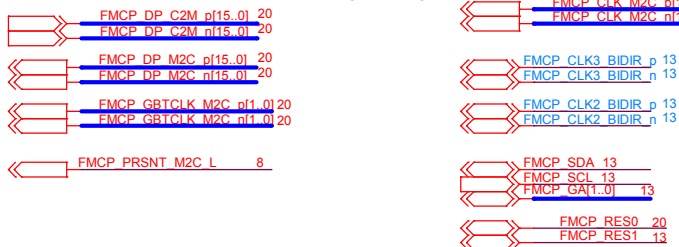
Size: B Document Number: FMC+1 Rev: A

Date: Tuesday, March 21, 2023 Sheet: 33 of 52

FMC+ 2



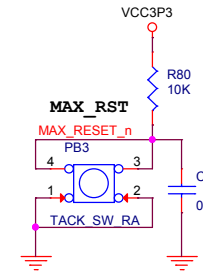
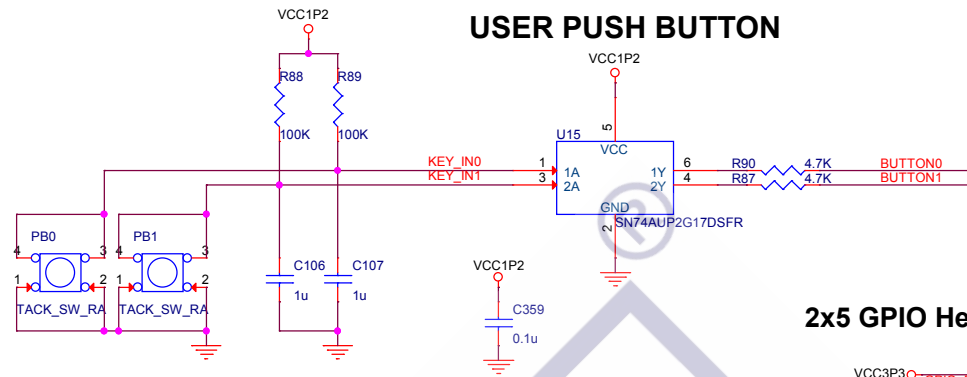
FMC+ PORT INTERFACE(HPC)



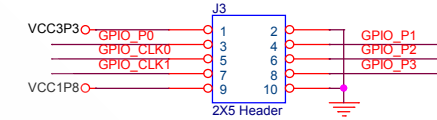
terasic Copyright (c) 2017 by Terasic Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
A7SK		
Size	Document Number	Rev
B	FMC+ 2	A
Date:	Tuesday, March 21, 2023	Sheet 34 of 52

USER PUSH BUTTON

8 << MAX_RESET_n
8,17 << CPU_RESET_n
13 << BUTTON1.0I

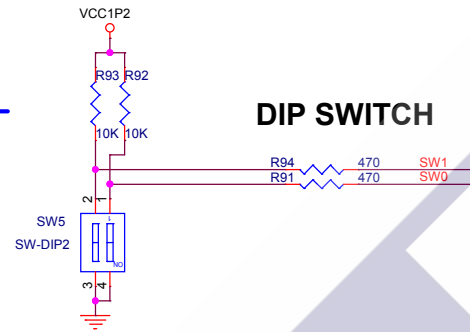


2x5 GPIO Header (Timing Expansion Header)



17 << GPIO_P3_0I
17 << GPIO_CLK0
17 << GPIO_CLK1

DIP SWITCH



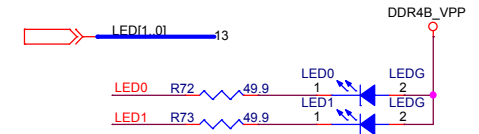
13 << SW1.0I

HPS User LED

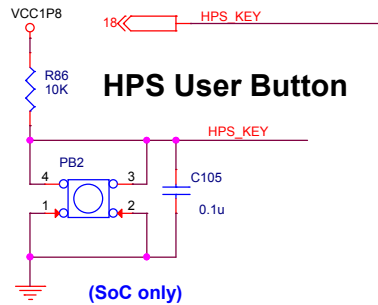


(SoC only)

USER LEDS

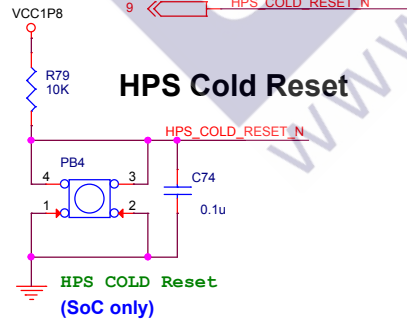


HPS User Button



(SoC only)

HPS Cold Reset



HPS COLD Reset
(SoC only)

terasic Copyright (c) 2017 by Terasic Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title		
A7SK		
Size	Document Number	Rev
B	GPIO, Button, Switch, User LED	A
Date:	Tuesday, March 21, 2023	Sheet 43 of 52