



**ULTRA LOW JITTER, ANY-FREQUENCY, ANY-OUTPUT
CLOCK GENERATOR
Si5341, Si5340
FAMILY REFERENCE MANUAL**

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1. Overview

The Si5341/40 Clock Generators combine MultiSynth™ technologies to enable any-frequency clock generation for applications that require the highest level of jitter performance. These devices are programmable via a serial interface with in-circuit programmable non-volatile memory (NVM) ensuring power up with a known frequency configuration. Using patented MultiSynth™ technology, the Si5341/40 generates up to 10 unique clock frequencies, each with 0 ppm frequency synthesis error. Each output clock has an independent VDDO reference and selectable signal format, simplifying format/level translation. The loop filter is fully integrated on-chip eliminating the risk of potential noise coupling associated with discrete solutions. The Si5341/40 is ideally suited for simplifying clock tree design by minimizing the number of timing components required. The Si5341/40 supports factory or in-circuit programmable non-volatile memory, enabling the device to power up in a user-specified configuration. The default configuration may be overwritten at any time by reprogramming the device via I2C/SPI.

1.1. Work Flow Expectations with ClockBuilder Pro and the Register Map

This reference manual is to be used to describe all the functions and features of the parts in the product family with register map details on how to implement them. It is important to understand that the intent is for customers to use the ClockBuilder Pro software to provide the initial configuration for the device. Although the register map is documented, all the details of the algorithms to implement a valid frequency plan are fairly complex and are beyond the scope of this document. Real-time changes to the frequency plan and other operating settings are supported by the devices. However, describing all the possible changes are not a primary purpose of this document. Refer to Applications Notes and [Knowledge Base](#) article links within the ClockBuilder Pro GUI for information on how to implement the most common, real-time frequency plan changes.

The primary purpose of the software is that it saves having to understand all the complexities of the device. The software abstracts the details from the user to allow focus on the high level input and output configuration, making it intuitive to understand and configure for the end application. The software walks the user through each step, with explanations about each configuration step in the process to explain the different options available. The software will restrict the user from entering an invalid combination of selections. The final configuration settings can be saved, written to an EVB and a custom part number can be created for customers who prefer to order a factory preprogrammed device. The final register maps can be exported to text files, and comparisons can be done by viewing the settings in the register map described in this document.

- Crystal Layout Guidelines with Recommended Crystals
- Device Specific Layout Guidelines
- Power Management and Filtering
- Output Driver Signal Swings and Terminations
- In-Circuit Programming

1.2. Family Product Comparison

Table 1 lists a comparison of the different family members.

Table 1. Product Selection Guide

Part Number	Number of Inputs	Number of Fractional Dividers	Number of Outputs	Package Type
Si5340	4	5	10	64-pin QFN
Si5341	4	4	4	44-pin QFN

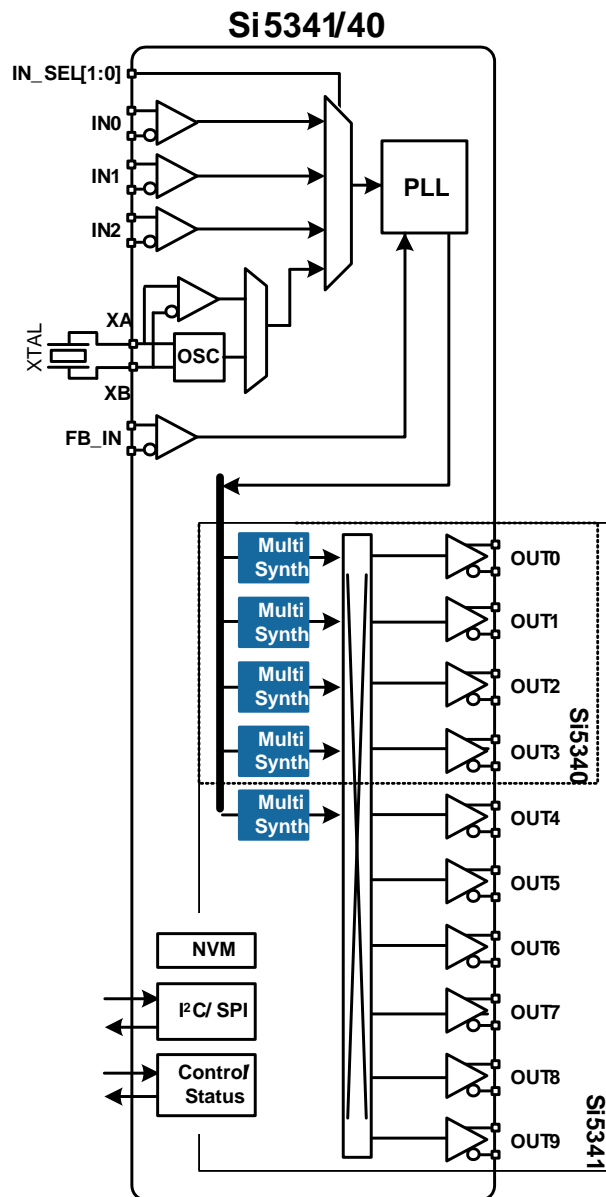


Figure 1. Block Diagram Si5341/40

1.3. Available Software Tools and Support

ClockBuilder Pro is a software tool that is used for the Si5341/40 family and other product families, capable of configuring the timing chip in an intuitive friendly step by step process. The software abstracts the details from the user to allow focus on the high level input and output configuration, making it intuitive to understand and configure for the end application. The software walks the user through each step, with explanations about each configuration step in the process to explain the different options available. The software will restrict the user from entering an invalid combination of selections. The final configuration settings can be saved, written to a device or written to the EVB and a custom part number can be created. ClockBuilder Pro integrates all the datasheets, application notes and information that might be helpful in one environment. It is intended that customers will use the software tool for the proper configuration of the device. Register map descriptions are given in the document should not be the only source of information for programming the device. The complexity of the algorithms is embedded in the software tool.

2. Functional Description

The Si5341/40 uses next generation MultiSynth™ technology to offer the industry's most frequency-flexible, high performance clock generator. The PLL locks to either an external crystal (XA/XB) or to an external input on XAXB, IN0, IN1 or IN2. The input frequency (crystal or external input) is multiplied by the DSPLL and divided by the MultiSynth™ stage and R divider to any frequency in the range of 100 Hz to 800 MHz per output. The phase-locked loop is fully contained and does not require external loop filter components to operate. Its function is to phase lock to the selected input and provide a common reference to all the output MultiSynth high-performance fractional dividers (N). The high-resolution fractional MultiSynth™ dividers enables true any-frequency input to any-frequency on any of the outputs. A crosspoint mux connects any of the MultiSynth divided frequencies to any of the outputs drivers. Additional output integer dividers (R) provide further frequency division if required. The frequency configuration of the device is programmed by setting the input dividers (P), the DSPLL feedback fractional divider (M_NUM/M_DEN), the MultiSynth fractional dividers (N_NUM/N_DEN), and the output integer dividers (R). Silicon Labs' Clockbuilder Pro configuration utility determines the optimum divider values for any desired input and output frequency plan.

The output drivers offer flexible output formats which are independently configurable on each of the outputs. This clock generator is fully configurable via its serial interface (I²C/SPI) and includes in-circuit programmable non-volatile memory. The block diagram for the Si5341 is shown in Figure 2, and the block diagram for the Si5340 is shown in Figure 3.

2.1. Work Flow Expectations with ClockBuilder Pro™ and the Register Map

This reference manual is to be used to describe all the functions and features of the parts in the product family with register map details on how to implement them. It is important to understand that the intent is for customers to use the ClockBuilder Pro software to provide the initial configuration for the device. Although the register map is documented, all the details of the algorithms to implement a valid frequency plan are fairly complex and are beyond the scope of this document. Real-time changes to the frequency plan and other operating settings are supported by the devices. However, describing all the possible changes are not a primary purpose of this document. Refer to Applications Notes and [Knowledge Base](#) article links within the ClockBuilder Pro GUI for information on how to implement the most common, real-time frequency plan changes.

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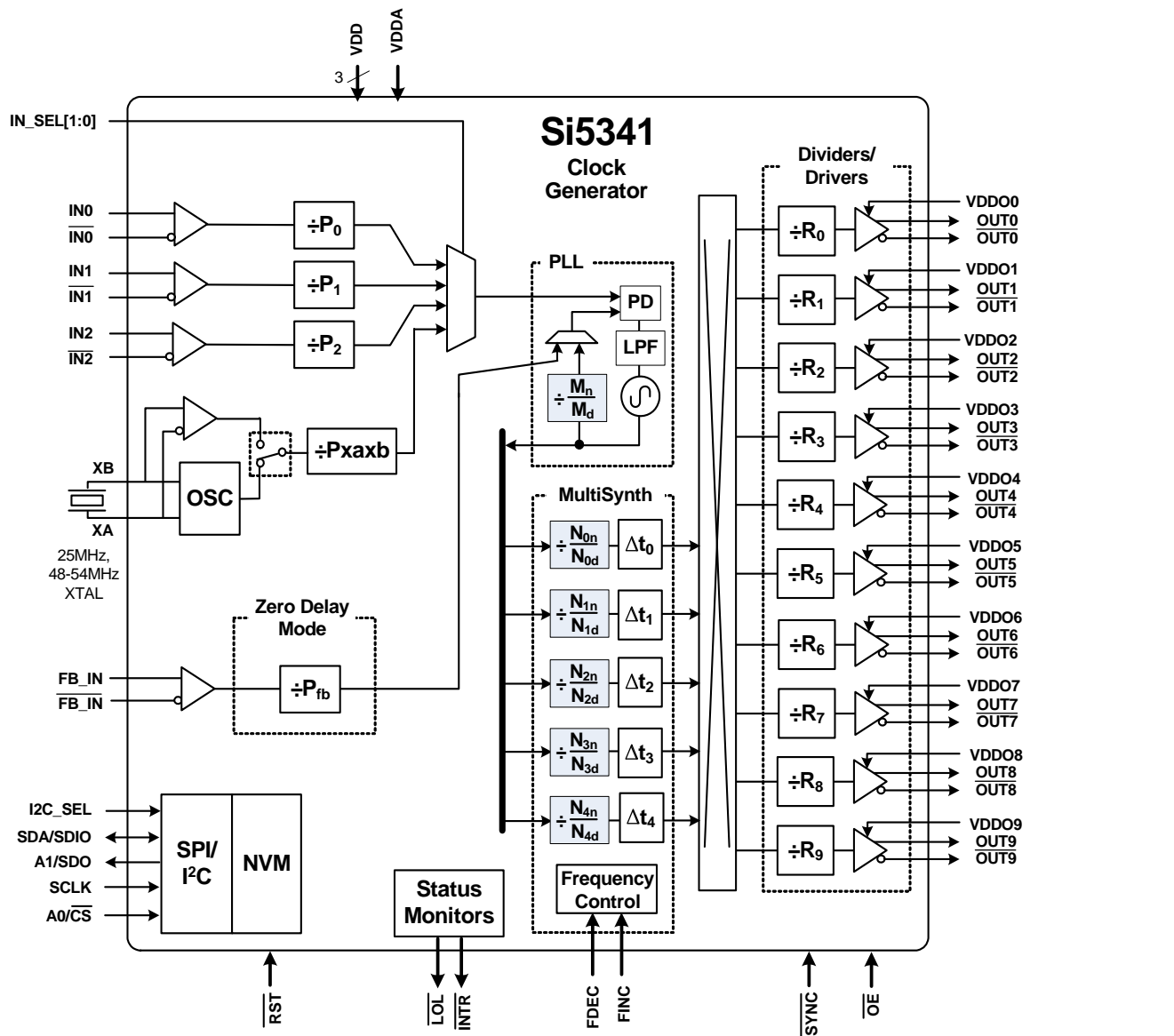


Figure 2. Si5341 Detailed Block Diagram

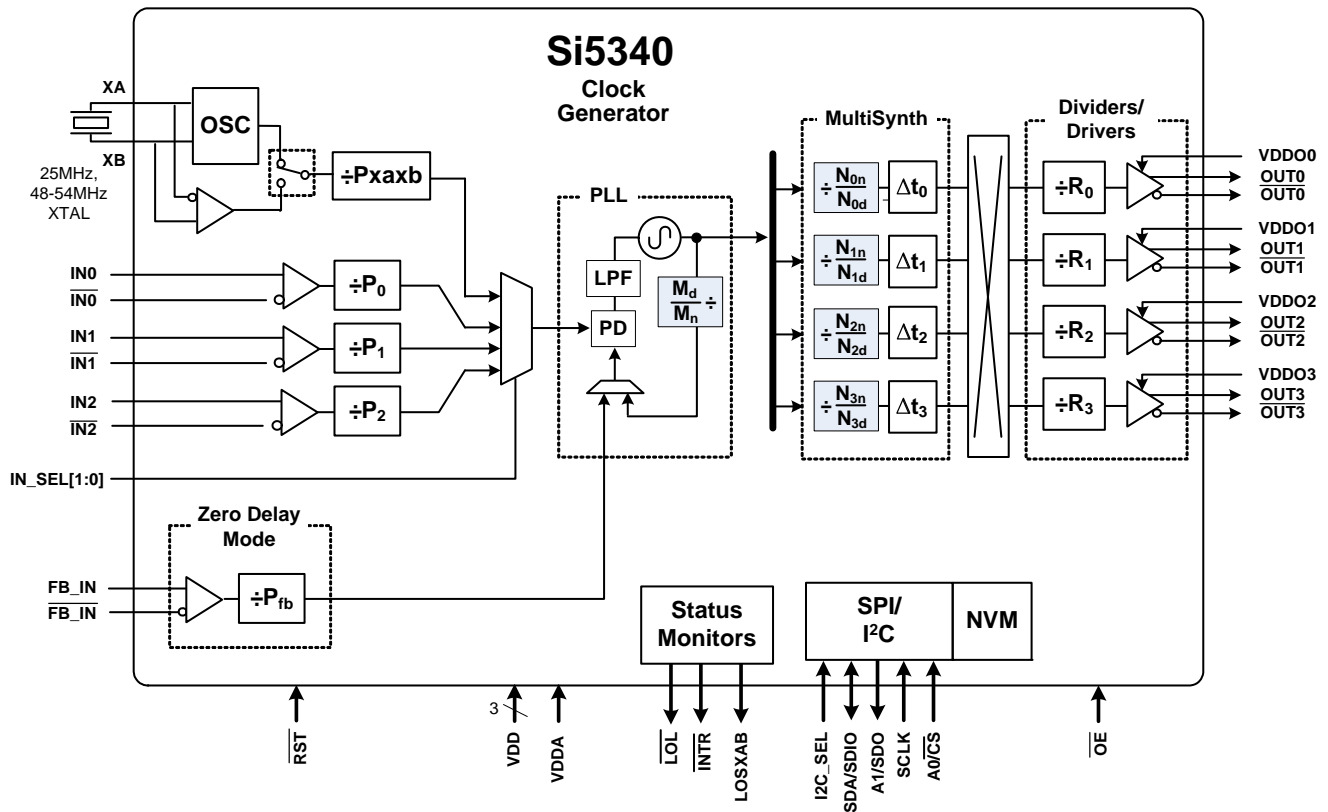


Figure 3. Si5340 Detailed Block Diagram

3. Power-Up and Initialization

Figure 4 shows the power-up and initialization sequenceFigure 4.

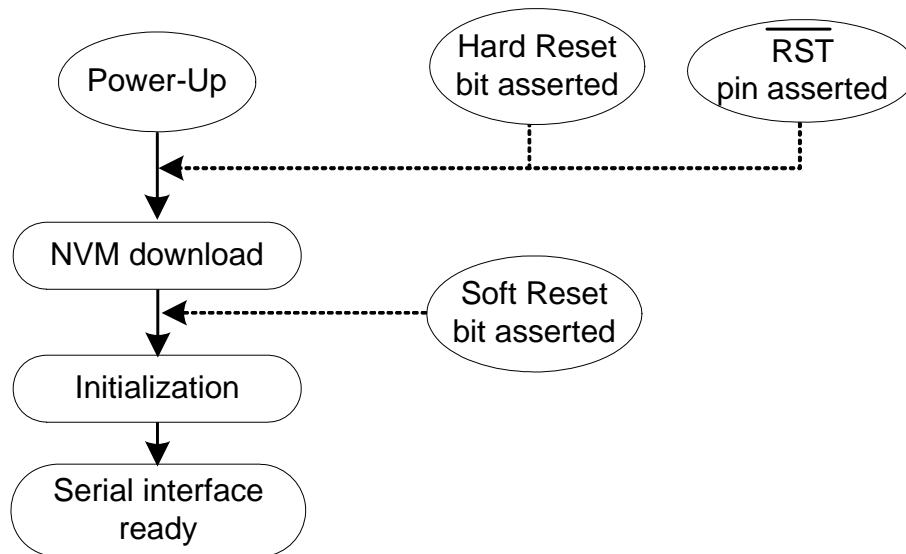


Figure 4. Power-Up and Initialization

3.1. Reset and Initialization

Once power is applied, the device begins an initialization period where it downloads default register values and configuration data from NVM and performs other initialization tasks. Communicating with the device through the serial interface is possible once this initialization period is complete. No clocks will be generated until the initialization is done. There are two types of resets available. A hard reset is functionally similar to a device power-up. All registers will be restored to the values stored in NVM, and all circuits will be restored to their initial state including the serial interface. A hard reset is initiated using the $\overline{\text{RST}}$ pin or by asserting the hard reset bit. A soft reset bypasses the NVM download. It is simply used to initiate register configuration changes.

Table 2. Reset Registers

Register Name	Hex Address [Bit Field]		Function
	Si5341	Si5340	
HARD_RST	001E[1]	001E[1]	Performs the same function as power cycling the device. All registers will be restored to their default values.
SOFT_RST	001C[0]	001C[0]	Performs a soft reset. Resets the device while it does not re-download the register configuration from NVM.

The Si541/40 is fully configurable using the serial interface (I²C or SPI). At power up the device downloads its default register values from internal non-volatile memory (NVM). Application specific default configurations can be written into NVM allowing the device to generate specific clock frequencies at power-up. Writing default values to NVM is in-circuit programmable with normal operating power supply voltages applied to its VDD (1.8V) and VDDA (3.3 V) pins.

3.2. NVM Programming

Because the NVM can only be written two times, it is important to configure the registers correctly before beginning the NVM programming process. Once a new configuration has been written to NVM, the old configuration is no longer accessible. Note: In-circuit programming is only supported over a temperature range of 0 to 80 °C.

The procedure for writing registers into NVM is as follows:

1. Ensure the part is configured correctly before proceeding.
2. Write 0xC7 to NVM_WRITE register.
3. Wait until DEVICE_READY = 0x0F
4. Set NVM_READ_BANK 0x00E4[0] ='1'.
5. Wait until DEVICE_READY = 0x0F.
6. Steps 3 and 4 can be replaced by simply powering down and then powering up the device.

Table 3. NVM Programming Registers

Register Name	Hex Address [Bit Field]		Function
	Si5340	Si5341	
NVM_WRITE	0x00E3[7:0]	0x00E3[7:0]	Initiates an NVM write when written with 0xC7.
NVM_READ_BANK	0x00E4[0]	0x00E4[0]	Download register values with content stored in NVM.
DEVICE_READY	0x00FE[7:0]	0x00FE[7:0]	Indicates that the device serial interface is ready to accept commands.

4. Reference Clock Inputs

The PLL in the Si5341/40 requires a single reference clock from either an external crystal at its XA/XB pins or an external clock at either XAXB or IN2,1,0.

4.1. Reference Clock Inputs on XA/XB

4.1.1. Crystal on XA/XB

An external standard crystal (XTAL) is connected to XA/XB when this input is configured as a crystal oscillator. A crystal frequency of 25 MHz can be used although crystals in the frequency range of 48 MHz to 54 MHz are recommended for the best jitter performance. Recommended crystals are listed below. The Si5341/40 includes a built-in XTAL load capacitance (C_L) of 8 pF, but crystals with CL specifications as high as 18 pF can also be used. When using crystals with CL specs higher than 8 pF it is not allowed to use external capacitors from XA/XB to ground to increase the crystal load capacitance. Rather the frequency offset due to C_L mismatch can be adjusted using the frequency adjustment feature which allows frequency adjustments of up to ± 1000 ppm. See section “9. Crystal and Device Circuit Layout Recommendations” for the PCB layout guidelines.

4.1.2. Clock Input on XA/XB

An external reference clock can also be input on the XA/XB pins. Selection between the external XTAL or REFCLK is controlled by register configuration. The internal crystal load capacitors (C_L) are disabled in external reference clock mode. Because the input buffer at XA/XB is a lower noise buffer than the buffers on IN2,1,0, a very clean input clock at XA/XB, such as a TCXO or XO, will, in some cases, produce lower output clock jitter than the same input at IN2,1,0. Both a single-ended or a differential REFCLK can be connected to the XA/XB pins as shown in Figure 5.

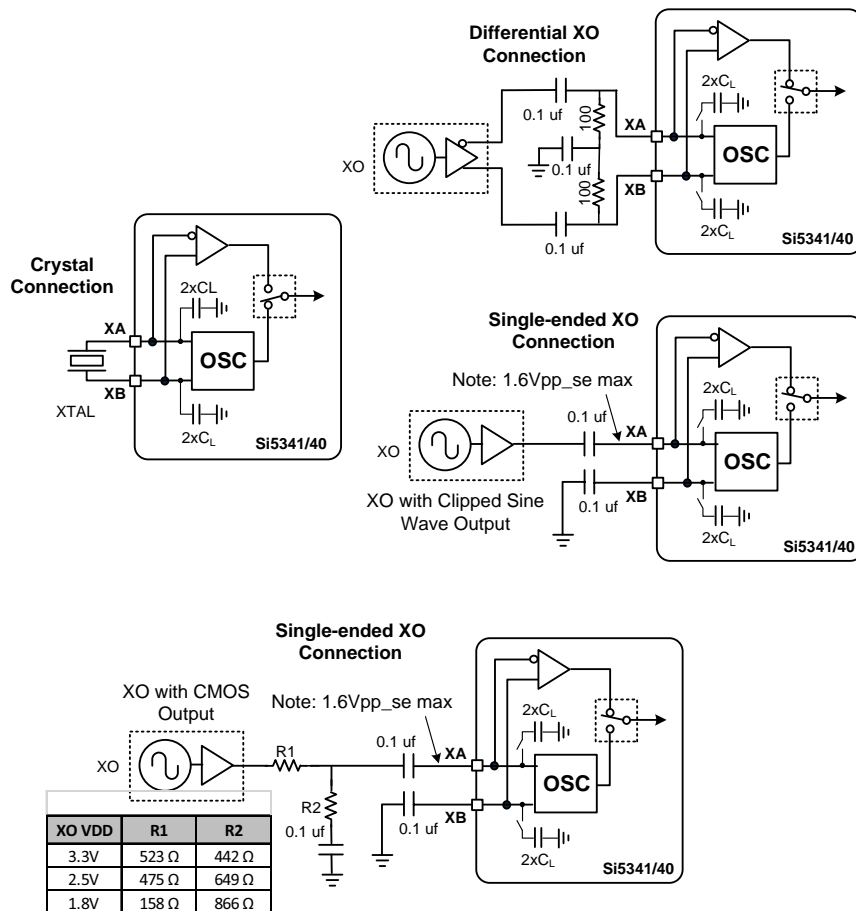


Figure 5. Crystal Resonator and External Reference Clock Connection Options

4.2. Reference Clock Inputs on IN2, IN1, IN0

A single ended or differential clock may be input to the IN2,1,0 inputs as shown below. All input signals must be ac-coupled. Unused inputs should have the inverted input tied to ground. The recommended input termination schemes are shown in Figure 6. Differential signals must be ac-coupled, while single-ended LVCMOS signals can be ac- or dc-coupled. Unused inputs can be disabled by register configuration.

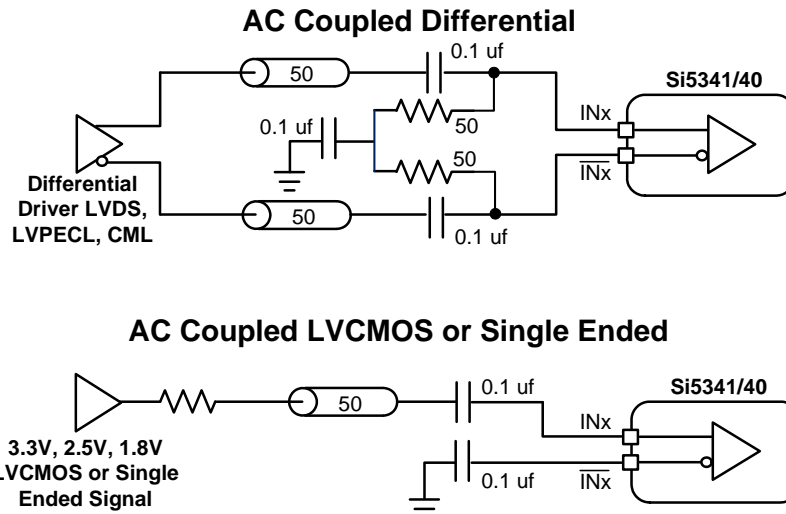


Figure 6. Terminations for Differential and Single-Ended Inputs

4.3. Reference Input Selection (IN0, IN1, IN2, XA/XB)

The active clock input is selected using the IN_SEL1,0 pins or by register control. A register bit determines input selection as pin or register selectable. The IN_SEL pins are selected by default. If the selected input does not have a clock, all output clocks will be shut off.

Table 4. Manual Input Selection Using IN_SEL[1:0] Pins

IN_SEL[1:0]		Selected Input
0	0	IN0
0	1	IN1
1	0	IN2
1	1	XA/XB

Table 5. Input Control Registers

Register Name	Hex Address [Bit Field]		Function
	Si5341	Si5340	
XAXB_FREQ_OFFSET	0202[7:0]–0205[7:0]		Adjusts for crystal load capacitance mismatch causing oscillation frequency errors up to ± 1000 ppm. Register values determined using ClockBuilder Pro.
XAXB_EXTCLK_EN	090E[0]		Selects between the XTAL or external REFCLK on the XA/XB pins
IN_SEL_REGCTRL	0021[0]		Determines pin or register clock input selection.
IN_SEL	0021[2:1]		Selects the input when in register input selection mode.
IN_EN	0949[3:0]		Allows enabling/disabling IN0, IN1, IN2 and FB_IN when not in use.

4.4. Fault Monitoring

The Si5341/40 provides fault indicators which monitor loss of signal (LOS) of the inputs (IN0, IN1, IN2, XA/XB, FB_IN) and loss of lock (LOL) for the PLL. This is shown in Figure 7.

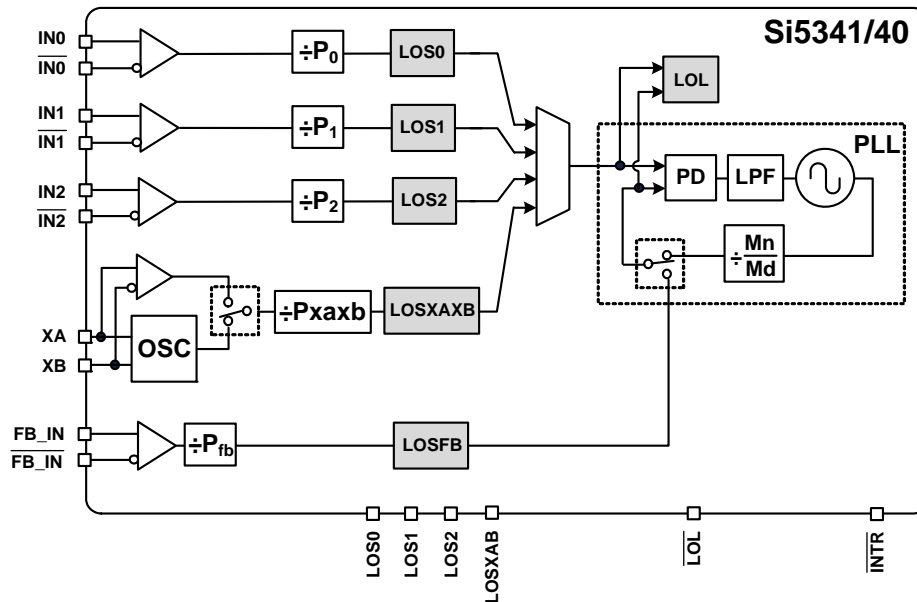


Figure 7. LOS and LOL Fault Monitors

4.4.1. Status Indicators

The state of the status monitors are accessible by reading registers through the serial interface or with dedicated pin (LOL). Each of the status indicator register bits has a corresponding sticky bit in a separate register location. Once a status bit is asserted its corresponding sticky bit will remain asserted until cleared. Writing a logic zero to a sticky register bit clears its state.

Table 6. Status Monitor Bits

Register Name	Hex Address [Bit Field]	Function
Status Register Bits		
SYSINCAL	0x000C[0]	Asserted when in calibration
LOSXAXB	0x000C[1]	Loss of Signal at the XA input
LOSREF	0x000C[2]	Loss of Signal for the input that has been selected
LOL	0x000C[3]	Loss of Lock for the PLL
SMBUS_TIMEOUT	0x000C[5]	The SMB bus has a timeout
LOSIN[2:0]	0x000D[2:0]	Loss of Signal for the LOS2,1,0 inputs
LOSFBI_IN	0x000D[3]	Loss of Signal for the FB_IN input

Table 6. Status Monitor Bits (Continued)

Register Name	Hex Address [Bit Field]	Function
Sticky Status Register Bits		
SYSINCAL_FLG	0x0011[0]	Sticky bit for SYSINCAL
LOSXAXB_FLG	0x0011[1]	Sticky bit for LOSXAXB
LOSREF_FLG	0x0011[2]	Sticky bit for LOSREF
LOL_FLG	0x0011[3]	Sticky bit for LOL
SMBUS_TIMEOUT_FLG	0x0011[5]	Sticky bit for SMBUS_TIMEOUT
LOSIN_FLG	0x0012[2:0]	Sticky bit for LOSIN
LOSFB_IN_FLG	0x0012[3]	Sticky bit for LOSFB_IN

4.4.2. Interrupt Pin ($\overline{\text{INTR}}$)

An interrupt pin ($\overline{\text{INTR}}$) indicates a change in state with any of the status registers. All status registers are maskable to prevent assertion of the interrupt pin. The state of the $\overline{\text{INTR}}$ pin is reset by writing zeros to all _FLG bits that are set or by writing a 1 to mask any _FLG bit that is set.

Table 7. Interrupt Mask Registers

Register Name	Hex Address [Bit Field]	Function
	Si5341 and Si5342	
SYSINCAL_INTR_MSK	0x00017[0]	1 = SYSINCAL_FLG is prevented from asserting the INTR pin
LOSXAXB_INTR_MSK	0x00017[1]	1 = LOSXAXB_FLG is prevented from asserting the INTR pin
LOSREF_INTR_MSK	0x00017[2]	1 = LOSREF_FLG is prevented from asserting the INTR pin
LOL_INTR_MSK	0x00017[3]	1 = LOL_FLG is prevented from asserting the INTR pin
SMBUS_TIMEOUT_INTR_MSK	0x00017[5]	1 = SMBUS_TIMEOUT_FLG is prevented from asserting the INTR pin
LOSIN_INTR_MSK[2:0]	0x0018[2:0]	1 = LOSIN_FLG is prevented from asserting the INTR pin
LOSFB_IN_INTR_MSK	0x0018[3]	1 = LOSFB_IN_FLG is prevented from asserting the INTR pin

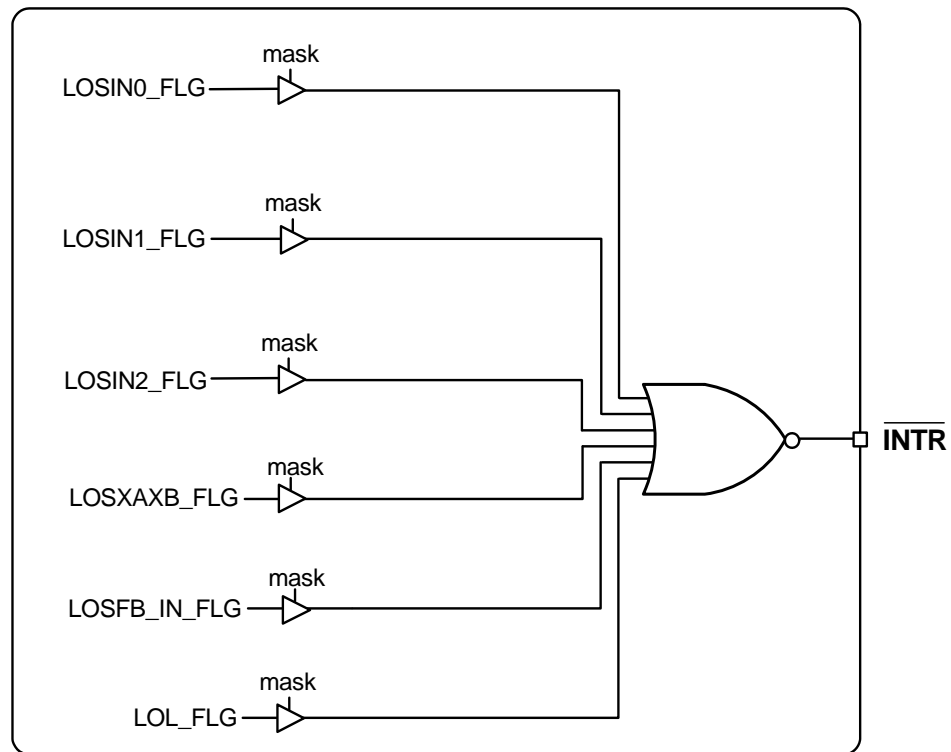


Figure 8. Interrupt Flags and Masks

5. Output Clocks

5.1. Outputs

The Si5341 supports ten differential output drivers which can be independently configured as differential or LVCMOS. The Si5340 supports four output drivers independently configurable as differential or LVCMOS.

5.2. Performance Guidelines for Outputs

Whenever a number of high frequency, fast rise time, large amplitude signals are all close to one another, the laws of physics dictate that there will be some amount of crosstalk. The jitter of the Si5341/40 is so low that crosstalk can become a significant portion of the final measured output jitter. Some of the source of the crosstalk will be the Si5341/40 and some will be introduced by the PCB. It is difficult (and possibly irrelevant) to allocate the jitter portions between these two sources because the jitter can only be measured when a Si5341/40 is mounted on a PCB.

For extra fine tuning and optimization in addition to following the usual PCB layout guidelines, crosstalk can be minimized by modifying the arrangements of different output clocks. For example, consider the following lineup of output clocks in Table 8.

Table 8. Example of Output Clock Frequency Sequencing Choice

Output	Not Recommended (Frequency MHz)	Recommended (Frequency MHz)
0	155.52	155.52
1	156.25	155.52
2	155.52	622.08
3	156.25	Not used
4	200	156.25
5	100	156.25
6	622.08	625
7	625	Not used
8	Not used	200
9	Not used	100

Using this example, a few guidelines are illustrated:

1. Avoid adjacent frequency values that are close. A 155.52 MHz clock should not be next to a 156.25 MHz clock. If the jitter integration bandwidth goes up to 20 MHz then keep adjacent frequencies at least 20 MHz apart.
2. Adjacent frequency values that are integer multiples of one another are okay and these outputs should be grouped accordingly. Noting that because $155.52 \times 4 = 622.08$ and $156.25 \times 4 = 625$, it is okay to place these frequency values close to one another.
3. Unused outputs can be used to separate clock outputs that might otherwise interfere with one another. In this case, see OUT3 and OUT7.

If some outputs have tight jitter requirements while others are relatively loose, rearrange the clock outputs so that the critical outputs are the least susceptible to crosstalk. These guidelines typically only need to be followed by those applications that wish to achieve the highest possible levels of jitter performance. Because CMOS outputs have large pk-pk swings and do not present a balanced load to the VDDO supplies, CMOS outputs generate much more crosstalk than differential outputs. For this reason, CMOS outputs should be avoided whenever possible. When CMOS is unavoidable, even greater care must be taken with respect to the above guidelines. It is highly recommended to read “AN862: Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems”.

5.3. Output Signal Format

The differential output swing and common mode voltage are both fully programmable covering a wide variety of signal formats including LVDS, LVPECL and HCSL. In addition to supporting differential signals, any of the outputs can be configured as LVCMOS (3.3, 2.5, or 1.8 V) drivers providing up to 20 single-ended outputs, or any combination of differential and single-ended outputs.

Table 9. Output Signal Format Control Registers

Register Name	Hex Address [Bit Field]		Function
	Si5341	Si5340	
OUT0_FORMAT	0109[2:0]	0113[2:0]	Selects the output signal format as differential or LVCMOS.
OUT1_FORMAT	010E[2:0]	0118[2:0]	
OUT2_FORMAT	0113[2:0]	0127[2:0]	
OUT3_FORMAT	0118[2:0]	012C[2:0]	
OUT4_FORMAT	011D[2:0]	—	
OUT5_FORMAT	0122[2:0]	—	
OUT6_FORMAT	0127[2:0]	—	
OUT7_FORMAT	012C[2:0]	—	
OUT8_FORMAT	0131[2:0]	—	
OUT9_FORMAT	013B[2:0]	—	

5.3.1. Differential Output Terminations

The differential output drivers support both ac-coupled and dc-coupled terminations as shown in Figure 9.

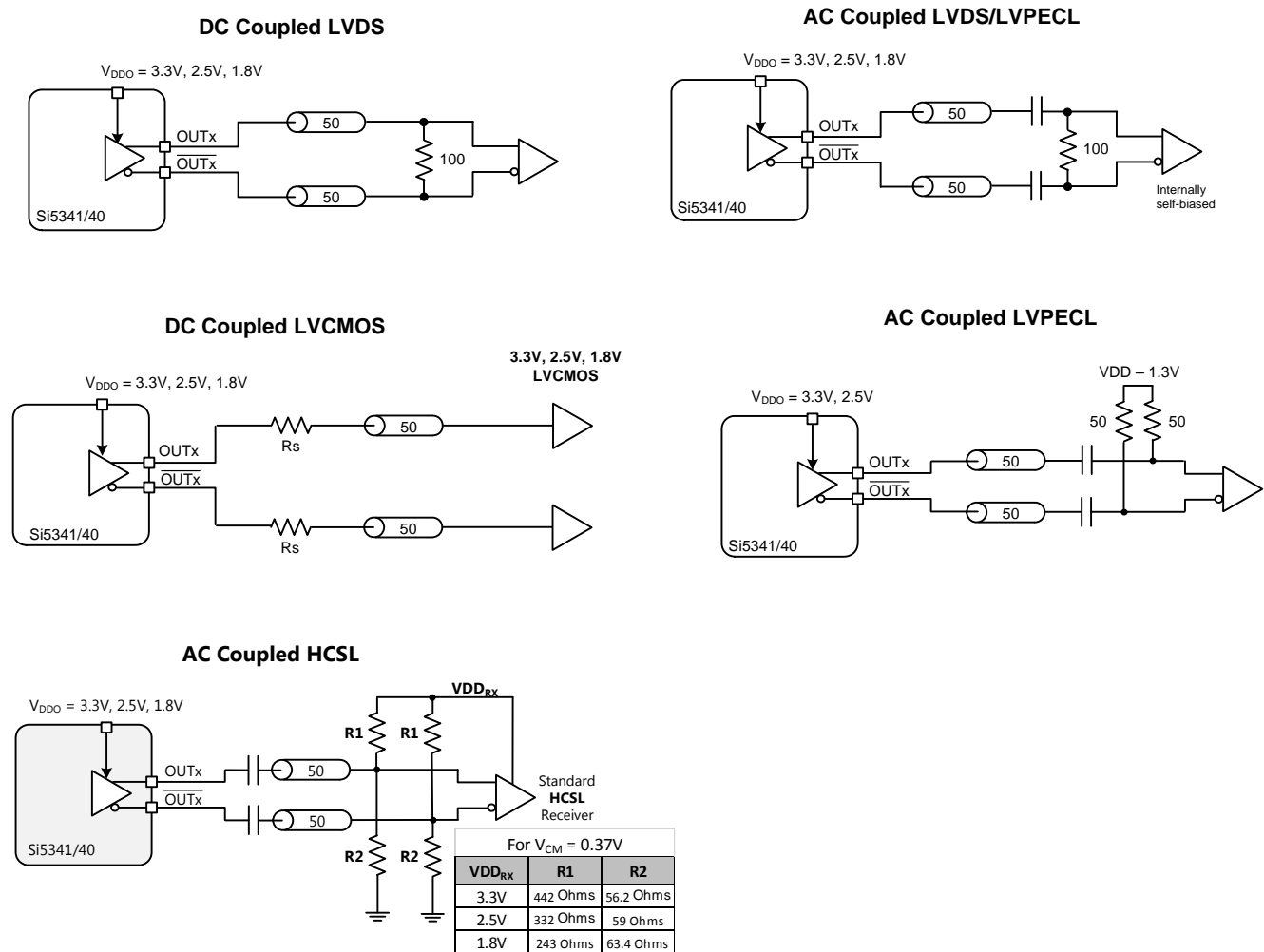


Figure 9. Supported Differential Output Terminations

5.3.2. Differential Output Swing Modes

There are two selectable differential output swing modes: Normal and High. Each output can support a unique mode.

- **Differential Normal Swing Mode:** This is the usual selection for differential outputs and should be used, unless there is a specific reason to do otherwise. When an output driver is configured in normal swing mode, its output swing is selectable as one of 7 settings ranging from 200 mVpp_{se} to 800 mVpp_{se} in increments of 100 mV. Table 11 shows typical voltage swing values. The output impedance in the Normal Swing Mode is 100 Ω differential.
- **Differential High Swing Mode:** When an output driver is configured in high swing mode, its output swing is configurable as one of 7 settings ranging from 400 mVpp_{se} to 1600 mVpp_{se} in increments of 200 mV. The output driver is in high impedance mode and supports standard 50 Ω PCB traces. Any of the terminations shown in Figure 9 are supported. The use of High Swing mode will result in larger pk-pk output swings that draw less power. The trade off will be slower rise and fall times.

Table 10. Differential Output Voltage Swing Control Registers

Register Name	Hex Address [Bit Field]		Function
	Si5341	Si5340	
OUT0_AMPL	010A[6:4]	0114[6:4]	Sets the voltage swing for the differential output drivers when in normal mode and high swing modes (Table 11).
OUT1_AMPL	010F[6:4]	0119[6:4]	
OUT2_AMPL	0114[6:4]	0128[6:4]	
OUT3_AMPL	0119[6:4]	012D[6:4]	
OUT4_AMPL	011E[6:4]	—	
OUT5_AMPL	0123[6:4]	—	
OUT6_AMPL	0128[6:4]	—	
OUT7_AMPL	012D[6:4]	—	
OUT8_AMPL	0132[6:4]	—	
OUT9_AMPL	013C[6:4]	—	

5.3.3. Programmable Common Mode Voltage For Differential Outputs

The common mode voltage (V_{CM}) for the differential Normal and High Swing modes is programmable in 100 mV increments from 0.7 V to 2.3 V depending on the voltage available at the output's VDDO pin. Setting the common mode voltage is useful when dc coupling the output drivers. The common-mode voltage swing values are shown in Table 11.

Table 11. Differential Output Common Mode Voltage Control Registers

Register Name	Hex Address [Bit Field]		Function
	Si5341	Si5340	
OUT0_CM	010A[3:0]	0114[3:0]	Sets the common mode voltage for the differential output driver.
OUT1_CM	010F[3:0]	0119[3:0]	
OUT2_CM	0114[3:0]	0128[3:0]	
OUT3_CM	0119[3:0]	012D[3:0]	
OUT4_CM	011E[3:0]	—	
OUT5_CM	0123[3:0]	—	
OUT6_CM	0128[3:0]	—	
OUT7_CM	012D[3:0]	—	
OUT8_CM	0132[3:0]	—	
OUT9_CM	013C[3:0]	—	

Table 12. Recommended Differential Signal Format Settings

Signal Format	Swing Mode	OUTx_FORMAT	ppSE (typ)	OUTx_AMPL	Common Mode Voltage	OUTx_CM	VDDO (3.3, 2.5, 1.8 V)
3.3 V LVPECL	Normal	001	800 mV	110	2.0 V	1011	3.3 V
	High	010		011			
2.5 V LVPECL	Normal	001		110	1.2 V	1011	2.5 V
	High	010		011			
3.3 V LVDS	Normal	001	~450 mV	011	1.2 V	0011	3.3 V
	High	010		001			
2.5 V LVDS	Normal	001		011		1011	2.5 V
	High	010		001			
1.8 V LVDS*	Normal	001		011	0.9 V	1110	1.8 V
1.8 V LVDS*	High	001		011	0.9 V	1110	1.8 V

***Note:** The 1.8 V LVDS setting will not meet the standard 1.2 V common-mode voltage. AC coupling to an LVDS receiver is recommended. The normal mode produces a faster rise/fall time than the high swing mode. For this reason the normal mode should be used unless there is a specific reason to use the high swing mode.

5.3.4. LVCMOS Output Terminations

LVCMOS outputs are dc coupled as shown in Figure 10.

DC Coupled LVCMOS

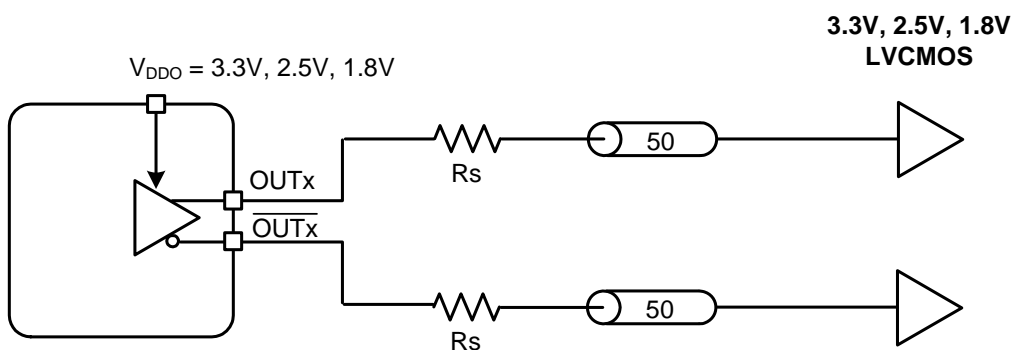


Figure 10. LVCMOS Output Terminations

5.3.5. LVCMOS Output Impedance And Drive Strength Selection

Each LVCMOS driver has a configurable output impedance to accommodate different trace impedances and drive strengths. A source termination resistor (R_s) is highly recommended to help match the selected output impedance to the trace impedance (i.e. $R_s \approx \text{Trace Impedance} - Z_s$). For the best signal integrity, Silicon Labs strongly recommends using the setting that produces the lowest source impedance and then choosing the proper external source resistor to produce the best signal shape at the end of the signal trace.

Table 13. Output Impedance and Drive Strength Selections

VDDO	OUTx_CMOS_DRV Register Value Setting	Source Impedance (Z_s)
3.3 V	0x01	38 Ω
	0x02	30 Ω
	0x03*	22 Ω
2.5 V	0x01	43 Ω
	0x02	35
	0x03*	24 Ω
1.8 V	0x02	46 Ω
	0x03*	31
Note: This setting is strongly recommended.		

Table 14. LVCMOS Drive Strength Control Registers

Register Name	Hex Address [Bit Field]		Function
	Si5341	Si5340	
OUT0_CMOS_DRV	0109[7:6]	0113[7:6]	LVCMOS output impedance. See Table 13.
OUT1_CMOS_DRV	010E[7:6]	0118[7:6]	
OUT2_CMOS_DRV	0113[7:6]	0127[7:6]	
OUT3_CMOS_DRV	0118[7:6]	012C[7:6]	
OUT4_CMOS_DRV	011D[7:6]	—	
OUT5_CMOS_DRV	0122[7:6]	—	
OUT6_CMOS_DRV	0127[7:6]	—	
OUT7_CMOS_DRV	012C[7:6]	—	
OUT8_CMOS_DRV	0131[7:6]	—	
OUT9_CMOS_DRV	013B[7:6]	—	

5.3.6. LVCMOS Output Signal Swing

The signal swing (V_{OL}/V_{OH}) of the LVCMOS output drivers is set by the voltage on the VDDO pins. Each output driver has its own VDDO pin allowing a unique output voltage swing for each of the LVCMOS drivers.

5.3.7. LVCMOS Output Polarity

When a driver is configured as an LVCMOS output it generates a clock signal on both pins ($OUTx$ and \overline{OUTx}). By default the clock on the \overline{OUTx} pin is generated with the opposite polarity (complementary) with the clock on the $OUTx$ pin. The polarity of these clocks is configurable enabling in-phase clock generation and/or inverted polarity with respect to other output drivers.

Table 15. LVCMOS Output Polarity Control Registers

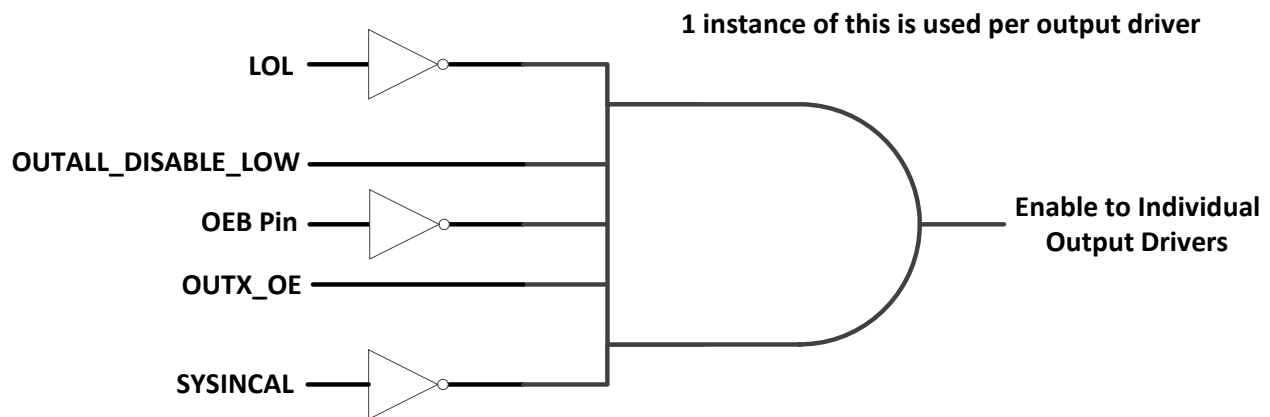
Register Name	Hex Address [Bit Field]		Function																				
	Si5341	Si5340																					
OUT0_INV	010B[7:6]	0115[7:6]	Controls output polarity of the $OUTx$ and \overline{OUTx} pins when in LVCMOS mode. Selections are:																				
OUT1_INV	0110[7:6]	011A[7:6]																					
OUT2_INV	0115[7:6]	0129[7:6]																					
OUT3_INV	011A[7:6]	012E[7:6]																					
OUT4_INV	011F[7:6]	—																					
OUT5_INV	0124[7:6]	—																					
OUT6_INV	0129[7:6]	—																					
OUT7_INV	012E[7:6]	—																					
OUT8_INV	0133[7:6]	—																					
OUT9_INV	0138[7:6]	—																					
			<table> <tr> <th>$OUTx_INV$</th><th>$OUTx$</th><th>\overline{OUTx}</th><th>Comment</th></tr> <tr> <td>0 0</td><td>CLK</td><td>\overline{CLK}</td><td>Complementary (default)</td></tr> <tr> <td>0 1</td><td>CLK</td><td>CLK</td><td>Both in phase</td></tr> <tr> <td>1 0</td><td>\overline{CLK}</td><td>CLK</td><td>Inverted</td></tr> <tr> <td>1 1</td><td>\overline{CLK}</td><td>\overline{CLK}</td><td>Both out of phase</td></tr> </table>	$OUTx_INV$	$OUTx$	\overline{OUTx}	Comment	0 0	CLK	\overline{CLK}	Complementary (default)	0 1	CLK	CLK	Both in phase	1 0	\overline{CLK}	CLK	Inverted	1 1	\overline{CLK}	\overline{CLK}	Both out of phase
$OUTx_INV$	$OUTx$	\overline{OUTx}	Comment																				
0 0	CLK	\overline{CLK}	Complementary (default)																				
0 1	CLK	CLK	Both in phase																				
1 0	\overline{CLK}	CLK	Inverted																				
1 1	\overline{CLK}	\overline{CLK}	Both out of phase																				

5.3.8. Output Enable/Disable

Clock outputs are disabled by four signals within Si5341/40 and the OEB pin:

- OUTALL_DISABLE_LOW
- SYSINCAL
- $OUTx_OE$
- LOL
- OEB pin

Figure 11 shows the logic of how these disable/enables occur.



$OUTx_OE$ are the individual Output Driver enables as shown in the table below

Figure 11. Output Enable

Table 16. Output Enable/Disable Control Registers

Register Name	Hex Address [Bit Field]		Function
	Si5341	Si5340	
OUTALL_DISABLE_LOW	0102[0]		0 = Disables all outputs. 1 = All outputs are not disabled by this signal but may be disabled by other signals or the OEB pin. See Figure 11 above.
OUT0_OE	0108[1]	0112[1]	0 = Specific output disabled. 1 = Specific output is not disabled. The OEB pin or other signals within the device may be causing an output disable. See Figure 11 above.
OUT1_OE	010D[1]	0117[1]	
OUT2_OE	0112[1]	0126[1]	
OUT3_OE	0117[1]	012B[1]	
OUT4_OE	011C[1]	—	
OUT5_OE	0121[1]	—	
OUT6_OE	0126[1]	—	
OUT7_OE	012B[1]	—	
OUT8_OE	0130[1]	—	
OUT9_OE	013A[1]	—	

5.3.9. Output Driver State When Disabled

The disabled state of an output driver is configurable as: disable low, disable high, or disable mid. When set for disable mid, the output common mode voltage will stay nearly the same when disabled as when enabled.

Table 17. Output Driver Disable State Control Registers

Register Name	Hex Address [Bit Field]		Function
	Si5341	Si5340	
OUT0_DIS_STATE	0109[5:4]	0113[5:4]	Determines the state of an output driver when disabled. Selectable as: <ul style="list-style-type: none"> ■ Disable logic low. ■ Disable logic high ■ Disable mid
OUT1_DIS_STATE	010E[5:4]	0118[5:4]	
OUT2_DIS_STATE	0113[5:4]	0127[5:4]	
OUT3_DIS_STATE	0118[5:4]	012C[5:4]	
OUT4_DIS_STATE	011D[5:4]	—	
OUT5_DIS_STATE	0122[5:4]	—	
OUT6_DIS_STATE	0127[5:4]	—	
OUT7_DIS_STATE	012C[5:4]	—	
OUT8_DIS_STATE	0131[5:4]	—	
OUT9_DIS_STATE	013B[5:4]	—	

5.3.10. Synchronous/Asynchronous Output Disable Feature

Outputs can be configured to disable synchronously or asynchronously. In synchronous disable mode the output will wait until a clock period has completed before the driver is disabled. This prevents unwanted runt pulses from occurring when disabling an output. In asynchronous disable mode the output clock will disable immediately without waiting for the period to complete.

Table 18. Synchronous Disable Control Registers

Register Name	Hex Address [Bit Field]		Function
	Si5341	Si5340	
OUT0_SYNC_EN	0109[3]	0113[3]	Synchronous output disable. When this feature is enabled, the output clock will always finish a complete period before disabling. When this feature is disabled, the output clock will disable immediately without waiting for the period to complete.
OUT1_SYNC_EN	010E[3]	0118[3]	
OUT2_SYNC_EN	0113[3]	0127[3]	
OUT3_SYNC_EN	0118[3]	012C[3]	
OUT4_SYNC_EN	011D[3]	—	This feature is disabled by default.
OUT5_SYNC_EN	0122[3]	—	
OUT6_SYNC_EN	0127[3]	—	
OUT7_SYNC_EN	012C[3]	—	
OUT8_SYNC_EN	0131[3]	—	
OUT9_SYNC_EN	013B[3]	—	

5.3.11. Output Skew Control ($\Delta t_0 - \Delta t_4$)

The Si5341/40 uses independent MultiSynth dividers ($N_0 - N_4$) to generate up to five unique frequencies to its ten outputs through a crosspoint switch. By default all clocks are phase aligned. A delay path ($\Delta t_0 - \Delta t_4$) associated with each of these dividers is available for applications that need a specific output skew configuration. This is useful for PCB trace length mismatch compensation. The resolution of the delay is approximately 0.28ps per step. Delays are register configurable but the delay adjustment is only applied at power up or after a Soft Reset. An example of generating two frequencies with unique configurable path delays is shown in Figure 12.

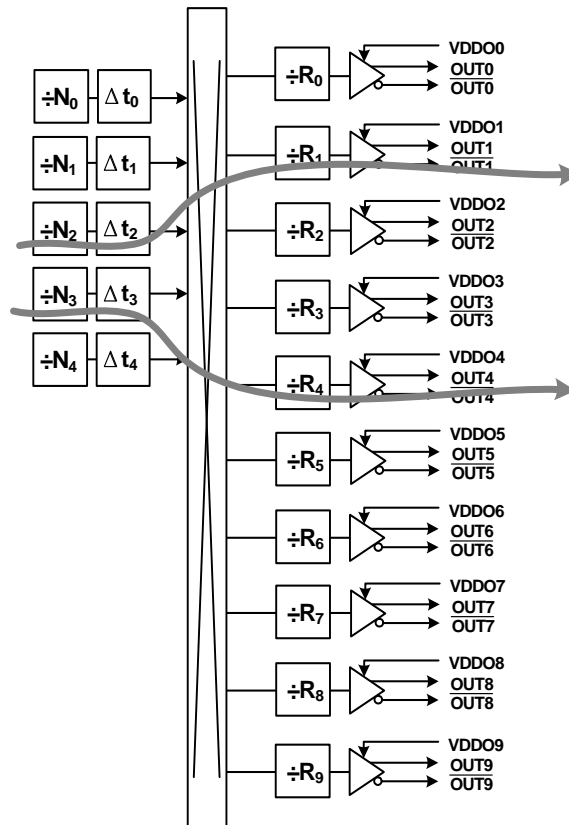


Figure 12. Example of Independently Configurable Path Delays

All delay values are restored to their default values after power-up, hard reset, or a reset using the $\overline{\text{RST}}$ pin. Delay default values can be written to NVM allowing a custom phase offset configuration at power-up or after power-on reset, or after a hardware reset using the $\overline{\text{RST}}$ pin.

Table 19. Delay Registers

Register Name	Hex Address [Bit Field]		Function
	Si5341	Si5340	
N0_DELAY	0359[7:0] - 035A[7:0]		Configures path delay values for each N divider. Each 16 bit number is 2s complement. The output delay is Nx_DELAY/(256 x Fvco) where Fvco is the frequency of the VCO in Hz and the delay is in seconds. Register values determined using ClockBuilder Pro. Note that the Si5340 only uses N0_DELAY-N3_DELAY.
N1_DELAY	035B[7:0] - 035C[7:0]		
N2_DELAY	035D[7:0] - 035E[7:0]		
N3_DELAY	035F[7:0] - 0360[7:0]		
N4_DELAY	0361[7:0] - 0362[7:0]		

5.3.12. Zero Delay Mode

A zero delay mode is available for applications that require fixed and consistent minimum delay between the selected input and outputs. The zero delay mode is configured by opening the internal feedback loop through software configuration and closing the loop externally as shown in Figure 13. This helps to cancel out the internal delay introduced by the dividers, the crosspoint, the input, and the output drivers. Any one of the outputs can be fed back to the FB_IN pins, although using the output driver that achieves the shortest trace length will help to minimize the input-to-output delay. The OUT9 (OUT3 for the Si5340) and FB_IN pins are highly recommended for the external feedback connection. Clock Builder Pro will calculate all the dividers to implement the Zero Delay Mode. The FB_IN input pins must be terminated and ac coupled when zero delay mode is used. A differential external feedback path connection is necessary for best performance.

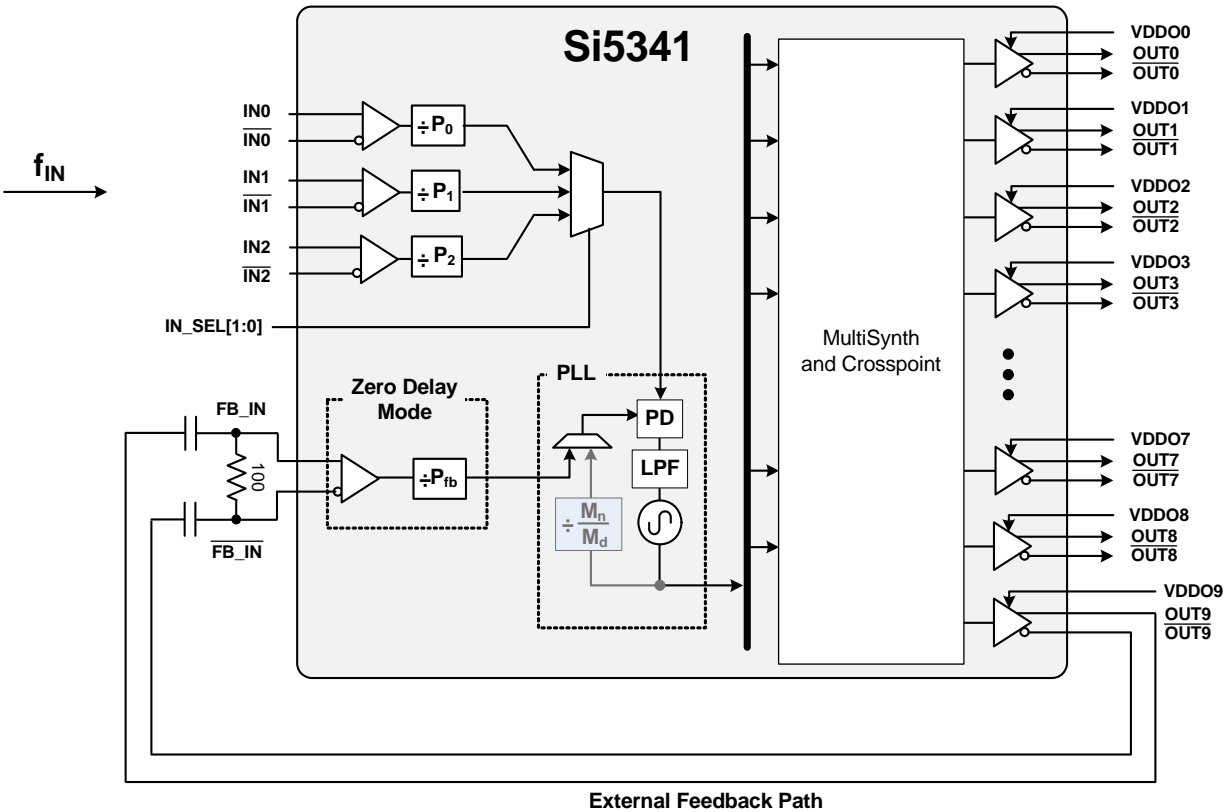


Figure 13. Si5341 Zero Delay Mode Set-up

Table 20. Zero Delay Mode Control Register

Register Name	Hex Address [Bit Field]		Function
	Si5341	Si5340	
ZDM_EN	091C[2:0]		Selects internal (normal) or external feedback (zero delay mode). Default is internal feedback.

5.3.13. Sync Pin (Synchronizing R Dividers)

All the output R dividers are reset to a known state during the power-up initialization period. This ensures consistent and repeatable phase alignment across all output drivers. Resetting the device using the $\overline{\text{RST}}$ pin or asserting the hard reset bit will have the same result. The SYNC pin provides another method of re-aligning the R dividers without resetting the device. This pin is positive edge triggered. Asserting the sync register bit provides the same function.

Table 21. R Divider Synchronization Control Registers

Register Name	Hex Address [Bit Field]		Function
	Si5341	Si5340	
SYNC	001E[2]		Logically equivalent to asserting the $\overline{\text{SYNC}}$ pin. Resets all R dividers to the same state.

5.4. Output Crosspoint

The output crosspoint allows any of the N dividers to connect to any of the output drivers.

Table 22. Output Crosspoint Control Registers

Register Name	Hex Address [Bit Field]		Function
	Si5341	Si5340	
OUT0_MUX_SEL	010B[2:0]	0115[2:0]	Connects the output drivers to one of the N dividers. Selections are: N0, N1, N2, N3, N4 for each output divider.
OUT1_MUX_SEL	0110[2:0]	011A[2:0]	
OUT2_MUX_SEL	0115[2:0]	0129[2:0]	
OUT3_MUX_SEL	011A[2:0]	012E[2:0]	
OUT4_MUX_SEL	011F[2:0]	—	
OUT5_MUX_SEL	0124[2:0]	—	
OUT6_MUX_SEL	0129[2:0]	—	
OUT7_MUX_SEL	012E[2:0]	—	
OUT8_MUX_SEL	0133[2:0]	—	
OUT9_MUX_SEL	013D[2:0]	—	

5.5. Dynamic and Glitchless Output Frequency Changes

5.5.1. Frequency Increment/Decrement

Each of the MultiSynth™ fractional dividers (Nx) can be independently stepped up or down in predefined steps by use of the FINC/FDEC pins or the FINC/FDEC register bits. The MultiSynth™ that is affected by the FINC/FDEC bits or pins is determined by the N_FSTEP_MSK bits. The frequency changes that happen are glitchless and instantaneous. The size of a single frequency increment or decrement is determined by the 44 bit Frequency Step Word (Nx_FSTEPW) for each MultiSynth divider. A frequency increment causes the Nx_FSTEPW to be subtracted from the Nx_NUM word. A frequency decrement causes the Nx_FSTEPW to be added to the Nx_NUM word. When the Nx_FSTEPW = 1 (smallest possible) and the Nx_NUM value is fully left shifted (as done by ClockBuilder), a single frequency step will be no larger than $1e9 \times (Nx_NUM / (Nx_NUM + 1) - 1)$ ppb. This equates to a ~.05 ppb with a 710 MHz output and ~.0007 ppb with a 10 MHz output. The frequency increment and decrement feature is useful in applications requiring a variable clock frequency (e.g., CPU speed control, FIFO overflow management, DCO or NCO, etc.) or in applications where frequency margining (e.g. fout ±5% or more) is necessary for design verification and manufacturing test. Defining FINC/FDEC step size can be easily determined using ClockBuilder Pro.

5.5.2. Direct Frequency Changes

The output frequency can be changed by directly writing to the Nx_NUM 44 bit word and then asserting either the Nx_UPDATE bit or the global update bit N_UPDATE. The Nx_UPDATE bit only updates the particular Nx_NUM word. The N_UPDATE bit will simultaneously update all Nx_NUM words. Writing the N_UPDATE bit will not interfere with Nx dividers that have not changed since the last time N_UPDATE or Nx_UPDATE was asserted. Output frequency changes due to changes of the Nx_NUM terms are guaranteed to be glitchless. The only restriction on writing to Nx_NUM is that Nx_NUM/Nx_DEN must always be ≥ 10 and $\leq 2^{12} - 1$, which means that the frequency changes can be quite large or quite small. The smallest frequency step possible is no larger than ~.05 ppb with a 710 MHz output and no larger than ~.0007 ppb with a 10 MHz output.

6. Serial Interface

Configuration and operation of the Si5341/40 is controlled by reading and writing registers using the I²C or SPI interface. The I2C_SEL pin selects I²C or SPI operation. The Si5341/40 supports communication with a 3.3 V or 1.8 V host by setting the IO_VDD_SEL (0x0943[0]) configuration bit. The SPI mode supports 4-wire or 3-wire by setting the SPI_3WIRE configuration bit.

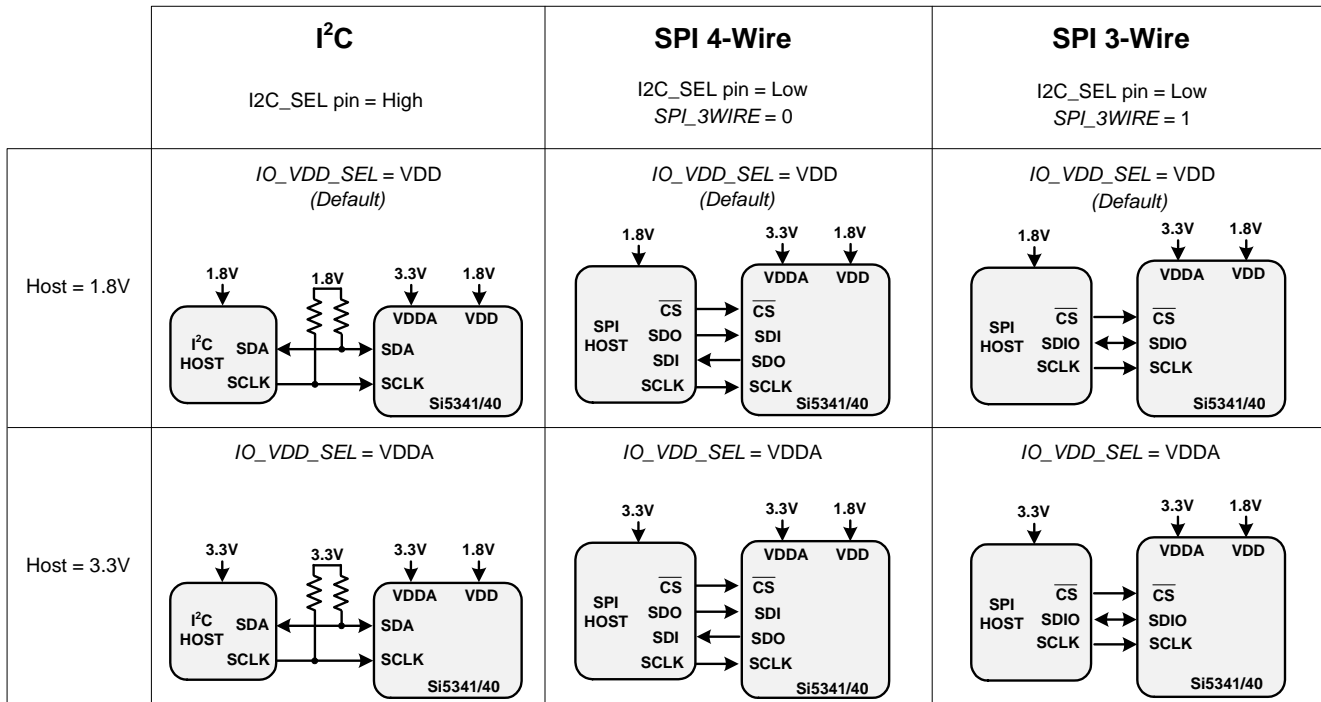


Figure 14. I²C/SPI Device Connectivity Configurations

Table 23 lists register settings of interest for the I²C/SPI.

Table 23. I²C/SPI Register Settings

Register Name	Hex Address [Bit Field]		Function
	Si5341	Si5340	
IO_VDD_SEL	0x0943[0]	0x0943[0]	The IO_VDD_SEL configuration bit selects the option of operating the serial interface voltage thresholds from the VDD or the VDDA pin. By default the IO_VDD_SEL bit is set to the VDD option. The serial interface pins are always 3.3 V tolerant even when the device's VDD pin is supplied from a 1.8 V source. When the I ² C or SPI host is operating at 3.3 V and the Si5341/40 at VDD = 1.8 V, the host must write the IO_VDD_SEL configuration bit to the VDDA option. This will ensure that both the host and the serial interface are operating at the optimum voltage thresholds.
SPI_3WIRE	0x002B[3]	0x002B[3]	The SPI_3WIRE configuration bit selects the option of 4-wire or 3-wire SPI communication. By default the SPI_3WIRE configuration bit is set to the 4-wire option. In this mode the Si5341/40 will accept write commands from a 4-wire or 3-wire SPI host allowing configuration of device registers. For full bidirectional communication in 3-wire mode, the host must write the SPI_3WIRE configuration bit to "1".

6.1. I²C Interface

When in I²C mode, the serial interface operates in slave mode with 7-bit addressing and can operate in Standard-Mode (100 kbps) or Fast-Mode (400 kbps) and supports burst data transfer with auto address increments. The I²C bus consists of a bidirectional serial data line (SDA) and a serial clock input (SCL) as shown in Figure 25. Both the SDA and SCL pins must be connected to a supply via an external pull-up (1k to 4.7k ohm) as recommended by the I²C specification as shown in Figure 15. Two address select bits (A0, A1) are provided allowing up to four Si5341/40 devices to communicate on the same bus. This also allows four choices in the I²C address for systems that may have other overlapping addresses for other I²C devices.

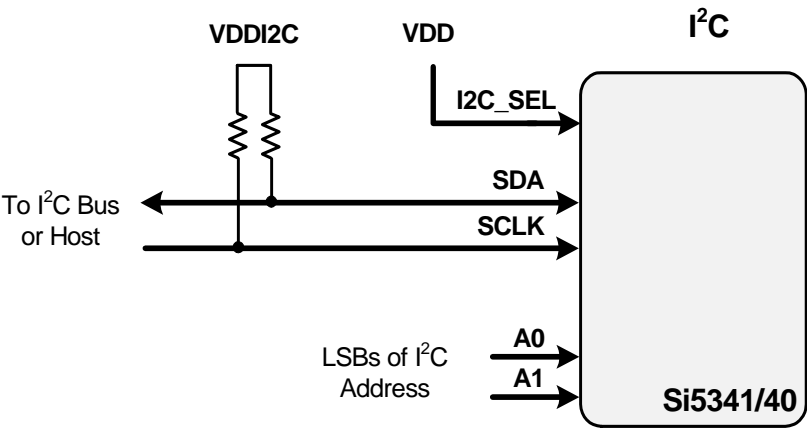


Figure 15. I²C Configuration

The 7-bit slave device address of the Si5341/40 consists of a 5-bit fixed address plus two pins that are selectable for the last two bits, as shown in Figure 16.

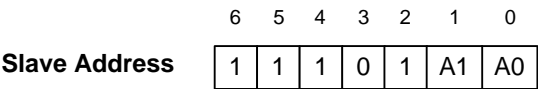


Figure 16. 7-bit I²C Slave Address Bit-Configuration

Data is transferred MSB first in 8-bit words as specified by the I²C specification. A write command consists of a 7-bit device (slave) address + a write bit, an 8-bit register address, and 8 bits of data as shown in Figure 19. A write burst operation is also shown where subsequent data words are written using to an auto-incremented address.

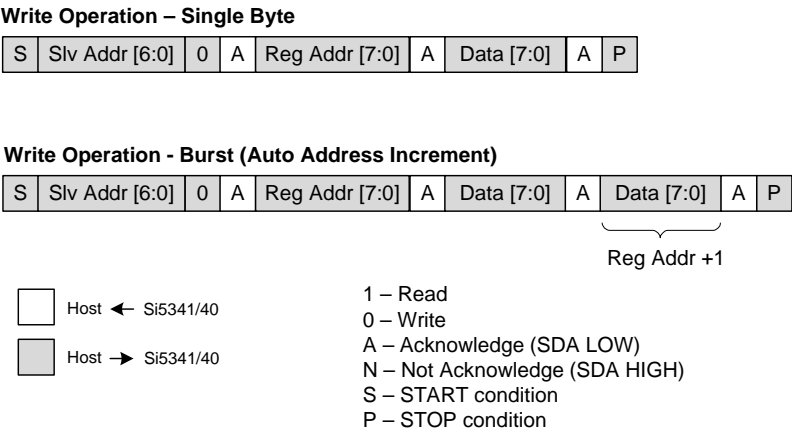
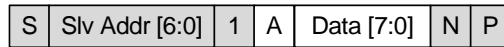


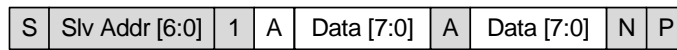
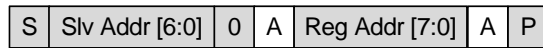
Figure 17. I²C Write Operation

A read operation is performed in two stages. A data write is used to set the register address, then a data read is performed to retrieve the data from the set address. A read burst operation is also supported. This is shown in Figure 18.

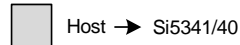
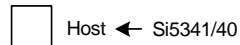
Read Operation – Single Byte



Read Operation - Burst (Auto Address Increment)



Reg Addr +1



1 – Read
 0 – Write
 A – Acknowledge (SDA LOW)
 N – Not Acknowledge (SDA HIGH)
 S – START condition
 P – STOP condition

Figure 18. I²C Read Operation

6.2. SPI Interface

When in SPI mode, the serial interface operates in 4-wire or 3-wire depending on the state of the SPI_3WIRE configuration bit. The 4-wire interface consists of a clock input (SCLK), a chip select input (CS), serial data input (SDI), and serial data output (SDO). The 3-wire interface combines the SDI and SDO signals into a single bidirectional data pin (SDIO). Both 4-wire and 3-wire interface connections are shown in Figure 19.

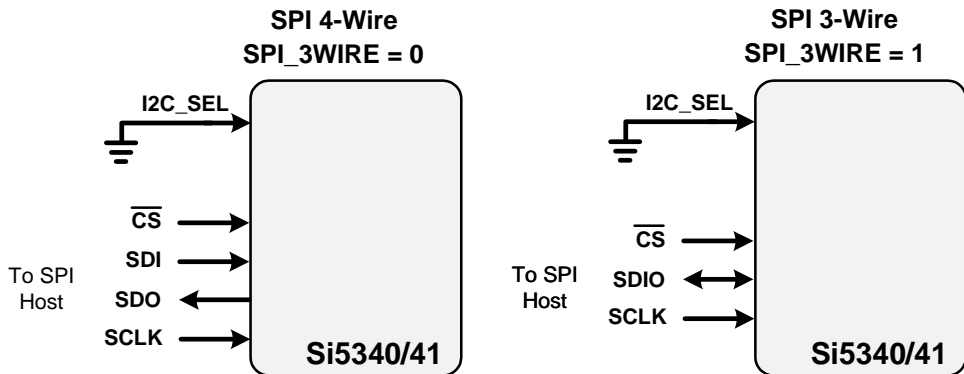


Figure 19. SPI Interface Connections

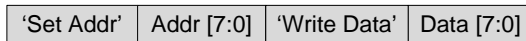
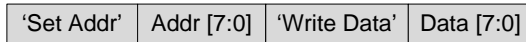
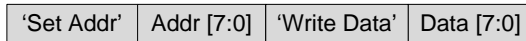
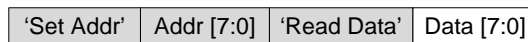
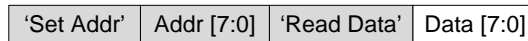
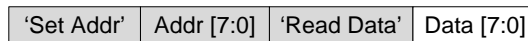
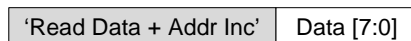
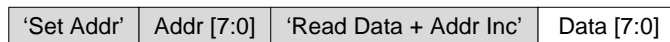
Table 24. SPI Command Format

Instruction	1 st Byte ¹	2 nd Byte	3 rd Byte	Nth Byte ^{2,3}
Set Address	000x xxxx	8-bit Address	—	—
Write Data	010x xxxx	8-bit Data	—	—
Read Data	100x xxxx	8-bit Data	—	—
Write Data + Address Increment	011x xxxx	8-bit Data	—	—
Read Data + Address Increment	101x xxxx	8-bit Data	—	—
Burst Write Data	1110 0000	8-bit Address	8-bit Data	8-bit Data

Notes:

1. X = don't care (1 or 0)
2. The Burst Write Command is terminated by de-asserting /CS (/CS = high)
3. There is no limit to the number of data bytes that may follow the Burst Write Command, but the address will wrap around to 0 in the byte after address 255 is written.

Writing or reading data consist of sending a “Set Address” command followed by a “Write Data” or “Read Data” command. The ‘Write Data + Address Increment’ or “Read Data + Address Increment” commands are available for cases where multiple byte operations in sequential address locations is necessary. The “Burst Write Data” instruction provides a compact command format for writing data since it uses a single instruction to define starting address and subsequent data bytes. Figure 20 shows an example of writing three bytes of data using the write commands. This demonstrates that the “Write Burst Data” command is the most efficient method for writing data to sequential address locations. Figure 21 provides a similar comparison for reading data with the read commands. Note that there is no burst read, only read increment.

'Set Address' and 'Write Data'**'Set Address' and 'Write Data + Address Increment'****'Burst Write Data'****Figure 20. Example Writing Three Data Bytes using the Write Commands****'Set Address' and 'Read Data'****'Set Address' and 'Read Data + Address Increment'****Figure 21. Example of Reading Three Data Bytes Using the Read Commands**

The timing diagrams for the SPI commands are shown in Figures 22, 23, 24, and 25.

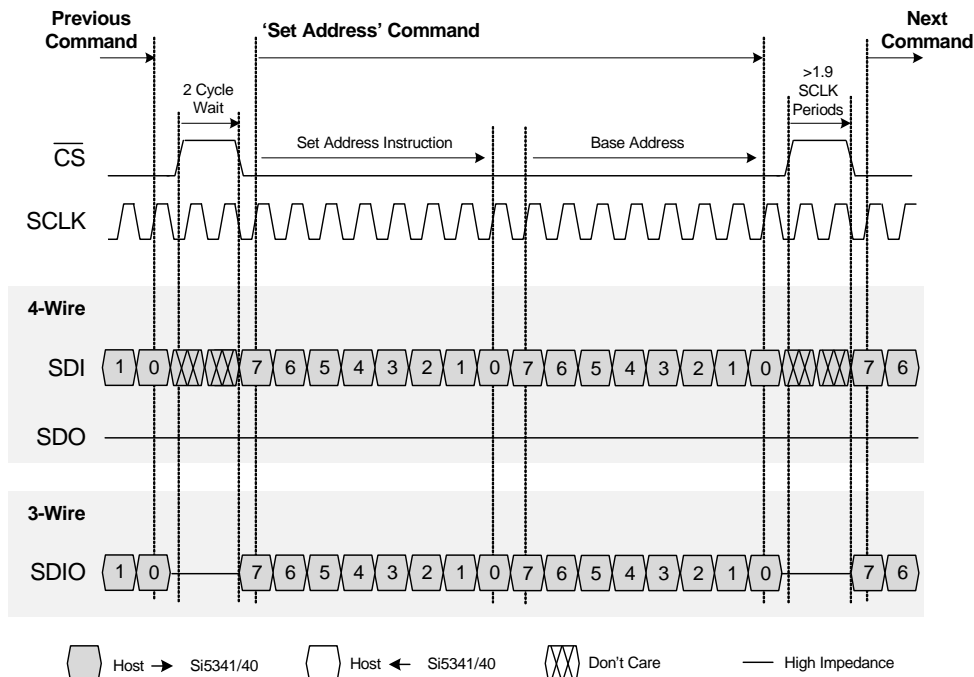


Figure 22. SPI “Set Address” Command Timing

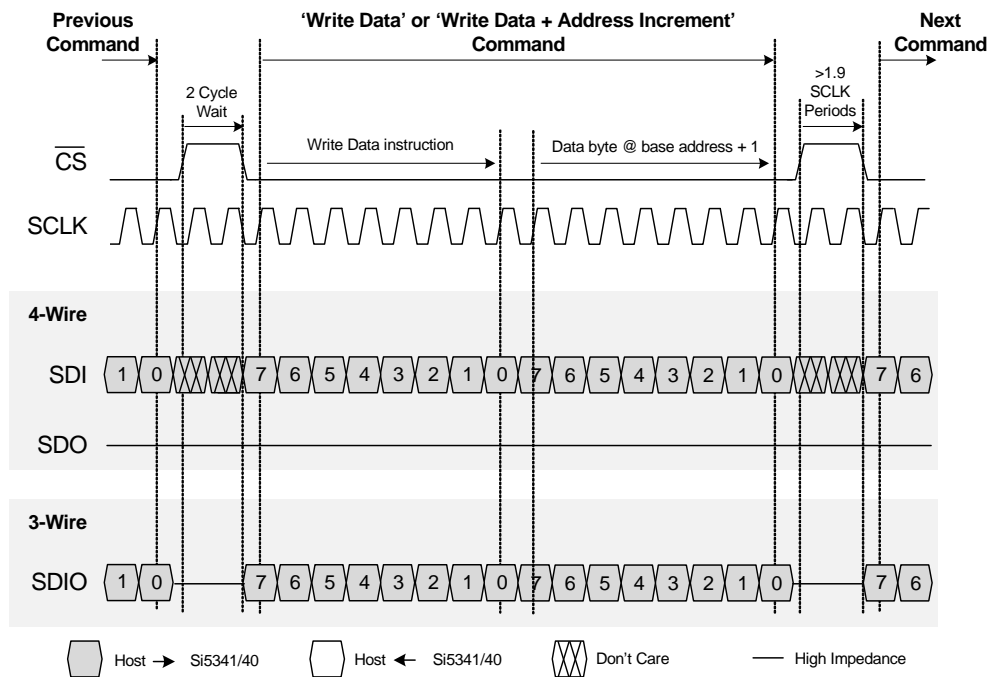


Figure 23. SPI “Write Data” and “Write Data+ Address Increment” Instruction Timing

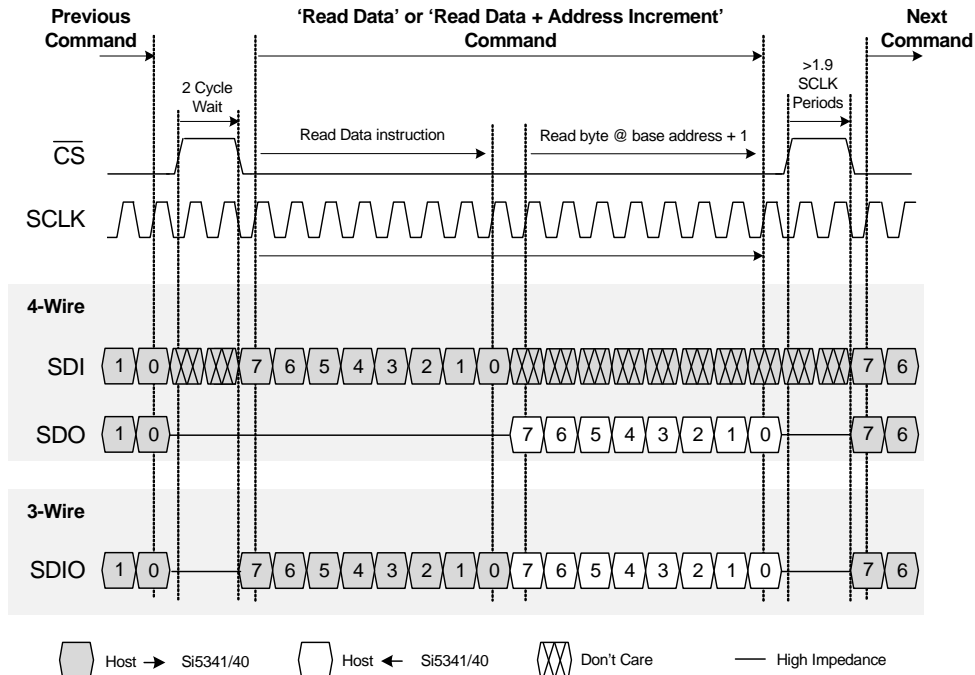


Figure 24. SPI "Read Data" and "Read Data + Address Increment" Instruction Timing

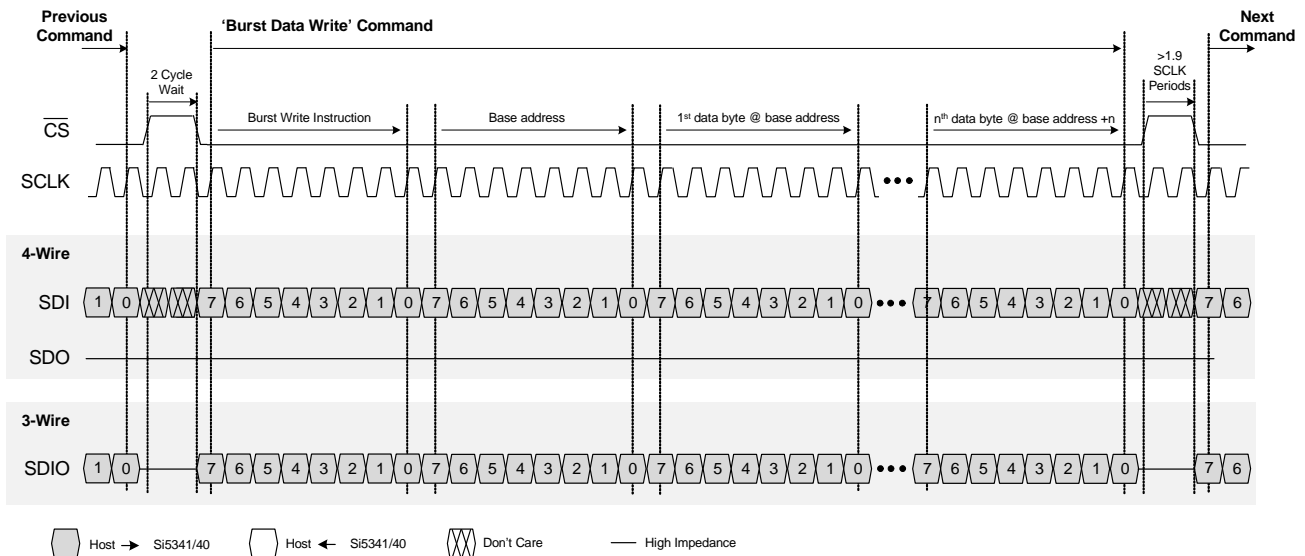


Figure 25. SPI "Burst Data Write" Instruction Timing

7. Field Programming Requirements

A field programming board will be available for customers or third parties who prefer to program their Si5341/40 devices outside the target system. Contact your [Silicon Labs sales representative](#) for availability.

8. Recommended Crystals and External Oscillators

8.1. Recommended Crystal

There are 2 classes of crystals that are recommended, those that are tested over temperature for activity dips and those that are not. There is a cost premium for testing over temperature. An activity dip is defined as when the crystal oscillation frequency changes by more than 2 ppm/C for any temperature between - 40C and 75C. It is estimated that ~0.1% of crystals that are not tested over temperature for activity dips will have an activity dip at some temperature. Customers may contact the vendors to ask that any non-premium crystal be tested over temperature for activity dips. Likewise any crystal that is tested over temperature can likely be purchased for a lower cost if you prefer to not pay the higher cost for the temperature testing.

Table 25 lists the presently recommended crystals. Other vendors can also supply crystals that meet the specs in Figures 25 and 26.

Table 25. Recommended Crystal

Supplier	Part Number	Frequency	Initial ppm + ppm from - 40 °C to +85 °C	Co Max	ESR Max	CL pF	Tested over Temp. for activity dips?	μW Max	Case Size mm x mm
TXC	7M48072002	48 MHz	25	2	22	8	yes	200	3.2 x 2.5
TXC	7M48072001	48 MHz	50	2	22	8	yes	200	3.2 x 2.5
TXC	7M54072002	54 MHz	25	2	22	8	yes	200	3.2x2.5
TXC	7M54072001	54 MHz	40	2	22	8	yes	200	3.2x2.5
Kyocera	CX3225SB4800 0D0FPJC1	48 MHz	25	2	23	8	No	200	3.2x2.5
Kyocera	CX3225SB4800 0D0WPSC1	48 MHz	50	2	23	8	No	200	3.2x2.5
Kyocera	CX3225SB5400 0D0WPSC1	54 MHz	50	2	23	8	No	200	3.2x2.5

In general, a crystal meeting the requirements of Figure 26 or Figure 27 and having a max power rating of at least 200 μW is guaranteed to oscillate.

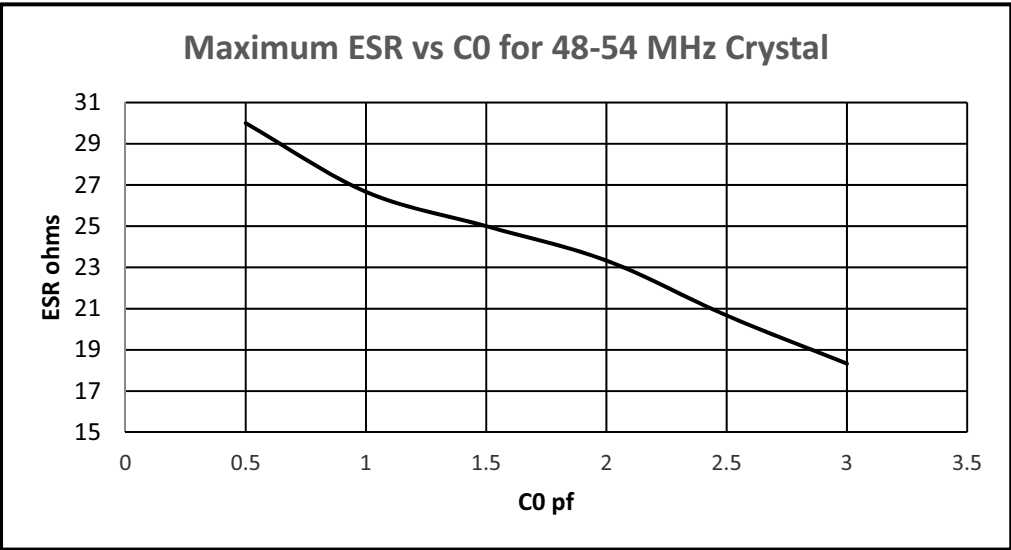


Figure 26. R1 (ESR) vs. C0 for 48 to 54 MHz Crystals

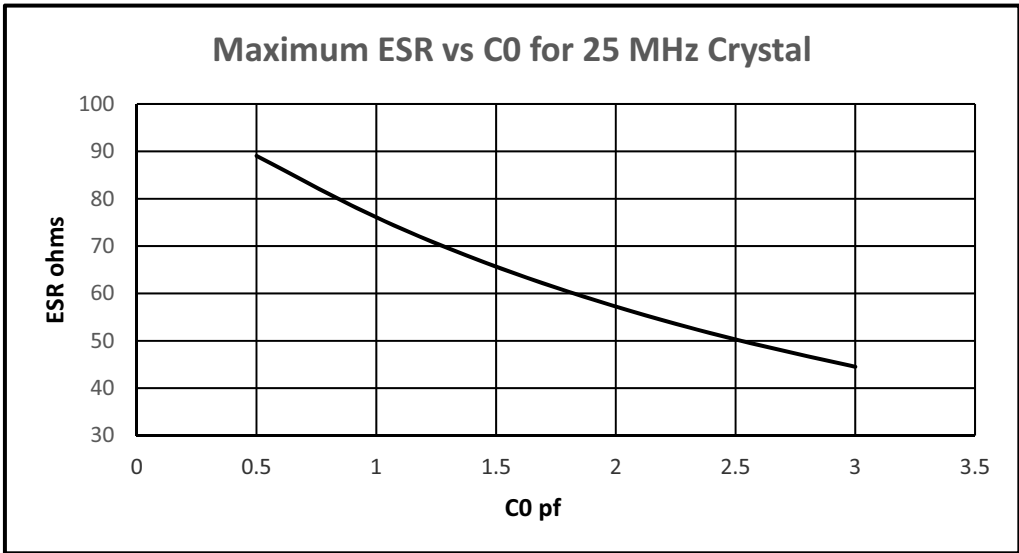


Figure 27. R1 (ESR) vs. C0 for 25 MHz Crystals

8.2. Recommended Oscillator Suppliers

Table 26 lists the recommended TCXO/OCXO suppliers.

Table 26. Recommended Oscillator Suppliers

Supplier	Part Number	TCXO OCXO	Model	Frequency	Case Size
Kyocera	KT7050A40000KAW33TAG	TCXO		40 MHz	5 x 7 x 1.7
Rakon	509768	TCXO	RTX7050A	40 MHz	5x7x1.87
Rakon	E6213LF	TCXO	RPT7050A	40 MHz	5x7x2
Kyocera	0010.000000M13133AT	OCXO	OCXO-1409A	10 MHz	14.8 x 9.1 x 6.2
Rakon	RFP050	OCXO		5–50 MHz	14.6 x 9.7 x 6.2
Rakon	M5686LF	OCXO		25 MHz	9 x 7 x 4

9. Crystal and Device Circuit Layout Recommendations

The main layout issues that should be carefully considered include the following:

1. Number and size of the ground vias for the Epad
2. Output clock trace routing
3. Input clock trace routing
4. Control and Status signals to input or output clock trace coupling
5. XTAL signal coupling
6. XTAL layout

If the application uses a crystal for the XAXB inputs a shield should be placed underneath the crystal connected to the X1 and X2 pins (4 and 7) to provide the best possible performance. The shield should not be connected to the ground plane and the planes underneath should have as little under the shield as possible. It may be difficult to do this for all the layers, but it is important to do this for the layers that are closest to the shield.

9.1. 64-Pin QFN Si5341 Layout Recommendations

This section details the recommended guidelines for the crystal layout of the 64-pin Si5341 device using an example 8-layer PCB. The following are the descriptions of each of the eight layers.

- Layer 1: device layer, with low speed CMOS control/status signals, ground flooded
- Layer 2: crystal shield
- Layer 3: ground plane
- Layer 4: power distribution, ground flooded
- Layer 5: power routing layer
- Layer 6: ground input clocks, ground flooded
- Layer 7: output clocks layer
- Layer 8: ground layer

Figure 28 is the top layer layout of the Si5341 device mounted on the top PCB layer. This particular layout was designed to implement either a crystal or an external oscillator as the XAXB reference. The crystal/ oscillator area is outlined with the white box around it. In this case, the top layer is flooded with ground. Note that this layout has a resistor in series with each pin of the crystal. In typical applications, these resistors should be removed.

9.1.1. Si5341 Applications without a Crystal as the Reference Clock

If the application does not use a crystal, then the X1 and X2 pins should be left as “no connect” and should not be tied to ground. In addition, there is no need for a crystal shield or the voids underneath the shield. If there is a differential external clock input on XAXB there should be a termination circuit near the XA and XB pins. This termination circuit should be two 50 Ω resistors and one 0.1 μ F cap connected in the same manner as on the other clock inputs (IN0, IN1 and IN2). See Figure 5. The clock input on XAXB must be ac-coupled. Care should be taken to keep all clock inputs well isolated from each other as well as any other dynamic signal.

9.1.2. Si5341 Crystal Layout Guidelines

The following are five recommended crystal layout guidelines:

1. Place the crystal as close as possible to the XA/XB pins.
2. Do not connect the crystal's GND pins to PCB gnd.
3. Connect the crystal's GND pins to the DUT's X1 and X2 pins via a local crystal shield placed around and under the crystal. See Figure 34 at the bottom left for an illustration of how to create a crystal shield by placing vias connecting the top layer traces to the shield layer underneath. Note that a zoom view of the crystal shield layer on the next layer down is shown in Figure 29.
4. Keep transitioning signal traces as distant as practical from the crystal/oscillator area especially if they are clocks or frequently toggling digital signals.
5. In general do not route GND, power planes/traces, or locate components on the other side, below the crystal shield. If necessary a ground layer may be placed under the crystal shield plane as long as it is at least 0.05" below the crystal shield layer.

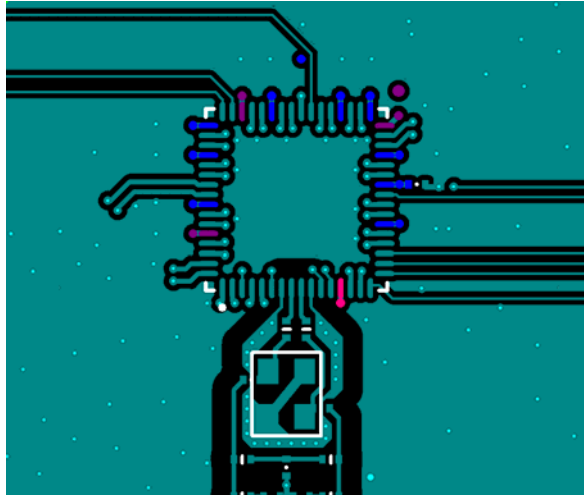


Figure 28. 64-pin Si5341 Crystal Layout Recommendations Top Layer (Layer 1)

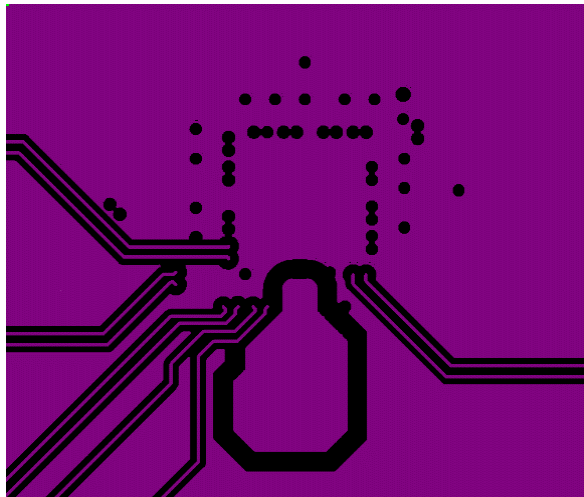


Figure 29. Zoom View Crystal Shield Layer, Below the Top Layer (Layer 2)

Figure 29 shows the layer that implements the shield underneath the crystal. The shield extends underneath the entire crystal and the X1 and X2 pins. This layer also has the clock input pins. The clock input pins go to layer 2 using vias to avoid crosstalk. As soon as the clock inputs are on layer 2 they have a ground shield above below and on the sides for protection.

Figure 30 is the ground plane and shows a void underneath the crystal shield. Figure 31 is a power plane and shows the clock output power supply traces. The void underneath the crystal shield is continued.

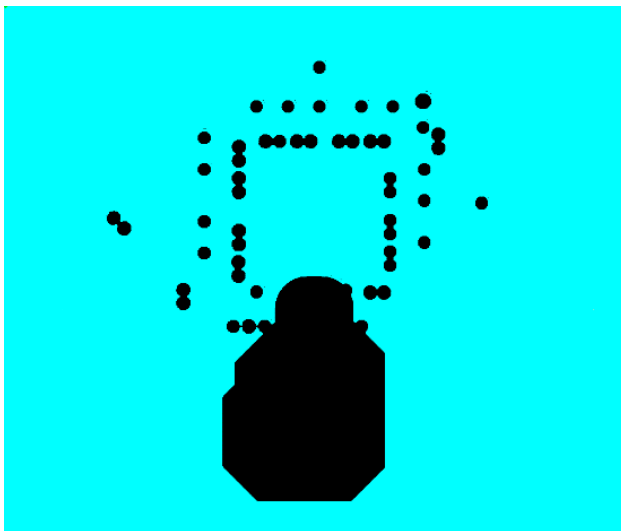


Figure 30. Crystal Ground Plane (Layer 3)

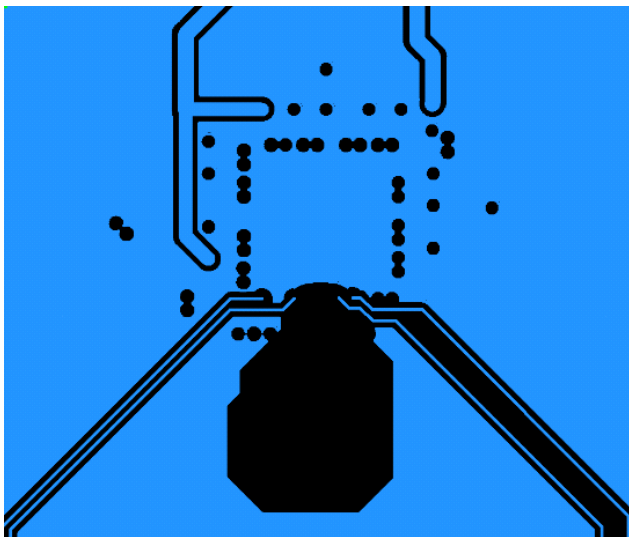


Figure 31. Power Plane (Layer 4)

Figure 32 shows layer 5, which is the power plane with the power routed to the clock output power pins.

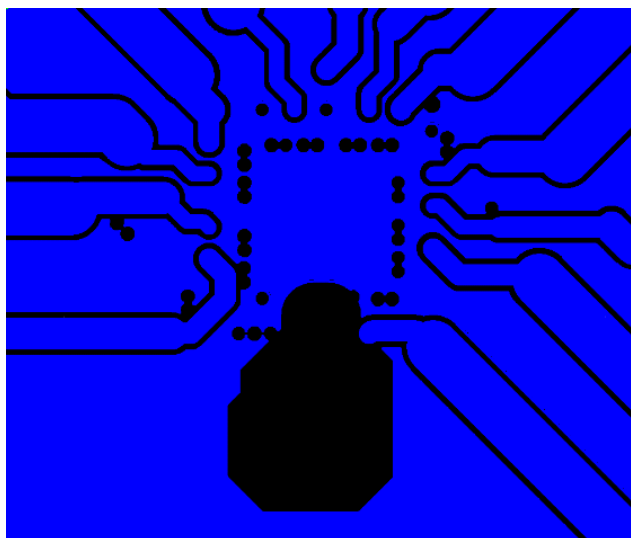


Figure 32. Layer 5 Power Routing on Power Plane (Layer 5)

Figure 33 is another ground plane similar to layer 3.

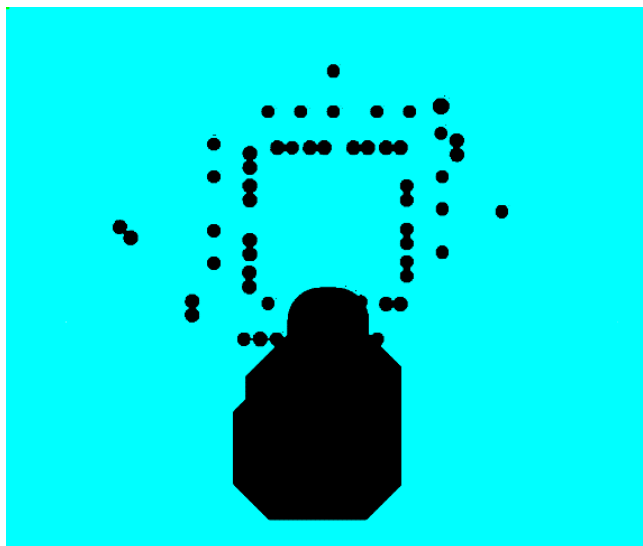


Figure 33. Ground Plane (Layer 6)

9.1.3. Output Clocks

Figure 34 shows the output clocks. Similar to the input clocks the output clocks have vias that immediately go to a buried layer with a ground plane above them and a ground flooded bottom layer. There is a ground flooding between the clock output pairs to avoid crosstalk. There should be a line of vias through the ground flood on either side of the output clocks to ensure that the ground flood immediately next to the differential pairs has a low inductance path to the ground plane on layers 3 and 6.

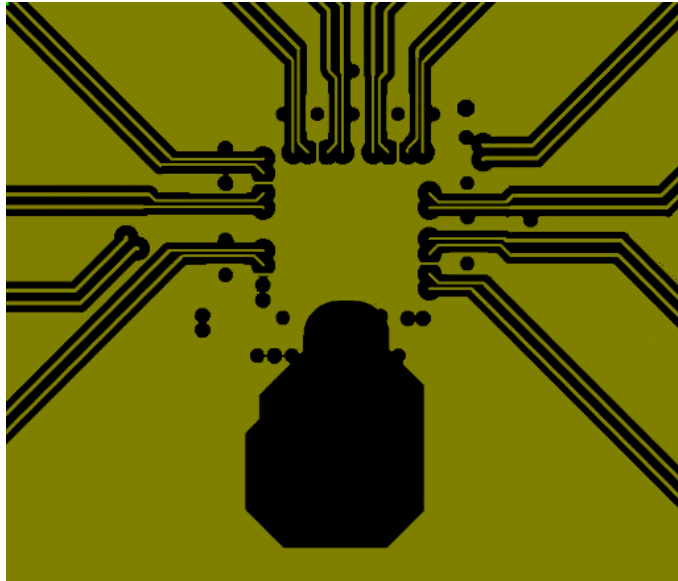


Figure 34. Output Clock Layer (Layer 7)

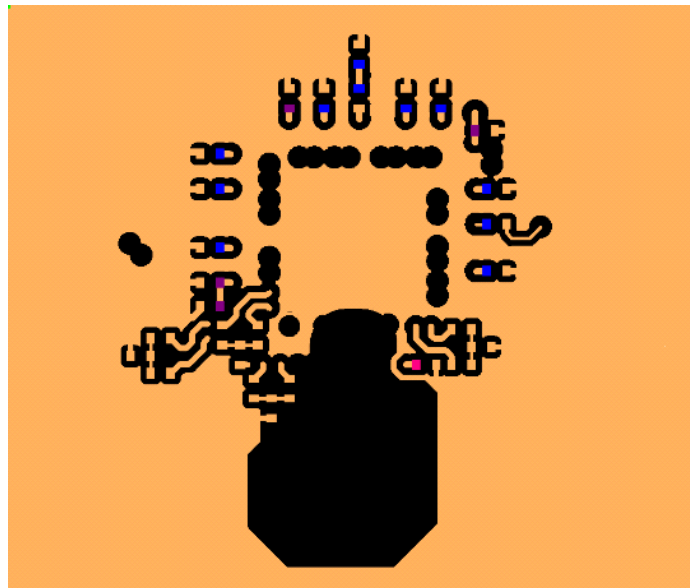


Figure 35. Bottom Layer Ground Flooded (Layer 8)

9.2. 44-Pin QFN Si5340 Layout Recommendations

This section details the layout recommendations for the 44-pin Si5340 device using an example 6-layer PCB.

The following guidelines details images of a six layer board with the following stack:

- Layer 1: device layer, with low speed CMOS control/status signals, ground flooded
- Layer 2: crystal shield, output clocks, ground flooded
- Layer 3: ground plane
- Layer 4: power distribution, ground flooded
- Layer 5: input clocks, ground flooded
- Layer 6: low-speed CMOS control/status signals, ground flooded

This layout was designed to implement either a crystal or an external clock as the XAXB reference. The top layer is flooded with ground. The clock output pins go to layer 2 using vias to avoid crosstalk during transit. When the clock output signals are on layer 2 there is a ground shield above, below and on all sides for protection. Output clocks should always be routed on an internal layer with ground reference planes directly above and below. The plane that has the routing for the output clocks should have ground flooded near the clock traces to further isolate the clocks from noise and other signals.

9.2.1. Si5340 Applications without a Crystal as the Reference Clock

If the application does not use a crystal, then the X1 and X2 pins should be left as “no connect” and should not be tied to ground. In addition, there is no need for a crystal shield or the voids underneath the shield. If there is a differential external clock input on XAXB there should be a termination circuit near the XA and XB pins. This termination circuit should be two $50\ \Omega$ resistors and one $0.1\ \mu\text{F}$ cap connected in the same manner as on the other clock inputs (IN0, IN1 and IN2). The clock input on XAXB must be ac-coupled. Care should be taken to keep all clock inputs well isolated from each other as well as any other dynamic signal.

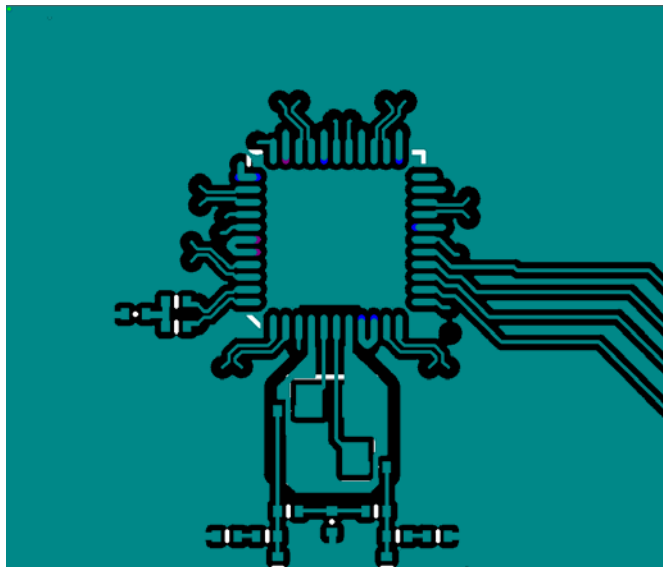


Figure 36. Device Layer (Layer 1)

9.2.2. Si5340 Crystal Guidelines

All recommendations from section 9.1.2 also apply to this section.

Figure 37 is the second layer. The second layer implements the shield underneath the crystal. The shield extends underneath the entire crystal and the X1 and X2 pins. There should be no less than 12 vias to connect the X1X2 planes on layers 1 and 2. These vias are not shown in any other figures. All traces with signals that are not static must be kept well away from the crystal and the X1X2 plane.

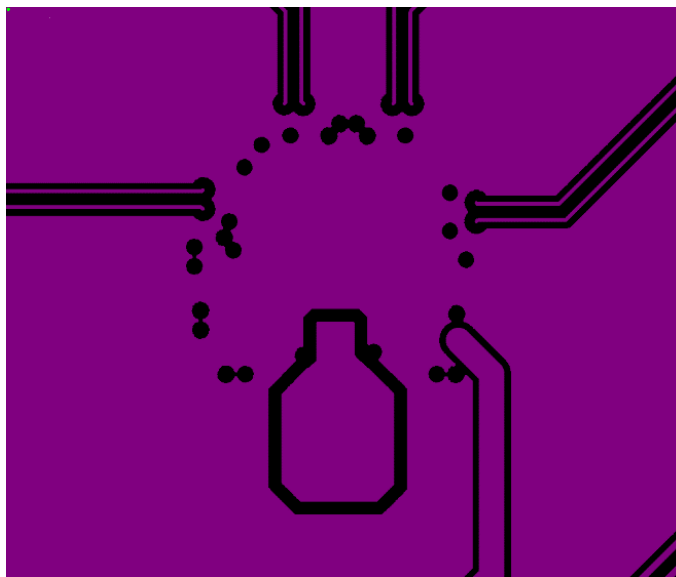


Figure 37. Crystal Shield Layer 2

Figure 38 is the ground plane and shows a void underneath the crystal shield.

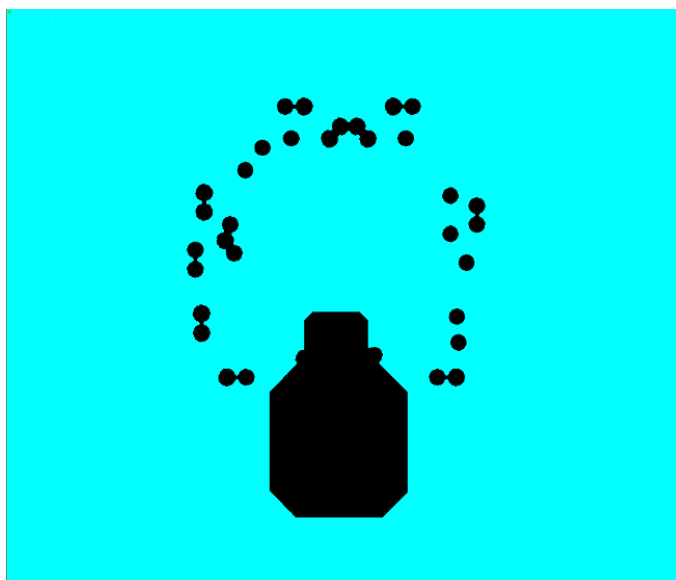


Figure 38. Ground Plane (Layer 3)

Figure 39 is a power plane showing the clock output power supply traces. The void underneath the crystal shield is continued.

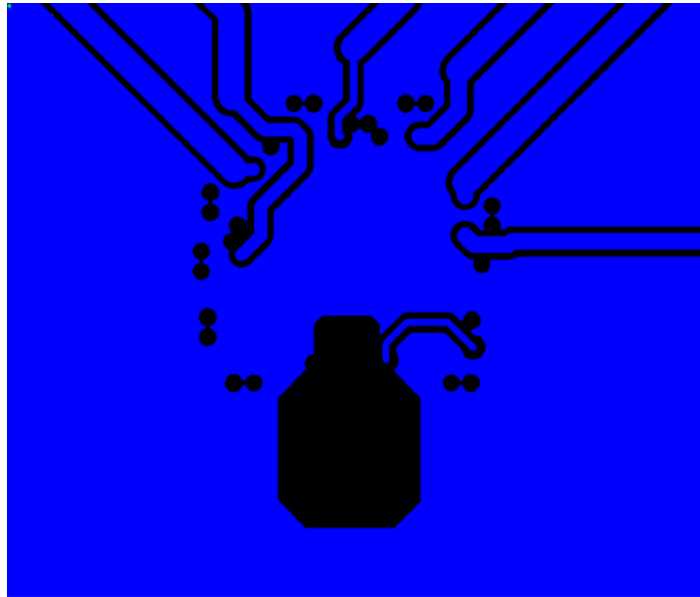


Figure 39. Power Plane and Clock Output Power Supply Traces (Layer 4)

Figure 40 shows layer 5 and the clock input traces. Similar to the clock output traces, they are routed to an inner layer and surrounded by ground to avoid crosstalk.

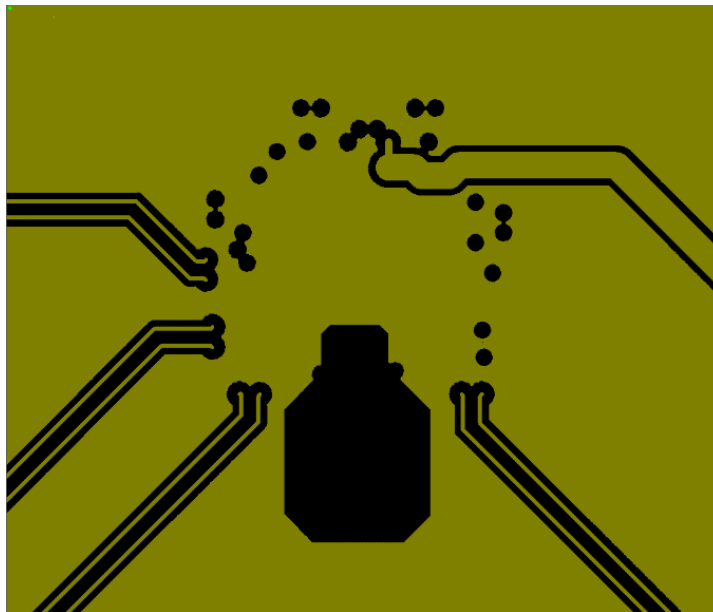


Figure 40. Clock Input Traces (Layer 5)

Figure 41 shows the bottom layer, which continues the void underneath the shield. Layer 6 and layer 1 are mainly used for low speed CMOS control and status signals for which crosstalk is not a significant issue. PCB ground can be placed under the X1X2 shield as long as the PCB ground is at least 0.05 inches below it.

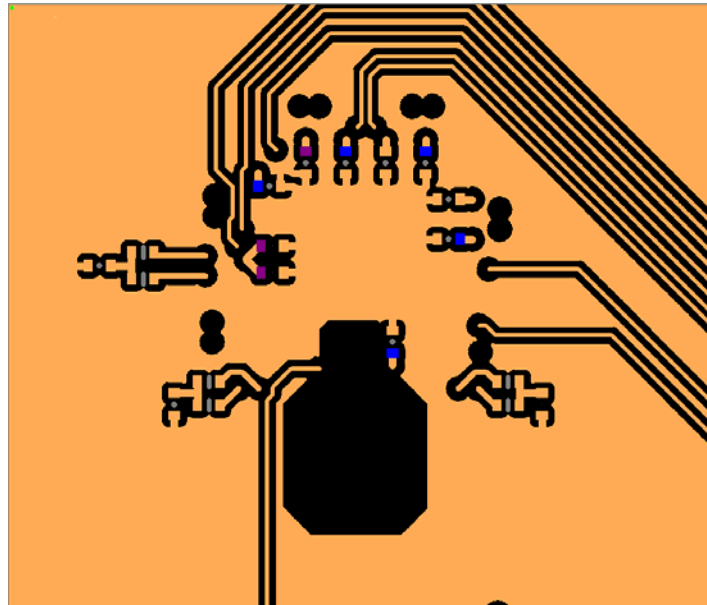


Figure 41. Low-Speed CMOS Control and Status Signal Layer 6 (Bottom Layer)

For any high-speed, low-jitter application, the clock signal runs should be impedance-controlled to $100\ \Omega$ differential or $50\ \Omega$ single-ended. Differential signaling is preferred because of its increased immunity to common-mode noise. All clock I/O runs should be properly terminated.

10. Power Management

10.1. Power Management Features

Several unused functions can be powered down to minimize power consumption. The registers listed in Table 27 are used for powering down different features.

Table 27. Power Management Registers

Register Name	Hex Address [Bit Field]		Function
	Si5341	Si5340	
PDN	0x001E[0]		This bit allows powering down the device. The serial interface remains powered during power down mode.
OUT0_PDN	0x0108[0]	0x0112[0]	Powers down unused clock outputs.
OUT1_PDN	0x010D[0]	0x011C[0]	
OUT2_PDN	0x0112[0]	0x0126[0]	
OUT3_PDN	0x0117[0]	0x012B[0]	
OUT4_PDN	0x011C[0]	—	
OUT5_PDN	0x0121[0]	—	
OUT6_PDN	0x0126[0]	—	
OUT7_PDN	0x012B[0]	—	
OUT8_PDN	0x0130[0]	—	
OUT9_PDN	0x013A[0]	—	
OUT_PDN_ALL	0x0145[0]		Power down all output drivers
XAXB_PDNB	0x090E[1]		0-Power down the oscillator and buffer circuitry at the XA/XB pins 1- No power down

10.2. Power Supply Recommendations

The power supply filtering generally is important for optimal timing performance. The Si5341/0 devices have multiple stages of on-chip regulation to minimize the impact of board level noise on clock jitter. Following conventional power supply filtering and layout techniques will further minimize signal degradation from the power supply.

It is recommended to use a 0402, 1.0 μ F ceramic capacitor on each VDD for optimal performance. Because of the extensive internal voltage regulation this will be sufficient unless the power supply has very high noise. If the power supply might have very high noise, then it is suggested to include an optional, single 0603 (resistor/ferrite) bead in series with each supply to enable additional filtering if needed for very high noise supply voltages. This resistor/ferrite should initially be a 0 ohm resistor. If additional supply filtering is needed then a ferrite component can replace the 0 ohm resistor. Note that the ferrite component will resonate with the bypass capacitor and can actually degrade the bypass filtering around the frequency of the resonance.

11. Register Map

11.1. Base (“Blank”) vs. Factory Preprogrammed (“Custom OPN”) Devices

The Si5341/40 devices can be ordered as “base” or “factory-preprogrammed” (custom OPN) versions.

11.1.1. “Base” Devices (Sometimes Referred to as “Blank” Devices)

- Example “base” orderable part numbers (OPNs) are of the form “Si5341A-A-GM” or “Si5340B-A-GM”.
- Base devices are available for applications where volatile reads and writes are used to program and configure the device for a particular application. Base devices do include a basic frequency plan to facilitate factory production testing. See on-line lookup utility at: <http://www.silabs.com/products/clocksoscillators/pages/clockbuilderlookup.aspx> to access the default configuration plan for any base OPN). However, base devices do not power up in a usable state (all output clock are disabled).
- Programming a base device is mandatory to achieve a usable configuration.

11.1.2. “Factory Preprogrammed” (Custom OPN) Devices

- Preprogrammed devices are specified using a “custom OPN”, such as Si5341A-A-xxxxx-GM, where xxxxx is a sequence of characters assigned by Silicon Labs for each customer-specific configuration.
- These characters are referred to as the “OPN ID”. Customers must initiate custom OPN creation using the ClockBuilder Pro software.
- Many customers prefer to order devices which are factory preprogrammed for a particular application that includes specifying the XAXB reference frequency/type, the clock input frequencies, the clock output frequencies, as well as the other options, such as automatic clock selection, loop BW, etc. The ClockBuilder Pro software is required to select among all of these options and produce a project file which Silicon Labs uses to preprogram all devices with custom orderable part number (“custom OPN”).
- Custom OPN devices contain all of the initialization information in their non-volatile memory (NVM) so that it powers up fully configured and ready to go.
- Because preprogrammed devices are inherently quite different from one another, the default power up values of the registers can be determined using the custom OPN utility at: <http://www.silabs.com/products/clocksoscillators/pages/clockbuilderlookup.aspx>
- Custom OPN devices include a device top mark which includes the unique OPN ID. Refer to the device data sheet’s Ordering Guide and Top Mark sections for details.

Both “base” and “factory preprogrammed” devices can have their operating configurations changed at any time using volatile reads and writes to the registers. Both types of devices can also have their current register configuration written to the NVM by executing an NVM bank burn sequence (see “3.2. NVM Programming” on page 13). NVM bank burns can be done up to two times, for either base or factory pre-programmed, custom OPN devices.

11.1.3. Register Map Overview and Default Settings Values

The Si5341/40 family has a large register map and is divided into separate pages. Each page contains a total of 256 registers, although all 256 registers are not used. Register 1 on each page is reserved to indicate the page and register 255 is reserved for the device ready status. The following is a summary of the content that can be found on each of the pages. Note any page that is not listed is not used for the device. Do not attempt to write to registers that have not been described in this document, even if they are accessible. Note that the default value will depend on the values loaded into NVM, which is determined by the part number.

Where not provided in the register map information below, you can get the default values of the register map settings, by accessing the part number lookup utility at: <http://www.silabs.com/products/clocksoscillators/pages/clockbuilderlookup.aspx> Register map settings values are listed in the datasheet addendum, which can be accessed by using the link above. The register maps are broken out for the Si5341 and Si5340 separately.

11.2. Si5341 Register Map

Because preprogrammed devices are inherently quite different from one another, the default power up values of the registers can be determined using the custom OPN utility at: <http://www.silabs.com/products/clocksoscillators/pages/clockbuilderlookup.aspx>.

Table 28. Register Map Paging Descriptions

Page	Start Address (Hex)	Start Address (Decimal)	Contents
Page 0	0000h	0	Alarms, interrupts, reset, device ID, revision ID
Page 1	0100h	256	Clock output configuration
Page 2	0200h	512	P,R dividers, scratch area
Page 3	0300h	768	Output N dividers, N divider Finc/Fdec
Page 9	0900h	2304	Control IO configuration

R = Read Only

R/W = Read Write

S = Self Clearing

Registers that are sticky are cleared by writing "0" to the bits that have been set in hardware. A self-clearing bit will clear on its own when the state has changed.

Some registers that are listed in the Data Sheet Addendum are not documented in the Register Map below because they are set and maintained by Clock Builder Pro. In almost all circumstances, these registers should not be modified by the user. For more details, please contact Silicon Labs.

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11.2.1. Page 0 Registers Si5341

Register 0x0000 Die Rev

Reg Address	Bit Field	Type	Name	Description
0x0000	3:0	R	DIE_REV	4- bit Die Revision Number 0 = Silicon Revision A0 1 = Silicon Revision A1

Register 0x0001 Page

Reg Address	Bit Field	Type	Name	Description
0x0001	7:0	R/W	PAGE	Selects one of 256 possible pages.

There is the “Page Register” which is located at address 0x01 on every page. When read, it will indicate the current page. When written, it will change the page to the value entered. There is a page register at address 0x0001, 0x0101, 0x0201, 0x0301, ... etc.

Register 0x0002–0x0003 Base Part Number

Reg Address	Bit Field	Type	Name	Description
0x0002	7:0	R	PN_BASE	Four-digit “base” part number, one nibble per digit Example: Si5341A-A-GM. The base part number (OPN) is 5341, which is stored in this register
0x0003	15:8	R	PN_BASE	

Register 0x0004 Device Speed/Synthesis Mode Grade

Reg Address	Bit Field	Type	Name	Description
0x0004	7:0	R	GRADE	One ASCII character indicating the device speed grade 0 = Not Graded 1 = A 2 = B 3 = C 4 = D

Register 0x0005 Device Revision

Reg Address	Bit Field	Type	Name	Description
0x0005	7:0	R	DEVICE_REV	One ASCII character indicating the device revision level. 0 = A Example Si5341C-A12345-GM, the device revision is “A” and stored as 0

Register 0x0006–0x0008 Tool Version

Reg Address	Bit Field	Type	Name	Description
0x0006	3:0	R	TOOL_VERSION[3:0]	Special
0x0006	7:4	R	TOOL_VERSION[7:4]	Revision
0x0007	7:0	R	TOOL_VERSION[15:8]	Minor[7:0]
0x0008	0	R	TOOL_VERSION[15:8]	Minor[8]
0x0008	4:1	R	TOOL_VERSION[16]	Major
0x0008	7:5	R	TOOL_VERSION[13:17]	Tool. 0 for Clockbuilder Pro

Register 0x0009 Temperature Grade

Reg Address	Bit Field	Type	Name	Description
0x0009	7:0		TEMP_GRADE	Device temperature grading 0 = Industrial (–40 ° C to 85 ° C) ambient conditions

Register 0x000A Package ID

Reg Address	Bit Field	Type	Name	Description
0x000A	7:0		PKG_ID	Package ID 0 = 9x9 mm 64 QFN 1 = 7x7 mm 44 QFN

Part numbers are of the form:

Si<Part Num Base><Grade>-<Device Revision><OPN ID>-<Temp Grade><Package ID>

Examples:

Si5341C-A12345-GM.

Applies to a “custom” OPN (Ordering Part Number) device. These devices are factory pre-programmed with the frequency plan and all other operating characteristics defined by the user’s ClockBuilder Pro project file.

Si5341C-A-GM.

Applies to a “base” or “blank” OPN device. Base devices are factory pre-programmed to a specific base part type (e.g., Si5341 but **exclude** any user-defined frequency plan or other user-defined operating characteristics selected in ClockBuilder Pro.

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Register 0x000C Status Bits

Reg Address	Bit Field	Type	Name	Description
0x000C	0	R	SYSINCAL	1 if the device is calibrating.
0x000C	1	R	LOSXAXB	1 if there is no signal at the XAXB pins.
0x000C	2	R		
0x000C	3	R		
0x000C	4	R		
0x000C	5	R	SMBUS_TIMEOUT	1 if there is an SMBus timeout error.

Register 0x000D INx Loss of Signal (LOS) Alarms

Reg Address	Bit Field	Type	Name	Description
0x000D	2:0	R	LOSIN	1 if no clock is present at [IN2, IN1, IN0]
0x000D	3	R	LOSFB_IN	1 if no clock is present at LOSFB_IN

Note that each bit corresponds to the input. The LOS bits are not sticky.

- Input 0 (IN0) corresponds to LOS at 0x000D [0]
- Input 1 (IN1) corresponds to LOS at 0x000D [1]
- Input 2 (IN2) corresponds to LOS at 0x000D [2]
- See also LOSXAXB for LOS at the XAXB input

Register 0x0011 Sticky versions of Status Bits

Reg Address	Bit Field	Type	Name	Description
0x0011	0	R	SYSINCAL_FLG	Sticky version of SYSINCAL
0x0011	1	R	LOSXAXB_FLG	Sticky version of LOSXAXB
0x0011	2	R		
0x0011	3	R		
0x0011	4	R		
0x0011	5	R	SMBUS_TIMEOUT_FLG	Sticky version of SMBUS_TIMEOUT

These are sticky flag bits. They are cleared by writing zero to the bit that has been set.

Register 0x0012 INx LOS Flags

Reg Address	Bit Field	Type	Name	Description
0x0012	2:0	R/W	LOSIN_FLG	Sticky version of LOSIN. Write a 0 to clear.
0x0012	3	R/W	LOSFB_IN_FLG	Sticky version of LOSFB_IN. Write a 0 to clear.

Register 0x0017 Status Flag Interrupt Masks

Reg Address	Bit Field	Type	Name	Description
0x0017	0	R/W	SYSINCAL_INTR_MSK	1 to mask SYSINCAL_FLG from causing an interrupt
0x0017	1	R/W	LOSXAXB_FLG_MSK	1 to mask the LOSXAXB_FLG from causing an interrupt
0x0017	2	R/W		
0x0017	3	R/W		
0x0017	4	R/W		
0x0017	5	R/W	SMBUS_TIMEOUT_FLG_MSK	1 to mask SMBUS_TIMEOUT_FLG from causing an interrupt

These are the interrupt mask bits for the fault flags in register 0x0011. If a mask bit is set, the alarm will be blocked from causing an interrupt.

Register 0x0018 Interrupt Masks

Reg Address	Bit Field	Type	Name	Description
0x0018	2:0	R/W	LOS_IN_INTR_MSK	1 to mask the interrupt from LOSIN_FLG[2:0]
0x0018	3	R/W	LOSFB_IN_INTR_MSK	1 to mask the interrupt from the LOSFB_IN_FLG

- Input 0 (IN0) corresponds to LOS_IN_INTR_MSK 0x0018 [0]
- Input 1 (IN1) corresponds to LOS_IN_INTR_MSK 0x0018 [1]
- Input 2 (IN2) corresponds to LOS_IN_INTR_MSK 0x0018 [2]

Register 0x001C Soft Reset

Reg Address	Bit Field	Type	Name	Description
0x001C	0	S	SOFT_RST	1 Performs a soft rest. Resets the device while not re-downloading the register configuration from NVM. 0 No effect

This bits are of type “S”, which is self-clearing.

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Register 0x001D FINC, FDEC

Reg Address	Bit Field	Type	Name	Description
0x001D	0	S	FINC	1 A rising edge will cause a frequency increment. See also N_FSTEP_MSK and Nx_FSTEPW 0 No effect
0x001D	1	S	FDEC	1 A rising edge will cause a frequency decrement. See also N_FSTEP_MSK and Nx_FSTEPWi 0 No effect

Register 0x001E Sync, Power Down and Hard Reset

Reg Address	Bit Field	Type	Name	Description
0x001E	0	R/W	PDN	1 to put the device into low power mode
0x001E	1	R/W	HARD_RST	1 causes hard reset. The same as power up except that the serial port access is not held at reset. NVM is re-downloaded. This does not self-clear, so after setting the bit it must be cleared. 0 No reset
0x001E	2	S	SYNC	Logically equivalent to asserting the $\overline{\text{SYNC}}$ pin. Resets all R dividers so that synchronous output frequencies will be aligned.

Register 0x0021 Input Clock Selection

Reg Address	Bit Field	Type	Name	Description
0x0021	0	R/W	IN_SEL_REGCTRL	Selects between register controlled reference clock selection and pin controlled clock selection using IN_SEL1 and IN_SEL0 pins: 0 for pin controlled clock selection; 1 for register clock selection via IN_SEL bits
0x0021	2:1	R/W	IN_SEL	Selects the reference clock input to the PLL when IN_SEL_REGCTRL=1. 0 IN0 1 IN1 2 IN2 3 XA/XB

Register 0x002B SPI 3 vs 4 Wire

Reg Address	Bit Field	Type	Name	Description
0x002B	3	R/W	SPI_3WIRE	0 for 4-wire SPI, 1 for 3-wire SPI

Register 0x002C LOS Enable

Reg Address	Bit Field	Type	Name	Description
0x002C	3:0	R/W	LOS_EN	1 to enable LOS for the inputs other than XAXB; 0 for disable
0x002C	4	R/W	LOSXAXB_DIS	0 to enable LOS for the XAXB input

- Input 0 (IN0): LOS_EN[0]
- Input 1 (IN1): LOS_EN[1]
- Input 2 (IN2): LOS_EN[2]
- FB_IN: LOS_EN[3]

Register 0x002D Loss of Signal Requalification Time

Reg Address	Bit Field	Type	Name	Description
0x002D	1:0	R/W	LOS0_VAL_TIME	Clock Input 0 0 for 2 msec 1 for 100 msec 2 for 200 msec 3 for one second
0x002D	3:2	R/W	LOS1_VAL_TIME	Clock Input 1, same as above
0x002D	5:4	R/W	LOS2_VAL_TIME	Clock Input 2, same as above

When an input clock is gone (and therefore has an active LOS alarm), if the clock returns, there is a period of time that the clock must be within the acceptable range before the alarm is removed. This is the LOS_VAL_TIME.

Register 0x002E-0x002F LOS0 Trigger Threshold

Reg Address	Bit Field	Type	Name	Description
0x002E	7:0	R/W	LOS0_TRG_THR	16-bit Threshold Value
0x002F	15:8	R/W	LOS0_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 0, given a particular frequency plan.

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Register 0x0030-0x0031 LOS1 Trigger Threshold

Reg Address	Bit Field	Type	Name	Description
0x0030	7:0	R/W	LOS1_TRG_THR	16-bit Threshold Value
0x0031	15:8	R/W	LOS1_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 1, given a particular frequency plan.

Register 0x0032-0x0033 LOS2 Trigger Threshold

Reg Address	Bit Field	Type	Name	Description
0x0032	7:0	R/W	LOS2_TRG_THR	16-bit Threshold Value
0x0033	15:8	R/W	LOS2_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 2, given a particular frequency plan.

Register 0x0041-0x0044 LOS Pre-Divider for IN0, IN1, IN3, FB_IN

Reg Address	Bit Field	Type	Name	Description
0x0041	7:0	R/W	LOS0_DIV_SEL	A pre-divider that is configured by Clock-BUILDER Pro
0x0042	7:0	R/W	LOS1_DIV_SEL	A pre-divider that is configured by Clock-BUILDER Pro
0x0043	7:0	R/W	LOS2_DIV_SEL	A pre-divider that is configured by Clock-BUILDER Pro
0x0044	7:0	R/W	LOSFB_IN_DIV_SEL	A pre-divider that is configured by Clock-BUILDER Pro

The following are the predivider values for the above register values.

Register Value (Decimal)	Divider Value
0	1 (bypass)
1	2
2	4
3	8
4	16
5	32
6	64

Register Value (Decimal)	Divider Value
7	128
8	256
9	512
10	1024
11	2048
12	4096
13	8192
14	16384
15	32768
16	65536

Register 0x00FE Device Ready

Reg Address	Bit Field	Type	Name	Description
0x00FE	7:0	R	DEVICE_READY	0x0F when device is ready 0xF3 when device is not ready

Read-only byte to indicate when the device is ready to accept serial bus transactions. The user can poll this byte starting at power-on; when DEVICE_READY is 0x0F the user can safely read or write to any other register. This is only needed after power up or a hard reset using register bit 0x001E[1]. The “Device Ready” register is available on every page in the device at the second last register, 0xFE.

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Register 0x0102 All Output Clock Driver Disable

Reg Address	Bit Field	Type	Name	Description
0x0102	0	R/W	OUTALL_DISABLE_LOW	0 disables all output drivers. 1 no output drivers are disabled by this bit but other signals may disable the outputs.

Register 0x0108 Clock Output 0 Configs and DIV2 Mode

Reg Address	Bit Field	Type	Name	Description
0x0108	0	R/W	OUT0_PDN	Output driver 0: 0 to power up the driver, 1 to power down the driver. Clock outputs will be weakly pulled-low.
0x0108	1	R/W	OUT0_OE	Output driver 0: 0 to disable the output, 1 to enable the output
0x0108	2	R/W	OUT0_RDIV_FORCE2	0 R0 divider value is set by R0_REG 1 R0 divider value is forced into divide by 2

Register 0x0109 Clock Output 0 Format

Reg Address	Bit Field	Type	Name	Description
0x0109	2:0	R/W	OUT0_FORMAT	0 Reserved 1 swing mode (normal swing) differential 2 swing mode (high swing) differential 3 rail to rail swing mode differential 4 LVCMOS single ended 5–7 reserved
0x0109	3	R/W	OUT0_SYNC_EN	0 disable 1 enable enable/disable synchronized (glitchless) operation. When enabled, the power down and output enables are synchronized to the output clock.
0x0109	5:4	R/W	OUT0_DIS_STATE	Determines the state of an output driver when disabled, selectable as Disable low (0), Disable high (1), Disable mid (2) When disable mid is selected, the output common mode voltage will be the same when the output is disabled as when the output is enabled.
0x0109	7:6	R/W	OUT0_CMOS_DRV	LVCMOS output impedance.

See "5.2. Performance Guidelines for Outputs" on page 20.

Register 0x010A Clock Output 0 Amplitude and Common Mode Voltage

Reg Address	Bit Field	Type	Name	Description
0x010A	3:0	R/W	OUT0_CM	Output common mode voltage adjustment Programmable swing mode with normal or high swing configuration: Step size = 100 mV Range = 0.9 V to 2.3 V if VDDO = 3.3 V Range=0.6 V to 1.5 V if VDDO=2.5 V Range=0.5 V to 0.9 V if VDDO=1.8 V Rail-to-rail swing Mode configuration: No flexibility DRV0_CM = 6 if VDDO = 3.3 V (Vcm = 1.5 V) DRV0_CM = 10 if VDDO = 2.5 V (Vcm = 1.1 V) DRV0_CM = 13 if VDDO = 1.8 V (Vcm = 0.8 V) LVCMOS mode: Not supported/No effect
0x010A	6:4	R/W	OUT0_AMPL	Output swing adjustment Programmable swing mode with normal swing configuration: Step size = 100 mV Range = 100 mVpp-se to 800 mVpp-se Programmable swing mode with high swing configuration: Step size = 200 mV Range = 200 mVpp-se to 1600 mVpp-se Rail-to-rail swing mode: Not supported/No effect LVCMOS mode: Not supported/No effect

See the settings and values from Table 12 on page 24 for details of the settings. ClockBuilder Pro is used to select the correct settings for this register.

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Register 0x010B Clock Output 0 Mux and Inversion

Reg Address	Bit Field	Type	Name	Description
0x010B	2:0	R/W	OUT0_MUX_SEL	Output driver 0 input mux select. This selects the source of the multisynth. 0: N0 1: N1 2: N2 3: N3 4: N4 5: reserved 6: reserved 7: reserved
0x010B	7:6	R/W	OUT0_INV	0: CLK and $\overline{\text{CLK}}$ not inverted 1: $\overline{\text{CLK}}$ inverted 2: CLK and $\overline{\text{CLK}}$ inverted 3: CLK inverted

Each of the 10 output drivers can be connected to any of the five N dividers. More than 1 output driver can connect to the same N divider.

The 10 output drivers are all identical. The single set of descriptions above for output driver 0 applies to the other 9 output drivers.

Table 29. Registers for OUT1,2,3,4,5,6,7,8,9 as per above for OUT0

Register Address	Description	(Same as) Address
0x010D	OUT1_PDN, OUT1_OE, OUT1_RDIV_FORCE2	0x0108
0x010E	OUT1_FORMAT, _SYNC_EN, DIS_STATE, _CMOS_DRV	0x0109
0x010F	OUT1_AMPL, OUT1_CM	0x010A
0x0110	OUT1_MUX_SEL, OUT1_INV	0x010B
0x0112	OUT2_PDN, OUT2_OE, OUT2_RDIV_FORCE2	0x0108
0x0113	OUT2_FORMAT, _SYNC_EN, DIS_STATE, _CMOS_DRV	0x0109
0x0114	OUT2_AMPL, OUT2_CM	0x010A
0x0115	OUT2_MUX_SEL, OUT2_INV	0x010B
0x0117	OUT3_PDN, OUT3_OE, OUT3_RDIV_FORCE2	0x0108
0x0118	OUT3_FORMAT, _SYNC_EN, DIS_STATE, _CMOS_DRV	0x0109
0x0119	OUT3_AMPL, OUT3_CM	0x010A
0x011A	OUT3_MUX_SEL, OUT3_INV	0x010B
0x011C	OUT4_PDN, OUT4_OE, OUT4_RDIV_FORCE2	0x0108
0x011D	OUT4_FORMAT, _SYNC_EN, DIS_STATE, _CMOS_DRV	0x010A
0x011E	OUT4_AMPL, OUT4_CM	0x0105
0x011F	OUT4_MUX_SEL, OUT4_INV	0x010B
0x0121	OUT5_PDN, OUT5_OE, OUT5_RDIV_FORCE2	0x0108

Table 29. Registers for OUT1,2,3,4,5,6,7,8,9 as per above for OUT0 (Continued)

Register Address	Description	(Same as) Address
0x0122	OUT5_FORMAT, _SYNC_EN, DIS_STATE, _CMOS_DRV	0x0109
0x0123	OUT5_AMPL, OUT5_CM	0x010A
0x0124	OUT5_MUX_SEL, OUT5_INV	0x010B
0x0126	OUT6_PDN, OUT6_OE, OUT6_RDIV_FORCE2	0x0108
0x0127	OUT6_AMPL, OUT6_CM	0x0109
0x0128	OUT6_FORMAT, _SYNC_EN, DIS_STATE, _CMOS_DRV	0x010A
0x0129	OUT6_MUX_SEL, OUT6_INV	0x010B
0x012B	OUT7_PDN, OUT7_OE, OUT7_RDIV_FORCE2	0x0108
0x012C	OUT7_FORMAT, _SYNC_EN, DIS_STATE, _CMOS_DRV	0x0109
0x012D	OUT7_AMPL, OUT7_CM	0x010A
0x012E	OUT7_MUX_SEL, OUT7_INV	0x010B
0x0130	OUT8_PDN, OUT8_OE, OUT8_RDIV_FORCE2	0x0108
0x0131	OUT8_FORMAT, _SYNC_EN, DIS_STATE, _CMOS_DRV	0x0109
0x0132	OUT8_AMPL, OUT8_CM	0x010A
0x0133	OUT8_MUX_SEL, OUT8_INV	0x010B
0x013A	OUT9_PDN, OUT9_OE, OUT9_RDIV_FORCE2	0x0108
0x013B	OUT9_FORMAT, _SYNC_EN, DIS_STATE, _CMOS_DRV	0x0109
0x013C	OUT9_AMPL, OUT9_CM	0x010A
0x013D	OUT9_MUX_SEL, OUT9_INV	0x010B

Registers 0x0135 to 0x0139 User Scratch

Reg Address	Bit Field	Type	Name	Description
0x0135	7:0	R/W	User Scratch	User R/W byte
0x0136	7:0	R/W	User Scratch	User R/W byte
0x0137	7:0	R/W	User Scratch	User R/W byte
0x0138	7:0	R/W	User Scratch	User R/W byte
0x0139	7:0	R/W	User Scratch	User R/W byte

Register 0x0145 Power Down All Outputs

Reg Address	Bit Field	Type	Name	Description
0x0145	0	R/W	OUT_PDN_ALL	0- no effect 1- all drivers powered down

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11.2.3. Page 2 Registers Si5341

Register 0x0202-0x0205 XAXB Frequency Adjust

Reg Address	Bit Field	Type	Name	Description
0x0202	7:0	R/W	XAXB_FREQ_OFFSET	32 bit offset adjustment
0x0203	15:8	R/W	XAXB_FREQ_OFFSET	
0x0204	23:16	R/W	XAXB_FREQ_OFFSET	
0x0205	31:24	R/W	XAXB_FREQ_OFFSET	

The clock that is present on XAXB pins is used to create an internal frequency reference for the PLL. The XAXB_FREQ_OFFSET word is used to adjust this feedback divider of the PLL to compensate for frequency errors in the frequency at the XAXB pins.

Register 0x0206 PXAXB Divider

Reg Address	Bit Field	Type	Name	Description
0x0206	1:0	R/W	PXAXB	Sets the value for the divider on the XAXB input.

- 0 = divider value 1
- 1 = divider value 2
- 2 = divider value 4
- 3 = divider value 8

Registers 0x0208, 0x0212, 0x021C, 0x0226 P Dividers

Reg Address	Bit Field	Type	Name	Description
0x0208	7:0	R/W	P0	8-bit Integer Number
0x0212	7:0	R/W	P1	
0x021C	7:0	R/W	P2	
0x0226	7:0	R/W	PFB	

This set of registers configure the P-dividers which are located at the four input clocks seen in Figure 2. ClockBuilder Pro calculates the correct values for the P-dividers.

Register 0x0235-0x023A M Divider Numerator

Reg Address	Bit Field	Type	Name	Description
0x0235	7:0	R/W	M_NUM	44-bit Integer Number
0x0236	15:8	R/W	M_NUM	
0x0237	23:16	R/W	M_NUM	
0x0238	31:24	R/W	M_NUM	
0x0239	39:32	R/W	M_NUM	
0x023A	43:40	R/W	M_NUM	

Register 0x023B-0x023E M Divider Denominator

Reg Address	Bit Field	Type	Name	Description
0x023B	7:0	R/W	M_DEN	32-bit Integer Number
0x023C	15:8	R/W	M_DEN	
0x023D	23:16	R/W	M_DEN	
0x023E	31:24	R/W	M_DEN	

The M-divider numerator and denominator are set by ClockBuilder Pro for a given frequency plan.

Register 0x024A-0x024C R0 Divider

Reg Address	Bit Field	Type	Name	Description
0x024A	7:0	R/W	R0_REG	24-bit Integer Number. Divide value = (R0_REG+1) x 2 To set R0 = 2, set OUT0_RDIV_FORCE2 = 1, and then the R0_REG value is irrelevant.
0x024B	15:8	R/W	R0_REG	
0x024C	23:16	R/W	R0_REG	

The R dividers are with the output drivers and are even integer dividers. The R1–R9 dividers follow the same format as the R0 divider described above.

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Table 30. R Dividers for Outputs 1,2,3,4,5,6,7,8,9

Register Address	Name	Size	Same as Address
0x024D-0x024F	R1_REG	24-bit Integer Number	0x024A-0x024C
0x0250-0x0252	R2_REG	24-bit Integer Number	0x024A-0x024C
0x0253-0x0255	R3_REG	24-bit Integer Number	0x024A-0x024C
0x0256-0x0258	R4_REG	24-bit Integer Number	0x024A-0x024C
0x0259-0x025B	R5_REG	24-bit Integer Number	0x024A-0x024C
0x025C-0x025E	R6_REG	24-bit Integer Number	0x024A-0x024C
0x025F-0x0261	R7_REG	24-bit Integer Number	0x024A-0x024C
0x0262-0x0264	R8_REG	24-bit Integer Number	0x024A-0x024C
0x0268-0x026A	R9_REG	24-bit Integer Number	0x024A-0x024C

Register 0x026B–0x0272 Design ID

Reg Address	Bit Field	Type	Name	Description
0x026B	7:0	R/W	DESIGN_ID0	ASCII encoded string defined by CBPro user, with user defined space or null padding of unused characters. A user will normally include a configuration ID + revision ID. For example, "ULT.1A" with null character padding sets: DESIGN_ID0: 0x55 DESIGN_ID1: 0x4C DESIGN_ID2: 0x54 DESIGN_ID3: 0x2E DESIGN_ID4: 0x31 DESIGN_ID5: 0x41 DESIGN_ID6: 0x 00 DESIGN_ID7: 0x00
0x026C	15:8	R/W	DESIGN_ID1	
0x026D	23:16	R/W	DESIGN_ID2	
0x026E	31:24	R/W	DESIGN_ID3	
0x026F	39:32	R/W	DESIGN_ID4	
0x0270	47:40	R/W	DESIGN_ID5	
0x0271	55:48	R/W	DESIGN_ID6	
0x0272	63:56	R/W	DESIGN_ID7	

Register 0x0278-0x027C OPN Identifier

Reg Address	Bit Field	Type	Name	Description
0x0278	7:0	R/W	OPN_ID0	OPN unique identifier. ASCII encoded. For example, with OPN: 5341C-A12345-GM, 12345 is the OPN unique identifier, which sets: OPN_ID0: 0x31 OPN_ID1: 0x32 OPN_ID2: 0x33 OPN_ID3: 0x34 OPN_ID4: 0x35
0x0279	15:8	R/W	OPN_ID1	
0x027A	23:16	R/W	OPN_ID2	
0x027B	31:24	R/W	OPN_ID3	
0x027C	39:32	R/W	OPN_ID4	

Part numbers are of the form:

Si<Part Num Base><Grade>-<Device Revision><OPN ID>-<Temp Grade><Package ID>

Examples:

Si5341C-A12345-GM.

Applies to a “custom” OPN (Ordering Part Number) device. These devices are factory pre-programmed with the frequency plan and all other operating characteristics defined by the user’s ClockBuilder Pro project file.

Si5341C-A-GM.

Applies to a “base” or “blank” OPN device. Base devices are factory pre-programmed to a specific base part type (e.g., Si5341 but **exclude** any user-defined frequency plan or other user-defined operating characteristics selected in ClockBuilder Pro.

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11.2.4. Page 3 Register Si5341

Register 0x027D OPN Revision

Reg Address	Bit Field	Type	Name	Description
0x27D	7:0	R/W	OPN_Revision	ClockBuilder Pro sets this value based upon changes to the NVM for a given OPN.

Register 0x027E Baseline ID

Reg Address	Bit Field	Type	Name	Description
0x27E	7:0	R/W	BaseLine ID	An identifier for the device NVM without the frequency plan programmed into NVM.

Register 0x0302-0x0307 N0 Numerator

Reg Address	Bit Field	Type	Name	Description
0x0302	7:0	R/W	N0_NUM	44-bit Integer Number
0x0303	15:8	R/W	N0_NUM	
0x0304	23:16	R/W	N0_NUM	
0x0305	31:24	R/W	N0_NUM	
0x0306	39:32	R/W	N0_NUM	
0x0307	43:40	R/W	N0_NUM	

The N dividers are interpolative dividers that are used as output dividers that feed into the R dividers. ClockBuilder Pro calculates the correct values for the N-dividers.

Register 0x0308-0x030B N0 Denominator

Reg Address	Bit Field	Type	Name	Description
0x0308	7:0	R/W	N0_DEN	32-bit Integer Number
0x0309	15:8	R/W	N0_DEN	
0x030A	23:16	R/W	N0_DEN	
0x030B	31:24	R/W	N0_DEN	

Table 31. N1, N2, N3 Numerator and Denominators

Register Address	Name	Size	Same as Address
0x030D-0x0312	N1_NUM	44-bit Integer Number	0x0302-0x0307
0x0313-0x0316	N1_DEN	32-bit Integer Number	0x0308-0x030B
0x0318-0x031D	N2_NUM	44-bit Integer Number	0x0302-0x0307
0x031E-0x0321	N2_DEN	32-bit Integer Number	0x0308-0x030B
0x0323-0x0328	N3_NUM	44-bit Integer Number	0x0302-0x0307
0x0329-0x032C	N3_DEN	32-bit Integer Number	0x0308-0x030B
0x032E-0x0333	N4_NUM	44-bit Integer Number	0x0302-0x0307
0x0334-0x0337	N4_DEN	32-bit Integer Number	0x0308-0x030B

Register 0x0339 FINC/FDEC Masks

Reg Address	Bit Field	Type	Name	Description
0x0339	4:0	R/W	N_FSTEP_MSK	0 to enable FINC/FDEC updates 1 to disable FINC/FDEC updates

- Bit 0 corresponds to MultiSynth N0 N_FSTEP_MSK 0x0339[0]
- Bit 1 corresponds to MultiSynth N1 N_FSTEP_MSK 0x0339[1]
- Bit 2 corresponds to MultiSynth N2 N_FSTEP_MSK 0x0339[2]
- Bit 3 corresponds to MultiSynth N3 N_FSTEP_MSK 0x0339[3]
- Bit 4 corresponds to MultiSynth N4 N_FSTEP_MSK 0x0339[4]

There is one mask bit for each of the five N dividers.

Register 0x033B-0x0340 N0 Frequency Step Word

Reg Address	Bit Field	Type	Name	Description
0x033B	7:0	R/W	N0_FSTEPW	44-bit Integer Number
0x033C	15:8	R/W	N0_FSTEPW	
0x033D	23:16	R/W	N0_FSTEPW	
0x033E	31:24	R/W	N0_FSTEPW	
0x033F	39:32	R/W	N0_FSTEPW	
0x0340	43:40	R/W	N0_FSTEPW	

This is a 44-bit integer value which is directly added (FDEC) or subtracted (FINC) from the Nx_NUM parameter when FINC or FDEC is asserted. ClockBuilder Pro calculates the correct values for the N0 Frequency Step Word. Each N divider has the ability to add or subtract up to a 44-bit value. The Nx_NUM register value does not change when an FINC or FDEC is performed so that the starting point of Nx_NUM is in the Nx_NUM register.

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Table 32. Frequency Step Word for N1, N2, N3, N4

Register Address	Name	Size	Same as Address
0x0341-0x0346	N1_FSTEPW	44-bit Integer Number	0x033B-0x0340
0x0347-0x034C	N2_FSTEPW	44-bit Integer Number	0x033B-0x0340
0x034D-0x0352	N3_FSTEPW	44-bit Integer Number	0x033B-0x0340
0x0353-0x0358	N4_FSTEPW	44-bit Integer Number	0x033B-0x0340

Register 0x0359–0x035A N0 Delay Control

Reg Address	Bit Field	Type	Name	Description
0x0359	7:0	R/W	N0_DELAY[7:0]	Lower byte of N0_DELAY[15:0]
0x035A	7:0	R/W	N0_DELAY[15:8]	Upper byte of N0_DELAY[15:0]

Register 0x035B-0x035C Divider N1 Delay Control

Reg Address	Bit Field	Type	Name	Description
0x35B	7:0	R/W	N1_DELAY[7:0]	Lower byte of N1_DELAY[15:0]
0x35C	7:0	R/W	N1_DELAY[15:8]	Upper byte of N1_DELAY[15:0]

Register 0x035D-0x035E Divider N2 Delay Control

Reg Address	Bit Field	Type	Name	Description
0x35D	7:0	R/W	N2_DELAY[7:0]	Lower byte of N2_DELAY[15:0]
0x35E	7:0	R/W	N2_DELAY[15:8]	Upper byte of N2_DELAY[15:0]

Register 0x035F-0x0360 Divider N3 Delay Control

Reg Address	Bit Field	Type	Name	Description
0x35F	7:0	R/W	N3_DELAY[7:0]	Lower byte of N3_DELAY[15:0]
0x360	7:0	R/W	N3_DELAY[15:8]	Upper byte of N3_DELAY[15:0]

Register 0x0361–0x0362 Divider N4 Delay Control

Reg Address	Bit Field	Type	Name	Description
0x0361	7:0	R/W	N4_DELAY[7:0]	Lower byte of N4_DELAY[15:0]
0x0362	15:8	R/W	N4_DELAY[15:8]	Upper byte of N4_DELAY[15:0]

The delay in seconds is $Nx_DELAY / (256 \times F_{vco})$ where F_{vco} is the VCO frequency in Hz. The maximum positive and negative delay is $\pm(2^{15}-1)/(256 \times F_{vco})$. Nx_DELAY values are only applied at power up or during a reset. ClockBuilder Pro calculates the correct value for this register. It is expected that only the upper byte of Nx_DELAY is necessary as the step sizes in the lower byte are so small as to be essentially irrelevant.

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Register 0x090E XAXB Configuration

Reg Address	Bit Field	Type	Name	Description
0x090E	0	R/W	XAXB_EXTCLK_EN	0 to use a crystal at the XAXB pins 1 to use an external clock source at the XAXB pins
0x090E	1	R/W	XAXB_PDNB	0-Power down the oscillator and buffer circuitry at the XA/XB pins 1- No power down

Register 0x091C Enable/Disable Zero Delay Mode

Reg Address	Bit Field	Type	Name	Description
0x091C	2:0	R/W	ZDM_EN	0-2 Reserved 3 Zero Delay Mode 4 Normal Mode 5-7 Reserved

Register 0x0943 Status and Control I/O Voltage Select

Reg Address	Bit Field	Type	Name	Description
0x0943	0	R/W	IO_VDD_SEL	0 for 1.8 V external connections 1 for 3.3 V external connections

The IO_VDD_SEL configuration bit selects the option of operating the serial interface voltage thresholds from the VDD or the VDDA pin. By default the IO_VDD_SEL bit is set to the VDD option. The serial interface pins are always 3.3 V tolerant even when the device's VDD pin is supplied from a 1.8 V source. When the I²C or SPI host is operating at 3.3 V and the Si5341/40 IO_VDD_SEL = 1.8 V, the host must write the IO_VDD_SEL configuration bit to the VDDA option. This will ensure that both the host and the serial interface are operating at the optimum voltage thresholds. When IO_VDD_SEL = 0, the status outputs will have a V_{OH} of ~1.8 V. When IO_VDD_SEL = 1 the status outputs will have a V_{OH} of ~3.3 V and the control inputs expect 3.3 V CMOS levels.

Register 0x0949 Clock Input Control and Configuration

Reg Address	Bit Field	Type	Name	Description
0x0949	3:0	R/W	IN_EN	Enables for the four inputs clocks, IN0 through FB_IN. 1 to enable, 0 to disable

- Input 0 corresponds to IN_EN 0x0949 [0]
- Input 1 corresponds to IN_EN 0x0949 [1]
- Input 2 corresponds to IN_EN 0x0949 [2]
- FB_IN corresponds to IN_EN 0x0949 [3]

11.3. Si5340 Registers

Because preprogrammed devices are inherently quite different from one another, the default power up values of the registers can be determined using the custom OPN utility at: <http://www.silabs.com/products/clocksoscillators/pages/clockbuilderlookup.aspx>. Some registers that are listed in the Data Sheet Addendum are not documented in the Register Map below because they are set and maintained by Clock Builder Pro. In almost all circumstances, these registers should not be modified by the user. For more details, please contact Silicon Labs.

11.3.1. Page 0 Registers Si5340

Register 0x0000 Die Rev

Reg Address	Bit Field	Type	Name	Description
0x0000	3:0	R	DIE_REV	4- bit Die Revision Number

Register 0x0001 Page

Reg Address	Bit Field	Type	Name	Description
0x0001	7:0	R/W	PAGE	Selects one of 256 possible pages.

There is the "Page Register" which is located at address 0x01 on every page. When read, it will indicate the current page. When written, it will change the page to the value entered. There is a page register at address 0x0001, 0x0101, 0x0201, 0x0301, ... etc.

Register 0x0002–0x0003 Base Part Number

Reg Address	Bit Field	Type	Name	Description
0x0002	7:0	R	PN_BASE	Four-digit "base" part number, one nibble per digit Example: Si5340A-A-GM. The base part number (OPN) is 5340, which is stored in this register
0x0003	15:8	R	PN_BASE	

Register 0x0004 Device Speed/Synthesis Mode Grade

Reg Address	Bit Field	Type	Name	Description
0x0004	7:0	R	GRADE	One ASCII character indicating the device speed grade 0 = Not Graded 1 = A 2 = B 3 = C 4 = D

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Register 0x0005 Device Revision

Reg Address	Bit Field	Type	Name	Description
0x0005	7:0	R	DEVICE_REV	One ASCII character indicating the device revision level. 0 = A Example Si5340C-A12345-GM, the device revision is "A" and stored as 0

Register 0x0006–0x0008 NVM Identifier

Reg Address	Bit Field	Type	Name	Description
0x0006	3:0	R	TOOL_VERSION[3:0]	Special
0x0006	7:4	R	TOOL_VERSION[7:4]	Revision
0x0007	7:0	R	TOOL_VERSION[15:8]	Minor[7:0]
0x0008	0	R	TOOL_VERSION[15:8]	Minor[8]
0x0008	4:1	R	TOOL_VERSION[16]	Major
0x0008	7:5	R	TOOL_VERSION[13:17]	Tool. 0 for Clockbuilder Pro

Register 0x0009 Temperature Grade

Reg Address	Bit Field	Type	Name	Description
0x0009	7:0		TEMP_GRADE	Device temperature grading 0 = Industrial (-40° C to 85° C) ambient conditions

Register 0x000A Package ID

Reg Address	Bit Field	Type	Name	Description
0x000A	7:0		PKG_ID	Package ID 0 = 9x9 mm 64 QFN 1 = 7x7 mm 44 QFN

Part numbers are of the form:

Si<Part Num Base><Grade>-<Device Revision><OPN ID>-<Temp Grade><Package ID>

Examples:

Si5341C-A-12345-GM.

Applies to a "custom" OPN (Ordering Part Number) device. These devices are factory pre-programmed with the frequency plan and all other operating characteristics defined by the user's ClockBuilder Pro project file.

Si5341C-A-GM.

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Applies to a “base” or “blank” OPN device. Base devices are factory pre-programmed to a specific base part type (e.g., Si5341 but **exclude** any user-defined frequency plan or other user-defined operating characteristics selected in ClockBuilder Pro.

Register 0x000C Status Bits

Reg Address	Bit Field	Type	Name	Description
0x000C	0	R	SYSINCAL	1 if the device is calibrating.
0x000C	1	R	LOSXAXB	1 if there is no signal at the XAXB pins.
0x000C	2	R		
0x000C	3	R		
0x000C	4	R		
0x000C	5	R	SMBUS_TIMEOUT	1 if there is an SMBus timeout error.

Register 0x000D INx Loss of Signal (LOS) Alarms

Reg Address	Bit Field	Type	Name	Description
0x000D	2:0	R	LOSIN	1 if no clock is present at [IN2, IN1, IN0]
0x000D	3	R	LOSFB_IN	1 if no clock is present at LOSFB_IN

Note that each bit corresponds to the input. The LOS bits are not sticky.

- Input 0 (IN0) corresponds to LOS at 0x000D [0]
- Input 1 (IN1) corresponds to LOS at 0x000D [1]
- Input 2 (IN2) corresponds to LOS at 0x000D [2]
- FB_IN corresponds to LOS at 0x000D [3]
- See also LOSXAXB for LOS at the XAXB input

Register 0x0011 Sticky versions of Status Bits

Reg Address	Bit Field	Type	Name	Description
0x0011	0	R	SYSINCAL_FLG	Sticky version of SYSINCAL
0x0011	1	R	LOSXAXB_FLG	Sticky version of LOSXAXB
0x0011	2	R		
0x0011	3	R		
0x0011	4	R		
0x0011	5	R	SMBUS_TIMEOUT_FLG	Sticky version of SMBUS_TIMEOUT

These are sticky flag bits. They are cleared by writing zero to the bit that has been set.

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Register 0x0012 INx LOS Flags

Reg Address	Bit Field	Type	Name	Description
0x0012	2:0	R/W	LOSIN_FLG	Sticky version of LOSIN. Write a 0 to clear.
0x0012	3	R/W	LOSFB_IN_FLG	Sticky version of LOSFB_IN. Write a 0 to clear.

Register 0x0017 Status Flag Interrupt Masks

Reg Address	Bit Field	Type	Name	Description
0x0017	0	R/W	SYSINCAL_INTR_MSK	1 to mask SYSINCAL_FLG from causing an interrupt
0x0017	1	R/W	LOSXAXB_FLG_MSK	1 to mask the LOSXAXB_FLG from causing an interrupt
0x0017	2	R/W		
0x0017	3	R/W		
0x0017	4	R/W		
0x0017	5	R/W	SMBUS_TIMEOUT_FLG_MSK	1 to mask SMBUS_TIMEOUT_FLG from causing an interrupt

These are the interrupt mask bits for the fault flags in register 0x0011. If a mask bit is set, the alarm will be blocked from causing an interrupt.

Register 0x0018 Interrupt Masks

Reg Address	Bit Field	Type	Name	Description
0x0018	2:0	R/W	LOSIN_INTR_MSK	1 to mask the interrupt from LOSIN_FLG[2:0]
0x0018	3	R/W	LOSFB_IN_INTR_MSK	1 to mask the interrupt from LOSFB_IN_FLG

Register 0x001C Soft Reset

Reg Address	Bit Field	Type	Name	Description
0x001C	0	S	SOFT_RST	1 Performs a soft rest. Resets the device while not re-downloading the register configuration from NVM. 0 No effect

This bits are of type “S”, which is self-clearing.

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Register 0x001D FINC, FDEC

Reg Address	Bit Field	Type	Name	Description
0x001D	0	S	FINC	1 A rising edge will cause a frequency increment. See also N_FSTEP_MSK and Nx_FSTEPW 0 No effect
0x001D	1	S	FDEC	1 A rising edge will cause a frequency decrement. See also N_FSTEP_MSK and Nx_FSTEPW 0 No effect

Register 0x001E Sync, Power Down and Hard Reset

Reg Address	Bit Field	Type	Name	Description
0x001E	0	R/W	PDN	1 to put the device into low power mode
0x001E	1	R/W	HARD_RST	1 causes hard reset. The same as power up except that the serial port access is not held at reset. NVM is re-downloaded. This does not self-clear, so after setting the bit it must be cleared. 0 No reset
0x001E	2	S	SYNC	Logically equivalent to asserting the SYNC pin. Resets all R dividers to the same state.

Register 0x0021 Input Clock Selection

Reg Address	Bit Field	Type	Name	Description
0x0021	0	R/W	IN_SEL_REGCTRL	Selects between register controlled reference clock selection and pin controlled clock selection using IN_SEL1 and IN_SEL0 pins: 0 for pin controlled clock selection 1 for register clock selection
0x0021	2:1	R/W	IN_SEL	Selects the reference clock input to the PLL when IN_SEL_REGCTRL=1. 0 IN0 1 IN1 2 IN2 3 XA/XB

Register 0x002B SPI 3 vs 4 Wire

Reg Address	Bit Field	Type	Name	Description
0x002B	3	R/W	SPI_3WIRE	0 for 4-wire SPI, 1 for 3-wire SPI

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Register 0x002C LOS Enable

Reg Address	Bit Field	Type	Name	Description
0x002C	3:0	R/W	LOS_EN	1 to enable LOS for a clock input; 0 for disable
0x002C	4	R/W	LOSXAXB_DIS	0 to enable LOS for the XAXB input 1 to disable the LOS for the XAXB input

- Input 0 (IN0): LOS_EN[0]
- Input 1 (IN1): LOS_EN[1]
- Input 2 (IN2): LOS_EN[2]
- FB_IN: LOS_EN[3]

Register 0x002D Loss of Signal Time Value

Reg Address	Bit Field	Type	Name	Description
0x002D	1:0	R/W	LOS0_VAL_TIME	Clock Input 0 0 for 2 msec 1 for 100 msec 2 for 200 msec 3 for one second
0x002D	3:2	R/W	LOS1_VAL_TIME	Clock Input 1, same as above
0x002D	5:4	R/W	LOS2_VAL_TIME	Clock Input 2, same as above

When an input clock is gone (and therefore has an active LOS alarm), if the clock returns, there is a period of time that the clock must be within the acceptable range before the alarm is removed. This is the LOS_VAL_TIME.

Register 0x002E-0x002F LOS0 Trigger Threshold

Reg Address	Bit Field	Type	Name	Description
0x002E	7:0	R/W	LOS0_TRG_THR	16-bit Threshold Value
0x002F	15:8	R/W	LOS0_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 0, given a particular frequency plan.

Register 0x0030-0x0031 LOS1 Trigger Threshold

Reg Address	Bit Field	Type	Name	Description
0x0030	7:0	R/W	LOS1_TRG_THR	16-bit Threshold Value
0x0031	15:8	R/W	LOS1_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 1, given a particular frequency plan.

Register 0x0032-0x0033 LOS2 Trigger Threshold

Reg Address	Bit Field	Type	Name	Description
0x0032	7:0	R/W	LOS2_TRG_THR	16-bit Threshold Value
0x0033	15:8	R/W	LOS2_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 2, given a particular frequency plan.

Register 0x0041-0x0044 LOS Pre-Divider for IN0, IN1, IN3, FB_IN

Reg Address	Bit Field	Type	Name	Description
0x0041	7:0	R/W	LOS0_DIV_SEL	A pre-divider that is configured by ClockBuilder Pro
0x0042	7:0	R/W	LOS1_DIV_SEL	A pre-divider that is configured by ClockBuilder Pro
0x0043	7:0	R/W	LOS2_DIV_SEL	A pre-divider that is configured by ClockBuilder Pro
0x0044	7:0	R/W	LOSFB_IN_DIV_SEL	A pre-divider that is configured by ClockBuilder Pro

The following are the predivider values for the above register values.

Register Value (Decimal)	Divider Value
0	1 (bypass)
1	2
2	4
3	8
4	16
5	32
6	64
7	128
8	256
9	512
10	1024
11	2048
12	4096
13	8192
14	16384
15	32768
16	65536

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Register 0x00FE Device Ready

Reg Address	Bit Field	Type	Name	Description
0x00FE	7:0	R	DEVICE_READY	0x0F when device is ready 0xF3 when device is not ready

Read-only byte to indicate when the device is ready to accept serial bus transactions. The user can poll this byte starting at power-on; when DEVICE_READY is 0x0F the user can safely read or write to any other register. This is only needed after power up or a hard reset using register bit 0x001E[1]. The “Device Ready” register is available on every page in the device at the second last register, 0xFE.

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Register 0x0102 All Output Clock Driver Disable

Reg Address	Bit Field	Type	Name	Description
0x0102	0	R/W	OUTALL_DISABLE_LOW	0 disables all output drivers 1 no output drivers are disabled by this bit but other signals may disable the outputs.

Register 0x0112 Clock Output Driver 0 Configs and Div2 Mode

Reg Address	Bit Field	Type	Name	Description
0x0112	0	R/W	OUT0_PDN	Output driver 0: 0 to power up the driver, 1 to power down the driver. Clock outputs will be weakly pulled-low.
0x0112	1	R/W	OUT0_OE	Output driver 0: 0 to disable the output, 1 to enable the output
0x0112	2	R/W	OUT0_RDIV_FORCE2	0 R0 divider value is set by R0_REG 1 R0 divider value is forced into divide by 2

Register 0x0113 Clock Output Driver 0 Format

Reg Address	Bit Field	Type	Name	Description
0x0113	2:0	R/W	OUT0_FORMAT	0 Reserved 1 swing mode (normal swing) differential 2 swing mode (high swing) differential 3 rail to rail swing mode differential 4 LVCMOS single ended 5–7 reserved
0x0113	3	R/W	OUT0_SYNC_EN	0 disable 1 enable
0x0113	5:4	R/W	OUT0_DIS_STATE	Determines the state of an output driver when disabled, selectable as Disable low (0), Disable high (1), Disable mid (2) When the disable state is mid, the output common mode voltage will be the same when the output is disabled as when the output is enabled.
0x0113	7:6	R/W	OUT0_CMOS_DRV	LVCMOS output impedance.

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Register 0x0114 Output 0 Amplitude and Common Mode Voltage

Reg Address	Bit Field	Type	Name	Description
0x0114	3:0	R/W	OUT0_CM	<p>Output common mode voltage adjustment</p> <p>Programmable swing mode with normal or high swing configuration:</p> <p>Step size = 100 mV</p> <p>Range = 0.9 V to 2.3 V if VDDO = 3.3 V</p> <p>Range = 0.6 V to 1.5V if VDDO = 2.5 V</p> <p>Range=0.5 V to 0.9 V if VDDO = 1.8 V</p> <p>Rail-to-rail swing Mode configuration:</p> <p>No flexibility</p> <p>DRV0_CM = 6 if VDDO = 3.3 V (Vcm = 1.5 V)</p> <p>DRV0_CM = 10 if VDDO = 2.5 V (Vcm = 1.1 V)</p> <p>DRV0_CM = 13 if VDDO = 1.8 V (Vcm = 0.8 V)</p> <p>LVC MOS mode:</p> <p>Not supported/No effect</p>
0x0114	6:4	R/W	OUT0_AMPL	<p>Output swing adjustment</p> <p>Programmable swing mode with normal swing configuration:</p> <p>Step size = 100 mV</p> <p>Range = 100 mVpp-se to 800 mVpp-se</p> <p>Programmable swing mode with high swing configuration:</p> <p>Step size = 200 mV</p> <p>Range = 200 mVpp-se to 1600 mVpp-se</p> <p>Rail-to-rail swing mode:</p> <p>Not supported/No effect</p> <p>LVC MOS mode:</p> <p>Not supported/No effect</p>

Register 0x0115 Clock Output 0 Mux and Inversion

Reg Address	Bit Field	Type	Name	Description
0x0115	2:0	R/W	OUT0_MUX_SEL	Output driver 0 input mux select. This selects the source of the multisynth. 0: N0 1: N1 2: N2 3: N3 4: reserved 5: reserved 6: reserved 7: reserved
0x0115	7:6	R/W	OUT0_INV	CLK and $\overline{\text{CLK}}$ not inverted $\overline{\text{CLK}}$ inverted CLK and $\overline{\text{CLK}}$ inverted CLK inverted

Each of the 10 output drivers can be connected to any of the five N dividers. More than 1 output driver can connect to the same N divider.

The four output drivers are all identical. The single set of descriptions above for output driver 0 applies to the other three output drivers.

Table 33. Registers for OUT1,2,3 as per OUT0 Above

Register Address	Description	(Same as) Address
0x0117	OUT1_PDN, OUT1_OE, OUT1_RDIV_FORCE2	0x0108
0x0118	OUT1_FORMAT, _SYNC_EN, DIS_STATE, _CMOS_DRV	0x0109
0x0119	OUT1_AMPL, OUT1_CM	0x010A
0x011A	OUT1_MUX_SEL, OUT1_INV	0x010B
0x011B	OUT2_PDN, OUT2_OE, OUT2_RDIV_FORCE2	0x0108
0x0126	OUT2_FORMAT, _SYNC_EN, DIS_STATE, _CMOS_DRV	0x0109
0x0127	OUT2_AMPL, OUT2_CM	0x010A
0x0128	OUT2_MUX_SEL, OUT2_INV	0x010B
0x0129	OUT3_PDN, OUT3_OE, OUT3_RDIV_FORCE2	0x0108
0x012A	OUT3_FORMAT, _SYNC_EN, DIS_STATE, _CMOS_DRV	0x0109
0x012B	OUT3_AMPL, OUT3_CM	0x010A
0x012C	OUT3_MUX_SEL, OUT3_INV	0x010B
0x012D	OUT4_PDN, OUT4_OE, OUT4_RDIV_FORCE2	0x0108
0x012E	OUT4_FORMAT, _SYNC_EN, DIS_STATE, _CMOS_DRV	0x010A
0x012F	OUT4_AMPL, OUT4_CM	0x0105

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Registers 0x0135–0x0139 User Scratch

Reg Address	Bit Field	Type	Name	Description
0x0135	7:0	R/W	User Scratch	User R/W byte
0x0136	7:0	R/W	User Scratch	User R/W byte
0x0137	7:0	R/W	User Scratch	User R/W byte
0x0138	7:0	R/W	User Scratch	User R/W byte
0x0139	7:0	R/W	User Scratch	User R/W byte

Register 0x0145 Power Down All Outputs

Reg Address	Bit Field	Type	Name	Description
0x0145	0	R/W	OUT_PDN_ALL	0- no effect 1- all drivers powered down

11.3.3. Page 2 Registers Si5340

Register 0x0202-0x0205 XAXB Frequency Adjust

Reg Address	Bit Field	Type	Name	Description
0x0202	7:0	R/W	XAXB_FREQ_OFFSET	32 bit offset adjustment
0x0203	15:8	R/W	XAXB_FREQ_OFFSET	
0x0204	23:16	R/W	XAXB_FREQ_OFFSET	
0x0205	31:24	R/W	XAXB_FREQ_OFFSET	

The clock that is present on XAXB pins is used to create an internal frequency reference for the PLL. The XAXB_FREQ_OFFSET word is used to adjust this feedback divider of the PLL to compensate for frequency errors in the frequency at the XAXB pins. The adjustment range is up to ± 1000 ppm. ClockBuilder Pro will calculate the value of XAXB Frequency adjust based upon the required shift in ppm.

Register 0x0206 PXAXB Divider Value

Reg Address	Bit Field	Type	Name	Description
0x0206	1:0	R/W	PXAXB	Sets the value for the divider on the XAXB input.

- 0 = divider value 1
- 1 = divider value 2
- 2 = divider value 4
- 3 = divider value 8

Registers 0x0208, 0x0212, 0x021C, 0x0226 P Dividers

Reg Address	Bit Field	Type	Name	Description
0x0208	7:0	R/W	P0	8-bit Integer Number
0x0212	7:0	R/W	P1	
0x021C	7:0	R/W	P2	
0x0226	7:0	R/W	PFB	

This set of registers configure the P-dividers which are located at the four input clocks seen in Figure 3 on page 11. ClockBuilder Pro calculates the correct values for the P-dividers.

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Register 0x0235-0x023A M Divider Numerator

Reg Address	Bit Field	Type	Name	Description
0x0235	7:0	R/W	M_NUM	44-bit Integer Number
0x0236	15:8	R/W	M_NUM	
0x0237	23:16	R/W	M_NUM	
0x0238	31:24	R/W	M_NUM	
0x0239	39:32	R/W	M_NUM	
0x023A	43:40		M_NUM	

Register 0x023B-0x023E M Divider Denominator

Reg Address	Bit Field	Type	Name	Description
0x023B	7:0	R/W	M_DEN	32-bit Integer Number
0x023C	15:8	R/W	M_DEN	
0x023D	23:16	R/W	M_DEN	
0x023E	31:24	R/W	M_DEN	

The M-divider numerator and denominator is determined by ClockBuilder Pro for a given frequency plan.

Register 0x0253-0x0255 R0 Divider

Reg Address	Bit Field	Type	Name	Description
0x0253	7:0	R/W	R0_REG	24-bit Integer Number. Divide value = (R0_REG+1) x 2 To set R0 = 2, set OUT0_RDIV_FORCE2 = 1, and then the R0_REG value is irrelevant.
0x0254	15:8	R/W	R0_REG	
0x0255	23:16	R/W	R0_REG	

The R dividers are with the output drivers and are even integer dividers. The R1–R3 dividers follow the same format as the R0 divider described above.

Table 34. R Dividers for Output 1,2,3

Register Address	Name	Size	Same as Address
0x0256-0x0258	R1_REG	24-bit Integer Number	0x0253-0x0255
0x025F-0x0261	R2_REG	24-bit Integer Number	0x0253-0x0255
0x0262-0x0264	R3_REG	24-bit Integer Number	0x0253-0x0255

Register 0x026B–0x0272 Design ID

Reg Address	Bit Field	Type	Name	Description
0x026B	7:0	R/W	DESIGN_ID0	ASCII encoded string defined by CBPro user, with user defined space or null padding of unused characters. A user will normally include a configuration ID + revision ID. For example, "ULT.1A" with null character padding sets: DESIGN_ID0: 0x55 DESIGN_ID1: 0x4C DESIGN_ID2: 0x54 DESIGN_ID3: 0x2E DESIGN_ID4: 0x31 DESIGN_ID5: 0x41 DESIGN_ID6: 0x 00 DESIGN_ID7: 0x00
0x026C	15:8	R/W	DESIGN_ID1	
0x026D	23:16	R/W	DESIGN_ID2	
0x026E	31:24	R/W	DESIGN_ID3	
0x026F	39:32	R/W	DESIGN_ID4	
0x0270	47:40	R/W	DESIGN_ID5	
0x0271	55:48	R/W	DESIGN_ID6	
0x0272	63:56	R/W	DESIGN_ID7	

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Register 0x0278-0x027C OPN Identifier

Reg Address	Bit Field	Type	Name	Description
0x0278	7:0	R/W	OPN_ID0	OPN unique identifier. ASCII encoded. For example, with OPN: 5340C-A12345-GM, 12345 is the OPN unique identifier, which sets: OPN_ID0: 0x31 OPN_ID1: 0x32 OPN_ID2: 0x33 OPN_ID3: 0x34 OPN_ID4: 0x35
0x0279	15:8	R/W	OPN_ID1	
0x027A	23:16	R/W	OPN_ID2	
0x027B	31:24	R/W	OPN_ID3	
0x027C	39:32	R/W	OPN_ID4	

Part numbers are of the form:

Si<Part Num Base><Grade>-<Device Revision><OPN ID>-<Temp Grade><Package ID>

Examples:

Si5340C-A12345-GM.

Applies to a “custom” OPN (Ordering Part Number) device. These devices are factory pre-programmed with the frequency plan and all other operating characteristics defined by the user’s ClockBuilder Pro project file.

Si5340C-A-GM.

Applies to a “base” or “blank” OPN device. Base devices are factory pre-programmed to a specific base part type (e.g., Si5340 but **exclude** any user-defined frequency plan or other user-defined operating characteristics selected in ClockBuilder Pro.

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Register 0x027D OPN Revision

Reg Address	Bit Field	Type	Name	Description
0x27D	7:0	R/W	OPN_Revision	ClockBuilder Pro sets this value based upon changes to the NVM for a given OPN.

Register 0x027E Baseline ID

Reg Address	Bit Field	Type	Name	Description
0x27E	7:0	R/W	BaseLine ID	An identifier for the device NVM without the frequency plan programmed into NVM.

Register 0x0302-0x0307 N0 Numerator

Reg Address	Bit Field	Type	Name	Description
0x0302	7:0	R/W	N0_NUM	44-bit Integer Number
0x0303	15:8	R/W	N0_NUM	
0x0304	23:16	R/W	N0_NUM	
0x0305	31:24	R/W	N0_NUM	
0x0306	39:32	R/W	N0_NUM	
0x0307	43:40	R/W	N0_NUM	

The N dividers are interpolative dividers that are used as output dividers that feed into the R dividers. ClockBuilder Pro calculates the correct values for the N-dividers.

Register 0x0308-0x030B N0 Denominator

Reg Address	Bit Field	Type	Name	Description
0x0308	7:0	R/W	N0_DEN	32-bit Integer Number
0x0309	15:8	R/W	N0_DEN	
0x030A	23:16	R/W	N0_DEN	
0x030B	31:24	R/W	N0_DEN	

Table 35. N Dividers for N1, N2, N3

Register Address	Name	Size	Same as Address
0x030D-0x0312	N1_NUM	48-bit Integer Number	0x0302-0x0307
0x0313-0x0316	N1_DEN	32-bit Integer Number	0x0308-0x030B
0x0318-0x031D	N2_NUM	48-bit Integer Number	0x0302-0x0307
0x031E-0x0321	N2_DEN	32-bit Integer Number	0x0308-0x030B
0x0323-0x0328	N3_NUM	48-bit Integer Number	0x0302-0x0307
0x0329-0x032C	N3_DEN	32-bit Integer Number	0x0308-0x030B

Register 0x0339 FINC/FDEC Masks

Reg Address	Bit Field	Type	Name	Description
0x0339	3:0	R/W	N_FSTEP_MSK	0 to enable FINC/FDEC updates 1 to disable FINC/FDEC updates

- Bit 0 corresponds to MultiSynth N0 N_FSTEP_MSK 0x0339[0]
- Bit 1 corresponds to MultiSynth N1 N_FSTEP_MSK 0x0339[1]
- Bit 2 corresponds to MultiSynth N2 N_FSTEP_MSK 0x0339[2]
- Bit 3 corresponds to MultiSynth N3 N_FSTEP_MSK 0x0339[3]

There is one mask bit for each of the four N dividers.

Register 0x033B-0x0340 N0 Frequency Step Word

Reg Address	Bit Field	Type	Name	Description
0x033B	7:0	R/W	N0_FSTEPW	44-bit Integer Number
0x033C	15:8	R/W	N0_FSTEPW	
0x033D	23:16	R/W	N0_FSTEPW	
0x033E	31:24	R/W	N0_FSTEPW	
0x033F	39:32	R/W	N0_FSTEPW	
0x0340	43:40	R/W	N0_FSTEPW	

This is a 44-bit integer value which is directly added (FDEC) or subtracted (FINC) from the Nx_NUM parameter when FINC or FDEC is asserted. ClockBuilder Pro calculates the correct values for the N0 Frequency Step Word. Each N divider has the ability to add or subtract up to a 44-bit value. The Nx_NUM register value does not change when an FINC or FDEC is performed so that the starting point of Nx_NUM is in the Nx_NUM register.

Table 36. Frequency Step Word for N1, N2, N3

Register Address	Name	Size	Same as Address
0x0341-0x0346	N1_FSTEPW	44-bit Integer Number	0x033B-0x0340
0x0347-0x034C	N2_FSTEPW	44-bit Integer Number	0x033B-0x0340
0x034D-0x0352	N3_FSTEPW	44-bit Integer Number	0x033B-0x0340

Register 0x0359–0x035A N0 Delay Control

Reg Address	Bit Field	Type	Name	Description
0x0359	7:0	R/W	N0_DELAY[7:0]	Lower byte of N0_DELAY[15:0]
0x035A	7:0	R/W	N0_DELAY[15:8]	Upper byte of N0_DELAY[15:0]

Register 0x035B–0x035C Divider N1 Delay Control

Reg Address	Bit Field	Type	Name	Description
0x035B	7:0	R/W	N1_DELAY[7:0]	Lower byte of N1_DELAY[15:0]
0x035C	7:0	R/W	N1_DELAY[15:8]	Upper byte of N1_DELAY[15:0]

Register 0x035D–0x035E Divider N2 Delay Control

Reg Address	Bit Field	Type	Name	Description
0x035D	7:0	R/W	N2_DELAY[7:0]	Lower byte of N2_DELAY[15:0]
0x035E	7:0	R/W	N2_DELAY[15:8]	Upper byte of N2_DELAY[15:0]

Register 0x035F–0x0360 Divider N3 Delay Control

Reg Address	Bit Field	Type	Name	Description
0x035F	7:0	R/W	N3_DELAY[7:0]	Lower byte of N3_DELAY[15:0]
0x0360	7:0	R/W	N3_DELAY[15:8]	Upper byte of N3_DELAY[15:0]

Nx_DELAY[15:0] is a 2s complement number that sets the output delay of MultiSynths.

The delay in seconds is $Nx_DELAY / (256 \times F_{VCO})$ where F_{VCO} is the VCO frequency in Hz. The maximum positive and negative delay is $\pm(2^{15}-1)/(256 \times F_{VCO})$. Nx_DELAY values are only applied at power up or during a reset. ClockBuilder Pro calculates the correct value for this register.

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Register 0x090E XAXB Configuration

Reg Address	Bit Field	Type	Name	Description
0x090E	0	R/W	XAXB_EXTCLK_EN	0 to use a crystal at the XAXB pins 1 to use an external clock source at the XAXB pins
0x090E	1	R/W	XAXB_PDNB	0-Power down the oscillator and buffer circuitry at the XA/XB pins 1- No power down

Register 0x091C Enable/Disable Zero Delay Mode

Reg Address	Bit Field	Type	Name	Description
0x091C	2:0	R/W	ZDM_EN	0-2 Reserved 3 Zero Delay Mode Using FB_IN 4 Normal Mode 5-7 Reserved

Register 0x0943 Status and Control I/O Voltage Select

Reg Address	Bit Field	Type	Name	Description
0x0943	0	R/W	IO_VDD_SEL	0 for 1.8 V external connections 1 for 3.3 V external connections

The IO_VDD_SEL configuration bit selects the option of operating the serial interface voltage thresholds from the VDD or the VDDA pin. By default the IO_VDD_SEL bit is set to the VDD option. The serial interface pins are always 3.3 V tolerant even when the device's VDD pin is supplied from a 1.8 V source. When the I²C or SPI host is operating at 3.3 V and the Si5341/40 IO_VDD_SEL = 1.8 V, the host must write the IO_VDD_SEL configuration bit to the VDDA option. This will ensure that both the host and the serial interface are operating at the optimum voltage thresholds. When IO_VDD_SEL = 0, the status outputs will have a VOH of ~1.8V. When IO_VDD_SEL = 1 the status outputs will have a VOH of ~3.3V and the control inputs expect 3.3 V CMOS levels.

Register 0x0949 Clock Input Control and Configuration

Reg Address	Bit Field	Type	Name	Description
0x0949	3:0	R/W	IN_EN	Enables for the four inputs clocks, IN0 through FB_IN. 1 to enable, 0 to disable

- Input 0 corresponds to IN_EN 0x0949 [0]
- Input 1 corresponds to IN_EN 0x0949 [1]
- Input 2 corresponds to IN_EN 0x0949 [2]
- FB_IN corresponds to IN_EN 0x0949 [3]

DOCUMENT CHANGE LIST

Revision 0.2 to Revision 0.3

- Corrected Figure 16, “7-bit I2C Slave Address Bit-Configuration,” on page 34.

CONTACT INFORMATION

Silicon Laboratories Inc.

400 West Cesar Chavez
Austin, TX 78701
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Please visit the Silicon Labs Technical Support web page:
<https://www.silabs.com/support/pages/contacttechnicalsupport.aspx>
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