Intel Agilex® 7 FPGAs and SoCs Device Data Sheet

F-Series and I-Series

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Intel Agilex® 7 FPGAs and SoCs Device Data Sheet: F-Series and I-Series

This data sheet describes the electrical characteristics, switching characteristics, configuration specifications, and timing.

Until the data sheet status for a device reaches Final, the specifications are subject to change at any time and at Intel's discretion.

Table 1. Data Sheet Status for Intel Agilex® 7 FPGAs and SoCs F-Series

Device	Tile	Package	Status
AGF 012/014	E-Tile and P-Tile	R24A	Final
AGF 012/014	E-Tile and P-Tile	R24B	Final
AGF 019/022/023/027	E-Tile and P-Tile	R25A	Final
AGF 006/008	F-Tile	R16A	Advance
AGF 006/008/012/014/019/022/023/027	F-Tile	R24C	Advance
AGF 019/022/023/027	F-Tile	R31C	Advance

Table 2. Data Sheet Status for Intel Agilex® 7 FPGAs and SoCs I-Series

Device	Tile	Package	Status
AGI 019/023	R-Tile and F-Tile	R18A	Preliminary
AGI 022/027	R-Tile and F-Tile	R29A	Preliminary
AGI 022/027	R-Tile and F-Tile	R31A	Advance
AGI 019/022/023/027	F-Tile	R31B	Preliminary

continued...

Device	Tile	Package	Status
AGI 035/040	F-Tile	R39A	Preliminary
AGI 041	R-Tile and F-Tile	R29D	Advance
AGI 041	F-Tile	R31B	Advance

The following descriptors designate the status level currently applicable to the relevant variant:

- Advance: These are target specifications based on simulation.
- Preliminary: These specifications are based on simulation, early validation, and/or early characterization data.
- Final: These are production specifications based on silicon validation and/or characterization.

Table 3. Device Grades, Core Speed Grades, and Power Options Supported

For specification status, see the *Data Sheet Status* table

Device Grade	Speed Grade and Power Option Supported
Extended	–E1V (fastest)
	–E2V
	–E3V
	–E3E
	–E4X
	–E4F
Industrial	–I1V
	–I2V
	–I3V
	–I3E

The suffix after the speed grade denotes the power options offered.

- V—standard power (VID)
- E—lower power (VID)
- X—lowest power (VID)
- F—fixed voltage

Related Information

Package and Thermal Resistance website

Electrical Characteristics

The following sections describe the operating conditions and power consumption.

Operating Conditions

The devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the devices, you must consider the operating requirements described in this section.

Absolute Maximum Ratings

This section defines the maximum operating conditions. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

Caution: Conditions outside the range listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 4. Absolute Maximum Ratings

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Minimum	Maximum	Unit
V_{CC}	Core voltage power supply	—	–0.5	1.14	V
V_{CCP}	Periphery circuitry power supply	—	–0.5	1.14	V

continued...

Symbol	Description	Condition	Minimum	Maximum	Unit
V_{CCPT}	Power supply for I/O PLL and I/O pre-driver	—	–0.5	2.08	V
$V_{CCRCORE}$	CRAM power supply	—	–0.5	1.64	V
V_{CCH}	Transceiver digital power supply	Devices with E-Tile and P-Tile	–0.5	1.21	V
		Devices with R-Tile and F-Tile	–0.5	1.07	V
		Devices with F-Tile only	–0.5	1.07	V
V_{CCH_SDM}	SDM block transceiver digital power sense	Devices with E-Tile and P-Tile	–0.5	1.21	V
		Devices with R-Tile and F-Tile	–0.5	1.21	V
		Devices with F-Tile only	–0.5	1.07	V
$V_{CCIO\_PIO\_SDM}$	SDM block I/O bank power sense of bank 3A	—	–0.5	2.01	V
V_{CCIO_SDM}	SDM block configuration pins power supply	—	–0.5	2.08	V
V_{CCL_SDM}	SDM block core voltage power supply	—	–0.5	1.07	V
$V_{CCFUSEWR\_SDM}$	SDM block fuse writing power supply	—	–0.5	2.4	V
$V_{CCPLLDIG\_SDM}$	SDM block PLL digital power supply	—	–0.5	1.07	V
V_{CCPLL_SDM}	SDM block PLL analog power supply	—	–0.5	2.08	V
V_{CCBAT}	Battery back-up power supply (For design security volatile key register)	—	–0.5	2.08	V
V_{CCADC}	ADC voltage sensor power supply	—	–0.5	2.08	V
V_{CCIO_PIO}	I/O bank power supply	—	–0.5	2.01	V

continued...

Symbol	Description	Condition	Minimum	Maximum	Unit
V_{CCA_PLL}	I/O clock network power supply	—	–0.5	1.64	V
V_{CCRT_GXE}	Transceiver power supply	E-Tile devices	–0.5	1.21	V
$V_{CC\_HSSI\_GXE}$	E-Tile digital signal power supply	E-Tile devices	–0.5	1.21	V
$V_{CCRTPLL\_GXE}$	Transceiver PLL power supply	E-Tile devices	–0.5	1.21	V
V_{CCH_GXE}	Analog power supply	E-Tile devices	–0.5	1.47	V
V_{CCCLK_GXE}	LVPECL REFCLK power supply	E-Tile devices	–0.5	3.41	V
V_{CCRT_GXP}	Transceiver power supply	P-Tile devices	–0.5	1.21	V
$V_{CC\_HSSI\_GXP}$	P-Tile digital signal power supply	P-Tile devices	–0.5	1.21	V
V_{CCFUSE_GXP}	P-Tile efuse power supply	P-Tile devices	–0.5	1.21	V
V_{CCCLK_GXP}	P-Tile I/O buffer power supply	P-Tile devices	–0.5	2.46	V
V_{CCH_GXP}	High voltage power for transceiver	P-Tile devices	–0.5	2.46	V
V_{CCEHT_GXR}	Transceiver analog high voltage power	R-Tile devices	–0.5	2.03	V
V_{CCERT_GXR}	Transceiver analog power supply	R-Tile devices	–0.5	1.33	V
V_{CCED_GXR}	Transceiver digital power supply	R-Tile devices	–0.5	1.21	V
$V_{CCE\_PLL\_GXR}$	PLLs power supply	R-Tile devices	–0.5	1.33	V
$V_{CCE\_DTS\_GXR}$	DTS power supply	R-Tile devices	–0.5	1.33	V
V_{CCCLK_GXR}	Reference clock power supply	R-Tile devices	–0.5	1.34	V
$V_{CCHFUSE\_GXR}$	R-Tile efuse power supply	R-Tile devices	–0.5	1.34	V
$V_{CC\_HSSI\_GXR}$	Digital signal power supply	R-Tile devices	–0.5	1.21	V

continued...

Symbol	Description	Condition	Minimum	Maximum	Unit
$V_{CC\_HSSI\_GXF}$	F-Tile digital signal power supply	F-Tile devices	–0.5	1.07	V
$V_{CCFUSECORE\_GXF}$	F-Tile fuse writing power supply	F-Tile devices	–0.5	1.37	V
$V_{CCFUSEWR\_GXF}$	F-Tile efuse power supply	F-Tile devices	–0.5	1.37	V
V_{CCCLK_GXF}	Reference clock power supply	F-Tile devices	–0.5	2.04	V
$V_{CCERT1\_FHT\_GXF}$	FHT analog core supply 1	F-Tile devices	–0.5	1.33	V
$V_{CCERT2\_FHT\_GXF}$	FHT analog core supply 2	F-Tile devices	–0.5	1.33	V
$V_{CCEHT\_FHT\_GXF}$	FHT high voltage power supply for analog circuit	F-Tile devices	–0.5	1.99	V
$V_{CCERT\_FGT\_GXF}$	FGT analog core supply	F-Tile devices	–0.5	1.34	V
$V_{CCH\_FGT\_GXF}$	FGT analog I/O power supply	F-Tile devices	–0.5	2.04	V
$V_{CCERT\_GXF\_COMBINE}$	Combined analog core supply	F-Tile devices	–0.5	1.33	V
V_{CCL_HPS}	HPS core voltage and periphery circuitry power supply	—	–0.5	1.21	V
$V_{CCPLLDIG\_HPS}$	HPS PLL digital power supply	—	–0.5	1.21	V
V_{CCPLL_HPS}	HPS PLL analog power supply	—	–0.5	2.08	V
V_{CCIO_HPS}	HPS I/O buffers power supply	—	–0.5	2.08	V
V_I	DC input voltage	V_{CCIO_PIO} = 1.2 V	–0.3	1.56	V
		V_{CCIO_PIO} = 1.5 V	0	1.7	V
		V_{CCIO_SDM}, V_{CCIO_HPS} = 1.8 V	–0.3	2.19	V
I_{OUT} (1) (2)	DC output current per pin	V_{CCIO_PIO} = 1.2 V, 1.5 V (3)	–15	15	mA

continued...

Symbol	Description	Condition	Minimum	Maximum	Unit
		V_{CCIO_SDM}, V_{CCIO_HPS} = 1.8 V (4)	–20	20	mA
T_J	Absolute junction temperature	—	–55	125	°C
T_{STG}	Storage temperature	—	–55	150	°C

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage listed in the following tables and undershoot to –1.1 V when using V_{CCIO_HPS}/ V_{CCIO_SDM} of 1.8 V and –0.3 V when using V_{CCIO_PIO} of 1.2 V for input currents less than 100 mA and periods shorter than 20 ns.

No overshooting beyond 1.7 V and undershooting below 0 V is allowed when using V_{CCIO_PIO} = 1.5 V.

The maximum allowed overshoot duration is specified as a percentage of high time (calculated as ([delta T]/T) × 100) over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

(1) Total current per I/O bank must not exceed 100 mA.

(2) Applies to all I/O standards and settings supported by I/O banks, including single-ended and differential I/Os.

(3) The maximum current allowed through any GPIO bank pin when the device is not turned on or during power-up/power-down conditions is 10 mA. Pin voltage during these conditions should not exceed 1.2 V or the V_{CCIO_PIO} supply rail of the bank where the I/O pin resides in, whichever is the lower voltage.

(4) The maximum current allowed through any HPS/SDM pin when the device is not turned on or during power-up/power-down conditions is 10 mA. Pin voltage during these conditions should not exceed V_{CCIO_HPS} or V_{CCIO_SDM} supply rail of the bank where the I/O pin resides in.

Table 5. Maximum Allowed Overshoot During Transitions (for 1.2 V I/O in GPIO Bank)

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Overshoot Duration as % at T_J = 100°C	Unit
V_i (AC)	AC input voltage	V_{CCIO_PIO} + 0.30	100	%
		V_{CCIO_PIO} + 0.35	37	%
		V_{CCIO_PIO} + 0.40	9	%
		V_{CCIO_PIO} + 0.45	3	%
		V_{CCIO_PIO} + 0.50	1	%
		> V_{CCIO_PIO} + 0.50	No overshoot allowed	%

Table 6. Maximum Allowed Overshoot During Transitions (for 1.8 V I/O in HPS and SDM I/O Banks)

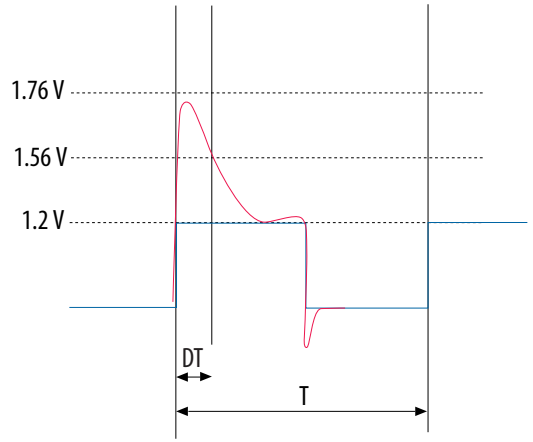
This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Overshoot Duration as % at T_J = 100°C	Unit
V_i (AC)	AC input voltage	V_{CCIO_SDM} + 0.30, V_{CCIO_HPS} + 0.30	100	%
		V_{CCIO_SDM} + 0.35, V_{CCIO_HPS} + 0.35	60	%
		V_{CCIO_SDM} + 0.40, V_{CCIO_HPS} + 0.40	30	%
		V_{CCIO_SDM} + 0.45, V_{CCIO_HPS} + 0.45	20	%
		V_{CCIO_SDM} + 0.50, V_{CCIO_HPS} + 0.50	10	%
		V_{CCIO_SDM} + 0.55, V_{CCIO_HPS} + 0.55	6	%
		>V_{CCIO_SDM} + 0.55, >V_{CCIO_HPS} + 0.55	No overshoot allowed	%

For example, when using 1.2 V I/O standard with 1.26 V V_{CCIO_PIO}, a signal that overshoots to 1.71 V can only be at 1.71 V for ~3% over the lifetime of the device. For an overshoot of 1.56 V, the percentage of high time for the overshoot can be as high as 100% over the lifetime of the device.

Figure 1. Overshoot Duration Example (for 1.2 V GPIO Bank at V_{CCIO_PIO} = 1.26 V)



Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters.

Recommended Operating Conditions

Table 7. Recommended Operating Conditions

This table lists the steady-state voltage values expected. Power supply ramps must all be strictly monotonic, without plateaus.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Minimum[5]	Typical	Maximum[5]	Unit
V_{CC}	Core voltage power supply	SmartVID[6] : –1V, –2V, –3V, –3E, –4X	(Typical) – 3%	0.70 – 0.90[7]	(Typical) + 3%	V
		Fixed voltage: –4F	0.776	0.8	0.824	V
V_{CCP}	Periphery circuitry power supply	SmartVID[6]: –1V, –2V, –3V, –3E, –4X	(Typical) – 3%	0.70 – 0.90[7]	(Typical) + 3%	V
		Fixed voltage: –4F	0.776	0.8	0.824	V
V_{CCPT}	Power supply for I/O PLL and I/O pre-driver	—	1.71	1.8	1.89	V
$V_{CCRCORE}$	CRAM power supply	—	1.14	1.2	1.26	V
V_{CCH}	Advanced interface bus (AIB) power supply	Devices with E-Tile and P-Tile	0.87	0.9	0.93	V
		Devices with R-Tile and F-Tile	0.776	0.8	0.824	V
		Devices with F-Tile only	0.776	0.8	0.824	V
V_{CCH_SDM}	SDM block transceiver digital power sense	Devices with E-Tile and P-Tile	0.87	0.9	0.93	V

continued...

(5) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise.

(6) The use of Power Management Bus (PMBus*) voltage regulator dedicated to SmartVID devices is mandatory. The PMBus voltage regulator and SmartVID devices are connected via PMBus.

(7) The typical value is based on the SmartVID programmed value.

Symbol	Description	Condition	Minimum[5]	Typical	Maximum[5]	Unit
		Devices with R-Tile and F-Tile	0.87	0.9	0.93	V
		Devices with F-Tile only	0.776	0.8	0.824	V
$V_{CCIO\_PIO\_SDM}$ [8]	SDM block I/O bank power sense of Bank 3A	1.5 V	1.455	1.5	1.545	V
		1.2 V	1.14	1.2	1.26	V
V_{CCIO_SDM}	SDM block configuration pins power supply	—	1.71	1.8	1.89	V
V_{CCL_SDM}	SDM block core voltage power supply	—	0.776	0.8	0.824	V
$V_{CCFUSEWR\_SDM}$	SDM block fuse writing power supply	—	1.75	1.8	1.85	V
$V_{CCPLLDIG\_SDM}$	SDM block PLL digital power supply	—	0.776	0.8	0.824	V
V_{CCPLL_SDM}	SDM block PLL analog power supply	—	1.71	1.8	1.89	V
V_{CCBAT} [9]	Battery back-up power supply (For design security volatile key register)	—	1	—	1.8	V

continued...

(5) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise.

(8) Must be powered up with the same voltage level as $V_{CCIO\_PIO\_3A}$. Must be supplied at 1.2 V when using Avalon®-ST ×16/×32 configuration schemes.

(9) Power up V_{CCBAT} with a non-volatile battery power source when using the device security AES BBRAM key. When not using the AES BBRAM key, tie this pin to ground.

Symbol	Description	Condition	Minimum(5)	Typical	Maximum(5)	Unit
I_{BAT} (10)	Battery back-up power supply (For design security volatile key register)	V_{CCBAT} = 1.2 V	—	—	200	nA
V_{CCADC}	ADC voltage sensor power supply	—	1.71	1.8	1.89	V
V_{CCIO_PIO}	I/O bank power supply	1.5 V	1.455	1.5	1.545	V
		1.2 V	1.14	1.2	1.26	V
V_{CCA_PLL}	I/O clock network power supply	—	1.14	1.2	1.26	V
V_I (11)	DC input voltage	V_{CCIO_PIO} = 1.2 V	–0.3	—	V_{CCIO_PIO} + 0.3	V
		V_{CCIO_PIO} = 1.5 V	0	—	1.7	V
		V_{CCIO_SDM} = 1.8 V	–0.3	—	V_{CCIO_SDM} + 0.3	V
		V_{CCIO_HPS} = 1.8 V	–0.3	—	V_{CCIO_HPS} + 0.3	V
V_O	Output voltage	V_{CCIO_PIO} = 1.2 V, 1.5 V	0	—	V_{CCIO_PIO}	V
		V_{CCIO_SDM} = 1.8 V	0	—	V_{CCIO_SDM}	V
		V_{CCIO_HPS} = 1.8 V	0	—	V_{CCIO_HPS}	V
T_J	Operating junction temperature	Extended	0	—	100	°C
		Industrial	–40(12)	—	100	°C
t_{RAMP} (13) (14)	Power supply ramp time	Standard POR	200 µs	—	100 ms	—

(5) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise.

(10) At 25 °C. This supply current specification does not apply to –E4F speed grade and power option device.

(11) This value applies to both input and tri-stated output configuration. Pin voltage should not be externally pulled higher than the maximum value.

E-Tile Transceiver Power Supply Recommended Operating Conditions

Table 8. E-Tile Transceiver Power Supply Recommended Operating Conditions

For specification status, see the *Data Sheet Status* table

Symbol	Description	Typical DC Level (V)	Recommended DC Setpoint (% of $V_{nominal}$)	Recommended VR Ripple (% of $V_{nominal}$)	Recommended AC Transient (% of $V_{nominal}$)	Maximum (DC Setpoint + Ripple + AC Transient) (% of $V_{nominal}$)	Unit
V_{CCRT_GXE} (15)	Transceiver power supply	0.9	± 0.5%	± 2.5%		± 3%	V
$V_{CC\_HSSI\_GXE}$	E-tile digital signal power supply	0.9	± 0.5%	± 2.5%		± 3%	V
$V_{CCRTPLL\_GXE}$ (15)	Transceiver PLL power supply	0.9	± 0.5%	± 2.5%		± 3%	V
V_{CCH_GXE}	Analog power supply	1.1	± 0.5%	± 0.5%	± 2%	± 3%	V
V_{CCCLK_GXE}	LVPECL REFCLK power supply	2.5	± 0.5%	± 0.5%	± 3.5%	± 5%	V

Related Information

AN 910: Intel Agilex 7 Power Distribution Network Design Guidelines
Provides the PCB design guidelines.

(12) E-Tile supports an operating temperature range of –40°C to 100°C. However, the E-Tile transceivers may experience a higher error rate from –40°C to –20°C because of the calibration procedure when starting at a low temperature. Therefore, the recommended operating temperature range for E-Tile protocol-compliant transceiver links is –20°C to 100°C. The maximum temperature ramp rate is 2°C per minute.

(13) t_{RAMP} is the ramp time of each individual power supply, not the ramp time of all combined power supplies.

(14) To support AS fast mode, all power supplies to the device must be fully ramped-up within 10 ms to the recommended operating conditions.

(15) The difference between V_{CCRT}/$V_{CCRTPLL}$ and V_{CCH} should be no less than 200 mV.

P-Tile Transceiver Power Supply Recommended Operating Conditions

Table 9. P-Tile Transceiver Power Supply Recommended Operating Conditions

The specifications below should be met at the board vias directly connected to the package power balls. Place the VR sense point in the FPGA pinfield (in the package shadow), as close as possible to the corresponding package power balls. For these rails, measure the output voltage at this remote sense location.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Typical DC Level (V)	Recommended DC Setpoint (% of $V_{nominal}$)	Recommended VR Ripple (% of $V_{nominal}$)	Recommended AC Transient (% of $V_{nominal}$)	Maximum (DC Setpoint + Ripple + AC Transient) (% of $V_{nominal}$)	Unit
V_{CCRT_GXP}	Transceiver power supply	0.9	± 0.5%	± 2.5%		± 3%	V
$V_{CC\_HSSI\_GXP}$	P-tile digital signal power supply	0.9	± 0.5%	± 2.5%		± 3%	V
V_{CCFUSE_GXP}	P-tile efuse power supply	0.9	± 0.5%	± 2.5%		± 3%	V
V_{CCCLK_GXP} (16)	P-tile I/O buffer power supply	1.8	± 0.5%	± 0.5%	± 2%	± 3%	V
V_{CCH_GXP} (16)	High voltage power for transceiver	1.8	± 0.5%	± 0.5%	± 2%	± 3%	V

Related Information

AN 910: Intel Agilex 7 Power Distribution Network Design Guidelines
Provides the PCB design guidelines.

(16) Follow the more stringent tolerance range for the voltage rails connecting multiple power supplies.

R-Tile Transceiver Power Supply Recommended Operating Conditions

Table 10. R-Tile Transceiver Power Supply Recommended Operating Conditions

For specification status, see the *Data Sheet Status* table

Symbol	Description	Typical DC Level (V)	Recommended DC Setpoint (% of $V_{nominal}$)	Recommended VR Ripple (% of $V_{nominal}$)	Recommended AC Transient (% of $V_{nominal}$)	Maximum (DC Setpoint + Ripple + AC Transient) (% of $V_{nominal}$)	Unit
$V_{CCH\_GXR[L,R]}$ (17)	Transceiver analog high voltage power	1.8	±0.5%	±2%		±2.5%	V
$V_{CCRT\_GXR[L,R]}$	Transceiver analog power supply	1	±0.5%	±2%		±2.5%	V
$V_{CCED\_GXR[L,R]}$	Transceiver digital power supply	0.9	±0.8%	±2.5%		±3.3%	V
$V_{CCE\_PLL\_GXR[L,R]}$	PLLs power supply	1	±0.5%	±1.5%		±2%	V
$V_{CCE\_DTS\_GXR[L,R]}$	DTS power supply	1	±0.5%	±1.5%		±2%	V
$V_{CCCLK\_GXR[L,R]}$ (17)	Reference clock power supply	1	±0.5%	±2.5%		±3%	V
$V_{CCHFUSE\_GXR}$	R-tile efuse power supply	1	±0.5%	±2.5%		±3%	V
$V_{CC\_HSSI\_GXR}$	Digital signal power supply	0.9	±0.8%	±2.5%		±3.3%	V

Related Information

AN 910: Intel Agilex 7 Power Distribution Network Design Guidelines
Provides the PCB design guidelines.

(17) Follow the more stringent tolerance range for the voltage rails connecting multiple power supplies.

F-Tile Transceiver Power Supply Recommended Operating Conditions

Table 11. F-Tile Transceiver Power Supply Recommended Operating Conditions

For specification status, see the *Data Sheet Status* table

Symbol	Description	Typical DC Level (V)	Recommended DC Setpoint (% of $V_{nominal}$)	Recommended VR Ripple (% of $V_{nominal}$)	Recommended AC Transient (% of $V_{nominal}$)	Maximum (DC Setpoint + Ripple + AC Transient) (% of $V_{nominal}$)	Unit
$V_{CC\_HSSI\_GXF}$	F-tile digital signal power supply	0.8	±0.5%	±0.5%	±2.5%	±3%	V
$V_{CCFUSECORE\_GXF}$	F-tile fuse writing power supply	1	±0.5%	±4.5%		±5%	V
$V_{CCFUSEWR\_GXF}$	F-tile efuse power supply	1	±0.5%	±4.5%		±5%	V
V_{CCCLK_GXF}	Reference clock power supply	1.8	±0.5%	±0.5%	±2%	±3%	V
$V_{CCERT1\_FHT\_GXF}$ (18)	FHT analog core supply 1	1	±0.5%	±0.5%	±1.5%	±2.5%	V
$V_{CCERT2\_FHT\_GXF}$ (19)	FHT analog core supply 2	1	±0.5%	±0.5%	±1.5%	±2.5%	V
$V_{CCEHT\_FHT\_GXF}$ (20)	FHT high voltage power supply for analog circuit	1.5	±0.5%	±0.5%	+1%/–1.5%	+2%/–2.5%	V
$V_{CCERT\_FGT\_GXF}$ (21)	FGT analog core supply alone	1	±0.5%	±0.5%	±1.5%	±3%	V
	FGT analog core supply when combined with	1	±0.5%	±0.5%	±1.5%	±2.5%	V

continued...

(18) HF noise requires AC 10 mVpp above 1 MHz; switching regulator ripple switching frequency: <500 kHz, ripple: ≤5 mVpp.

(19) HF noise requires AC 30 mVpp above 1 MHz; switching regulator ripple switching frequency: <500 kHz, ripple: ≤5 mVpp.

(20) HF noise requires AC 30 mVpp above 1 MHz; switching regulator ripple switching frequency: <500 kHz, ripple: ≤7 mVpp.

(21) HF noise requires AC 30 mVpp above 1 MHz; switching regulator ripple: ≤5mVpp.

Symbol	Description	Typical DC Level (V)	Recommended DC Setpoint (% of $V_{nominal}$)	Recommended VR Ripple (% of $V_{nominal}$)	Recommended AC Transient (% of $V_{nominal}$)	Maximum (DC Setpoint + Ripple + AC Transient) (% of $V_{nominal}$)	Unit
	$V_{CCERT1\_FHT\_GX}$ and $V_{CCERT2\_FHT\_GXF}$ 1 V supply						
$V_{CCH\_FGT\_GXF}$ (21)	FGT analog I/O power supply	1.8	±0.5%	≤5 mV	±1.5%	±3%	V

Related Information

AN 910: Intel Agilex 7 Power Distribution Network Design Guidelines
Provides the PCB design guidelines.

HPS Power Supply Recommended Operating Conditions

Table 12. HPS Power Supply Recommended Operating Conditions

This table lists the steady-state voltage and current values expected for system-on-a-chip (SoC) devices with ARM-based hard processor system (HPS). Power supply ramps must all be strictly monotonic, without plateaus. Refer to the *Recommended Operating Conditions* table for the steady-state voltage values expected from the FPGA portion of the SoC devices.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CCL_HPS}	HPS core voltage and periphery circuitry power supply	Performance boost, fixed voltage: –1V	(Typical) – 3%	0.95	(Typical) + 3%	V
		SmartVID: –1V, –2V, –3V, –3E (22)	(Typical) – 3%	0.70 – 0.90	(Typical) + 3%	V
		Fixed voltage: –4F, –4X	0.776	0.8	0.824	V
$V_{CCPLLDIG\_HPS}$	HPS PLL digital power supply (can be connected to V_{CCL_HPS})	Performance boost, fixed voltage: –1V	(Typical) – 3%	0.95	(Typical) + 3%	V

continued...

(22) The use of Power Management Bus (PMBus) voltage regulator dedicated to SmartVID devices is mandatory. The PMBus voltage regulator and SmartVID devices are connected via PMBus.

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
		SmartVID: –1V, –2V, –3V, –3E (22)	(Typical) – 3%	0.70 – 0.90	(Typical) + 3%	V
		Fixed voltage: –4F, –4X	0.776	0.8	0.824	V
V_{CCPLL_HPS}	HPS PLL analog power supply	1.8 V	1.71	1.8	1.89	V
V_{CCIO_HPS}	HPS I/O buffers power supply	1.8 V	1.71	1.8	1.89	V

Related Information

- Recommended Operating Conditions on page 12
  Provides the steady-state voltage values for the FPGA portion of the device.
- HPS Clock Performance on page 79

DC Characteristics

Supply Current and Power Consumption

Intel® offers two ways to estimate power for your design—the Intel FPGA Power and Thermal Calculator (PTC) and the Intel Quartus® Prime Power Analyzer feature.

Use the PTC before you start your design to estimate the supply current for your design. The PTC provides a magnitude estimate of the device power because these currents vary greatly with the usage of the resources.

The Intel Quartus Prime Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yield very accurate power estimates.

I/O Pin Leakage Current

Table 13. I/O Pin Leakage Current (for GPIO Bank)

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Min	Max	Unit
I_I	Input pin	V_I = 0 V to $V_{CCIO\_PIO\ (MAX)}$	–360	360	µA
I_{OZ}	Tri-stated I/O pin	V_O = 0 V to $V_{CCIO\_PIO\ (MAX)}$	–360	360	µA

Table 14. I/O Pin Leakage Current (for HPS and SDM I/O Banks)

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Min	Max	Unit
I_I	Input or tri-stated I/O pin	V_I, V_O = 0 V	0.015	6	µA
		V_I, V_O = $V_{CCIO\_HPS\ (MAX)}$, $V_{CCIO\_SDM\ (MAX)}$	0.01	1	µA

Bus Hold Specifications

The bus-hold trip points are based on calculated input voltages from the JEDEC* standard.

Table 15. Bus Hold Parameters (for GPIO Bank)

For specification status, see the *Data Sheet Status* table

Parameter	Symbol	Condition	V_{CCIO_PIO} (V)		Unit
			1.2		
			Min	Max	
Bus-hold, low, sustaining current	I_{SUSL}	$V_{IN} > V_{IL}$ (max)	50	—	µA
Bus-hold, high, sustaining current	I_{SUSH}	$V_{IN} < V_{IH}$ (min)	–50	—	µA

continued...

Parameter	Symbol	Condition	V_{CCIO_PIO} (V)		Unit
			1.2		
			Min	Max	
Bus-hold, low, overdrive current	I_{ODL}	0 V < V_{IN} < V_{CCIO_PIO}	—	1,400	µA
Bus-hold, high, overdrive current	I_{ODH}	0 V < V_{IN} < V_{CCIO_PIO}	—	–1,400	µA
Bus-hold trip point	V_{TRIP}	—	0.33 × V_{CCIO_PIO}	0.67 × V_{CCIO_PIO}	V

OCT Calibration Accuracy Specifications

If you enable on-chip termination (OCT) calibration, calibration is automatically performed at power up for I/Os connected to the calibration block.

Table 16. OCT Calibration Accuracy Specifications (for GPIO Bank)

Calibration accuracy for the calibrated on-chip series termination (R_S OCT) and on-chip parallel termination (R_T OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

These specifications require RZQ reference accuracy of 240 Ω ±1%.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Calibration Accuracy	Unit
34-Ω and 40-Ω R_S	Internal series termination with calibration (34-Ω and 40-Ω setting)	V_{CCIO_PIO} = 1.2	±20	%
50-Ω and 60-Ω R_T	Internal parallel termination with calibration (50-Ω and 60-Ω setting)	SSTL-12 and HSTL-12 I/O standards	–10 to +60	%
		POD12 I/O standard	±15	%

OCT Without Calibration Resistance Tolerance Specifications

Table 17. OCT Without Calibration Resistance Tolerance Specifications (for GPIO Bank)

This table lists the GPIO OCT without calibration resistance tolerance to PVT changes.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Calibration Accuracy	Unit
34-Ω and 40-Ω R_S	Internal series termination without calibration (34-Ω and 40-Ω setting)	V_{CCIO_PIO} = 1.2	–30 to +60	%
100-Ω R_D	Internal differential termination (100-Ω setting)	V_{CCIO_PIO} = 1.5	±40	%
		V_{CCIO_PIO} = 1.2	±40	%

Pin Capacitance

Table 18. Pin Capacitance (for GPIO Bank)

For specification status, see the *Data Sheet Status* table

Symbol	Description	Maximum	Unit
C_{IO}	Input/output capacitance of I/O pins	2.6[23]	pF

Internal Weak Pull-Up Resistor

All I/O pins in GPIO bank have an option to enable weak pull-up when using 1.2 V LVCMOS I/O standard. For SDM and HPS, the configuration I/O and peripheral I/O are supported with weak pull-up and weak pull-down options.

Table 19. Internal Weak Pull-Up Resistor Values (for GPIO Bank)

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Min	Typ	Max	Unit
R_{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well	V_{CCIO_PIO} = 1.2 ±5%	0.5	2.5	15	kΩ

(23) This value refers to die-level pin capacitance without the device package.

Symbol	Description	Condition (V)	Min	Typ	Max	Unit
	as user mode if you have enabled the programmable pull-up resistor option.					

Table 20. Internal Weak Pull-Up and Weak Pull-Down Resistor Values (for HPS and SDM I/O Banks)

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition (V)	Min	Typ	Max	Unit
20 kΩ R_{PU}, 20 kΩ R_{PD}	Value of the I/O pin pull-up and pull-down resistor during user mode if you have enabled the programmable pull-up or pull-down resistor option.	V_{CCIO_SDM} = 1.8 ±5%, V_{CCIO_HPS} = 1.8 ±5%	15	20	25	kΩ
50 kΩ R_{PU}, 50 kΩ R_{PD}	Value of the I/O pin pull-up and pull-down resistor during user mode if you have enabled the programmable pull-up or pull-down resistor option.	V_{CCIO_SDM} = 1.8 ±5%, V_{CCIO_HPS} = 1.8 ±5%	37.5	50	62.5	kΩ
80 kΩ R_{PU}, 80 kΩ R_{PD}	Value of the I/O pin pull-up and pull-down resistor during user mode if you have enabled the programmable pull-up or pull-down resistor option.	V_{CCIO_SDM} = 1.8 ±5%, V_{CCIO_HPS} = 1.8 ±5%	60	80	100	kΩ

Related Information

Intel Agilex 7 Device Family Pin Connection Guidelines: F-Series and I-Series
Provides more information about the pins that support internal weak pull-up and internal weak pull-down features.

Hysteresis Specifications for Schmitt Trigger Input

Table 21. Hysteresis Specifications for Schmitt Trigger Input (for HPS I/O Bank)

The devices support Schmitt trigger input on HPS I/O bank. A Schmitt trigger feature introduces hysteresis to the input signal for improved noise immunity, especially for signal with slow edge rate.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Condition	Min	Typ	Max	Unit
V_{HYS}	Hysteresis for Schmitt trigger input	V_{CCIO_HPS} = 1.8 V	180	250	350	mV

I/O Standard Specifications

Tables in this section list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported.

For minimum voltage values, use the minimum V_{CCIO_PIO} values. For maximum voltage values, use the maximum V_{CCIO_PIO} values.

You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.

Related Information

Recommended Operating Conditions on page 12

Single-Ended I/O Standards Specifications

Table 22. Single-Ended I/O Standards Specifications (for GPIO Bank)

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_PIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)[24]	V_{OH} (V)[24]
	Min	Typ	Max	Min	Max	Min	Max	Max	Min
1.2 V LVCMOS	1.14	1.2	1.26	–0.3	0.35 × V_{CCIO_PIO}	0.65 × V_{CCIO_PIO}	V_{CCIO_PIO} + 0.3	0.25 × V_{CCIO_PIO}	0.75 × V_{CCIO_PIO}

(24) Applicable to test condition of I_{OH} and I_{OL} at 2 mA.

Table 23. Single-Ended I/O Standards Specifications (for HPS and SDM I/O Banks)

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_HPS}, V_{CCIO_SDM} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)(25)	I_{OH} (mA)(25)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min	Max	Min
1.8 V LVCMOS	1.71	1.8	1.89	–0.3	0.35 × V_{CCIO_HPS}, 0.35 × V_{CCIO_SDM}	0.65 × V_{CCIO_HPS}, 0.65 × V_{CCIO_SDM}	V_{CCIO_HPS} + 0.3, V_{CCIO_SDM} + 0.3	0.4	V_{CCIO_HPS} – 0.4, V_{CCIO_SDM} – 0.4	8	–8

Single-Ended SSTL, HSTL, HSUL, and POD I/O Reference Voltage Specifications

Table 24. Single-Ended SSTL, HSTL, HSUL, and POD I/O Reference Voltage Specifications (for GPIO Bank)

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_PIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-12	1.14	1.2	1.26	0.49 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO}	0.51 × V_{CCIO_PIO}	0.475 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO}	0.525 × V_{CCIO_PIO}
HSTL-12	1.14	1.2	1.26	0.47 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO}	0.53 × V_{CCIO_PIO}	0.475 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO}	0.525 × V_{CCIO_PIO}
HSUL-12	1.14	1.2	1.26	0.49 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO}	0.51 × V_{CCIO_PIO}	—	—	—
POD12	1.14	1.2	1.26	—	Internally calibrated	—	—	V_{CCIO_PIO}	—

(25) To meet the I_{OH} and I_{OL} specifications, you must set the current strength settings accordingly. For example, to meet the 1.8 V LVCMOS specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OH} and I_{OL} specifications in the data sheet.

Single-Ended SSTL, HSTL, HSUL, and POD I/O Standards Signal Specifications

Table 25. Single-Ended SSTL, HSTL, HSUL, and POD I/O Standards Signal Specifications (for GPIO Bank)

For specification status, see the *Data Sheet Status* table

I/O Standard	$V_{IL(DC)}$ (V)	$V_{IH(DC)}$ (V)	$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)
	Max	Min	Max	Min
SSTL-12	V_{REF} – 0.075	V_{REF} + 0.075	V_{REF} – 0.100	V_{REF} + 0.100
HSTL-12	V_{REF} – 0.080	V_{REF} + 0.080	V_{REF} – 0.150	V_{REF} + 0.150
HSUL-12	V_{REF} – 0.100	V_{REF} + 0.100	V_{REF} – 0.135	V_{REF} + 0.135
POD12[26]	V_{REF} – 0.055	V_{REF} + 0.055	V_{REF} – 0.070	V_{REF} + 0.070

Note: For output voltage swing calculation example, refer to the related information.

Related Information

1.2 V I/O Interface Voltage Level Compatibility section, Intel Agilex 7 General-Purpose I/O User Guide: F-Series and I-Series
Provides output voltage swing calculation examples.

[26] This specification is defined over internal V_{ref} range from 0.6 × V_{CCIO_PIO} to 0.92 × V_{CCIO_PIO}.

Differential SSTL, HSTL, and HSUL I/O Standards Specifications

Table 26. Differential SSTL, HSTL, and HSUL I/O Standards Specifications (for GPIO Bank)

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_PIO} (V)			$V_{ILdiff(DC)}$ (V)	$V_{IHdiff(DC)}$ (V)	$V_{ILdiff(AC)}$ (V)	$V_{IHdiff(AC)}$ (V)	$V_{IX(AC)}$ (V)			$V_{OX(AC)}$ (V)		
	Min	Typ	Max	Max	Min	Max	Min	Min	Typ	Max	Min	Typ	Max
SSTL-12	1.14	1.2	1.26	–0.15	0.15	–0.2	0.2	0.5 × V_{CCIO_PIO} – 0.12	0.5 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO} + 0.12	0.5 × V_{CCIO_PIO} – 0.12	0.5 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO} + 0.12
HSTL-12	1.14	1.2	1.26	–0.16	0.16	–0.3	0.3	0.5 × V_{CCIO_PIO} – 0.12	0.5 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO} + 0.12	0.5 × V_{CCIO_PIO} – 0.12	0.5 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO} + 0.12
HSUL-12	1.14	1.2	1.26	–0.2	0.2	–0.27	0.27	0.5 × V_{CCIO_PIO} – 0.12	0.5 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO} + 0.12	0.5 × V_{CCIO_PIO} – 0.12	0.5 × V_{CCIO_PIO}	0.5 × V_{CCIO_PIO} + 0.12

Related Information

1.2 V I/O Interface Voltage Level Compatibility section, Intel Agilex 7 General-Purpose I/O User Guide: F-Series and I-Series
Provides output voltage swing calculation examples.

Differential POD I/O Standards Specifications

Table 27. Differential POD I/O Standards Specifications (for GPIO Bank)

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_PIO} (V)			$V_{ILdiff(DC)}$ (V)	$V_{IHdiff(DC)}$ (V)	$V_{ILdiff(AC)}$ (V)	$V_{IHdiff(AC)}$ (V)	$V_{IX(AC)}$ (%)[27]
	Min	Typ	Max	Max	Min	Max	Min	Max
POD12	1.14	1.2	1.26	–0.11	0.11	–0.14	0.14	25

Related Information

1.2 V I/O Interface Voltage Level Compatibility section, Intel Agilex 7 General-Purpose I/O User Guide: F-Series and I-Series
Provides output voltage swing calculation examples.

(27) Percentage of P-leg and N-leg crossing relative to the midpoint of P-leg and N-leg signal swings.

Differential I/O Standards Specifications

Table 28. Differential I/O Standards Specifications (for GPIO Bank)

For specification status, see the *Data Sheet Status* table

I/O Standard	V_{CCIO_PIO} (V)			V_{ID} (mV)		$V_{ICM(DC)}$ (V)			V_{OD} (V)[28] [29]			V_{OCM} (V)[28]		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
True Differential Signaling (Transmitter & Receiver)[30]	1.455	1.5	1.545	200	600	0.3	Data rate ≤700 Mbps	<0.9	0.247	—	0.454	0.99	1.1	1.21
				100	600	0.9		1.4						
				100	600	0.9	Data rate >700 Mbps	1.4						
True Differential Signaling (Receiver only)[30]	1.14	1.2	1.26	200	600	0.3	Data rate ≤700 Mbps	<0.9	—	—	—	—	—	—
				100	600	0.9		1.1						
				100	600	0.9	Data rate >700 Mbps	1.1						

Switching Characteristics

This section provides the performance characteristics of core and periphery blocks.

(28) R_L range: $90 \leq R_L \leq 110\ \Omega$.

(29) The specification is only applicable to default V_{OD} and pre-emphasis setting.

(30) The True Differential Signaling input buffer is supported on 1.2 V and 1.5 V V_{CCIO_PIO} bank. The maximum input voltage driven into the True Differential Signaling input buffer must not exceed $V_{ICM(max)} + V_{ID(max)}/2$.

Core Performance Specifications

Clock Tree Specifications

Table 29. Clock Tree Performance

For specification status, see the *Data Sheet Status* table

Parameter	Performance		Unit
	–1V, –2V	–3V, –3E, –4F, –4X	
Programmable clock routing	1,000	780	MHz

I/O PLL Specifications

Table 30. I/O PLL Specifications

For specification status, see the *Data Sheet Status* table

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	–1V	10	—	1,100(31)	MHz
		–2V	10	—	900(31)	MHz
		–3V, –3E	10	—	750(31)	MHz
		–4F, –4X	10	—	650(31)	MHz
f_{INPFD}	Input clock frequency to the PFD	—	10	—	325	MHz
f_{VCO}	I/O PLL VCO operating range	–1V	600	—	1,600	MHz
		–2V	600	—	1,434	MHz
		–3V, –3E	600	—	1,250	MHz
		–4F, –4X	600	—	1,067	MHz

continued...

(31) This specification is limited by the I/O maximum frequency. The maximum achievable I/O frequency is different for each I/O standard and is dependent on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{CLBW}	I/O PLL closed-loop bandwidth	I/O bank I/O PLL	0.5	—	10	MHz
		Fabric-feeding I/O PLL	1	—	10	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	—	40	—	60	%
f_{OUT}	Output frequency for internal clock (C counter)	–1V	—	—	1,100	MHz
		–2V	—	—	900	MHz
		–3V, –3E	—	—	750	MHz
		–4F, –4X	—	—	650	MHz
f_{OUT_EXT}	Output frequency for external clock output	–1V	—	—	800	MHz
		–2V	—	—	717	MHz
		–3V, –3E	—	—	625	MHz
		–4F, –4X	—	—	500	MHz
$t_{OUTDUTY}$	Duty cycle for dedicated external clock output (when set to 50%)	f_{OUT_EXT} < 300 MHz	45	50	55	%
		f_{OUT_EXT} ≥ 300 MHz	40/45 (32)	50	55 (32)/60	%
t_{FCOMP} (33)	External feedback clock compensation time	—	—	—	5	ns
$f_{DYCONFIGCLK}$	Dynamic configuration clock for mgmt_clk	—	—	—	100	MHz
t_{LOCK}	Time required to lock from end-of-device configuration or deassertion of areset	—	—	—	1	ms

continued...

(32) To achieve 5% duty cycle for f_{OUT_EXT} ≥ 300 MHz, you only can use `tx_outclk` port from the LVDS SERDES Intel FPGA IP. Refer to the related information for the detail design guidelines.

(33) Not applicable for fabric-feeding I/O PLL.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/ delays)	—	—	—	1	ms
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	—	±50	ps
t_{ARESET}	Minimum pulse width on the areset signal	—	10	—	—	ns
t_{INCCJ}	Input clock cycle-to-cyle jitter	f_{REF} < 100 MHz (34)	—	—	750	ps (p-p)
		f_{REF} ≥ 100 MHz (34)	—	—	0.15	UI (p-p)
t_{REFPJ}	Reference phase jitter (rms)(35)	Carrier frequency: 100 MHz with integrated bandwidth of 10 kHz to 50 MHz	—	—	1.42	ps
t_{REFPN}	Reference phase noise(36) (35)	10 Hz	—	—	–90	dBc/Hz
		100 Hz	—	—	–100	dBc/Hz
		1 kHz	—	—	–110	dBc/Hz
		10 kHz	—	—	–120	dBc/Hz
		100 kHz	—	—	–130	dBc/Hz
		1 MHz	—	—	–138	dBc/Hz
		10 MHz	—	—	–142	dBc/Hz

continued...

(34) f_{REF} is f_{IN}/N, specification applies when N = 1.

(35) Requirement for Advanced Interface Bus (AIB), High Bandwidth Memory (HBM) Interface, Mobile Industry Processor Interface (MIPI), DDR4 protocol, and LVDS applications only.

(36) The phase noise numbers in the table above are the maximum acceptable phase noise values measured at a carrier frequency of 100 MHz. To calculate the phase noise requirement at any other frequency, use the formula: REFCLK phase noise at f (MHz) = REFCLK phase noise at 100 MHz + (20 × log10 (f/100)).

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		100 MHz	—	—	–144	dBc/Hz
t_{OUTPJ_DC} (33) (37)	Period jitter for dedicated clock output	f_{OUT} < 100 MHz (34)	—	—	17.5	mUI (p-p)
		f_{OUT} ≥ 100 MHz (34)	—	—	175	ps (p-p)
t_{OUTCCJ_DC} (33) (37)	Cycle-to-cycle jitter for dedicated clock output	f_{OUT} < 100 MHz (34)	—	—	17.5	mUI (p-p)
		f_{OUT} ≥ 100 MHz (34)	—	—	175	ps (p-p)
t_{OUTPJ_IO} (38) (37)	Period jitter for clock output on the regular I/O	f_{OUT} < 100 MHz (34)	—	—	60	mUI (p-p)
		f_{OUT} ≥ 100 MHz (34)	—	—	600	ps (p-p)
t_{OUTCCJ_IO} (38) (37)	Cycle-to-cycle jitter for clock output on the regular I/O	f_{OUT} < 100 MHz (34)	—	—	60	mUI (p-p)
		f_{OUT} ≥ 100 MHz (34)	—	—	600	ps (p-p)
$t_{CASC\_OUTPJ\_DC}$ (33)	Period jitter for dedicated clock output in cascaded PLLs	f_{OUT} < 100 MHz (34)	—	—	17.5	mUI (p-p)
		f_{OUT} ≥ 100 MHz (34)	—	—	175	ps (p-p)

Related Information

- Memory Output Clock Jitter Specifications on page 48
  Provides more information about the external memory interface clock output jitter specifications.
- Intel Agilex 7 Clocking and PLL User Guide: F-Series and I-Series
  Provides the recommended spread-spectrum clock profile and design guidelines to achieve 5% duty cycle using the LVDS SERDES Intel FPGA IP.

(37) This jitter specification does not include the effect of spread-spectrum clock. The magnitude of jitter deterioration is largely depend on the spread-spectrum clock profile used. Refer to the related information for the recommended spread-spectrum clock profile.

(38) External memory interface clock output jitter specifications use a different measurement method, which are available in the *Memory Output Clock Jitter Specifications* table.

DSP Block Specifications

Table 31. DSP Block Performance Specifications

For specification status, see the *Data Sheet Status* table

Mode	Performance				Unit
	–1V	–2V	–3V, –3E	–4F, –4X	
Fixed-point 18 × 19 multiplication mode	900	771	676	600	MHz
Fixed-point 27 × 27 multiplication mode(39)	900	771	676	600	MHz
Fixed-point 18 × 19 multiplier adder mode(39)	900	771	676	600	MHz
Fixed-point 18 × 19 multiplier adder summed with 36-bit input mode(39)	900	771	676	600	MHz
Fixed-point four 9 × 9 multiplier adder mode(39)	900	771	676	600	MHz
Fixed-point 18 × 19 systolic mode	900	771	676	600	MHz
Fixed-point 18 × 19 complex multiplication mode	900	771	676	600	MHz
FP32 floating-point multiplication mode	750	579	507	475	MHz
FP32 floating-point adder or subtract mode	750	579	507	475	MHz

continued...

(39) When Chainout is enabled but systolic registers are not used, the performance specifications for the following speed grades are as follows:

- –1V: 675 MHz
- –2V: 578 MHz
- –3V and –3E: 507 MHz
- –4F and –4X: 450 MHz

Mode	Performance				Unit
	–1V	–2V	–3V, –3E	–4F, –4X	
FP32 floating-point multiplier adder or subtract mode	750	579	507	475	MHz
FP32 floating-point multiplier accumulate mode	750	579	507	475	MHz
Addition or subtraction of two FP16 floating-point multiplication mode	750	579	507	475	MHz
Sum/sub of two FP16 multiplications with FP32 (addition/subtraction)	750	579	507	475	MHz
Sum/sub of two FP16 multiplications with accumulation (addition/ subtraction)	750	579	507	475	MHz
FP32 floating-point complex multiplication	750	579	507	475	MHz
FP32 floating-point vector dot product	750	579	507	475	MHz
FP16 floating-point complex multiplication	750	579	507	475	MHz
FP16 floating-point vector dot product	750	579	507	475	MHz

Memory Block Specifications

To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL and set to 50% output duty cycle. Use the Intel Quartus Prime software to report timing for the memory block clocking schemes.

When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in f_{MAX}.

Table 32. Memory Block Performance Specifications

For specification status, see the *Data Sheet Status* table

Memory	Mode	Performance				Unit
		–1V	–2V	–3V, –3E	–4F, –4X	
MLAB	Single-port RAM/ROM Simple dual-port RAM	1,000	782	667	600	MHz
	Simple dual-port RAM with read-during-write option	630	510	460	330	MHz
M20K Block[40]	Single-port RAM/ROM Simple dual-port RAM	1,000 (HS) 850 (LP)	782 (HS) 664 (LP)	667 (HS) 567 (LP)	600 (HS) 510 (LP)	MHz
	Simple dual-port RAM, coherent read enabled	1,000 (HS) 850 (LP)	782 (HS) 664 (LP)	667 (HS) 567 (LP)	600 (HS) 510 (LP)	MHz
	Single-port RAM with the read-during-write option set to Old Data Simple dual-port RAM with the read-during-write option set to Old Data	800 (HS) 680 (LP)	640 (HS) 540 (LP)	560 (HS) 476 (LP)	480 (HS) 410 (LP)	MHz
	Simple dual-port RAM with ECC enabled, 512 × 32	600 (HS) 500 (LP)	480 (HS) 400 (LP)	420 (HS) 357 (LP)	360 (HS) 300 (LP)	MHz
	Simple dual-port RAM with ECC, optional pipeline registers enabled, 512 × 32	1,000 (HS) 850 (LP)	782 (HS) 664 (LP)	667 (HS) 567 (LP)	600 (HS) 510 (LP)	MHz
	Dual-port ROM True dual-port RAM	600 (HS)	500 (HS)	420 (HS)	360 (HS)	MHz
	Simple quad-port RAM	600 (HS)	500 (HS)	420 (HS)	360 (HS)	MHz
eSRAM	Simple dual-port	750	640	500	500	MHz

(40) For M20K block, timing/power optimization feature is available. The available options are High Speed (HS) and Low Power (LP). For details on this timing/power optimization feature, refer to the related information.

Related Information

Intel Agilex 7 Embedded Memory User Guide
Provides details on M20K block timing/power optimization feature.

Local Temperature Sensor Specifications

Table 33. Local Temperature Sensor Specifications

For specification status, see the *Data Sheet Status* table

Description	Temperature Range	Accuracy	Sampling Rate(41)	Conversion Time
Local Temperature Sensor	–40 to 125°C(42)	±5°C	1 KSPS	< 1 ms

Remote Temperature Diode Specifications

Note the following for the remote temperature diode specifications:

- The temperature diode characteristics in this table target for three-currents temperature sensing chip implementation. The characteristics can also apply to two-currents temperature sensing chip implementation.
- Absolute accuracy is dependent on third-party external diode ADC and integration specifics.

Table 34. Remote Temperature Diode Specifications (Core Fabric TSD)

For specification status, see the *Data Sheet Status* table

Description	Min	Typ	Max	Unit
I_{bias}, diode source current	10	—	170	µA
V_{bias}, voltage across diode	0.43	—	0.75	V
Series resistance	—	—	<3	Ω
Diode ideality factor	—	1.006(43)	—	—

(41) The read out is subject to the SDM mailbox activity status.

(42) Temperature range refers to junction temperature.

(43) When using lower injection current (two-currents) implementation, the ideality factor is 1.009.

Table 35. Remote Temperature Diode Specifications (E-Tile TSD)

For specification status, see the *Data Sheet Status* table

Description	Min	Typ	Max	Unit
I_{bias}, diode source current	10	—	170	µA
V_{bias}, voltage across diode	0.56	—	0.82	V
Series resistance	—	—	<2	Ω
Diode ideality factor	—	1.005	—	—

Table 36. Remote Temperature Diode Specifications (P-Tile TSD)

For specification status, see the *Data Sheet Status* table

Description	Min	Typ	Max	Unit
I_{bias}, diode source current	10	—	170	µA
V_{bias}, voltage across diode	0.56	—	0.87	V
Series resistance	—	—	<10	Ω
Diode ideality factor	—	1.0108(44)	—	—

Table 37. Remote Temperature Diode Specifications (R-Tile TSD)

For specification status, see the *Data Sheet Status* table

Description	Min	Typ	Max	Unit
I_{bias}, diode source current	20	—	170	µA
V_{bias}, voltage across diode	0.5	—	0.78	V
Series resistance	—	—	<10	Ω
Diode ideality factor	—	1.000(45)	—	—

(44) When using lower injection current (two-currents) implementation, the ideality factor is 1.03.

(45) When using lower injection current (two-currents) implementation, the ideality factor is 1.008.

Table 38. Remote Temperature Diode Specifications (F-Tile TSD)

For specification status, see the *Data Sheet Status* table

Description	Min	Typ	Max	Unit
I_{bias}, diode source current	20	—	170	µA
V_{bias}, voltage across diode	0.5	—	0.78	V
Series resistance	—	—	<10	Ω
Diode ideality factor	—	1.002(46)	—	—

Voltage Sensor Specifications

Table 39. Voltage Sensor Specifications

For specification status, see the *Data Sheet Status* table

Parameter		Minimum	Typical	Maximum	Unit
Resolution		—	7	—	Bit
Sampling rate(47)		—	—	1	KSPS
Input capacitance		—	—	40	pF
Voltage sensor accuracy, V_{in} range: 0 V to 1.1 V(48)		—	—	±3.5	%
Unipolar Input Mode	Input signal range for Vsigp	—	—	1.35	V
	Common mode voltage on Vsign	—	—	0.25	V
	Input signal range for Vsigp – Vsign	—	—	1.1	V

(46) When using lower injection current (two-currents) implementation, the ideality factor is 1.016.

(47) The read out is subject to the SDM mailbox activity status.

(48) For 1.8 V channel 3, 4, 5, and 9, the accuracy is ±4.5%.

Periphery Performance Specifications

This section describes the periphery performance, LVDS SERDES, and external memory interface.

Actual achievable frequency depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

LVDS SERDES Specifications

Table 40. LVDS SERDES Specifications

LVDS serializer/deserializer (SERDES) block supports SERDES factor J = 3 to 10.

DDR registers support SERDES factor J = 1 to 2.

You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.

For specification status, see the *Data Sheet Status* table

Parameter	Symbol	Condition	–1 Speed Grade			–2 Speed Grade			–3 Speed Grade			–4 Speed Grade			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Clock frequency	f_{HSCLK_in} (input clock frequency) True Differential I/O Standards	Clock boost factor W = 1 to 40[49]	10	—	800	10	—	700	10	—	625	10	—	625	MHz
	f_{HSCLK_in} (input clock frequency) Single-Ended	Clock boost factor W = 1 to 40[49]	10	—	625	10	—	625	10	—	525	10	—	525	MHz

continued...

[49] Clock Boost Factor (W) is the ratio between the input data rate and the input clock rate.

Parameter	Symbol	Condition	–1 Speed Grade			–2 Speed Grade			–3 Speed Grade			–4 Speed Grade			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	I/O Standards														
	f_{HSCLK_OUT} (output clock frequency)	—	—	—	800(50)	—	—	700(50)	—	—	625(50)	—	—	625(50)	MHz
Transmitter	True Differential I/O Standards - f_{HSDR} (data rate)(51)	SERDES factor J = 4 to 10(52) (53) (54)	150	—	1,600	150	—	1,434	150	—	1,250	150	—	1,000	Mbps
		SERDES factor J = 3(52) (53) (54)	150	—	1,200	150	—	1,076	150	—	938	150	—	600	Mbps

continued...

(50) This is achieved by using the PHY clock network.

(51) Requires package skew compensation with PCB trace length.

(52) The F_{max} specification is based on the fast clock used for serial data. The interface F_{max} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

(53) The V_{CC} and V_{CCP} must be on a combined power layer and a maximum load of 5 pF for chip-to-chip interface.

(54) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource that you use. The I/O differential buffer and serializer do not have a minimum toggle rate.

Parameter	Symbol	Condition	–1 Speed Grade			–2 Speed Grade			–3 Speed Grade			–4 Speed Grade			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		SERDES factor J = 2, uses DDR registers	150	—	840(55)	150	—	(55)	150	—	(55)	150	—	(55)	Mbps
		SERDES factor J = 1, uses DDR registers	150	—	420(55)	150	—	(55)	150	—	(55)	150	—	(55)	Mbps
	$t_{x\ Jitter}$ - True Differential I/O Standards	Total jitter for data rate, 600 Mbps – 1.6 Gbps	≤1,600 Mbps: 160 ≤1,434 Mbps: 200 ≤1,250 Mbps: 250 ≤1,000 Mbps: 300 ≤800 Mbps: 320 600 Mbps: 340			≤1,434 Mbps: 200 ≤1,250 Mbps: 250 ≤1,000 Mbps: 300 ≤800 Mbps: 320 600 Mbps: 340			≤1,250 Mbps: 250 ≤1,000 Mbps: 300 ≤800 Mbps: 320 600 Mbps: 340			≤1,000 Mbps: 300 ≤800 Mbps: 320 600 Mbps: 340			ps
		Total jitter for data rate, < 600 Mbps	—	—	0.21	—	—	0.21	—	—	0.21	—	—	0.21	UI
	t_{DUTY} (56)	TX output clock duty cycle for	45	50	55	45	50	55	45	50	55	45	50	55	%

continued...

(55) The maximum ideal data rate is the SERDES factor (J) × the PLL maximum output frequency (f_{OUT}) provided you can close the design timing and the signal integrity meets the interface requirements.

(56) Not applicable for DIVCLK = 1.

Parameter	Symbol	Condition	–1 Speed Grade			–2 Speed Grade			–3 Speed Grade			–4 Speed Grade			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		Differential I/O Standards													
	t_{RISE} & t_{FALL} (53) (57)	True Differential I/O Standards	—	—	160	—	—	180	—	—	200	—	—	220	ps
	T_{CCS} (51) (56)	True Differential I/O Standards	—	—	330	—	—	330	—	—	330	—	—	330	ps
Receiver	True Differential I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 4 to 10(52) (53) (54)	150	—	1,600	150	—	1,434	150	—	1,250	150	—	1,000	Mbps
		SERDES factor J = 3(52) (53) (54)	150	—	1,200	150	—	1,076	150	—	938	150	—	600	Mbps
	f_{HSDR} (data rate) (without DPA)(51)	SERDES factor J = 3 to 10	(54)	—	(58)	(54)	—	(58)	(54)	—	(58)	(54)	—	(58)	Mbps
		SERDES factor J = 2, uses	(54)	—	(55)	(54)	—	(55)	(54)	—	(55)	(54)	—	(55)	Mbps

continued...

(57) This applies to default pre-emphasis and V_{OD} settings only.

(58) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

Parameter	Symbol	Condition	–1 Speed Grade			–2 Speed Grade			–3 Speed Grade			–4 Speed Grade			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		DDR registers													
		SERDES factor J = 1, uses DDR registers	(54)	—	(55)	(54)	—	(55)	(54)	—	(55)	(54)	—	(55)	Mbps
DPA (FIFO mode)	DPA run length	—	—	—	10,000	—	—	10,000	—	—	10,000	—	—	10,000	UI
DPA (soft CDR mode)	DPA run length	SGMII/ GbE protocol	—	—	5	—	—	5	—	—	5	—	—	5	UI
		All other protocols	—	—	50 data transition per 208 UI	—	—	50 data transition per 208 UI	—	—	50 data transition per 208 UI	—	—	50 data transition per 208 UI	—
Soft CDR mode	Soft-CDR ppm tolerance	—	–300	—	300	–300	—	300	–300	—	300	–300	—	300	ppm
Non DPA mode	Sampling Window	—	—	—	330	—	—	330	—	—	330	—	—	330	ps

DPA Lock Time Specifications

Table 41. DPA Lock Time Specifications

The DPA lock time is for one channel. One data transition is defined as a 0-to-1 or 1- to-0 transition.

For specification status, see the *Data Sheet Status* table

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions(59)	Maximum Data Transition
SPI-4	00000000001111111111	2	128	768
Parallel Rapid I/O	00001111	2	128	768
	10010000	4	64	768
Miscellaneous	10101010	8	32	768
	01010101	8	32	768

(59) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

LVDS SERDES Soft-CDR Sinusoidal Jitter Tolerance Specifications

Figure 2. LVDS SERDES Soft-CDR Sinusoidal Jitter Tolerance Specifications for a Data Rate Equal to 1.6 Gbps

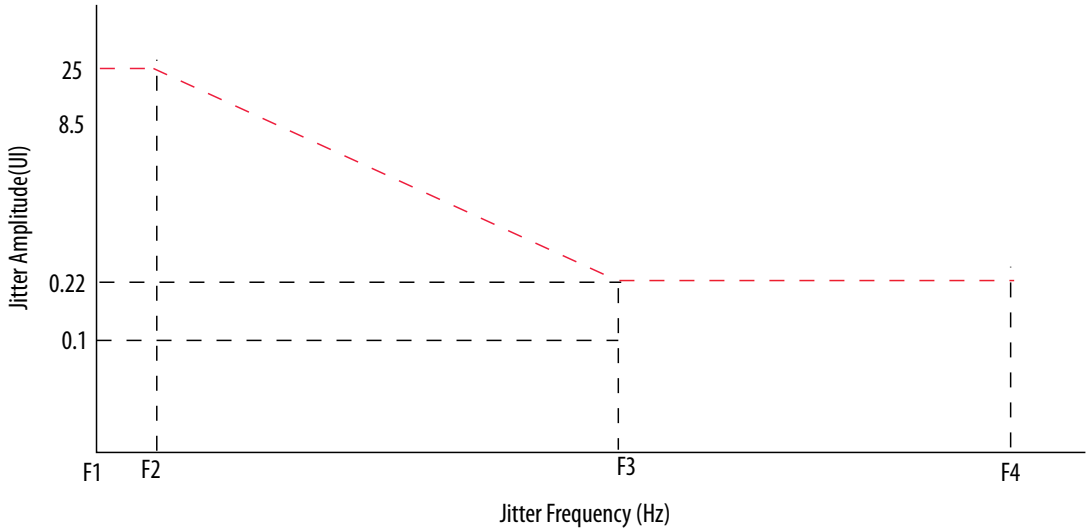
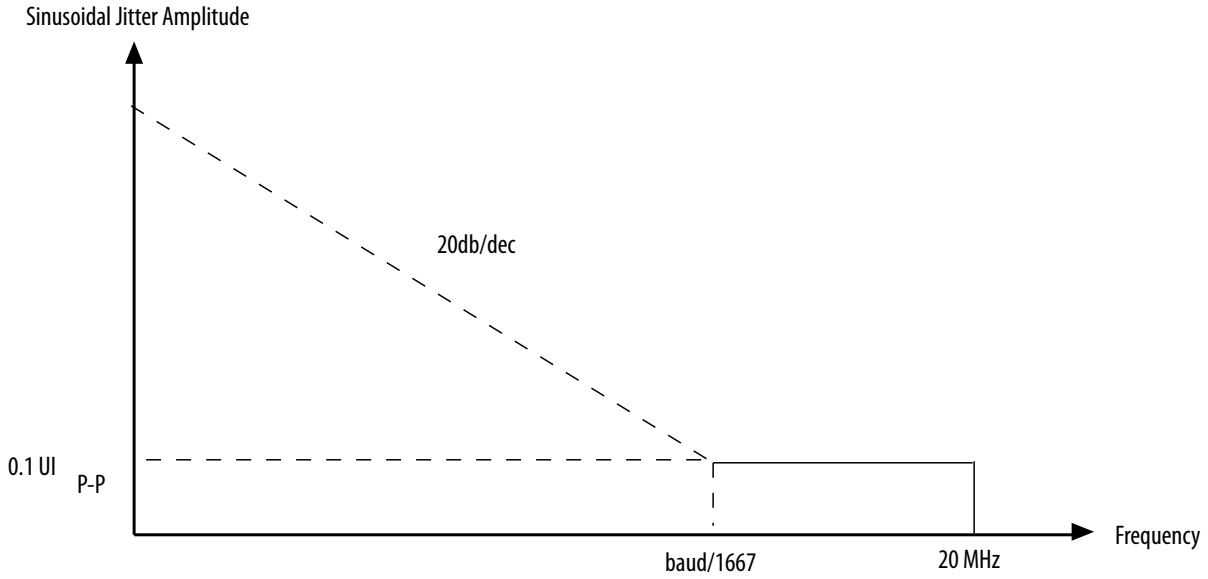


Table 42. LVDS SERDES Soft-CDR Sinusoidal Jitter Mask Values for a Data Rate Equal to 1.6 Gbps

For specification status, see the *Data Sheet Status* table

Parameter	Jitter Frequency (Hz)	Sinusoidal Jitter (UI)
F1	10,000	25
F2	17,565	25
F3	1,493,000	0.22
F4	50,000,000	0.22

Figure 3. LVDS SERDES Soft-CDR Sinusoidal Jitter Tolerance Specifications for a Data Rate Less than 1.6 Gbps



Memory Standards Supported

Table 43. Memory Standards Supported

This table lists the overall capability of External Memory Interface supported. For specific details, refer to the *External Memory Interface Spec Estimator*.

For specification status, see the *Data Sheet Status* table

Memory Standard	Controller Type	Maximum Frequency (MHz)
DDR4 SDRAM	Hard memory controller	1,600
QDR IV SRAM	Soft memory controller	1,066
DDR4 SDRAM	HPS hard memory controller	1,600

Related Information

External Memory Interface Spec Estimator
Provides the specific details of the memory standards supported.

DLL Range Specifications

Table 44. DLL Frequency Range Specifications

For specification status, see the *Data Sheet Status* table

Parameter	Performance (for All Speed Grades)	Unit
DLL operating frequency range	600 – 1,600	MHz
DLL reference clock input	Minimum 600	MHz

Memory Output Clock Jitter Specifications

The clock jitter specification applies to the memory output clock pins clocked by an I/O PLL, or generated using differential signal-splitter and double data I/O circuits clocked by a PLL output routed on a PHY clock network as specified. Intel recommends using PHY clock networks for better jitter performance.

The memory clock output jitter is within the JEDEC specifications when the phase jitter (integration bandwidth 10 kHz to 50 MHz) of the input clock is not more than 20 ps peak-to-peak, or 1.42 ps RMS at $1e^{-12}$ BER and 1.22 ps at $1e^{-16}$ BER.

E-Tile Transceiver Performance Specifications

This section provides E-tile transceiver specifications and timing.

E-Tile Transceiver Performance

Table 45. E-Tile Transmitter and Receiver Data Rate Performance Specifications

For specification status, see the *Data Sheet Status* table

Symbol/Description	Condition	Transceiver Speed Grade			Unit
		–1	–2	–3	
Supported data rate(60)	NRZ	28.9	28.3	17.4	Gbps
	PAM4	57.8(61)	56	32	Gbps

E-Tile Transceiver Reference Clock Specifications

Table 46. E-Tile Reference Clock LVPECL DC Electrical Characteristics

For specification status, see the *Data Sheet Status* table

Symbol	Refclk Parameter	Min	Typ	Max	Unit
V_{TT}	Termination voltage (2.5 V compliant)	0.4	0.5	0.6	V
	Termination voltage (3.3 V compliant)	1.04	1.3	1.56	V
R_{TT}	Termination resistor	40	50	60	Ω
V_{DIFF}	Differential voltage	0.4	0.8	1.2	V
V_{CM}	Input common mode voltage (2.5 V compliant, no internal termination resistor)	$V_{DIFF}/2$	—	$V_{CCCLK\_GXE} - V_{DIFF}/2$	V
	Input common mode voltage (2.5 V compliant, internal termination resistor)	$V_{CCCLK\_GXE} - 1.6$	$V_{CCCLK\_GXE} - 1.3$	$V_{CCCLK\_GXE} - 1.0$	V
	Input common mode voltage (3.3 V compliant, no internal termination resistor)	$V_{DIFF}/2$	—	$V_{CCCLK\_GXE} - V_{DIFF}/2$	V
	Input common mode voltage (3.3 V compliant, internal termination resistor)	1.4	2	2.6	V

(60) The supported data rate is for chip-to-chip and backplane links.

(61) Two channels are combined to support up to 57.8 Gbps.

Table 47. E-Tile Reference Clock Electrical and Jitter Requirements

For specification status, see the *Data Sheet Status* table

Parameter	Condition	Min	Typ	Max	Unit
Frequency	—	125	156.25	700	MHz
Frequency tolerance	—	–100	—	100	ppm
Clock duty cycle	—	45	50	55	%
Rise/Fall times	20% to 80%	40	—	300	ps
Phase jitter	12 kHz to 20 MHz	—	0.375	0.5	ps rms
Phase noise(62)	10 kHz	—	—	–130	dBc/Hz
	100 kHz	—	—	–138	dBc/Hz
	500 kHz	—	—	–138	dBc/Hz
	3 MHz	—	—	–140	dBc/Hz
	10 MHz	—	—	–144	dBc/Hz
	20 MHz	—	—	–146	dBc/Hz

E-Tile Transmitter Specifications

Table 48. E-Tile Transmitter Specifications

For specification status, see the *Data Sheet Status* table

Symbol/Description	Condition	Min	Typ	Max	Unit
Transmitter differential output voltage peak-to-peak	No precursor/postcursor de-emphasis	—	0.965	—	V
Transmitter common mode voltage	—	$V_{CCRT\_GXE}/2$			V

(62) The phase noise numbers in this table are the maximum acceptable phase noise values measured at a carrier frequency of 156.25 MHz. To calculate the phase noise requirement at any other frequency, use the formula: REFCLK phase noise at f (MHz) = REFCLK phase noise at 156.25 MHz + $20*\log_{10}(f/156.25)$.

E-Tile Receiver Specifications

Table 49. E-Tile Receiver Specifications

For specification status, see the *Data Sheet Status* table

Symbol/Description	Condition	Min	Typ	Max	Unit
Absolute V_{MAX} for a receiver pin	NRZ	—	V_{CCH_GXE} + 0.3	—	V
	PAM4	—	V_{CCH_GXE}	—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before/after device configuration	—	1.2			V
V_{CM} (Internal AC coupled)(63)	NRZ	GND	—	V_{CCH_GXE}	V
	PAM4	GND + 0.3	—	V_{CCH_GXE} – 0.3	V
Receiver run length(64)	—	—	—	100(65)	symbols
DC input impedance	—	40	—	60	Ω
DC differential input impedance	—	80	100	120	Ω
Powered down DC input impedance	Receiver pin impedance when the receiver termination is powered down	100k	—	—	Ω
Differential termination	From DC to 100 MHz	80	100	120	Ω
PPM tolerance	Allowed frequency mismatch between REFCLK and RX data	—	—	750	ppm

(63) This value uses internal AC coupling. External coupling capacitors are required beyond the range mentioned in this table.

(64) No additional transition density requirements apply.

(65) The incoming data must be statistically DC-balanced.

P-Tile Transceiver Performance Specifications

This section provides P-tile transceiver specifications and timing.

P-Tile Transceiver Performance

Table 50. P-Tile Transmitter and Receiver Data Rate Performance

For specification status, see the *Data Sheet Status* table

Symbol/Description	Condition	Gen 1	Gen 2	Gen 3	Gen 4	Unit
Supported data rate	PCIe*	2.5	5	8	16	Gbps

Table 51. P-Tile PLLA Performance

For specification status, see the *Data Sheet Status* table

Symbol/Description	Condition	Transceiver Speed Grade			Unit
		Min	Typ	Max	
VCO frequency	—	—	5	—	GHz
PLL bandwidth (BWTX-PKG_PLL1)(66)	PCIe 2.5 GT/s	1.5	—	22	MHz
	PCIe 5.0 GT/s	8	—	16	MHz
PLL bandwidth (BWTX-PKG_PLL2)(66)	PCIe 5.0 GT/s	5	—	16	MHz
PLL peaking (PKGTX-PLL1)	PCIe 2.5 GT/s	—	—	3	dB
	PCIe 5.0 GT/s	—	—	3	dB
PLL peaking (PKGTX-PLL2)(66)	PCIe 5.0 GT/s	1	—	—	dB

(66) The Tx PLL bandwidth must lie between the minimum and maximum ranges given in this table. PLL peaking must lie below the value in this table. Note that the PLL bandwidth extends from zero up to the values specified in this table. The PLL bandwidth is defined at the point where its transfer function crosses the –3 dB point.

Table 52. P-Tile PLLB Performance

For specification status, see the *Data Sheet Status* table

Symbol/Description	Condition	Transceiver Speed Grade			Unit
		Min	Typ	Max	
VCO frequency	—	—	8	—	GHz
PLL bandwidth (BWTX-PKG_PLL1)(67)	PCIe 8.0 GT/s	2	—	4	MHz
	PCIe 16.0 GT/s	2	—	4	MHz
PLL bandwidth (BWTX-PKG_PLL2)(67)	PCIe 8.0 GT/s	2	—	5	MHz
	PCIe 16.0 GT/s	2	—	5	MHz
PLL peaking (PKGTX-PLL1)(67)	PCIe 8.0 GT/s	—	—	2	dB
	PCIe 16.0 GT/s	—	—	2	dB
PLL peaking (PKGTX-PLL2)(67)	PCIe 8.0 GT/s	—	—	1	dB
	PCIe 16.0 GT/s	—	—	1	dB

P-Tile Transceiver Reference Clock Specifications

Table 53. P-Tile Reference Clock Specifications

For specification status, see the *Data Sheet Status* table

Symbol/Description	Condition	All Transceiver Speed Grades			Unit
		Min	Typ	Max	
Supported I/O standards	—	HCSL			—
Input reference clock frequency(68)	—	99.97	100	100.03	MHz

continued...

(67) The Tx PLL bandwidth must lie between the minimum and maximum ranges given in this table. PLL peaking must lie below the value in this table. Note that the PLL bandwidth extends from zero up to the values specified in this table. The PLL bandwidth is defined at the point where its transfer function crosses the –3 dB point.

Symbol/Description	Condition	All Transceiver Speed Grades			Unit
		Min	Typ	Max	
Rising edge rate(69)	PCIe	0.6	—	4	V/ns
Falling edge rate(69)	PCIe	0.6	—	4	V/ns
Duty cycle	PCIe	40	—	60	%
Spread-spectrum modulating clock frequency	—	30	—	33	kHz
Spread-spectrum downspread	—	–0.5	—	0	%
Absolute V_{MAX}	—	—	—	1.15	V
Absolute V_{MIN}	—	—	—	–0.3	V
Peak-to-peak differential input voltage	—	300	—	1,500	mV
V_{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	mV
Cycle to cycle jitter (TCCJITTER)(70)	PCIe	—	—	150	ps
TSSC-MAX-PERIOD-SLEW	Max SSC df/dt	—	—	1,250	ppm/µs

Related Information

- PCI Express Base Specification Revision 3.0
- PCI Express Base Specification Revision 4.0

(68) This number is with spread spectrum clocking (SSC) turned off. For systems with spread spectrum clocking, follow the specifications in *Section 8.6.3 Data Rate Independent Refclk Parameters* in the *PCI Express* Base Specification Revision 4.0*.

(69) Measured from –150 mV to +150 mV on the differential waveform. The 300 mV measurement window is centered on the differential zero crossing.

(70) For common reference clock architecture, follow the jitter limit specified in the *PCI Express* Card Electromechanical Specification* for 2.5 GT/s, *Section 4.3.7 Refclk Specifications* for 5.0 GT/s and *Section 4.3.8 Refclk Specifications* for 8.0 GT/s in the *PCI Express Base Specification Revision 3.0*, and *Section 8.6 Refclk Specifications* for 16.0 GT/s in the *PCI Express Base Specification Revision 4.0*.

P-Tile Transmitter Specifications

Table 54. P-Tile Transmitter Specifications

For specification status, see the *Data Sheet Status* table

Symbol/Description	Condition	All Transceiver Speed Grades			Unit
		Min	Typ	Max	
Supported I/O standards	PCIe	High Speed Differential I/O			—
Differential on-chip termination resistors	PCIe	80	—	120	Ω
Differential peak-to-peak voltage for full swing	PCIe 2.5 GT/s	800	—	1,100	mV
	PCIe 5.0 GT/s	800	—	1,100	mV
	PCIe 8.0 GT/s	800	—	1,100	mV
	PCIe 16.0 GT/s	800	—	1,100	mV
Differential peak-to-peak voltage during EIEOS	PCIe 8.0 GT/s and 16.0 GT/s	250	—	—	mV
Lane-to-lane output skew	PCIe 2.5 GT/s	—	—	2.5	ns
	PCIe 5.0 GT/s	—	—	2	ns
	PCIe 8.0 GT/s	—	—	1.5	ns
	PCIe 16.0 GT/s	—	—	1.25	ns

P-Tile Receiver Specifications

Table 55. P-Tile Receiver Specifications

For specification status, see the *Data Sheet Status* table

Symbol/Description	Condition	All Transceiver Speed Grades			Unit
		Min	Typ	Max	
Supported I/O standards	PCIe	High Speed Differential I/O			—
Peak-to-peak differential input voltage V_{ID} (diff p-p)	PCIe 2.5 GT/s[71]	175[72]	—	1,200	mV
	PCIe 5.0 GT/s[71]	100[72]	—	1,200	mV

continued...

Symbol/Description	Condition	All Transceiver Speed Grades			Unit
		Min	Typ	Max	
	PCIe 8.0 GT/s	25[72]	—	—[73]	mV
	PCIe 16.0 GT/s	15[72]	—	—[73]	mV
Differential on-chip termination resistors	—	80	—	120	Ω
RESREF[74]	—	167.3	169	170.7	Ω
RREF	—	2.772	2.8	2.828	kΩ

Related Information

PCI Express Base Specification Revision 4.0

(71) Voltage shown for PCIe 2.5 GT/s and 5.0 GT/s are at the package pins (TP2).

(72) For PCIe at 2.5 GT/s and 5 GT/s, the V_{ID} is measured at TP2, which is the accessible test point at the device under test. For PCIe 8.0 GT/s and 16.0 GT/s, the V_{ID} is measured at TP2P. TP2P defines a reference point that comprehends the effects of the behavioral Rx package plus Rx equalization and represents the only location where a meaningful eye height and eye width limits can be defined.

(73) The maximum eye height value depends on the transmitter launch voltage maximum value. Refer to the *PCIe Express Base Specification Rev. 4.0* for the generator (TX) launch voltage value.

(74) Connecting RESREF at 169 Ω calibrates PCIe channel on-chip termination to 85 Ω.

R-Tile Transceiver Performance Specifications

R-Tile Transceiver Performance

Table 56. R-Tile Transmitter and Receiver Data Rate Performance

For specification status, see the *Data Sheet Status* table

Symbol/Description	Condition	Transceiver Speed Grade		Unit
		–1	–2	
Supported data rate	PCIe	2.5, 5, 8, 16, 32	2.5, 5, 8, 16, 32	Gbps
	CXL	8, 16, 32	—	Gbps

Table 57. R-Tile Slow PLL Performance

For specification status, see the *Data Sheet Status* table

Symbol/Description	Condition	All Transceiver Speed Grades			Unit
		Min	Typ	Max	
VCO frequency	PCIe	—	10	—	GHz
	CXL	—	—	—	GHz
PLL bandwidth (BWTX-PKG_PLL1)(75)	PCIe 2.5 GT/s	1.5	—	22	MHz
	PCIe 5.0 GT/s	8	—	16	MHz
PLL bandwidth BWTX-PKG_PLL2)(75)	PCIe 2.5 GT/s	—	—	—	MHz
	PCIe 5.0 GT/s	5	—	16	MHz
PLL peaking (PKGTX-PLL1)(75)	PCIe 2.5 GT/s	—	—	3	dB
	PCIe 5.0 GT/s	—	—	3	dB
PLL peaking (PKGTX-PLL2)(75)	PCIe 2.5 GT/s	—	—	—	dB
	PCIe 5.0 GT/s	1	—	—	dB

(75) The Tx PLL bandwidth must lie between the minimum and maximum ranges given in this table. PLL peaking must lie below the value in this table. Note that the PLL bandwidth extends from zero up to the values specified in this table. The PLL bandwidth is defined at the point where its transfer function crosses the –3 dB point.

Table 58. R-Tile Fast PLL Performance

For specification status, see the *Data Sheet Status* table

Symbol/Description	Condition	All Transceiver Speed Grades			Unit
		Min	Typ	Max	
VCO frequency	PCIe	—	16	—	GHz
	CXL	—	16	—	GHz
PLL bandwidth (BWTX-PKG_PLL1)(76)	PCIe 8.0 GT/s	0.5	—	4	MHz
	PCIe 16.0 GT/s	0.5	—	4	MHz
	PCIe 32.0 GT/s	0.5	—	1.8	MHz
	CXL 8.0 GT/s	0.5	—	4	MHz
	CXL 16.0 GT/s	0.5	—	4	MHz
	CXL 32.0 GT/s	0.5	—	1.8	MHz
PLL bandwidth (BWTX-PKG_PLL2)(76)	PCIe 8.0 GT/s	0.5	—	5	MHz
	PCIe 16.0 GT/s	0.5	—	5	MHz
	PCIe 32.0 GT/s	—	—	—	—
	CXL 8.0 GT/s	0.5	—	5	MHz
	CXL 16.0 GT/s	0.5	—	5	MHz
	CXL 32.0 GT/s	—	—	—	—
PLL peaking (PKGTX-PLL1)(76)	PCIe 8.0 GT/s	—	—	2	dB
	PCIe 16.0 GT/s	—	—	2	dB
	PCIe 32.0 GT/s	—	—	2	dB
	CXL 8.0 GT/s	—	—	2	dB
	CXL 16.0 GT/s	—	—	2	dB

continued...

(76) The Tx PLL bandwidth must lie between the minimum and maximum ranges given in this table. PLL peaking must lie below the value in this table. Note that the PLL bandwidth extends from zero up to the values specified in this table. The PLL bandwidth is defined at the point where its transfer function crosses the –3 dB point.

Symbol/Description	Condition	All Transceiver Speed Grades			Unit
		Min	Typ	Max	
	CXL 32.0 GT/s	—	—	2	dB
PLL peaking (PKGTX-PLL2)(76)	PCIe 8.0 GT/s	—	—	1	dB
	PCIe 16.0 GT/s	—	—	1	dB
	PCIe 32.0 GT/s	—	—	—	—
	CXL 8.0 GT/s	—	—	1	dB
	CXL 16.0 GT/s	—	—	1	dB
	CXL 32.0 GT/s	—	—	—	—

R-Tile Transceiver Reference Clock Specifications

Table 59. R-Tile Reference Clock Specifications

For specification status, see the *Data Sheet Status* table

Symbol/Description	Condition	All Transceiver Speed Grades			Unit
		Min	Typ	Max	
Supported I/O standards	PCIe	HCSL			—
	CXL	HCSL			—
Refclk frequency for devices that support 32.0 GT/s(77)	PCIe	99.99	100	100.01	MHz
	CXL	99.99	100	100.01	MHz
Rising edge rate(78)	PCIe	0.6	—	4	V/ns
	CXL	0.6	—	4	V/ns

continued...

(77) This number is with spread-spectrum clocking (SSC) turned off. For systems with spread spectrum clocking, follow the specifications in *Section 8.6 Refclk Specifications of PCI Express Base Specification Revision 5.0 Version 1.0*.

(78) Measured from –150 mV to +150 mV on the differential waveform. The 300 mV measurement window is centered on the differential zero crossing.

Symbol/Description	Condition	All Transceiver Speed Grades			Unit
		Min	Typ	Max	
Falling edge rate[78]	PCIe	0.6	—	4	V/ns
	CXL	0.6	—	4	V/ns
Duty cycle	PCIe	40	—	60	%
	CXL	40	—	60	%
Absolute V_{MAX}	PCIe	—	—	1.15	V
	CXL	—	—	1.15	V
Absolute V_{MIN}	PCIe	—	—	–0.3	V
	CXL	—	—	–0.3	V
Peak-to-peak differential input voltage	PCIe	300	—	1,450	mV
	CXL	300	—	1,450	mV
Vcross	PCIe	250	—	550	mV
	CXL	250	—	550	mV
Cycle-to-cycle jitter ($T_{CCJITTER}$)[79]	PCIe	—	—	150	ps
	CXL	—	—	150	ps
Spread-spectrum modulating clock frequency	PCIe	30	—	33	kHz
	CXL	30	—	33	kHz
SSC deviation for devices that support 32.0 GT/s and SRIS when operating in SRIS mode at all speeds	PCIe	–0.3	—	0	%
	CXL	–0.3	—	0	%
$T_{SSC-MAX-PERIOD-SLEW}$	Max SSC df/dt for PCIe	—	—	1,250	ppm/µs
	Max SSC df/dt for CXL	—	—	1,250	ppm/µs

(79) For common reference clock architecture, you must meet the jitter limit specified in *Section 8.6 Refclk Specifications of PCI Express Base Specification Revision 5.0 Version 1.0*.

Related Information

PCI Express Base Specification Revision 5.0

R-Tile Transmitter Specifications

Table 60. R-Tile Transmitter Specifications

For specification status, see the *Data Sheet Status* table

Symbol/Description	Condition	All Transceiver Speed Grades			Unit
		Min	Typ	Max	
Supported I/O standards	PCIe	High-Speed Differential I/O			—
	CXL	High-Speed Differential I/O			—
Differential on-chip termination resistors	PCIe	80	100	120	Ω
	CXL	80	100	120	Ω
Differential peak-to-peak voltage for full swing	PCIe 2.5 GT/s	800	—	1,200	mV
	PCIe 5.0 GT/s	800	—	1,200	mV
	PCIe 8.0 GT/s	800	—	1,300	mV
	PCIe 16.0 GT/s	800	—	1,300	mV
	PCIe 32.0 GT/s	800	—	1,300	mV
	CXL 8.0 GT/s	800	—	1,300	mV
	CXL 16.0 GT/s	800	—	1,300	mV
	CXL 32.0 GT/s	800	—	1,300	mV
Differential peak-to-peak voltage during EIEOS	PCIe 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s	250	—	—	mV
	CXL 8.0 GT/s, 16.0 GT/s, and 32.0 GT/s	250	—	—	mV
Lane-to-lane output skew	PCIe 2.5 GT/s	—	—	2.5	ns
	PCIe 5.0 GT/s	—	—	2	ns
	PCIe 8.0 GT/s	—	—	1.5	ns

continued...

Symbol/Description	Condition	All Transceiver Speed Grades			Unit
		Min	Typ	Max	
	PCIe 16.0 GT/s	—	—	1.25	ns
	PCIe 32.0 GT/s	—	—	1.25	ns
	CXL 8.0 GT/s	—	—	1.5	ns
	CXL 16.0 GT/s	—	—	1.25	ns
	CXL 32.0 GT/s	—	—	1.25	ns

R-Tile Receiver Specifications

Table 61. R-Tile Receiver Specifications

For specification status, see the *Data Sheet Status* table

Symbol/Description	Condition	All Transceiver Speed Grades			Unit
		Min	Typ	Max	
Supported I/O standards	PCIe	High-Speed Differential I/O			—
	CXL	High-Speed Differential I/O			—
Peak-to-peak differential input voltage V_{ID} (diff p-p)	PCIe 2.5 GT/s(80)	175	—	1,200	mVPP
	PCIe 5.0 GT/s(80)	100	—	1,200	mVPP
	PCIe 8.0 GT/s(80)	25	—	1,200	mVPP
	PCIe 16.0 GT/s(80)	15	—	800	mVPP
	PCIe 32.0 GT/s(80)	15	—	800	mVPP
	CXL 8.0 GT/s(80)	25	—	1,200	mVPP
	CXL 16.0 GT/s(80)	15	—	800	mVPP

continued...

(80) For PCIe at 2.5 GT/s and 5 GT/s, V_{ID} is measured at TP2, which is the accessible test point at the device under test. For PCIe and CXL 8.0 GT/s, 16.0 GT/s and 32.0 GT/s, V_{ID} is measured at TP2P. TP2P defines a reference point that comprehends the effects of the behavioral Rx package plus Rx equalization and represents the only location where a meaningful eye height and eye width limits can be defined.

Symbol/Description	Condition	All Transceiver Speed Grades			Unit
		Min	Typ	Max	
	CXL 32.0 GT/s(80)	15	—	800	mVPP
Differential on-chip termination resistors	PCIe	80	100	120	Ω
	CXL	80	100	120	Ω
RCOMP	PCIe (81)	148.5	150	151.5	Ω
	CXL(81)	148.5	150	151.5	Ω

F-Tile Transceiver Performance Specifications

F-Tile Transceiver Performance

Table 62. F-Tile FHT Transmitter and Receiver Data Rate Performance

For specification status, see the *Data Sheet Status* table

Symbol/Description	Condition	Transceiver Speed Grade			Unit
		–1	–2	–3	
Supported data rate	NRZ	24–29, 48–58	24–29	24–29	Gbps
	PAM4	48–58, 96–116	48–58	48–58	Gbps

Table 63. F-Tile FGT Transmitter and Receiver Data Rate Performance

For specification status, see the *Data Sheet Status* table

Symbol/Description	Condition	Transceiver Speed Grade			Unit
		–1	–2	–3	
Supported data rate	NRZ	1–32	1–32	1–17.4	Gbps
	PAM4	20–58.125	20–58.125	20–32	Gbps

(81) Connecting RCOMP at 150 Ω calibrates PCIe and CXL channel on-chip termination to 100 Ω.

F-Tile Transceiver Reference Clock Specifications

Table 64. F-Tile FHT Reference Clock Requirements

For specification status, see the *Data Sheet Status* table

Parameter	Description	Condition	Min	Typical	Max	Unit
Frequency	Reference clock frequency	—	100	156.25	200	MHz
Frequency accuracy	Frequency accuracy of the reference clock, including temperature variability, aging, and initial variation	—	—	—	±100	ppm
Single sideband phase noise	Measured SSB phase noise must be smaller than phase noise mask(82)	10 kHz	—	–130	—	dB
		100 kHz	—	–138	—	dB
		500 kHz	—	–138	—	dB
		3 MHz	—	–140	—	dB
		10 MHz	—	–144	—	dB
		20 MHz	—	–146	—	dB
		1 GHz	—	–146 (83)	—	dB
Integrated RMS jitter	Integrated over 10 kHz – 20 MHz, include spurious	—	—	—	522	fs

(82) Add an offset of 20 × log10(F_{clk}/156.25 MHz) dB to mask values, where F_{clk} is reference clock frequency.

(83) The phase noise mask requirement between 20 MHz and 1 GHz excludes any harmonics power of the fundamental clock.

Table 65. F-Tile FHT Reference Clocks Input Specifications

For specification status, see the *Data Sheet Status* table

Parameter	Description	Condition	Min	Typical	Max	Unit
$T_{REF-DUTY}$	Duty cycle	—	45	50	55	%
$T_{REF-RISE/FALL}$	Rising and falling edge rate	20% – 80%	40	—	300	ps
$T_{REF-SINGLEEND-SKEW}$	Skew between REFCLKP and REFCLKN	—	—	—	5	ps
$Z_{REF-SINGLEEND-DC}$	Reference clock input impedance – terminated mode	—	40	50	60	Ω
$V_{REFIN-SE-PP}$	Input reference clock single-ended peak-to-peak voltage	—	200	—	510	mV
$V_{REFIN-CM-AC}$	Input reference clock common-mode voltage when AC-coupled on board	—	Set on-chip (no user access)			—
$V_{REFIN-IL-DC}$	Input reference clock input low voltage when DC-coupled on board	—	0.1	—	—	V
$V_{REFIN-IH-DC}$	Input reference clock input high voltage when DC-coupled on board	—	—	—	0.9	V

Table 66. F-Tile FGT Reference Clock Input Specifications

For specification status, see the *Data Sheet Status* table

Parameter	Description	Condition	Min	Typical	Max	Unit
F_{REF}	Reference clock operating frequency	—	100(84)	—	380	MHz
$T_{REF-DUTY}$	Duty cycle	—	45	50	55	%
$T_{REF-RISE/FALL}$	Rising and falling edge rate	20% – 80%	—	—	0.15 × T_{ref_period}	ps
$T_{REF-SINGLEEND-SKEW}$	Skew between REFCLKP and REFCLKN	—	—	—	50	ps
$Z_{REF-DIFF-DC}$	Reference clock differential input impedance – terminated mode	—	80	100	120	Ω
$V_{REFIN-DIFF}$ (85)	Input reference clock differential peak-to-peak voltage	—	0.6	1.2	1.7	V
$V_{REFIN-IL-DC}$	Input reference clock input low voltage when DC-coupled on board	—	0	—	—	V
$V_{REFIN-IH-DC}$	Input reference clock input high voltage when DC-coupled on board	—	—	—	1	V
$V_{REFIN-CM-AC}$	Input reference clock common-mode voltage when AC-coupled on board	—	Set on-chip (no user access)			V

continued...

(84) This value is 100 MHz for down SSC (Spread Spectrum Clocking) clocking. This value can also be 25 MHz for HDMI rate of less than 1 Gbps.

(85) LVDS is recommended with on-board AC-coupling and subject to 0.6 V ≤ $V_{REFIN-DIFF}$ ≤ 1.7 V.

Parameter	Description	Condition	Min	Typical	Max	Unit
$V_{REFIN-CM-DC}$	Input reference clock common-mode voltage when DC-coupled on board	—	0.2	—	0.8	V
$PN_{REF-SSB}$ (156.25MHz)	Reference clock measured single sideband phase noise mask including spurs must be smaller than phase noise mask(86)	10 kHz	—	–130	—	dBc/Hz
		100 kHz	—	–138	—	dBc/Hz
		500 kHz	—	–138	—	dBc/Hz
		3 MHz	—	–140	—	dBc/Hz
		10 MHz	—	–144	—	dBc/Hz
		20 MHz	—	–146	—	dBc/Hz
		1 GHz	—	–146	—	dBc/Hz
$V_{REFIN-RJ-RMS}$	RMS jitter integrated from 10 kHz – 20 MHz including spurs	—	—	—	522	fs
$V_{REFIN-PPM-ERROR}$	Reference clock frequency error	—	–350 + SSC	—	+350 + SSC	ppm

Table 67. F-Tile FGT Reference Clock Output Driver Specifications

For specification status, see the *Data Sheet Status* table

Parameter	Description	Condition	Min	Typical	Max	Unit
F_{REF_OUT}	Reference clock operating frequency	—	25	—	800	MHz
$T_{REF-DUTY\_OUT}$	Duty cycle	—	45	50	55	%
$T_{REF-RISE\_OUT/FALL\_OUT}$	Rising and falling edge rate	20% – 80%	—	—	0.15 × T_{ref_period}	ps
$T_{REF-SINGLEEND-SKEW}$	Skew between REFCLKP and REFCLKN	—	—	—	50	ps

continued...

(86) Add an offset of 20 × log10(Fcc/Hzlk/156.25 MHz) dB to mask values, where F_{clk} is reference clock frequency.

Parameter	Description	Condition	Min	Typical	Max	Unit
$Z_{REF-DIFF-DC\_OUT}$	Reference clock differential output impedance – terminated mode	—	80	100	120	Ω
$V_{REFIN-DIFF-AC\_OUT}$	Output reference clock differential peak to peak voltage when AC-coupled on board	—	0.9	1	1.1	V
$V_{REFIN-CM-OUT}$ (87)	Output reference clock common-mode	—	0.45	0.5	0.55	V

F-Tile Transmitter Specifications

Table 68. F-Tile FHT Transmitter Electrical Specifications

For specification status, see the *Data Sheet Status* table

Parameter	Symbol	Description	Min	Typical	Max	Unit
Output eye specifications	$V_{TX-DIFF-PKPK}$	Transmit amplitude (low frequency)	800	—	1,200	$mV_{diff-pkpk}$
	$V_{TX-DEEMP\_STEP}$	Transmit tap resolution for c(0), c(1), and c(–1)	0.5	—	5	%
		Transmit tap resolution for c(–2)	0.5	—	2.5	%
	$T_{TX-SLEW}$	Rise/fall time	8	—	—	ps
Transmitter output voltage	$V_{TX-CM\ OUT}$	Transmitter output common-mode voltage	0.1	0.85	0.9	V

continued...

(87) If your far-end differential termination is comprised of two 50 Ω terminations to GND, the common-mode voltage is nominally 250 mV. If your far-end differential termination is comprised of a single 100 Ω differential termination between the P and N signals, the common-mode voltage is nominally 500 mV.

Parameter	Symbol	Description	Min	Typical	Max	Unit
Transmitter DC impedance	$Z_{TX-DIFF-DC}$	Transmitter output differential DC impedance 100 W mode while configured	80	100	120	Ω
	$Z_{TX-CM-DC}$	Transmitter output common-mode DC impedance	20	25	30	Ω
Transmitter return loss	$Z_{RL-DIFF-DC}$	Transmitter differential DC return loss	—	—	–14.5	dB
	$Z_{RL-DIFF-NYQ}$	Transmitter differential return loss at Nyquist frequency ($F_{BAUD}/2$)	—	—	–8	dB
	Z_{RL-CMN}	Transmitter common-mode return loss below 10 GHz	—	—	–6	dB
Electrical idle	$V_{TX-IDLE}$	Idle output voltage	—	—	50	mV_{pkpk}
	$V_{CM-DELTA-SQUELCH}$	Maximum common-mode step entering/ exiting squelch mode	—	—	100	mV
	$T_{TX-IDLE-LATENCY}$	Latency entering/ exiting idle (cold boot)	—	—	28	ms
		Power state cycle (re-establish CM)	—	—	5	µs

Table 69. F-Tile FGT Transmitter Electrical Specifications

For specification status, see the *Data Sheet Status* table

Parameter	Symbol	Description	Min	Typical	Max	Unit
Output eye specifications	$V_{TX-DIFF-PKPK}$	Back-porch transmit amplitude	300	—	1,050	mV
	$V_{TX-DEEMP\_STEP}$	Transmit tap resolution	—	—	2	%
	$D_{TX-N+2-DEEMP}$	N+2 precursor tap de-emphasis	0	—	2.5	dB

continued...

Parameter	Symbol	Description	Min	Typical	Max	Unit
	$D_{TX-N+1-DEEMP}$	N+1 precursor tap de-emphasis	0	—	4.5	dB
	$D_{TX-N-1-DEEMP}$	N-1 postcursor tap de-emphasis	0	—	6.5	dB
	$T_{TX-SLEW}$	Rise/fall time at 20%–80%	10	—	20	ps
	T_{TX-DJ}	Transmit deterministic jitter at 25 Gbps	—	—	0.15	UI_{pkpk}
	T_{TX-RJ}	Transmit total peak-peak random jitter(88)	—	—	0.15	UI_{pkpk}
	T_{TX-TJ}	Transmit total peak-peak jitter (T_{TX-TJ} = T_{TX-DDJ} + T_{TX-PJ} + T_{TX-RJ})(88)	—	—	0.28	UI_{pkpk}
Transmitter output voltage	$V_{TX-CM\ OUT}$	Transmitter output common-mode voltage	0.45	0.5	0.55	V
Transmitter DC impedance	$Z_{TX-DIFF-DC}$	Transmitter output differential DC impedance 90 Ω mode while configured(89)	80	90	120	Ω
	$Z_{TX-CM-DC}$	Transmitter output common-mode DC impedance	20	25	30	Ω
Transmitter return loss	$Z_{RL-DIFF-DC}$	Transmitter differential DC return loss	—	—	–12	dB
	$Z_{RL-DIFF-NYQ}$	Transmitter differential return loss at Nyquist frequency (F_{BAUD}/2)	—	—	–6	dB

continued...

(88) Assume a 1st order high-pass jitter measurement filter with a cutoff of $F_{baud}/F_{gpll} = N_{gpll}$.

(89) TX pins are driven to 0 V before mode configuration.

Parameter	Symbol	Description	Min	Typical	Max	Unit
	Z_{RL-CMN}	Transmitter common-mode return loss below 10 GHz	—	—	–6	dB
Electrical idle	$V_{TX-IDLE}$	Idle output voltage	—	—	20	mV
	$V_{CM-DELTA-SQUELCH}$	Maximum common-mode step entering/ exiting squelch mode	—	—	100	mV
	$T_{TX-IDLE-LATENCY}$	Latency entering/ exiting idle (cold boot), power state cycle (re-establish CM)	—	—	8	µs
Receiver detect	$V_{TX-RCV-DETECT}$	Voltage change allowed during receiver detection	—	—	600	mV
Lane-to-lane output skew	—	Lane count ≤ 8	—	—	2 UI + 200 ps	ps
	—	Lane count = 16	—	—	2 UI + 300 ps	ps

F-Tile Receiver Specifications

Table 70. F-Tile FHT Receiver Electrical Specifications

For specification status, see the *Data Sheet Status* table

Parameter	Symbol	Description	Min	Typical	Max	Unit
Receiver input eye specifications	$V_{RX-DIFF-PKPK}$	Receiver input differential peak-to-peak voltage	Closed eye	—	1,200	$mV_{diff-pkpk}$
	$V_{RX-CM-DC}$	Receiver input DC common-mode voltage(90)	100	750	900	mV
	V_{RX-MAX}	Receiver input maximum voltage	—	—	1,200	mV

continued...

(90) Referenced to RX GND. This specification is also supported before mode configuration.

Parameter	Symbol	Description	Min	Typical	Max	Unit
	V_{RX-MIN}	Receiver input minimum voltage	–200	—	—	mV
	T_{RX-DDJ}	Receive input signal data dependent jitter (inter-symbol interference)	—	—	1	UI_{pkpk}
	T_{RX-RJ}	Receive input random jitter	—	—	0.15	UI_{pkpk}
	T_{RX-PJ}	Receive input periodic jitter (at high frequency)	—	—	0.05	UI_{pkpk}
	T_{RX-TJ}	Receive input total jitter (DDJ + RJ + PJ)	—	—	1	UI_{pkpk}
Equalizer specifications	$F_{PPM-OFFSET}$	Tolerable data frequency offset	–200	—	200	ppm
Receiver return loss	$Z_{RL-DIFF-DC}$	Receiver differential DC return loss	—	—	–10	dB
	$Z_{RL-DIFF-NYQ}$	Receiver differential return loss at Nyquist frequency ($F_{BAUD}/2$)	—	—	–6	dB
	Z_{RL-CM}	Receiver common-mode return loss below 10 GHz	—	—	–6	dB
Receiver DC impedance	$R_{DIFF-DC}$	DC differential receive impedance	80	100	120	Ω
	R_{CM-DC}	DC common-mode receive impedance	20	25	30	Ω

Table 71. F-Tile FGT Receiver Electrical Specifications

For specification status, see the *Data Sheet Status* table

Parameter	Symbol	Description	Min	Typical	Max	Unit
Receiver input eye specifications	$V_{RX-DIFF-PKPK}$	Receiver input differential peak-to-peak voltage	—	—	1,200	mV
	V_{RX-MAX}	Receiver input maximum voltage(91)	—	—	1	V
	V_{RX-MIN}	Receiver input minimum voltage(91)	–0.3	—	—	V
	$V_{RX-CM-DC}$	Receiver input DC common-mode voltage(92)	0	—	700	mV
	T_{RX-RJ}	Receive input random jitter	—	—	0.15	UI_{pkpk}
	T_{RX-PJ}	Receive input periodic jitter (at high frequency)	—	—	0.05	UI_{pkpk}
Insertion loss specifications	$I_{INS-LOSS-56Gb/s}$	Insertion loss at 56 Gbps PAM42/BER $<10^{-4}$	—	—	–30	dB
	$I_{INS-LOSS-53Gb/s}$	Insertion loss at 53 Gbps PAM42/BER $<10^{-4}$	5(93)	—	—	dB
	$I_{INS-LOSS-30Gb/s}$	Insertion loss at 32 Gbps NRZ(94) /BER $<10^{-12}$	—	—	–30	dB

continued...

(91) V_{RX_MAX} and V_{RX_MIN} are before and after configuration.

(92) The specified common-mode range is supported when the receiver is powered and configured, powered and unconfigured, or unpowered. This specification is also supported before mode configuration. If squelch detect is used, receiver DC input common-mode voltage should be within 200 mV to 300 mV. Otherwise, use AC coupling capacitors on board.

(93) The minimum insertion loss specification assumes a PAM4 transmitter with 800 mVppd. For transmitters with output amplitude adjustment capabilities and can reduce output amplitude to below 800 mVppd, this minimum insertion loss can be further relaxed.

Parameter	Symbol	Description	Min	Typical	Max	Unit
	$I_{INS-LOSS-25Gb/s}$	Insertion loss at 25.78125 Gbps NRZ(94)/ BER <10^{-12}	—	—	–30	dB
Receiver return loss	$Z_{RL-DIFF-DC}$	Receiver differential DC return loss	—	—	–12	dB
	$Z_{RL-DIFF-NYQ}$	Receiver differential return loss at Nyquist frequency ($F_{BAUD}/2$)	—	—	–6	dB
	Z_{RL-CM}	Receiver common-mode return loss below 10 GHz	—	—	–6	dB
Receiver DC impedance	$R_{DIFF-DC}$	DC differential receive impedance	65	85	102	Ω
			80	100	120	Ω
	R_{CM-DC}	DC common-mode receive impedance	20	25	30	Ω
Receiver signal detection(95)	$V_{IDLE-THRESH}$	Receiver signal detect input voltage threshold	75	120	175	$mV_{diff-pkpk}$

F-Tile Electrical Compliance

Table 72. F-Tile FHT Electrical Compliance List

For specification status, see the *Data Sheet Status* table

Specification/Clause	Protocol	Encoding	Lane Rate (Gbps)
IEEE 802.3bs 120D/120E	400GAUI-4	PAM4	106.25
	200GAUI-2	PAM4	106.25
	200GAUI-4	PAM4	53.125

continued...

(94) 2COM compliant package and channel.

(95) Receiver signal detection values in this table are applicable to PCIe and similar standards, such as SATA, where a clock pattern like PCIe EIEOS 500 MHz clock pattern is used.

Specification/Clause	Protocol	Encoding	Lane Rate (Gbps)
IEEE 802.3cd 135G/135F	100GAUI-1	PAM4	106.25
	100GAUI-2	PAM4	53.125
	100GAUI-4	NRZ	25.78125
	50GAUI-1	PAM4	53.125
	50GAUI-2	NRZ	25.78125
IEEE 802.3cd 109A/109B	25GAUI-1	NRZ	25.78125
IEEE 802.3ck 163/162	400GBASE-KR4/CR4	PAM4	106.25
	200GBASE-KR2/CR2	PAM4	106.25
	100GBASE-KR/CR	PAM4	106.25
CEI 4.0/5.0	OIF-CEI-112G XSR/VSR/MR/LR	PAM4	96 – 116
	OIF-CEI-56G VSR/MR	PAM4	48 – 58
	OIF-CEI-28G VSR/SR/MR	NRZ	24 – 29
	OIF-25G	NRZ	24 – 29

Table 73. F-Tile FGT Electrical Compliance List

For specification status, see the *Data Sheet Status* table

Specification/Clause	Protocol	Encoding	Lane Rate (Gbps)
IEEE 802.3bs 120D/120E	400GAUI-8	PAM4	53.125
	400GAUI-16	NRZ	26.5625
	200GAUI-4	PAM4	53.125
	200GAUI-8	NRZ	26.5625
IEEE 802.3cd 135G/135F	100GAUI-2	PAM4	53.125
	100GAUI-4	NRZ	25.78125
	50GAUI-1	PAM4	53.125
	50GAUI-2	NRZ	26.5625

continued...

Specification/Clause	Protocol	Encoding	Lane Rate (Gbps)
IEEE 802.3cd 109A/109B	25GAUI-1	NRZ	25.78125
IEEE 802.3cd 137/136	200GBASE-KR4/CR4	PAM4	53.125
	100GBASE-KR2/CR2	PAM4	53.125
	50GBASE-KR/CR	PAM4	53.125
IEEE 802.3bj/bm 93 IEEE 802.3bj/bm 92	100GBASE-KR4	NRZ	25.78125
	100GBASE-CR4	NRZ	25.78125
IEEE 802.3bj/ba 85 IEEE 802.3bj/ba 84	40GBASE-KR4	NRZ	10.3125
	40GBASE-CR4	NRZ	10.3125
IEEE 802.3ap 2007	10GBASE-KR/CR	NRZ	10.3125
IEEE 802.3ap 2008	10GBASE-KX4	NRZ	10.3125
IEEE 802.3by 111/110	25GBASE-KR/CR	NRZ	25.78125
CEI 4.0	CEI-56G VSR/MR/LR	PAM4	36 – 58
	CEI-28G VSR/SR/MR	NRZ	19.9 – 28.1
	IOF-CEI-25G LR	NRZ	19.9 – 28.1
	CEI-11G SR/MR/LR	NRZ	9.95 – 11.2
	CEI-6G SR/LR	NRZ	4.976 – 6.375
G.709 G.sup56 G.sup43 G.sup58	OTU0	NRZ	1.327451
	OTU1	NRZ	2.666057
	OTU1e	NRZ	11.049107
	OTU2/2e	NRZ	10.709225/11.095728
	OTU2f	NRZ	11.317642
	OTU2r	NRZ	12.639086
	OTU3	NRZ	4x10.754603
	OTU4(OTL4.4)	NRZ	4x27.952493
	OTU4(OTL4.10)	NRZ	10x11.180997

continued...

Specification/Clause	Protocol	Encoding	Lane Rate (Gbps)
G.709.1	100G FlexO-SR (FOIC1.4)	NRZ	4x27.952369
	100G FlexO-SR (FOIC1.2)	PAM4	2x55.904737
	100G FlexO-SR (FOIC2.4)	PAM4	4x55.904737
	100G FlexO-SR (FOIC4.8)	PAM4	8x55.904737
G.709, G.709.4	OTU25u	NRZ	25.781651
	OTU25	NRZ	27.952.493
	OTU50u (OTU50u.2-RS)	NRZ	2x26.562.914
	OTU50u (OTU50u.1-RS)	PAM4	53.125827
	OTU50 (OTU50.2-RS)	NRZ	2x27.952493
	OTU50	PAM4	55.904987
PCIE BASE 4.0	PCIE	NRZ	2.5, 5, 8, 16
SMPTE 259M	SDI	NRZ	0.27
SMPTE 292M		NRZ	1.485/1.483516484
SMPTE 372M		NRZ	2.97/2.967032967
SMPTE ST 2081		NRZ	5.94/5.934065934
SMPTE ST 2082		NRZ	11.88/11.868131868
CPRI V7.0	CPRI	NRZ	1.2288
		NRZ	2.4576
		NRZ	3.072
		NRZ	4.9152
		NRZ	6.144
		NRZ	8.11008
		NRZ	9.8304
		NRZ	10.1376
		NRZ	12.16512

continued...

Specification/Clause	Protocol	Encoding	Lane Rate (Gbps)
		NRZ	24.33024
JESD204B	JESD204B	NRZ	up to 19.2
JESD204C	JESD204C	NRZ	up to 32
DP 2.0	DisplayPort 2.0	NRZ	1.62
		NRZ	2.7
		NRZ	5.4
		NRZ	8.1
		NRZ	10
		NRZ	13.5
		NRZ	20
FC-PI-2	Fiber Channel	NRZ	1.0625
		NRZ	2.125
FC-PI-5		NRZ	4.25
		NRZ	8.5
10GFC		NRZ	10.52
FC-PI-5		NRZ	14.025
FC-PI-6		NRZ	28.05
FC-PI-7		PAM4	57.8
Serial ATA revision 3.0	Sata Gen 1, 2, 3	NRZ	1, 3, 6
T10/BSR INCITS 519	SAS 1, 2, 3, 4	NRZ	3, 6, 12, 22.5
IEEE 802.3av	10G-EPON	NRZ	10
IEEE 802.3ah	1G-EPON	NRZ	1
G.984	GPON	NRZ	1.25, 2.5, 10.3
CEI-6G-SR	Interlaken	NRZ	6.25
CEI-11G-SR		NRZ	10.3125

continued...

Specification/Clause	Protocol	Encoding	Lane Rate (Gbps)
CEI-11G-SR+		NRZ	12.5
OIF-28G MR (OIF-CEI3.0)		NRZ	25.78125
OIF-CEI 56G PAM4-MR		PAM4	53.125
JESD204C	SerialLite IV	NRZ	32
HDMI1.0-1.2a	HDMI	NRZ	1.65 × 3 = 4.95
HDMI1.3-1.4b		NRZ	3.4 × 3 = 10.2
HDMI2.0-2.0b		NRZ	6 × 3 = 18
HDMI2.1		NRZ	12 × 4 = 48
SFF8431	SFP+	NRZ	9.8304 – 12.5
ITU-T G.8261 and G.8262	SyncE	NRZ/PAM4	10, 25, 50
InfiniBand™ Architecture Specification	InfiniBand	NRZ	5, 10, 14.062, 25.78125
RapidIO™ Interconnect Specification	SRIO	NRZ	1.25, 2.5, 3.125, 6.25, 10.3125

HPS Performance Specifications

This section provides hard processor system (HPS) specifications and timing.

HPS Clock Performance

Table 74. Maximum HPS Clock Frequencies

For specification status, see the *Data Sheet Status* table

Performance	V_{CCL_HPS} (V)	MPU Frequency (MHz)	L3 Frequency (MHz) (l3_main_free_clk)	MPFE Frequency (MHz)	Rate	DDR Clock (MHz)	DDR (Mb/s per pin)
–1 speed grade	Fixed: 0.95	1,500	400	400	Quarter	1,600	3,200
				667	Half	1,333	2,666
	SmartVID	1,350	400	400	Quarter	1,600	3,200

continued...

Performance	V_{CCL_HPS} (V)	MPU Frequency (MHz)	L3 Frequency (MHz) (l3_main_free_clk)	MPFE Frequency (MHz)	Rate	DDR Clock (MHz)	DDR (Mb/s per pin)
				667	Half	1,333	2,666
–2 speed grade	SmartVID	1,200	400	334	Quarter	1,333	2,666
				600	Half	1,200	2,400
–3 speed grade	SmartVID	1,000	400	300	Quarter	1,200	2,400
				534	Half	1,067	2,133
–4 speed grade	Fixed: 0.8	1,000	400	267	Quarter	1,067	2,133
				467	Half	933	1,866

Related Information

External Memory Interface Spec Estimator
Provides the specific details of the maximum allowed SDRAM operating frequency.

HPS Internal Oscillator Frequency

Table 75. HPS Internal Oscillator Frequency

For specification status, see the *Data Sheet Status* table

Description	Min	Typ	Max	Unit
Internal oscillator frequency	150	300	400	MHz

HPS PLL Specifications

Table 76. HPS PLL Input Requirements

The main HPS PLL receives its clock signals from the HPS_OSC_CLK pin. Refer to the related information for details about assigning this pin.

For specification status, see the *Data Sheet Status* table

Description	Min	Typ	Max	Unit
Clock input range	25	—	125	MHz
Clock input accuracy	—	—	50	ppm
Clock input duty cycle	45	50	55	%

Table 77. HPS PLL Performance

For specification status, see the *Data Sheet Status* table

Description	Min	Max	Unit
Main PLL VCO output	—	3,000	MHz
Peripheral PLL VCO output	—	3,000	MHz
h2f_user0_clk[96]	—	500	MHz
h2f_user1_clk[96]	—	500	MHz

Related Information

Intel Agilex 7 Device Family Pin Connection Guidelines: F-Series and I-Series
Provides more information about the HPS_OSC_CLK pin assignment.

(96) The HPS PLL provides this clock to the FPGA fabric.

HPS Cold Reset

Table 78. HPS Cold Reset

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Max	Unit
t_{RST0}	Minimum time for HPS_COLD_nRESET asserted(97)	3	—	ms

HPS SPI Timing Characteristics

Table 79. SPI Master Timing Requirements

You can adjust the input delay timing by programming the `rx_sample_dly` register.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
$T_{spi\_ref\_clk}$	The period of the SPI internal reference clock, sourced from `l4_main_clk`	2.5	—	—	ns
T_{clk}	SPIM_CLK clock period	16.67	—	—	ns
$T_{dutycycle}$	SPIM_CLK duty cycle	45	50	55	%
T_{ck_jitter}	SPIM_CLK output jitter	—	—	2	%
T_{dio}	Master-out slave-in (MOSI) output skew	–3	—	2	ns
$T_{dssfrst}$ (98)	SPI_SS_N asserted to first SPIM_CLK edge	$(1.5 \times T_{clk}) - 2$	—	—	ns

continued...

(97) HPS_COLD_nRESET may be ignored if HPS is not running or if the device is being configured.

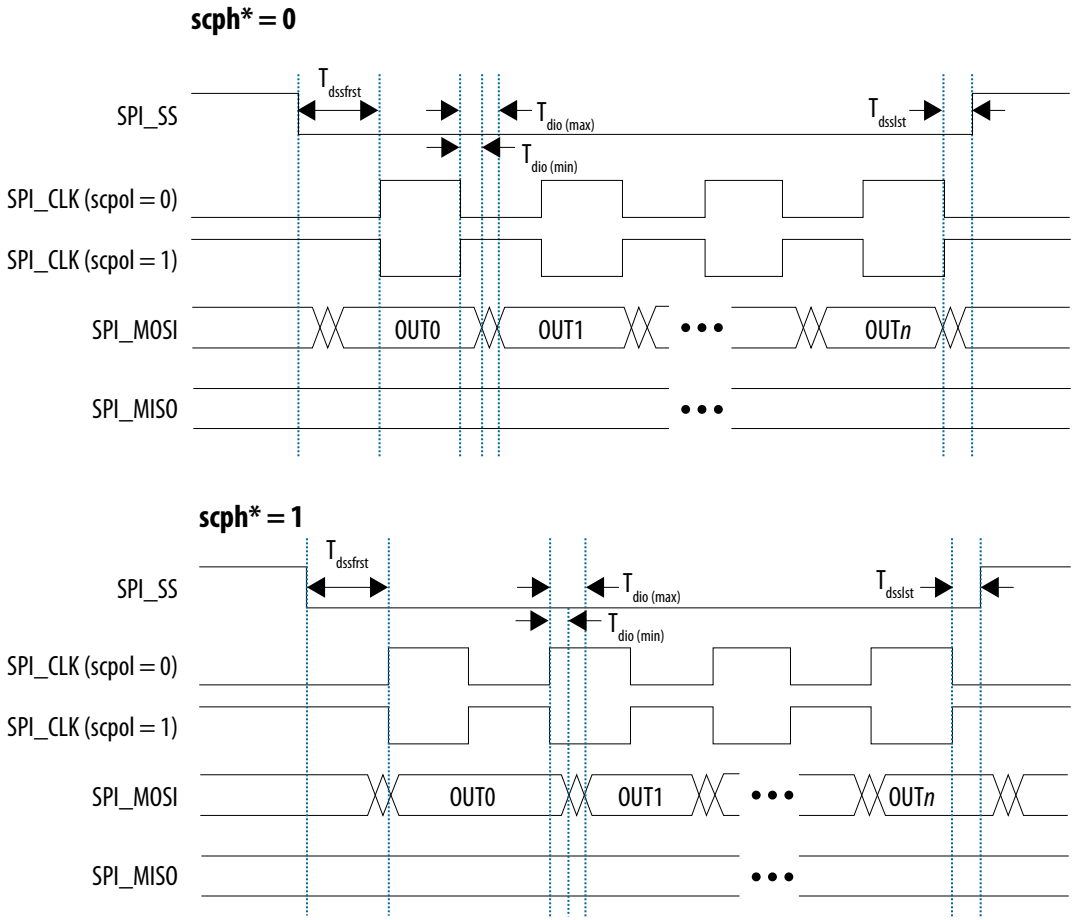
(98) SPI_SS_N behavior differs depending on Motorola SPI, TI SSP, or Microwire operational mode.

Symbol	Description	Min	Typ	Max	Unit
T_{dsslst} (98)	Last SPIM_CLK edge to SPI_SS_N deasserted	T_{clk} – 2	—	—	ns
T_{su} (99)	SPIM_MISO setup time with respect to SPIM_CLK capture edge	5.0 – (`rx_sample_dly` × $T_{spi\_ref\_clk}$)(100)	—	—	ns
T_h (99)	Input hold in respect to SPIM_CLK capture edge	1.3 + (`rx_sample_dly` × $T_{spi\_ref\_clk}$)	—	—	ns

(99) The capture edge differs depending on the operational mode. For Motorola SPI, the capture edge can be the rising or falling edge depending on the `scpol` register bit; for TI SSP, the capture edge is the falling edge; for Microwire, the capture edge is the rising edge.

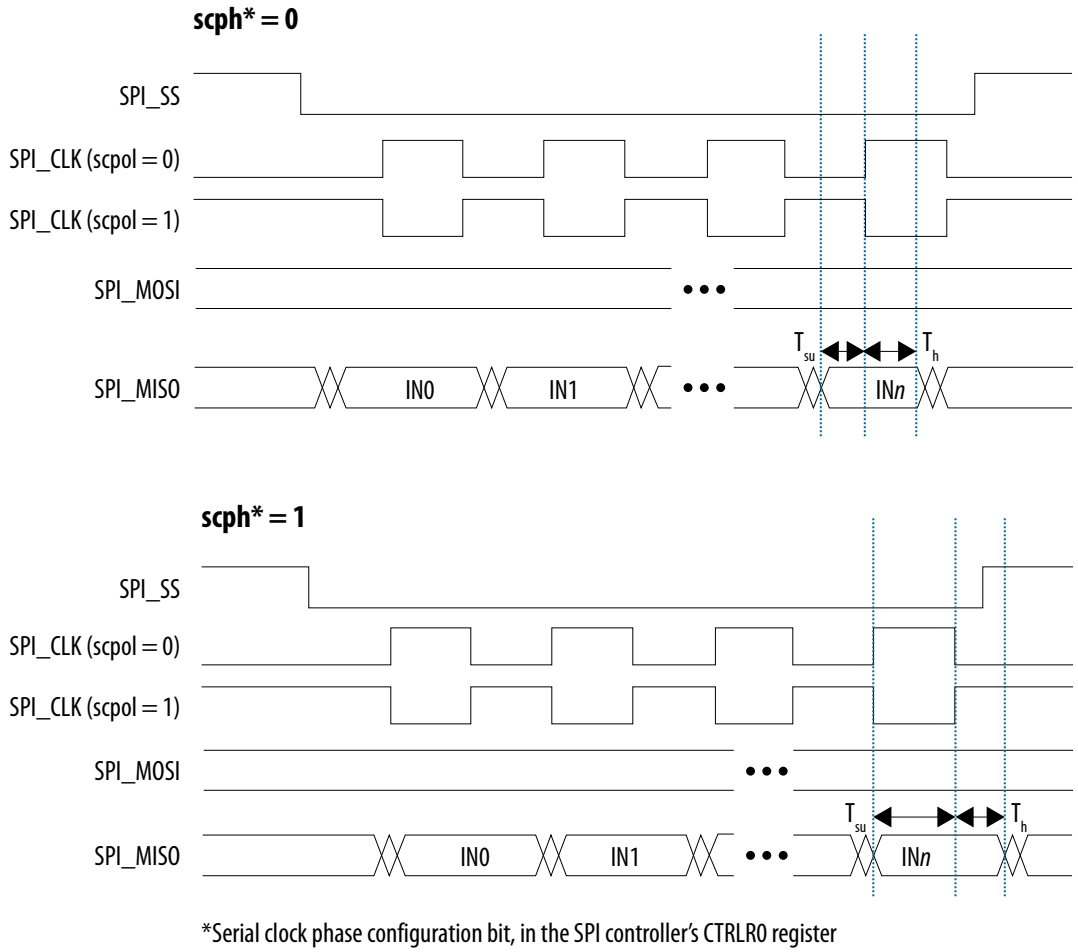
(100) Valid values of `rx_sample_dly` range from 1 to 64 (units are in $T_{spi\_ref\_clk}$ steps).

Figure 4. SPI Master Output Timing Diagram



*Serial clock phase configuration bit, in the SPI controller's CTRLR0 register

Figure 5. SPI Master Input Timing Diagram



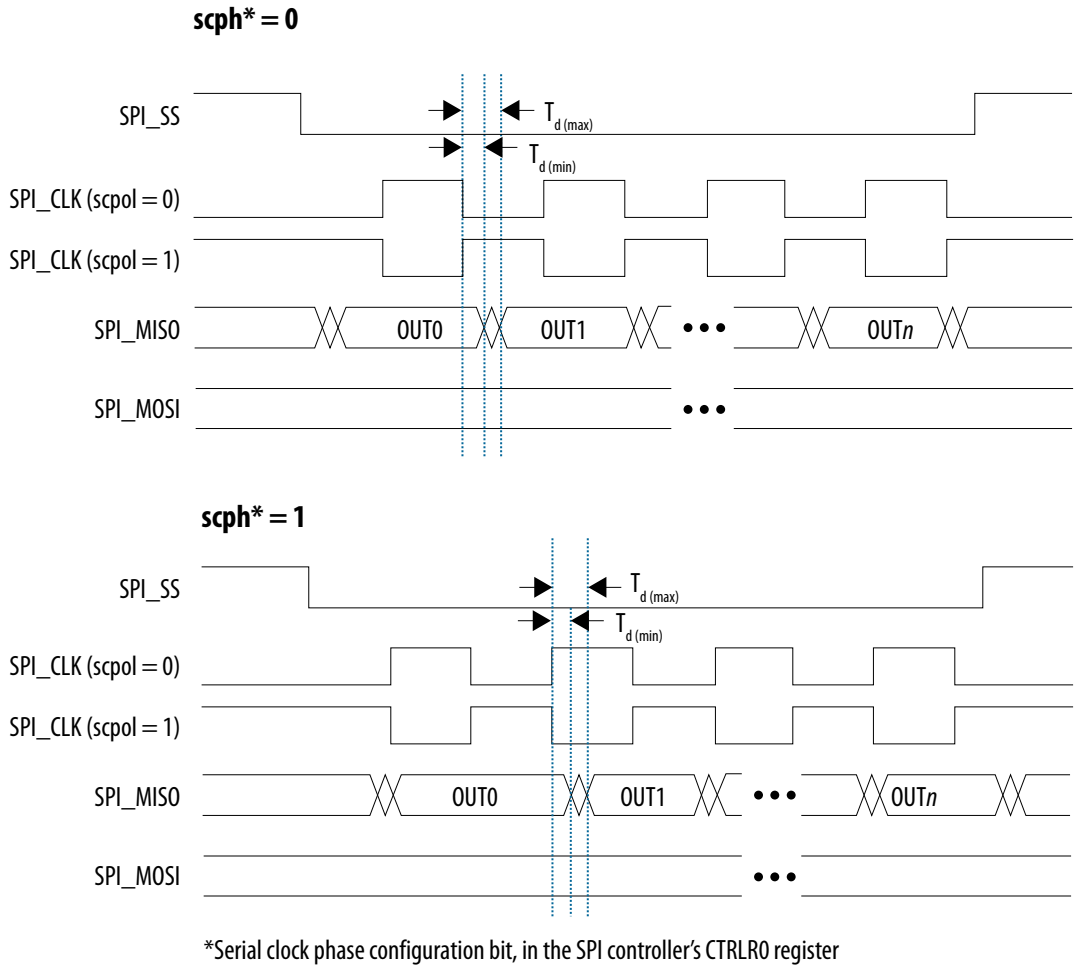
*Serial clock phase configuration bit, in the SPI controller's CTRLR0 register

Table 80. SPI Slave Timing Requirements

For specification status, see the *Data Sheet Status* table

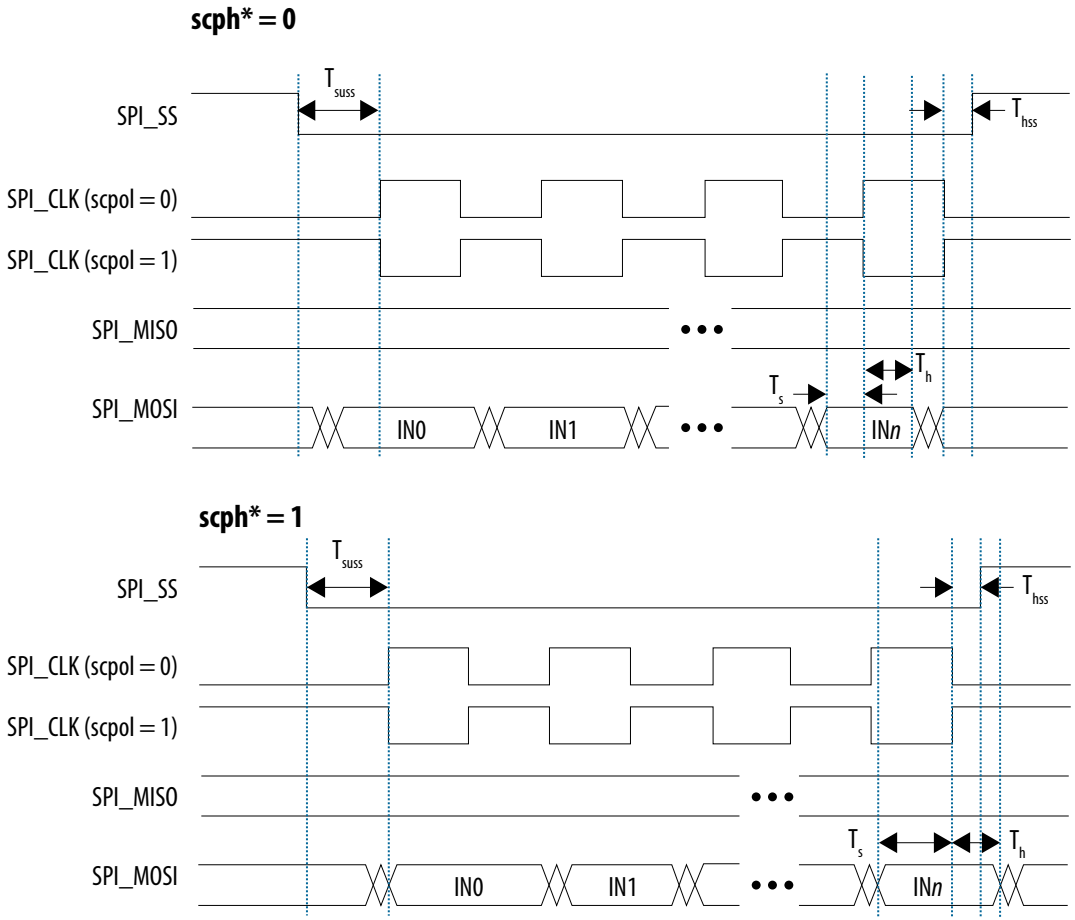
Symbol	Description	Min	Typ	Max	Unit
$T_{spi\_ref\_clk}$	The period of the SPI internal reference clock, sourced from `l4_main_clk`	2.5	—	—	ns
T_{clk}	SPIM_CLK clock period	30	—	—	ns
$T_{dutycycle}$	SPIM_CLK duty cycle	45	50	55	%
T_d	Master-in slave-out (MISO) output skew	$(2 \times T_{spi\_ref\_clk}) + 3$	—	$(3 \times T_{spi\_ref\_clk}) + 11$	ns
T_{su}	Master-out slave-in (MOSI) setup time	4	—	—	ns
T_h	Master-out slave-in (MOSI) hold time	9	—	—	ns
T_{suss}	SPI_SS_N asserted to first SPIM_CLK edge	$T_{spi\_ref\_clk} + 4.2$	—	—	ns
T_{hss}	Last SPIM_CLK edge to SPI_SS_N deasserted	$T_{spi\_ref\_clk} + 4.2$	—	—	ns

Figure 6. SPI Slave Output Timing Diagram



*Serial clock phase configuration bit, in the SPI controller's CTRLR0 register

Figure 7. SPI Slave Input Timing Diagram



*Serial clock phase configuration bit, in the SPI controller's CTRLR0 register

HPS SD/MMC Timing Characteristics

Table 81. HPS Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements

These timings apply to SD, MMC, and embedded MMC (eMMC) cards operating at 1.8 V.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{sdmmc_cclk}	SDMMC_CCLK clock period (Identification mode)	2,500	—	—	ns
	SDMMC_CCLK clock period (SDR12)	40	—	—	ns
	SDMMC_CCLK clock period (SDR25)	20	—	—	ns
$T_{dutycycle}$	SDMMC_CCLK duty cycle	45	50	55	%
$T_{sdmmc\_cclk\_jitter}$	SDMMC_CCLK output jitter	—	—	2	%
T_{sdmmc_clk}	Internal reference clock before division by 4	5	—	—	ns
T_d	SDMMC_CMD/ SDMMC_DATA[7:0] output delay(101)	$-0.5 + T_{sdmmc\_clk} \times$ drvsel/2	—	$2.5 + (T_{sdmmc\_clk} \times$ drvsel/2)	ns
T_{su}	SDMMC_CMD/ SDMMC_DATA[7:0] input setup(102)	$6 - (T_{sdmmc\_clk} \times$ smplsel/2)	—	—	ns
T_h	SDMMC_CMD/ SDMMC_DATA[7:0] input hold(102)	$0.5 + (T_{sdmmc\_clk} \times$ smplsel/2)	—	—	ns

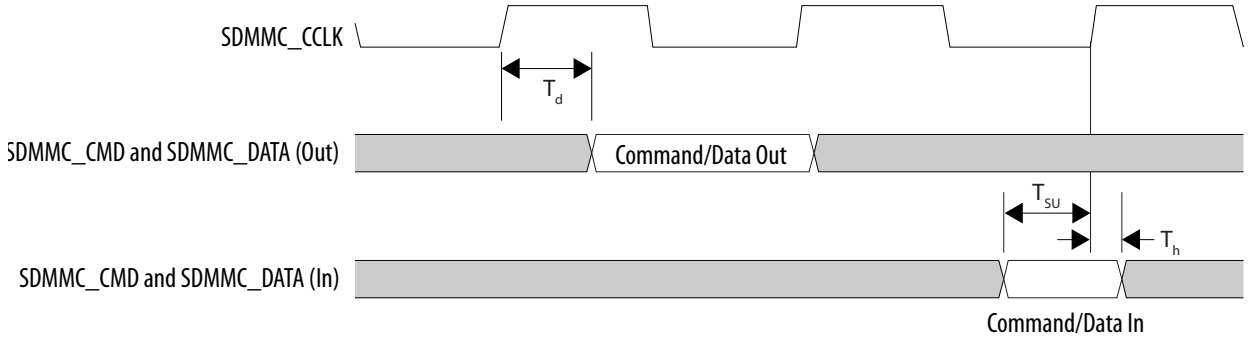
None of the HPS I/Os supports 3 V mode, while SD/MMC cards must operate at 3 V at power on. eMMC devices can operate at 1.8 V at power on.

(101) When the drvsel bitfield in the sdmmc register is set to 3 (in the system manager) and the reference clock (sdmmc_clk) is 200 MHz for example, the output delay time is 7.5 to 10.5 ns.

(102) When the smplsel bitfield in the sdmmc register is set to 2 (in the system manager) and the reference clock (sdmmc_clk) is 200 MHz for example, the setup time is 1 ns and the hold time is 5.5 ns.

Note: SD cards power up at 3 V. To support SD, your design must include a level shifter between the SD card and the HPS SD/MMC interface.

Figure 8. SD/MMC Timing Diagram



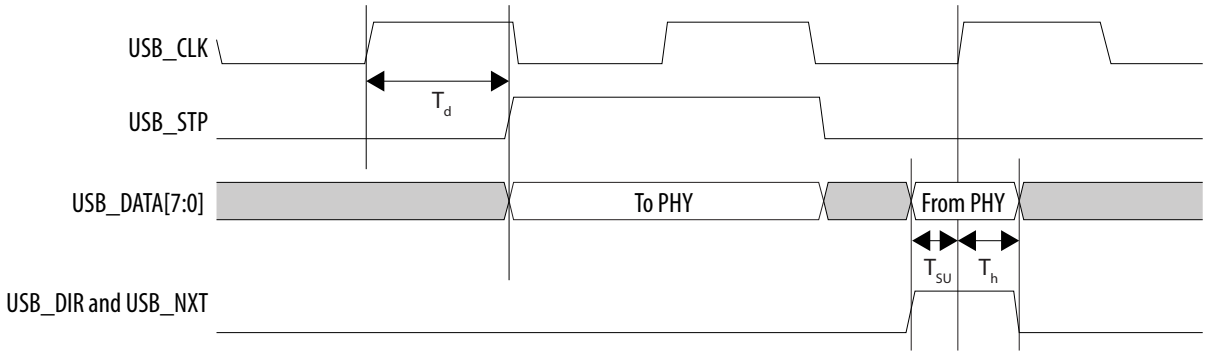
HPS USB UPLI Timing Characteristics

Table 82. HPS USB 2.0 Transceiver Macrocell Interface Plus (UTMI+) Low Pin Interface (ULPI) Timing Requirements

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{usb_clk}	USB_CLK clock period	—	16.667	—	ns
T_d	Clock to USB_STP/ USB_DATA[7:0] output delay	2	—	7	ns
T_{su}	Setup time for USB_DIR/ USB_NXT/USB_DATA[7:0]	4	—	—	ns
T_h	Hold time for USB_DIR/ USB_NXT/USB_DATA[7:0]	4	—	—	ns

Figure 9. USB ULPI Timing Diagram



Note: The USB interface supports single data rate (SDR) timing only.

HPS Ethernet Media Access Controller (EMAC) Timing Characteristics

Table 83. Reduced Gigabit Media Independent Interface (RGMII) TX Timing Requirements

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{clk} (1000Base-T)	TX_CLK clock period	—	8	—	ns
T_{clk} (100Base-T)	TX_CLK clock period	—	40	—	ns
T_{clk} (10Base-T)	TX_CLK clock period	—	400	—	ns
$T_{dutycycle}$ (1000Base-T)	TX_CLK duty cycle	45	50	55	%
$T_{dutycycle}$ (10/100Base-T)	TX_CLK duty cycle	40	50	60	%
T_d (103) (104)	TXD/TX_CTL to TX_CLK output skew	–0.5	—	0.5	ns

(103) Rise and fall times depend on the I/O standard, drive strength, and loading. Intel recommends simulating your configuration.

(104) If you connect a PHY that does not implement clock-to-data skew, you can delay TX_CLK by 1.5—2.0 ns with the HPS I/O programmable delay, to meet the PHY's 1-ns data-to-clock skew requirement.

Figure 10. RGMII TX Timing Diagram

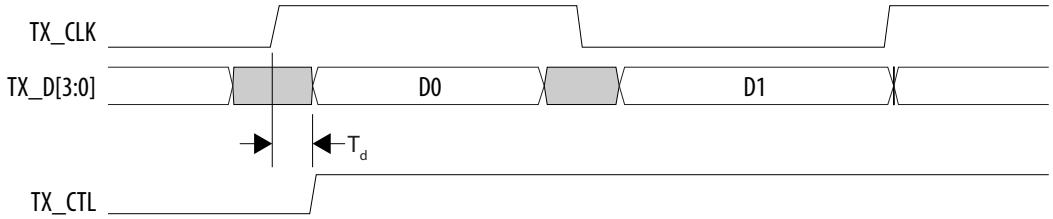


Table 84. RGMII RX Timing Requirements

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{clk} (1000Base-T)	RX_CLK clock period	—	8	—	ns
T_{clk} (100Base-T)	RX_CLK clock period	—	40	—	ns
T_{clk} (10Base-T)	RX_CLK clock period	—	400	—	ns
$T_{dutycycle}$ (1000Base-T)	RX_CLK duty cycle	45	50	55	%
$T_{dutycycle}$ (10/100Base-T)	RX_CLK duty cycle	40	50	60	%
T_{su}	RX_D/RX_CTL to RX_CLK setup time	1	—	—	ns
T_h (105)	RX_CLK to RX_D/RX_CTL hold time	1	—	—	ns

(105) If you connect a PHY that does not implement clock-to-data skew, you can meet the HPS EMAC's 1 ns setup time by delaying RX_CLK by 1.5-2 ns, using the HPS I/O programmable delay.

Figure 11. RGMII RX Timing Diagram

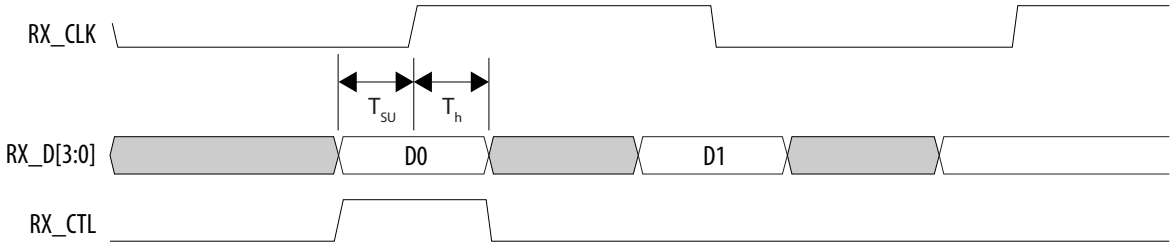


Table 85. Reduced Media Independent Interface (RMII) Clock Timing Requirements

For specification status, see the *Data Sheet Status* table

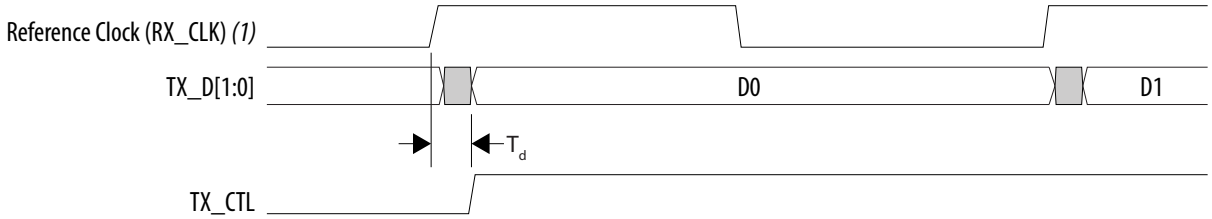
Symbol	Description	Min	Typ	Max	Unit
T_{clk}	REF_CLK clock period, sourced by HPS TX_CLK	—	20	—	ns
	REF_CLK clock period, sourced by external clock source	—	20	—	ns
$T_{dutycycle\_int}$	Clock duty cycle, REF_CLK sourced by TX_CLK	35	50	65	%
$T_{dutycycle\_ext}$	Clock duty cycle, REF_CLK sourced by external clock source	35	50	65	%

Table 86. RMII TX Timing Requirements

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_d	TX_CLK to TXD/TX_CTL output data delay	2	—	10	ns

Figure 12. RMII TX Timing Diagram



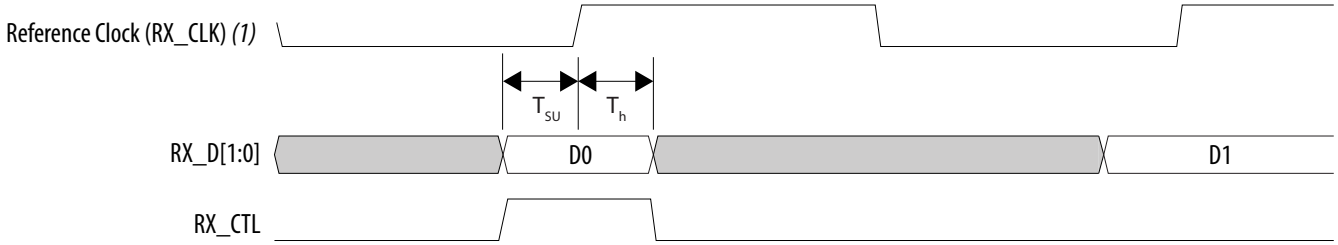
Note:
1. For RMII mode, RX_CLK is always used as the reference clock. Refer to the related information for example system-level topologies.

Table 87. RMII RX Timing Requirements

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{su}	RX_D/RX_CTL setup time	2	—	—	ns
T_h	RX_D/RX_CTL hold time	1	—	—	ns

Figure 13. RMII RX Timing Diagram



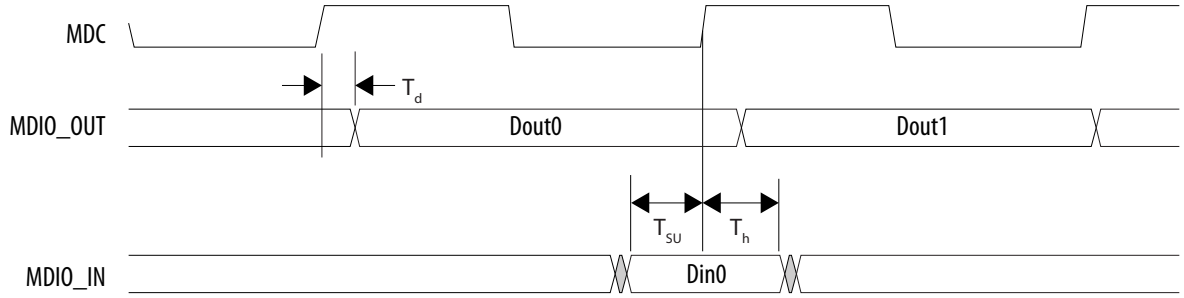
Note:
1. For RMII mode, RX_CLK is always used as the reference clock. Refer to the related information for example system-level topologies.

Table 88. Management Data Input/Output (MDIO) Timing Requirements

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	MDC clock period	400	—	—	ns
T_d	MDC to MDIO output data delay	10	—	300	ns
T_{su}	Setup time for MDIO data	10	—	—	ns
T_h	Hold time for MDIO data	0	—	—	ns

Figure 14. MDIO Timing Diagram



Related Information

HPS-to-PHY Interface Diagrams section, Intel Agilex 7 Hard Processor System Technical Reference Manual
Provides the example system-level topologies.

HPS I²C Timing Characteristics

Table 89. HPS I²C Timing Requirements

For specification status, see the *Data Sheet Status* table

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
T_{clk}	Serial clock (SCL) clock period	10	—	2.5	—	µs
T_{clk_jitter}	I²C clock output jitter	—	2	—	2	%
T_{HIGH} (106)	SCL high period	4(107)	—	0.6(108)	—	µs
T_{LOW} (109)	SCL low period	4.7(110)	—	1.3(111)	—	µs
$T_{SU;DAT}$	Setup time for serial data line (SDA) data to SCL	0.25	—	0.1	—	µs
$T_{HD;DAT}$ (112)	Hold time for SCL to SDA data	0	3.15	0	0.6	µs
$T_{VD;DAT}$ and $T_{VD;ACK}$ (113)	SCL to SDA output data delay	—	3.45(114)	—	0.9(115)	µs

continued...

(106) You can adjust T_{high} using the `ic_ss_scl_hcnt` or `ic_fs_scl_hcnt` register.

(107) The recommended minimum setting for `ic_ss_scl_hcnt` is 428. Refer to the related information for the SCL_High_time equation.

(108) The recommended minimum setting for `ic_fs_scl_hcnt` is 75. Refer to the related information for the SCL_High_time equation.

(109) You can adjust T_{low} using the `ic_ss_scl_lcnt` or `ic_fs_scl_lcnt` register.

(110) The recommended minimum setting for `ic_ss_scl_lcnt` is 464. Refer to the related information for the SCL_Low_time equation.

(111) The recommended minimum setting for `ic_fs_scl_lcnt` is 163. Refer to the related information for the SCL_Low_time equation.

(112) $T_{HD;DAT}$ is affected by the rise and fall time.

(113) $T_{VD;DAT}$ and $T_{VD;ACK}$ are affected by the rise and fall time, as well as the SDA hold time (set by adjusting the `ic_sda_hold` register).

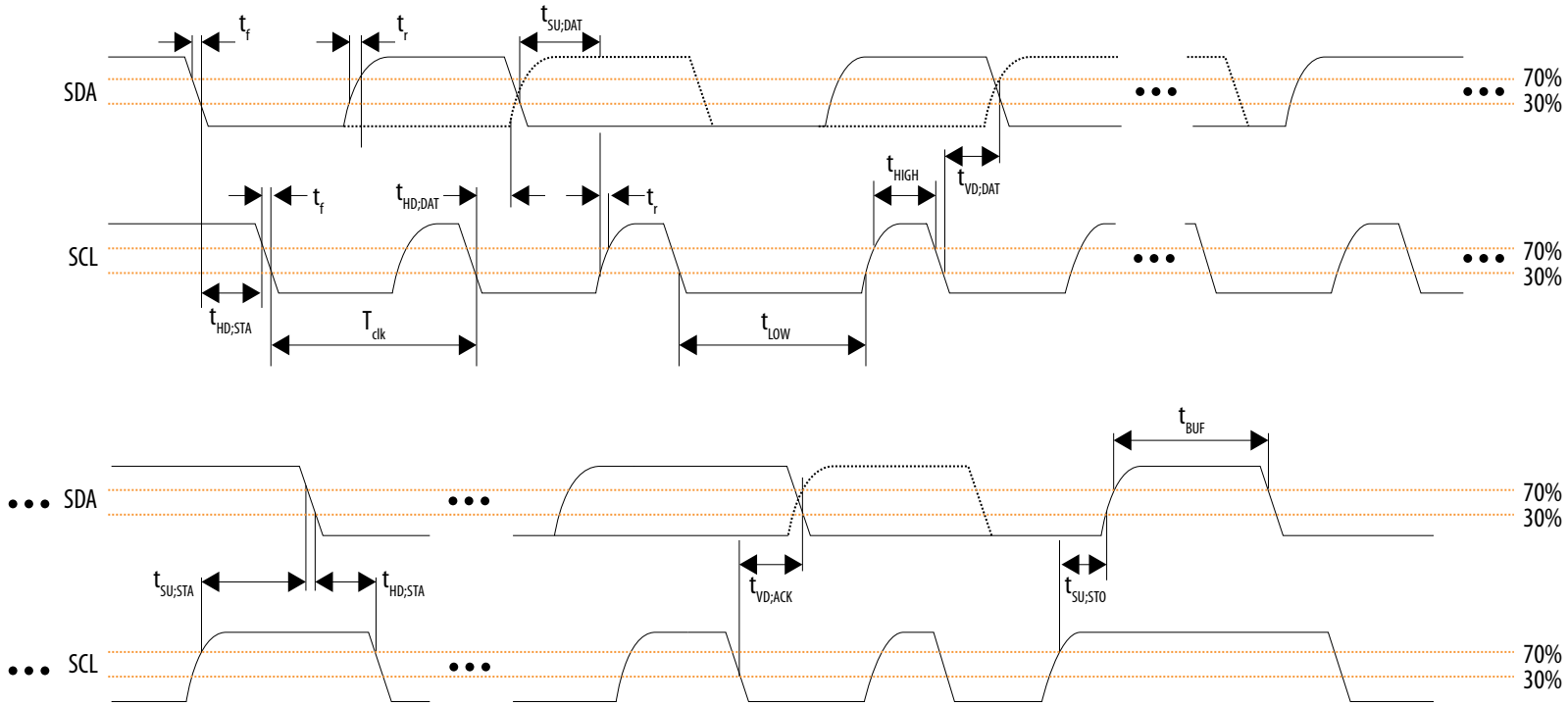
Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
$T_{SU;STA}$	Setup time for a repeated start condition	4.7	—	0.6	—	µs
$T_{HD;STA}$	Hold time for a repeated start condition	4	—	0.6	—	µs
$T_{SU;STO}$	Setup time for a stop condition	4	—	0.6	—	µs
T_{BUF}	SDA high pulse duration between STOP and START	4.7	—	1.3	—	µs
$T_{scl:r}$ (116)	SCL rise time	—	1,000	20	300	ns
$T_{scl:f}$ (116)	SCL fall time	—	300	6.54	300	ns
$T_{sda:r}$ (116)	SDA rise time	—	1,000	20	300	ns
$T_{sda:f}$ (116)	SDA fall time	—	300	6.54	300	ns

(114) Use maximum SDA_HOLD = 240 to be within the specification.

(115) Use maximum SDA_HOLD = 60 to be within the specification.

(116) Rise and fall time parameters vary depending on external factors such as the characteristics of the I/O driver, pull-up resistor value, and total capacitance on the transmission line.

Figure 15. I²C Timing Diagram



Related Information

Clock Synchronization section, Intel Agilex 7 Hard Processor System Technical Reference Manual
Provides the SCL high and low time equations.

HPS NAND Timing Characteristics

Table 90. HPS NAND ONFI 1.0 Timing Requirements

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Max	Unit
T_{WP} (117)	Write enable pulse width	10	—	ns
T_{WH} (117)	Write enable hold time	7	—	ns
T_{RP} (117)	Read enable pulse width	10	—	ns
T_{REH} (117)	Read enable hold time	7	—	ns
T_{CLS} (117)	Command latch enable to write enable setup time	10	—	ns
T_{CLH} (117)	Command latch enable to write enable hold time	5	—	ns
T_{CS} (117)	Chip enable to write enable setup time	15	—	ns
T_{CH} (117)	Chip enable to write enable hold time	5	—	ns
T_{ALS} (117)	Address latch enable to write enable setup time	10	—	ns
T_{ALH} (117)	Address latch enable to write enable hold time	5	—	ns
T_{DS} (117)	Data to write enable setup time	7	—	ns
T_{DH} (117)	Data to write enable hold time	5	—	ns
T_{WB} (117)	Write enable high to R/B low	—	200	ns
T_{CEA}	Chip enable to data access time	—	100	ns

continued...

(117) This timing is software programmable. Refer to the related information for more information about software-programmable timing in the NAND flash controller.

Symbol	Description	Min	Max	Unit
T_{REA}	Read enable to data access time	—	40	ns
T_{RHZ}	Read enable to data high impedance	—	200	ns
T_{RR}	Ready to read enable low	20	—	ns

Figure 16. NAND Command Latch Timing Diagram

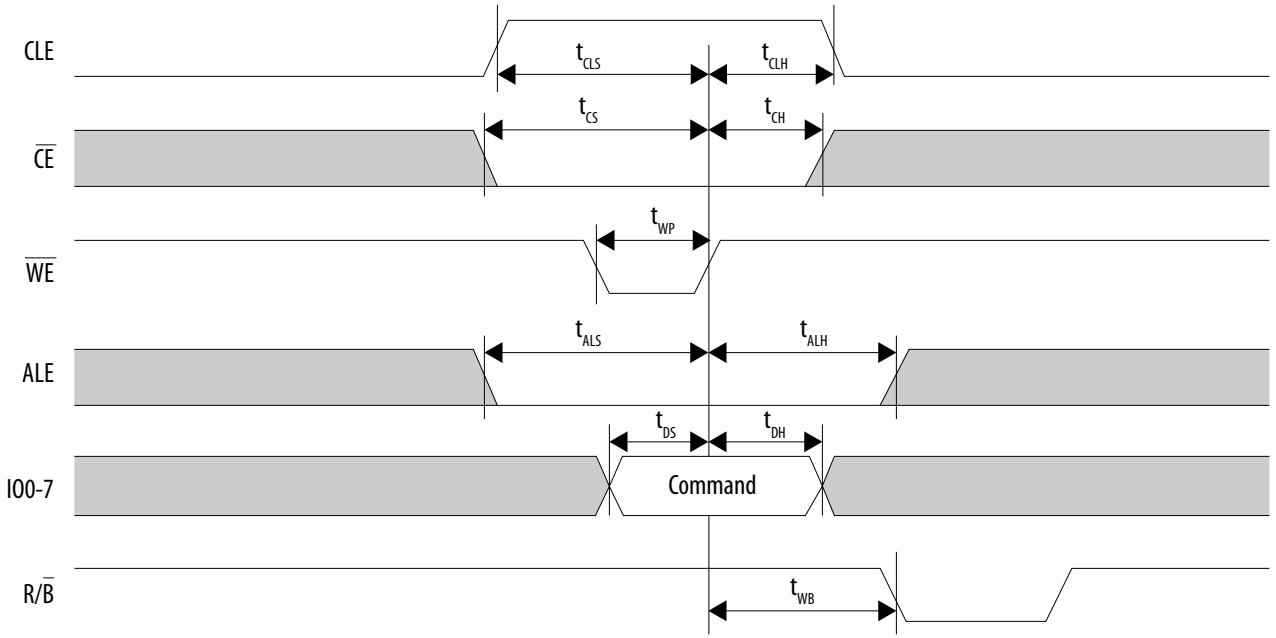


Figure 17. NAND Address Latch Timing Diagram

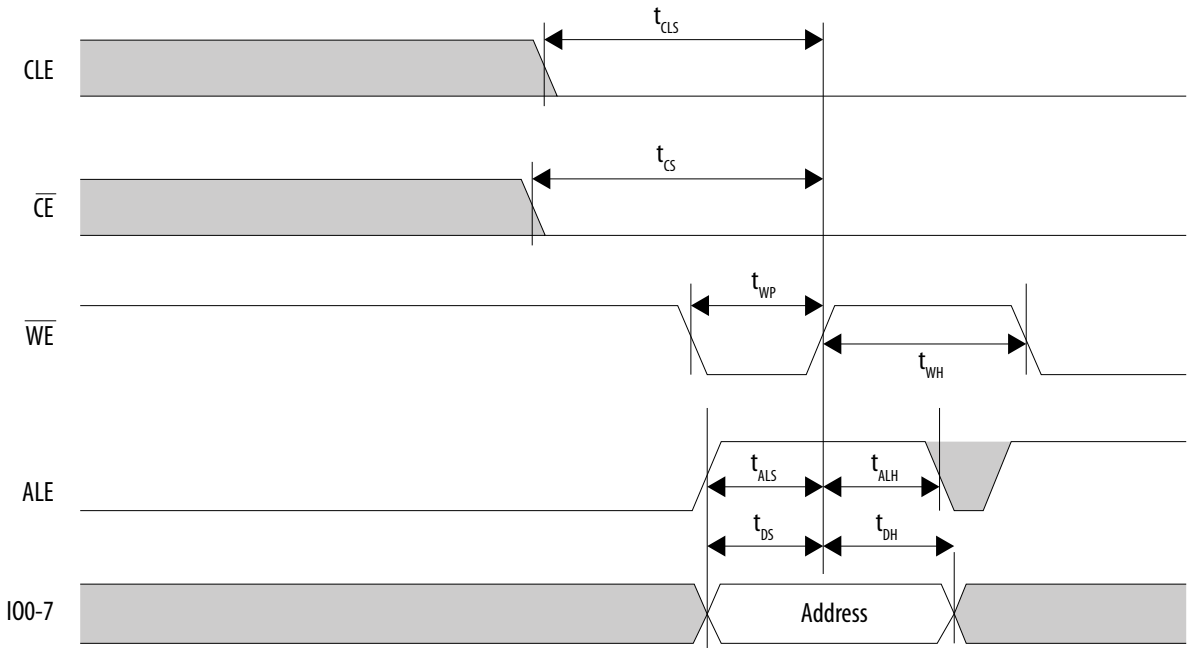


Figure 18. NAND Data Output Cycle Timing Diagram

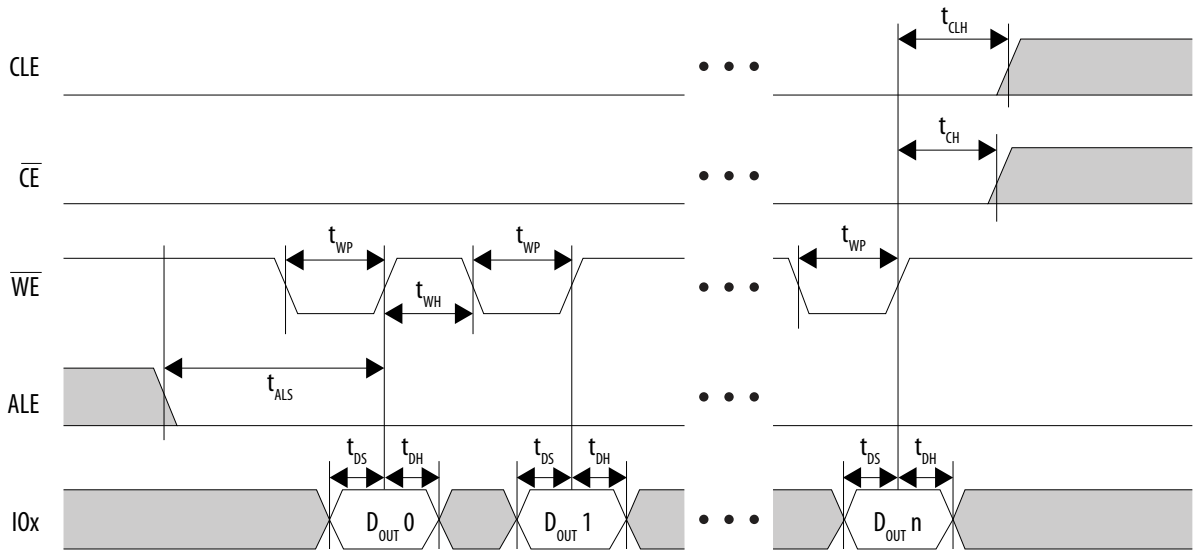


Figure 19. NAND Data Input Cycle Timing Diagram

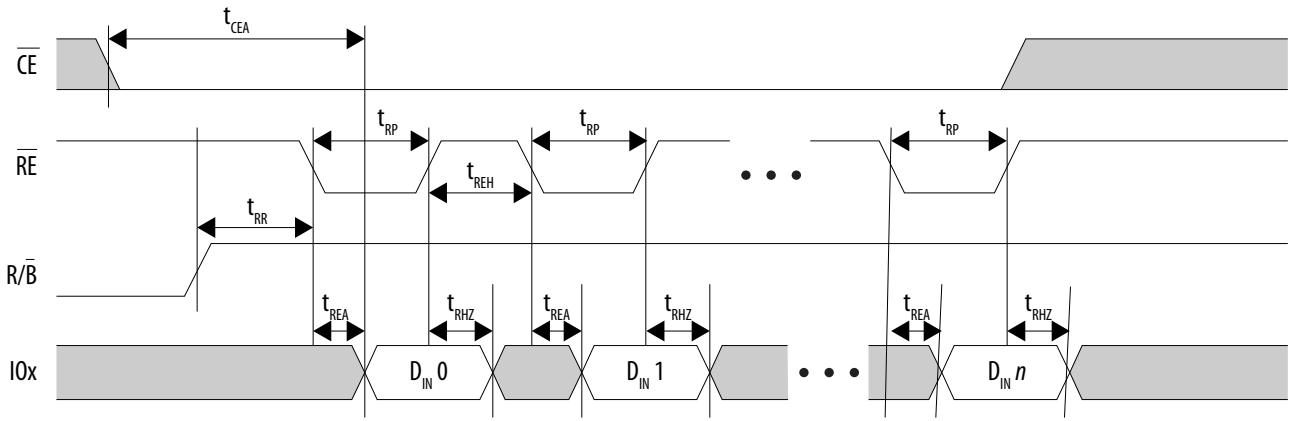


Figure 20. NAND Data Input Timing Diagram for Extended Data Output (EDO) Cycle

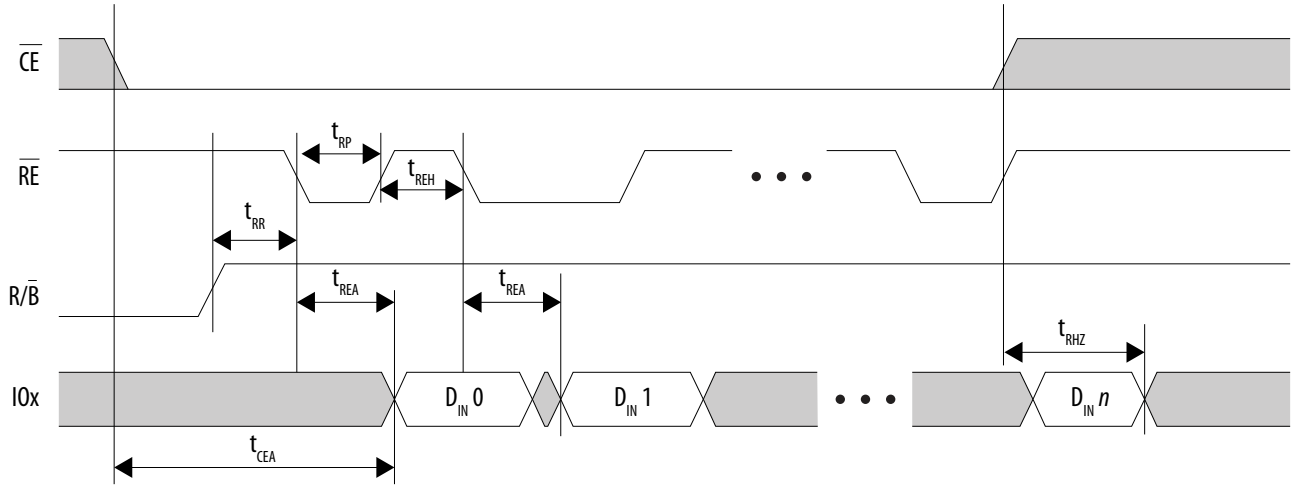


Figure 21. NAND Read Status Timing Diagram

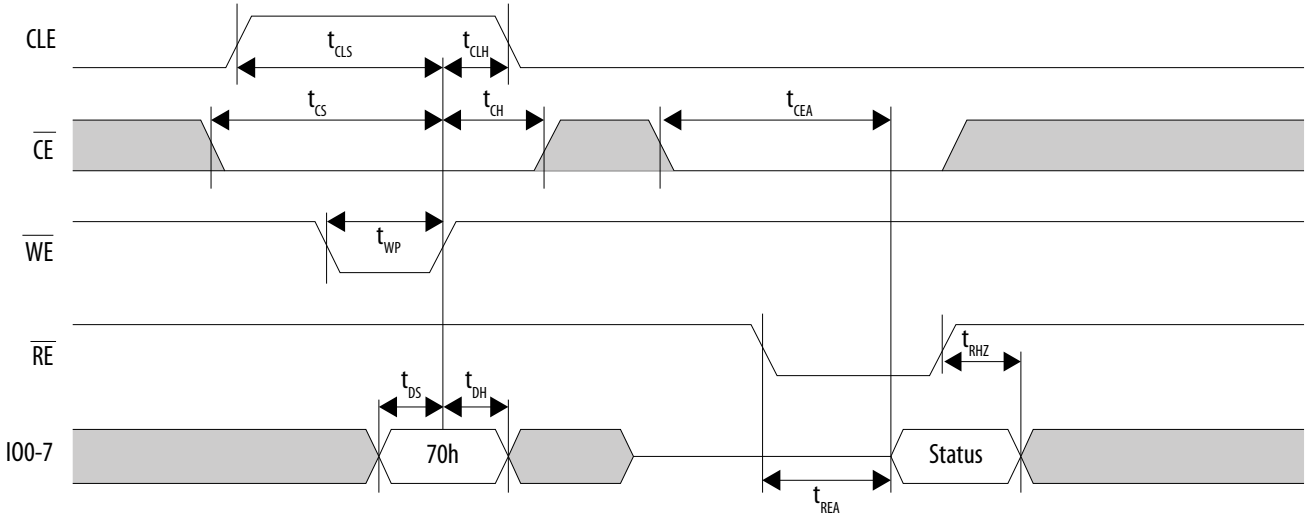
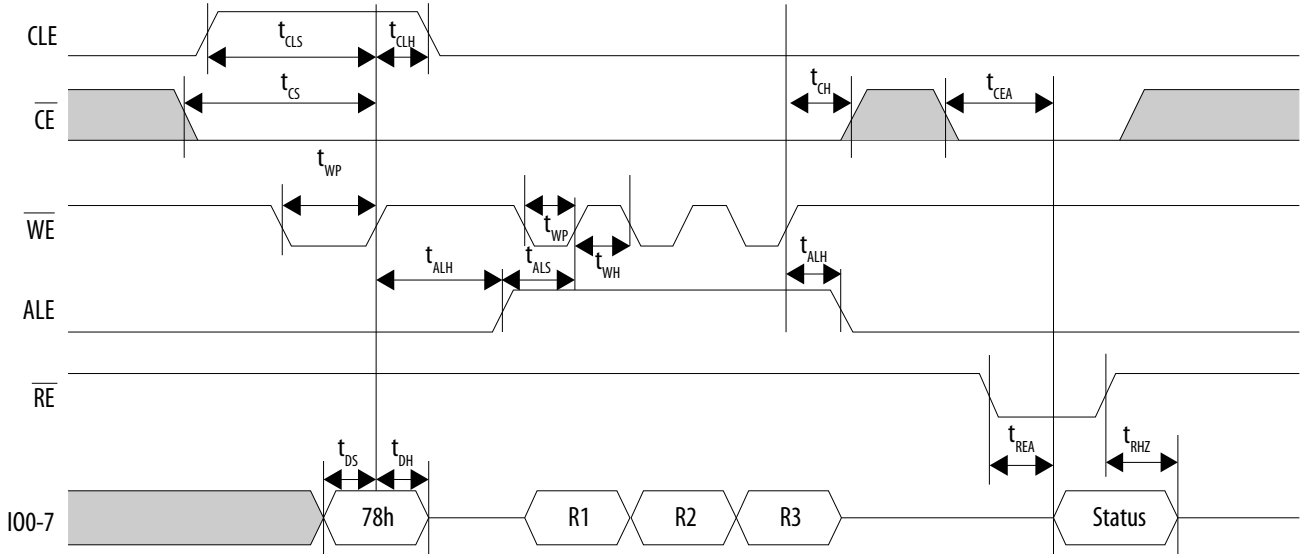


Figure 22. NAND Read Status Enhanced Timing Diagram



Related Information

NAND Flash Controller section, Intel Agilex 7 Hard Processor System Technical Reference Manual
Provides more information about software-programmable timing in the NAND flash controller.

HPS Trace Timing Characteristics

Table 91. Trace Timing Requirements

To increase the trace bandwidth, Intel recommends routing the trace interface to the FPGA in the HPS Platform Designer component. The FPGA trace interface offers a 64-bit single data rate path that can be converted to double data rate to minimize FPGA I/O usage.

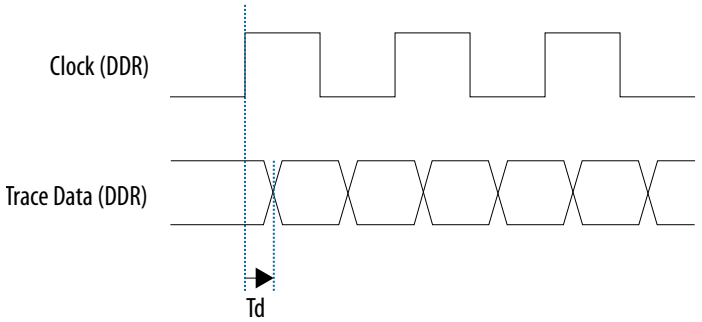
Depending on the trace module that you connect to the HPS trace interface, you may need to include board termination to achieve the maximum sampling speed possible. Refer to your trace module data sheet for termination recommendations.

Most trace modules implement programmable clock and data skew, to improve trace data timing margins. Alternatively, you can change the clock-to-data timing relationship with the HPS programmable I/O delay.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	Trace clock period	6.667	—	—	ns
T_{clk_jitter}	Trace clock output jitter	—	—	2	%
$T_{dutycycle}$	Trace clock maximum duty cycle	45	50	55	%
T_d	T_{clk} to D0–D15 output data delay	–0.5	—	1.3	ns

Figure 23. Trace Timing Diagram



HPS GPIO Interface

The general-purpose I/O (GPIO) interface has debounce circuitry included to remove signal glitches. The debounce clock frequency ranges from 125 Hz to 32 kHz. The minimum pulse width is 1 debounce clock cycle and the minimum detectable GPIO pulse width is 62.5 µs (at 32 kHz).

If the external signal is driven into the GPIO for less than one clock cycle, the external signal is filtered. If the external signal is between one and two clock cycles, the external signal may or may not be filtered depending on the phase of the signal. If the external signal is more than two clock cycles, the external signal is not filtered.

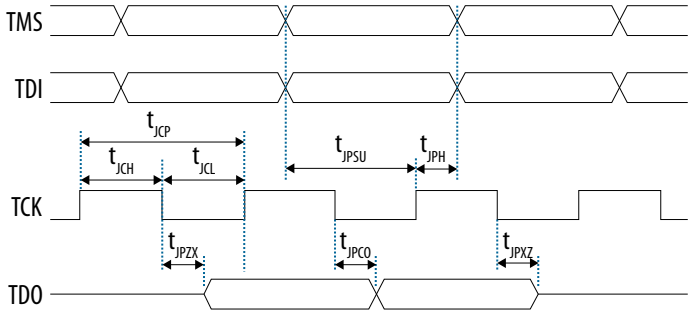
HPS JTAG Timing Characteristics

Table 92. HPS JTAG Timing Requirements

For specification status, see the *Data Sheet Status* table

Symbol	Description	Min	Typ	Max	Unit
t_{JCP}	TCK clock period	41.66	—	—	ns
t_{JCH}	TCK clock high time	20	—	—	ns
t_{JCL}	TCK clock low time	20	—	—	ns
$t_{JPSU\ (TDI)}$	TDI JTAG port setup time	5	—	—	ns
$t_{JPSU\ (TMS)}$	TMS JTAG port setup time	5	—	—	ns
t_{JPH}	JTAG port hold time	0.5	—	—	ns
t_{JPCO}	JTAG port clock to output	0	—	8	ns
t_{JPZX}	JTAG port high impedance to valid output	—	—	10	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	—	10	ns

Figure 24. HPS JTAG Timing Diagram



HPS Programmable I/O Timing Characteristics

Table 93. HPS Programmable I/O Delay (Output Path)

For specification status, see the *Data Sheet Status* table

Name	output_val_en	output_val	Description	Min	Typ	Max	Unit
ZERO_CHAIN_DELAY	0	0	Intrinsic I/O delay. Bypasses the delay chain	—	0	—	ps
CHAIN_DELAY	1	0	Intrinsic I/O delay + Minimum + 0 × Chain Delay	—	0	—	ps
ONE_CHAIN_DELAY	1	1	Intrinsic I/O delay + Minimum + 1 × Chain Delay	—	422	—	ps
TWO_CHAIN_DELAY	1	2	Intrinsic I/O delay + Minimum + 2 × Chain Delay	—	518	—	ps
THREE_CHAIN_DELAY	1	3	Intrinsic I/O delay + Minimum + 3 × Chain Delay	—	607	—	ps
FOUR_CHAIN_DELAY	1	4	Intrinsic I/O delay + Minimum + 4 × Chain Delay	—	705	—	ps

continued...

Name	output_val_en	output_val	Description	Min	Typ	Max	Unit
FIVE_CHAIN_DELAY	1	5	Intrinsic I/O delay + Minimum + 5 × Chain Delay	—	786	—	ps
SIX_CHAIN_DELAY	1	6	Intrinsic I/O delay + Minimum + 6 × Chain Delay	—	874	—	ps
SEVEN_CHAIN_DELAY	1	7	Intrinsic I/O delay + Minimum + 7 × Chain Delay	—	955	—	ps
EIGHT_CHAIN_DELAY	1	8	Intrinsic I/O delay + Minimum + 8 × Chain Delay	—	1,042	—	ps
NINE_CHAIN_DELAY	1	9	Intrinsic I/O delay + Minimum + 9 × Chain Delay	—	1,126	—	ps
TEN_CHAIN_DELAY	1	10	Intrinsic I/O delay + Minimum + 10 × Chain Delay	—	1,214	—	ps
ELEVEN_CHAIN_DELAY	1	11	Intrinsic I/O delay + Minimum + 11 × Chain Delay	—	1,296	—	ps
TWELVE_CHAIN_DELAY	1	12	Intrinsic I/O delay + Minimum + 12 × Chain Delay	—	1,382	—	ps
THIRTEEN_CHAIN_DELAY	1	13	Intrinsic I/O delay + Minimum + 13 × Chain Delay	—	1,462	—	ps
FOURTEEN_CHAIN_DELAY	1	14	Intrinsic I/O delay + Minimum + 14 × Chain Delay	—	1,552	—	ps
FIFTEEN_CHAIN_DELAY	1	15	Intrinsic I/O delay + Minimum + 15 × Chain Delay	—	1,626	—	ps
—	1	[16:30]	INVALID	—	—	—	—
—	2	—	INVALID	—	—	—	—

continued...

Name	output_val_en	output_val	Description	Min	Typ	Max	Unit
—	3	[0:15]	INVALID	—	—	—	—
SIXTEEN_CHAIN_DELAY	3	16	Intrinsic I/O delay + Minimum + 16 × Chain Delay	—	1,798	—	ps
SEVENTEEN_CHAIN_DELAY	3	17	Intrinsic I/O delay + Minimum + 17 × Chain Delay	—	1,885	—	ps
EIGHTEEN_CHAIN_DELAY	3	18	Intrinsic I/O delay + Minimum + 18 × Chain Delay	—	1,967	—	ps
NINETEEN_CHAIN_DELAY	3	19	Intrinsic I/O delay + Minimum + 19 × Chain Delay	—	2,054	—	ps
TWENTY_CHAIN_DELAY	3	20	Intrinsic I/O delay + Minimum + 20 × Chain Delay	—	2,137	—	ps
TWENTYONE_CHAIN_DELAY	3	21	Intrinsic I/O delay + Minimum + 21 × Chain Delay	—	2,222	—	ps
TWENTYTWO_CHAIN_DELAY	3	22	Intrinsic I/O delay + Minimum + 22 × Chain Delay	—	2,305	—	ps
TWENTYTHREE_CHAIN_DELAY	3	23	Intrinsic I/O delay + Minimum + 23 × Chain Delay	—	2,395	—	ps
TWENTYFOUR_CHAIN_DELAY	3	24	Intrinsic I/O delay + Minimum + 24 × Chain Delay	—	2,475	—	ps
TWENTYFIVE_CHAIN_DELAY	3	25	Intrinsic I/O delay + Minimum + 25 × Chain Delay	—	2,564	—	ps
TWENTYSIX_CHAIN_DELAY	3	26	Intrinsic I/O delay + Minimum + 26 × Chain Delay	—	2,644	—	ps

continued...

Name	output_val_en	output_val	Description	Min	Typ	Max	Unit
TWENTYSEVEN_CHAIN_DELAY	3	27	Intrinsic I/O delay + Minimum + 27 × Chain Delay	—	2,732	—	ps
TWENTYEIGHT_CHAIN_DELAY	3	28	Intrinsic I/O delay + Minimum + 28 × Chain Delay	—	2,808	—	ps
TWENTYNINE_CHAIN_DELAY	3	29	Intrinsic I/O delay + Minimum + 29 × Chain Delay	—	2,901	—	ps
THIRTY_CHAIN_DELAY	3	30	Intrinsic I/O delay + Minimum + 30 × Chain Delay	—	2,979	—	ps

Table 94. HPS Programmable I/O Delay (Input Path)

For specification status, see the *Data Sheet Status* table

Name	input_val_en	input_val	Description	Min	Typ	Max	Unit
ZERO_CHAIN_DELAY	0	0	Intrinsic I/O delay. Bypasses the delay chain	—	0	—	ps
CHAIN_DELAY	1	0	Intrinsic I/O delay + Minimum + 0 × Chain Delay	—	0	—	ps
ONE_CHAIN_DELAY	1	1	Intrinsic I/O delay + Minimum + 1 × Chain Delay	—	422	—	ps
TWO_CHAIN_DELAY	1	2	Intrinsic I/O delay + Minimum + 2 × Chain Delay	—	518	—	ps
THREE_CHAIN_DELAY	1	3	Intrinsic I/O delay + Minimum + 3 × Chain Delay	—	607	—	ps
FOUR_CHAIN_DELAY	1	4	Intrinsic I/O delay + Minimum + 4 × Chain Delay	—	705	—	ps

continued...

Name	input_val_en	input_val	Description	Min	Typ	Max	Unit
FIVE_CHAIN_DELAY	1	5	Intrinsic I/O delay + Minimum + 5 × Chain Delay	—	786	—	ps
SIX_CHAIN_DELAY	1	6	Intrinsic I/O delay + Minimum + 6 × Chain Delay	—	874	—	ps
SEVEN_CHAIN_DELAY	1	7	Intrinsic I/O delay + Minimum + 7 × Chain Delay	—	955	—	ps
EIGHT_CHAIN_DELAY	1	8	Intrinsic I/O delay + Minimum + 8 × Chain Delay	—	1,042	—	ps
NINE_CHAIN_DELAY	1	9	Intrinsic I/O delay + Minimum + 9 × Chain Delay	—	1,126	—	ps
TEN_CHAIN_DELAY	1	10	Intrinsic I/O delay + Minimum + 10 × Chain Delay	—	1,214	—	ps
ELEVEN_CHAIN_DELAY	1	11	Intrinsic I/O delay + Minimum + 11 × Chain Delay	—	1,296	—	ps
TWELVE_CHAIN_DELAY	1	12	Intrinsic I/O delay + Minimum + 12 × Chain Delay	—	1,382	—	ps
THIRTEEN_CHAIN_DELAY	1	13	Intrinsic I/O delay + Minimum + 13 × Chain Delay	—	1,462	—	ps
FOURTEEN_CHAIN_DELAY	1	14	Intrinsic I/O delay + Minimum + 14 × Chain Delay	—	1,552	—	ps
FIFTEEN_CHAIN_DELAY	1	15	Intrinsic I/O delay + Minimum + 15 × Chain Delay	—	1,626	—	ps
—	1	[16:30]	INVALID	—	—	—	—
—	2	—	INVALID	—	—	—	—

continued...

Name	input_val_en	input_val	Description	Min	Typ	Max	Unit
—	3	[0:15]	INVALID	—	—	—	—
SIXTEEN_CHAIN_DELAY	3	16	Intrinsic I/O delay + Minimum + 16 × Chain Delay	—	1,798	—	ps
SEVENTEEN_CHAIN_DELAY	3	17	Intrinsic I/O delay + Minimum + 17 × Chain Delay	—	1,885	—	ps
EIGHTEEN_CHAIN_DELAY	3	18	Intrinsic I/O delay + Minimum + 18 × Chain Delay	—	1,967	—	ps
NINETEEN_CHAIN_DELAY	3	19	Intrinsic I/O delay + Minimum + 19 × Chain Delay	—	2,054	—	ps
TWENTY_CHAIN_DELAY	3	20	Intrinsic I/O delay + Minimum + 20 × Chain Delay	—	2,137	—	ps
TWENTYONE_CHAIN_DELAY	3	21	Intrinsic I/O delay + Minimum + 21 × Chain Delay	—	2,222	—	ps
TWENTYTWO_CHAIN_DELAY	3	22	Intrinsic I/O delay + Minimum + 22 × Chain Delay	—	2,305	—	ps
TWENTYTHREE_CHAIN_DELAY	3	23	Intrinsic I/O delay + Minimum + 23 × Chain Delay	—	2,395	—	ps
TWENTYFOUR_CHAIN_DELAY	3	24	Intrinsic I/O delay + Minimum + 24 × Chain Delay	—	2,475	—	ps
TWENTYFIVE_CHAIN_DELAY	3	25	Intrinsic I/O delay + Minimum + 25 × Chain Delay	—	2,564	—	ps
TWENTYSIX_CHAIN_DELAY	3	26	Intrinsic I/O delay + Minimum + 26 × Chain Delay	—	2,644	—	ps

continued...

Name	input_val_en	input_val	Description	Min	Typ	Max	Unit
TWENTYSEVEN_CHAIN_DELAY	3	27	Intrinsic I/O delay + Minimum + 27 × Chain Delay	—	2,732	—	ps
TWENTYEIGHT_CHAIN_DELAY	3	28	Intrinsic I/O delay + Minimum + 28 × Chain Delay	—	2,808	—	ps
TWENTYNINE_CHAIN_DELAY	3	29	Intrinsic I/O delay + Minimum + 29 × Chain Delay	—	2,901	—	ps
THIRTY_CHAIN_DELAY	3	30	Intrinsic I/O delay + Minimum + 30 × Chain Delay	—	2,979	—	ps

You can program the number of delay steps by adjusting the I/O Delay register (`io0_delay` through `io47_delay` for I/Os 0 through 47).

Configuration Specifications

General Configuration Timing Specifications

Table 95. General Configuration Timing Specifications

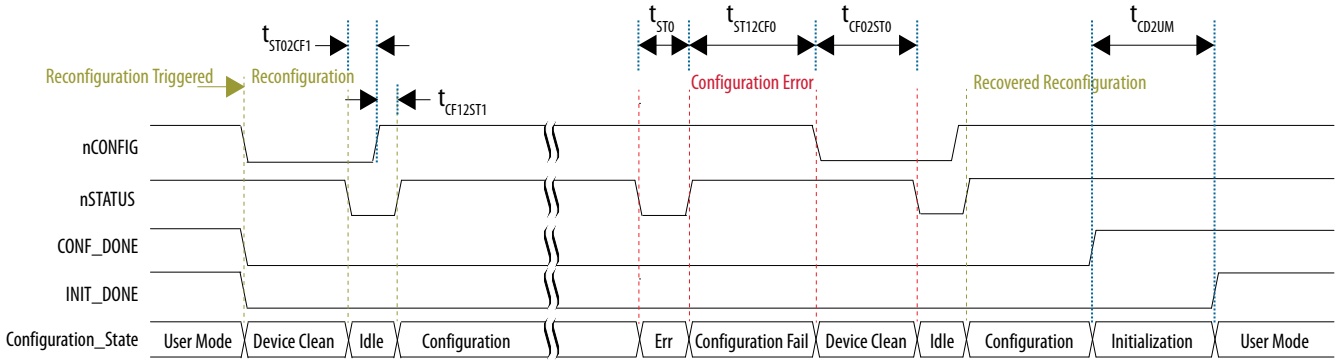
For specification status, see the *Data Sheet Status* table

Symbol	Description	Requirement		Unit
		Min	Max	
$t_{CF12ST1}$	nCONFIG high to nSTATUS high	—	20	ms
$t_{CF02ST0}$	nCONFIG low to nSTATUS low	—	400	ms
t_{ST0}	nSTATUS low pulse during configuration error	0.5	10	ms

continued...

Symbol	Description	Requirement		Unit
		Min	Max	
t_{CD2UM} (118)	CONF_DONE high to user mode	—	5	ms
$t_{ST12CF0}$	Minimum time to drive nCONFIG from high to low after nSTATUS transitions from low to high	0	—	ms
$t_{ST02CF1}$	Minimum time to drive nCONFIG from low to high after nSTATUS transitions from high to low	0	—	ms

Figure 25. General Configuration Timing Diagram



POR Specifications

Power-on reset (POR) delay is defined as the delay between the time when all the power supplies monitored by the POR circuitry reach the minimum recommended operating voltage to the time when the nSTATUS is released high and your device is ready to begin configuration.

(118) This specification is the initialization time that indicates the time from CONF_DONE signal goes high to INIT_DONE signal goes high.

Table 96. POR Delay Specification

For specification status, see the *Data Sheet Status* table

POR Delay	Minimum	Maximum	Unit
AS (Normal mode), AVST ×8, AVST ×16, AVST ×32	11.5	20.2	ms
AS (Fast mode)	1.5	7.6	ms

External Configuration Clock Source Requirements

Table 97. External Configuration Clock Source (OSC_CLK_1) Clock Input Requirements

For specification status, see the *Data Sheet Status* table

Description	External Clock Source	Min	Typ	Max	Unit
Clock input frequency(119)	Powered by V_{CCIO_SDM}		25/100/125		MHz
Clock input peak-to-peak period jitter tolerance		—	—	2	%
Clock input duty cycle		45	50	55	%

JTAG Configuration Timing

Table 98. JTAG Timing Parameters and Values

For specification status, see the *Data Sheet Status* table

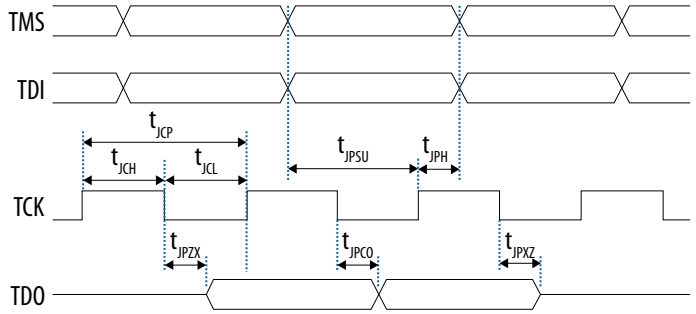
Symbol	Description	Requirement		Unit
		Minimum	Maximum	
t_{JCP}	TCK clock period	30	—	ns
t_{JCH}	TCK clock high time	14	—	ns

continued...

(119) The acceptable clock frequencies are 25 MHz, 100 MHz, and 125 MHz only. You must match the external configuration clock frequency on the OSC_CLK_1 pin to the configuration clock source assignment in the Intel Quartus Prime software. Other frequencies in the range are not supported.

Symbol	Description	Requirement		Unit
		Minimum	Maximum	
t_{JCL}	TCK clock low time	14	—	ns
$t_{JPSU\ (TDI)}$ (120)	TDI JTAG port setup time	2	—	ns
$t_{JPSU\ (TMS)}$ (120)	TMS JTAG port setup time	3	—	ns
t_{JPH} (120)	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	7(121)	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14	ns

Figure 26. JTAG Timing Diagram



(120) For boundary-scan testing, the TMS and TDI JTAG ports minimum setup time and hold time are 7 ns.

(121) Capacitance loading at 10 pF.

AS Configuration Timing

Table 99. AS Timing Parameters

Intel recommends performing trace length matching for nCSO and AS_DATA pins to AS_CLK to minimize the skew. Refer to the related information to calculate the maximum allowable skew tolerance for nCSO and AS_DATA pins to AS_CLK.

For specification status, see the *Data Sheet Status* table

Symbol	Description	Minimum	Typical	Maximum	Unit
T_{clk} (122)	AS_CLK clock period	—	6.02	—	ns
$T_{dutycycle}$	AS_CLK duty cycle	45	50	55	%
T_{dcsfrs}	AS_nCSO[3:0] asserted to first AS_CLK edge	8.5(123)	—	—	ns
T_{dcslst}	Last AS_CLK edge to AS_nCSO[3:0] deasserted	6.8(123)	—	—	ns

continued...

(122) AS_CLK f_{MAX} has dependency on the maximum board loading. For AS single device configuration or AS using multiple serial flash devices configuration, use the equations in T_{do} and T_{ext_delay} notes to ensure your board has sufficient timing margin to meet flash setup/hold time specifications and AS timing specifications in this d*ata sheet*. For AS using multiple serial flash devices, refer to the related information for the recommended AS_CLK frequency and maximum board loading.

(123) AS operating at maximum clock frequency = 166 MHz. The delay is larger when operating at AS clock frequency lower than 166 MHz.

Symbol	Description	Minimum	Typical	Maximum	Unit
T_{do} (124)	AS_DATA[3:0] output delay	–0.6	—	0.6	ns
T_{ext_delay} (125) (126)	Total external propagation delay on AS signals	0	—	13.5	ns
T_{dcsb2b}	Minimum delay of slave select deassertion between two back-to-back transfers	62	—	—	ns

(124) Load capacitance for DCLK = 12 pF and AS_DATA = 27 pF. Intel recommends obtaining the T_{do} for a given link (including receiver, transmission lines, connectors, termination resistors, and other components) through IBIS or HSPIC simulation. To analyze flash setup time,

- $T_{su} = T_{clk}/2 - T_{do(max)} + T_{bd\_clk} - T_{bd\_data(max)}$
- $T_{ho} = T_{clk}/2 + T_{do(min)} - T_{bd\_clk} + T_{bd\_data(min)}$

(125) $T_{ext\_delay} = T_{bd\_clk} + T_{co} + T_{bd\_data} + T_{add}$

- T_{bd_clk}: Propagation delay for AS_CLK between FPGA and flash device.
- T_{co}: Output hold time and clock low to output valid of flash device. This delay must be used to ensure T_{ext_delay} is within the minimum and maximum specification values.
- T_{bd_data}: Propagation delay for AS_DATA bus between FPGA and flash device.
- T_{add}: Propagation delay for active/passive components on AS_DATA interfaces.

(126) T_{ext_delay} specification is based on AS_CLK = 166 MHz. The value can be larger at lower AS_CLK frequency. For more details, refer to the related information.

Figure 27. AS Configuration Serial Output Timing Diagram

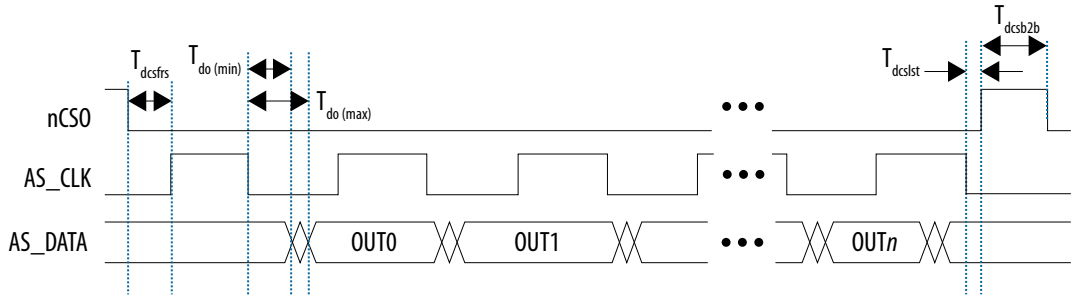
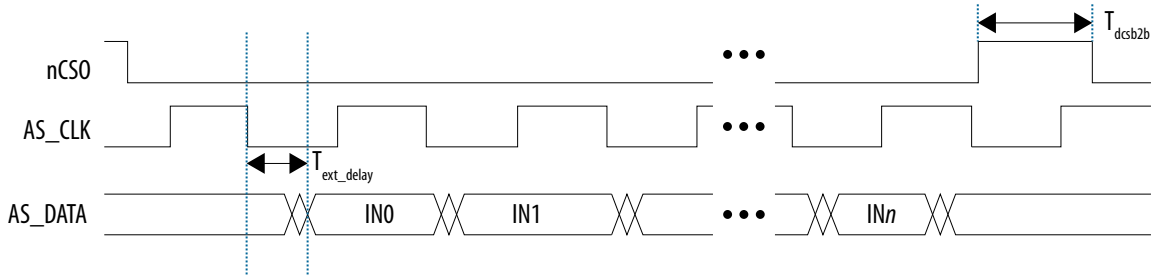


Figure 28. AS Configuration Serial Input Timing Diagram



Related Information

Intel Agilex 7 Configuration User Guide
Provides more information about AS_CLK.

Avalon Streaming (Avalon-ST) Configuration Timing

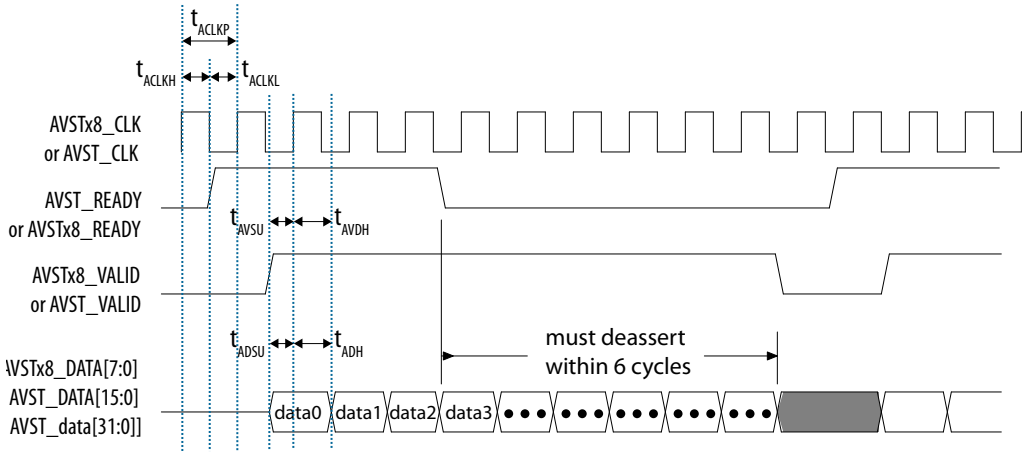
Table 100. Avalon-Streaming Timing Parameters for x8, ×16, and ×32 Configurations

For specification status, see the *Data Sheet Status* table

Symbol	Description	Minimum	Unit
t_{ACLKH}	AVST_CLK high time	3.6	ns
t_{ACLKL}	AVST_CLK low time	3.6	ns
t_{ACLKP}	AVST_CLK period	8	ns
t_{ADSU} (127)	AVST_DATA setup time before rising edge of AVST_CLK	2.1	ns
t_{ADH} (127)	AVST_DATA hold time after rising edge of AVST_CLK	0.1	ns
t_{AVSU}	AVST_VALID setup time before rising edge of AVST_CLK	2.1	ns
t_{AVDH}	AVST_VALID hold time after rising edge of AVST_CLK	0	ns

(127) Data sampled by the FPGA (sink) at the next rising clock edge.

Figure 29. Avalon-ST Configuration Timing Diagram



Configuration Bit Stream Sizes

Table 101. Configuration Bit Stream Sizes

Configuration bit stream sizes shown in this table are based on worst-case scenarios. The sizes are typically substantially smaller because of the use of the Intel bit stream compression. The Intel bit stream compression efficiency has dependency on your design complexity.

128 Mb quad SPI flash size is adequate to store the periphery image.

For specification status, see the *Data Sheet Status* table

Variant	Compressed Configuration Bit Stream Size (Mbits)
AGF 006, AGF 008	293
AGF 012, AGF 014	511
AGF 019, AGF 023	628
AGI 019, AGI 023	733
AGF 022, AGF 027	928

continued...

Variant	Compressed Configuration Bit Stream Size (Mbits)
AGI 022, AGI 027	969
AGI 035, AGI 040	1,436
AGI 041	1,166

I/O Timing

I/O timing data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the timing analysis. You may generate the I/O timing report manually using the Timing Analyzer.

The Intel Quartus Prime Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

Related Information

AN 775: Generating Initial I/O Timing Data and I/O Element Delays for Intel FPGAs
Provides the techniques to generate I/O timing information using the Intel Quartus Prime software.

Programmable IOE Delay

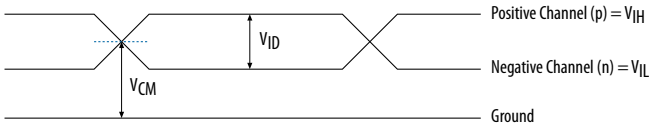
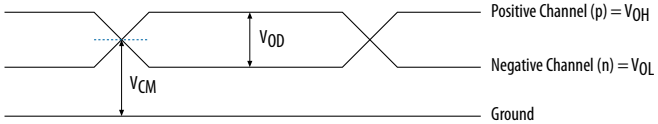
Table 102. Programmable IOE Delay

For specification status, see the *Data Sheet Status* table

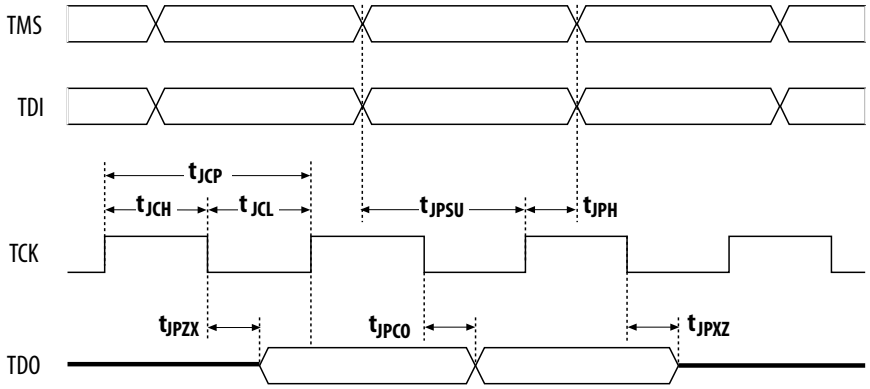
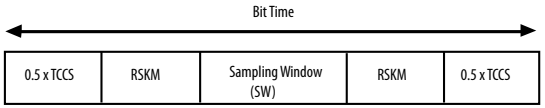
Parameter	Maximum Offset	Minimum Offset	Fast Model	Slow Model			Unit
			Extended, Industrial	–E1, –I1	–E2, –I2	–E3, –I3V	
Input Delay Chain (INPUT_DELAY_CHAIN)	63	0	1.474	2.324	2.631	3.343	ns
Output Delay Chain (OUTPUT_DELAY_CHAIN)	15	0	0.356	0.552	0.629	0.808	ns

Glossary

Table 103. Glossary

Term	Definition
Differential I/O Standards	Receiver Input Waveforms **Single-Ended Waveform**  **Differential Waveform**  Transmitter Output Waveforms **Single-Ended Waveform**  **Differential Waveform** 
f_{HSCLK}	I/O PLL input clock frequency.
f_{HSDR}	LVDS SERDES block—maximum/minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.

continued...

Term	Definition
$f_{HSDRDPA}$	LVDS SERDES block—maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
J (SERDES factor)	LVDS SERDES block—deserialization factor (width of parallel data bus).
JTAG Timing Specifications	JTAG Timing Specifications: 
R_L	Receiver differential input discrete resistor (external to the device).
Sampling window (SW)	Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window, as shown: 
Single-ended voltage referenced I/O standard	The JEDEC standard for the SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing. Single-Ended Voltage Referenced I/O Standard

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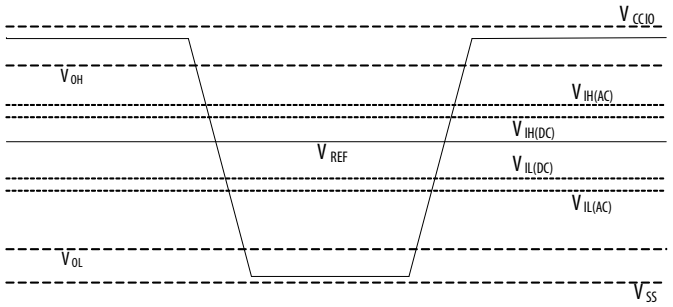
Term	Definition
	
t_C	High-speed receiver/transmitter input and output clock period.
TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including the t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table).
t_{DUTY}	LVDS SERDES block—duty cycle on high-speed transmitter output clock.
t_{FALL}	Signal high-to-low transition time (80–20%).
t_{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input.
t_{OUTPJ_IO}	Period jitter on the GPIO driven by a PLL.
t_{OUTPJ_DC}	Period jitter on the dedicated clock output driven by a PLL.
t_{RISE}	Signal low-to-high transition time (20–80%).
Timing Unit Interval (TUI)	The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w).
$V_{CM(DC)}$	DC Common mode input voltage.
V_{ICM}	Input Common mode voltage—the common mode of the differential signal at the receiver.
$V_{ICM(DC)}$	$V_{CM(DC)}$ DC Common mode input voltage.
V_{ID}	Input differential voltage swing—the difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
$V_{DIF(AC)}$	AC differential input voltage—minimum AC input differential voltage required for switching.
$V_{DIF(DC)}$	DC differential input voltage—minimum DC input differential voltage required for switching.

continued...

Term	Definition
V_{IH}	Voltage input high—the minimum positive voltage applied to the input which is accepted by the device as a logic high.
$V_{IH(AC)}$	High-level AC input voltage.
$V_{IH(DC)}$	High-level DC input voltage.
V_{IL}	Voltage input low—the maximum positive voltage applied to the input which is accepted by the device as a logic low.
$V_{IL(AC)}$	Low-level AC input voltage.
$V_{IL(DC)}$	Low-level DC input voltage.
V_{OCM}	Output Common mode voltage—the common mode of the differential signal at the transmitter.
V_{OD}	Output differential voltage swing—the difference in voltage between the positive and complementary conductors of a differential transmission line at the transmitter.
V_{SWING}	Differential input voltage.
V_{OX}	Output differential cross point voltage.
$V_{IX(AC)}$	V_{IX} Input differential cross point voltage.
W	LVDS SERDES block—Clock Boost Factor.

Document Revision History for the Intel Agilex 7 FPGAs and SoCs Device Data Sheet: F-Series and I-Series

Document Version	Changes
2023.04.19	Added AGI 041 R31B package in the *Data Sheet Status for Intel Agilex Devices (I-Series)* table.
2023.04.03	• Updated the *Absolute Maximum Ratings* table. — Updated V_{CCH} (for R-Tile and F-Tile devices), V_{CCH_SDM} (for R-Tile and F-Tile devices), V_{CCEHT_GXR}, V_{CCERT_GXR}, V_{CCED_GXR}, $V_{CCE\_PLL\_GXR}$, $V_{CCE\_DTS\_GXR}$, V_{CCCLK_GXR}, $V_{CCHFUSE\_GXR}$, $V_{CC\_HSSI\_GXR}$, and $V_{CCH\_FGT\_GXF}$ specifications. — Added $V_{CC\_HSSI\_GXF}$, $V_{CCFUSECORE\_GXF}$, $V_{CCFUSEWR\_GXF}$, and V_{CCCLK_GXF} specifications. • Updated V_{CCH} (for R-Tile and F-Tile devices) and V_{CCH_SDM} (for R-Tile and F-Tile devices) in the *Recommended Operating Conditions* table. • Updated the simple quad-port RAM specification for –2V speed grade in the *Memory Block Performance Specifications* table. • Updated specifications for AGF 006/008 and AGI 019/023 in the *Configuration Bit Stream Sizes* table.

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Document Version	Changes
2023.02.20	• Updated product family name to "Intel Agilex 7". • Retitled the document from *Intel Agilex F-Series and I-Series Device Data Sheet* to *Intel Agilex 7 FPGAs and SoCs Device Data Sheet: F-Series and I-Series*. • Added AGI 041 R29D package in the following tables: — *Data Sheet Status for Intel Agilex 7 FPGAs and SoCs I-Series* — *Configuration Bit Stream Sizes* • Updated the status from Advance to Preliminary for the following devices in the *Data Sheet Status for Intel Agilex 7 FPGAs and SoCs I-Series* table: — AGI 019/023 R18A package — AGI 022/027 R29A package — AGI 019/022/023/027 R31B package — AGI 035/040 R39A package • Updated $V_{CCH\_GXR[L,R]}$ and $V_{CCRT\_GXR[L,R]}$ specifications in the *R-Tile Transceiver Power Supply Recommended Operating Conditions* table. • Added quad SPI flash size to store periphery image in the *Configuration Bit Stream Sizes* table.
2022.12.19	• Added AGI 022/027 R31A package in the *Data Sheet Status for Intel Agilex Devices (I-Series)* table. • Updated table description for the *AS Timing Parameters* table. • Added T_{dcsb2b} symbol in the *AS Configuration Serial Output Timing Diagram*. • Updated specifications for AGI 022 and AGI 027 devices in the *Configuration Bit Stream Sizes* table.
2022.11.01	• Renamed document title from *Intel Agilex Device Data Sheet* to *Intel Agilex F-Series and I-Series Device Data Sheet*. • Removed device name in tables and descriptions. • Changed the status for AGF 019/023 R25A package from Preliminary to Final in the *Data Sheet Status for Intel Agilex Devices (F-Series)* table. • Removed conditions for CXL 2.5 GT/s and CXL 5 GT/s in the *R-Tile Slow PLL Performance* table. • Updated typical frequency specification in the *F-Tile FHT Reference Clock Requirements* table. • Updated $V_{REFIN-CM-AC}$ in the *F-Tile FHT Reference Clocks Input Specifications* table. • Updated the parameter and description, and added a footnote for $V_{REFIN-DIFF}$ in the *F-Tile FGT Reference Clock Input Specifications* table. • Added $V_{TX-CM\ OUT}$ specifications in the following tables: — *F-Tile FHT Transmitter Electrical Specifications* — *F-Tile FGT Transmitter Electrical Specifications*
2022.07.04	• Added AGI 035/040 R39A package in the *Data Sheet Status for Intel Agilex Devices (I-Series)* table. • Added V_{CCH_SDM} specifications for F-tile devices in the *Recommended Operating Conditions for Intel Agilex Devices* table. • Updated $Z_{TX-DIFF-DC}$ description and specifications in the *F-Tile FGT Transmitter Electrical Specifications* table. • Updated $R_{DIFF-DC}$ specifications in the *F-Tile FGT Receiver Electrical Specifications* table. • Added specifications for AGI 035 and AGI 040 devices in the *Configuration Bit Stream Sizes for Intel Agilex Devices* table.

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Document Version	Changes
2022.05.12	• Added R-tile and F-tile devices for V_{CCH} specifications in the *Absolute Maximum Rating for Intel Agilex Devices* table. • Updated the *F-Tile FGT Reference Clock Input Specifications for Intel Agilex Devices* table. — Updated unit for $V_{REFIN-DIFF-AC}$. — Updated $V_{REFIN-IL-DC}$ and $V_{REFIN-IH-DC}$ specifications. — Updated unit and specifications for $T_{REF-RISE/FALL}$. — Added $V_{REFIN-CM-AC}$ and $V_{REFIN-CM-DC}$ specifications. — Updated parameter from $P_{NREF-SSB}$ to $P_{NREF-SSB}$ (156.25MHz). • Updated the *F-Tile FGT Reference Clock Output Driver Specifications for Intel Agilex Devices* table. — Updated $T_{REF-RISE\_OUT/FALL\_OUT}$ specifications. — Updated unit for $V_{REFIN-DIFF-AC\_OUT}$. — Added footnote to $V_{REFIN-CM-OUT}$. • Updated the *F-Tile FHT Transmitter Electrical Specifications* table. — Removed T_{TX-DJ} and T_{TX-RJ} specifications. — Updated unit for Transmitter DC impedance. • Updated the *F-Tile FGT Transmitter Electrical Specifications* table. — Updated unit for $V_{TX-DIFF-PKPK}$. — Removed $V_{TX-EYE-PKPK}$ specifications. — Updated description and unit for Transmitter DC impedance. — Updated $Z_{RL-DIFF-DC}$ specifications. • Updated unit for Receiver DC impedance in the *F-Tile FHT Receiver Electrical Specifications* table. • Updated the *F-Tile FGT Receiver Electrical Specifications* table. — Updated $I_{INS-LOSS-56Gb/s}$, $I_{INS-LOSS-30Gb/s}$, and $I_{INS-LOSS-25Gb/s}$ specifications. — Updated unit for Receiver DC impedance. • Updated the *F-Tile FGT Electrical Compliance List* table. — Removed JESD204A specifications. — Updated specifications for JESD204B, JESD204C, and HDMI protocols. • Updated $t_{CF02ST0}$ specifications in the *General Configuration Timing Specifications for Intel Agilex Devices* table.
2022.04.15	• Removed R31A package in the *Data Sheet Status for Intel Agilex Devices (I-Series)* table. • Updated footnote to V_{CCBAT} in the *Recommended Operating Conditions for Intel Agilex Devices* table. • Changed the symbol from V_{CCR_CORE} to $V_{CCRCORE}$ in the following tables: — *Absolute Maximum Rating for Intel Agilex Devices* — *Recommended Operating Conditions for Intel Agilex Devices*
2021.12.13	Updated the *R-Tile Transmitter and Receiver Data Rate Performance for Intel Agilex Devices* table.

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Document Version	Changes
2021.10.26	• Updated the *Data Sheet Status for Intel Agilex Devices (F-Series)* table. — Updated status for AGF 012/014 R24A package. — Updated status for AGF 022/027 R25A package. — Added AGF 012/014 R24B package. — Added AGF 019/023 R25A, R24C, and R31C packages. • Added AGI 019/023 R18A and R31B packages in the *Data Sheet Status for Intel Agilex Devices (I-Series)* table. • Updated the *Absolute Maximum Rating for Intel Agilex Devices* table. — Updated footnotes for I_{OUT} condition. — Changed symbol from $V_{CCEH\_FGT\_GXF}$ to $V_{CCH\_FGT\_GXF}$. • Updated the *Recommended Operating Conditions for Intel Agilex Devices* table. — Added I_{BAT} specifications. — Updated V_I and V_O specifications. • Added footnote to V_{CCCLK_GXP} and V_{CCH_GXP} in the *P-Tile Transceiver Power Supply Operating Conditions for Intel Agilex Devices* table. • Updated the *R-Tile Transceiver Power Supply Operating Conditions for Intel Agilex Devices* table. — Updated symbol from $V_{CCEHT\_GXR[L,R]}$ to $V_{CCH\_GXR[L,R]}$. — Updated symbol from $V_{CCERT\_GXR[L,R]}$ to $V_{CCRT\_GXR[L,R]}$. — Updated specifications for $V_{CCH\_GXR[L,R]}$, $V_{CCED\_GXR[L,R]}$, $V_{CCCLK\_GXR[L,R]}$, and $V_{CC\_HSSI\_GXR}$. — Added footnote to $V_{CCH\_GXR[L,R]}$ and $V_{CCCLK\_GXR[L,R]}$. • Updated descriptions in the *Internal Weak Pull-Up Resistor* section. • Added V_{IL} (min) and V_{IH} (max) in the *Single-Ended I/O Standards Specifications for Intel Agilex Devices (for HPS and SDM I/O Banks)* table. • Added footnotes to t_{REFPJ} and t_{REFPN} in the *I/O PLL Specifications for Intel Agilex Devices* table. • Updated descriptions in the *Remote Temperature Diode Specifications* section. • Added the following tables: — *Remote Temperature Diode Specifications for Intel Agilex Devices (R-Tile TSD)* — *Remote Temperature Diode Specifications for Intel Agilex Devices (F-Tile TSD)* • Removed the reference to rate support and combined the following tables into one table: *Memory Standards Supported by Intel Agilex Devices* — *Memory Standards Supported by the Hard Memory Controller for Intel Agilex Devices* — *Memory Standards Supported by the Soft Memory Controller for Intel Agilex Devices* — *Memory Standards Supported by the HPS Hard Memory Controller for Intel Agilex Devices* • Added footnote to F_{REF} in the *F-Tile FGT Reference Clock Input Specifications for Intel Agilex Devices* table. • Updated $Z_{REF\text{-}DIFF\text{-}DC\_OUT}$ and $V_{REFIN\text{-}DIFF\text{-}AC\_OUT}$ descriptions in the *F-Tile FGT Reference Clock Output Driver Specifications for Intel Agilex Devices* table. • Updated the *F-Tile FHT Transmitter Electrical Specifications* table. — Updated $T_{TX\text{-}DJ}$ specification. — Removed N_{GPLL} specification.

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Document Version	Changes
	• Updated the *F-Tile FGT Transmitter Electrical Specifications* table. — Updated $V_{TX-DIFF-PKPK}$ description. — Added $V_{TX-EYE-PKPK}$ specifications. — Removed $N_{GPLL-PAM}$ and $N_{GPLL-NRZ}$ specifications. • Updated the *F-Tile FHT Receiver Electrical Specifications* table. — Added V_{RX-MAX} and V_{RX-MIN} specifications. — Removed N_{GPLL} specification. • Updated the *F-Tile FGT Receiver Electrical Specifications* table. — Added V_{RX-MIN} specifications. — Updated footnote to V_{RX-MAX}, $V_{RX-CM-DC}$, and $V_{IDLE-THRESH}$. — Removed $N_{GPLL-PAM}$ and $N_{GPLL-NRZ}$ specifications. • Updated the *F-Tile FHT Electrical Compliance List* table. — Removed IEEE 802.3cd 137/136, IEEE 802.3bj/bm 93, IEEE 802.3bj/bm 92, and IEEE 802.3by 111/110 specifications. — Updated the protocols for CEI 4.0/5.0 specification. • Updated the *F-Tile FGT Electrical Compliance List* table. — Updated specifications for SDI, JESD204A, JESD204B, JESD204C, Fiber Channel, Interlaken, and HDMI protocols. — Added specifications for GPON protocol. • Updated $t_{CF02ST0}$ to add specifications when security features enabled in the *General Configuration Timing Specifications for Intel Agilex Devices* table. • Updated the description for T_{do} in the *AS Timing Parameters for Intel Agilex Devices* table. • Updated the *Configuration Bit Stream Sizes for Intel Agilex Devices* table. — Added table description. — Added specifications for AGF 019, AGF 023, AGI 019, and AGI 023 devices. — Updated specifications for AGF 012, AGF 014, AGF 022, AGF 027, AGI 022, and AGI 027 devices. • Updated the *Programmable IOE Delay for Intel Agilex Devices* table. — Added Industrial grade and updated the fast model specifications. — Added –E1, –I1, –I2, and –I3V speed grades, and updated the slow model specifications.
2021.06.02	• Updated the *Data Sheet Status for Intel Agilex Devices (F-Series)* table. — Removed R17A and R20A packages. — Added AGF 006 and AGF 008 devices for R24C package. • Added support for –E4X speed grade in the *Intel Agilex Device Grades, Core Speed Grades, and Power Options Supported* table. • Updated the *Absolute Maximum Rating for Intel Agilex Devices* table. — Updated the maximum specifications for V_{CCR_CORE} and V_{CCA_PLL}. — Removed V_{CCIO3V_GXB}, V_I (for V_{CCIO3V_GXB}), $V_{CC\_HSSI\_GXB}$, V_{CCH_GXB}, V_{CCT_GXB}, and V_{CCR_GXB} specifications. — Added R-tile specifications: V_{CCEHT_GXR}, V_{CCERT_GXR}, V_{CCED_GXR}, $V_{CCE\_PLL\_GXR}$, $V_{CCE\_DTS\_GXR}$, V_{CCCLK_GXR}, $V_{CCHFUSE\_GXR}$, and $V_{CC\_HSSI\_GXR}$. — Added F-tile specifications: $V_{CCERT1\_FHT\_GXF}$, $V_{CCERT2\_FHT\_GXF}$, $V_{CCEHT\_FHT\_GXF}$, $V_{CCERT\_FGT\_GXF}$, $V_{CCEH\_FGT\_GXF}$, and $V_{CCERT\_GXF\_COMBINE}$.

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Document Version	Changes
	• Updated the *Recommended Operating Conditions for Intel Agilex Devices* table. — Added specifications for –4X speed grade for V_{CC} and V_{CCP}. — Removed V_{CCH} and V_{CCH_SDM} specifications for H-tile and P-tile devices. — Removed V_{CCIO3V_GXB} and V_I (for V_{CCIO3V_GXB}) specifications. — Added V_{CCH} specifications for R-tile and F-tile devices. — Removed condition for V_{CCH_SDM}. • Updated the *HPS Power Supply Operating Conditions for Intel Agilex Devices* table. — Added specifications for –4X speed grade for V_{CCL_HPS} and $V_{CCPLLDIG\_HPS}$. — Added footnote for V_{CCL_HPS} and $V_{CCPLLDIG\_HPS}$. • Updated specifications for 34-Ω and 40-Ω R_S in the *OCT Calibration Accuracy Specifications for Intel Agilex Devices (for GPIO Bank)* table. • Updated V_{ID} and $V_{ICM(DC)}$ specifications in the *Differential I/O Standards Specifications for Intel Agilex Devices (for GPIO Bank)* table. • Added specifications for –4X speed grade in the *Clock Tree Performance for Intel Agilex Devices* table. • Updated the *I/O PLL Specifications for Intel Agilex Devices* table. — Added specifications for –4X speed grade for f_{IN}, f_{VCO}, f_{OUT}, and f_{OUT_EXT}. — Updated $t_{OUTDUTY}$ specifications. — Updated footnote for t_{OUTPJ_DC}, t_{OUTCCJ_DC}, t_{OUTPJ_IO}, and t_{OUTCCJ_IO}. • Updated the *DSP Block Performance Specifications for Intel Agilex Devices* table. — Added specifications for –4X speed grade. — Added footnote for Fixed-point 18 × 19 multiplier adder summed with 36-bit input mode — Updated the modes as FP32 floating-point vector dot product and FP16 floating-point vector dot product. — Added the following modes: • Sum/sub of two FP16 multiplications with FP32 (addition/subtraction) • Sum/sub of two FP16 multiplications with accumulation (addition/subtraction) • Added specifications for –4X speed grade in the *Memory Block Performance Specifications for Intel Agilex Devices* table. • Added footnote to Sampling Rate in the *Local Temperature Sensor Specifications for Intel Agilex Devices* table. • Removed description on H-tile in the *Remote Temperature Diode Specifications* section. • Updated the *Voltage Sensor Specifications for Intel Agilex Devices* table. — Added footnote to Sampling Rate and Voltage sensor accuracy. — Removed Differential non-linearity (DNL) and Integral non-linearity (INL) specifications. • Updated the description for the *Memory Standards Supported by the Soft Memory Controller for Intel Agilex Devices* table. • Updated MPU frequency specifications in the *Maximum HPS Clock Frequencies for Intel Agilex Devices* table. • Added the *HPS Cold Reset for Intel Agilex Devices* table. • Updated T_{su} specification in the *SPI Master Timing Requirements for Intel Agilex Devices* table. • Updated T_{suss} and T_{hss} specifications in the *SPI Slave Timing Requirements for Intel Agilex Devices* table. • Updated T_d specifications in the *HPS Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Intel Agilex Devices* table. • Updated T_h specification in the *HPS USB 2.0 Transceiver Macrocell Interface Plus (UTMI+) Low Pin Interface (ULPI) Timing Requirements for Intel Agilex Devices* table.

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Document Version	Changes
	• Updated footnotes for T_{HIGH} and T_{LOW} specifications in the *HPS I^2C Timing Requirements for Intel Agilex Devices* table. • Updated T_d specifications in the *Trace Timing Requirements for Intel Agilex Devices* table. • Updated t_{JPH} specification in the *HPS JTAG Timing Requirements for Intel Agilex Devices* table. • Updated typical specifications in the *HPS Programmable I/O Delay (Output Path) for Intel Agilex Device* and *HPS Programmable I/O Delay (Input Path) for Intel Agilex Device* tables. • Added $t_{ST12CF0}$ and $t_{ST02CF1}$ specifications in the *General Configuration Timing Specifications for Intel Agilex Devices* table. • Added *General Configuration Timing Diagram*. • Updated the *AS Timing Parameters for Intel Agilex Devices* table. — Updated table description. — Updated T_{clk}, T_{dcsfrs}, T_{dcslst}, T_{do}, T_{ext_delay}, and T_{dcsb2b} specifications. — Updated footnote for T_{ext_delay}. • Updated t_{ADH} specification in the *Avalon-ST Timing Parameters for x8, ×16, and ×32 Configurations in Intel Agilex Devices* table. • Updated the *Configuration Bit Stream Sizes for Intel Agilex Devices* table. — Removed AGF 004 device. — Updated specifications for AGF 006 device. • Added R-tile and F-tile specifications. Added the following tables/sections: — *R-Tile Transceiver Power Supply Operating Conditions for Intel Agilex Devices* table — *F-Tile Transceiver Power Supply Operating Conditions for Intel Agilex Devices* table — *R-Tile Transceiver Performance Specifications* section — *F-Tile Transceiver Performance Specifications* section • Removed H-Tile specifications. The following tables/section are removed: — *H-Tile Transceiver Power Supply Operating Conditions for Intel Agilex Devices* — *Remote Temperature Diode Specifications for Intel Agilex Devices (H-Tile TSD)* — *H-Tile Transceiver Performance Specifications* • Removed the following tables for 3 V I/O banks: — *Maximum Allowed Overshoot During Transitions for Intel Agilex Devices (for 3 V I/O Bank)* — *I/O Pin Leakage Current for Intel Agilex Devices (for 3 V I/O Bank)* — *Bus Hold Parameters for Intel Agilex Devices (for 3 V I/O Bank)* — *OCT Without Calibration Resistance Tolerance Specifications for Intel Agilex Devices (for 3 V I/O Bank)* — *Pin Capacitance for Intel Agilex Devices (for 3 V I/O Bank)* — *Internal Weak Pull-Up Resistor Values for Intel Agilex Devices (for 3 V I/O Bank)* — *Single-Ended I/O Standards Specifications for Intel Agilex Devices (for 3 V I/O Bank)*

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Document Version	Changes
2021.01.07	• Updated the *Data Sheet Status for Intel Agilex Devices* tables. • Updated table title from *Intel Agilex Device Grades and Speed Grades Supported* to *Intel Agilex Device Grades, Core Speed Grades, and Power Options Supported*. • Added V_{CCIO3V_GXB}, V_I (for V_{CCIO3V_GXB}), $V_{CC\_HSSI\_GXB}$, V_{CCH_GXB}, V_{CCT_GXB}, and V_{CCR_GXB} specifications in the *Absolute Maximum Rating for Intel Agilex Devices* table. • Updated the description in the *Maximum Allowed Overshoot and Undershoot Voltage* section. • Updated the figure title to *Intel Agilex Devices Overshoot Duration Example (for 1.2 V GPIO Bank at V_{CCIO_PIO} = 1.26 V)*. • Updated the *Recommended Operating Conditions for Intel Agilex Devices* table. — Updated V_{CC} and V_{CCP} specifications. — Updated description for V_{CCH}. — Added V_{CCH} and V_{CCH_SDM} specifications for H-tile and P-tile devices. — Updated note to V_{CCBAT}. — Added V_{CCIO3V_GXB} and V_I (for V_{CCIO3V_GXB}) specifications. — Updated the minimum specification for t_{RAMP}. • Added the *H-Tile Transceiver Power Supply Operating Conditions for Intel Agilex Devices* table. • Updated V_{CCL_HPS} and $V_{CCPLLDIG\_HPS}$ specifications in the *HPS Power Supply Operating Conditions for Intel Agilex Devices* table. • Updated the specifications in the *I/O Pin Leakage Current for Intel Agilex Devices (For GPIO Bank)* table. • Updated the specifications in the *Bus Hold Parameters for Intel Agilex Devices (For GPIO Bank)* table. • Added specifications for 100-Ω R_D for V_{CCIO_PIO} = 1.2 V in the *OCT Without Calibration Resistance Tolerance Specifications for Intel Agilex Devices (For GPIO Bank)* table. • Updated the specifications in the *Pin Capacitance for Intel Agilex Devices* table. • Updated the specifications in the *Internal Weak Pull-Up Resistor Values for Intel Agilex Devices (For GPIO Bank)* table. • Updated the *Single-Ended I/O Standards Specifications for Intel Agilex Devices (For GPIO Bank)* table. — Removed note to 1.2 V LVCMOS in the *Single-Ended I/O Standards Specifications for Intel Agilex Devices (for GPIO Bank)* table. — Added V_{OL} and V_{OH} specifications.

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Document Version	Changes
	• Added the following tables for HPS, SDM, and 3 V I/O banks: — *Maximum Allowed Overshoot During Transitions for Intel Agilex Devices (for 3 V I/O Bank)* — *I/O Pin Leakage Current for Intel Agilex Devices (for HPS and SDM I/O Bank)* — *I/O Pin Leakage Current for Intel Agilex Devices (for 3 V I/O Bank)* — *Bus Hold Parameters for Intel Agilex Devices (for 3 V I/O Bank)* — *OCT Without Calibration Resistance Tolerance Specifications for Intel Agilex Devices (for 3 V I/O Bank)* — *Pin Capacitance for Intel Agilex Devices (for 3 V I/O Bank)* — *Internal Weak Pull-Up and Weak Pull-Down Resistor Values for Intel Agilex Devices (for HPS and SDM I/O Banks)* — *Internal Weak Pull-Up Resistor Values for Intel Agilex Devices (for 3 V I/O Bank)* — *Hysteresis Specifications for Schmitt Trigger Input for Intel Agilex Devices (for HPS I/O Bank)* — *Single-Ended I/O Standards Specifications for Intel Agilex Devices (for HPS and SDM I/O Banks)* — *Single-Ended I/O Standards Specifications for Intel Agilex Devices (for 3 V I/O Bank)* • Updated specification for –1 speed grade in the *Clock Tree Performance for Intel Agilex Devices* table. • Updated the *I/O PLL Specifications for Intel Agilex Devices* table. — Updated f_{IN}, f_{VCO}, and f_{OUT} specifications for –4F speed grade. — Updated f_{OUT_EXT} specifications for –2, –3, and –4 speed grades. — Added t_{INCCJ} specifications. — Added note to t_{OUTPJ_DC}, t_{OUTCCJ_DC}, t_{OUTPJ_IO}, and t_{OUTCCJ_IO}. — Updated condition for t_{OUTPJ_DC}, t_{OUTCCJ_DC}, t_{OUTPJ_IO}, t_{OUTCCJ_IO}, and $t_{CASC\_OUTPJ\_DC}$. • Updated the description in the *Remote Temperature Diode Specifications* section. • Updated I_{bias}, V_{bias}, and diode ideality factor specifications in the *Remote Temperature Diode Specifications for Intel Agilex Devices (E-Tile TSD)* table. • Added the *Remote Temperature Diode Specifications for Intel Agilex Devices (H-Tile TSD)* table. • Updated the *Voltage Sensor Specifications for Intel Agilex Devices* table. — Updated voltage sensor accuracy V_{in} range and specifications. — Updated Unipolar Input Mode specifications. • Updated tx Jitter for data rate 600 Mbps – 1.6 Gbps in the *LVDS SERDES Specifications for Intel Agilex Devices* table. • Updated the jitter amplitude in the *LVDS SERDES Soft-CDR Sinusoidal Jitter Tolerance Specifications for a Data Rate Equal to 1.6 Gbps* diagram. • Updated the sinusoidal jitter for F3 and F4 in the *LVDS SERDES Soft-CDR Sinusoidal Jitter Mask Values for a Data Rate Equal to 1.6 Gbps* table. • Removed RLDRAM 3 specifications from the *Memory Standards Supported by the Soft Memory Controller for Intel Agilex Devices* table. • Updated the *E-Tile Receiver Specifications* table. — Updated absolute V_{MAX} for a receiver pin specifications. — Changed from V_{ICM} (AC coupled) to V_{CM} (Internal AC coupled) and updated the specifications. • Updated the *P-Tile PLLA Performance* table. — Added PLL bandwidth (BWTX-PKG_PLL1) and PLL peaking (PKGTX-PLL1) specifications for PCIe 5.0 GT/s. — Updated PLL peaking (PKGTX-PLL2) specifications. — Added note on PLL bandwidth and PLL peaking.

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Document Version	Changes
	• Updated the *P-Tile PLLB Performance* table. — Added PLL bandwidth (BWTX-PKG_PLL2) and PLL peaking (PKGTX-PLL2) specifications. — Added note on PLL bandwidth and PLL peaking. • Updated the *P-Tile Reference Clock Specifications* table. — Updated notes to Input reference clock frequency and TCCJITTER. — Added conditions for Rising edge rate, Falling edge rate, Duty cycle, V_{ICM}, TCCJITTER, and TSSC-MAX-PERIOD-SLEW parameters. — Updated spread-spectrum downspread, absolute V_{MAX}, and absolute V_{MIN} specifications. • Added condition for differential on-chip termination resistors parameter in the *P-Tile Transmitter Specifications* table. • Updated the *P-Tile Receiver Specifications* table. — Updated V_{ID} (diff p-p) specifications for PCIe 16.0 GT/s. — Removed V_{ICM} (AC coupled) specifications. — Added RREF specifications. • Added *H-Tile Transceiver Performance Specifications* section. • Updated fixed V_{CCL_HPS} and MPU frequency for –1 speed grade in the *Maximum HPS Clock Frequencies for Intel Agilex Devices* table. • Updated the internal oscillator frequency in the *HPS Internal Oscillator Frequency for Intel Agilex Devices* table. • Added the *HPS JTAG Timing Diagram*. • Updated the *HPS Programmable I/O Delay (Output Path) for Intel Agilex Device* and *HPS Programmable I/O Delay (Input Path) for Intel Agilex Device* tables. • Removed note to $t_{CF12ST1}$ in the *General Configuration Timing Specifications for Intel Agilex Devices* table. • Updated the *POR Delay Specification for Intel Agilex Devices* table. • Updated the description for clock input peak-to-peak period jitter tolerance parameter in the *External Configuration Clock Source (OSC_CLK_1) Clock Input Requirements* table. • Added notes to $t_{JPSU\ (TDI)}$, $t_{JPSU\ (TMS)}$, t_{JPH}, and t_{JPCO} in the *JTAG Timing Parameters and Values for Intel Agilex Devices* table. • Updated the *AS Timing Parameters for Intel Agilex Devices* table. — Updated the note to T_{do}. — Updated T_{dcsb2b} specification. • Updated the *AS Configuration Serial Input Timing Diagram* to include T_{dcsb2b}. • Removed Maximum Configuration Time Estimation specifications.
2020.06.30	• Updated the *Recommended Operating Conditions for Intel Agilex Devices* table. — Added note to $V_{CCIO\_PIO\_SDM}$. — Removed the note on HPS_PORSEL from t_{RAMP}. HPS_PORSEL pin is not available for Intel Agilex devices. • Added note to T_{ext_delay} in the *AS Timing Parameters for Intel Agilex Devices* table. • Removed SD/MMC configuration mode specifications in the following tables: — *POR Delay Specification for Intel Agilex Devices* — *Maximum Configuration Time Estimation for Intel Agilex Devices*
2020.05.14	Updated $V_{CCFUSEWR\_SDM}$ specifications in the *Recommended Operating Conditions for Intel Agilex Devices* table.

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Document Version	Changes
2020.03.18	• Added the *Absolute Maximum Rating for Intel Agilex Devices* table. • Added *Maximum Allowed Overshoot and Undershoot Voltage* section. • Updated the *Recommended Operating Conditions for Intel Agilex Devices* table. — Updated the typical values for V_{CC} and V_{CCP}. — Added V_{CCR_CORE} specifications. — Updated description for V_{CCPT} and $V_{CCIO\_PIO\_SDM}$. — Updated $V_{CCFUSEWR\_SDM}$ and V_I specifications. — Updated V_{CCA_PLL} specifications and description. — Added a note for T_J minimum specifications for Industrial. — Updated t_{RAMP} minimum specification. • Updated the *E-Tile Transceiver Power Supply Operating Conditions* table. — Updated V_{CCCLK_GXE} for maximum DC level. — Updated V_{CCCLK_GXE} for recommended AC transient level. — Updated wording for all recommended DC values from % of DC level to % of $V_{nominal}$. • Updated wording for all recommended DC values from % of DC level to % of $V_{nominal}$ in the *P-Tile Transceiver Power Supply Operating Conditions*. • Updated the *E-Tile Transmitter and Receiver Data Rate Performance Specifications* table with the transceiver speed grades for the NRZ and PAM4 supported data rates. • Updated the transmitter differential output voltage peak-to-peak typical value in the *E-Tile Transmitter Specifications* table. • Updated the *E-tile Receiver Specifications* table: — Added the absolute V_{max} for a receiver pin specification — Added the maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before/after device configuration specification — Added V_{ICM} (AC coupled) specification — Removed the electrical idle detection voltage specification • Updated *P-Tile Transceiver Performance*: — Added supported data rate for Gen1, Gen 2, Gen 3, and Gen 4 in the *P-Tile Transmitter and Receiver Data Rate Performance* table. — Removed the maximum VCO frequency value and replaced it with a typical value in the *P-Tile PLLA Performance* table. — Removed the maximum VCO frequency value and replaced it with a typical value in the *P-Tile PLLB Performance* table. • Updated *P-Tile Transmitter Specifications*: — Added PCIe condition for Supported I/O Standards. — Removed V_{OCM} (AC Coupled). • Updated *P-Tile Receiver Specifications*: — Added PCIe condition for Supported I/O Standards. — Added PCIe 8.0 GT/s and 16.0 GT/s specifications for the peak-to-peak differential input voltage V_{ID} (diff p-p) and added corresponding notes. — Updated RESREF specification. Added a note to the RESREF specification. • Updated V_{CCL_HPS} and $V_{CCPLLDIG\_HPS}$ specifications for SmartVID in the *HPS Power Supply Operating Conditions for Intel Agilex Devices* table. • Changed *Early Power Estimator (EPE)* to *Intel FPGA Power and Thermal Calculator*.

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Document Version	Changes
	• Added a note to 1.2 V LVCMOS in the *Single-Ended I/O Standards Specifications for Intel Agilex Devices* table. • Added a note in the *Single-Ended SSTL, HSTL, HSUL, and POD I/O Standards Signal Specifications for Intel Agilex Devices* table. • Updated the *Differential I/O Standards Specifications for Intel Agilex Devices* table. — Updated I/O standard name from "1.5 V True Differential Signaling" to "True Differential Signaling (Transmitter & Receiver)". — Added specifications for True Differential Signaling (Receiver only). — Updated note to True Differential Signaling. • Updated the *I/O PLL Specifications for Intel Agilex Devices* table. — Added notes for t_{FCOMP}, t_{OUTPJ_DC}, and t_{OUTCCJ_DC}. — Removed t_{INCCJ} specifications. — Added t_{REFPJ} and t_{REFPN} specifications. — Updated t_{OUTPJ_DC}, t_{OUTCCJ_DC}, t_{OUTPJ_IO}, t_{OUTCCJ_IO}, and $t_{CASC\_OUTPJ\_DC}$ specifications. • Added a note for fixed-point 27 × 27 multiplication mode in the *DSP Block Performance Specifications for Intel Agilex Devices* table. • Updated the *Memory Block Performance Specifications for Intel Agilex Devices* table. — Updated the specifications for MLAB memory. — Updated the specifications for M20K block and added low power (LP) specifications. • Updated the specifications in the *Remote Temperature Diode Specifications for Intel Agilex Devices (Core Fabric TSD)* table. • Added the *Remote Temperature Diode Specifications for Intel Agilex Devices (P-Tile TSD)* table. • Updated the *LVDS SERDES Specifications for Intel Agilex Devices* table. — Updated the tx Jitter - True Differential I/O Standards specifications for –4 speed grade. — Removed global, regional, or local in clock routing resource. • Updated the DPA Lock Time Specifications for Intel Agilex Devices table. — Updated the description of the table. — Updated the maximum data transition from 960 to 768. • Updated the jitter requirements in the *Memory Output Clock Jitter Specifications* section. • Updated the specifications in the *Maximum HPS Clock Frequencies for Intel Agilex Devices* table. • Updated the *HPS Programmable I/O Delay (Output Path) for Intel Agilex Device* and *HPS Programmable I/O Delay (Input Path) for Intel Agilex Device* tables. • Updated the following diagrams: — *USB ULPI Timing Diagram* — *RGMII TX Timing Diagram* — *RMII TX Timing Diagram* — *RMII RX Timing Diagram* • Updated t_{ST0} and t_{CD2UM} specifications in the *General Configuration Timing Specifications for Intel Agilex Devices* table.

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Document Version	Changes
	• Added notes to T_{clk} and T_{do} specifications in the *AS Timing Parameters for Intel Agilex Devices* table. • Updated t_{ADSU} and t_{AVSU} specifications in the *Avalon-ST Timing Parameters for ×8, ×16, and ×32 Configurations in Intel Agilex Devices* table. • Added the following tables: — *Configuration Bit Stream Sizes for Intel Agilex Devices* — *Maximum Configuration Time Estimation for Intel Agilex Devices* — *Programmable IOE Delay for Intel Agilex Devices*
2019.12.18	Updated the *I/O PLL Specifications for Intel Agilex Devices* table. • Removed `scanclk` from $f_{DYCONFIGCLK}$ parameter. • Corrected the maximum specification for $f_{DYCONFIGCLK}$ from 200 MHz to 100 MHz.
2019.04.02	Initial release.