Agilex 7 FPGA Starter Kit

User Manual

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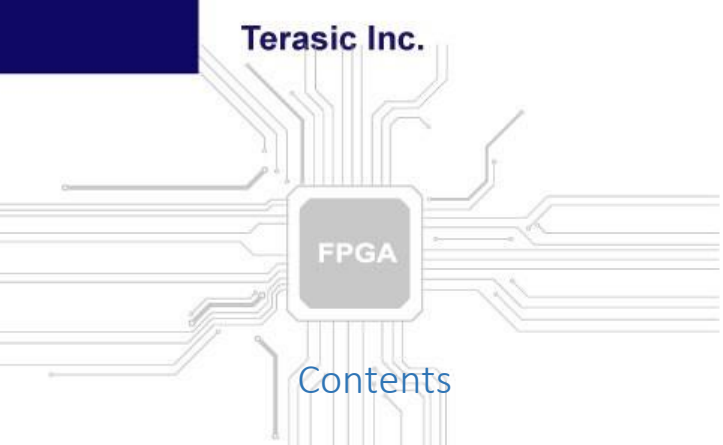


Contents

Chapter 1

Overview

This chapter provides an overview of the **Terasic Agilex 7 FPGA Starter Kit (A7SK)** and installation guide.

1.1 General Description

The Terasic Agilex 7 FPGA Starter Kit takes advantage of the latest Intel Agilex™ 7 FPGA F-Series devices with 2x F-Tile and from 600K to 2.7M logic elements options, offering 50% higher fabric performance and 40% lower power consumption than equivalent Stratix® 10 devices. (Note: Standard kits are built with 2.7M LEs version. Other device options are available for customized requests.)

Combining PCI Express 4.0 x8, one 100G QSFP-28 connector, and offering up to 16GB of DDR4, the Terasic Agilex 7 FPGA Starter Kit provides optimal acceleration and throughput for communications, high-performance computing, data center, and other compute-intensive applications. In addition, the on-board FMC+ connector makes the board extensible and can work with various daughter cards, such as Terasic's HDMI-FMC, XTS-FMC, 12G SDI-FMC and HDMI 2.1 FMC daughter card.

1.2 Key Features

The following hardware is implemented on the Agilex 7 FPGA Starter Kit board:

- **Intel® Agilex™ F-Series**
  - AGFB027R24C2E2V
    - 2.7M logic elements (LEs)

- 287 Mb On-chip RAM (M20K and MLAB)
- 17,056 18-bit x 19-bit multipliers
- 4,510 Variable-precision DSP blocks

FPGA Configuration

- On-Board USB Blaster II (UB2) for FPGA programming and Debug
- AS x4 (QSPI Flash 2048 or 1024 Gbit)

FPGA Fabric

- PCIe Gen4 x8
- DDR4-A: DDR4 SO-DIMM Socket shared with HPS,shipping with 8GB ECC SO-DIMM
- DDR4-B: On-board components 8GB DDR4 with x72 data bus, suppor t ECC (Note)
- One FMC+ connectors with 16 transceivers, supporting VADJ 1.2V
- One QSFP28 Port for 100/40/25/10 GbE network interface
- 2x5 Timing Expansion Header
- User LED x2, Button x2, DIP Switch x2

HPS(Hard Processor System) Fabric

- Quad-core 64 bit ARM Cortex-A53 MPCore* processor
- MicroSD Socket
- DDR4-A: DDR4 SO-DIMM Socket shared with FPGA
- Gigabit Ethernet PHY + RJ45
- UART to USB Port
- LED x1, Button x1, Cold Reset Button

Board Management System

- Power Monitor
- Temperature Monitor
- Auto fan Control

1.3. Block Diagram

Figure 1-1 shows the block diagram of the Agilex 7 FPGA Starter Kit board. To provide maximum flexibility for the users, all key components are connected to the Agilex™ FPGA device. Thus, users can configure the FPGA to implement any system design.

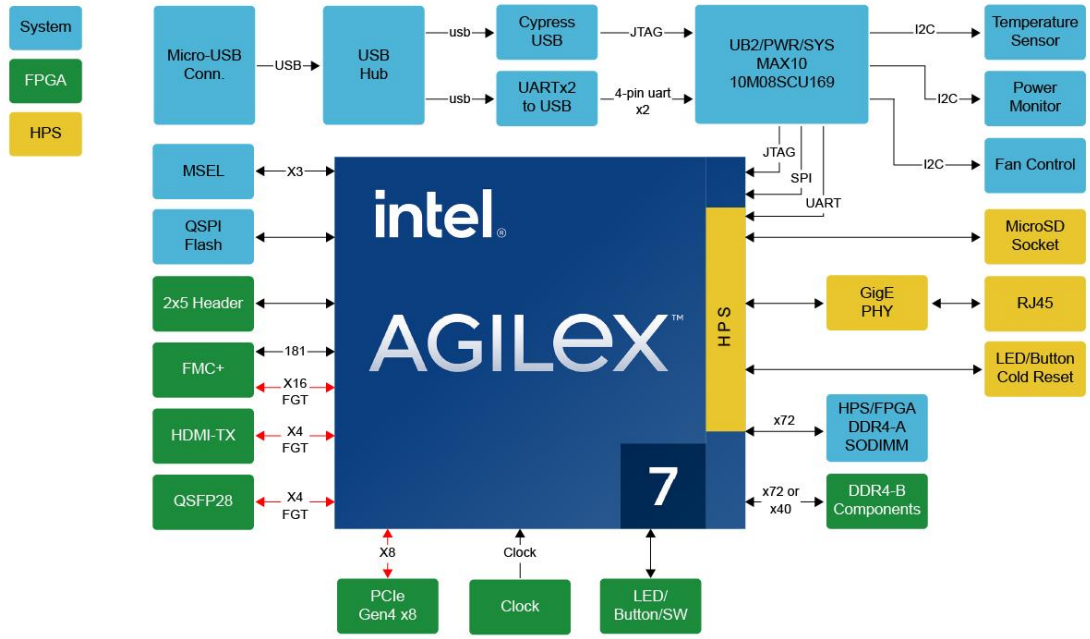


Figure 1-1 Block diagram of the Agilex 7 FPGA Starter Kit board

1.4. Board Power On

The Agilex 7 FPGA Starter Kit board can be used in stand-alone or be installed to the Host through PCIe slot. This section will introduce how to power on the board and the information that user should notice in these two modes.

■ Stand-alone Mode

When the Agilex 7 FPGA Starter Kit board is used in stand-alone mode, users can use the 12V ATX power provided in the kit to connect to the 8-pin 12V ATX power connector (See **Figure 1-2**) of the Agilex 7 FPGA Starter Kit board. To power up the board, user need to turn the power switch **SW2** to “ON” position.

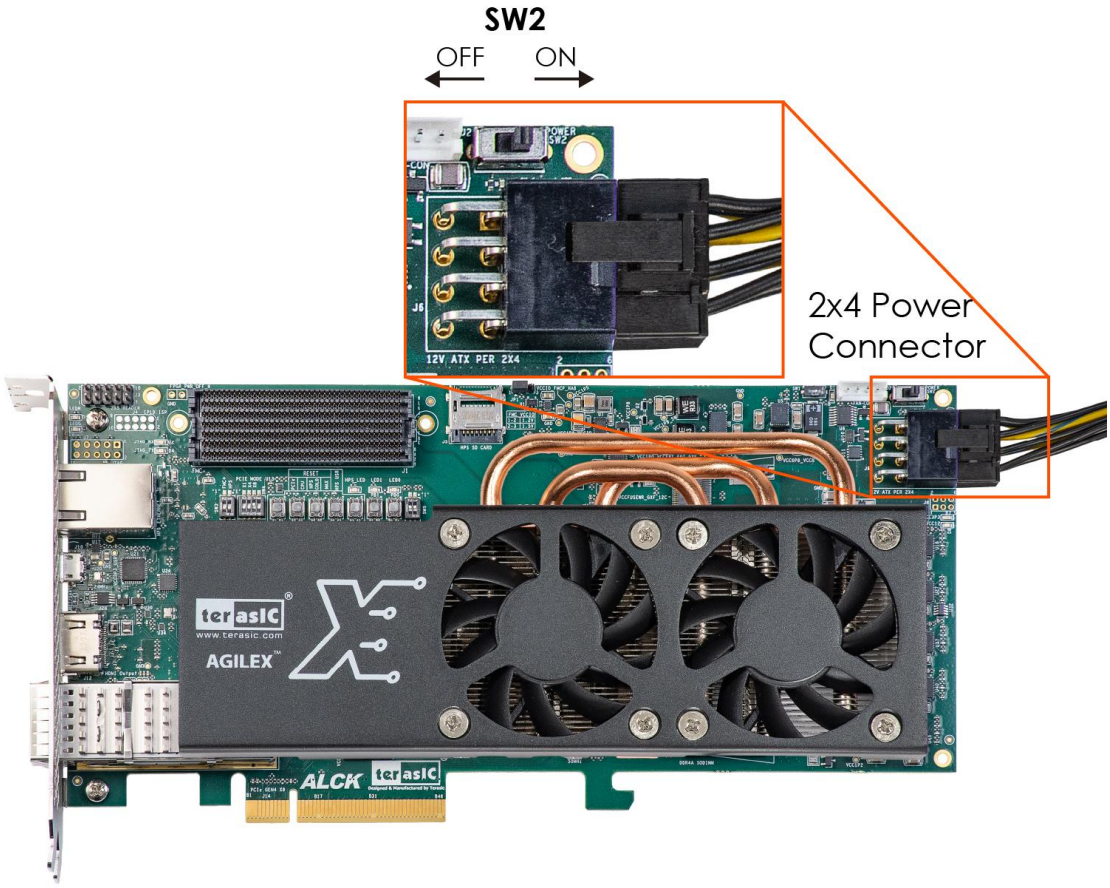


Figure 1-2 Board Power Control Switch

■ Install to Host

When the Agilex 7 FPGA Starter Kit is installed on the Host via PCIe slot. Although the Host can provide power to Agilex 7 FPGA Starter Kit board via PCIe slot, but Terasic strongly recommends that users connect an external power (through the 2x4 ATX power connector) to the board. This can prevent the power provided from Host unable to meet the power requirement of Agilex 7 FPGA Starter Kit. If the power supply to the board is insufficient, it may cause some components to be abnormal.

In order to avoid insufficient power supply to the board, there is a force external power switch (**SW1**) on the board (See **Figure 1-4**). The **SW1** is default set as **ON**. When install the board on the PCIe slot in the PC, users must connect the 2x4 pin 12V DC external power connector to the board, otherwise the board will not be power on. This

restriction is designed to avoid FPGA damage due to insufficient power. Users can set it as **OFF** if the FPGA utilization rate is low and PCIe edge power source is sufficient.

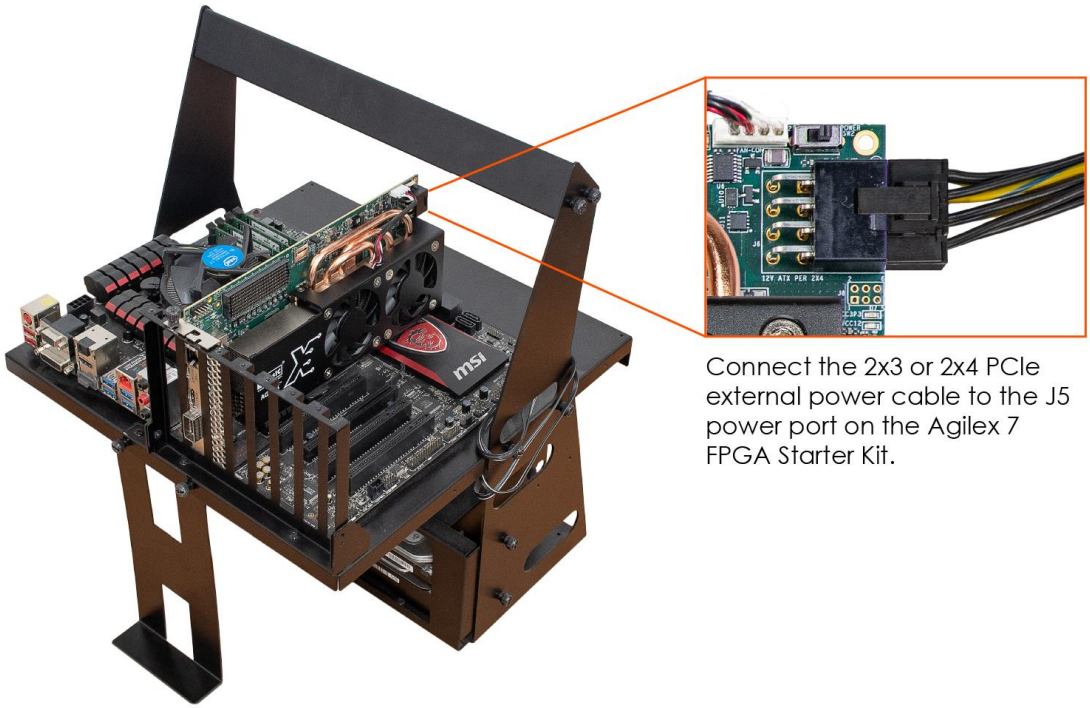


Figure 1-3 Plug external power on the board

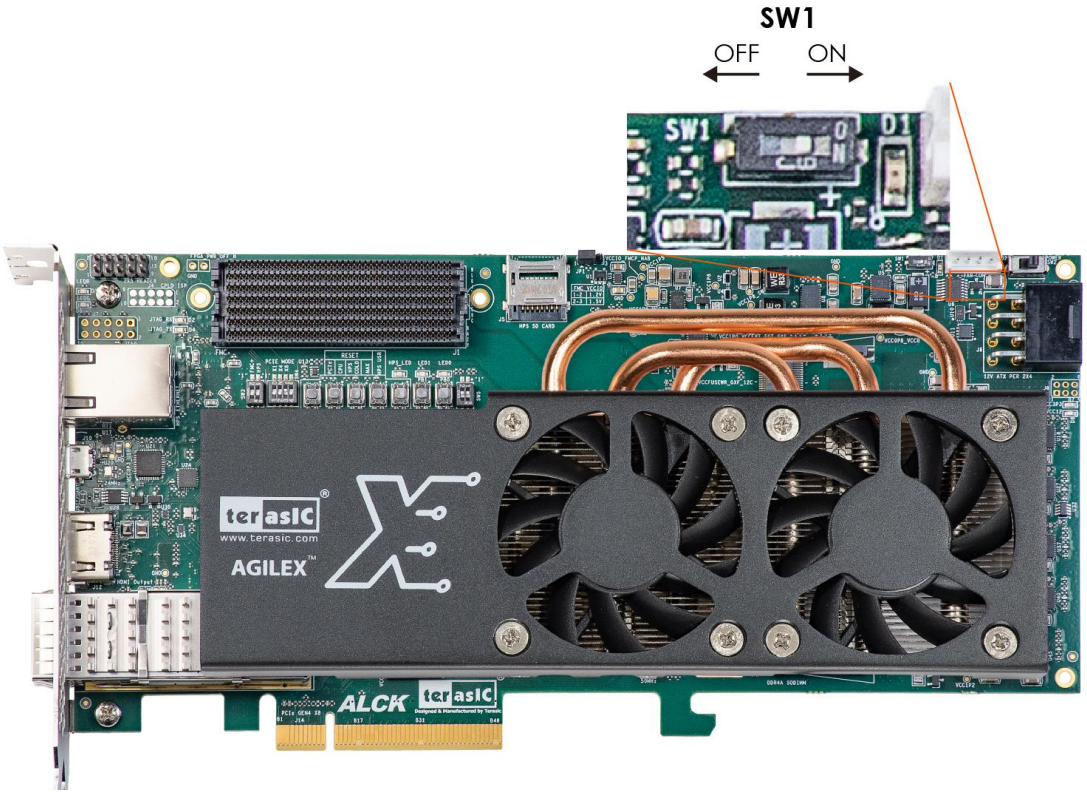


Figure 1-4 Force external power switch

1.5. Install Drivers for USB port

The Micro USB connector on the board provides 3 functions:

- USB blaster II circuit
- HPS USB to UART
- MAX10 USB to UART

The first one is **USB blaster II circuit**, which provides the JTAG interface between host and FPGA board.The second function is the serial communication function of HPS Fabric, which allows Host to communicate or debug with HPS Fabric. The last one is the UART function for board system monitoring. It allows user to monitor the staus on the board such as temperature and fan speed in real time.These three functions are all connected to the Micro USB connector through the USB hub. The user only needs to connect the host with a USB cable to the board to realize these

three functions.

At the same time, some drivers need to be installed on the host to use these functions. Users can refer to the following steps.

1. Please refer to this link to install USB Blaster II driver : Terasic Wiki

2. For the UART driver of HPS and system monitoring, please refer to section 3.1.

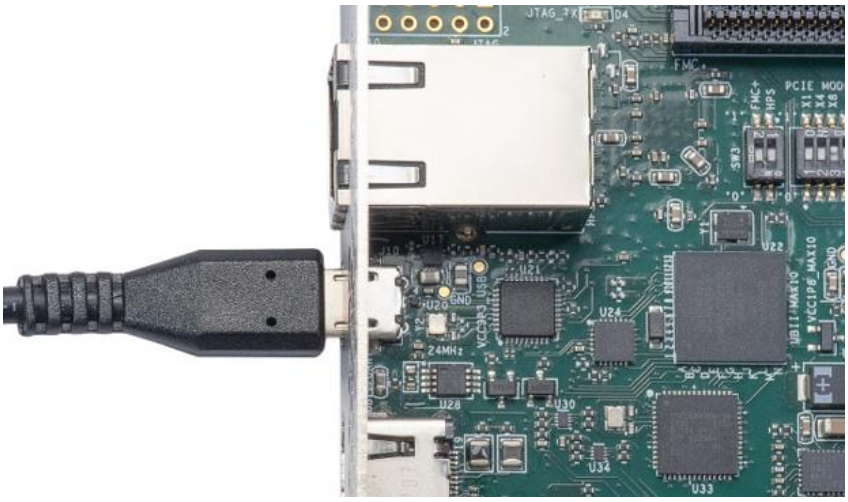


Figure 1-5 The Micro USB port

2.1. Board Protection

The temperature of Agilex 7 FPGA Starter Kit board will have a lot to do with the user's design code, chassis, and ambient temperature. When using Agilex 7 FPGA Starter Kit board in the server. Customers should pay attention to whether the temperature of Agilex 7 FPGA Starter Kit board is too high to avoid abnormal work for user's design or even damage to the board.

The **Dashbaord_gui** software (see chapter 3 of this user manual) is provided in the system CD to allow users to monitor the temperature status of the board. A temperature monitor IP (see section 2.4 in the demonstration manual) is also provided so that the user can directly monitor the temperature status in the Agilex FPGA.

If the board temperature is too high, it is recommended that customers can switch the PCIe slot position in the server chassis or increasing the fan strength in the chassis, or replace the chassis to a big space, or reduce the ambient temperature to improve cooling system.

In addition, the efficiency of the Agilex 7 FPGA Starter Kit cooling system will decrease with the aging of dust and fans, so customers should re-evaluate the cooling efficiency regularly.

2.2. Mechanical Specifications

Figure 1-6 shows the Mechanical Layout of Agilex 7 FPGA Starter Kit. The unit of the Mechanical Layout is millimeter (mm).

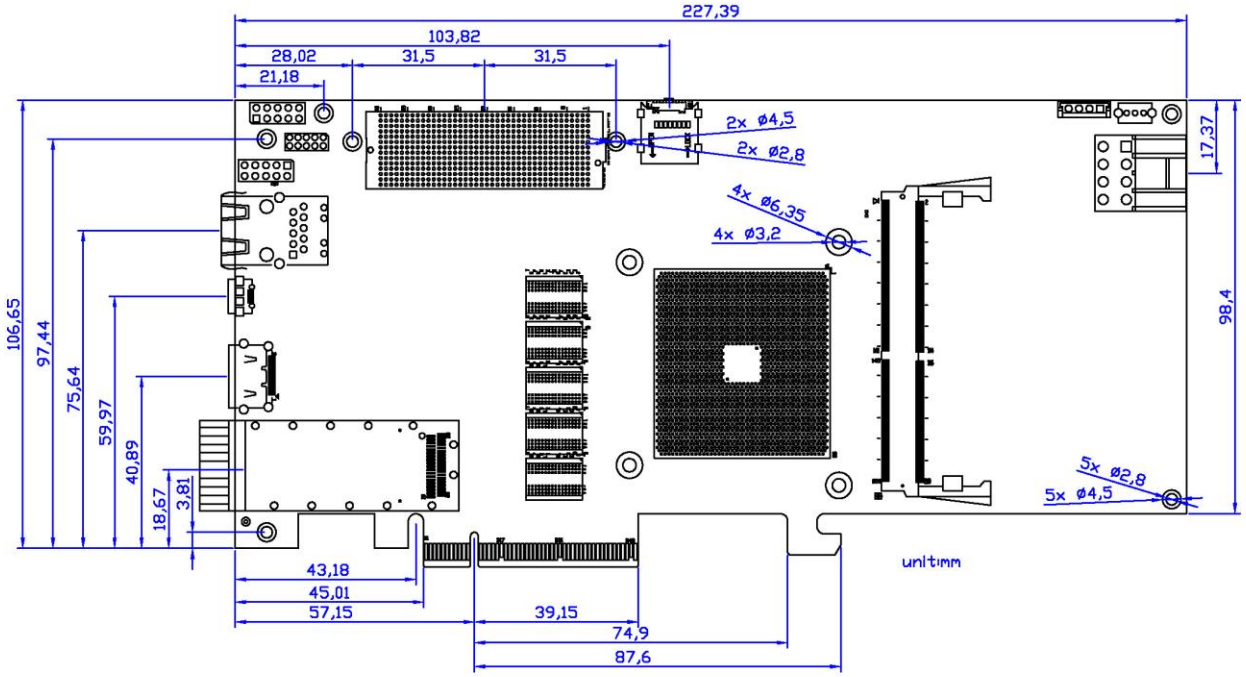


Figure 1-6 Mechanical layout

Chapter 2

Board Component

This chapter introduces all the important components on the Agilex 7 FPGA Starter Kit.

2.1 Board Overview

Figure 2-1 and **Figure 2-2** is the top and bottom view of the Agilex 7 FPGA Starter Kit development board. It depicts the layout of the board and indicates the location of the connectors and key components. Users can refer to this figure for relative location of the connectors and key components.

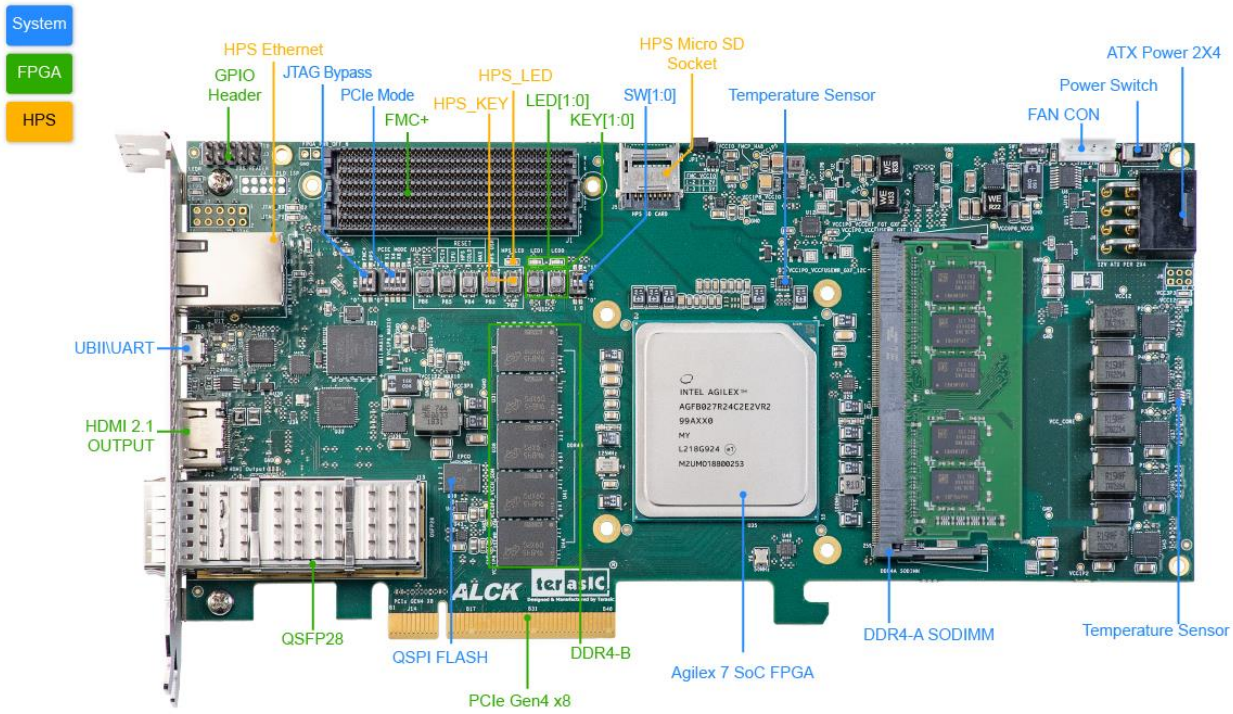


Figure 2-1 FPGA Board (Top)

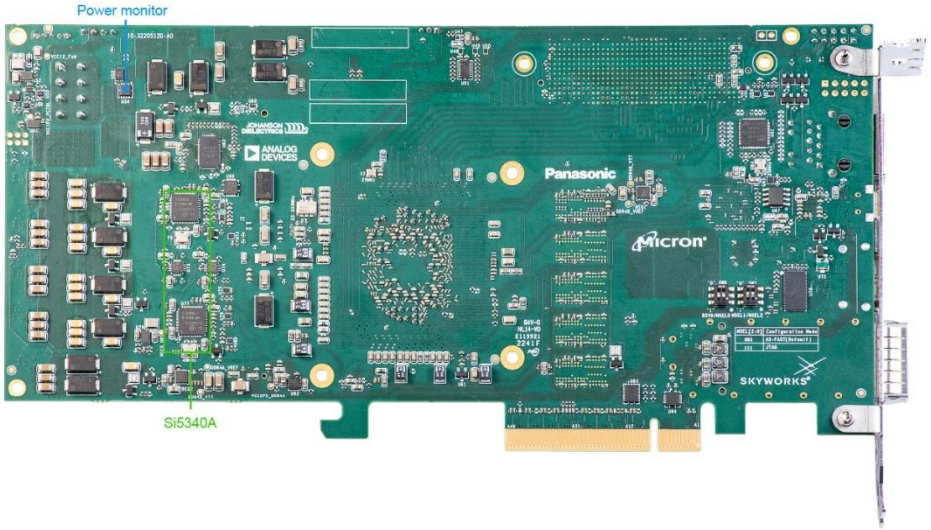


Figure 2-2 FPGA Board (Bottom)

2.2 Configuration

This section describes the configuration mode for Intel Agilex® 7 device available on the Board. The peripheral circuits and usage scenarios for each mode will be listed.

As shown in **Figure 2-3**, the mode select pin of the FPGA on the Agilex 7 FPGA Starter Kit has been set to **Active Serial (AS) Fast mode** using switches. Thus, the Agilex 7 FPGA Starter Kit supports the following configuration modes:

- JTAG Mode (Configure the FPGA using the on-board USB Blaster II, MSEL[2:0] = 3'b111).
- Active Serial Fast mode (MSEL[2:0] = 3'b001)

Users can use these modes to configure the FPGA or HPS (Hardware Process System) fabric in the Intel Agilex® 7 device and make the FPGA to run the user's logic or boot the HPS to run the OS.

Below we will introduce more detailed information of AS mode, as well as other configuration information.

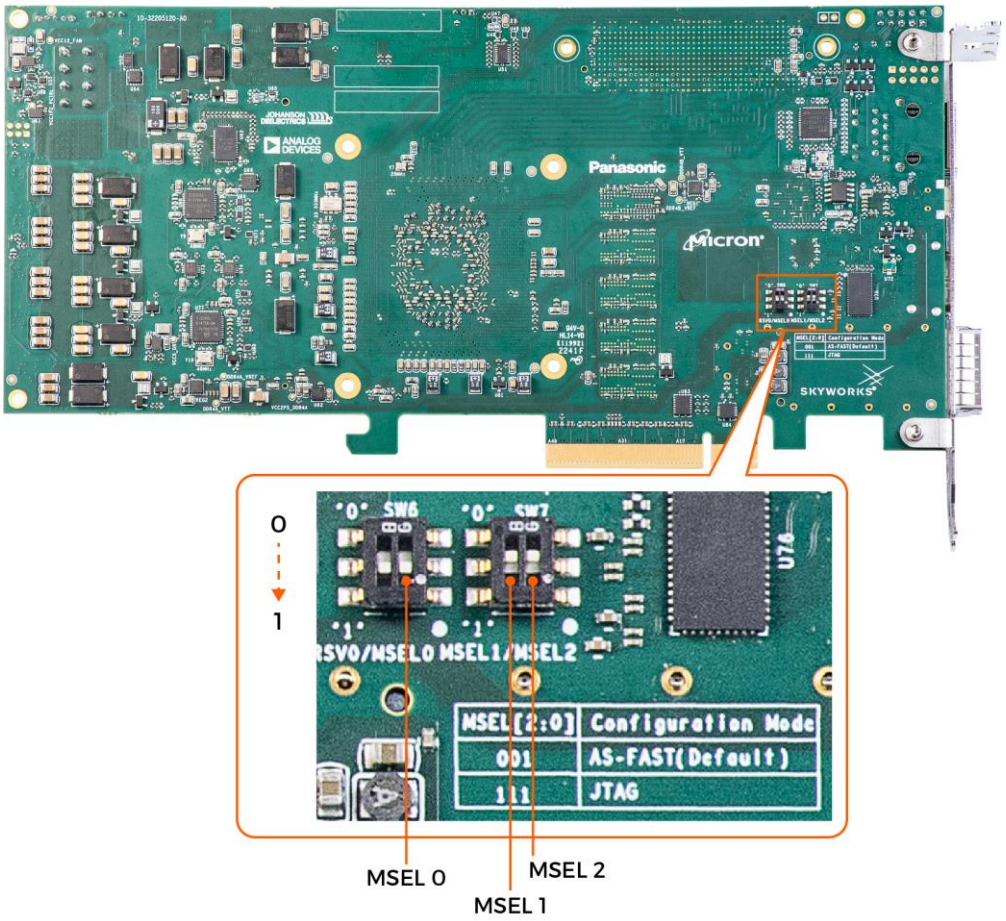


Figure 2-3 The MSEL pin setting

■ Active Serial (Fast) mode

In AS mode, the FPGA's configuration file is stored in the QSPI flash. The Secure Device Manager (SDM) in Intel Agilex® 7 device is responsible for the entire AS mode process and interface. The SDM will load the initial configuration firmware from the QSPI flash to configure the FPGA including FPGA I / O and core configuration. HPS part of the boot can also be completed in this mode. **Figure 2-4** shows the architecture of the AS mode of the Agilex 7 FPGA Starter Kit.

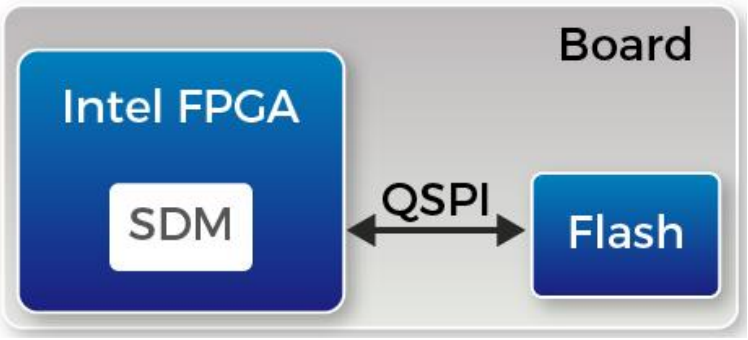


Figure 2-4 AS mode for the Agilex 7 FPGA Starter Kit

For more information on the configuration of Intel Agilex® 7 devices, please refer to the file: Intel Agilex Configuration User Guide

■ SoC FPGA boot

The boot process for Intel Agilex® 7 device can be divided into two different methods:

- FPGA Configuration First Mode
- HPS Boot First Mode

The difference between the two methods is the initial difference between HPS and FPGA fabric after powering on. More details can be found in the user documentation: Intel® Agilex™ SoC FPGA Boot User Guide.

The factory setting of the SoC boot of the Agilex 7 FPGA Starter Kit is the **FPGA Configuration First Mode**. The architecture is shown in the **Figure 2-5**. Two storage mediums are used. The system needs QSPI flash on Board as SDM flash for booting.

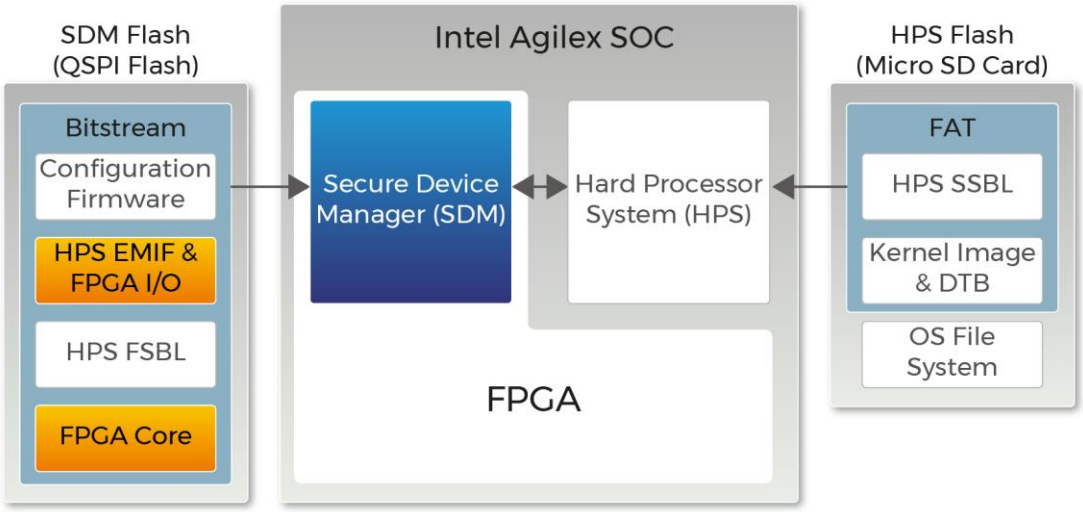


Figure 2-5 FPGA Configuration First Dual SDM and HPS Flash

The QSPI flash memory has the following boot data for the first part of the SoC FPGA configuration:

- Configuration firmware for the SDM
- FPGA I/O and HPS external memory interface (EMIF) I/O configuration data
- FPGA core configuration data
- HPS First-Stage Boot Loader(FSBL) code and FSBL hardware handoff binary data

Meanwhile, Terasic provides the micro SD card with built-in image data as HPS flash, which is used for HPS boot in the later part. The micro SD card stores the following data:

- Second-Stage Boot Loader(SSBL)
- Kernel Image and Device Tree Blob(DTB)
- Operating System

The factory SoC boot process of Board is summarized as follows:

When the Agilex 7 FPGA Starter Kit is powered on, the SDM will read the configuration firmware and complete SDM initial form the QSPI flash according to the MSEL pin setting. Then, the SDM will configure the FPGA I/O and core (full configuration).

After the FPGA is first configured, SDM continues to load the FSBL(First-Stage Boot Loader) from the QSPI flash and transfer it to the HPS on-chip RAM, and releases the HPS reset to let the HPS start using the FSBL hardware handoff file to setup the clocks, HPS dedicated I/Os, and peripherals.

The FSBL then loads the SSBL(Second-Stage Boot Loader) from the Micro SD Card into HPS SDRAM and passes the control to the SSBL. The SSBL enables more advanced peripherals and loads OS into SDRAM.

Finally, the OS boots and applications are scheduled for runtime launch.

■ JTAG Programming

The JTAG interface of the Board is mainly implemented by the USB Blaster II circuit on the board. For programming by on-board USB Blaster II, the following procedures show how to download a configuration bit stream into the Intel Agilex® 7 device:

- Make sure that power is provided to the FPGA board
- Connect your PC to the FPGA board using a micro-USB cable and make sure the USB Blaster II driver is installed on the PC.
- Launch Quartus Prime programmer and make sure the USB Blaster II is detected.
- In Quartus Prime Programmer, add the configuration bit stream file (.sof), check the associated “Program/Configure” item, and click “Start” to start FPGA programming.

2.3 Status and Setup Components

■ Status LED

The FPGA Board development board includes board-specific status LEDs to indicate board status. Please refer to **Figure 2-6** and **Table 2-1** for the description of the LED indicator.

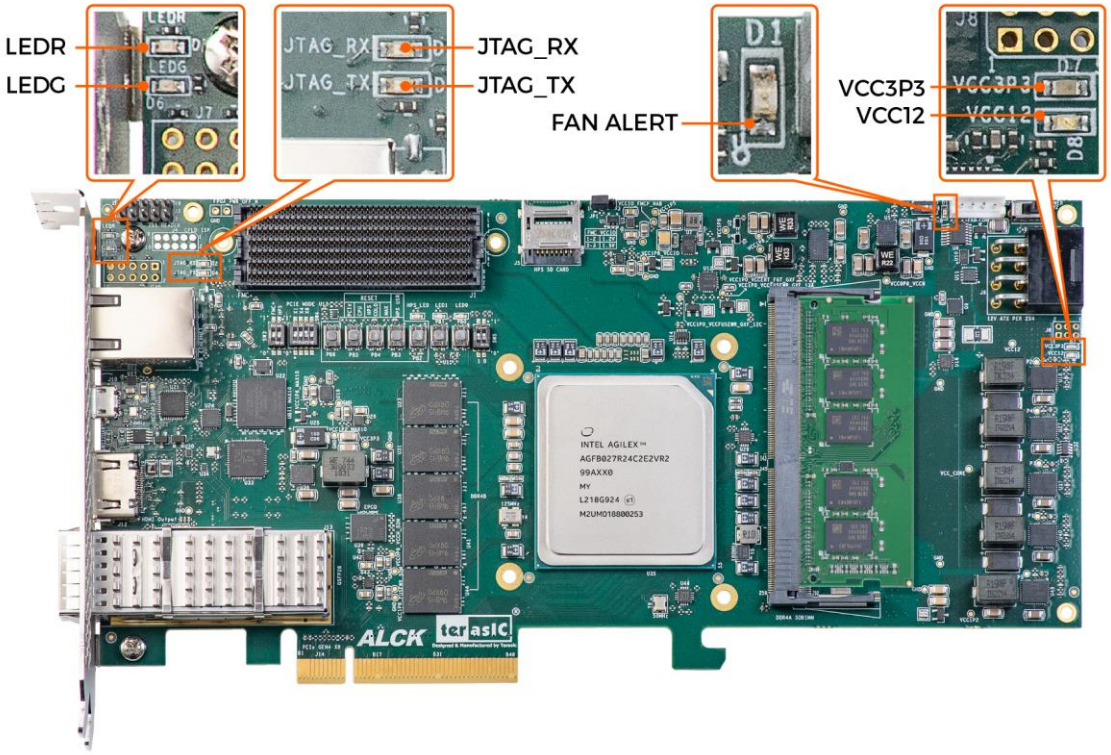


Figure 2-6 Position of the status LED

Table 2-1 Status LED

Board Reference	LED Name	Description
D8	12-V Power	Illuminates when 12-V power is active.
D7	3.3-V Power	Illuminates when 3.3-V power is active.
D1	FAN_ALERT_n	Illuminates when the fan is abnormal, such as when the fan speed is different from expected
D6	POWER_LEDG	Illuminates when the 3.3V power good and power sequence process finished. (*1)
D5	POWER_LEDR	Illuminates when the 3.3V power abnormal or power sequence process failed. (*1)
D2	JTAG_RX	Illuminates when the USB Blaster II circuit is transmitting data

D4	JTAG_TX	Illuminates when the USB Blaster II circuit is receiving data

■ Setup PCI Express Control DIP switch

The PCI Express Control DIP switch (SW8) is provided to enable or disable different configurations of the PCIe Connector (See **Figure 2-7**). **Table 2-2** lists the switch controls and description.

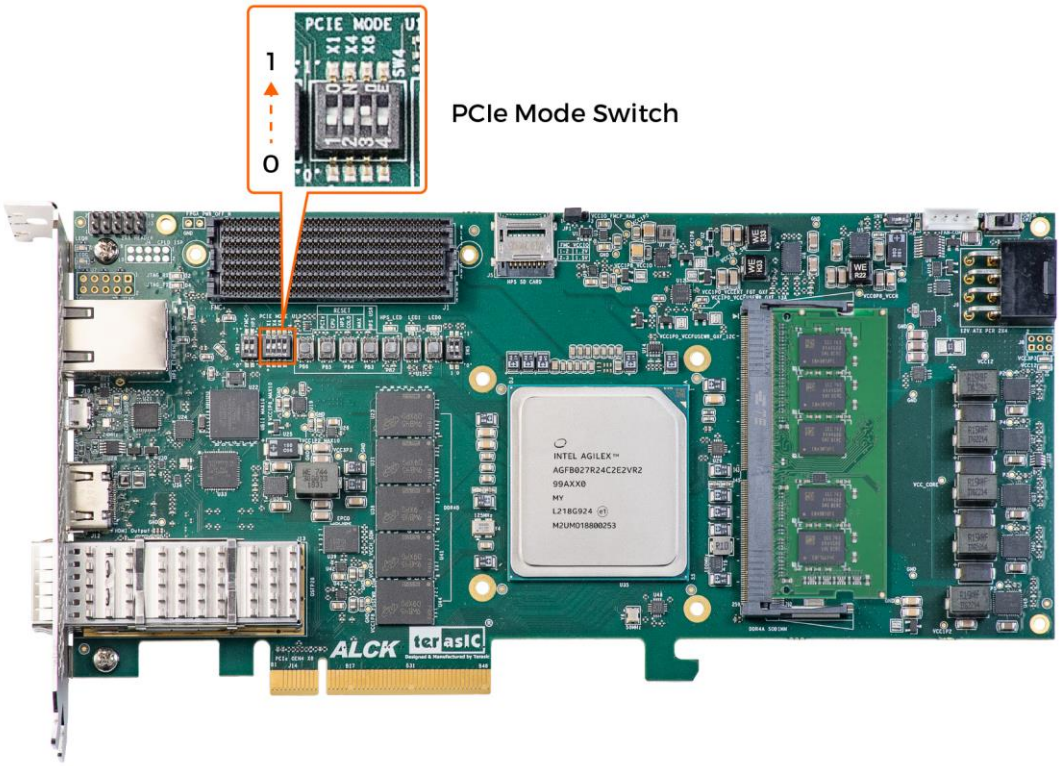


Figure 2-7 Position of the PCIe mode switch

Table 2-2 SW8 PCIe Control DIP Switch

Board Reference	Signal Name	Description	Default
SW4.1	PCIE_PRSNT2n_x1	On : Enable x1 presence detect Off: Disable x1 presence detect	Off
SW4.2	PCIE_PRSNT2n_x4	On : Enable x4 presence detect Off: Disable x4 presence detect	Off

SW4.3	PCIE_PRSNT2n_x8	On : Enable x8 presence detect Off: Disable x8 presence detect	On
SW4.4	N.C	--	--

■ Setup Configure Mode

The **SW7** and **SW6** slide switches (see **Figure 2-8**) are used to specify the configuration mode of the FPGA. As currently only AS Fast and JTAG mode are supported.

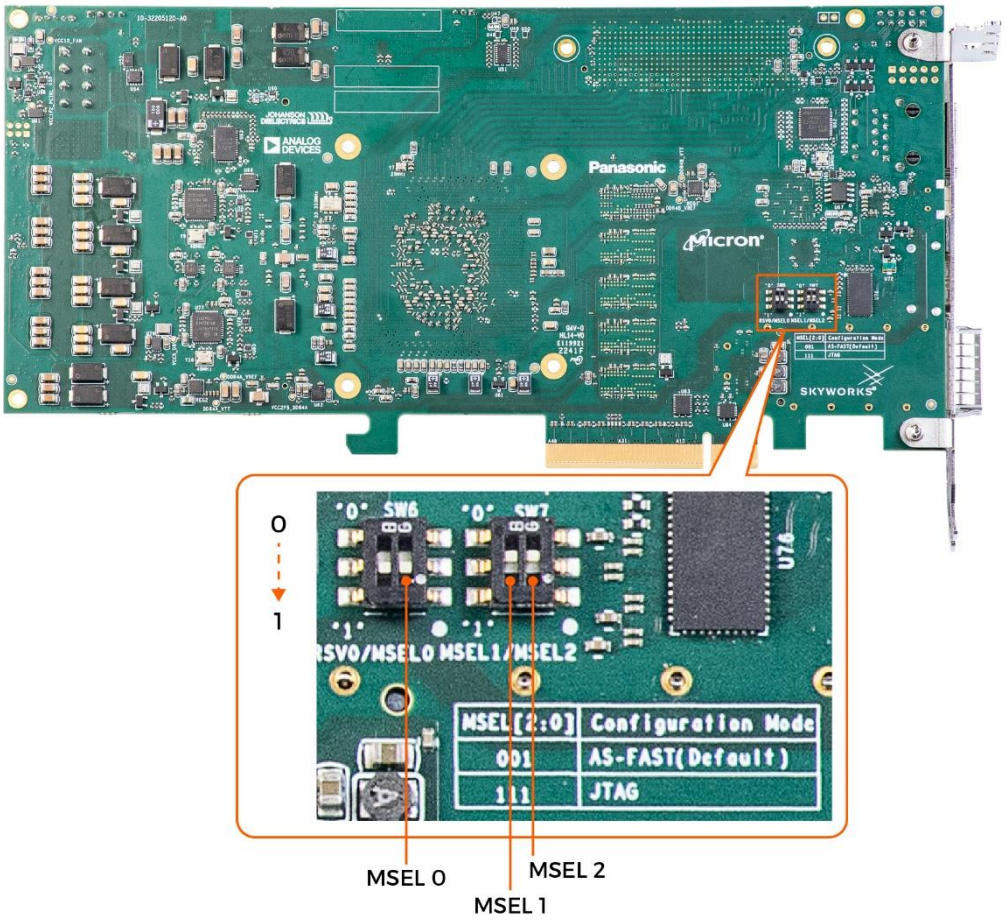


Figure 2-8 Position of slide switches SW6 and SW7 for Configuration Mode

Table 2-3 MSEL Settings for supported configuration Scheme of the board

FPGA Configuration Mode	MSEL2	MSEL1	MSEL0
AS Fast (Default)	0	0	1

JTAG	1	1	1

■ JTAG Bypass Switch

The JTAG interface switch SW3 is to set whether the JTAG interface of the HPS fabric and FMC + connector is connected to the JTAG chain in the board. Both the HPS and FMC+ connector will not be included in the JTAG chain if the switches are set to ON position (See **Figure 2-9**).**Table 2-4** lists the setting of the SW3. Note, if the user turns any of the position on SW3 to the OFF position, but does not connect the JTAG device on the HPS or FMC+ connector. The JTAG chain on the board will not be able to form a closed loop and Quartus will not be able to detect the FPGA device.

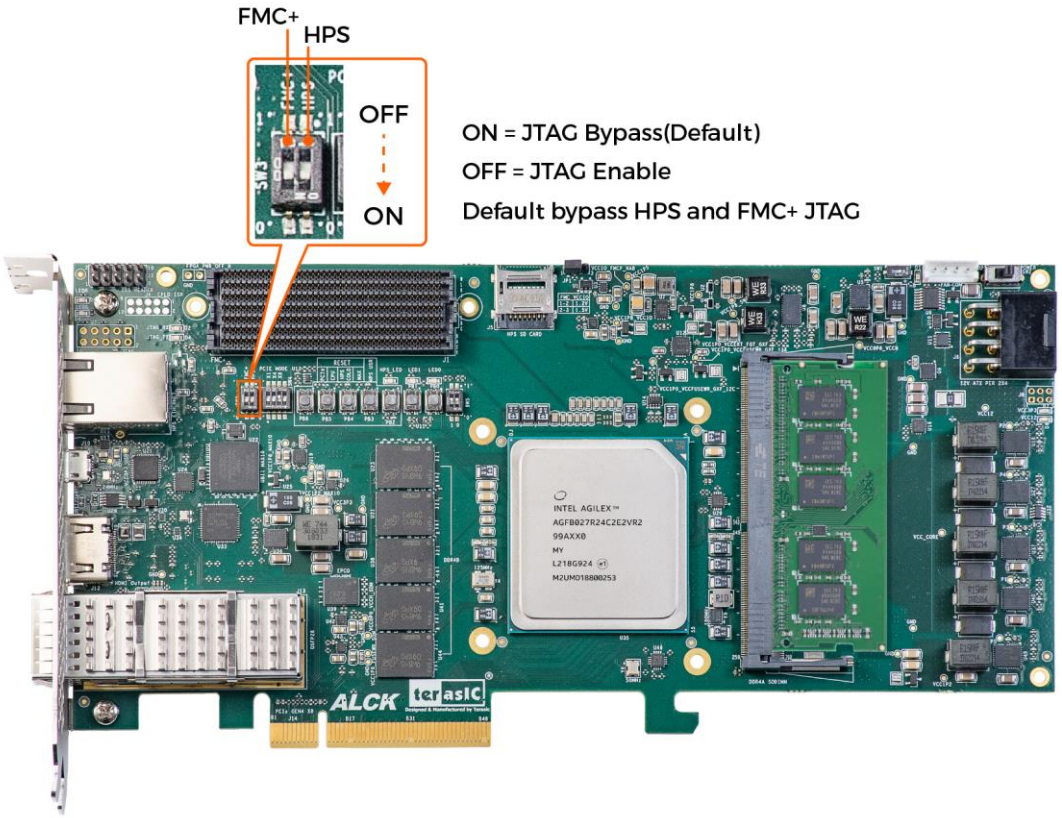


Figure 2-9 JTAG Bypass Switch

Table 2-4 SW3 setting

Board Reference	Signal Name	Description	Default

SW3.1	HPS_JTAG_BYPASS_n	**ON** : **Disable** the JTAG interface of the **HPS** into the JTAG chain **OFF**: **Enable** the JTAG interface of the **HPS** into the JTAG chain	ON
SW3.2	FMCP_JTAG_BYPASS_n	**ON** : **Disable** the JTAG interface of the **FMC+** connector into the JTAG chain **OFF**: **Enable** the JTAG interface of the **FMC+** connector into the JTAG chain	ON

■ FMC_VCCIO Select Header

Some of the FPGA pin's I/O standard connected with the HPC (High Pin Count) part of the **FMC+ connector** can be set to voltages: 1.5V and 1.2V (See **Table 2-5**). This function can be achieved because the VCCIO power pin of the FPGA bank where these FPGA I/Os are located can adjust the input voltage through the 3 pin header (JP1). **Figure 2-10** shows the position of the JP1. **Table 2-6** list the setting for the JP1, user can short 2 pins of the header to modify the voltage level of the VCCIO_FMCP_HAB.

Table 2-5 FPGA I/Os on the FMC+ connector which can be changed I/O standard to 1.2 or 1.5V

FMC+ Pins which can modify I/O stadnard
FMCP_HA_p[23..0]
FMCP_HA_n[23..0]
FMCP_HB_p[21..0]
FMCP_HB_p[21..0]
FMCP_HB_n[21..0]
FMCP_CLK_M2C_p1
FMCP_CLK_M2C_n1

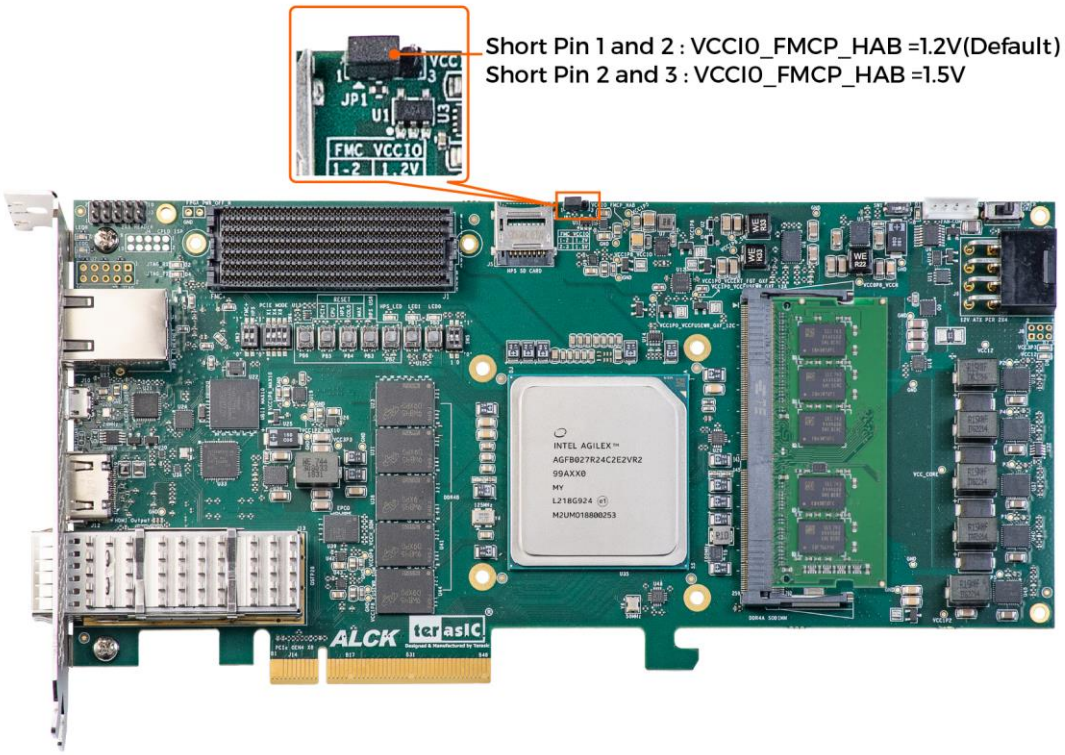
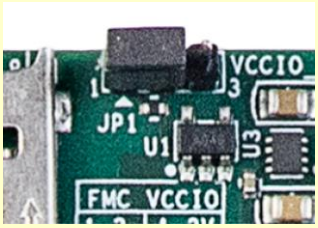


Figure 2-10 FMC and FMC+ I/O standard setting headers

Table 2-6 JP3 Setting for FMC+ I/O standard

JP3 Setting	FMC I/O Standard
	1.2V (Default)
	1.5V

2.4 Reset Devices

The board provides 4 reset buttons for different system reset situations (see **Figure 2-11**). These buttons can reset FPGA, System MAX, HPS and FPGA respectively. Please refer to the following **Table 2-7** for details.

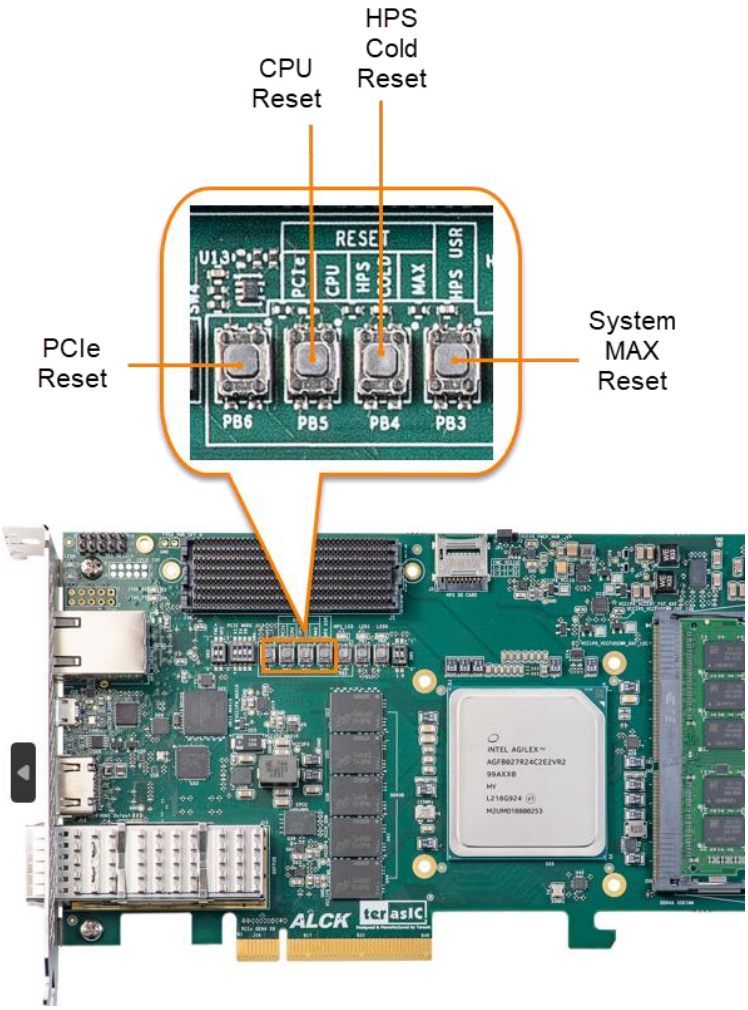


Figure 2-11 Rest devices of the board

Table 2-7 Reset Devices Pin Assignments, Schematic Signal Names, and Functions

Part Number	Schematic Signal Name	I/O Standard	Agilex Pin Number	Application
PB5	CPU_RESET_n	1.2V	PIN_A49	This button can be used for rest FPGA
PB3	MAX_RESET_n	--	--	For resetting System MAX10
PB4	HPS_COLD_RESET_N	--	--	For resetting System HPS Fabric
PB6	PCIE_PERST_n	1.2V	PIN_BR43	PCIe reset

2.5 General User Input/Output

This section describes the user I/O interface of the FPGA. **Figure 2-12** shows the position of all these components and interface.

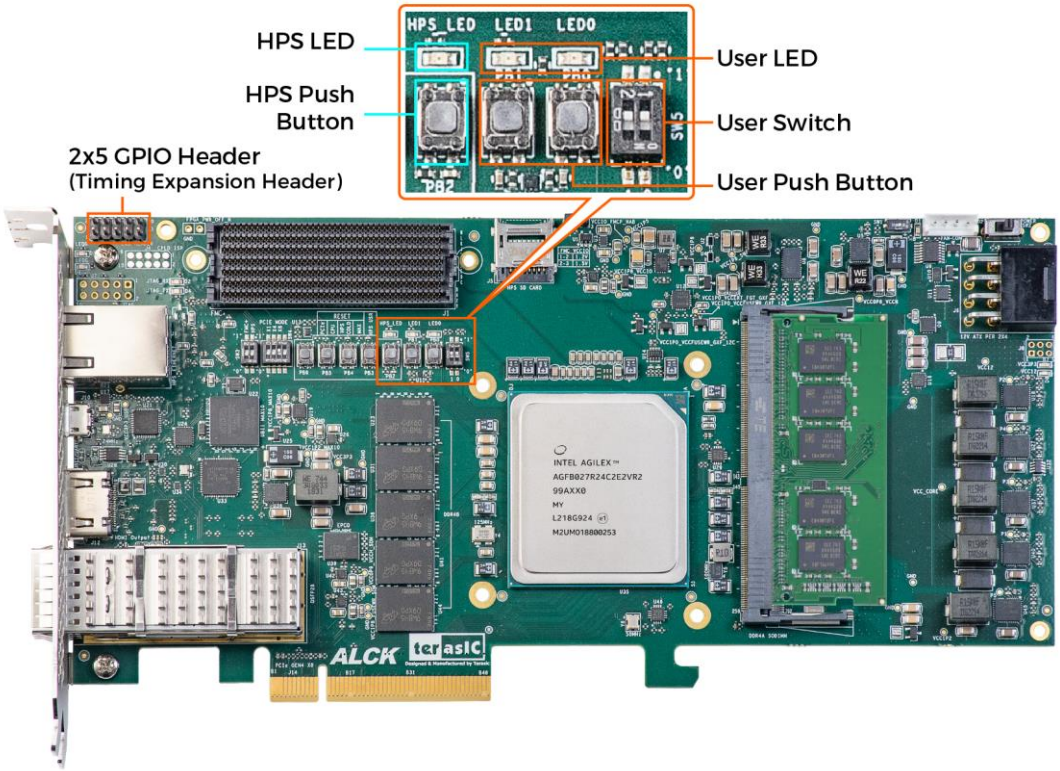


Figure 2-12 Position of all the general user components

■ User Defined Push-buttons

The FPGA board includes two user defined push-buttons that allow users to interact with the Agilex device. Each push-button provides a high logic level or a low logic level when it is not pressed or pressed, respectively. **Table 2-8** lists the board references, signal names and their corresponding Agilex device pin numbers.

Table 2-8 Push-button Pin Assignments, Schematic Signal Names, and Functions

Board Reference	Schematic Signal Name	Description	I/O Standard	Agilex Pin Number
PB0	BUTTON0	High Logic Level when the button is not pressed	1.2V	PIN_DA9
PB1	BUTTON1		1.2V	PIN_CY8

■ User-Defined Dip Switch

There are two positions dip switches (SW5) on the FPGA board to provide additional FPGA input control. When a position of dip switch is in the DOWN position or the UPPER position, it provides a low logic level or a high logic level to the Agilex FPGA, respectively.

Table 2-9 lists the signal names and their corresponding Agilex device pin numbers.

Table 2-9 Push-button (FPGA) Pin Assignments, Schematic Signal Names

Board Reference	Schematic Signal Name	Description	I/O Standard	FPGA Pin Number
SW0	SW0	High logic level when SW in the UPPER position.	1.2 V	PIN_DD16
SW1	SW1		1.2 V	PIN_ DC17

■ User-Defined LEDs

The FPGA board consists of 4 user-controllable LEDs and a housing LED lamp with four LEDs to allow status and debugging signals to be driven to the LEDs from the designs loaded into the Agilex device. Each LED is driven directly by the Agilex FPGA. The LED is turned on or off when the associated pins are driven to a low or high logic level, respectively. A list of the pin names on the FPGA that are connected to the LEDs is given in **Table 2-10**.

Table 2-10 User LEDs Pin Assignments, Schematic Signal Names, and Functions

Board Reference	Schematic Signal Name	Description	I/O Standard	Agilex Pin Number
LED0	LED0	Driving a logic 0 on the I/O port turns the LED ON.	1.2V	PIN_DD8
LED1	LED1	Driving a logic 1 on the I/O port turns the LED OFF.	1.2V	PIN_DC9

■ 2x5 GPIO Header (Timing Expansion Header)

The FPGA board has one 2x5 GPIO header J5 for expansion function. The pin-out of J5 is shown in **Figure 2-13**. GPIO_P0 ~ GPIO_P3 are bi-direction 1.2V GPIO. GPIO_CLK0 and GPIO_CLK1 are connected to FPGA dedicated clock input and can be configured as two single-ended clock signals. **Table 2-11** shows the mapping of the

FPGA pin assignments to the 2x5 GPIO header.

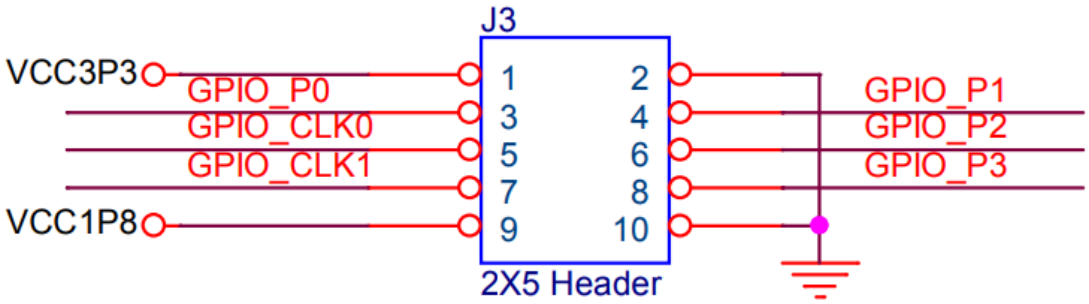


Figure 2-13 Pin-out of 2x5 expansion header

Table 2-11 2x5 GPIO Header Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	Description	I/O Standard	Agilex Pin Number
GPIO_P0	Bi-direction 1.2V GPIO	1.2V	PIN_J43
GPIO_P1	Bi-direction 1.2V GPIO	1.2V	PIN_K46
GPIO_P2	Bi-direction 1.2V GPIO	1.2V	PIN_G45
GPIO_P3	Bi-direction 1.2V GPIO	1.2V	PIN_D50
GPIO_CLK0	FPGA dedicated clock input or Bi-direction 1.2V GPIO	1.2V	PIN_J45
GPIO_CLK1	FPGA dedicated clock input or Bi-direction 1.2V GPIO	1.2V	PIN_G49

2.6 Clock Circuit

The development board includes several oscillator (25/50/33.33/100/125 MHz) and two programmable clock generators. **Figure 2-14** shows the default frequencies of on-board all external clocks going to the Agilex FPGA.

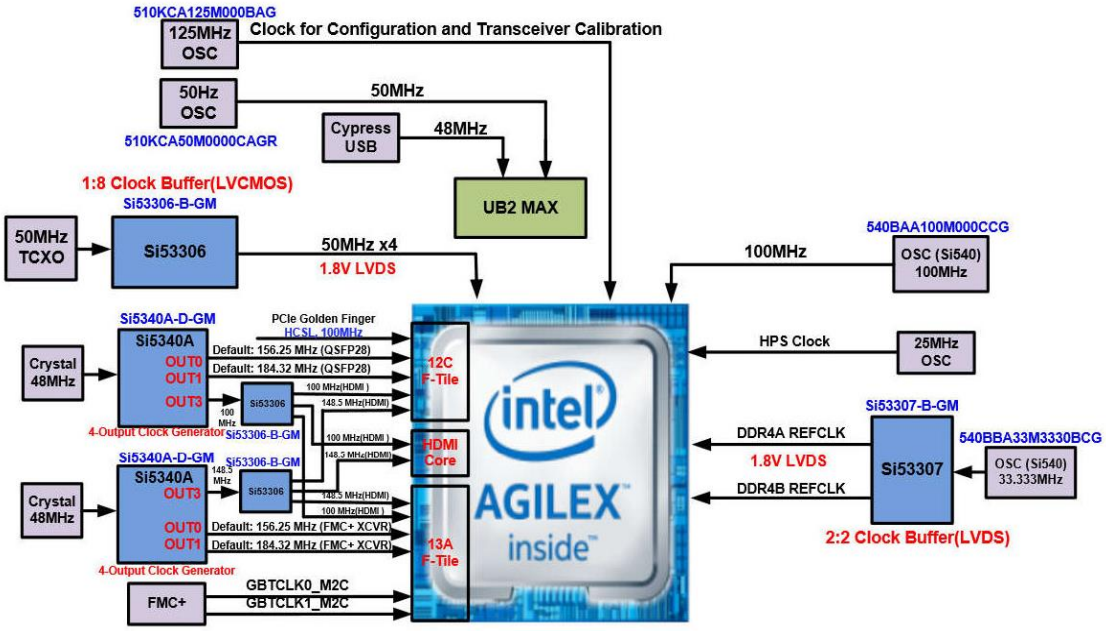


Figure 2-14 Clock circuit of the FPGA Board

A clock buffer (Si53306) is used to duplicate the 50 MHz TCXO output clock, so there are four 50MHz clocks fed into different Agilex FPGA banks. Two programming clock generators (Si5340A) with low-jitter clock output which are used to provide special and high-quality clock signals for high-speed transceivers for QSFP28, HDMI and FMC interfaces.

For memory interface, the board provide a 33.333Mhz clock and fan out it to two different clocks to the Agilex FPGA via clock buffer (Si53307). The two clocks are used for the reference clock of the DDR4 SODIMMs and the on-chip DDR4 devices.

Finally, for PCIe application, the board uses the clock output on the PCIe edge connector to Agilex FPGA.

Table 2-12 lists the clock source, signal names, default frequency and their corresponding Agilex device pin numbers.

Table 2-12 Clock Source, Signal Name, Default Frequency, Pin Assignments and Functions

Source	Schematic Signal Name	Default Frequency	I/O Standard	Agilex Pin Number	Application
U46	CLK_50_B2D_p	50.0 MHz	LVDS	PIN_DD12	User application
	CLK_50_B2E_p		LVDS	PIN_CM52	User application
	CLK_50_B3A_p		LVDS	PIN_R41	User application
	CLK_50_B3C_p		LVDS	PIN_E17	User application
Y5	CLK_100_B3A_p	100.0MHz	LVDS	PIN_L43	User application
U68	FMCP_REFCLK_p0	156.25 MHz	LVDS	PIN_ BP8	FMC+ application
	FMCP_REFCLK_p1	184.32 MHz	LVDS	PIN_A24	FMC+ application
	FMCP_REFCLK_p3(*1)	148.5Mhz	LVDS	PIN_BH8	FMC+ application
	CLK_148M5_p(*1)	148.5Mhz	LVDS	PIN_G43	User application
	HDMI_REFCLK_148M5_p(*1)	148.5Mhz	LVDS	PIN_ AB46	HDMI application
U77	QSFP28_REFCLK_p0	156.25 MHz	LVDS	PIN_AN49	QSFP28 application
	QSFP28_REFCLK_p1	184.32 MHz	LVDS	PIN_AJ49	QSFP28 application
	HDMI_REFCLK_100_p(*2)	100MHz	LVDS	PIN_ AD48	HDMI application
	FMCP_REFCLK_p2(*2)	100MHz	LVDS	PIN_BW7	FMC+ application
	CLK_100 _p(*2)	100.0MHz	LVDS	PIN_E45	User application
Y4	OSC_CLK_1	125MHz	LVDS	PIN_CC60	User-supplied configuration clock
Y8	DDR4A_REFCLK_p	33.333 MHz	LVDS	PIN_DD36	DDR4 reference clock for SODIMM
	DDR4B_REFCLK_p	33.333 MHz	LVDS	PIN_U5	DDR4 reference clock for on-chip devices

(*1) Fan-out by Si53306 clock buffer (U73).

(*2) Fan-out by Si53306 clock buffer (U74).

Table 2-13 lists two SI5340A programming clock generator (U68 and U77) control pin, signal names, I/O standard and their corresponding Agilex device pin numbers.

Table 2-13 Programmable clock generator control pin, Signal Name, I/O standard, Pin Assignments and Descriptions

Programmable clock generator	Schematic Signal Name	I/O Standard	Agilex Pin Number	Description
Si5340A (U77)	SI5340A0_I2C_SCL	1.2V	PIN_D44	I2C bus, connected with Si5397A
	SI5340A0_I2C_SDA	1.2V	PIN_B46	
	SI5340A0_OE_n	1.2V	PIN_D40	Si5340A output enable signal
	SI5340A0_RST_n	1.2V	PIN_B40	Si5340A reset signal
Si5340A (U68)	SI5340A1_I2C_SCL	1.2V	PIN_D44	I2C bus, connected with Si5397A
	SI5340A1_I2C_SDA	1.2V	PIN_B46	
	SI5340A1_OE_n	1.2V	PIN_D40	Si5340A output enable signal
	SI5340A1_RST_n	1.2V	PIN_B40	Si5340A reset signal

2.7 DDR4 SDRAM Interface

The development board supports two independent banks of DDR4 SDRAM interface (DDR4 SO-DIMM Socket and 8GB on-board DDR4 chips). The DDR4 SO-DIMM socket can support 16GB DDR4 SO-DIMM memory (Single Rank). The I/O bank where DDR4 SO-DIMM Socket is located can implement Intel Agilex FPGA EMIF IP with the Intel Agilex FPGA Hard Processor Subsystem (HPS). If HPS EMIF is not used in a system, the DDR4 SO-DIMM Socket A can be used for the EMIF of the FPGA fabric. In addtion, the 8GB on-board DDR4 chips are supported for FPGA logic.

The DDR4 SO-DIMM Socket and on-board DDR4 can run at the fastest clock frequency of 1600MHz clock for a maximum theoretical bandwidth up to 170 Gbps.

Figure 2-15 shows the connections between the DDR4 interface and Intel Agilex® 7 device.

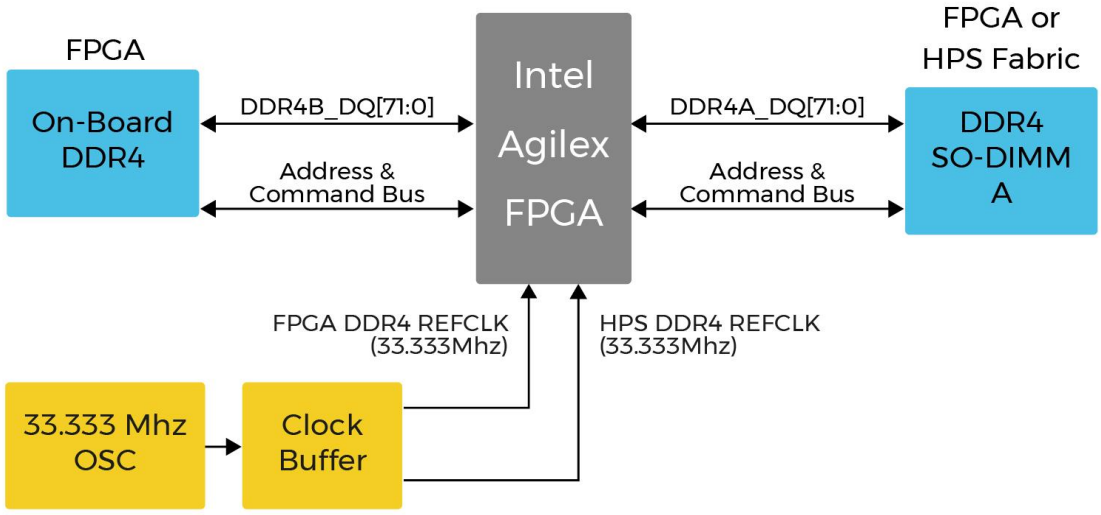


Figure 2-15 Connection between the DDR4 and Agilex FPGA

The pin assignments for DDR4 SDRAM SO-DIMM Bank-A and Bank-B are listed in **Table 2-14** and **Table 2-15**.

Table 2-14 DDR4-A Bank Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	Description	I/O Standard	Agilex Pin Number
DDR4A_DQ0	Data [0]	1.2V POD	PIN_L1
DDR4A_DQ1	Data [1]	1.2V POD	PIN_M2
DDR4A_DQ2	Data [2]	1.2V POD	PIN_M6
DDR4A_DQ3	Data [3]	1.2V POD	PIN_L5
DDR4A_DQ4	Data [4]	1.2V POD	PIN_P2
DDR4A_DQ5	Data [5]	1.2V POD	PIN_R1
DDR4A_DQ6	Data [6]	1.2V POD	PIN_P6
DDR4A_DQ7	Data [7]	1.2V POD	PIN_R5
DDR4A_DQ8	Data [8]	1.2V POD	PIN_J5
DDR4A_DQ9	Data [9]	1.2V POD	PIN_K2
DDR4A_DQ10	Data [10]	1.2V POD	PIN_F2
DDR4A_DQ11	Data [11]	1.2V POD	PIN_J1
DDR4A_DQ12	Data [12]	1.2V POD	PIN_K6

DDR4A_DQ13	Data [13]	1.2V POD	PIN_G5
DDR4A_DQ14	Data [14]	1.2V POD	PIN_F6
DDR4A_DQ15	Data [15]	1.2V POD	PIN_G1
DDR4A_DQ16	Data [16]	1.2V POD	PIN_B6
DDR4A_DQ17	Data [17]	1.2V POD	PIN_C5
DDR4A_DQ18	Data [18]	1.2V POD	PIN_D10
DDR4A_DQ19	Data [19]	1.2V POD	PIN_A9
DDR4A_DQ20	Data [20]	1.2V POD	PIN_E9
DDR4A_DQ21	Data [21]	1.2V POD	PIN_E5
DDR4A_DQ22	Data [22]	1.2V POD	PIN_B10
DDR4A_DQ23	Data [23]	1.2V POD	PIN_D6
DDR4A_DQ24	Data [24]	1.2V POD	PIN_F12
DDR4A_DQ25	Data [25]	1.2V POD	PIN_F8
DDR4A_DQ26	Data [26]	1.2V POD	PIN_G11
DDR4A_DQ27	Data [27]	1.2V POD	PIN_K8
DDR4A_DQ28	Data [28]	1.2V POD	PIN_J7
DDR4A_DQ29	Data [29]	1.2V POD	PIN_G7
DDR4A_DQ30	Data [30]	1.2V POD	PIN_J11
DDR4A_DQ31	Data [31]	1.2V POD	PIN_K12
DDR4A_DQ32	Data [32]	1.2V POD	PIN_M14
DDR4A_DQ33	Data [33]	1.2V POD	PIN_L17
DDR4A_DQ34	Data [34]	1.2V POD	PIN_P18
DDR4A_DQ35	Data [35]	1.2V POD	PIN_R17
DDR4A_DQ36	Data [36]	1.2V POD	PIN_L13
DDR4A_DQ37	Data [37]	1.2V POD	PIN_P14
DDR4A_DQ38	Data [38]	1.2V POD	PIN_M18
DDR4A_DQ39	Data [39]	1.2V POD	PIN_R13
DDR4A_DQ40	Data [40]	1.2V POD	PIN_U23
DDR4A_DQ41	Data [41]	1.2V POD	PIN_U19
DDR4A_DQ42	Data [42]	1.2V POD	PIN_Y24
DDR4A_DQ43	Data [43]	1.2V POD	PIN_Y20
DDR4A_DQ44	Data [44]	1.2V POD	PIN_T24
DDR4A_DQ45	Data [45]	1.2V POD	PIN_W19
DDR4A_DQ46	Data [46]	1.2V POD	PIN_W23

DDR4A_DQ47	Data [47]	1.2V POD	PIN_T20
DDR4A_DQ48	Data [48]	1.2V POD	PIN_L19
DDR4A_DQ49	Data [49]	1.2V POD	PIN_L23
DDR4A_DQ50	Data [50]	1.2V POD	PIN_R23
DDR4A_DQ51	Data [51]	1.2V POD	PIN_P24
DDR4A_DQ52	Data [52]	1.2V POD	PIN_M20
DDR4A_DQ53	Data [53]	1.2V POD	PIN_R19
DDR4A_DQ54	Data [54]	1.2V POD	PIN_P20
DDR4A_DQ55	Data [55]	1.2V POD	PIN_M24
DDR4A_DQ56	Data [56]	1.2V POD	PIN_U17
DDR4A_DQ57	Data [57]	1.2V POD	PIN_U13
DDR4A_DQ58	Data [58]	1.2V POD	PIN_Y14
DDR4A_DQ59	Data [59]	1.2V POD	PIN_Y18
DDR4A_DQ60	Data [60]	1.2V POD	PIN_T14
DDR4A_DQ61	Data [61]	1.2V POD	PIN_T18
DDR4A_DQ62	Data [62]	1.2V POD	PIN_W17
DDR4A_DQ63	Data [63]	1.2V POD	PIN_W13
DDR4A_DQ64	Data [64]	1.2V POD	PIN_AB8
DDR4A_DQ65	Data [65]	1.2V POD	PIN_AE1
DDR4A_DQ66	Data [66]	1.2V POD	PIN_AD2
DDR4A_DQ67	Data [67]	1.2V POD	PIN_AA7
DDR4A_DQ68	Data [68]	1.2V POD	PIN_AE7
DDR4A_DQ69	Data [69]	1.2V POD	PIN_AD6
DDR4A_DQ70	Data [70]	1.2V POD	PIN_AA1
DDR4A_DQ71	Data [71]	1.2V POD	PIN_AB2
DDR4A_DQS0	Data Strobe p[0]	DIFFERENTIAL 1.2V POD	PIN_L3
DDR4A_DQS_n0	Data Strobe n[0]	DIFFERENTIAL 1.2V POD	PIN_M4
DDR4A_DQS1	Data Strobe p[1]	DIFFERENTIAL 1.2V POD	PIN_G3
DDR4A_DQS_n1	Data Strobe n[1]	DIFFERENTIAL 1.2V POD	PIN_F4
DDR4A_DQS2	Data Strobe p[2]	DIFFERENTIAL 1.2V	PIN_A7

		POD	
DDR4A_DQS_n2	Data Strobe n[2]	DIFFERENTIAL 1.2V POD	PIN_B8
DDR4A_DQS3	Data Strobe p[3]	DIFFERENTIAL 1.2V POD	PIN_G9
DDR4A_DQS_n3	Data Strobe n[3]	DIFFERENTIAL 1.2V POD	PIN_F10
DDR4A_DQS4	Data Strobe p[4]	DIFFERENTIAL 1.2V POD	PIN_L15
DDR4A_DQS_n4	Data Strobe n[4]	DIFFERENTIAL 1.2V POD	PIN_M16
DDR4A_DQS5	Data Strobe p[5]	DIFFERENTIAL 1.2V POD	PIN_U21
DDR4A_DQS_n5	Data Strobe n[5]	DIFFERENTIAL 1.2V POD	PIN_T22
DDR4A_DQS6	Data Strobe p[6]	DIFFERENTIAL 1.2V POD	PIN_L21
DDR4A_DQS_n6	Data Strobe n[6]	DIFFERENTIAL 1.2V POD	PIN_M22
DDR4A_DQS7	Data Strobe p[7]	DIFFERENTIAL 1.2V POD	PIN_U15
DDR4A_DQS_n7	Data Strobe n[7]	DIFFERENTIAL 1.2V POD	PIN_T16
DDR4A_DQS8	Data Strobe p[8]	DIFFERENTIAL 1.2V POD	PIN_AA5
DDR4A_DQS_n8	Data Strobe n[8]	DIFFERENTIAL 1.2V POD	PIN_AB6
DDR4A_DBI_n0	Data Bus Inversion [0]	1.2V POD	PIN_R3
DDR4A_DBI_n1	Data Bus Inversion [1]	1.2V POD	PIN_J3
DDR4A_DBI_n2	Data Bus Inversion [2]	1.2V POD	PIN_E7
DDR4A_DBI_n3	Data Bus Inversion [3]	1.2V POD	PIN_J9

DDR4A_DBI_n4	Data Bus Inversion [4]	1.2V POD	PIN_R15
DDR4A_DBI_n5	Data Bus Inversion [5]	1.2V POD	PIN_W21
DDR4A_DBI_n6	Data Bus Inversion [6]	1.2V POD	PIN_R21
DDR4A_DBI_n7	Data Bus Inversion [7]	1.2V POD	PIN_W15
DDR4A_DBI_n8	Data Bus Inversion [8]	1.2V POD	PIN_AA3
DDR4A_A0	Address [0]	SSTL-12	PIN_U11
DDR4A_A1	Address [1]	SSTL-12	PIN_T12
DDR4A_A2	Address [2]	SSTL-12	PIN_W11
DDR4A_A3	Address [3]	SSTL-12	PIN_Y12
DDR4A_A4	Address [4]	SSTL-12	PIN_U9
DDR4A_A5	Address [5]	SSTL-12	PIN_T10
DDR4A_A6	Address [6]	SSTL-12	PIN_W9
DDR4A_A7	Address [7]	SSTL-12	PIN_Y10
DDR4A_A8	Address [8]	SSTL-12	PIN_U7
DDR4A_A9	Address [9]	SSTL-12	PIN_T8
DDR4A_A10	Address [10]	SSTL-12	PIN_W7
DDR4A_A11	Address [11]	SSTL-12	PIN_Y8
DDR4A_A12	Address [12]	SSTL-12	PIN_Y6
DDR4A_A13	Address [13]	SSTL-12	PIN_U3
DDR4A_A14	Address [14]/ WE_n	SSTL-12	PIN_T4
DDR4A_A15	Address [15]/ CAS_n	SSTL-12	PIN_W3
DDR4A_A16	Address [16]/ RAS_n	SSTL-12	PIN_Y4
DDR4A_BA0	Bank Select [0]	SSTL-12	PIN_T2
DDR4A_BA1	Bank Select [1]	SSTL-12	PIN_W1
DDR4A_BG0	Bank Group Select [0]	SSTL-12	PIN_Y2

DDR4A_BG1	Bank Group Select [1]	SSTL-12	PIN_L11
DDR4A_CK	Clock p	DIFFERENTIAL 1.2V SSTL	PIN_L7
DDR4A_CK_n	Clock n	DIFFERENTIAL 1.2V SSTL	PIN_M8
DDR4A_CKE	Clock Enable pin	SSTL-12	PIN_R9
DDR4A_ODT	On Die Termination	SSTL-12	PIN_L9
DDR4A_CS_n	Chip Select	SSTL-12	PIN_R11
DDR4A_PAR	Command and Address Parity Input	SSTL-12	PIN_P8
DDR4A_ALERT_n	Register ALERT_n output	1.2 V	PIN_U1
DDR4A_ACT_n	Activation Command Input	SSTL-12	PIN_P12
DDR4A_RESET_n	Chip Reset	1.2 V	PIN_M12
DDR4A_EVENT_n	Chip Temperature Event	1.2 V	PIN_G47
DDR4A_SDA	Chip I2C Serial Data Bus	1.2 V	PIN_E37
DDR4A_SCL	Chip I2C Serial Clock	1.2 V	PIN_E35
DDR4A_REFCLK_p	DDR4 A port Reference Clock p	True Differential Signaling	PIN_U5
DDR4A_REFCLK_n	DDR4 A port Reference Clock n	True Differential Signaling	PIN_T6
DDR4A_RZQ	Calibrated pins for OCT block	1.2 V	PIN_W5

Table 2-15 DDR4-B Bank Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	Description	I/O Standard	Agilex Pin Number

DDR4B_DQ0	Data [0]	1.2V POD	PIN_DE29
DDR4B_DQ1	Data [1]	1.2V POD	PIN_DH32
DDR4B_DQ2	Data [2]	1.2V POD	PIN_DJ29
DDR4B_DQ3	Data [3]	1.2V POD	PIN_DF32
DDR4B_DQ4	Data [4]	1.2V POD	PIN_DH28
DDR4B_DQ5	Data [5]	1.2V POD	PIN_DJ33
DDR4B_DQ6	Data [6]	1.2V POD	PIN_DF28
DDR4B_DQ7	Data [7]	1.2V POD	PIN_DE33
DDR4B_DQ8	Data [8]	1.2V POD	PIN_CV36
DDR4B_DQ9	Data [9]	1.2V POD	PIN_CT40
DDR4B_DQ10	Data [10]	1.2V POD	PIN_CT36
DDR4B_DQ11	Data [11]	1.2V POD	PIN_CV40
DDR4B_DQ12	Data [12]	1.2V POD	PIN_CR37
DDR4B_DQ13	Data [13]	1.2V POD	PIN_CW41
DDR4B_DQ14	Data [14]	1.2V POD	PIN_CW37
DDR4B_DQ15	Data [15]	1.2V POD	PIN_CR41
DDR4B_DQ16	Data [16]	1.2V POD	PIN_CV42
DDR4B_DQ17	Data [17]	1.2V POD	PIN_CV46
DDR4B_DQ18	Data [18]	1.2V POD	PIN_CW43
DDR4B_DQ19	Data [19]	1.2V POD	PIN_CW47
DDR4B_DQ20	Data [20]	1.2V POD	PIN_CT42
DDR4B_DQ21	Data [21]	1.2V POD	PIN_CR47
DDR4B_DQ22	Data [22]	1.2V POD	PIN_CT46
DDR4B_DQ23	Data [23]	1.2V POD	PIN_CR43
DDR4B_DQ24	Data [24]	1.2V POD	PIN_CN43
DDR4B_DQ25	Data [25]	1.2V POD	PIN_CN47
DDR4B_DQ26	Data [26]	1.2V POD	PIN_CP46
DDR4B_DQ27	Data [27]	1.2V POD	PIN_CL47
DDR4B_DQ28	Data [28]	1.2V POD	PIN_CP42
DDR4B_DQ29	Data [29]	1.2V POD	PIN_CK46
DDR4B_DQ30	Data [30]	1.2V POD	PIN_CL43
DDR4B_DQ31	Data [31]	1.2V POD	PIN_CK42
DDR4B_DQ32	Data [32]	1.2V POD	PIN_CN37
DDR4B_DQ33	Data [33]	1.2V POD	PIN_CP40

DDR4B_DQ34	Data [34]	1.2V POD	PIN_CL37
DDR4B_DQ35	Data [35]	1.2V POD	PIN_CL41
DDR4B_DQ36	Data [36]	1.2V POD	PIN_CP36
DDR4B_DQ37	Data [37]	1.2V POD	PIN_CK40
DDR4B_DQ38	Data [38]	1.2V POD	PIN_CK36
DDR4B_DQ39	Data [39]	1.2V POD	PIN_CN41
DDR4B_DQ40	Data [40]	1.2V POD	PIN_DC45
DDR4B_DQ41	Data [41]	1.2V POD	PIN_DD48
DDR4B_DQ42	Data [42]	1.2V POD	PIN_DA45
DDR4B_DQ43	Data [43]	1.2V POD	PIN_DC49
DDR4B_DQ44	Data [44]	1.2V POD	PIN_CY44
DDR4B_DQ45	Data [45]	1.2V POD	PIN_DA49
DDR4B_DQ46	Data [46]	1.2V POD	PIN_DD44
DDR4B_DQ47	Data [47]	1.2V POD	PIN_CY48
DDR4B_DQ48	Data [48]	1.2V POD	PIN_DC51
DDR4B_DQ49	Data [49]	1.2V POD	PIN_DD54
DDR4B_DQ50	Data [50]	1.2V POD	PIN_DA51
DDR4B_DQ51	Data [51]	1.2V POD	PIN_DA55
DDR4B_DQ52	Data [52]	1.2V POD	PIN_DD50
DDR4B_DQ53	Data [53]	1.2V POD	PIN_CY54
DDR4B_DQ54	Data [54]	1.2V POD	PIN_CY50
DDR4B_DQ55	Data [55]	1.2V POD	PIN_DC55
DDR4B_DQ56	Data [56]	1.2V POD	PIN_DE47
DDR4B_DQ57	Data [57]	1.2V POD	PIN_DH50
DDR4B_DQ58	Data [58]	1.2V POD	PIN_DH46
DDR4B_DQ59	Data [59]	1.2V POD	PIN_DG51
DDR4B_DQ60	Data [60]	1.2V POD	PIN_DF46
DDR4B_DQ61	Data [61]	1.2V POD	PIN_DF52
DDR4B_DQ62	Data [62]	1.2V POD	PIN_DJ47
DDR4B_DQ63	Data [63]	1.2V POD	PIN_DE53
DDR4B_DQ64	Data [64]	1.2V POD	PIN_DJ41
DDR4B_DQ65	Data [65]	1.2V POD	PIN_DJ45
DDR4B_DQ66	Data [66]	1.2V POD	PIN_DE41
DDR4B_DQ67	Data [67]	1.2V POD	PIN_DF44

DDR4B_DQ68	Data [68]	1.2V POD	PIN_DF40
DDR4B_DQ69	Data [69]	1.2V POD	PIN_DE45
DDR4B_DQ70	Data [70]	1.2V POD	PIN_DH40
DDR4B_DQ71	Data [71]	1.2V POD	PIN_DH44
DDR4B_DQS0	Data Strobe p[0]	DIFFERENTIAL 1.2V POD	PIN_DH30
DDR4B_DQS_n0	Data Strobe n[0]	DIFFERENTIAL 1.2V POD	PIN_DJ31
DDR4B_DQS1	Data Strobe p[1]	DIFFERENTIAL 1.2V POD	PIN_CV38
DDR4B_DQS_n1	Data Strobe n[1]	DIFFERENTIAL 1.2V POD	PIN_CW39
DDR4B_DQS2	Data Strobe p[2]	DIFFERENTIAL 1.2V POD	PIN_CV44
DDR4B_DQS_n2	Data Strobe n[2]	DIFFERENTIAL 1.2V POD	PIN_CW45
DDR4B_DQS3	Data Strobe p[3]	DIFFERENTIAL 1.2V POD	PIN_CP44
DDR4B_DQS_n3	Data Strobe n[3]	DIFFERENTIAL 1.2V POD	PIN_CN45
DDR4B_DQS4	Data Strobe p[4]	DIFFERENTIAL 1.2V POD	PIN_CP38
DDR4B_DQS_n4	Data Strobe n[4]	DIFFERENTIAL 1.2V POD	PIN_CN39
DDR4B_DQS5	Data Strobe p[5]	DIFFERENTIAL 1.2V POD	PIN_DD46
DDR4B_DQS_n5	Data Strobe n[5]	DIFFERENTIAL 1.2V POD	PIN_DC47
DDR4B_DQS6	Data Strobe p[6]	DIFFERENTIAL 1.2V POD	PIN_DD52
DDR4B_DQS_n6	Data Strobe n[6]	DIFFERENTIAL 1.2V POD	PIN_DC53
DDR4B_DQS7	Data Strobe p[7]	DIFFERENTIAL 1.2V POD	PIN_DH48
DDR4B_DQS_n7	Data Strobe n[7]	DIFFERENTIAL 1.2V	PIN_DJ49

		POD	
DDR4B_DQS8	Data Strobe p[8]	DIFFERENTIAL 1.2V POD	PIN_DH42
DDR4B_DQS_n8	Data Strobe n[8]	DIFFERENTIAL 1.2V POD	PIN_DJ43
DDR4B_DBI_n0	Data Bus Inversion [0]	1.2V POD	PIN_DF30
DDR4B_DBI_n1	Data Bus Inversion [1]	1.2V POD	PIN_CT38
DDR4B_DBI_n2	Data Bus Inversion [2]	1.2V POD	PIN_CT44
DDR4B_DBI_n3	Data Bus Inversion [3]	1.2V POD	PIN_CK44
DDR4B_DBI_n4	Data Bus Inversion [4]	1.2V POD	PIN_CK38
DDR4B_DBI_n5	Data Bus Inversion [5]	1.2V POD	PIN_CY46
DDR4B_DBI_n6	Data Bus Inversion [6]	1.2V POD	PIN_CY52
DDR4B_DBI_n7	Data Bus Inversion [7]	1.2V POD	PIN_DF48
DDR4B_DBI_n8	Data Bus Inversion [8]	1.2V POD	PIN_DF42
DDR4B_A0	Address [0]	SSTL-12	PIN_DH38
DDR4B_A1	Address [1]	SSTL-12	PIN_DJ39
DDR4B_A2	Address [2]	SSTL-12	PIN_DF38
DDR4B_A3	Address [3]	SSTL-12	PIN_DE39
DDR4B_A4	Address [4]	SSTL-12	PIN_DH36
DDR4B_A5	Address [5]	SSTL-12	PIN_DJ37
DDR4B_A6	Address [6]	SSTL-12	PIN_DF36
DDR4B_A7	Address [7]	SSTL-12	PIN_DE37
DDR4B_A8	Address [8]	SSTL-12	PIN_DH34
DDR4B_A9	Address [9]	SSTL-12	PIN_DJ35
DDR4B_A10	Address [10]	SSTL-12	PIN_DF34

DDR4B_A11	Address [11]	SSTL-12	PIN_DE35
DDR4B_A12	Address [12]	SSTL-12	PIN_DA37
DDR4B_A13	Address [13]	SSTL-12	PIN_DD34
DDR4B_A14	Address [14]/ WE_n	SSTL-12	PIN_DC35
DDR4B_A15	Address [15]/ CAS_n	SSTL-12	PIN_CY34
DDR4B_A16	Address [16]/ RAS_n	SSTL-12	PIN_DA35
DDR4B_BA0	Bank Select [0]	SSTL-12	PIN_DC33
DDR4B_BA1	Bank Select [1]	SSTL-12	PIN_CY32
DDR4B_BG0	Bank Group Select [0]	SSTL-12	PIN_DA33
DDR4B_BG1	Bank Group Select [1]	SSTL-12	PIN_DD42
DDR4B_CK	Clock p	DIFFERENTIAL 1.2V SSTL	PIN_DD38
DDR4B_CK_n	Clock n	DIFFERENTIAL 1.2V SSTL	PIN_DC39
DDR4B_CKE	Clock Enable pin	SSTL-12	PIN_CY40
DDR4B_ODT	On Die Termination	SSTL-12	PIN_DD40
DDR4B_CS_n	Chip Select	SSTL-12	PIN_CY42
DDR4B_PAR	Command and Address Parity Input	SSTL-12	PIN_DA39
DDR4B_ALERT_n	Register ALERT_n output	1.2 V	PIN_DD32
DDR4B_ACT_n	Activation Command Input	SSTL-12	PIN_DA43
DDR4B_RESET_n	Chip Reset	1.2 V	PIN_DC43
DDR4B_REFCLK_p	DDR4 B port Reference Clock p	True Differential Signaling	PIN_DD36
DDR4B_REFCLK_n	DDR4 B port Reference Clock n	True Differential Signaling	PIN_DD37

DDR4B_RZQ	Calibrated pins for OCT block	1.2 V	PIN_CY36

2.8 QSFP28 Port

The development board has one QSFP28 connector that use four pair transceiver channels from the Agilex FPGA device. The QSFP28 module receives the serial data from the Agilex FPGA, and transform them to optical signals. A Low-Jitter programmable clock generator (Si5340A) will provide flexible clock for serial transceivers of the FPGA (See section 2.6). **Figure 2-16** shows the connections between the QSFP28 and Agilex FPGA.

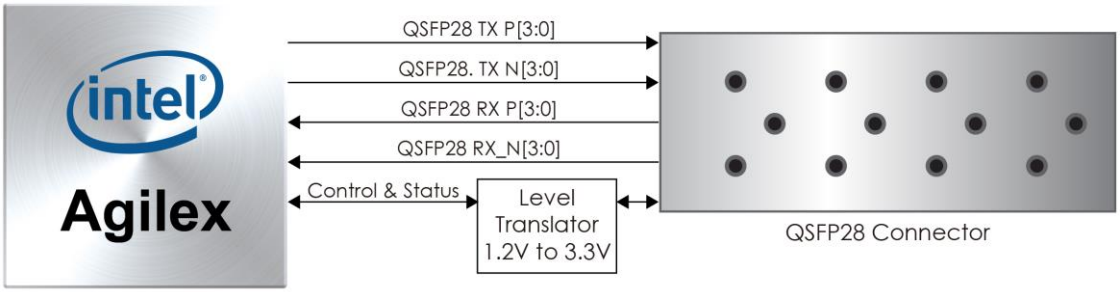


Figure 2-16 Connection between the QSFP28 and FPGA

Table 2-16 lists the QSFP28 pin assignments and signal names relative to the Intel Agilex® 7 device.

Table 2-16 QSFP28 Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	Description	I/O Standard	Agilex Pin Number
QSFP28_TX_P0	Transmitter data of channel 0	HSSI DIFFERENTIAL I/O	PIN_AV52
QSFP28_TX_N0	Transmitter data of channel 0	HSSI DIFFERENTIAL I/O	PIN_AU51
QSFP28_RX_P0	Receiver data of channel 0	HSSI DIFFERENTIAL I/O	PIN_AR55

QSFP28_RX_N0	Receiver data of channel 0	HSSI DIFFERENTIAL I/O	PIN_AT54
QSFP28_TX_P1	Transmitter data of channel 1	HSSI DIFFERENTIAL I/O	PIN_AP52
QSFP28_TX_N1	Transmitter data of channel 1	HSSI DIFFERENTIAL I/O	PIN_AN51
QSFP28_RX_P1	Receiver data of channel 1	HSSI DIFFERENTIAL I/O	PIN_AL55
QSFP28_RX_N1	Receiver data of channel 1	HSSI DIFFERENTIAL I/O	PIN_AM54
QSFP28_TX_P2	Transmitter data of channel 2	HSSI DIFFERENTIAL I/O	PIN_AK52
QSFP28_TX_N2	Transmitter data of channel 2	HSSI DIFFERENTIAL I/O	PIN_AJ51
QSFP28_RX_P2	Receiver data of channel 2	HSSI DIFFERENTIAL I/O	PIN_AG55
QSFP28_RX_N2	Receiver data of channel 2	HSSI DIFFERENTIAL I/O	PIN_AH54
QSFP28_TX_P3	Transmitter data of channel 3	HSSI DIFFERENTIAL I/O	PIN_AF52
QSFP28_TX_N3	Transmitter data of channel 3	HSSI DIFFERENTIAL I/O	PIN_AE51
QSFP28_RX_P3	Receiver data of channel 3	HSSI DIFFERENTIAL	PIN_AC55

		I/O	
QSFP28_RX_N3	Receiver data of channel 3	HSSI DIFFERENTIAL I/O	PIN_AD54
QSFP28_REFCLK_p0	QSFP28 transceiver reference clock p	LVDS	PIN_AN49
QSFP28_REFCLK_n0	QSFP28 transceiver reference clock n	LVDS	PIN_AP48
QSFP28_REFCLK_p1	QSFP28 transceiver reference clock p	LVDS	PIN_AJ49
QSFP28_REFCLK_n1	QSFP28 transceiver reference clock n	LVDS	PIN_AH48
QSFP28_MOD_SEL_n	Module Select	3.0-V LVTTL	PIN_B36
QSFP28_RST_n	Module Reset	3.0-V LVTTL	PIN_B38
QSFP28_SCL	2-wire serial interface clock	3.0-V LVTTL	PIN_B42
QSFP28_SDA	2-wire serial interface data	3.0-V LVTTL	PIN_E39
QSFP28_LP_MODE	Low Power Mode	3.0-V LVTTL	PIN_E47
QSFP28_INTERRUPT_n	Interrupt	3.0-V LVTTL	PIN_A45
QSFP28_MOD_PRS_n	Module Present	3.0-V LVTTL	PIN_A39

2.9 PCI Express

The FPGA development board is designed to fit entirely into a PC motherboard with x8 PCI Express slot. Utilizing built-in transceivers on an Agilex device, it is able to provide a fully integrated PCI Express-compliant solution for multi-lane (x1, x4, and x8) applications. With the PCI Express hard IP block incorporated in the Agilex device, it will allow users to implement simple and fast protocol, as well as saving logic resources for logic application. **Figure 2-17** presents the pin connection established between the Agilex FPGA and PCI Express.

The PCI Express interface supports complete PCI Express Gen1 at 2.5Gbps/lane, Gen2 at 5.0Gbps/lane, Gen3 at 8.0Gbps/lane and Gen4 at 16.0Gbps/lane protocol stack solution compliant to PCI Express base specification 4.0 that includes PHY-MAC, Data Link, and transaction layer circuitry embedded in PCI Express hard IP blocks.

Please note that it is a requirement that you connect the PCIe external power connector 8-pin 12V DC power connector in the FPGA to avoid FPGA damage due to insufficient power. The PCIE_REFCLK_p signal is a differential input that is driven from the PC motherboard on this board through the PCIe edge connector. A DIP switch (SW4) is connected to the PCI Express to allow different configurations to enable x1, x4 or x8 PCIe lane.

Table 2-17 summarizes the PCI Express pin assignments of the signal names relative to the Agilex FPGA.

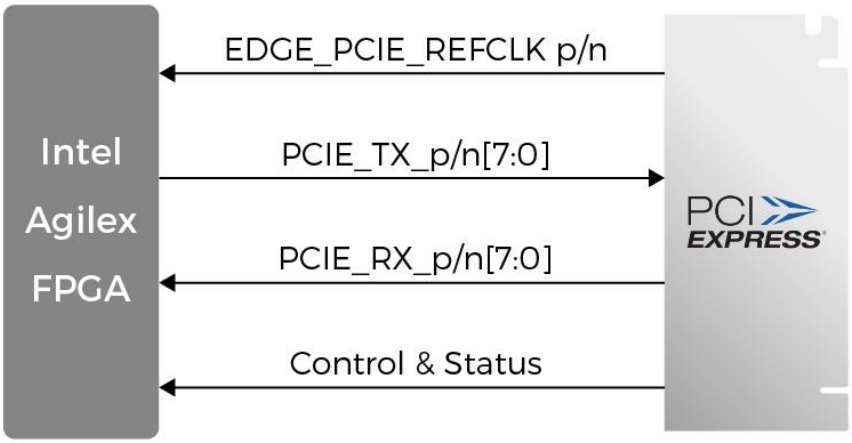


Figure 2-17 PCI Express pin connection

Table 2-17 PCI Express Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	Description	I/O Standard	Agilex Pin Number
PCIE_TX_p0	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_BW49
PCIE_TX_n0	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_BY48
PCIE_TX_p1	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_BV52
PCIE_TX_n1	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_BU51
PCIE_TX_p2	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_BR49
PCIE_TX_n2	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_BT48
PCIE_TX_p3	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_BP52
PCIE_TX_n3	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_BN51
PCIE_TX_p4	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_BL49
PCIE_TX_n4	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_BM48
PCIE_TX_p5	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_BK52
PCIE_TX_n5	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_BJ51
PCIE_TX_p6	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_BF52
PCIE_TX_n6	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_BE51
PCIE_TX_p7	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_BB52

PCIE_TX_n7	Add-in card transmit bus	HIGH Speed Differential I/O	PIN_BA51
PCIE_RX_p0	Add-in card receive bus	HIGH Speed Differential I/O	PIN_CC55
PCIE_RX_n0	Add-in card receive bus	HIGH Speed Differential I/O	PIN_CD54
PCIE_RX_p1	Add-in card receive bus	HIGH Speed Differential I/O	PIN_CB52
PCIE_RX_n1	Add-in card receive bus	HIGH Speed Differential I/O	PIN_CA51
PCIE_RX_p2	Add-in card receive bus	HIGH Speed Differential I/O	PIN_BW55
PCIE_RX_n2	Add-in card receive bus	HIGH Speed Differential I/O	PIN_BY54
PCIE_RX_p3	Add-in card receive bus	HIGH Speed Differential I/O	PIN_BR55
PCIE_RX_n3	Add-in card receive bus	HIGH Speed Differential I/O	PIN_BT54
PCIE_RX_p4	Add-in card receive bus	HIGH Speed Differential I/O	PIN_BL55
PCIE_RX_n4	Add-in card receive bus	HIGH Speed Differential I/O	PIN_BM54
PCIE_RX_p5	Add-in card receive bus	HIGH Speed Differential I/O	PIN_BG55
PCIE_RX_n5	Add-in card receive bus	HIGH Speed Differential I/O	PIN_BH54
PCIE_RX_p6	Add-in card receive bus	HIGH Speed Differential I/O	PIN_BC55
PCIE_RX_n6	Add-in card receive bus	HIGH Speed Differential I/O	PIN_BD54
PCIE_RX_p7	Add-in card receive bus	HIGH Speed Differential I/O	PIN_AW55
PCIE_RX_n7	Add-in card receive bus	HIGH Speed Differential I/O	PIN_AY54
PCIE_CLKREQ_n	Clock request signal	1.2V	PIN_A37

PCIE_REFCLK_p	Motherboard reference clock	HCSL	PIN_BC49
PCIE_REFCLK_n	Motherboard reference clock	HCSL	PIN_BC49
PCIE_PERST_n	Reset	1.8V	PIN_BR43
PCIE_SMBCLK	SMB clock	1.2V	PIN_A35
PCIE_SMBDAT	SMB data	1.2V	PIN_D38
PCIE_WAKE_n	Wake signal	1.2V	PIN_D36
PCIE_PRSNT1n	Hot plug detect	-	-
PCIE_PRSNT2n_x1	Hot plug detect x1 PCIe slot enabled using SW6 dip switch	-	-
PCIE_PRSNT2n_x4	Hot plug detect x4 PCIe slot enabled using SW6 dip switch	-	-
PCIE_PRSNT2n_x8	Hot plug detect x8 PCIe slot enabled using SW6 dip switch	-	-

2.10 FMC+ Connector

In addition to an FMC connector on the Agilex 7 FPGA Starter Kit, there is an FMC + connector for expanding FPGA I/Os (See **Figure 2-18**). The main difference between FMC + and FMC specifications is that the number of FMC + transceiver can provide up to 24 pairs (**High Serial Pin Count version, HSPC**), but in the Agilex 7 FPGA Starter Kit it provides **16** pair F-title transceivers.

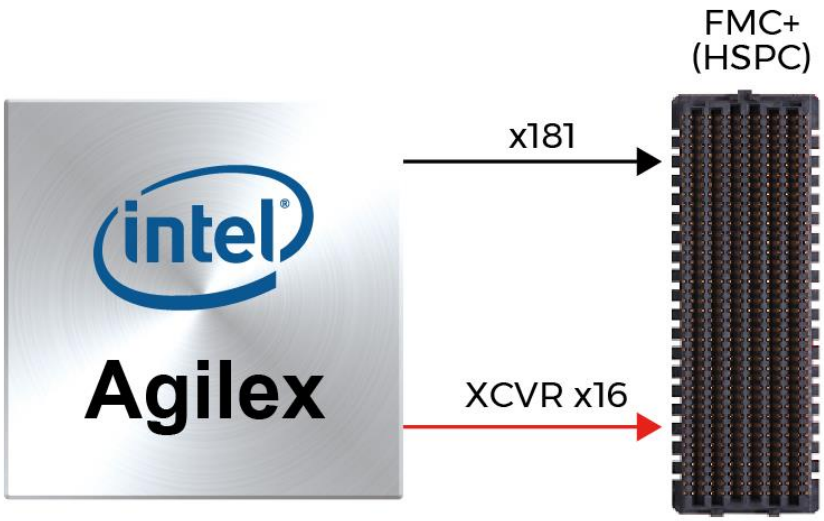


Figure 2-18 FMC+ connector on Agilex 7 FPGA Starter Kit

As the number of transceivers increases, the connector size of the FMC+ becomes a 14x40 array, compared to the 10x40 array of the FMC.

Below we will introduce according to the individual functions of FMC+ connector.

■ Clock Interface

Table 2-18 shows the FPGA dedicated clock input pin placement on the FMC+ connector.

Table 2-18 FMCP clock input interface distribution

Signal Name	FMC Clock in/out pin name	FPGA Clock Input Pin Placement	FPGA Pin Assignment
FMCP_CLK_M2C_p0	CLK0_M2C_P	CLK_B_2D_0P	CK18
FMCP_CLK_M2C_n0	CLK0_M2C_N	CLK_B_2D_0N	CL19
FMCP_CLK_M2C_p1	CLK1_M2C_P	CLK_B_2C_1P	CV28
FMCP_CLK_M2C_n1	CLK1_M2C_N	CLK_B_2C_1N	CW29
FMCP_HA_p1	HA01_P_CC	CLK_T_2C_1P	DF22
FMCP_HA_n1	HA01_N_CC	CLK_T_2C_1N	DE23
FMCP_HA_p17	HA_P17	CLK_T_2C_0P	DD24
FMCP_HA_n17	HA_P17	CLK_T_2C_0N	DC25
FMCP_HB_p1	HB_P11	CLK_B_2C_0P	CT30
FMCP_HB_n1	HB_P11	CLK_B_2C_0N	CR31
FMCP_LA_p0	LA00_P_CC	CLK_T_2D_1P	DF10
FMCP_LA_p0	LA00_N_CC	CLK_T_2D_1N	DE11
FMCP_LA_p17	LA_P17	CLK_B_2D_1P	CV16
FMCP_LA_n17	LA_N17	CLK_B_2D_1N	CW17

■ Power Supply

The Agilex 7 FPGA Starter Kit provides 12V, 3.3V and 1.2V(VADJ) power through FMC+ port. **Table 2-19** indicates the maximum power consumption for the FMC+ connector.

CAUTION: Before powering on the Agilex 7 FPGA Starter Kit with a daughter card, please check to see if there is a short circuit between the power pins and FPGA I/O.

Table 2-19 Power Supply of the FMC

Supplied Voltage	Max. Current Limit
12V	1A
3.3V	3A
1.2V(VADJ)	4A

■ JTAG Chain on FMC

The JTAG chain on the Agilex 7 FPGA Starter Kit supports JTAG interface extension to the FMC+ connector so that the JTAG device on the user's FMC+ daughter card can be joined with JTAG chain on the Agilex 7 FPGA Starter Kit. Users can enable this feature through the switch (**SW3.1**) on the Agilex 7 FPGA Starter Kit. In the board's default setting, the JTAG interface of the FMC connector is bypassed to keep the Agilex 7 FPGA Starter Kit JTAG chain to maintain close loop. For detailed setting, please refer to Section 2.3: **JTAG Interface Switch.**

■ Adjustable I/O Standards

Some of the FPGA pin's I/O standard connected with the HPC (High Pin Count) part of the FMC connector can be set to voltages: 1.2V and 1.5V. This function can be achieved because the VCCIO power pin of the FPGA bank where these FPGA I/Os are located can adjust the input voltage through the 3 pin header (**JP3**). For detailed setting, please refer to Section 2.3: **FMC_VCCIO Select Header**.

■ Transceiver Channels Speed

There are 16 **F-Tile** transceivers connected to the Agilex FPGA on the FMC connector and the maximum test transmission speed is **16 G bps**.

■ Refernce clock for FMC+ transceivers

There are four clocks are feed to the FPGA for the FMC+ transceivers as the reference

clock. These clocks are provides by two programmable clock generator(SI5340A). User can modify the clock frequencies via I2C interface for differential applications.

Table 2-20 FMC+ Reference clock

Source	Schematic Signal Name	Default Frequency	I/O Standard	Agilex Pin Number
U68	FMCP_REFCLK_p0	156.25 MHz	LVDS	PIN_ BP8
U68	FMCP_REFCLK_p1	184.32 MHz	LVDS	PIN_A24
U77	FMCP_REFCLK_p2	100MHz	LVDS	PIN_BW7
U68	FMCP_REFCLK_p3	148.5Mhz	LVDS	PIN_BH8

■ FPGA Pin Assignments for FMC+ Connector

Figure 2-19 shows the pin out table of the FMC+ connector on the Agilex FPGA and **Table 2-21** lists the FMC+ connector pin assignments, signal names and function.

	M	L	K	J	H	G	F	E	D	C	B	A	Z	Y
1	GND	RES1	FMC_VREFB	GND	FMC_VREFA	GND	M2C_PG	GND	C2M_PG	GND	GND	GND	FMCP_PRSNT_M2C_L	GND
2	NC	GND	GND	CLK3_BIDIR_P	FMCP_PRSNT_M2C_L	CLK_M2C_P1	GND	HA_P1	GND	DP_C2M_P0	GND	DP_M2C_P1	GND	NC
3	NC	GND	GND	CLK3_BIDIR_N	GND	CLK_M2C_N1	GND	HA_N1	GND	DP_C2M_N0	GND	DP_M2C_N1	GND	NC
4	GND	GBTCLK_M2C_P4	CLK2_BIDIR_P	GND	CLK_M2C_P0	GND	HA_P0	GND	GBTCLK_M2C_P0	GND	DP_M2C_P9	GND	NC	GND
5	GND	GBTCLK_M2C_N4	CLK2_BIDIR_N	GND	CLK_M2C_N0	GND	HA_N0	GND	GBTCLK_M2C_N0	GND	DP_M2C_N9	GND	NC	GND
6	NC	GND	GND	HA_P3	GND	LA_P0	GND	HA_P5	GND	DP_M2C_P0	GND	DP_M2C_P2	GND	NC
7	NC	GND	HA_P2	HA_N3	LA_P2	LA_N0	HA_P4	HA_N5	GND	DP_M2C_N0	GND	DP_M2C_N2	GND	NC
8	GND	GBTCLK_M2C_P3	HA_N2	GND	LA_N2	GND	HA_N4	GND	LA_P1	GND	DP_M2C_P8	GND	NC	GND
9	GND	GBTCLK_M2C_N3	GND	HA_P7	GND	LA_P3	GND	HA_P9	LA_N1	GND	DP_M2C_N8	GND	NC	GND
10	NC	GND	HA_P6	HA_N7	LA_P4	LA_N3	HA_P8	HA_N9	GND	LA_P6	GND	DP_M2C_P3	GND	DP_M2C_P10
11	NC	GND	HA_N6	GND	LA_N4	GND	HA_N8	GND	LA_P5	LA_N6	GND	DP_M2C_N3	GND	DP_M2C_N10
12	GND	GBTCLK_M2C_P2	GND	HA_P11	GND	LA_P8	GND	HA_P13	LA_N5	GND	DP_M2C_P7	GND	DP_M2C_P11	GND
13	GND	GBTCLK_M2C_N2	HA_P10	HA_N11	LA_P7	LA_N8	HA_P12	HA_N13	GND	GND	DP_M2C_N7	GND	DP_M2C_N11	GND
14	NC	GND	HA_N10	GND	LA_N7	GND	HA_N12	GND	LA_P9	LA_P10	GND	DP_M2C_P4	GND	DP12_M2C_P
15	NC	GND	GND	HA_P14	GND	LA_P12	GND	HA_P16	LA_N9	LA_N10	GND	DP_M2C_N4	GND	DP12_M2C_N
16	GND	SYNC_C2M_P	HA_P17	HA_N14	LA_P11	LA_N12	HA_P15	HA_N16	GND	GND	DP_M2C_P6	GND	DP13_M2C_P	GND
17	GND	SYNC_C2M_N	HA_N17	GND	LA_N11	GND	HA_N15	GND	LA_P13	GND	DP_M2C_N6	GND	DP13_M2C_N	GND
18	DP_C2M_P14	GND	GND	HA_P18	GND	LA_P16	GND	HA_P20	LA_N13	LA_P14	GND	DP_M2C_P5	GND	DP14_M2C_P
19	DP_C2M_N14	GND	HA_P21	HA_N18	LA_P15	LA_N16	HA_P19	HA_N20	GND	LA_N14	GND	DP_M2C_N5	GND	DP14_M2C_N
20	GND	REFCLK_C2M_P	HA_N21	GND	LA_N15	GND	HA_N19	GND	LA_P17	GND	GBTCLK_M2C_P1	GND	NC	GND
21	GND	REFCLK_C2M_N	GND	HA_P22	GND	LA_P20	GND	HB_P3	LA_N17	GND	GBTCLK_M2C_N1	GND	NC	GND
22	DP_C2M_P15	GND	HA_P23	HA_N22	LA_P19	LA_N20	HB_P2	HB_N3	GND	LA_P18	GND	DP_C2M_P1	GND	DP15_M2C_P
23	DP_C2M_N15	GND	HA_N23	GND	LA_N19	GND	HB_N2	GND	LA_P23	LA_N18	GND	DP_C2M_N1	GND	DP15_M2C_N
24	GND	REFCLK_M2C_P	GND	HB_P1	GND	LA_P22	GND	HB_P5	LA_N23	GND	DP_C2M_P9	GND	DP_C2M_P10	GND
25	GND	REFCLK_M2C_N	HB_P0	HB_N1	LA_P21	LA_N22	HB_P4	HB_N5	GND	GND	DP_C2M_N9	GND	DP_C2M_N10	GND
26	NC	GND	HB_N0	GND	LA_N21	GND	HB_N4	GND	LA_P26	LA_P27	GND	DP_C2M_P2	GND	DP_C2M_P11
27	NC	GND	GND	HB_P7	GND	LA_P25	GND	HB_P9	LA_N26	LA_N27	GND	DP_C2M_N2	GND	DP_C2M_N11
28	GND	SYNC_M2C_P	HB_P6	HB_N7	LA_P24	LA_N25	HB_P8	HB_N9	GND	GND	DP_C2M_P8	GND	DP_C2M_P12	GND
29	GND	SYNC_M2C_N	HB_N6	GND	LA_N24	GND	HB_N8	GND	JTAG_TCK	GND	DP_C2M_N8	GND	DP_C2M_N12	GND
30	NC	GND	GND	HB_P11	GND	LA_P29	GND	HB_P13	JTAG_TDI	SCL	GND	DP_C2M_P3	GND	DP_C2M_P13
31	NC	GND	HB_P10	HB_N11	LA_P28	LA_N29	HB_P12	HB_N13	JTAG_TDO	SDA	GND	DP_C2M_N3	GND	DP_C2M_N13
32	GND	GND	HB_N10	GND	LA_N28	GND	HB_N12	GND	VCC3P3	GND	DP_C2M_P7	GND	NC	GND
33	GND	GND	GND	HB_P15	GND	LA_P31	GND	HB_P19	JTAG_TMS	GND	DP_C2M_N7	GND	NC	GND
34	NC	GND	HB_P14	HB_N15	LA_P30	LA_N31	HB_P16	HB_N19	JTAG_TRST	GA0	GND	DP_C2M_P4	GND	NC
35	NC	GND	HB_N14	GND	LA_N30	GND	HB_N16	GND	GA1	VCC12	GND	DP_C2M_N4	GND	NC
36	GND	12P0V	GND	HB_P18	GND	LA_P33	GND	HB_P21	VCC3P3	GND	DP_C2M_P6	GND	NC	GND
37	GND	12P0V	HB_P17	HB_N18	LA_P32	LA_N33	HB_P20	HB_N21	GND	VCC12	DP_C2M_N6	GND	NC	GND
38	NC	GND	HB_N17	GND	LA_N32	GND	HB_N20	GND	VCC3P3	GND	GND	DP_C2M_P5	GND	NC
39	NC	GND	GND	NC	GND	VCCIO_FMC	GND	VCCIO_FMC	GND	VCC3P3	GND	DP_C2M_N5	GND	NC
40	GND	12P0V	NC	GND	VCCIO_FMC	GND	VCCIO_FMC	GND	VCC3P3	GND	RES0	GND	3P3V	GND

Figure 2-19 FMC+ pin out table

Table 2-21 FMCP Connector Pin Assignments, Signal Names and Functions

Signal Name	FPGA Pin	Description	I/O Standard

	Number		
FMCP_CLK2_BIDIR_p	PIN_CV14	FMCP data bus	1.2 V
FMCP_CLK2_BIDIR_n	PIN_CW15	FMCP data bus	1.2 V
FMCP_CLK3_BIDIR_p	PIN_CP14	FMCP data bus	1.2 V
FMCP_CLK3_BIDIR_n	PIN_CN15	FMCP data bus	1.2 V
FMCP_CLK_M2C_p[0]	PIN_CK18	Clock from mezzanine module to carrier card positive 0	True Differential Signaling
FMCP_CLK_M2C_n[0]	PIN_CL19	Clock from mezzanine module to carrier card negative 0	True Differential Signaling
FMCP_CLK_M2C_p[1]	PIN_CV28	Clock from mezzanine module to carrier card positive 1	True Differential Signaling*(1)
FMCP_CLK_M2C_n[1]	PIN_CW29	Clock from mezzanine module to carrier card negative 1	True Differential*(1) Signaling
FMCP_HA_p[0]	PIN_DD22	FMCP HA bank data p0	1.2V or 1.5V*(1)
FMCP_HA_p[1]	PIN_DF22	FMCP HA bank data p1	1.2V or 1.5V*(1)
FMCP_HA_p[2]	PIN_DD20	FMCP HA bank data p2	1.2V or 1.5V*(1)
FMCP_HA_p[3]	PIN_CY22	FMCP HA bank data p3	1.2V or 1.5V*(1)
FMCP_HA_p[4]	PIN_DH16	FMCP HA bank data p4	1.2V or 1.5V*(1)
FMCP_HA_p[5]	PIN_CY20	FMCP HA bank data p5	1.2V or 1.5V*(1)
FMCP_HA_p[6]	PIN_DH20	FMCP HA bank data p6	1.2V or 1.5V*(1)
FMCP_HA_p[7]	PIN_DF16	FMCP HA bank data p7	1.2V or 1.5V*(1)
FMCP_HA_p[8]	PIN_DH18	FMCP HA bank data p8	1.2V or 1.5V*(1)
FMCP_HA_p[9]	PIN_DF18	FMCP HA bank data p9	1.2V or 1.5V*(1)
FMCP_HA_p[10]	PIN_DH22	FMCP HA bank data p10	1.2V or 1.5V*(1)
FMCP_HA_p[11]	PIN_CY26	FMCP HA bank data p11	1.2V or 1.5V*(1)

FMCP_HA_p[12]	PIN_DH24	FMCP HA bank data p12	1.2V or 1.5V*(1)
FMCP_HA_p[13]	PIN_DF20	FMCP HA bank data p13	1.2V or 1.5V*(1)
FMCP_HA_p[14]	PIN_DF26	FMCP HA bank data p14	1.2V or 1.5V*(1)
FMCP_HA_p[15]	PIN_DH26	FMCP HA bank data p15	1.2V or 1.5V*(1)
FMCP_HA_p[16]	PIN_DF24	FMCP HA bank data p16	1.2V or 1.5V*(1)
FMCP_HA_p[17]	PIN_DD24	FMCP HA bank data p17	1.2V or 1.5V*(1)
FMCP_HA_p[18]	PIN_CY30	FMCP HA bank data p18	1.2V or 1.5V*(1)
FMCP_HA_p[19]	PIN_DD26	FMCP HA bank data p19	1.2V or 1.5V*(1)
FMCP_HA_p[20]	PIN_CY28	FMCP HA bank data p20	1.2V or 1.5V*(1)
FMCP_HA_p[21]	PIN_DD28	FMCP HA bank data p21	1.2V or 1.5V*(1)
FMCP_HA_p[22]	PIN_CY24	FMCP HA bank data p22	1.2V or 1.5V*(1)
FMCP_HA_p[23]	PIN_DD30	FMCP HA bank data p23	1.2V or 1.5V*(1)
FMCP_HA_n[0]	PIN_DC23	FMCP HA bank data n0	1.2V or 1.5V*(1)
FMCP_HA_n[1] *(1)	PIN_DE23	FMCP HA bank data n1	1.2V or 1.5V*(1)
FMCP_HA_n[2]	PIN_DC21	FMCP HA bank data n2	1.2V or 1.5V*(1)
FMCP_HA_n[3]	PIN_DA23	FMCP HA bank data n3	1.2V or 1.5V*(1)
FMCP_HA_n[4]	PIN_DJ17	FMCP HA bank data n4	1.2V or 1.5V*(1)
FMCP_HA_n[5]	PIN_DA21	FMCP HA bank data n5	1.2V or 1.5V*(1)
FMCP_HA_n[6]	PIN_DJ21	FMCP HA bank data n6	1.2V or 1.5V*(1)
FMCP_HA_n[7]	PIN_DE17	FMCP HA bank data n7	1.2V or 1.5V*(1)
FMCP_HA_n[8]	PIN_DJ19	FMCP HA bank data n8	1.2V or 1.5V*(1)
FMCP_HA_n[9]	PIN_DE19	FMCP HA bank data n9	1.2V or 1.5V*(1)
FMCP_HA_n[10]	PIN_DJ23	FMCP HA bank data n10	1.2V or 1.5V*(1)
FMCP_HA_n[11]	PIN_DA27	FMCP HA bank data n11	1.2V or 1.5V*(1)
FMCP_HA_n[12]	PIN_DJ25	FMCP HA bank data n12	1.2V or 1.5V*(1)
FMCP_HA_n[13]	PIN_DE21	FMCP HA bank data n13	1.2V or 1.5V*(1)
FMCP_HA_n[14]	PIN_DE27	FMCP HA bank data n14	1.2V or 1.5V*(1)

FMCP_HA_n[15]	PIN_DJ27	FMCP HA bank data n15	1.2V or 1.5V*(1)
FMCP_HA_n[16]	PIN_DE25	FMCP HA bank data n16	1.2V or 1.5V*(1)
FMCP_HA_n[17]	PIN_DC25	FMCP HA bank data n17	1.2V or 1.5V*(1)
FMCP_HA_n[18]	PIN_DA31	FMCP HA bank data n18	1.2V or 1.5V*(1)
FMCP_HA_n[19]	PIN_DC27	FMCP HA bank data n19	1.2V or 1.5V*(1)
FMCP_HA_n[20]	PIN_DA29	FMCP HA bank data n20	1.2V or 1.5V*(1)
FMCP_HA_n[21]	PIN_DC29	FMCP HA bank data n21	1.2V or 1.5V*(1)
FMCP_HA_n[22]	PIN_DA25	FMCP HA bank data n22	1.2V or 1.5V*(1)
FMCP_HA_n[23]	PIN_DC31	FMCP HA bank data n23	1.2V or 1.5V*(1)
FMCP_HB_p[0]	PIN_CV26	FMCP HB bank data p0	1.2V or 1.5V*(1)
FMCP_HB_p[1]	PIN_CT30	FMCP HB bank data p1	1.2V or 1.5V*(1)
FMCP_HB_p[2]	PIN_CP26	FMCP HB bank data p2	1.2V or 1.5V*(1)
FMCP_HB_p[3]	PIN_CK28	FMCP HB bank data p3	1.2V or 1.5V*(1)
FMCP_HB_p[4]	PIN_CP24	FMCP HB bank data p4	1.2V or 1.5V*(1)
FMCP_HB_p[5]	PIN_CT28	FMCP HB bank data p5	1.2V or 1.5V*(1)
FMCP_HB_p[6]	PIN_CP28	FMCP HB bank data p6	1.2V or 1.5V*(1)
FMCP_HB_p[7]	PIN_CT24	FMCP HB bank data p7	1.2V or 1.5V*(1)
FMCP_HB_p[8]	PIN_CV24	FMCP HB bank data p8	1.2V or 1.5V*(1)
FMCP_HB_p[9]	PIN_CK30	FMCP HB bank data p9	1.2V or 1.5V*(1)
FMCP_HB_p[10]	PIN_CV30	FMCP HB bank data p10	1.2V or 1.5V*(1)
FMCP_HB_p[11]	PIN_CK26	FMCP HB bank data p11	1.2V or 1.5V*(1)
FMCP_HB_p[12]	PIN_CP30	FMCP HB bank data p12	1.2V or 1.5V*(1)
FMCP_HB_p[13]	PIN_CT32	FMCP HB bank data p13	1.2V or 1.5V*(1)
FMCP_HB_p[14]	PIN_CV32	FMCP HB bank data p14	1.2V or 1.5V*(1)
FMCP_HB_p[15]	PIN_CK24	FMCP HB bank data p15	1.2V or 1.5V*(1)
FMCP_HB_p[16]	PIN_CP32	FMCP HB bank data p16	1.2V or 1.5V*(1)
FMCP_HB_p[17]	PIN_CV34	FMCP HB bank data p17	1.2V or 1.5V*(1)

FMCP_HB_p[18]	PIN_CK34	FMCP HB bank data p18	1.2V or 1.5V*(1)
FMCP_HB_p[19]	PIN_CK32	FMCP HB bank data p19	1.2V or 1.5V*(1)
FMCP_HB_p[20]	PIN_CP34	FMCP HB bank data p20	1.2V or 1.5V*(1)
FMCP_HB_p[21]	PIN_CT34	FMCP HB bank data p21	1.2V or 1.5V*(1)
FMCP_HB_n[0]	PIN_CW27	FMCP HB bank data n0	1.2V or 1.5V*(1)
FMCP_HB_n[1]	PIN_CR31	FMCP HB bank data n1	1.2V or 1.5V*(1)
FMCP_HB_n[2]	PIN_CN27	FMCP HB bank data n2	1.2V or 1.5V*(1)
FMCP_HB_n[3]	PIN_CL29	FMCP HB bank data n3	1.2V or 1.5V*(1)
FMCP_HB_n[4]	PIN_CN25	FMCP HB bank data n4	1.2V or 1.5V*(1)
FMCP_HB_n[5]	PIN_CR29	FMCP HB bank data n5	1.2V or 1.5V*(1)
FMCP_HB_n[6]	PIN_CN29	FMCP HB bank data n6	1.2V or 1.5V*(1)
FMCP_HB_n[7]	PIN_CR25	FMCP HB bank data n7	1.2V or 1.5V*(1)
FMCP_HB_n[8]	PIN_CW25	FMCP HB bank data n8	1.2V or 1.5V*(1)
FMCP_HB_n[9]	PIN_CL31	FMCP HB bank data n9	1.2V or 1.5V*(1)
FMCP_HB_n[10]	PIN_CW31	FMCP HB bank data n10	1.2V or 1.5V*(1)
FMCP_HB_n[11]	PIN_CL27	FMCP HB bank data n11	1.2V or 1.5V*(1)
FMCP_HB_n[12]	PIN_CN31	FMCP HB bank data n12	1.2V or 1.5V*(1)
FMCP_HB_n[13]	PIN_CR33	FMCP HB bank data n13	1.2V or 1.5V*(1)
FMCP_HB_n[14]	PIN_CW33	FMCP HB bank data n14	1.2V or 1.5V*(1)
FMCP_HB_n[15]	PIN_CL25	FMCP HB bank data n15	1.2V or 1.5V*(1)
FMCP_HB_n[16]	PIN_CN33	FMCP HB bank data n16	1.2V or 1.5V*(1)
FMCP_HB_n[17]	PIN_CW35	FMCP HB bank data n17	1.2V or 1.5V*(1)
FMCP_HB_n[18]	PIN_CL35	FMCP HB bank data n18	1.2V or 1.5V*(1)
FMCP_HB_n[19]	PIN_CL33	FMCP HB bank data n19	1.2V or 1.5V*(1)
FMCP_HB_n[20]	PIN_CN35	FMCP HB bank data n20	1.2V or 1.5V*(1)
FMCP_HB_n[21]	PIN_CR35	FMCP HB bank data n21	1.2V or 1.5V*(1)
FMCP_LA_p[0]	PIN_DF10	FMCP LA bank data p0	1.2 V

FMCP_LA_p[1]	PIN_DD10	FMCP LA bank data p1	1.2 V
FMCP_LA_p[2]	PIN_DD18	FMCP LA bank data p2	1.2 V
FMCP_LA_p[3]	PIN_CY12	FMCP LA bank data p3	1.2 V
FMCP_LA_p[4]	PIN_DD14	FMCP LA bank data p4	1.2 V
FMCP_LA_p[5]	PIN_DH6	FMCP LA bank data p5	1.2 V
FMCP_LA_p[6]	PIN_DF6	FMCP LA bank data p6	1.2 V
FMCP_LA_p[7]	PIN_DH14	FMCP LA bank data p7	1.2 V
FMCP_LA_p[8]	PIN_DF8	FMCP LA bank data p8	1.2 V
FMCP_LA_p[9]	PIN_DH8	FMCP LA bank data p9	1.2 V
FMCP_LA_p[10]	PIN_DF12	FMCP LA bank data p10	1.2 V
FMCP_LA_p[11]	PIN_DF4	FMCP LA bank data p11	1.2 V
FMCP_LA_p[12]	PIN_CY18	FMCP LA bank data p12	1.2 V
FMCP_LA_p[13]	PIN_DH10	FMCP LA bank data p13	1.2 V
FMCP_LA_p[14]	PIN_DF14	FMCP LA bank data p14	1.2 V
FMCP_LA_p[15]	PIN_DH12	FMCP LA bank data p15	1.2 V
FMCP_LA_p[16]	PIN_DF2	FMCP LA bank data p16	1.2 V
FMCP_LA_p[17]	PIN_CV16	FMCP LA bank data p17	1.2 V
FMCP_LA_p[18]	PIN_CT14	FMCP LA bank data p18	1.2 V
FMCP_LA_p[19]	PIN_CV12	FMCP LA bank data p19	1.2 V
FMCP_LA_p[20]	PIN_CT12	FMCP LA bank data p20	1.2 V
FMCP_LA_p[21]	PIN_CV20	FMCP LA bank data p21	1.2 V
FMCP_LA_p[22]	PIN_CK12	FMCP LA bank data p22	1.2 V
FMCP_LA_p[23]	PIN_CP16	FMCP LA bank data p23	1.2 V
FMCP_LA_p[24]	PIN_CP18	FMCP LA bank data p24	1.2 V
FMCP_LA_p[25]	PIN_CT18	FMCP LA bank data p25	1.2 V
FMCP_LA_p[26]	PIN_CV18	FMCP LA bank data p26	1.2 V
FMCP_LA_p[27]	PIN_CT16	FMCP LA bank data p27	1.2 V

FMCP_LA_p[28]	PIN_CV22	FMCP LA bank data p28	1.2 V
FMCP_LA_p[29]	PIN_CT20	FMCP LA bank data p29	1.2 V
FMCP_LA_p[30]	PIN_CP20	FMCP LA bank data p30	1.2 V
FMCP_LA_p[31]	PIN_CK16	FMCP LA bank data p31	1.2 V
FMCP_LA_p[32]	PIN_CK20	FMCP LA bank data p32	1.2 V
FMCP_LA_p[33]	PIN_CT22	FMCP LA bank data p33	1.2 V
FMCP_LA_n[0]	PIN_DE11	FMCP LA bank data n0	1.2 V
FMCP_LA_n[1]	PIN_DC11	FMCP LA bank data n1	1.2 V
FMCP_LA_n[2]	PIN_DC19	FMCP LA bank data n2	1.2 V
FMCP_LA_n[3]	PIN_DA13	FMCP LA bank data n3	1.2 V
FMCP_LA_n[4]	PIN_DC15	FMCP LA bank data n4	1.2 V
FMCP_LA_n[5]	PIN_DJ7	FMCP LA bank data n5	1.2 V
FMCP_LA_n[6]	PIN_DE7	FMCP LA bank data n6	1.2 V
FMCP_LA_n[7]	PIN_DJ15	FMCP LA bank data n7	1.2 V
FMCP_LA_n[8]	PIN_DE9	FMCP LA bank data n8	1.2 V
FMCP_LA_n[9]	PIN_DJ9	FMCP LA bank data n9	1.2 V
FMCP_LA_n[10]	PIN_DE13	FMCP LA bank data n10	1.2 V
FMCP_LA_n[11]	PIN_DE5	FMCP LA bank data n11	1.2 V
FMCP_LA_n[12]	PIN_DA19	FMCP LA bank data n12	1.2 V
FMCP_LA_n[13]	PIN_DJ11	FMCP LA bank data n13	1.2 V
FMCP_LA_n[14]	PIN_DE15	FMCP LA bank data n14	1.2 V
FMCP_LA_n[15]	PIN_DJ13	FMCP LA bank data n15	1.2 V
FMCP_LA_n[16]	PIN_DE3	FMCP LA bank data n16	1.2 V
FMCP_LA_n[17]	PIN_CW17	FMCP LA bank data n17	1.2 V
FMCP_LA_n[18]	PIN_CR15	FMCP LA bank data n18	1.2 V
FMCP_LA_n[19]	PIN_CW13	FMCP LA bank data n19	1.2 V
FMCP_LA_n[20]	PIN_CR13	FMCP LA bank data n20	1.2 V

FMCP_LA_n[21]	PIN_CW21	FMCP LA bank data n21	1.2 V
FMCP_LA_n[22]	PIN_CL13	FMCP LA bank data n22	1.2 V
FMCP_LA_n[23]	PIN_CN17	FMCP LA bank data n23	1.2 V
FMCP_LA_n[24]	PIN_CN19	FMCP LA bank data n24	1.2 V
FMCP_LA_n[25]	PIN_CR19	FMCP LA bank data n25	1.2 V
FMCP_LA_n[26]	PIN_CW19	FMCP LA bank data n26	1.2 V
FMCP_LA_n[27]	PIN_CR17	FMCP LA bank data n27	1.2 V
FMCP_LA_n[28]	PIN_CW23	FMCP LA bank data n28	1.2 V
FMCP_LA_n[29]	PIN_CR21	FMCP LA bank data n29	1.2 V
FMCP_LA_n[30]	PIN_CN21	FMCP LA bank data n30	1.2 V
FMCP_LA_n[31]	PIN_CL17	FMCP LA bank data n31	1.2 V
FMCP_LA_n[32]	PIN_CL21	FMCP LA bank data n32	1.2 V
FMCP_LA_n[33]	PIN_CR23	FMCP LA bank data n33	1.2 V
FMCP_GBTCLK_M2C_p[0]	PIN_CD8	LVDS input from the installed FMCP card to dedicated reference clock input pin	HCSL
FMCP_GBTCLK_M2C_p[1]	PIN_CJ7	LVDS input from the installed FMCP card to dedicated reference clock input pin	HCSL
FMCP_DP_C2M_p[0]	PIN_AK4	Transmit pair p0 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_C2M_p[1]	PIN_AN7	Transmit pair p1 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_C2M_p[2]	PIN_AP4	Transmit pair p2 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_C2M_p[3]	PIN_AU7	Transmit pair p3 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_C2M_p[4]	PIN_AV4	Transmit pair p4 of the	High Speed

		FPGA transceiver	Differential I/O
FMCP_DP_C2M_p[5]	PIN_BA7	Transmit pair p5 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_C2M_p[6]	PIN_BB4	Transmit pair p6 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_C2M_p[7]	PIN_BF4	Transmit pair p7 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_C2M_p[8]	PIN_BK4	Transmit pair p8 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_C2M_p[9]	PIN_BP4	Transmit pair p9 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_C2M_p[10]	PIN_BV4	Transmit pair p10 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_C2M_p[11]	PIN_CB4	Transmit pair p11 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_C2M_p[12]	PIN_CF4	Transmit pair p12 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_C2M_p[13]	PIN_CK4	Transmit pair p13 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_C2M_p[14]	PIN_CN7	Transmit pair p14 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_C2M_p[15]	PIN_CU7	Transmit pair p15 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[0]	PIN_AF4	Receiver pair p0 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[1]	PIN_AJ1	Receiver pair p1 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[2]	PIN_AN1	Receiver pair p2 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[3]	PIN_AU1	Receiver pair p3 of the FPGA transceiver	High Speed Differential I/O

FMCP_DP_M2C_p[4]	PIN_BA1	Receiver pair p4 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[5]	PIN_BE1	Receiver pair p5 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[6]	PIN_BJ1	Receiver pair p6 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[7]	PIN_BN1	Receiver pair p7 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[8]	PIN_BU1	Receiver pair p8 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[9]	PIN_CA1	Receiver pair p9 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[10]	PIN_CE1	Receiver pair p10 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[11]	PIN_CJ1	Receiver pair p11 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[12]	PIN_CN1	Receiver pair p12 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[13]	PIN_CP4	Receiver pair p13 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[14]	PIN_CU1	Receiver pair p14 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[15]	PIN_CV4	Receiver pair p15 of the FPGA transceiver	High Speed Differential I/O
FMCP_REFCLK_C2M_p	PIN_CK14	Reference clock from carrier card mezzanine module to positive	DIFFERENTIAL 1.2-V SSTL
FMCP_REFCLK_M2C_p	PIN_CK22	Reference clock from mezzanine module to carrier card positive	True Differential Signaling
FMCP_GA[0]	PIN_DA17	FMCP geographical	3.3 V*(2)

		address 0	
FMCP_GA[1]	PIN_CY16	FMCP geographical address 1	3.3 V*(2)
FMCP_SCL	PIN_DA11	Management serial clock line	3.3 V*(2)
FMCP_SDA	PIN_CP12	Management serial data line	3.3 V*(2)
FMCP_RES[0]	PIN_CG13	Reserved	1.8 V*(3)
FMCP_RES[1]	PIN_CN13	Reserved	1.2 V
FMCP_SYNC_C2M_p	PIN_CP22	Synchronize signal from carrier card to mezzanine module positive	DIFFERENTIAL 1.2-V SSTL
FMCP_SYNC_M2C_p	PIN_CY14	Synchronize signal from mezzanine module to carrier card positive	True Differential Signaling

- *(1): The FMC_VCCIO value depends on the setting of JP2, which can adjust the FMC_VCCIO to **1.2V or 1.5V**. Please refer to section 2.3 : "*FMC_VCCIO Select Header*" for details.
  *(2): There are level shift ICs that convert FMCP_VCCIO to 3.3V between the FPGA pins and the FMC pins.
  *(3): For PCIe Card Applications

2.11 USB to UART

The board provides two UART functions (See **Figure 2-20**). One of them is connected to HPS fabric in the Agilex FPGA, allowing host to communicate and debug with the HPS fabric through the UART interface. The other one is to connect to the system MAX10 device. It allows users to monitor various status of the board such as temperature and voltage value from the Host.

The board uses a USB hub to allow two USB to UART interface (HPS fabric and system MAX10) and a USB Blaster II circuit to share a Micro USB connector to connect to the host. Users only need one Micro USB cable to establish several UART and JTAG connections with the Host to transmit data.

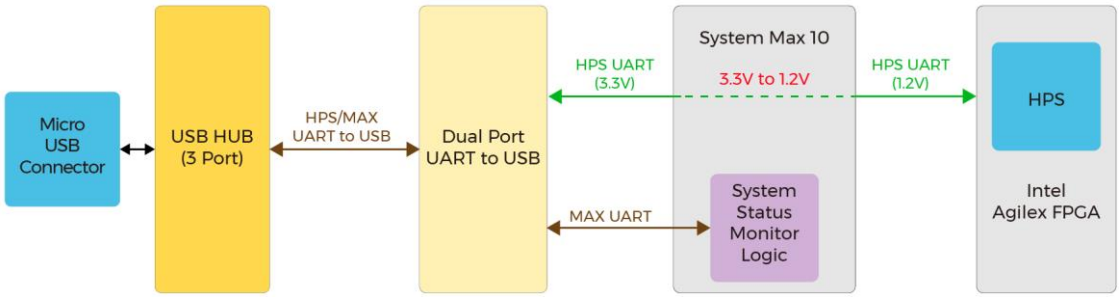


Figure 2-20 The UART interface on the board

■ USB to UART for HPS Fabric

The board provides a UART interface for users to communicate and transfer data with HPS through the host. This interface is mainly implemented via a dual UART to USB (CP2105). For detailed chip information, please refer to \Datasheets\UART_TO_USB\ of the system CD. It can convert commands and data from the host via USB protocol to the UART interface and send it to HPS. **Figure 2-21** shows the connections between the HPS, CP2105 chip, and the Micro USB connector.

Table 2-22 lists the pin assignment of UART interface connected to the HPS.

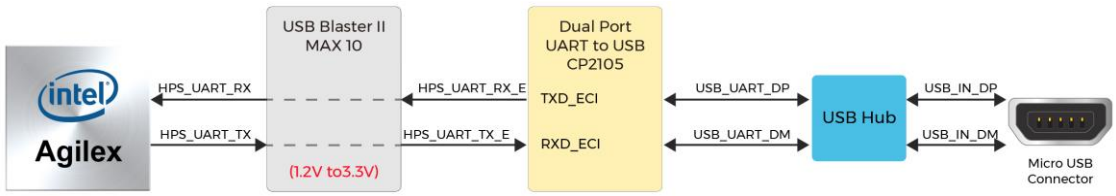


Figure 2-21 Connections between the HPS of Board and FT232R Chip

Table 2-22 Pin Assignment of UART Interface

Signal Name	FPGA Pin No.	Description	I/O Standard
HPS_UART_RX	PIN_AF8	HPS UART Receiver	1.8V
HPS_UART_TX	PIN_AT12	HPS UART Transmitter	1.8V

■ USB to UART for System MAX10

The other USB to UART interface is connected with the System MAX10. It allows users to monitor the status of the board from the host through the UART interface. As shown in **Figure 2-22**, the board provides several sensors to monitor the status of the board, such as FPGA temperature, board power monitor, and fan speed status. These interfaces are connected to the System MAX10 FPGA on the board. The board management logic (**Dashboard**) in the system MAX10 FPGA will monitor these status and perform corresponding control according to the status. For example, when the temperature of the FPGA increases, the system will automatically increase the fan speed to reduce the temperature. When the temperature of the FPGA continues to exceed the working range (such as a fan failure condition), the FPGA power will be cut to protect the board.

See **chapter 3** for details. Terasic also provide a "board information IP" that allow user can place it in the Agilex FPGA to read these board status. Please refer to the section 2.5 of the demonstration manual.

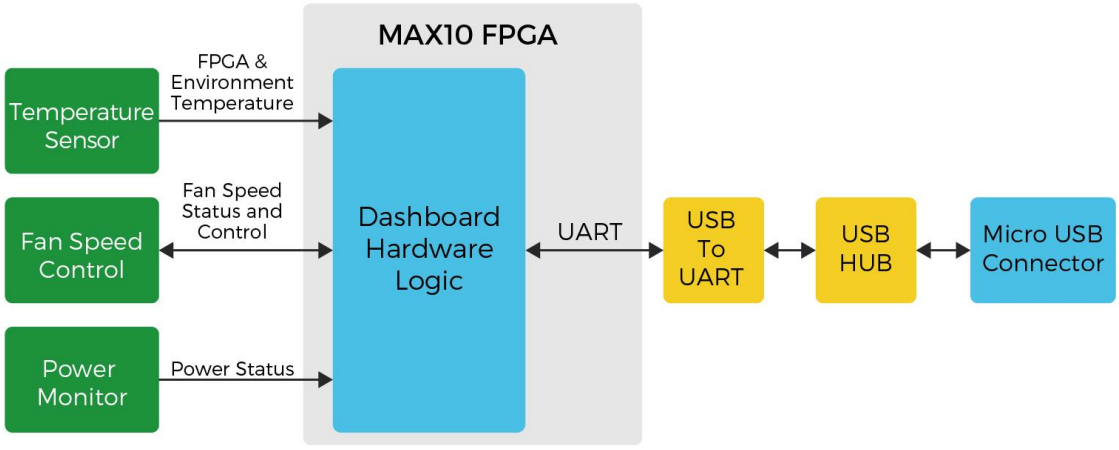


Figure 2-22 Block diagram of the system status interface

2.12 Micro SD Card Socket

The board supports Micro SD card interface with x4 data lines. It serves for an external storage for the **HPS fabric**. Figure 2-23 shows signals connected between the HPS and Micro SD card socket. **Table 2-23** lists the pin assignment of Micro SD card socket

to the HPS.

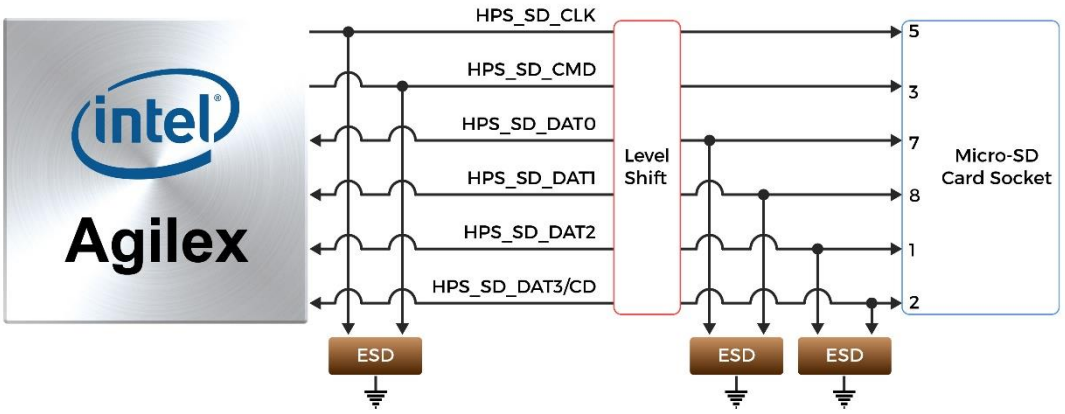


Figure 2-23 Pin-out of Micro SD Card socket

Table 2-23 Micro SD Card Socket Header Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	Description	I/O Standard	FPGA Pin Number
HPS_SD_CLK	HPS SD Clock	1.8-V	PIN_AB9
HPS_SD_CMD	HPS SD Command Line	1.8-V	PIN_V3
HPS_SD_DATA[0]	HPS SD Data[0]	1.8-V	PIN_AD9
HPS_SD_DATA[1]	HPS SD Data[1]	1.8-V	PIN_T3
HPS_SD_DATA[2]	HPS SD Data[2]	1.8-V	PIN_AC10
HPS_SD_DATA[3]	HPS SD Data[3]	1.8-V	PIN_P3

2.13 Gigabit Ethernet

The board supports Gigabit Ethernet transfer by an external Micrel KSZ9031RN PHY chip and **HPS** Ethernet MAC function. The KSZ9031RN chip with integrated 10/100/1000 Mbps Gigabit Ethernet transceiver also supports RGMII MAC interface. **Figure 2-24** shows the connections between the HPS, Gigabit Ethernet PHY, and RJ-45 connector.

For more information about the KSZ9031RN PHY chip and its datasheet, as well as the application notes, which are available on the manufacturer's website.

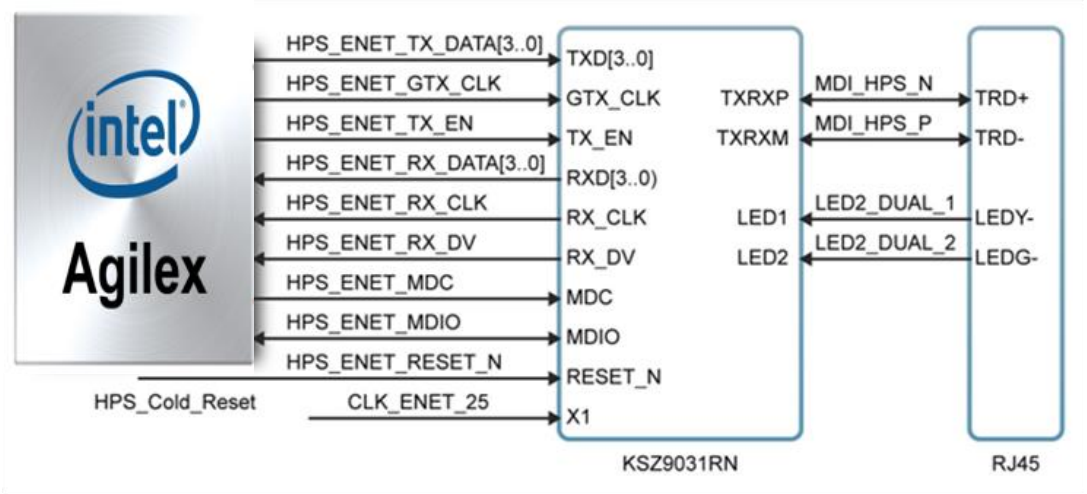


Figure 2-24 Connections between the HPS of Board and RGMII MAC

There are two LEDs, a green LED (LEDG) and a yellow LED (LEDY), which represent the status of the Ethernet PHY (KSZ9031RN). The LED control signals are connected to the LEDs on the RJ45 connector. The state and the definition of LEDG and LEDY are listed in **Table 2-24**. For instance, the connection from board to Gigabit Ethernet is established once the LEDG lights on.

Table 2-24 State and Definition of LED Mode Pins

LED (State)		LED (Definition)		Link /Activity
LEDG	LEDY	LEDG	LEDY	
H	H	OFF	OFF	Link off
L	H	ON	OFF	1000 Link / No Activity
Toggle	H	Blinking	OFF	1000 Link / Activity (RX, TX)
H	L	OFF	ON	100 Link / No Activity
H	Toggle	OFF	Blinking	100 Link / Activity (RX, TX)
L	L	ON	ON	10 Link/ No Activity
Toggle	Toggle	Blinking	Blinking	Link / Activity (RX, TX)

Table 2-25 Pin Assignment of Gigabit Ethernet PHY

Signal Name	FPGA Pin No	Description	I/O Standard
HPS_ENET_TX_CTL	PIN_AL13	GMII and MII transmit enable	1.8V

HPS_ENET_TX_DATA[0]	PIN_AD14	MII transmit data[0]	1.8V
HPS_ENET_TX_DATA[1]	PIN_AN13	MII transmit data[1]	1.8V
HPS_ENET_TX_DATA[2]	PIN_AG9	MII transmit data[2]	1.8V
HPS_ENET_TX_DATA[3]	PIN_AT14	MII transmit data[3]	1.8V
HPS_ENET_RX_CTL	PIN_AM14	GMII and MII receive data valid	1.8V
HPS_ENET_RX_DATA[0]	PIN_AG11	GMII and MII receive data[0]	1.8V
HPS_ENET_RX_DATA[1]	PIN_AP14	GMII and MII receive data[1]	1.8V
HPS_ENET_RX_DATA[2]	PIN_AF12	GMII and MII receive data[2]	1.8V
HPS_ENET_RX_DATA[3]	PIN_AU13	GMII and MII receive data[3]	1.8V
HPS_ENET_RX_CLK	PIN_AH8	GMII and MII receive clock	1.8V
HPS_ENET_MDIO	PIN_AB12	Management Data	1.8V
HPS_ENET_MDC	PIN_AJ9	Management Data Clock Reference	1.8V
HPS_ENET_TX_CLK	PIN_AJ7	GMII Transmit Clock	1.8V

2.14 System Status Interface

As shown in **Figure 2-25**, the Agilex 7 FPGA Starter Kit board provides several sensors to monitor the status of the board, such as FPGA temperature, board power monitor, and fan speed status. These interfaces are connected to the System MAX10 FPGA on the board. The board management logic (Dashboard) in the System MAX10 FPGA will monitor those status and perform corresponding control according to the status. For example, when the temperature of the FPGA increases, the system will automatically increase the fan speed to reduce the temperature. When the temperature of the FPGA continues to exceed the working range (such as a fan failure condition), the FPGA power will be cut to protect the board.

The board also provides USB to UART interface to connect with the System MAX10 FPGA, so that users can monitor the status of the board from the host through the UART interface. See chapter 8 for details.

Finally, the board status also can be read on the Agilex FPGA side via the SPI interface connected to the System MAX10 FPGA. Terasic had provided a “board information IP” that allow user can place it in the FPGA to read these board status. Please refer to the **section 5.4** for detailed. **Table 2-26** shows the pin assignments of the SPI interface on the Agilex FPGA.

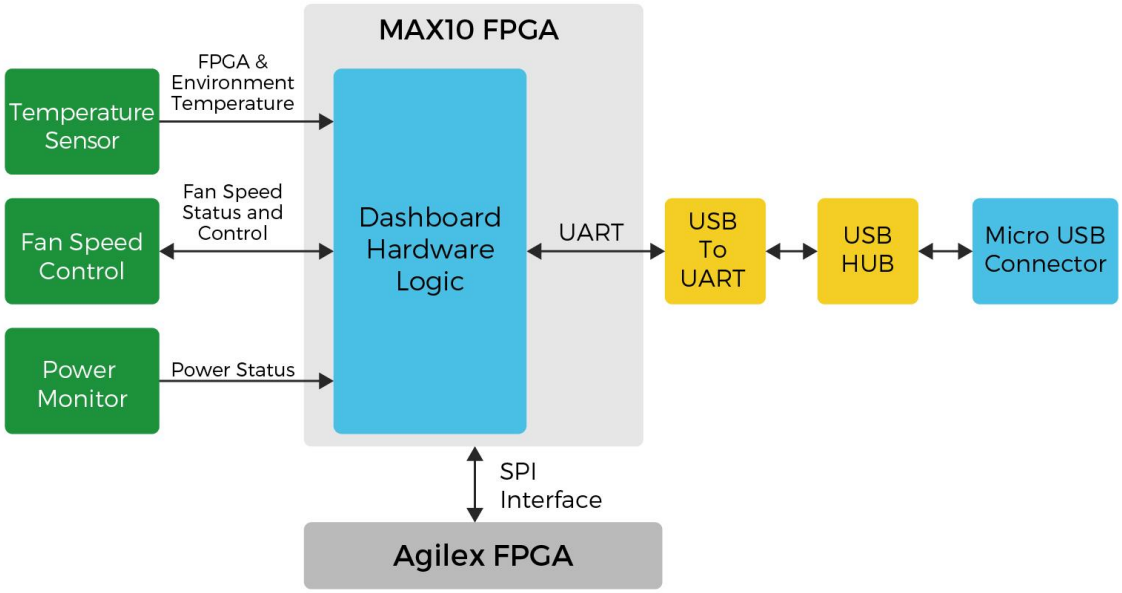


Figure 2-25 Block diagram of the system status interface

Table 2-26 Pin Assignments, Schematic Signal Names, and Functions for SPI interface of the board status

Schematic Signal Name	Description	I/O Standard	Agilex Pin Number
INFO_SPI_SCLK	Serial Clock, SPI master output to salve.	1.2V	PIN_D54
INFO_SPI_MISO	Master input.	1.2V	PIN_E51
INFO_SPI_MOSI	Master output.	1.2V	PIN_E53
INFO_SPI_CS_n	Slave Select, Master output.	1.2V	PIN_E49

Chapter 3

Dashboard GUI

The Agilex 7 FPGA Starter Kit Dashboard GUI is a board status monitor system. This system is connected from the Host to the System MAX10 FPGA on the Agilex 7 FPGA Starter Kit through the UART interface, and reads various status on the board (See section 2.14 for detailed). The reported status includes FPGA/Board temperature, fan speed, FPGA core power and 12V input power. **Figure 3-1** shows the block diagram of the Agilex 7 FPGA Starter Kit Dashboard. Note that, the Dashboard GUI software only support windows OS.

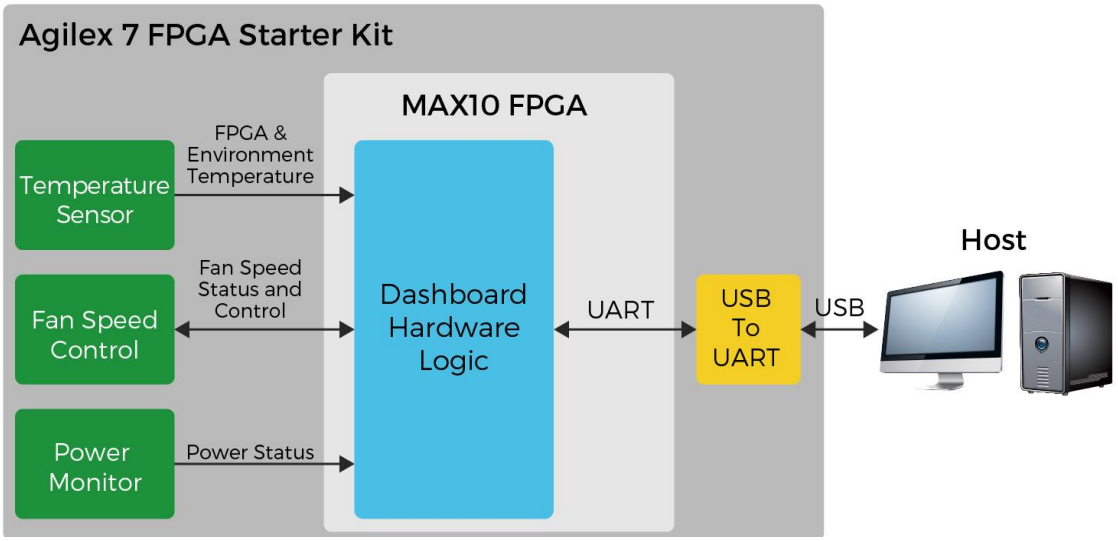


Figure 3-1 Block Diagram of the Agilex 7 FPGA Starter Kit Dashboard

3.1 Driver Installed on Host

To use the dashboard system, users need to install the USB to UART driver on the host first, so that user can establish a connection with the Agilex 7 FPGA Starter Kit board. This section will describe how to install USB to UART driver on the windows OS host.

■ USB to UART driver location

Users can find it from the path: Tool\dashboard_gui\Driver in the Agilex 7 FPGA Starter Kit system CD and copy it to the Host.

■ Connection Setting

1. Connect the Micro USB connector of the Agilex 7 FPGA Starter Kit board to the Host USB port through Micro USB cable.

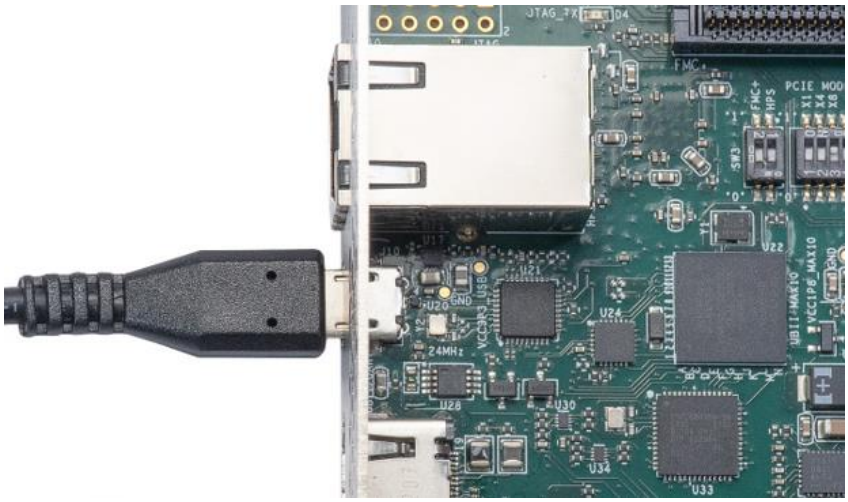


Figure 3-2 Connection setup for using dashboard system

2. Connect power to the Agilex 7 FPGA Starter Kit board.
3. Power on the Agilex 7 FPGA Starter Kit board.

■ Install Driver

When connect the Agilex 7 FPGA Starter Kit board to the Host. As shown in **Figure 3-3**, two USB to UART Com Port device is shown in “Device Manager” of Host.

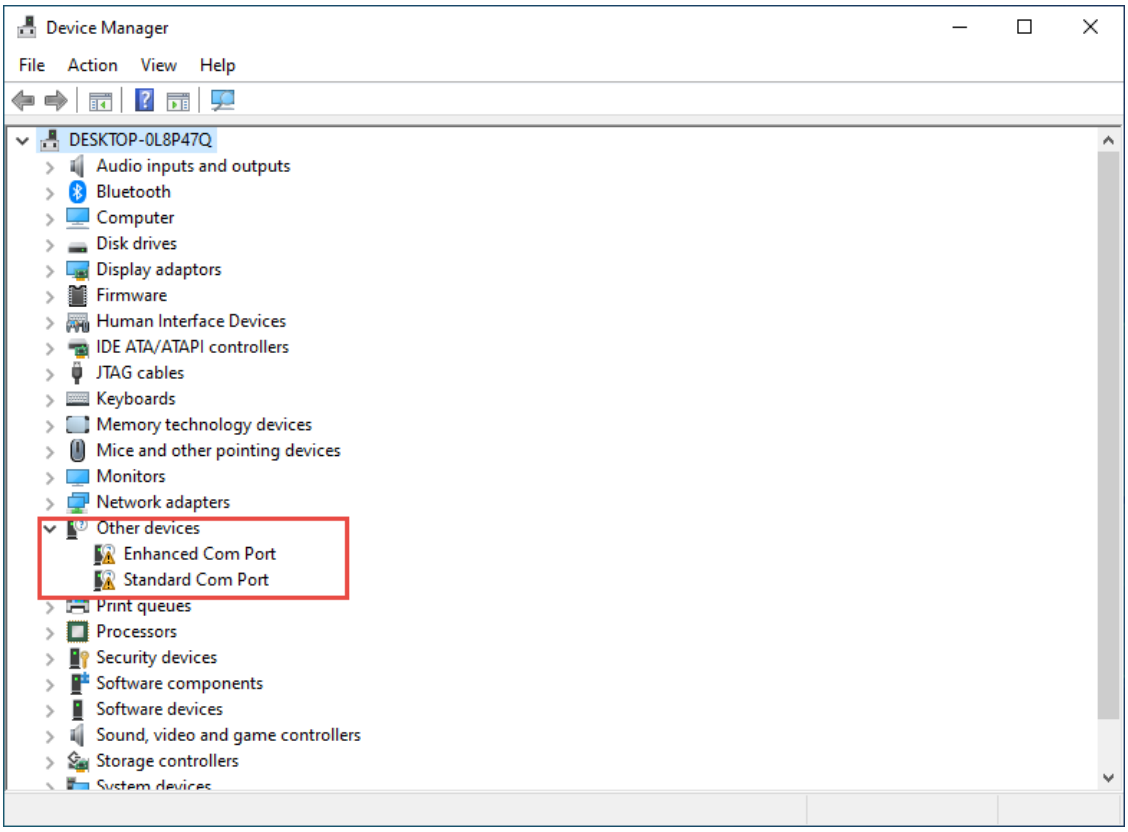


Figure 3-3 Uninstalled USB to UART device

Copy the device driver (System CD\Tool\dashboard_gui\Driver) to the Host and install it, as shown in **Figure 3-4.** Please note that the COM Port number is different in different Host.

Figure 3-4 Install USB to UART driver

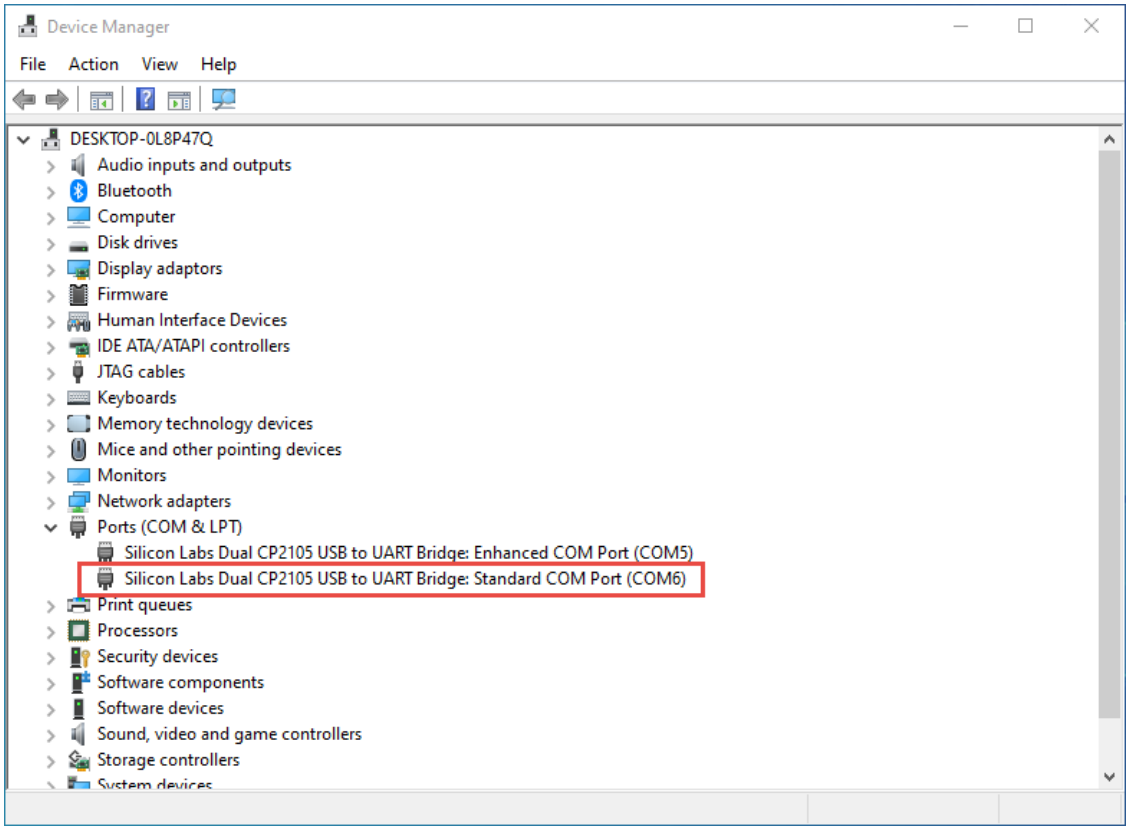


Figure 3-5 The USB to UART device after driver is installed successfully

3.2 Run Dashboard GUI

■ Dashboard GUI software location

Users can find it from the path: Tool\dashboard_gui\Dashboard.exe in the Agilex 7 FPGA Starter Kit system CD and copy it to the Host.

Execute the Dashboard.exe, a window will show as **Figure 3-6**. It will describe the detail functions as below.

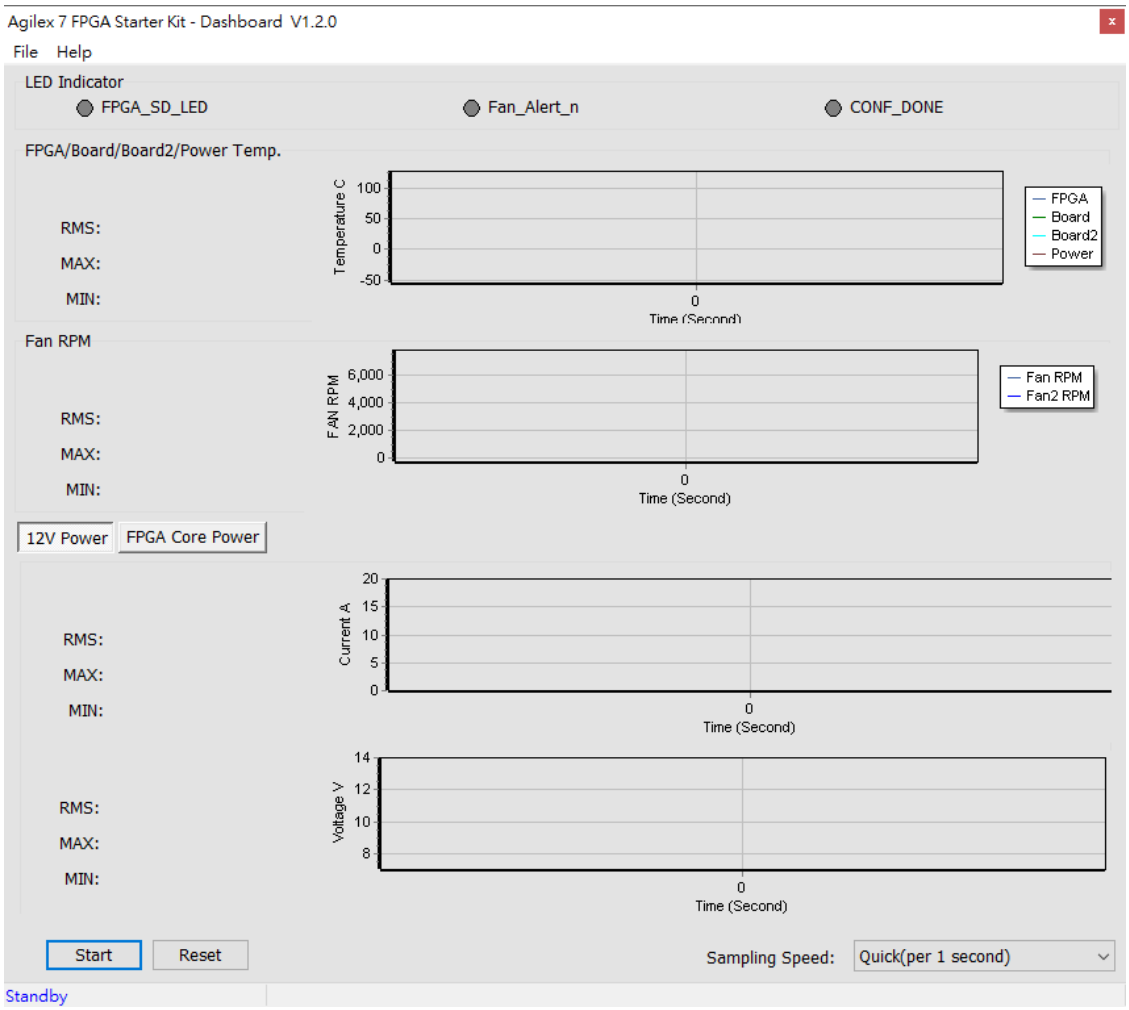


Figure 3-6 Dashboard GUI

■ Dashboard GUI function introduction

- **Start/Stop**: As shown in **Figure 3-7**, there is a Start button at the bottom-left of the GUI window. Click it to run the program (Start will change to Stop), it will show the Agilex 7 FPGA Starter Kit board status. Users can press Stop button to stop the status data transmission and display.
- **Reset Button**: Press this button to clear the historical data shown in GUI, and record the data again.

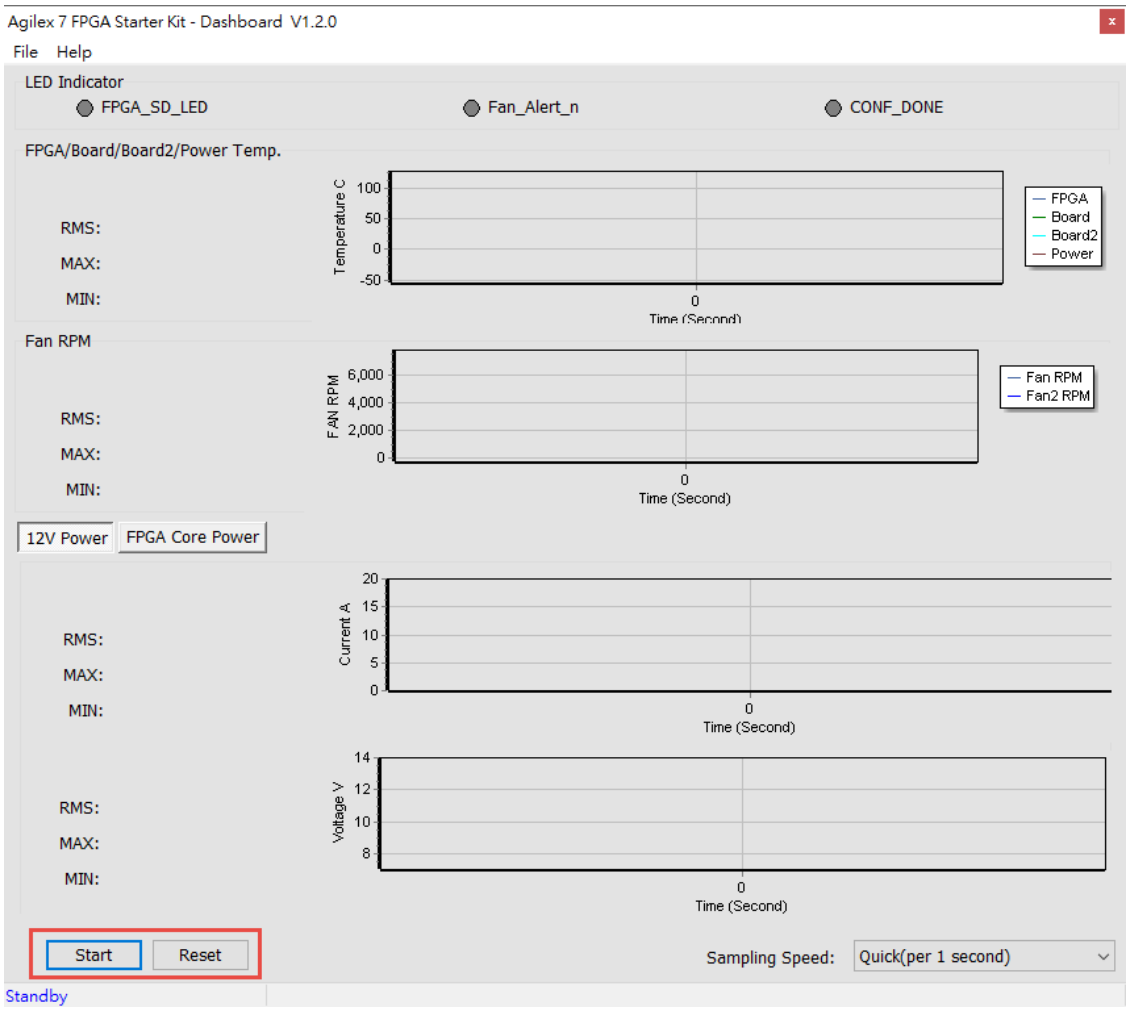


Figure 3-7 Start and Reset button

- **FPGA Status**: As shown in **Figure 3-8**, it will show the status LED number on the Agilex 7 FPGA Starter Kit board. The definitions of these indicator LEDs are as follows:

  - **FPGA_SD_LED**

    When this status is shown in green on the GUI, it means that the FPGA temperature or the board temperature exceeds 95 degrees or the power consumption exceeds 180W. All the power of the FPGA will be cut off.

  - **FPGA_Altert_n**

    When this status is shown in green on the GUI, it means that the fan is abnormal, such as when the fan speed is different from expected

- **CONF_DONE**

  Stands for FPGA configure done status. When this status is shown in green on the GUI, it means that FPGA configuration has been completed.

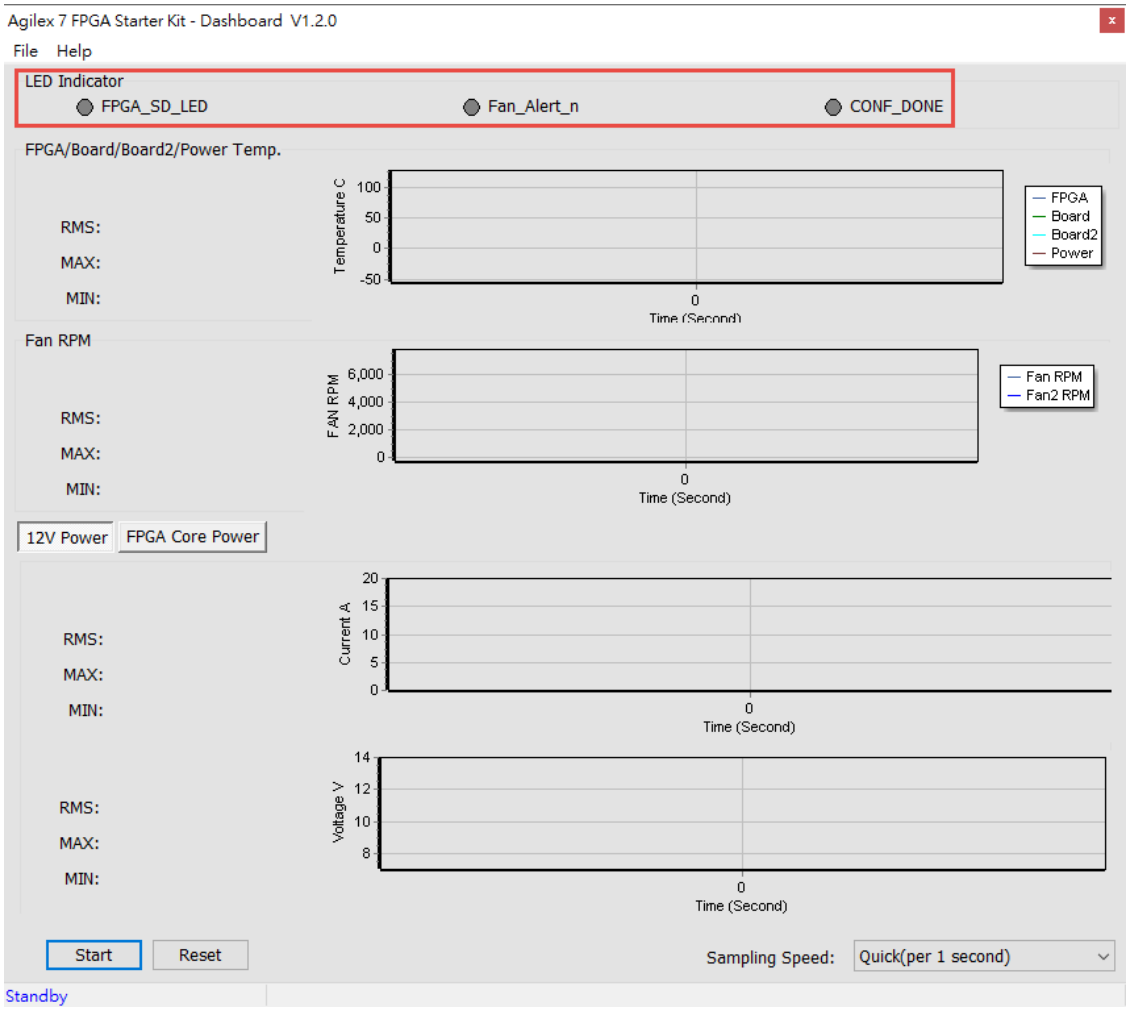


Figure 3-8 FPGA Status section

- **FPGA/Board/Transceiver Temperature**: The Dashboard GUI will real-time show the Agilex 7 FPGA Starter Kit board's ambient temperature (**Board** and **Board2** data in the GUI) and FPGA and FPGA's transceiver (**F-Tile 12C** and **F-Tile 13A**) temperature. Users can know the board's temperature status in time. The information will be refreshed per 1 second, and displays through diagram and number, as shown in **Figure 3-9**. **Figure 3-10** shows the location of the two temperature sensors of **Board** and **Board2** on the GUI.

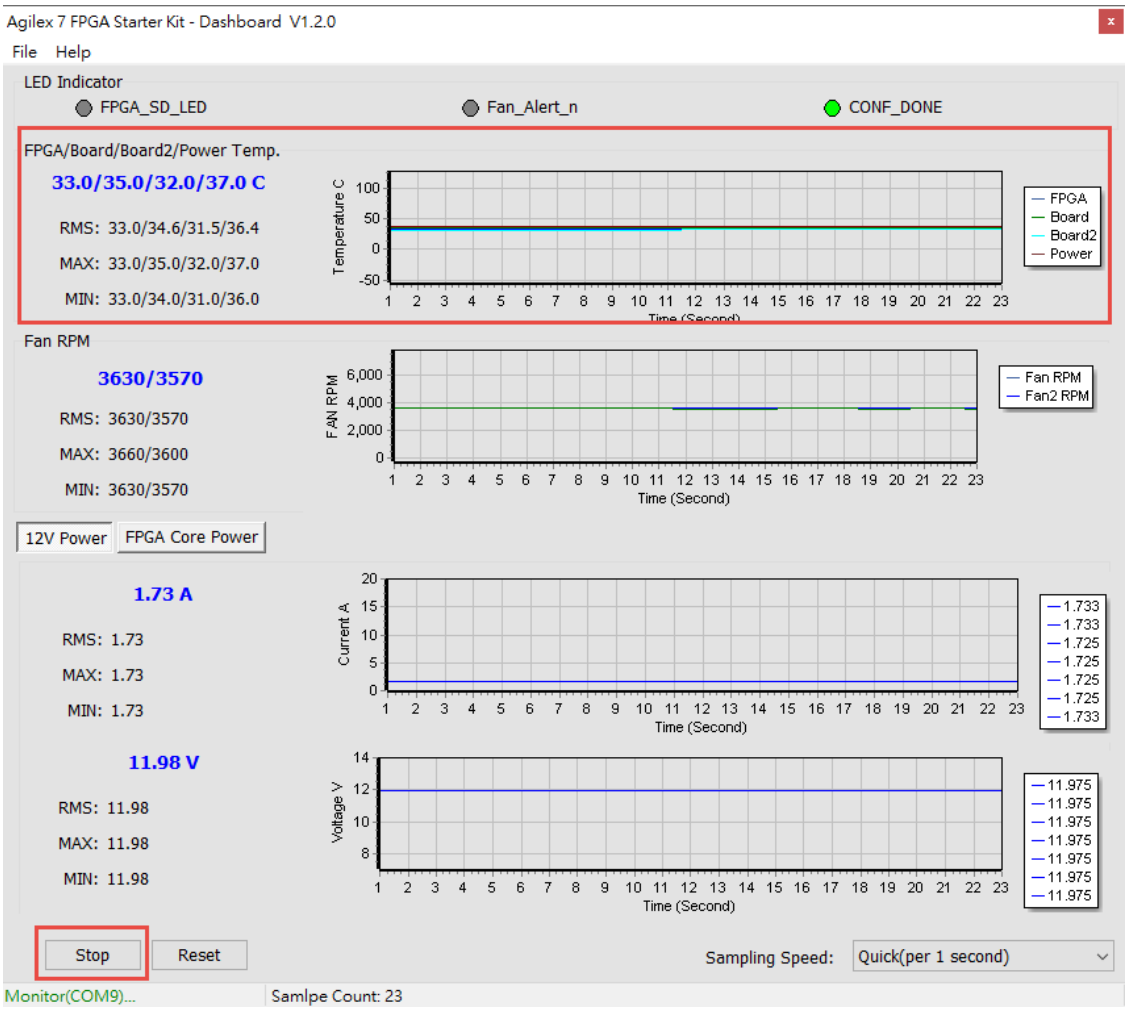


Figure 3-9 Temperature section

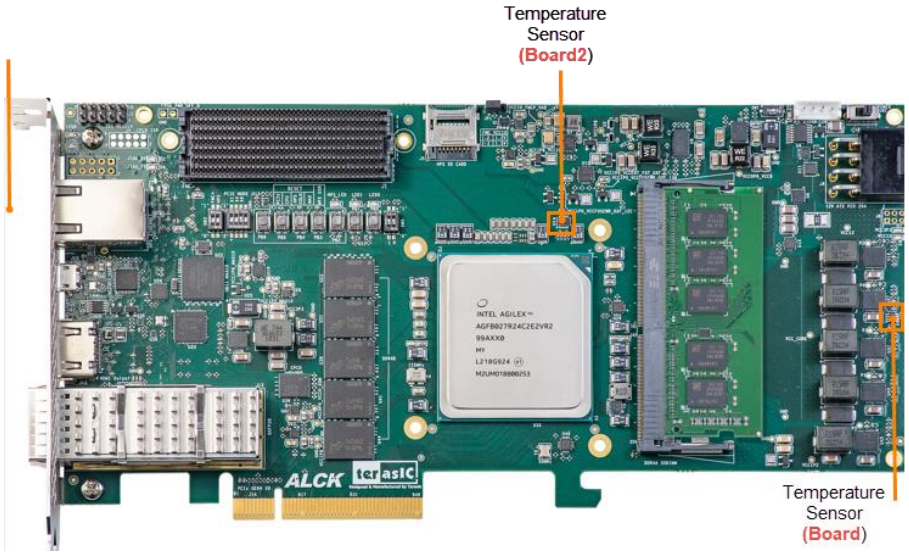


Figure 3-10 Location of the board's ambient temperature

- **Fan RPM**: It displays the real-time speed of the **two** fans (Fan and Fan2 in the GUI) on the Agilex 7 FPGA Starter Kit board, as shown in **Figure 3-11**.

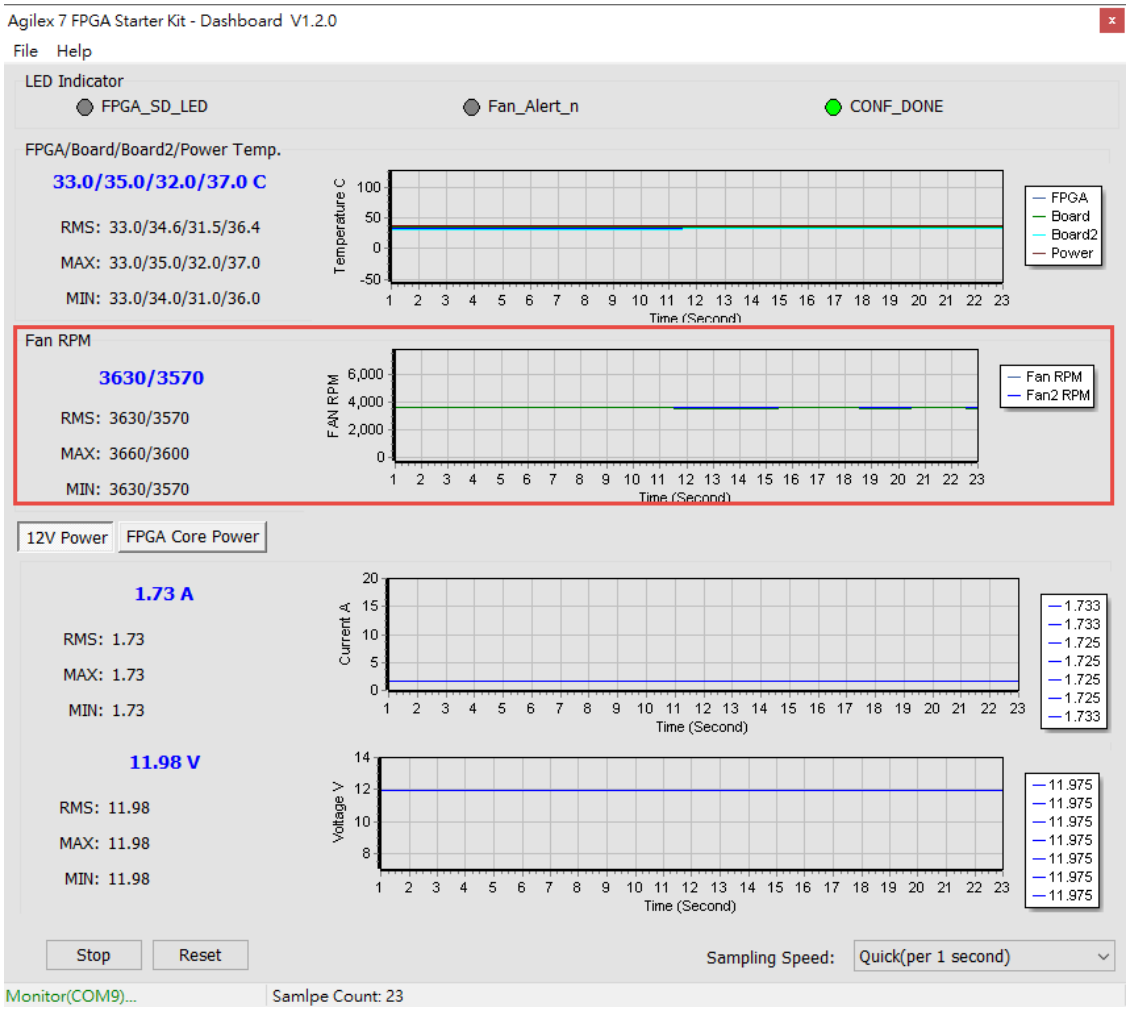


Figure 3-11 FAN RPM section

- **12V/Core Power monitor**: It displays the real-time 12V/Core Power (0.8V~0.85V) voltage and consumption current on the Agilex 7 FPGA Starter Kit board.

  When the user clicks the "**12V Power**" button (See **Figure 3-12**), the GUI will display the voltage level and current number of 12V Power on the board.

  While user clicking the "**FPGA Core Power**" button (See **Figure 3-13**), the GUI will show the voltage level and current value of the FPGA core power on the board.

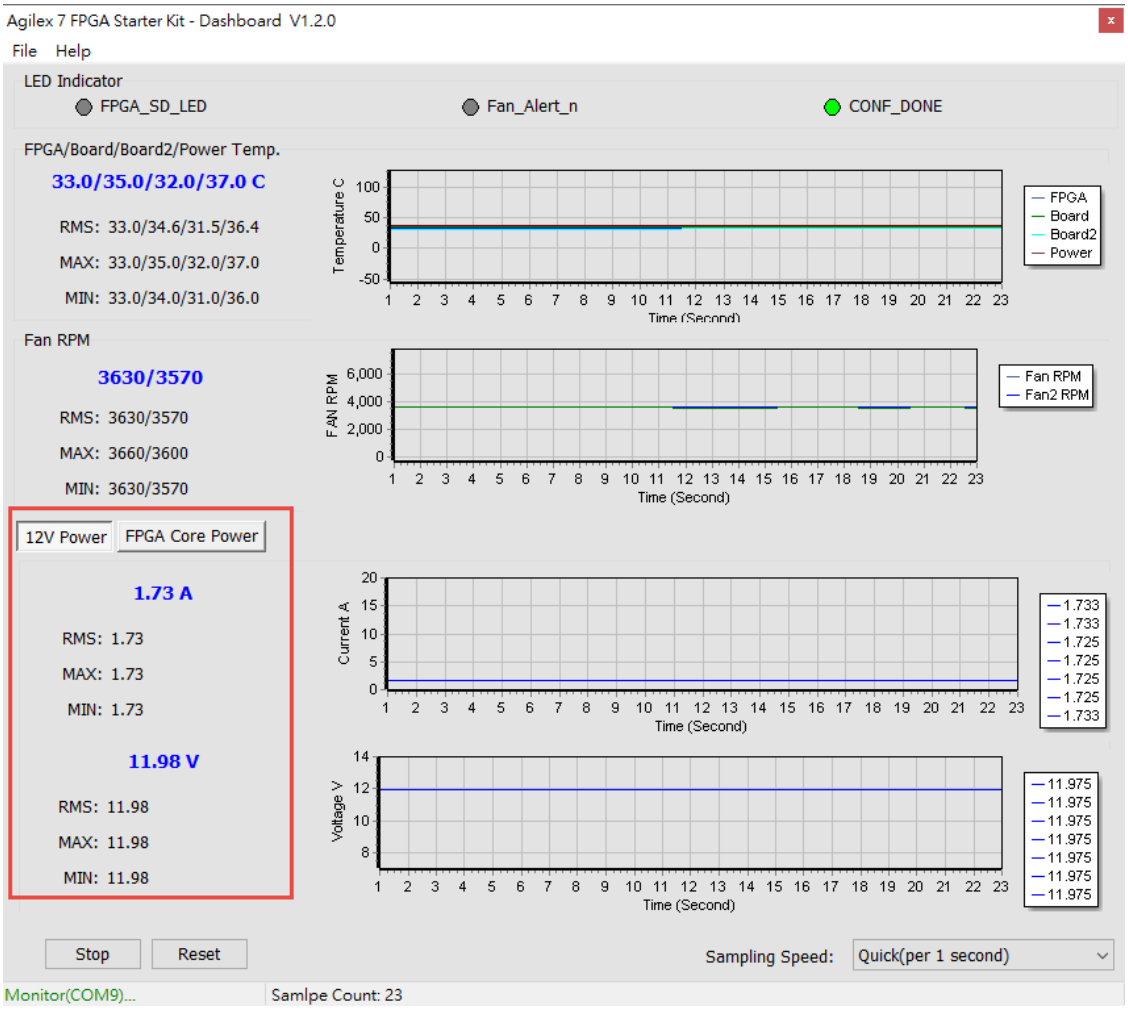


Figure 3-12 Select "12V Power"

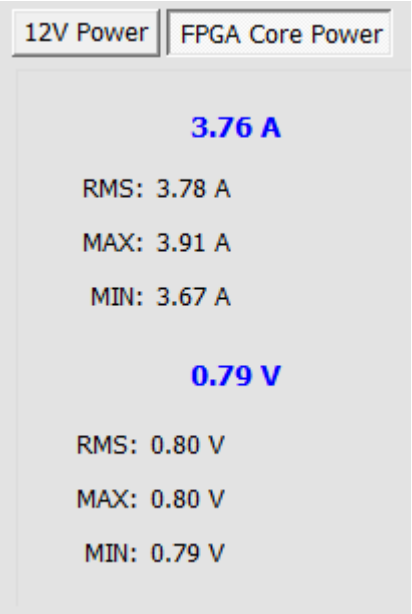


Figure 3-13 Select "FPGA Monitor Section"

- **Sampling Speed**: It can change interval time that the Dashboard GUI sample the board status. Users can adjust it to 1s/10s/1min/Full Speed (0.1s) to sample the board status, as shown in **Figure 3-14** and **Figure 3-15**.

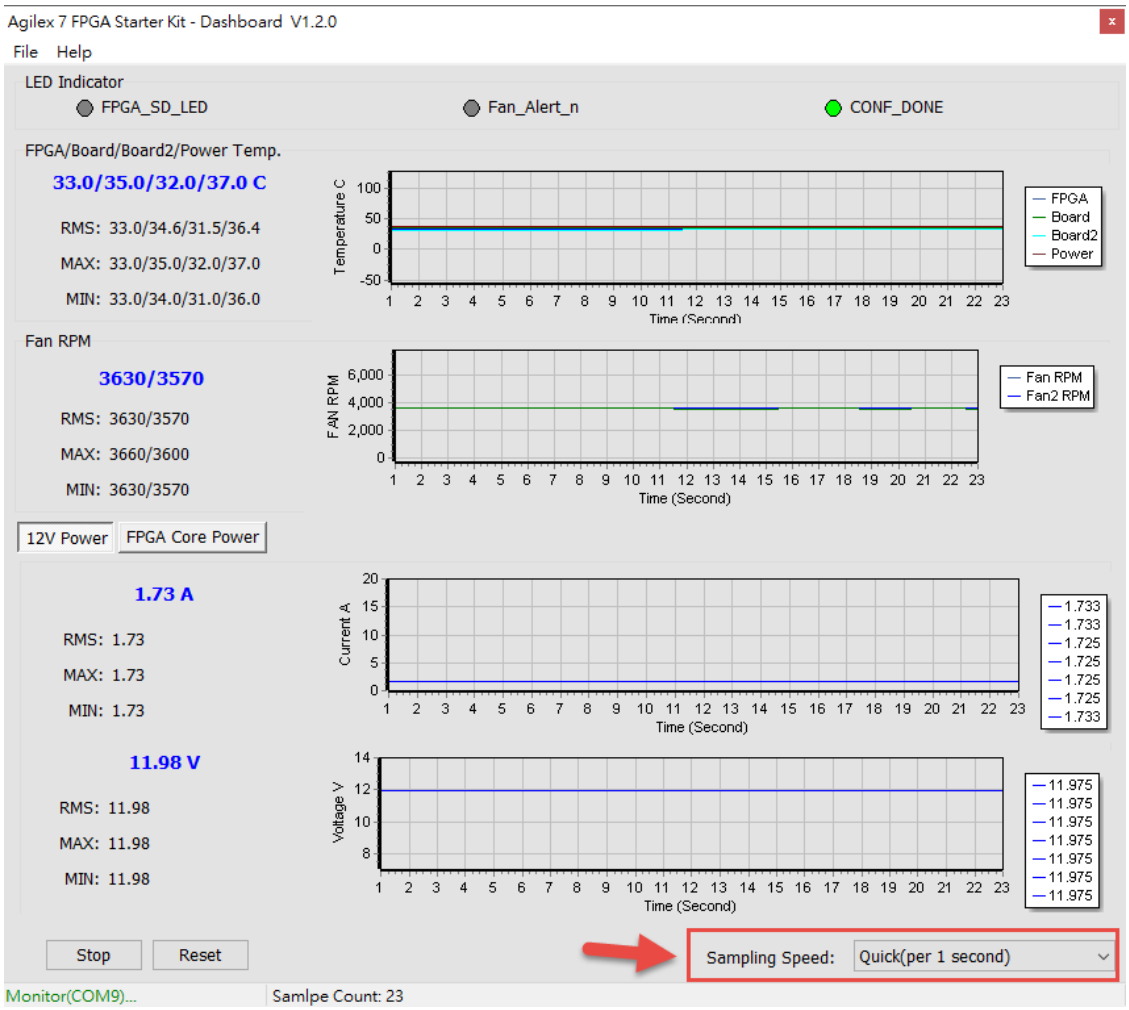


Figure 3-14 Sampling Speed section

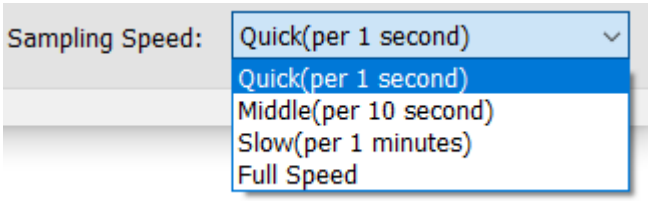


Figure 3-15 Options of Sampling Speed

- **File Manu:** The user can click "**File**" menu at the top left of the GUI (See **Figure 3-16**) and some options such as board information and status export will appear. Note that to active these functions, you will need to **stop** obtaining the board status (i.e. Don't Press "**Start**" button or Press "**Stop**" button) in the GUI. Detailed introductions of these functions are described in below.

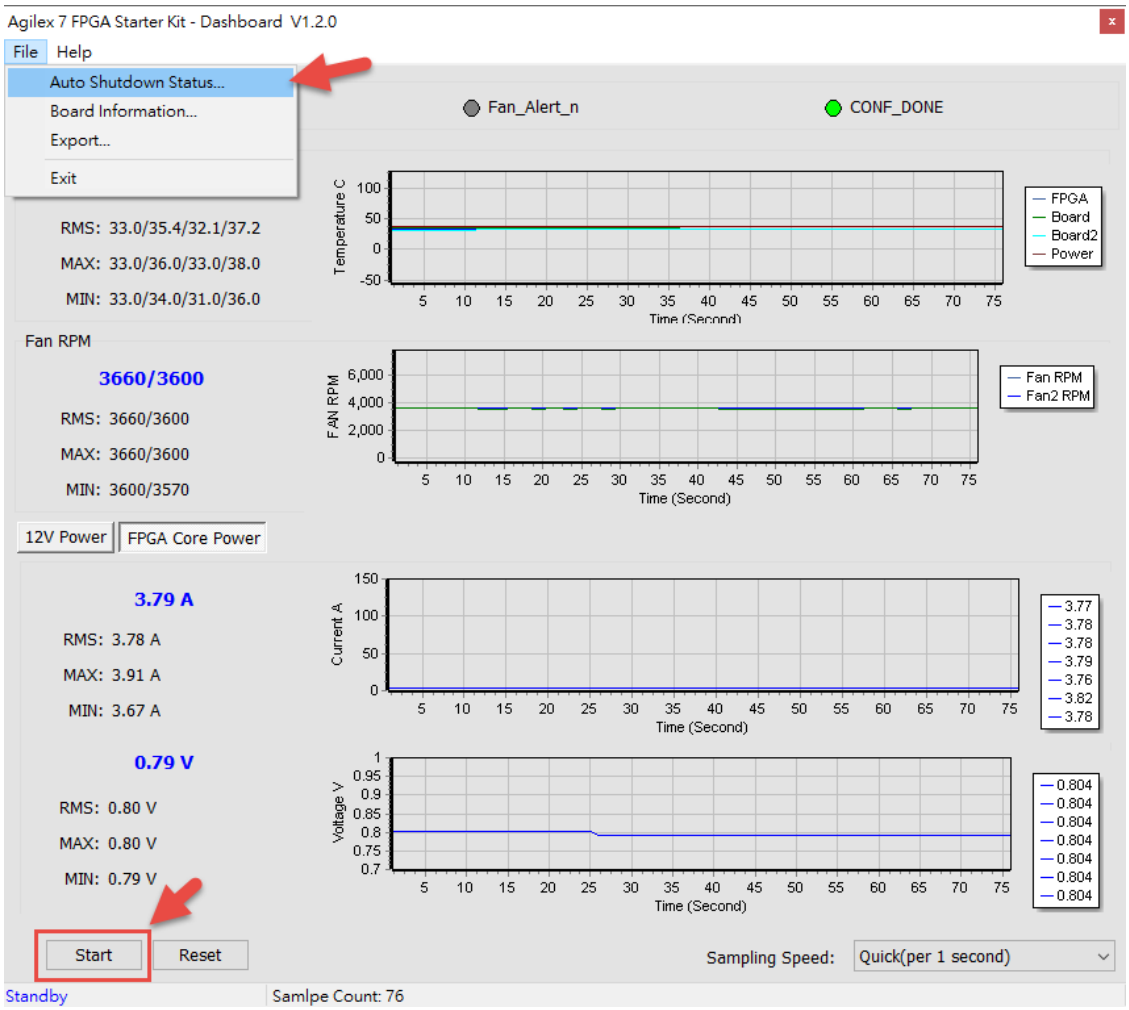


Figure 3-16 File Menu Options

- **Auto Shutdown Status**: This option will report whether the board entered "Auto shutdown status" because the FPGA temperature is too high or the fan speed is abnormal.
- **Board Information**: Click the "Board Information" to get the current MAX 10 FPGA software version and the Agilex 7 FPGA Starter Kit board version, as shown in **Figure 3-17**.

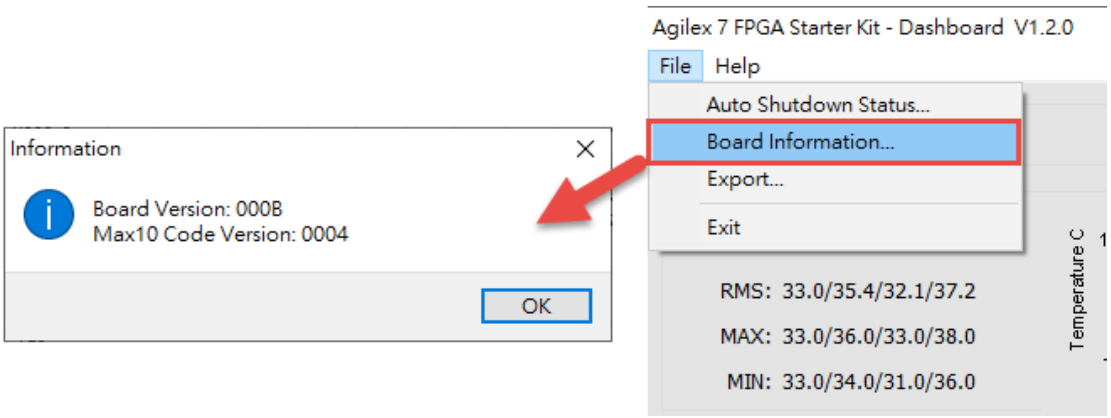


Figure 3-17 Board Information

- **Log File**: Click the Export in the File page to save the board temperature, fan speed and voltage data in .csv format document, as shown in **Figure 3-18** and Figure 3-19.

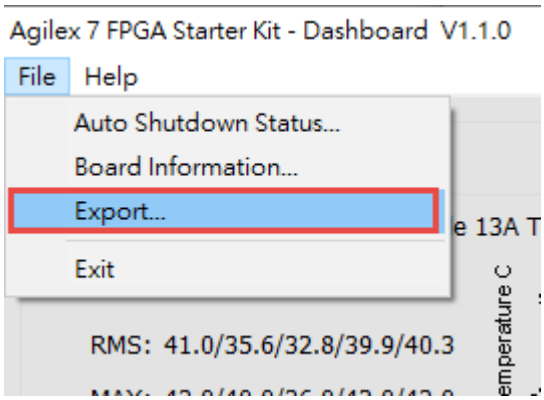


Figure 3-18 Export the log file

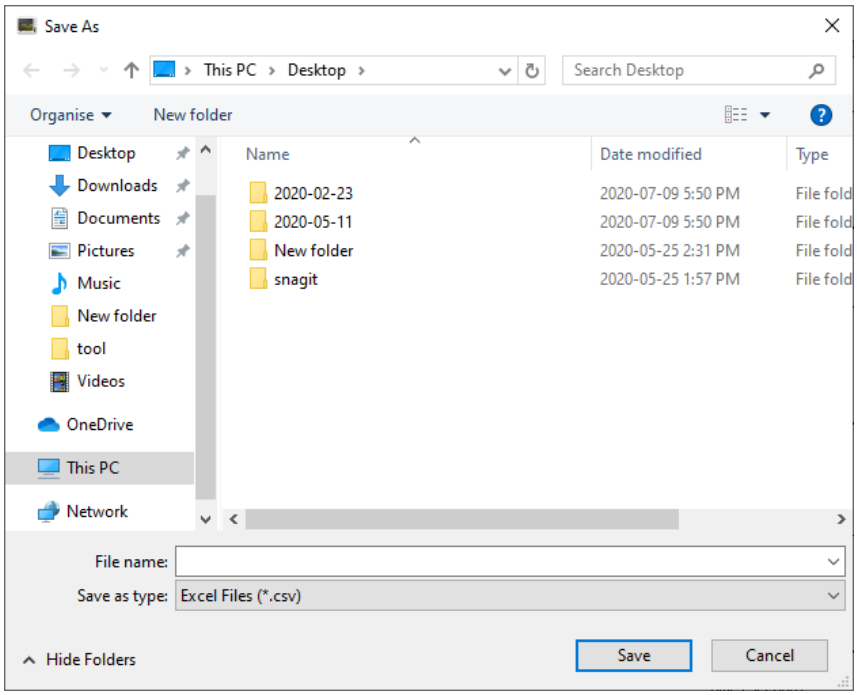


Figure 3-19 Export the log file in .csv format

Chapter 4

Additional Information

4.1 Getting Help

Here are the addresses where you can get help if you encounter problems:

■ Terasic Technologies

No.80, Fenggong Rd., Hukou Township, Hsinchu County 303035. Taiwan
Email: support@terasic.com
Web: www.terasic.com
Agilex 7 FPGA Starter Kit Web: A7SK.terasic.com

■ Revision History

Date	Version	Changes
2023.05	First publication	
2023.08	V1.0	Modify Table2-8

■