Intel Agilex® 7 Device Family Pin Connection Guidelines

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Contents

1. Intel Agilex® 7 Device Family Pin Connection Guidelines

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1.1. Pins Status for Intel Agilex® 7 Devices

The following descriptors designate the status level currently applicable to the relevant variant:

- Preliminary: Information in this document is **subject to change**. Intended for pre-production development, for production designs use with caution.
- Final: Information in this document is intended for use in **production design**.

Table 1. Pins Status for Intel Agilex® 7 Devices

Tile	Status
Core Pins	Final
HPS Pins	Final
E-Tile	Final
P-Tile	Final
F-Tile	Preliminary
R-Tile	Preliminary

1.2. Intel Agilex® 7 FPGA Core Pins

1.2.1. Clock and PLL Pins

Note: Intel® recommends that you create an Intel Quartus® Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 2. Clock and PLL Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
CLK_[T,B]_2[A,B,C,D,E,F]_[0:1][p,n] CLK_[T,B]_3[A,B,C,D,E,F]_[0:1][p,n]	I/O, Clock Input	Dual-purpose I/O pins that can be used for data inputs or outputs. Differential input OCT Rd, single-ended input OCT Rt, and single-ended output OCT Rs are supported on these pins. For more information about the supported pins, refer to the device pin-out file. When you do not use these pins as dedicated clock pins, you can use them as regular I/O pins. Supported I/O standards: • 1.2 V • True Differential Signaling These pins support the programmable pull-up resistor. For more information, refer to the *Intel Agilex® 7 FPGAs and SoCs Device Data Sheet: F-Series and I-Series*.	Tie the unused pins to GND. If the pins are not connected, use the Intel Quartus Prime software programmable options to internally bias these pins. These pins can be reserved as inputs tristate with weak internal pull-up resistor enabled, or as outputs driving GND.
PLL_[2][A,B,C,D,E,F]_[T,B]_FB[0:1] PLL_[3][A,B,C,D,E,F]_[T,B]_FB[0:1]	I/O, Clock Input	Dual-purpose I/O pins that can be used as single-ended inputs, single-ended outputs, or external feedback input pins. For more information about the supported pins, refer to the device pin-out file. Supported I/O standards: • 1.2 V • True Differential Signaling These pins support the programmable pull-up resistor. For more information, refer to the *Intel Agilex 7 FPGAs and SoCs Device Data Sheet: F-Series and I-Series*.	Tie the unused pins to GND. If the pins are not connected, use the Intel Quartus Prime software programmable options to internally bias these pins. These pins can be reserved as inputs tristate with weak internal pull-up resistor enabled, or as outputs driving GND.
PLL_[2][A,B,C,D,E,F]_[T,B]_CLKOUT[0:1][p,n] PLL_[3][A,B,C,D,E,F]_[T,B]_CLKOUT[0:1][p,n]	I/O, Clock Output	I/O pins that can be used as two single-ended clock output pins or one differential clock output pair. For more information about the supported pins, refer to the device pin-out file. Supported I/O standards: • 1.2 V • True Differential Signaling These pins support the programmable pull-up resistor. For more information, refer to the *Intel Agilex 7 FPGAs and SoCs Device Data Sheet: F-Series and I-Series*.	Tie the unused pins to GND. If the pins are not connected, use the Intel Quartus Prime software programmable options to internally bias these pins. These pins can be reserved as inputs tristate with weak internal pull-up resistor enabled, or as outputs driving GND.

Related Information

- Intel Agilex 7 Device Pin-Out Files

- Intel Agilex 7 FPGAs and SoCs Device Data Sheet: F-Series and I-Series

1.2.2. Dedicated Configuration/JTAG Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 3. Dedicated Configuration/JTAG Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
TCK	Input	Dedicated JTAG test clock input pin located in the Secure Device Manager (SDM) bank. This pin can also be used to access the HPS JTAG chain. For more information, refer to the HPS JTAG Pins on page 49. This pin supports the 1.8-V single-ended I/O standard. This pin has an internal 20-kΩ pull-down resistor. JTAG clock speed is 33 MHz for JTAG split mode. In the JTAG split mode, the SDM JTAG mode is independent of the HPS JTAG. JTAG clock speed is 22 MHz for JTAG daisy-chain mode. In the JTAG daisy-chain mode, the HPS DAP TAP is daisy chained with the SDM mTAP.	Connect this pin through a 1-kΩ pull-down resistor to GND. If you plan to use the attestation and/or Black Key Provisioning (BKP) security features, do not connect this pin to GND. Connect this pin to the VCCIO_SDM supply using a 10-kΩ pull-up resistor.
TMS	Input	Dedicated JTAG test mode select input pin located in the SDM bank. This pin can also be used to access the HPS JTAG chain. For more information, refer to the HPS JTAG Pins on page 49. This pin supports the 1.8-V single-ended I/O standard. This pin has an internal 20-kΩ pull-up resistor.	Connect this pin to a 1-kΩ – 10-kΩ pull-up resistor to the VCCIO_SDM supply. If the JTAG interface is not used, connect the TMS pin to the VCCIO_SDM supply using a 1-kΩ resistor.
TDO	Output	Dedicated JTAG test data output pin located in the SDM bank. This pin can also be used to access the HPS JTAG chain. For more information, refer to the HPS JTAG Pins on page 49. This pin supports the 1.8-V single-ended I/O standard.	If the JTAG interface is not used, leave the TDO pin unconnected.
TDI	Input	Dedicated JTAG test data input pin located in the SDM bank. This pin can also be used to access the HPS JTAG chain. For more information, refer to the HPS JTAG Pins on page 49. This pin supports the 1.8-V single-ended I/O standard.	Connect this pin to a 1-kΩ – 10-kΩ pull-up resistor to the VCCIO_SDM supply. If the JTAG interface is not used, connect the TDI pin to the VCCIO_SDM supply using a 1-kΩ resistor.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
		This pin has an internal 20-kΩ pull-up resistor.	
nSTATUS	Output	Configuration status pin. This pin is used for synchronization with the configuration host driving nCONFIG and to report errors. This pin supports the 1.8-V single-ended I/O standard. This pin has an internal 20-kΩ pull-up resistor. The drive strength is 8 mA. ***Attention:*** Ensure that during power up, no external component drives the nSTATUS signal low.	When you are using the Avalon® streaming configuration scheme, connect this pin to the configuration host. For other configuration schemes, you can use this pin to monitor the configuration status. This pin must be pulled up through a 10-kΩ resistor to VCCIO_SDM for all configuration schemes.
nCONFIG	Input	The nCONFIG pin is used to clear the device and prepare for reconfiguration. This pin supports the 1.8-V single-ended I/O standard. This pin has an internal 20-kΩ pull-up resistor.	When you use the Avalon streaming configuration scheme, connect this pin to the configuration host. When you use other configuration schemes, pull this pin to VCCIO_SDM through an external 10-KΩ pull-up resistor. This pin can be used to restart configuration by driving it low and then high again. Ensure that you follow all the requirements for the nCONFIG operation as specified in the *Intel Agilex 7 Configuration User Guide* and *AN 886: Intel Agilex 7 SoC Device Design Guidelines*.
OSC_CLK_1	Input	Reference clock source for SDM PLL. This pin is used as the clock for device configuration and transceiver calibration. This pin supports the 1.8-V single-ended I/O standard. This pin has an internal 20-kΩ pull-down resistor.	You must provide an external clock source to this pin if you are using transceivers. If you choose to use the external clock source for configuration and/or instantiate any transceivers in your design, you must provide a 25-MHz, 100-MHz, or 125-MHz free-running clock source to this pin and enable it in the Intel Quartus Prime software when you compile your design. If you are using the internal oscillator for configuration and do not instantiate any transceivers in your design, leave this pin unconnected.

Related Information

- AN 886: Intel Agilex 7 SoC Device Design Guidelines
- Intel Agilex 7 Configuration User Guide Configuration User Guide

1.2.3. Optional/Dual-Purpose Configuration Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Attention: There are pins usage restriction for the dual-purpose pins in the Avalon-ST x16 and x32 modes. For more information, refer to section 2.5.3.2. *Enabling Dual-Purpose Pins* in the *Intel Agilex 7 Configuration User Guide*.

Table 4. Optional/Dual-Purpose Configuration Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
AVST_DATA[31:0]	I/O, Input	Dual-purpose configuration data input pins. Use AVST_DATA[15:0] pins for Avalon Streaming Interface (Avalon-ST) x16 mode, AVST_DATA [31:0] pins for Avalon-ST x32 mode, or as regular I/O pins. This pin supports the 1.2-V LVCMOS I/O standard. These pins support the programmable pull-up resistor. For more information, refer to the *Intel Agilex 7 FPGAs and SoCs Device Data Sheet: F-Series and I-Series* . ***Attention:*** Access to the I/O pins located in bank 3A with pin index[91...95] is not allowed for the AvSTx16 or AvSTx32 configuration scheme. You must leave these pins unconnected. For more information, refer to the device pin mapping files to identify the exact pin location.	If these pins are not used as the dual-purpose pins and they are not used as I/O pins, leave these pins unconnected.
AVST_READY(3A bank)	I/O, Output	Dual-purpose Avalon-ST interface data ready output pin. This pin is used for the Avalon-ST x16 and x32 configuration schemes. This pin cannot be used as a user I/O pin if you are using the AvST x16 or AvST x32 configuration scheme. This pin supports the 1.2-V LVCMOS I/O standard. These pins support the programmable pull-up resistor. For more information, refer to the *Intel Agilex 7 FPGAs and SoCs Device Data Sheet: F-Series and I-Series* .	Connect this pin to the ready signal input of the external configuration controller when configuring using the Avalon-ST x16 or x32 interface.
AVST_CLK(3A bank)	I/O, Input	Dual-purpose Avalon-ST interface clock input pin. This pin is used for the Avalon-ST x16 and x32 configuration schemes.	Connect this pin to the clock signal of the external configuration controller when configuring using the Avalon-ST x16 or x32 interface.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
		This pin can also be used as a user I/O pin after configuration. This pin supports the 1.2-V LVCMOS I/O standard. These pins support the programmable pull-up resistor. For more information, refer to the *Intel Agilex 7 FPGAs and SoCs Device Data Sheet: F-Series and I-Series* .	Connect unused pins as defined in the Intel Quartus Prime software.
AVST_VALID(3A bank)	I/O, Input	Dual-purpose configuration data valid pin. This pin is used for the Avalon-ST x16 and x32 configuration schemes. This pin can also be used as a user I/O pin after configuration. This pin supports the 1.2-V LVCMOS I/O standard. These pins support the programmable pull-up resistor. For more information, refer to the *Intel Agilex 7 FPGAs and SoCs Device Data Sheet: F-Series and I-Series* .	Connect this pin to the data valid signal of the external configuration controller when configuring using the Avalon-ST x16 or x32 interface. Connect unused pins as defined in the Intel Quartus Prime software.

1.2.4. Differential I/O Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 5. Differential I/O Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
DIFF_RX[2][A,B,C,D,E,F][1:24][p,n] DIFF_RX[3][A,B,C,D,E,F][1:24][p,n]	I/O, RX channel	These are SERDES receiver channels on GPIO banks. If these pins are not used in SERDES implementation, these pins are available as user I/O pins. Supported I/O standards: • 1.5-V I/O standard for true differential I/O • 1.2-V I/O standard for single-ended voltage referenced and non-voltage referenced I/O • 1.2-V I/O standard for differential voltage referenced I/O These pins support the programmable pull-up resistor. For more information, refer to the *Intel Agilex 7 FPGAs and SoCs Device Data Sheet: F-Series and I-Series*.	Connect unused pins as defined in the Intel Quartus Prime software.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
		For more information about the supported pins, refer to the device pin-out file.	
DIFF_TX[2][A,B,C,D,E,F][1:24][p,n] DIFF_TX[3][A,B,C,D,E,F][1:24][p,n]	I/O, TX channel	These are SERDES transmitter channels on GPIO banks. If these pins are not used in SERDES implementation, these pins are available as user I/O pins. Supported I/O standards: • 1.5-V I/O standard for true differential I/O • 1.2-V I/O standard for single-ended voltage referenced and non-voltage referenced I/O • 1.2-V I/O standard for differential voltage referenced I/O These pins support the programmable pull-up resistor. For more information, refer to the *Intel Agilex 7 FPGAs and SoCs Device Data Sheet: F-Series and I-Series*. For more information about the supported pins, refer to the device pin-out file.	Connect unused pins as defined in the Intel Quartus Prime software.

1.2.5. External Memory Interface Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 6. External Memory Interface Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
DQS[0:63]	I/O, bidirectional	Optional data strobe signal for use in external memory interfacing. These pins drive to the dedicated DQS phase shift circuitry. Supported I/O standards: • POD 1.2-V I/O standard • SSTL 1.2-V I/O standard	Connect unused pins as defined in the Intel Quartus Prime software.
DQSn[0:63]	I/O, bidirectional	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to the dedicated DQS phase shift circuitry.	Connect unused pins as defined in the Intel Quartus Prime software.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
		Supported I/O standards: • POD 1.2-V I/O standard • SSTL 1.2-V I/O standard	
DQ[0:63]	I/O, bidirectional	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important. However, if you plan on migrating to a different memory interface that has a different DQ bus width, you need to reevaluate your pin assignments. Analyze the available DQ pins across all pertinent DQS columns in the device pin-out file. Supported I/O standards: • POD 1.2-V I/O standard • SSTL 1.2-V I/O standard	Connect unused pins as defined in the Intel Quartus Prime software.

Related Information

External Memory Interface Pin Information for Intel Agilex 7 Devices

1.2.6. Voltage Sensor and Voltage Reference Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 7. Voltage Sensor and Voltage Reference Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
VREFP_ADC	Input	Dedicated precision analog voltage reference.	Tie these pins to GND.
VREFN_ADC	Input		
VSIGP_[0,1]	Input	Analog differential inputs pins used with the voltage sensor inside the FPGA to monitor external analog voltages.	Tie these pins to GND if you do not use the voltage sensor feature. For more information on the usage of these pins, refer to the *Intel Agilex 7 Power Management User Guide*. Do not drive the VSIGP and VSIGN pins until the VCCADC power rail has reached 1.62 V to prevent damage.
VSIGN_[0,1]	Input		

1.2.7. Remote Temperature Sensing Diode Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 8. Remote Temperature Sensing Diode Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
`TEMPDIODE0[A,C][p,n]`	Input	These pins connect to the internal temperature sensing diodes in the FPGA core and corner areas of the FPGA.	Connect these pins to an external temperature sensing device to allow sensing of the FPGA's temperature. If you do not use the temperature sensing diode with an external temperature sensing device, leave these pins unconnected. For more information about the locations and channel numbers of the temperature sensors, refer to the sensor monitoring system chapter in the *Intel Agilex 7 Power Management User Guide*.
`TEMPDIODE[1,3,4,6][P,N]`	Input	These pins connect to the internal temperature sensing diodes in the E-tile, P-tile, R-tile, and F-tile transceivers. For more information about the supported pins, refer to the device pin-out file.	Connect these pins to an external temperature sensing device to allow sensing of the E-tile, P-tile, R-tile, and F-tile temperature. If you do not use the temperature sensing diode with an external temperature sensing device, leave these pins unconnected. For more information about the locations and channel numbers of the temperature sensors, refer to the sensor monitoring system chapter in the *Intel Agilex 7 Power Management User Guide*.

Related Information

Intel Agilex 7 Power Management User Guide

1.2.8. Reference Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 9. Reference Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
RZQ_[T,B]_2[A,B,C,D,E,F] RZQ_[T,B]_3[A,B,C,D,E,F]	I/O, bidirectional	Reference pins for I/O banks. The RZQ pins share the same VCCIO_PIO with the I/O bank where they are located. Connect the external precision resistor to the designated pin within the bank. If not required, this pin is a regular I/O pin. These pins support 1.2-V I/O standard. These pins support the programmable pull-up resistor. For more information, refer to the *Intel Agilex 7 FPGAs and SoCs Device Data Sheet: F-Series and I-Series*. For more information about the supported pins, refer to the device pin-out file.	When using OCT, tie these pins to GND through a 240-Ω resistor. When you do not use these pins as dedicated input for the external precision resistor or as I/O pins, leave these pins unconnected.

1.2.9. No Connect and DNU Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 10. No Connect and DNU Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
DNU	Do Not Use	Do Not Use (DNU).	Do not connect to power, GND, or any other signal. These pins must be left floating.
NC	No Connect	Do not drive signals into these pins.	When designing for device migration, you have the option to connect these pins to either power, GND, or a signal trace depending on the pin assignment of the devices selected for migration. However, if device migration is not a concern, leave these pins floating.

1.2.10. Power Supply Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Note: Intel recommends you to generate a **.pin** file from the Intel Quartus Prime Fitter to verify power pin assignment. Intel also recommends using this **.pin** file to determine if it is safe to power down or ground certain power supplies for your specific design. This step will inform you to make the appropriate design choices for unused power supplies for your design.

Table 11. Power Supply Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
VCCP	Power	VCCP supplies power to the periphery.	VCC and VCCP must operate at the same voltage level, should share the same power plane on the board, and be sourced from the same regulator. For details about the recommended operating conditions, refer to the *Electrical Characteristics* section in the *Intel Agilex 7 FPGAs and SoCs Device Data Sheet: F-Series and I-Series*. Use the Intel FPGA Power and Thermal Calculator and the Intel Quartus Prime Power Analyzer to determine the current requirements for VCCP and other power supplies. Decoupling for these pins depends on the decoupling requirements of the specific board.
VCC	Power	VCC supplies power to the core.	VCC and VCCP must operate at the same voltage level, should share the same power plane on the board, and be sourced from the same regulator. For details about the recommended operating conditions, refer to the *Electrical Characteristics* section in the *Intel Agilex 7 FPGAs and SoCs Device Data Sheet: F-Series and I-Series*. Use the Intel FPGA Power and Thermal Calculator and the Intel Quartus Prime Power Analyzer to determine the current requirements for VCC and other power supplies. Decoupling for these pins depends on the decoupling requirements of the specific board.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
VCCPT	Power	Power supply for the IOPLL, programmable power technology, and I/O pre-drivers.	Connect VCCPT to a 1.8-V low noise switching regulator. You have the option to source the following from the same regulator as VCCPT: • VCCPLL_SDM, VCCPLL_HPS, and VCCADC with proper isolation filtering Voltage spike ringing may be observed on VCCPT during device power-down sequencing if VCC is powered down before VCCPT, with the magnitude of the voltage spike ringing higher than VCCPT. This is the expected behavior and will neither cause any functional failure nor reliability concerns to the device. For more details about the decoupling recommendations for this voltage rail, refer to the *AN 910: Intel Agilex 7 Power Distribution Network Design Guidelines*. For the power rail sharing, refer to the *Power Supply Sharing Guidelines for Intel Agilex 7 Devices*.
VCCRCORE	Power	CRAM power supply. For use in Intel Agilex 7 production devices only (placed here for migration purposes).	Connect the VCCRCORE to 1.2-V power supply. You have the option to source VCCRCORE from the same regulator as VCCIO_PIO when VCCIO_PIO is connected to 1.2 V.
VCCH	Power	Analog Interface Bridge (AIB) and digital transceiver power supply.	Connect all VCCH pins to a 0.9-V low noise switching power supply for Intel Agilex 7 devices with E-tile and P-tile. Connect all VCCH pins to a 0.8-V low noise switching power supply for Intel Agilex 7 devices with F-tile or R-tile. For more details, refer to the *Intel Agilex 7 FPGAs and SoCs Device Data Sheet: F-Series and I-Series*.
VCCH_SDM	Power	Voltage rail sense.	Must connect this sense to the VCCH rail for the Intel Agilex 7 devices with E-tile and P-tile. Must connect this sense to the VCC_HSSI_GXR rail for the Intel Agilex 7 devices with both F-tile and R-tile. Must connect this sense to the VCCH rail for the Intel Agilex 7 device with F-tile only.
VCCA_PLL	Power	I/O clock network power supply.	For Intel Agilex 7 production devices and other Intel Agilex 7 ES (except 2486A package) devices, connect VCCA_PLL to a 1.2-V low noise switching regulator. You have the option to source VCCA_PLL from the same regulator as VCCIO_PIO with proper isolation filtering. The VCCA_PLL rail must reside in Group 3 power rails.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
VCCIO_PIO[2][A,B,C,D,E,F] VCCIO_PIO[3][A,B,C,D,E,F]	Power	These are the supply voltage pins for the I/O banks. Each bank can support a different voltage level. Supported VCCIO standards include the following: • 1.2-V LVCMOS • SSTL12/Diff SSTL12 • HSTL12/ Diff HSTL12 • HSUL12/ Diff HSUL12 • POD12/ Diff POD12 • True Differential Signaling For more information about the supported pins, refer to the device pin-out file.	Connect these pins to a 1.2-V or 1.5-V power supplies, depending on the I/O standard required by the specific bank. Connect the unused I/O bank power to 1.2V or 1.5V if the I/O bank will be used in future. Connect unused I/O bank power to GND and I/O pins floating if the I/O bank will not be used in future. Do not leave the VCCIO_PIO floating. If VCCIO_PIO_3A is tied to GND, connect VCCIO_PIO_SDM to VCCRCORE. During the power-up sequence only, a transient current whose magnitude is less than the VCCIO_PIO operating static current may be observed as the VCCIO_PIO transistors become operational. This is the expected behavior and will neither cause any functional failure nor reliability concerns to the device if the power-up or power-down sequence is followed. For more details, refer to the sensor monitoring system chapter in the *Intel Agilex 7 Power Management User Guide*. For the power rail sharing, refer to the *Power Supply Sharing Guidelines for Intel Agilex 7 Devices*.
VCCIO_PIO_SDM	Power	VCCIO_PIO voltage rail sense line.	Connect these pins to bank VCCIO_PIO_3A. You must supply 1.2 V to VCCIO_PIO_3A if you are using AVST x16 or AVST x32 mode.
VCCIO_SDM	Power	Configuration pins power supply.	Connect these pins to a 1.8-V power supply. For more details about the decoupling recommendations for this voltage rail, refer to the *AN 910: Intel Agilex 7 Power Distribution Network Design Guidelines*. For the power rail sharing, refer to the *Power Supply Sharing Guidelines for Intel Agilex 7 Devices*.
VCCPLLDIG_SDM	Power	SDM block PLL power pins.	VCCPLLDIG_SDM must be sourced from the same regulator as VCCL_SDM with proper isolation filtering.
VCCL_SDM	Power	SDM power supply.	Connect these pins to a 0.8-V power supply.
VCCBAT	Power	Battery back-up power supply for device security Advanced Encryption Standard, Battery-backed RAM (AES BBRAM) key register.	When using the device security AES BBRAM key, connect this pin to a non-volatile battery power source in the range of 1.0 V – 1.8 V. A series RC (R=10 kΩ, C=1µF) circuit must be added to the VCCBAT rail. Connect a 10 kΩ resistor in series between the battery power source and VCCBAT. You must also connect a 1µF capacitor between VCCBAT and ground.

continued...

Pin Name	Pin Functions	Pin Description	Connection Guidelines
			For more information about the schematic diagram, refer to *AN 910: Intel Agilex 7 Power Distribution Network Design Guidelines*. Provide a minimum decoupling of 47 nF for the VCCBAT power rail near the VCCBAT pin. When not using the AES BBRAM key, tie this pin to ground.
VCCPLL_SDM	Power	VCCPLL_SDM supplies analog power to the SDM block PLLs.	With proper isolation filtering, you have the option to source VCCPLL_SDM from the same regulator as VCCPT. Decoupling for these pins depends on the design decoupling requirements of the specific board.
GND	Ground	Device ground pins.	Connect all GND pins to the board ground plane.
VREFB[2] [AN0,BN0,CN0,DN0,EN0,FN0] VREFB[3] [AN0,BN0,CN0,DN0,EN0,FN0]	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then use these pins as voltage-reference pins for the bank. For more information about the supported pins, refer to the device pin-out file.	If VREF pins are not used, connect them to GND.
VCCLSENSE	Output	Differential sense line to external regulator.	VCCLSENSE and GNDSENSE are differential remote sense pins for the VCC power. Connect your regulators' differential remote sense lines to the respective VCCLSENSE and GNDSENSE pins. This compensates for the DC IR drop associated with the PCB and device package from the VCC power. Route these connections as differential pair traces and keep them isolated from any other noise source. You must connect the VCCLSENSE and GNDSENSE lines to the regulator's remote sense inputs.
GNDSENSE			
VCCADC	Power	ADC power pin for the voltage sensors.	You must supply a low noise 1.8-V power supply to this pin if you are using the internal voltage sensors of the Intel Agilex 7 device. Tie this pin to VCCPT with proper isolation filtering.
VCCFUSEWR_SDM	Power	The required power supply to program (write) the optional, one-time programmable eFuses. These eFuses are an integral part of the Intel Agilex 7 security architecture.	Connect this pin to 1.8V. The capability of the low-dropout (LDO) regulator should be ≥1 A.

Related Information

- Intel Agilex 7 Power Management User Guide
- Intel Agilex 7 FPGAs and SoCs Device Data Sheet: F-Series and I-Series

- AN 910: Intel Agilex 7 Power Distribution Network Design Guidelines

1.2.11. Secure Device Manager (SDM) Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 12. SDM Pins

Pin Name	Pin Description	MSEL[2:0]	Pin Functions	Connection Guidelines
RREF_SDM	Reference resistor input for the PLLs of the SDM interface.	—	Input to read reference resistance	Connect a 2-kΩ +/-1% resistor to GND.
SDM_IO0	This pin is pulled low internally by a 20-kΩ resistor when the device is powered up.	Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the Secure Device Manager (SDM) Optional Signal Pins on page 24.
SDM_IO1	This pin is pulled high internally by a 20-kΩ resistor when the device is powered up. This pin functions differently depending on the configuration scheme used by setting the MSEL pins.	3'b110	AVSTx8_DATA2	Connect this pin to the data2 pin of an external configuration controller when configuring using the Avalon-ST x8 interface.
		3'b001 or 3'b011	AS_DATA1	Connect this pin to the data1 pin of the QSPI flash device when configuring from the QSPI flash device.
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the Secure Device Manager (SDM) Optional Signal Pins on page 24.
SDM_IO2	This pin is pulled high internally by a 20-kΩ resistor when the device is powered up. This pin functions differently depending on the configuration scheme used by setting the MSEL pins.	3'b110	AVSTx8_DATA0	Connect this pin to the data0 pin of an external configuration controller when configuring using the Avalon-ST x8 interface.
		3'b001 or 3'b011	AS_CLK	Connect this pin to the clock input of the QSPI flash device when configuring from the QSPI flash device.

continued...

Pin Name	Pin Description	MSEL[2:0]	Pin Functions	Connection Guidelines
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the Secure Device Manager (SDM) Optional Signal Pins on page 24.
SDM_IO3	This pin is pulled high internally by a 20-kΩ resistor when the device is powered up. This pin functions differently depending on the configuration scheme used by setting the MSEL pins.	3'b110	AVSTx8_DATA3	Connect this pin to the data3 pin of an external configuration controller when configuring using the Avalon-ST x8 interface.
		3'b001 or 3'b011	AS_DATA2	Connect this pin to the data2 pin of the QSPI flash device when configuring from the QSPI flash device.
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the Secure Device Manager (SDM) Optional Signal Pins on page 24.
SDM_IO4	This pin is pulled high internally by a 20-kΩ resistor when the device is powered up. This pin functions differently depending on the configuration scheme used by setting the MSEL pins.	3'b110	AVSTx8_DATA1	Connect this pin to the data1 pin of an external configuration controller when configuring using the Avalon-ST x8 interface.
		3'b001 or 3'b011	AS_DATA0	Connect this pin to the data0 pin of the QSPI flash device when configuring from the QSPI flash device.
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the Secure Device Manager (SDM) Optional Signal Pins on page 24.
SDM_IO5	This pin is pulled high internally by a 20-kΩ resistor when the device is powered up. This pin will function as MSEL[0] during power up and reset to determine the configuration scheme. Once the pin completes the MSEL function, it will then function according to the configuration scheme you have selected.	—	MSEL[0]	This pin needs to be pulled-up to VCCIO_SDM or pulled-down to GND through a 4.7-kΩ resistor depending on your configuration scheme.
		3'b001 or 3'b011	AS_nCSO0	Connect this pin to the nCS input of the first QSPI flash device when configuring from QSPI flash devices.

continued...

Pin Name	Pin Description	MSEL[2:0]	Pin Functions	Connection Guidelines
	For more information, refer to the *Intel Agilex 7 Configuration User Guide*.	Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the Secure Device Manager (SDM) Optional Signal Pins on page 24.
SDM_IO6	This pin is pulled high internally by a 20-kΩ resistor when the device is powered up. This pin functions differently depending on the configuration scheme used by setting the MSEL pins.	3'b110	AVSTx8_DATA4	Connect this pin to the data4 pin of an external configuration controller when configuring using the Avalon-ST x8 interface.
		3'b001 or 3'b011	AS_DATA3	Connect this pin to the data3 pin of the QSPI flash device when configuring from the QSPI flash device.
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the Secure Device Manager (SDM) Optional Signal Pins on page 24.
SDM_IO7	This pin is pulled high internally by a 20-kΩ resistor when the device is powered up. This pin will function as MSEL[1] during power up to determine the configuration scheme. Once the pin completes the MSEL function, it will then function according to the configuration scheme you have selected. For more information, refer to the *Intel Agilex 7 Configuration User Guide*.	—	MSEL[1]	This pin needs to be pulled-up to VCCIO_SDM or pulled-down to GND through a 4.7-kΩ resistor depending on your configuration scheme.
		3'b001 or 3'b011	AS_nCSO2	Connect this pin to the nCS input of the third QSPI flash device when you use cascaded QSPI flash devices for HPS application.
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the Secure Device Manager (SDM) Optional Signal Pins on page 24.
SDM_IO8	This pin is pulled low internally by a 20-kΩ resistor when the device is powered up. This pin functions differently depending on the configuration scheme used by setting the MSEL pins.	3'b110	AVSTx8_READY	Connect this pin to the ready signal output of the external configuration controller when configuring using the Avalon-ST x8 interface.
		3'b001 or 3'b011	AS_nCSO3	Connect this pin to the nCS input of the fourth QSPI flash device when you use cascaded QSPI flash devices for HPS application.

continued...

Pin Name	Pin Description	MSEL[2:0]	Pin Functions	Connection Guidelines
				Connect with a 1-kΩ pull-up resistor to VCCIO_SDM.
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the Secure Device Manager (SDM) Optional Signal Pins on page 24.
SDM_IO9	This pin is pulled high internally by a 20-kΩ resistor when the device is powered up. This pin will function as MSEL[2] during power up to determine the configuration scheme. Once the pin completes the MSEL function, it will then function according to the configuration scheme you have selected. For more information, refer to the *Intel Agilex 7 Configuration User Guide*.	—	MSEL[2]	This pin needs to be pulled-up to VCCIO_SDM or pulled-down to GND through a 4.7-kΩ resistor depending on your configuration scheme.
		3'b001 or 3'b011	AS_nCSO1	Connect this pin to the nCS input of the second QSPI flash device when you use cascaded QSPI flash devices for HPS application.
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the Secure Device Manager (SDM) Optional Signal Pins on page 24.
SDM_IO10	This pin is pulled high internally by a 20-kΩ resistor when the device is powered up. This pin functions differently depending on the configuration scheme used by setting the MSEL pins.	3'b110	AVSTx8_DATA7	Connect this pin to the data7 pin of an external configuration controller when configuring using the Avalon-ST x8 interface.
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the Secure Device Manager (SDM) Optional Signal Pins on page 24.
SDM_IO11	This pin is pulled high internally by a 20-kΩ resistor when the device is powered up. This pin functions differently depending on the configuration scheme used by setting the MSEL pins.	3'b110	AVSTx8_VALID	Connect this pin to the data valid pin of an external configuration controller when configuring using the Avalon-ST x8 interface.
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the Secure Device Manager (SDM) Optional Signal Pins on page 24.

continued...

Pin Name	Pin Description	MSEL[2:0]	Pin Functions	Connection Guidelines
SDM_IO12	This pin is pulled high internally by a 20-kΩ resistor when the device is powered up.	—	Any MSEL setting	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the Secure Device Manager (SDM) Optional Signal Pins on page 24.
SDM_IO13	This pin is pulled high internally by a 20-kΩ resistor when the device is powered up. This pin functions differently depending on the configuration scheme used by setting the MSEL pins.	3'b110	AVSTx8_DATA5	Connect this pin to the data5 pin of an external configuration controller when configuring using the Avalon-ST x8 interface.
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the Secure Device Manager (SDM) Optional Signal Pins on page 24.
SDM_IO14	This pin is pulled high internally by a 20-kΩ resistor when the device is powered up. This pin functions differently depending on the configuration scheme used by setting the MSEL pins.	3'b110	AVSTx8_CLK	Connect this pin to the clock output of an external configuration controller when configuring using the Avalon-ST x8 interface.
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the Secure Device Manager (SDM) Optional Signal Pins on page 24.
SDM_IO15	This pin is pulled high internally by a 20-kΩ resistor when the device is powered up. This pin functions differently depending on the configuration scheme used by setting the MSEL pins.	3'b110	AVSTx8_DATA6	Connect this pin to the data6 pin of an external configuration controller when configuring using the Avalon-ST x8 interface.
		3'b001 or 3'b011	AS_nRST	Connect this pin to the reset pin of the QSPI flash device when configuring from the QSPI flash device.
		Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the Secure Device Manager (SDM) Optional Signal Pins on page 24.
SDM_IO16	This pin is pulled low internally by a 20-kΩ resistor when the device is powered up.	Any valid MSEL setting	Optional signals	The connection guidelines for this pin has dependency on signal assignments. For more information, refer to the Secure Device Manager (SDM) Optional Signal Pins on page 24.

1.2.12. Secure Device Manager (SDM) Optional Signal Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 13. SDM Optional Signal Pins

Signal Name	Signal Description	Connection Guidelines	Configuration Schemes			
			ASx4	AVSTx8	AVSTx16	AVSTx32
PWRMGT_SCL	PMBus Power Management Clock. This pin is used as the clock pin for the PMBus interface.	This pin requires a pull-up resistor to the 1.8-V VCCIO_SDM supply. Intel recommends a pull-up value of 5.1-kΩ to 10-kΩ depending on the loading of this pin. Use the voltage level translators when interfacing to the PMBus interfaces requiring voltages other than 1.8 V. Connect this pin to the PMBus clock pin of your regulator. When a –V or –E power option device is used, you must enable the SmartVID connection between the device and the VCC voltage regulator to allow the FPGA to directly control its core voltage requirements. You can do this by connecting the PWRMGT_SCL and PWRMGT_SDA signals to the VCC voltage regulator for the PMBus master mode and the PWRMGT_SCL, PWRMGT_SDA, and PWRMGT_ALERT signals to the external master controller for the PMBus slave mode.	SDM_IO0 SDM_IO14	SDM_IO0	SDM_IO0 SDM_IO14	SDM_IO0 SDM_IO14

continued...

Signal Name	Signal Description	Connection Guidelines	Configuration Schemes			
			ASx4	AVSTx8	AVSTx16	AVSTx32
		Note: Intel recommends holding the voltage level translators disabled by default to ensure that bus contention, excessive currents, or oscillations do not occur during FPGA rails ramp up or down.				
PWRMGT_SDA	PMBus Power Management Serial Data. This pin is used as the data pin for the PMBus interface.	This pin requires a pull-up resistor to the 1.8-V VCCIO_SDM supply. Intel recommends a pull-up value of 5.1-kΩ to 10-kΩ depending on the loading of this pin. Use the voltage level translators when interfacing to the PMBus interfaces requiring voltages other than 1.8V. Connect this pin to the PMBus data pin of your regulator. When a –V or –E power option device is used, you must enable the SmartVID connection between the device and the VCC voltage regulator to allow the FPGA to directly control its core voltage requirements. You can do this by connecting the PWRMGT_SCL and PWRMGT_SDA signals to the VCC voltage regulator for the PMBus master mode and the PWRMGT_SCL, PWRMGT_SDA, and PWRMGT_ALERT signals to the external master controller for the PMBus slave mode.	SDM_IO11 SDM_IO12 SDM_IO16	SDM_IO12 SDM_IO16	SDM_IO11 SDM_IO12 SDM_IO16	SDM_IO11 SDM_IO12 SDM_IO16

continued...

Signal Name	Signal Description	Connection Guidelines	Configuration Schemes			
			ASx4	AVSTx8	AVSTx16	AVSTx32
		Note: Intel recommends holding the voltage level translators disabled by default to ensure that bus contention, excessive currents, or oscillations do not occur during FPGA rails ramp up or down.				
PWRMGT_ALERT	PMBus Power Management Alert. This pin is used as the ALERT function for the PMBus interface when the Intel Agilex 7 –V or –E power option device is the PMBus slave.	This pin requires a pull-up resistor to the 1.8-V VCCIO_SDM supply. Intel recommends a pull-up value of 5.1-kΩ to 10-kΩ depending on the loading of this pin. Use the voltage level translators when interfacing to the PMBus interfaces requiring voltages other than 1.8 V. Connect this pin to the PMBus ALERT pin of the external master controller. When using the SmartVID feature with the Intel Agilex 7 –V or –E power option device as a PMBus slave, you must connect the PWRMGT_ALERT signal along with the PWRMGT_SCL and PWRMGT_SDA signals to the PMBus master device to complete the SmartVID power management interface. The PMBus master device reads the VID codes from the Intel Agilex 7 slave and programs the voltage regulator to output the correct VID voltage.	SDM_IO0 SDM_IO12	SDM_IO0 SDM_IO9 SDM_IO12	SDM_IO0 SDM_IO9 SDM_IO12	SDM_IO0 SDM_IO12

continued...

Signal Name	Signal Description	Connection Guidelines	Configuration Schemes			
			ASx4	AVSTx8	AVSTx16	AVSTx32
		Note: Intel recommends holding the voltage level translators disabled by default to ensure that bus contention, excessive currents, or oscillations do not occur during FPGA rails ramp up or down.				
CONF_DONE	The CONF_DONE pin indicates all configuration data has been received.	By default, Intel recommends using the SDM_IO16 pin to implement the CONF_DONE function. If SDM_IO16 is unavailable, the CONF_DONE function can also be implemented using any unused SDM_IO pins. Except for SDM_IO0 and SDM_IO16, other SDM_IO pins are required to connect to an external 4.7-kΩ pull-down resistor for the CONF_DONE signal. Connect the CONF_DONE pin to the external configuration controller when configuring using the Avalon-ST (AVST) interface. You have an option to monitor this signal with an external component if you are using the active serial (AS) x4 configuration scheme.	SDM_IO0 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO16	SDM_IO0 SDM_IO5 SDM_IO12 SDM_IO16	SDM_IO0 SDM_IO1 SDM_IO2 SDM_IO3 SDM_IO4 SDM_IO6 SDM_IO7 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO15 SDM_IO16	SDM_IO0 SDM_IO1 SDM_IO2 SDM_IO3 SDM_IO4 SDM_IO5 SDM_IO6 SDM_IO7 SDM_IO8 SDM_IO9 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO15 SDM_IO16
INIT_DONE	The INIT_DONE pin indicates the device has enter user mode upon completion of configuration. When used for this purpose, this pin must be enabled by the Intel Quartus Prime software.	Intel recommends you to use SDM_IO0 or SDM_IO16 to implement the INIT_DONE function when available as it has an internal weak pull-down for the correct function of INIT_DONE during power up.	SDM_IO0 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO16	SDM_IO0 SDM_IO5 SDM_IO12 SDM_IO16	SDM_IO0 SDM_IO1 SDM_IO2 SDM_IO3 SDM_IO4 SDM_IO6 SDM_IO7	SDM_IO0 SDM_IO1 SDM_IO2 SDM_IO3 SDM_IO4 SDM_IO5 SDM_IO6

continued...

Signal Name	Signal Description	Connection Guidelines	Configuration Schemes			
			ASx4	AVSTx8	AVSTx16	AVSTx32
	When the INIT_DONE function is enabled, this pin will drive high when configuration is completed and the device goes into user mode.	If SDM_IO0 and SDM_IO16 are unavailable, SDM_IO5 can also be used for the INIT_DONE function when the configuration mode is set to Avalon–ST x8 or Avalon–ST x32 (AVST x8 or AVST x32) as these modes require an external 4.7–kΩ pull-down resistor. If SDM_IO0, SDM_IO5, and SDM_IO16 are unavailable, the INIT_DONE function can also be implemented using any unused SDM_IO pins provided that an external 4.7–kΩ pull-down resistor is provided for the INIT_DONE signal.			SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO15 SDM_IO16	SDM_IO7 SDM_IO8 SDM_IO9 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO15 SDM_IO16
CvP_CONFDONE	The CvP_CONFDONE pin indicates the device has received the complete bitstream during configuration via protocol (CvP) core image configuration. When used for this purpose, enable this pin using the Intel Quartus Prime software.	Connect this output pin to an external logic device that monitors the CvP operation. The VCCIO_SDM power supply must meet the input voltage specification of the receiving side.	SDM_IO0 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO16	SDM_IO0 SDM_IO5 SDM_IO7 SDM_IO9 SDM_IO12 SDM_IO16	—	—
SEU_ERROR	The SEU_ERROR pin drives high to indicate there is an SEU error message inside the SEU error queue. This pin stays high whenever the error message queue contains one or more error messages. The SEU_ERROR signal goes low only when the SEU error message queue is empty. When used for this purpose, enable this pin using the Intel Quartus Prime software.	Connect this output pin to an external logic device that monitors the SEU event.	SDM_IO0 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO16	SDM_IO0 SDM_IO5 SDM_IO7 SDM_IO9 SDM_IO12 SDM_IO16	SDM_IO0 SDM_IO1 SDM_IO2 SDM_IO3 SDM_IO4 SDM_IO5 SDM_IO6 SDM_IO7 SDM_IO9 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14	SDM_IO0 SDM_IO1 SDM_IO2 SDM_IO3 SDM_IO4 SDM_IO5 SDM_IO6 SDM_IO7 SDM_IO9 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14

continued...

Signal Name	Signal Description	Connection Guidelines	Configuration Schemes			
			ASx4	AVSTx8	AVSTx16	AVSTx32
					SDM_IO15 SDM_IO16	SDM_IO15 SDM_IO16
HPS_COLD_nRESET	This is an active low, bidirectional pin. By default, this pin acts as an input pin to the SDM. When asserted externally, this pin will generate interrupt to the SDM. The SDM will then initiate a cold reset procedure to the HPS and its peripherals. If the cold reset is generated from internal sources (for example, the HPS EL3 software), the SDM will switch this pin to output and drive a pulse to indicate reset. Once the cold reset procedure is complete, this pin will be switched back to input.	Connect this pin through a 1–10-kΩ pull up to the VCCIO_SDM supply. Do not connect this pin to the reset input of any connected quad serial peripheral interface (quad SPI) devices.	SDM_IO0 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO16	SDM_IO0 SDM_IO5 SDM_IO7 SDM_IO9 SDM_IO12 SDM_IO16	SDM_IO0 SDM_IO1 SDM_IO2 SDM_IO3 SDM_IO4 SDM_IO5 SDM_IO6 SDM_IO7 SDM_IO9 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO15 SDM_IO16	SDM_IO0 SDM_IO1 SDM_IO2 SDM_IO3 SDM_IO4 SDM_IO5 SDM_IO6 SDM_IO7 SDM_IO9 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO15 SDM_IO16
Direct to Factory Image	Direct to factory input pin. When using the remote system upgrade feature, this optional pin allows you to choose between factory or application image. Driving logic high into this pin will instruct the device to load factory image, while driving logic low into this pin will instruct the device to load the application image.	Connect this input pin to an external logic device that manages the remote system upgrade of the device. By default, the external logic should provide logic low to this pin so that the application image will be the default image of the device, and only switch to factory image if required.	SDM_IO0 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO16	—	—	—
nCATTRIP	The catastrophic trip signal, nCATTRIP, is an optional signal that you can assign to any unused SDM_IO pin. If enabled, the nCATTRIP signal will always stay high and drives low when the core temperature is greater than 120°C. When the signal drives low, you must	Connect this output pin to an external device that monitors the nCATTRIP event.	SDM_IO0 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO16	SDM_IO0 SDM_IO5 SDM_IO7 SDM_IO9 SDM_IO12 SDM_IO16	SDM_IO0 SDM_IO1 SDM_IO2 SDM_IO3 SDM_IO4 SDM_IO5 SDM_IO6 SDM_IO7	SDM_IO0 SDM_IO1 SDM_IO2 SDM_IO3 SDM_IO4 SDM_IO5 SDM_IO6 SDM_IO7

Signal Name	Signal Description	Connection Guidelines	Configuration Schemes			
			ASx4	AVSTx8	AVSTx16	AVSTx32
	immediately power down the FPGA to avoid permanent damage to the device.				SDM_IO9 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO15 SDM_IO16	SDM_IO9 SDM_IO10 SDM_IO11 SDM_IO12 SDM_IO13 SDM_IO14 SDM_IO15 SDM_IO16

1.3. Intel Agilex 7 E-Tile Pins

1.3.1. E-Tile Power Supply Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 14. E-Tile Power Supply Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
VCCH_GXE[R1]	Power	Analog power, block level transmitter buffers for E-tile, specific to the right (R) side of the device.	Connect VCCH_GXE to a 1.1-V low noise switching regulator. VCCH_GXE must be powered up even when the E-tile transceivers are not used. For more details about the decoupling recommendations for this voltage rail, refer to the *AN 910: Intel Agilex 7 Power Distribution Network Design Guidelines*.
VCCRT_GXE[R1]	Power	Analog power, used for the high-speed circuitry for the E-tile, specific to the right (R) side of the device.	VCCRT_GXE can be connected to a 0.9-V low noise switching regulator. You must connect VCCRT_GXE to VCCH through an LC filter. For more information about the LC filter design, refer to the *AN 910: Intel Agilex 7 Power Distribution Network Design Guidelines*.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
			VCCRT_GXE must be powered up even when the E-tile transceivers are not used. For more details about the decoupling recommendations for this voltage rail, refer to the *AN 910: Intel Agilex 7 Power Distribution Network Design Guidelines*.
VCCRTPLL_GXE[R1]	Power	Analog power, used for the high-speed circuitry for the E-tile, specific to the right (R) side of the device.	You must source the VCCRTPLL_GXE from the VCCH with proper isolation filtering. Filtering may be optional if this voltage rail can meet the noise mask requirement. For more information about the noise mask requirements, refer to the *Intel Agilex 7 Power Management User Guide*. VCCRTPLL_GXE must be powered up even when the E-tile transceivers are not used. For more details about the decoupling recommendations for this voltage rail, refer to the *AN 910: Intel Agilex 7 Power Distribution Network Design Guidelines*.
VCCCLK_GXE[R1]	Power	I/O power, specific to the E-tile reference clock buffers.	Connect VCCCLK_GXE to a 2.5-V low noise switching regulator. VCCCLK_GXE must be powered up even when the E-tile transceivers are not used. For more details about the decoupling recommendations for this voltage rail, refer to the *AN 910: Intel Agilex 7 Power Distribution Network Design Guidelines*.
VCC_HSSI_GXE[R1]	Power	Primary digital supply for all digital signals, specific to E-tile.	Connect VCC_HSSI_GXE to a 0.9-V low noise switching regulator. This voltage rail must be shared with VCCH. VCC_HSSI_GXE must be powered up even when the E-tile transceivers are not used.

Related Information

- E-Tile Transceiver PHY User Guide
- AN 910: Intel Agilex 7 Power Distribution Network Design Guidelines

1.3.2. E-Tile Transceiver Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 15. E-Tile Transceiver Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
GXE[R9A]_RX_CH[0:23][p,n]	Input	High speed differential serial inputs to receiver circuitry. Specific to the E-tile transceiver on the right (R) side of the device. Supports both NRZ and PAM4 modulation. For the supported data rates, refer to the *Intel Agilex 7 FPGAs and SoCs Device Data Sheet: F-Series and I-Series*.	No off-chip AC-coupling capacitor is required if the RX input common mode is between VCCRT_GXE and GND, and the RX input amplitude difference is less than 1200 mVp-p. The absolute maximum input to the E-Tile SerDes is VCCRT_GXE + 300 mV to prevent forward biasing of the ESD diodes. When using external AC-coupling capacitors, the RX termination is to the VCCH_GXE supply. For more information about the external AC-coupling, refer to the *E-Tile Transceiver PHY User Guide*. Leave unused pins floating.
GXE[R9A]_TX_CH[0:23][p,n]	Output	High speed differential serial outputs from the transmitter circuitry. Specific to the E-tile transceiver on the right (R) side of the device. Supports both NRZ and PAM4 modulation. For the supported data rates, refer to the *Intel Agilex 7 FPGAs and SoCs Device Data Sheet: F-Series and I-Series*.	Leave unused pins floating.
REFCLK_GXE[R9A]_CH[0:8][p,n]	Input	High speed differential reference clock connects to the E-tile transceiver of the right (R) side of the device. REFCLK_GXE is supplied to both RX and TX independently. REFCLK_GXE can be used as dedicated clock input pins for core clock generation by configuring transceiver channel (Native PHY IP core) in the PLL mode. Supported I/O standard: • LVPECL	The default internal REFCLK inputs are 2.5-V LVPECL with a 50-Ω termination. You have to enable the internal terminations in the Intel Quartus Prime software. Optional external termination is 2.5-V LVPECL or 3.3-V LVPECL. For more information about the external termination, refer to the *Reference Clock Pins* section of the *E-Tile Transceiver PHY User Guide*. Tie each unused REFCLK pin to GND through a 1-kΩ resistor. REFCLK[1] must always be bonded out on board and connected to a clock source in case dynamic reconfiguration of REFCLK is planned. For more details on how to use it, refer to the *Dynamic Reconfiguration Flow for Special Cases* section of the *E-Tile Transceiver PHY User Guide*.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
			Preservation of unused transceiver channels may need extra REFCLK_GXE to be bonded out on board based on use cases. For more details, refer to the *Unused Transceiver Channels* section of the *E-Tile Transceiver PHY User Guide*. The input reference clock must be stable and free-running at FPGA power-up for proper PLL calibrations and a successful configuration.
IO_AUX_RREF[20]	Input	Precision reference resistor for the AIB auxiliary channel.	Connect to a 2-kΩ resistor (±1%) to GND.

1.4. Intel Agilex 7 P-Tile Pins

This section contains connection guidelines that are specific to the Intel Agilex 7 P-tile devices. The connection guidelines for the Intel Agilex 7 core pins are listed in the *Intel Agilex 7 Core Pins* section.

Note: You cannot change the P-tile IP for the PCI Express (PCIe) pin allocation in the Intel Quartus Prime project, but the P-tile IP for the PCIe supports lane reversal and polarity inversion on the PCB.

1.4.1. P-Tile Power Supply Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 16. P-Tile Power Supply Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
VCCH_GXP[L1,L3]	Power	Secondary high-voltage analog supply for transceivers, and on-die PLL specific to P-tile. For more information about the supported pins, refer to the device pin-out file.	Connect VCCH_GXP to a 1.8-V low noise switching regulator. This voltage rail can be shared with VCCPT using proper isolation filtering.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
			VCCH_GXP must be powered up even when the P-tile transceivers are not used. For more details about the decoupling recommendations for this voltage rail, refer to the *AN 910: Intel Agilex 7 Power Distribution Network Design Guidelines*.
VCCRT_GXP[L1,L3]	Power	Primary analog supply for the TX and RX channels, specific to P-tile. For more information about the supported pins, refer to the device pin-out file.	Connect VCCRT_GXP to a 0.9-V low noise switching regulator. This voltage rail can be shared with VCCH using proper isolation filtering. VCCRT_GXP must be powered up even when the P-tile transceivers are not used. For more details about the decoupling recommendations for this voltage rail, refer to the *AN 910: Intel Agilex 7 Power Distribution Network Design Guidelines*.
VCCCLK_GXP[L1,L3]	Power	LVCMOS I/O buffer supply rail, specific to P-tile. For more information about the supported pins, refer to the device pin-out file.	Connect VCCCLK_GXP to a 1.8V low noise switching regulator. This voltage rail can be shared with VCCPT using proper isolation filtering. VCCCLK_GXP must be powered up even when the P-tile transceivers are not used. For more details about the decoupling recommendations for this voltage rail, refer to the *AN 910: Intel Agilex 7 Power Distribution Network Design Guidelines*.
VCCFUSE_GXP	Power	Required power supply for the firmware to read internal settings for the one-time programmable eFuses.	Connect this voltage rail to a 0.9-V power supply. This rail must be shared with VCC_HSSI_GXP. VCCFUSE_GXP must be powered up even when the P-tile transceivers are not used. For more details about the decoupling recommendations for this voltage rail, refer to the *AN 910: Intel Agilex 7 Power Distribution Network Design Guidelines*.
VCC_HSSI_GXP[L1,L3]	Power	Primary digital supply for all digital signals, specific to P-tile. For more information about the supported pins, refer to the device pin-out file.	Connect VCC_HSSI_GXP to a 0.9-V low noise switching regulator. This voltage rail must be shared with VCCH. VCC_HSSI_GXP must be powered up even when the P-tile transceivers are not used.

Related Information

AN 910: Intel Agilex 7 Power Distribution Network Design Guidelines

1.4.2. P-Tile Transceiver Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 17. P-Tile Transceiver Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
GXP[L10A,L10C]_RX_CH[15:0][p,n]	Input	PCIe* Gen4-based receiver pins, specific to the P-tile transceivers on the left (L) side of the device. For more information about the supported pins, refer to the device pin-out file.	When these pins are not used, they must be tied via a 1kΩ pull-down resistor to GND.
GXP[L10A,L10C]_TX_CH[15:0][p,n]	Output	PCIe Gen4-based transmitter pins, specific to the P-tile transceivers on the left (L) side of the device. For more information about the supported pins, refer to the device pin-out file.	Transmitter pins must be AC coupled. The capacitor value ranges from 176 nF to 256 nF per PCIe Gen4 specification. When these pins are not used, they must be floating.
REFCLK_GXP[L10A,L10C]_CH[0,2][p,n]	Input	Standard PCIe HCSL reference clock input pins, specific to the P-tile transceivers on the left (L) side of the device. For more information about the supported pins, refer to the device pin-out file.	For HCSL I/O standard, it only supports DC coupling. You must connect a 100-MHz reference clock to both reference clock inputs for x16 and 4x4 modes. These reference clocks must be derived from the same clock source. A fan-out buffer can be used but must meet a ± 300 ppm requirement. For 2x8 modes, you must connect both reference clock inputs to the same clock source or connect to two independent clock sources. If the P-tile is completely unused, tie both REFCLK inputs to GND. Unused reference clock pins must be tied to 1kΩ pull-down resistor to GND.
IO_AUX_RREF[10,12]_P	Input	Reference resistor for the Embedded Multi-Die-Interconnect Bridge (EMIB) of the P-tile transceivers. Not all pins are available in each device density and package combination. For more information, refer to the specific device pin-out file.	Connect each IO_AUX_RREF to a 2.8 kΩ resistor (±1%) to GND. In the PCB layout, the trace from this pin to the resistor needs to be routed such that it avoids any aggressor signals.
U[10,12]_P_IO_RESREF_0	Input	Transceiver reference resistor connection for PMA circuitry to provide termination for calibration.	Connect each pin to a 169Ω 1% (100 ppm/°C) precision resistor to GND.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
		Not all pins are available in each device density and package combination. For more information, refer to the specific device pin-out file.	Place this resistor very close to the IO_RESREF pin. Avoid routing any noisy signals next to this reference resistor or its traces. Tie resistor to GND plane through a via placed very close to the reference resistor. External reference resistor parasitic capacitance load must be less than 14 pF. Maximum parasitic capacitance includes external loading of PHY count, package trace, and PCB trace. Each PHY connected to the IO_RESREF pin adds an additional 1.5 pF of loading.
I_PIN_PERST_N_U[10,12]_P	Input	PCI Express* (PCIe) Platform reset pin. For more information about the supported pins, refer to the device pin-out file.	In a PCI Express (PCIe) adapter card implementation, connect the PCIe nPERST signal from the PCIe edge connector to each P-tile transceiver bank I_PIN_PERST_N input. Use a level translator to fan out and change the 3.3-V open-drain nPERST signal from the PCIe connector to the 1.8-V I_PIN_PERST_N input of each P-tile transceiver that is used on the board. Provide a 1.8-V pull-up resistor to the I_PIN_PERST_N input as the nPERST signal from the PCIe connector is an open-drain signal. You must pull up the 3.3-V PCIe nPERST signal on the adapter card. If the tile is unused, tie to GND. In cases where two independent clock sources are used for 2x8 bifurcation mode, ensure I_PIN_PERST_N be de-asserted high after both reference clocks are stable.

1.5. Intel Agilex 7 F-Tile Pins

1.5.1. F-Tile Power Supply Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 18. F-Tile Power Supply Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
VCC_HSSI_GXF[L,R]	Power	F-tile digital 0.8-V logic. For more information about the supported pins, refer to the device pin-out file.	Connect VCC_HSSI_GXF to low noise switching regulator. Refer to *AN 910: Intel Agilex 7 Power Distribution Network Design Guidelines* for decoupling capacitor requirement. Tie to GND if this tile is not used.
VCCH_FGT_GXF[L,R]	Power	F-tile general purpose transceiver (FGT) digital 1.8-V logic. For more information about the supported pins, refer to the device pin-out file.	VCCH_FGT_GXF should share 1.8-V rail with VCCPT through ferrite bead. Refer to *AN 910: Intel Agilex 7 Power Distribution Network Design Guidelines* for fitter details and decoupling capacitor requirement. Tie to GND if this tile is not used.
VCCEHT_FHT_GXF[L,R]	Power	F-tile high-speed transceiver (FHT) digital 1.5-V logic. For more information about the supported pins, refer to the device pin-out file.	Connect VCCEHT_FHT_GXF to dedicated regulator. Refer to *AN 910: Intel Agilex 7 Power Distribution Network Design Guidelines* for decoupling capacitor requirement. Tie to GND if there is no FHT channel used.
VCCERT_FGT_GXF[L,R]	Power	F-tile FGT analog 1.0-V logic. For more information about the supported pins, refer to the device pin-out file.	Connect VCCERT_FGT_GXF to dedicated regulator. Refer to *AN 910: Intel Agilex 7 Power Distribution Network Design Guidelines* for decoupling capacitor requirement. This analog supply should not share with others. Tie to GND if this tile is not used.
VCCERT1_FHT_GXF[L,R]	Power	F-tile FHT analog 1.0-V supply 1. For more information about the supported pins, refer to the device pin-out file.	Connect VCCERT1_FHT_GXF to dedicated regulator. Refer to *AN 910: Intel Agilex 7 Power Distribution Network Design Guidelines* for decoupling capacitor requirement. You have an option to share the same regulator with VCCERT_FGT_GXF. This analog supply should not share with others. Tie to GND if there is no FHT channel used.
VCCERT2_FHT_GXF[L,R]	Power	F-tile FHT analog 1.0-V supply 2. For more information about the supported pins, refer to the device pin-out file.	Connect VCCERT2_FHT_GXF to dedicated regulator. Refer to *AN 910: Intel Agilex 7 Power Distribution Network Design Guidelines* for decoupling capacitor requirement. You have an option to share the same regulator with VCCERT_FGT_GXF. This analog supply should not share with others. Tie to GND if there is no FHT channel used.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
VCCFUSECORE_GXF[L,R]	Power	F-tile fuse sense 1.0-V supply. For more information about the supported pins, refer to the device pin-out file.	VCCFUSECORE_GXF should share 1.0-V rail from power group 2. Refer to *AN 910: Intel Agilex 7 Power Distribution Network Design Guidelines* for decoupling capacitor requirement. Tie to GND if this tile is not used.
VCCFUSEWR_GXF[L,R]	Power	F-tile fuse sense 1.0-V supply. For more information about the supported pins, refer to the device pin-out file.	VCCFUSEWR_GXF should share 1.0-V rail from power group 2. Refer to *AN 910: Intel Agilex 7 Power Distribution Network Design Guidelines* for decoupling capacitor requirement. Tie to GND if this tile is not used
VCCCLK_GXF[L,R]	Power	F-tile 1.8-V supply. For more information about the supported pins, refer to the device pin-out file.	VCCCLK_GXF should share 1.8-V rail with VCCPT through ferrite bead. Refer to *AN 910: Intel Agilex 7 Power Distribution Network Design Guidelines* for filter details and decoupling capacitor requirement. Tie to GND if this tile is not used.
VCC_SENSE_FHT_GXF VSS_SENSE_FHT_GXF	Power Sense	Differential sense line to external regulator.	VCC_SENSE_FHT_GXF and VSS_SENSE_FHT_GXF are differential remote sense pins for the VCCERT1_FHT_GXF power. Connect the differential remote sense lines of the regulator to the respective VCC_SENSE_FHT_GXF and VSS_SENSE_FHT_GXF pins. This compensates for the DC IR drop associated with the PCB and device package from the VCCERT1_FHT_GXF power. Route these connections as differential pair traces and keep them isolated from any other noise source. You must connect the VCC_SENSE_FHT_GXF and VSS_SENSE_FHT_GXF lines to the remote sense inputs of the regulator. Tie to GND if there is no FHT channel used.

Related Information

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1.5.2. F-Tile Transceiver Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 19. F-Tile Transceiver Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
RCOMP_P_FHT_GXF RCOMP_N_FHT_GXF	Input	External biasing resistor for F-tile FHT.	Connect each RCOMP_P_FHT_GXF pin with a 1.5-KΩ resistor (0.1%) to the RCOMP_N_FHT_GXF pin. In the PCB layout, the trace from this pin to the resistor needs to be routed such that it avoids any aggressor signals. If this tile is unused, you must connect the 1.5-KΩ resistor between the RCOMP_P_FHT_GXF and RCOMP_N_FHT_GXF pins.
RCOMP_P_Q2_CH1_FGT_GXF RCOMP_N_Q2_CH1_FGT_GXF	Input	External biasing resistor for F-tile FGT.	Connect each RCOMP_P_Q2_CH1_FGT_GXF pin with a 499-Ω resistor (0.1%) to the RCOMP_N_Q2_CH1_FGT_GXF pin. In the PCB layout, the trace from this pin to the resistor needs to be routed such that it avoids any aggressor signals. If this tile is unused, you must connect the 499-Ω resistor between the RCOMP_P_Q2_CH1_FGT_GXF and RCOMP_N_Q2_CH1_FGT_GXF pins.
REFCLK_FHT[L,R]_CH[0,1]P REFCLK_FHT[L,R]_CH[0,1]N	Input	F-tile FHT reference clock input pins. For more information about the supported pins, refer to the device pin-out file.	AC or DC coupled. Clock driver must be compatible with input requirement in DC coupling case. Tie to GND if these pins are not used.
REFCLK_FGT[L,R]_Q[0,1,2,3]_RX_CH[0,1,2,3,4,5,6,7]P REFCLK_FGT[L,R]_Q[0,1,2,3]_RX_CH[0,1,2,3,4,5,6,7]N	Input	F-tile FGT reference clock input pins. For more information about the supported pins, refer to the device pin-out file.	AC or DC coupled. Clock driver must be compatible with input requirement in DC coupling case. Tie to GND if these pins are not used.
REFCLK_FGT[L,R]_Q[2,3]_CH[8,9]P REFCLK_FGT[L,R]_Q[2,3]_CH[8,9]N	Input/Output	F-tile FGT reference clock input or recovery clock output pins. For more information about the supported pins, refer to the device pin-out file.	AC or DC coupled. Clock driver must be compatible with input requirement in DC coupling input case. Tie to GND or leave floating if this tile is not used. Tie to GND if the tile is used, and the pin is not used.
FHT[L,R]_RX_CH[0,1,2,3]P FHT[L,R]_RX_CH[0,1,2,3]N	Input	F-tile FHT transceiver input pins. For more information about the supported pins, refer to the device pin-out file.	AC or DC coupled. Tie to GND if these pins are not used.

continued...

Pin Name	Pin Functions	Pin Description	Connection Guidelines
FHT[L,R]_TX_CH[0,1,2,3]P	Output	F-tile FHT transceiver output pins. For more information about the supported pins, refer to the device pin-out file.	Leave unused pins floating.
FHT[L,R]_TX_CH[0,1,2,3]N			
FGT[L,R]_RX_Q[0,1,2,3]_CH[0,1,2,3]P	Input	F-tile FGT transceiver input pins. For more information about the supported pins, refer to the device pin-out file.	AC or DC coupled. Tie to GND if these pins are not used. The F-tile PCI Express hard IP supports x2 or x1 link width configuration via link downtraining from x4. For these two cases, leave the unused upper lanes unconnected on the PCB and do not tie them to GND.
FGT[L,R]_RX_Q[0,1,2,3]_CH[0,1,2,3]N			
FGT[L,R]_TX_Q[0,1,2,3]_CH[0,1,2,3]P	Output	F-tile FGT transceiver output pins. For more information about the supported pins, refer to the device pin-out file.	Leave unused pins floating.
FGT[L,R]_TX_Q[0,1,2,3]_CH[0,1,2,3]N			
I_PIN_PERST_N_GXF	Input	External reset for F-tile in one PCIe case.	1.8-V LVCMOS reset input in PCIe case. In a PCIe adapter card implementation, connect this signal from the PCIe edge connector to each F-tile PCIe reset input pin. Use a level translator to fan out and change the 3.3-V open-drain nPERST signal from the PCIe connector to the 1.8-V input of each F-tile transceiver that is used on the board. Provide a 1.8-V pull-up resistor for this input pin as the nPERST signal from the PCIe connector is an open-drain signal. You must pull up the 3.3-V PCIe nPERST signal on the adapter card. If the F-tile is unused, or the F-tile is used but PCI Express is unused, tie to GND. In case one reset pin controls multiple PCIe IPs in bifurcation mode, ensure that this signal is de-asserted high after all IPs reference clocks are stable.
ENB_GXF_FHT	Input	Enable or disable FHT support in F-tile.	Tie to VCCCLK_GXF if FHT channels are used; tie to GND if FHT channel is not used.
APROBE_GXF_FGT[12A]_Q[0,2,3]_CH3	—	—	Leave these pins floating.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
APROBE2_GXF_FGT[12A]_Q3_CH3	—	—	Leave these pins floating.
APROBE1_GXF_FHT[12A]	—	—	Leave these pins floating.
APROBE2_GXF_FHT[12A]	—	—	Leave these pins floating.

1.6. Intel Agilex 7 R-Tile Pins

1.6.1. R-Tile Power Supply Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 20. R-Tile Power Supply Pins

Pin Name	Pin Functions	Pin Description	Connection Guidelines
VCC_HSSI_GXR[L,R]	Power	Primary digital supply for all digital signals, specific to R-tile. For more information about the supported pins, refer to the device pin-out file.	Connect VCC_HSSI_GXR to a 0.9-V low noise switching regulator. Refer to *AN 910: Intel Agilex 7 Power Distribution Network Design Guidelines* for decoupling capacitor requirement. Connect to GND if not used.
VCCH_GXR[L,R]	Power	Secondary high-voltage analog supply for transceivers. For more information about the supported pins, refer to the device pin-out file.	Connect VCCH_GXR to a 1.8-V low noise switching regulator. This voltage rail can be shared with VCCPT using proper isolation filtering. To minimize regulator switching noise impact on channel jitter performance, keep the regulator switching frequency below 1 MHz. Refer to *AN 910: Intel Agilex 7 Power Distribution Network Design Guidelines* for decoupling capacitor requirement. Connect to GND if not used.

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Pin Name	Pin Functions	Pin Description	Connection Guidelines
VCCED_GXR[L,R]	Power	Transceiver digital supply. For more information about the supported pins, refer to the device pin-out file.	Connect VCCED_GXR to a dedicated 0.9-V linear regulator or low noise switching regulator. Refer to *AN 910: Intel Agilex 7 Power Distribution Network Design Guidelines* for decoupling capacitor requirement. Connect to GND if not used.
VCCRT_GXR[L,R]	Power	Analog power, used for the high-speed circuitry for the R-tile. For more information about the supported pins, refer to the device pin-out file.	Connect VCCRT_GXR to a dedicated 1.0-V linear regulator or low noise switching regulator with filter. Refer to *AN 910: Intel Agilex 7 Power Distribution Network Design Guidelines* for fitter details and decoupling capacitor requirement. This analog supply cannot be shared. Connect to GND if not used.
VCCE_DTS_GXR[L,R]	Power	DTS reference voltage at 1.0 V. For more information about the supported pins, refer to the device pin-out file.	Connect VCCE_DTS_GXR to the same regulator as VCCE_PLL_GXR. Refer to *AN 910: Intel Agilex 7 Power Distribution Network Design Guidelines* for fitter details and decoupling capacitor requirement. Connect to GND when not used.
VCCE_PLL_GXR[L,R]	Power	Power for PLL reference signal. For more information about the supported pins, refer to the device pin-out file.	Connect VCCE_PLL_GXR to the same regulator as VCCE_DTS_GXR. Refer to *AN 910: Intel Agilex 7 Power Distribution Network Design Guidelines* for fitter details and decoupling capacitor requirement. Connect to GND when not used.
VCCHFUSE_GXR[L,R]	Power	Power supply for programmable eFuse. For more information about the supported pins, refer to the device pin-out file.	Connect VCCHFUSE_GXR to a dedicated 1.0-V linear or low noise switching regulator. Tie it to GND if the R-tile is unused. For more details about the decoupling recommendations for this voltage rail, refer to *AN 910: Intel Agilex 7 Power Distribution Network Design Guidelines*.
VCCCLK_GXR[L,R]	Power	Primary digital supply for all digital signals, specific to R-tile. For more information about the supported pins, refer to the device pin-out file.	Connect VCCCLK_GXR to a 1.0-V low noise switching regulator. VCCCLK_GXR can share through ferrite bead. Refer to *AN 910: Intel Agilex 7 Power Distribution Network Design Guidelines* for decoupling capacitor requirement. Connect to GND when not used.

1.6.2. Intel Agilex 7 R-Tile Transceiver Pins

Table 21. Intel Agilex 7 R-Tile Transceiver Pins

For more information, refer to the *R-Tile PCIe IP User Guide*.

Pin Name	Pin Functions	Pin Description	Connection Guidelines
IO_RCOMP_0_P_GXR	Input	External biasing resistor for R-tile.	Connect a 150 Ω 1% resistor between the IO_RCOMP_0_N_GXR pin and IO_RCOMP_0_P_GXR pin of each R-tile bank. RCOMP_P and RCOMP_N total trace routing (package and board) resistance is less than 0.500 Ω. In the PCB layout, do not route traces next to high-speed clock or data aggressors. You are required to keep the maximum capacitance on RCOMP_P less than 5.0 pF. IO_ROMP_1_P and IO_ROMP_1_N are only available on the Intel Agilex 7 AGI041 device. If this tile is unused, leave these pins floating.
IO_RCOMP_0_N_GXR			
IO_RCOMP_1_P_GXR	Input	External biasing resistor for R-tile.	
IO_RCOMP_1_N_GXR			
I_PIN_PERST_N_GXR	Input	PCI Express (PCIe) Platform reset pin.	The usage of this pin is different between the Intel Agilex 7 AGI041 device and other Intel Agilex 7 FPGA devices. For Intel Agilex 7 I-series devices except for the Intel Agilex 7 AGI041 device: • In a PCIe adapter card implementation, connect the PCIe nPERST signal from the PCIe edge connector to each R-tile transceiver bank I_PIN_PERST_N input. Use a level translator to fan out and change the 3.3 V open-drain nPERST signal from the PCIe connector to the 1.0 V I_PIN_PERST_N input of each R-tile transceiver that is used on the board. Provide a 1.0 V pull-up resistor to the I_PIN_PERST_N input as the nPERST signal from the PCIe connector is an open-drain signal. You must pull up the 3.3 V PCIe nPERST signal on the adapter card. • In 2 x 8 bifurcation EP mode, in cases where two independent clock sources are used for 2 x 8 bifurcation mode, ensure that the I_PIN_PERST_N is de-asserted high after both REFCLK_GXR_CH0 and REFCLK_GXR_CH1 are stable.

continued...

Pin Name	Pin Functions	Pin Description	Connection Guidelines
			For Intel Agilex 7 AGI041 device: • In 1 x 16 root port (RP), 1 x 16 TLP bypass mode (BP), 1 x 16 end point (EP), 2 x 8 RP, 2 x 8 BP, 2 x 8 EP (with the **Enable Independent PERST pins** parameter set to **disable** in the Intel Quartus Prime IP), 4 x 4 RP, 4 x 4 BP, and 4 x 4 EP, connect the PCIe nPERST signal from the PCIe edge connector to each R-tile transceiver bank I_PIN_PERST_N input. Use a level translator to fan out and change the 3.3 V open-drain nPERST signal from the PCIe connector to the 1.0 V I_PIN_PERST_N input of each R-tile transceiver that is used on the board. Provide a 1.0 V pull-up resistor to the I_PIN_PERST_N input as the nPERST signal from the PCIe connector is an open-drain signal. You must pull up the 3.3 V PCIe nPERST signal on the adapter card. • In 2 x 8 EP (with the **Enable Independent PERST pins** parameter set to **enable** in the Intel Quartus Prime IP), this I_PIN_PERST_N pin must be de-asserted high after REFCLK_GXR_CH2 is stable for at least 100 µs. If the tile is unused for both Intel Agilex 7 AGI041 and other Intel Agilex 7 devices, tie to GND.
			continued...

Pin Name	Pin Functions	Pin Description	Connection Guidelines
I_PIN_PERST[0,1]_N_GXR	Input	PCI Express (PCIe) PORT0 and PORT1 reset pin.	Active low. These two pins are only available in the Intel Agilex 7 AGI041 device. • In 1 x 16 RP, 1 x 16 BP, 1 x 16 EP, 2 x 8 RP, 2 x 8 BP, 2 x 8 EP (with the **Enable Independent PERST pins** parameter set to **disable** in the Intel Quartus Prime IP), 4 x 4 RP, 4 x 4 BP, and 4 x 4 EP, leave these two pins floating. • In 2 x 8 EP (with the **Enable Independent PERST pins** parameter set to **enable** in the Intel Quartus Prime IP), I_PIN_PERST0_N is the independent reset signal for PORT0 and I_PIN_PERST1_N is the independent reset signal for PORT1. In a PCIe adapter card implementation with 2 x 8 EP mode, connect the PCIe nPERST signal from the PCIe edge connector to the corresponding I_PIN_PERST0_N or I_PIN_PERST1_N signal. Use a level translator to fan out and change the 3.3 V open-drain nPERST signal from the PCIe connector to the 1.0 V I_PIN_PERST0_N or I_PIN_PERST1_N input of each R-tile transceiver that is used on the board. Provide a 1.0 V pull-up resistor to the I_PIN_PERST0_N or I_PIN_PERST1_N input if the nPERST signal from the PCIe connector is an open-drain signal. You must pull up the 3.3 V PCIe nPERST signal on the adapter card. In cases where two independent clock sources are used, ensure that I_PIN_PERST0_N is de-asserted high after REFCLK_GXR_CH0 is stable and I_PIN_PERST1_N is de-asserted high after REFCLK_GXR_CH1 is stable. If any port is unused, its corresponding I_PIN_PERST_N pin must be tied to GND.
REFCLK_GXR[R,L][14A,14C,15A,15C]_CH[0,1]P REFCLK_GXR[R,L][14A,14C,15A,15C]_CH[0,1]N	Input	Standard PCIe High Speed Current Steering Logic (HCSL) reference clock input pins, specific to the R-tile transceivers on the left (L) side or right (R) side of the device. For more information about the supported pins, refer to the device pin-out file.	It supports HCSL I/O standard only, must be DC coupled.

continued...

Pin Name	Pin Functions	Pin Description	Connection Guidelines
			For all Intel Agilex 7 I-series devices, including the Intel Agilex 7 AGI041 device: • In 1 x 16 RP, 1 x 16 BP, 1 x 16 EP, 2 x 8 RP, 2 x 8 BP, 2 x 8 EP (with the **Enable Independent PERST pins** parameter set to **disable** in the Intel Quartus Prime IP), 4 x 4 RP, 4 x 4 BP, and 4 x 4 EP, you must connect a 100 MHz ±100 ppm reference clock to both reference clock inputs. These reference clocks must be derived from the same clock source. A fan-out buffer can be used but must meet a ±100 ppm requirement for Gen 5. • In 2 x 8 EP (with the **Enable Independent PERST pins** parameter set to **enable** in the Intel Quartus Prime IP), you can connect both reference clock inputs to the same clock source or connect to two independent clock sources. Leave these pins floating if unused.
REFCLK_GXR[R,L][14A,14C,15A,15C]_CH2P REFCLK_GXR[R,L][14A,14C,15A,15C]_CH2N	Input	Standard PCIe High Speed Current Steering Logic (HCSL) reference clock input pins, specific to the FPGA core fabric. For more information about the supported pins, refer to the device pin-out file.	These two pins are only available in the Intel Agilex 7 AGI041 device. It supports HCSL I/O standard only, must be DC coupled. • In 1 x 16 RP, 1 x 16 BP, 1 x 16 EP, 2 x 8 RP, 2 x 8 BP, 2 x 8 EP (with the **Enable Independent PERST pins** parameter set to **disable** in the Intel Quartus Prime IP), 4 x 4 RP, 4 x 4 BP, and 4 x 4 EP, this reference clock can be tied to GND or connect a 100 MHz ±100 ppm local board reference clock to this reference clock input. • In 2 x 8 EP (with the **Enable Independent PERST pins** parameter set to **enable** in the Intel Quartus Prime IP), you must connect a 100 MHz ±100 ppm local board reference clock to the reference clock input to ensure this reference clock is always provided. Leave these pins floating if unused.
GXR[R,L][14A,14C,15A,15C]_RX_CH[0:15]P	Input	Transceiver receiver pins, specific to the R-tile transceivers on the left (L) side or right (R) side of the device. For PCIe Gen 5 mode, use the lower 16 bits [15:0]. These pins also support NRZ encoding up to 32 Gbps. For more information about the supported pins, refer to the device pin-out file.	Leave these pins floating if unused.

continued...

Pin Name	Pin Functions	Pin Description	Connection Guidelines
GXR[R,L][14A,14C,15A,15C]_RX_CH[0:15]N			
GXR[R,L][14A,14C,15A,15C]_TX_CH[0:15]P	Output	Transceiver transmitter pins, specific to the R-tile transceivers on the left (L) side or right (R) side of the device. For PCIe Gen 5 mode, use the lower 16 bits [15:0]. These pins also support NRZ encoding up to 32 Gbps. For more information about the supported pins, refer to the device pin-out file.	Transmitter pins must be AC coupled. Leave these pins floating if unused.
GXR[R,L][14A,14C,15A,15C]_TX_CH[0:15]N			

1.7. Intel Agilex 7 Hard Processor System (HPS) Pins

1.7.1. HPS Supply Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 22. HPS Supply Pins

<table>
<tr><th>Pin Name</th><th>Pin Functions</th><th>Pin Description</th><th colspan="3">Connection Guidelines</th></tr>
<tr><td rowspan="3">VCCL_HPS</td><td rowspan="3">Power</td><td rowspan="3">VCCL_HPS supplies power to the HPS core.</td><td colspan="3">For the range of the VCCL_HPS power supply voltage, refer to the Intel Agilex 7 FPGAs and SoCs Device Data Sheet: F-Series and I-Series .</td></tr>
<tr><td rowspan="2">Speed Grade</td><td colspan="2">Power Supply Voltage (V)</td></tr>
<tr><td>VCC</td><td>VCCL_HPS</td></tr>
<tr><td>–1</td><td>VID</td><td>VID or standalone 0.95 (performance boost option)</td></tr>
</table>

continued...

Pin Name	Pin Functions	Pin Description	Connection Guidelines		
			–2	VID	VID
			–3	VID	VID
			–4X	VID	0.8
			–4F	0.8	0.8
			VCCL_HPS can be shared with VCC if they are at the same VID voltage level. If you do not intend to utilize the HPS in the Intel Agilex 7 device, you must still provide power to the HPS power supply. Do not leave the VCCL_HPS floating or connected to GND.		
VCCIO_HPS	Power	The HPS dedicated I/Os support 1.8-V voltage level.	Connect these pins to 1.8-V power supply. You have the option to source VCCIO_HPS pins from the same regulator as VCCIO_SDM. If you do not intend to utilize the HPS in the Intel Agilex 7 device, you must still provide power to the HPS power supply. Do not leave the VCCIO_HPS floating or connected to GND.		
VCCPLL_HPS	Power	VCCPLL_HPS supplies analog power to the HPS PLLs.	Connect these pins to a 1.8-V power supply. You have the option to share VCCPLL_HPS with the same regulator as VCCPLL_SDM. If you do not intend to utilize the HPS in the Intel Agilex 7 device, you must still provide power to the HPS power supply. Do not leave the VCCPLL_HPS floating or connected to GND.		
VCCPLLDIG_HPS	Power	Digital power supply of the PLL in HPS.	Connect this to the VCCL_HPS with proper isolation filtering. If you do not intend to utilize the HPS in the Intel Agilex 7 device, you must still provide power to the HPS power supply. Do not leave the VCCPLLDIG_HPS floating or connected to GND.		

1.7.2. HPS Oscillator Clock Input Pin

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 23. HPS Oscillator Clock Input Pin

You must provide one input clock source to the HPS.

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
HPS_OSC_CLK	Clock input pin that drives the main PLL. Connect a single-ended clock source to this pin. The I/O standard of the clock source must be compatible with VCCIO_HPS.	Input	Select one of the 48 HPS dedicated I/O. For details of the supported frequency, refer to the *Intel Agilex 7 FPGAs and SoCs Device Data Sheet: F-Series and I-Series* .

1.7.3. HPS JTAG Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 24. HPS JTAG Pins

You have the option to connect HPS JTAG pins to the HPS Dedicated I/O using the following assignments.

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
JTAG_TCK	HPS JTAG test clock input pin. Connect this pin through a 1-kΩ – 10-kΩ pull-down resistor to GND. Do not drive voltage higher than the VCCIO_HPS supply. You can use the FPGA dedicated JTAG pins as an option to access the HPS JTAG.	Input	HPS_IOB_9
JTAG_TMS	HPS JTAG test mode select input pin. Connect this pin to a 1-kΩ – 10-kΩ pull-up resistor to the VCCIO_HPS supply. Do not drive voltage higher than the VCCIO_HPS supply.	Input	HPS_IOB_10

continued...

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
	You can use the FPGA dedicated JTAG pins as an option to access the HPS JTAG.		
JTAG_TDO	HPS JTAG test data output pin. You can use the FPGA dedicated JTAG pins as an option to access the HPS JTAG.	Output	HPS_IOB_11
JTAG_TDI	HPS JTAG test data input pin. Connect this pin to a 1-kΩ – 10-kΩ pull-up resistor to the VCCIO_HPS supply. Do not drive voltage higher than the VCCIO_HPS supply. You can use the FPGA dedicated JTAG pins as an option to access the HPS JTAG.	Input	HPS_IOB_12

1.7.4. HPS GPIO Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 25. HPS GPIO Pins

There are two GPIO controllers (GPIO0 and GPIO1) for the Intel Agilex 7 HPS.

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
GPIO0_IO[0..23]	General purpose input output. Ensure that the I/O standard used is compatible with VCCIO_HPS.	I/O	HPS_IOA_[1..24] HPS_IOB_[1..24]
GPIO1_IO[0..23]			

1.7.5. HPS SDMMC Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 26. HPS SDMMC Pins

Intel recommends adding a 1-kΩ to 10-kΩ pull-up resistor to every SDMMC data signal that is used.

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the groups)	
			Group 1	Group 2
SDMMC_CCLK	SDMMC clock out	Output	HPS_IOA_1	HPS_IOB_15
SDMMC_CMD	SDMMC command line. Pull this pin high on the board with a weak pull-up resistor. For example, a 10-kΩ to VCCIO_HPS.	I/O	HPS_IOA_2	HPS_IOB_14
SDMMC_DATA0	SDMMC Data 0	I/O	HPS_IOA_3	HPS_IOB_13
SDMMC_DATA1	SDMMC Data 1	I/O	HPS_IOA_4	HPS_IOB_16
SDMMC_DATA2	SDMMC Data 2	I/O	HPS_IOA_5	HPS_IOB_17
SDMMC_DATA3	SDMMC Data 3 When using SD card, there is an existing 50-kΩ pull-up on SDMMC Data Bit 3 which can be disabled in the HPS software by using the SET_CLR_CARD_DETECT (ACMD42) command. This is not applicable to the eMMC flash.	I/O	HPS_IOA_6	HPS_IOB_18
SDMMC_DATA4	SDMMC Data 4	I/O	HPS_IOA_7	HPS_IOB_19
SDMMC_DATA5	SDMMC Data 5	I/O	HPS_IOA_8	HPS_IOB_20
SDMMC_DATA6	SDMMC Data 6	I/O	HPS_IOA_9	HPS_IOB_21
SDMMC_DATA7	SDMMC Data 7	I/O	HPS_IOA_10	HPS_IOB_22
SDMMC_PWR_EN	SDMMC Power Enable	Output	HPS_IOA_11	HPS_IOB_23

1.7.6. HPS NAND Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 27. HPS NAND Pins

HPS Pin Functions	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the groups)	
			Group 1	Group 2
NAND_ADQ0	NAND Data Bit 0	I/O	HPS_IOA_1	HPS_IOB_1
NAND_ADQ1	NAND Data Bit 1	I/O	HPS_IOA_2	HPS_IOB_2
NAND_WE_N	NAND Write Enable. This is an active-low signal.	Output	HPS_IOA_3	HPS_IOB_3
NAND_RE_N	NAND Read Enable. This is an active-low signal.	Output	HPS_IOA_4	HPS_IOB_4
NAND_WP_N	NAND Write Protect	Output	HPS_IOA_5	HPS_IOB_5
NAND_ADQ2	NAND Data Bit 2	I/O	HPS_IOA_6	HPS_IOB_6
NAND_ADQ3	NAND Data Bit 3	I/O	HPS_IOA_7	HPS_IOB_7
NAND_CLE	NAND Command Latch Enable	Output	HPS_IOA_8	HPS_IOB_8
NAND_ADQ4	NAND Data Bit 4	I/O	HPS_IOA_9	HPS_IOB_9
NAND_ADQ5	NAND Data Bit 5	I/O	HPS_IOA_10	HPS_IOB_10
NAND_ADQ6	NAND Data Bit 6	I/O	HPS_IOA_11	HPS_IOB_11
NAND_ADQ7	NAND Data Bit 7	I/O	HPS_IOA_12	HPS_IOB_12
NAND_ALE	NAND Address Latch Enable	Output	HPS_IOA_13	HPS_IOB_13
NAND_RB	NAND Ready/Busy.	Input	HPS_IOA_14	HPS_IOB_14

continued...

HPS Pin Functions	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the groups)	
			Group 1	Group 2
	Connect this pin through a pull-up resistor to VCCIO_HPS. For more information of the pull-up resistor value, refer to the NAND flash specification.			
NAND_CE_N	NAND Chip Enable. This is an active-low signal.	Output	HPS_IOA_15	HPS_IOB_15
NAND_ADQ8	NAND Data Bit 8	I/O	HPS_IOA_17	HPS_IOB_17
NAND_ADQ9	NAND Data Bit 9	I/O	HPS_IOA_18	HPS_IOB_18
NAND_ADQ10	NAND Data Bit 10	I/O	HPS_IOA_19	HPS_IOB_19
NAND_ADQ11	NAND Data Bit 11	I/O	HPS_IOA_20	HPS_IOB_20
NAND_ADQ12	NAND Data Bit 12	I/O	HPS_IOA_21	HPS_IOB_21
NAND_ADQ13	NAND Data Bit 13	I/O	HPS_IOA_22	HPS_IOB_22
NAND_ADQ14	NAND Data Bit 14	I/O	HPS_IOA_23	HPS_IOB_23
NAND_ADQ15	NAND Data Bit 15	I/O	HPS_IOA_24	HPS_IOB_24

1.7.7. HPS USB Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 28. HPS USB Pins

There are two USB controllers (USB0 and USB1) for the Intel Agilex 7 HPS.

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
USB0_CLK	USB0 Clock	Input	HPS_IOA_1
USB0_STP	USB0 Stop Data	Output	HPS_IOA_2
USB0_DIR	USB0 Direction	Input	HPS_IOA_3
USB0_DATA0	USB0 Data Bit 0	I/O	HPS_IOA_4
USB0_DATA1	USB0 Data Bit 1	I/O	HPS_IOA_5
USB0_NXT	USB0 Next Data	Input	HPS_IOA_6
USB0_DATA2	USB0 Data Bit 2	I/O	HPS_IOA_7
USB0_DATA3	USB0 Data Bit 3	I/O	HPS_IOA_8
USB0_DATA4	USB0 Data Bit 4	I/O	HPS_IOA_9
USB0_DATA5	USB0 Data Bit 5	I/O	HPS_IOA_10
USB0_DATA6	USB0 Data Bit 6	I/O	HPS_IOA_11
USB0_DATA7	USB0 Data Bit 7	I/O	HPS_IOA_12
USB1_CLK	USB1 Clock	Input	HPS_IOA_13
USB1_STP	USB1 Stop Data	Output	HPS_IOA_14
USB1_DIR	USB1 Direction	Input	HPS_IOA_15
USB1_DATA0	USB1 Data Bit 0	I/O	HPS_IOA_16
USB1_DATA1	USB1 Data Bit 1	I/O	HPS_IOA_17
USB1_NXT	USB1 Next Data	Input	HPS_IOA_18
USB1_DATA2	USB1 Data Bit 2	I/O	HPS_IOA_19
USB1_DATA3	USB1 Data Bit 3	I/O	HPS_IOA_20
USB1_DATA4	USB1 Data Bit 4	I/O	HPS_IOA_21

continued...

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
USB1_DATA5	USB1 Data Bit 5	I/O	HPS_IOA_22
USB1_DATA6	USB1 Data Bit 6	I/O	HPS_IOA_23
USB1_DATA7	USB1 Data Bit 7	I/O	HPS_IOA_24

1.7.8. HPS EMAC Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 29. HPS EMAC Pins

There are three EMAC controllers (EMAC0, EMAC1, and EMAC2) for the Intel Agilex 7 HPS.

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
EMAC0_TX_CLK	EMAC0 Transmit Clock	Output	HPS_IOA_13
EMAC0_TX_CTL	EMAC0 Transmit Control	Output	HPS_IOA_14
EMAC0_RX_CLK	EMAC0 Receive Clock	Input	HPS_IOA_15
EMAC0_RX_CTL	EMAC0 Receive Control	Input	HPS_IOA_16
EMAC0_TXD0	EMAC0 Transmit Data Bit 0	Output	HPS_IOA_17
EMAC0_TXD1	EMAC0 Transmit Data Bit 1	Output	HPS_IOA_18
EMAC0_RXD0	EMAC0 Receive Data Bit 0	Input	HPS_IOA_19
EMAC0_RXD1	EMAC0 Receive Data Bit 1	Input	HPS_IOA_20
EMAC0_TXD2	EMAC0 Transmit Data Bit 2	Output	HPS_IOA_21
EMAC0_TXD3	EMAC0 Transmit Data Bit 3	Output	HPS_IOA_22
EMAC0_RXD2	EMAC0 Receive Data Bit 2	Input	HPS_IOA_23

continued...

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
EMAC0_RXD3	EMAC0 Receive Data Bit 3	Input	HPS_IOA_24
EMAC1_TX_CLK	EMAC1 Transmit Clock	Output	HPS_IOB_1
EMAC1_TX_CTL	EMAC1 Transmit Control	Output	HPS_IOB_2
EMAC1_RX_CLK	EMAC1 Receive Clock	Input	HPS_IOB_3
EMAC1_RX_CTL	EMAC1 Receive Control.	Input	HPS_IOB_4
EMAC1_TXD0	EMAC1 Transmit Data Bit 0	Output	HPS_IOB_5
EMAC1_TXD1	EMAC1 Transmit Data Bit 1	Output	HPS_IOB_6
EMAC1_RXD0	EMAC1 Receive Data Bit 0	Input	HPS_IOB_7
EMAC1_RXD1	EMAC1 Receive Data Bit 1	Input	HPS_IOB_8
EMAC1_TXD2	EMAC1 Transmit Data Bit 2	Output	HPS_IOB_9
EMAC1_TXD3	EMAC1 Transmit Data Bit 3	Output	HPS_IOB_10
EMAC1_RXD2	EMAC1 Receive Data Bit 2	Input	HPS_IOB_11
EMAC1_RXD3	EMAC1 Receive Data Bit 3	Input	HPS_IOB_12
EMAC2_TX_CLK	EMAC2 Transmit Clock	Output	HPS_IOB_13
EMAC2_TX_CTL	EMAC2 Transmit Control	Output	HPS_IOB_14
EMAC2_RX_CLK	EMAC2 Receive Clock	Input	HPS_IOB_15
EMAC2_RX_CTL	EMAC2 Receive Control	Input	HPS_IOB_16
EMAC2_TXD0	EMAC2 Transmit Data Bit 0	Output	HPS_IOB_17
EMAC2_TXD1	EMAC2 Transmit Data Bit 1	Output	HPS_IOB_18
EMAC2_RXD0	EMAC2 Receive Data Bit 0	Input	HPS_IOB_19
EMAC2_RXD1	EMAC2 Receive Data Bit 1	Input	HPS_IOB_20
EMAC2_TXD2	EMAC2 Transmit Data Bit 2	Output	HPS_IOB_21

continued...

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
EMAC2_TXD3	EMAC2 Transmit Data Bit 3	Output	HPS_IOB_22
EMAC2_RXD2	EMAC2 Receive Data Bit 2	Input	HPS_IOB_23
EMAC2_RXD3	EMAC2 Receive Data Bit 3	Input	HPS_IOB_24

1.7.9. HPS I2C_EMAC and MDIO Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

There are three sets of I2C_EMAC interfaces that can be used as I2C interfaces or as the MDIO pins for the EMACs. Please take note that the I2C_EMAC and MDIO modules must be used with the corresponding EMAC interfaces. For example, you can use either I2C_EMAC0_SDA and I2C_EMAC0_SCL or MDIO0_MDIO and MDIO0_MDC with EMAC0.

The I2C protocol requires pull-up resistors to VCCIO_HPS on both the serial data and serial clock signals for them to function correctly. The value of the pull-up resistor varies depending on your board loading, but it is typically 4.7-kΩ or lower.

Typically the MDIO pin requires an external pull-up resistor to VCCIO_HPS in the range of 1.0-kΩ to 4.7-kΩ.

Table 30. HPS I2C_EMAC and MDIO Pins

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the groups)		
			Group 1	Group 2	Group 3
I2C_EMAC2_SDA	I2C EMAC2 Serial Data	I/O	HPS_IOA_7	HPS_IOB_9	HPS_IOB_21
I2C_EMAC2_SCL	I2C EMAC2 Serial Clock	I/O	HPS_IOA_8	HPS_IOB_10	HPS_IOB_22
I2C_EMAC1_SDA	I2C EMAC1 Serial Data	I/O	HPS_IOA_9	HPS_IOB_19	—
I2C_EMAC1_SCL	I2C EMAC1 Serial Clock	I/O	HPS_IOA_10	HPS_IOB_20	—
I2C_EMAC0_SDA	I2C EMAC0 Serial Data	I/O	HPS_IOA_11	HPS_IOB_11	HPS_IOB_23
I2C_EMAC0_SCL	I2C EMAC0 Serial Clock	I/O	HPS_IOA_12	HPS_IOB_12	HPS_IOB_24

continued...

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the groups)		
			Group 1	Group 2	Group 3
MDIO2_MDIO	EMAC2 MDIO	I/O	HPS_IOA_7	HPS_IOB_9	—
MDIO2_MDC	EMAC2 MDC	Output	HPS_IOA_8	HPS_IOB_10	—
MDIO1_MDIO	EMAC1 MDIO	I/O	HPS_IOA_9	HPS_IOB_19	—
MDIO1_MDC	EMAC1 MDC	Output	HPS_IOA_10	HPS_IOB_20	—
MDIO0_MDIO	EMAC0 MDIO	I/O	HPS_IOA_11	HPS_IOB_11	HPS_IOB_23
MDIO0_MDC	EMAC0 MDC	Output	HPS_IOA_12	HPS_IOB_12	HPS_IOB_24

1.7.10. HPS I2C Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

In addition to the three I2C_EMAC controllers, there are two additional I2C controllers (I2C0 and I2C1) for dedicated I2C usage in the Intel Agilex 7 HPS.

The I2C protocol requires pull-up resistors to VCCIO_HPS on both the serial data and serial clock signals for them to function correctly. The value of the pull-up resistor varies depending on your board loading, but it is typically 4.7-kΩ or lower.

Table 31. HPS I2C Pins

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the groups)			
			Group 1	Group 2	Group 3	Group 4
I2C0 _SDA	I2C0 Serial Data	I/O	HPS_IOA_5	HPS_IOA_23	HPS_IOB_3	—
I2C0 _SCL	I2C0 Serial Clock	I/O	HPS_IOA_6	HPS_IOA_24	HPS_IOB_4	—
I2C1 _SDA	I2C1 Serial Data	I/O	HPS_IOA_3	HPS_IOA_21	HPS_IOB_7	HPS_IOB_13
I2C1 _SCL	I2C1 Serial Clock	I/O	HPS_IOA_4	HPS_IOA_22	HPS_IOB_8	HPS_IOB_14

1.7.11. HPS SPI Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 32. HPS SPI Pins

There are two SPI Master (SPIM0 and SPIM1) and two SPI Slave (SPIS0 and SPIS1) controllers for the Intel Agilex 7 HPS.

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the group)		
			Group 1	Group 2	Group 3
SPIM0_CLK	SPIM0 Clock	Output	HPS_IOA_5	HPS_IOB_21	HPS_IOB_21
SPIM0_MOSI	SPIM0 Master Out Slave In	Output	HPS_IOA_6	HPS_IOB_22	HPS_IOB_22
SPIM0_MISO	SPIM0 Master In Slave Out	Input	HPS_IOA_7	HPS_IOB_19	HPS_IOB_23
SPIM0_SS0_N	SPIM0 Slave Select 0 This is an active-low signal.	Output	HPS_IOA_8	HPS_IOB_20	HPS_IOB_24
SPIM0_SS1_N	SPIM0 Slave Select 1 This is an active-low signal.	Output	HPS_IOA_1	HPS_IOB_18	HPS_IOB_18
SPIM1_CLK	SPIM1 Clock	Output	HPS_IOA_9	HPS_IOA_21	HPS_IOB_1
SPIM1_MOSI	SPIM1 Master Out Slave In	Output	HPS_IOA_10	HPS_IOA_22	HPS_IOB_2
SPIM1_MISO	SPIM1 Master In Slave Out	Input	HPS_IOA_11	HPS_IOA_23	HPS_IOB_3
SPIM1_SS0_N	SPIM1 Slave Select 0 This is an active-low signal.	Output	HPS_IOA_12	HPS_IOA_24	HPS_IOB_4
SPIM1_SS1_N	SPIM1 Slave Select 1 This is an active-low signal.	Output	HPS_IOA_2	HPS_IOA_20	HPS_IOB_5
SPIS0_CLK	SPIS0 Clock	Input	HPS_IOA_1	HPS_IOA_21	HPS_IOB_9
SPIS0_MOSI	SPIS0 Master Out Slave In	Input	HPS_IOA_2	HPS_IOA_22	HPS_IOB_10

continued...

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the group)		
			Group 1	Group 2	Group 3
SPIS0_MISO	SPIS0 Master In Slave Out	Output	HPS_IOA_4	HPS_IOA_24	HPS_IOB_12
SPIS0_SS0_N	SPIS0 Slave Select 0 This is an active-low signal.	Input	HPS_IOA_3	HPS_IOA_23	HPS_IOB_11
SPIS1_CLK	SPIS1 Clock	Input	HPS_IOA_9	HPS_IOB_5	HPS_IOB_21
SPIS1_MOSI	SPIS1 Master Out Slave In	Input	HPS_IOA_10	HPS_IOB_6	HPS_IOB_22
SPIS1_MISO	SPIS1 Master In Slave Out	Output	HPS_IOA_12	HPS_IOB_8	HPS_IOB_24
SPIS1_SS0_N	SPIS1 Slave Select 0 This is an active-low signal.	Input	HPS_IOA_11	HPS_IOB_7	HPS_IOB_23

1.7.12. HPS UART Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 33. HPS UART Pins

There are two UART (UART0 and UART1) controllers for the Intel Agilex 7 HPS.

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the groups)		
			Group 1	Group 2	Group 3
UART0_CTS_N	UART0 Clear to Send This is an active-low signal.	Input	HPS_IOA_1	HPS_IOA_21	HPS_IOB_1
UART0_RTS_N	UART0 Request to Send This is an active-low signal.	Output	HPS_IOA_2	HPS_IOA_22	HPS_IOB_2
UART0_TX	UART0 Transmit	Output	HPS_IOA_3	HPS_IOA_23	HPS_IOB_3

continued...

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments (select from one of the groups)		
			Group 1	Group 2	Group 3
UART0_RX	UART0 Receive	Input	HPS_IOA_4	HPS_IOA_24	HPS_IOB_4
UART1_CTS_N	UART1 Clear to Send This is an active-low signal.	Input	HPS_IOA_5	HPS_IOB_5	HPS_IOB_17
UART1_RTS_N	UART1 Request to Send This is an active-low signal.	Output	HPS_IOA_6	HPS_IOB_6	HPS_IOB_18
UART1_TX	UART1 Transmit	Output	HPS_IOA_7	HPS_IOB_7	HPS_IOB_15
UART1_RX	UART1 Receive	Input	HPS_IOA_8	HPS_IOB_8	HPS_IOB_16

1.7.13. HPS Trace Pins

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Table 34. HPS Trace Pins

You can select up to 16 trace output pins in the Intel Agilex 7 HPS. These pins do not have to be located in the same quadrant.

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
Trace_CLK	Trace Clock	Output	HPS_IOA_20
			HPS_IOB_20
Trace_D0	Trace Data 0	Output	HPS_IOA_21
			HPS_IOB_21
Trace_D1	Trace Data 1	Output	HPS_IOA_22
			HPS_IOB_22
Trace_D2	Trace Data 2	Output	HPS_IOA_23

continued...

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
			HPS_IOB_23
Trace_D3	Trace Data 3	Output	HPS_IOA_24
			HPS_IOB_24
Trace_D4	Trace Data 4	Output	HPS_IOA_19
			HPS_IOA_7
			HPS_IOB_19
			HPS_IOB_7
Trace_D5	Trace Data 5	Output	HPS_IOA_18
			HPS_IOA_6
			HPS_IOB_18
			HPS_IOB_6
Trace_D6	Trace Data 6	Output	HPS_IOA_17
			HPS_IOA_5
			HPS_IOB_17
			HPS_IOB_5
Trace_D7	Trace Data 7	Output	HPS_IOA_16
			HPS_IOA_4
			HPS_IOB_16
			HPS_IOB_4
Trace_D8	Trace Data 8	Output	HPS_IOA_15
			HPS_IOA_3
			HPS_IOB_15
			HPS_IOB_3
Trace_D9	Trace Data 9	Output	HPS_IOA_14

continued...

HPS Pin Function	Pin Description and Connection Guidelines	Pin Type	Valid Assignments
			HPS_IOA_2
			HPS_IOB_14
			HPS_IOB_2
Trace_D10	Trace Data 10	Output	HPS_IOA_13
			HPS_IOA_1
			HPS_IOB_13
			HPS_IOB_1
Trace_D11	Trace Data 11	Output	HPS_IOA_12
			HPS_IOB_12
Trace_D12	Trace Data 12	Output	HPS_IOA_11
			HPS_IOB_11
Trace_D13	Trace Data 13	Output	HPS_IOA_10
			HPS_IOB_10
Trace_D14	Trace Data 14	Output	HPS_IOA_9
			HPS_IOB_9
Trace_D15	Trace Data 15	Output	HPS_IOA_8
			HPS_IOB_8

1.8. Intel Agilex 7 Power Supply Sharing Guidelines

Intel Agilex 7 devices have specific power-up and power-down sequence requirements. For more information, refer to the *Intel Agilex 7 Power Management User Guide*.

Note: Intel recommends you to generate a **.pin** file from the Intel Quartus Prime Fitter to verify power pin assignment. Intel also recommends using this **.pin** file to determine if it is safe to power down or ground certain power supplies for your specific design. This step will inform you to make the appropriate design choices for unused power supplies for your design.

Related Information

Intel Agilex 7 Power Management User Guide

1.8.1. Example 1—Intel Agilex 7 Devices (P-Tile and E-Tile)

Table 35. Power Supply Sharing Guidelines for Intel Agilex 7 Devices with P-Tile and E-Tile Transceivers

Example Requiring 8 Power Regulators

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	SmartVID(1), 0.8	± 3%	Switcher(2)	Share	Source VCC and VCCP from the same regulator, sharing the same voltage plane. You have the option to connect VCCL_HPS to the same regulator as VCC and VCCP when the power rails require the same voltage level. You may also connect the VCCPLLDIG_HPS power to the shared VCC, VCCP, and VCCL_HPS power planes with proper isolation filtering. For -4X devices, VCC and VCCP are powered by SmartVID and a separate fixed 0.8V supply must be used for VCCL_HPS and filtered VCCPLLDIG_HPS. When implementing a filtered supply topology, you must consider the IR drop across the filter. If you do not intend to utilize the HPS in the Intel Agilex 7 device, you must still provide power to these power supply pins. Do not leave the VCCL_HPS and VCCPLLDIG_HPS power supply pins floating or connected to GND.
VCCP					Share	
VCCL_HPS					Share	
VCCPLLDIG_HPS					Filter	
VCCH	2	0.9	± 30 mV	Switcher(2)	Share	Connect the VCCH to a dedicated 0.9-V power supply.
VCC_HSSI_GXE					Share	

continued...

(1) For the SmartVID voltage range, refer to the *Intel Agilex 7 FPGAs and SoCs Device Data Sheet: F-Series and I-Series* .

(2) When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined in note 4 of the *Notes to Intel Agilex 7 Pin Connection Guidelines*.

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCCFUSE_GXP					Share	When implementing a filtered supply topology, you must consider the IR drop across the filter.
VCC_HSSI_GXP[L]					Share	
VCCH_SDM					Share	
VCCRT_GXE					LC Filter	
VCCRTPLL_GXE					Filter	
VCCRT_GXP					Filter	
VCCL_SDM	3	0.8	± 3%	Switcher(2)	Share	Connect the VCCL_SDM to a dedicated 0.8-V power supply. When implementing a filtered supply topology, you must consider the IR drop across the filter.
VCCPLLDIG_SDM					Filter	
VCCH_GXE	4	1.1	± 3%	Switcher(2)	Isolate	Connect the VCCH_GXE to a dedicated 1.1-V power supply.
VCCCLK_GXE	5	2.5	± 5%	Switcher(2)	Isolate	Connect the VCCCLK_GXE to a dedicated 2.5-V power supply.
VCCPT	6	1.8	± 3%	Switcher(2)	Share	Connect VCCPT to a dedicated 1.8-V power supply. Connect VCCADC, VCCPLL_SDM, VCCPLL_HPS, and VCCCLK_GXP to the same power plane with proper isolation filtering. Depending on the regulator capabilities, you have the option to share this supply with multiple Intel Agilex 7 devices. If you do not intend to utilize the HPS in the Intel Agilex 7 device, you must still provide power to the HPS power supply pins. When implementing a filtered supply topology, you must consider the IR drop across the filter.
VCCADC					Filter	
VCCPLL_SDM						
VCCPLL_HPS						
VCCCLK_GXP					Filter	
VCCH_GXP					Filter	
VCCRCORE	7	1.2	± 5%	Switcher(2)	Share	Connect the VCCRCORE to 1.2-V power supply. Connect VCCIO_PIO and VCCIO_PIO_SDM to dedicated 1.2-V power supply.
VCCIO_PIO(3)						
VCCIO_PIO_SDM						

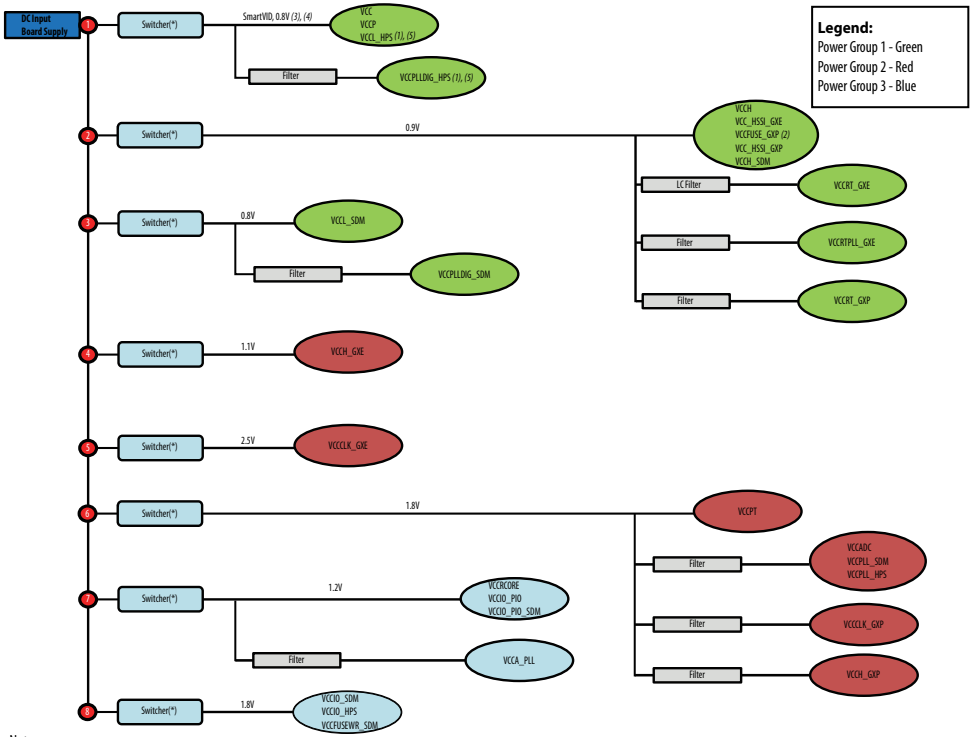
continued...

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCCA_PLL					Filter	Connect VCCA_PLL to the VCCRCORE, VCCIO_PIO, and VCCIO_PIO_SDM supplies with proper isolation filtering.
VCCIO_SDM	8	1.8	± 5%	Switcher(2)	Share	Connect VCCIO_SDM and VCCIO_HPS to dedicated 1.8-V power supply. If you do not intend to utilize the HPS in the Intel Agilex 7 device, you must still provide power to these power supply pins. Do not leave the VCCIO_HPS power supply pins floating or connected to GND.
VCCIO_HPS					Share	
VCCFUSEWR_SDM					Share	A 1.8-V power supply is required on this pin if field-programming of the eFuses is required. If field-programming of the eFuses is not required, tie this pin to VCCIO_SDM or leave it unconnected (floating). Do not tie this pin to GND. If field-programming of the eFuses is required, Intel recommends using an adjustable regulator set to 1.8-V output when programming the eFuses.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Intel Agilex 7 device is provided in Figure 1 on page 67.

(3) The supported tolerance for the VCCIO_PIO power supply varies depending on the I/O standards. For more details, refer to the I/O standard specification in the *Intel Agilex 7 FPGAs and SoCs Device Data Sheet: F-Series and I-Series* . Use the Intel FPGA Power and Thermal Calculator and the Intel Quartus Prime Power Analyzer tool to assist in determining the power required for your specific design.

Figure 1. Example Power Supply Sharing Guidelines for Intel Agilex 7 Devices with P-Tile and E-Tile Transceivers



Notes:
(1) VCCL_HPS and VCCPLLDIG_HPS can run at 0.95V for higher performance. In this case, these voltages need to run from its own dedicated voltage regulator. For more information about the VCCL_HPS power connection, refer to the VCCL_HPS connection guidelines.
(2) VCCFUSE_GXP in this configuration does not support eFuse programming.
(3) When a -V device is used, you must enable the SmartVID connection between the device and the VCC voltage regulator. For more information, refer to the connection guidelines of the PWRMGT_SCL and PWRMGT_SDA pin functions.
(4) When selecting a voltage regulator controller for SmartVID operation, you must choose a controller with the PMBus capability, a feedback node, and a selectable VID format. For example, 4 to 6 bits pattern.
(5) For -4X devices, VCC and VCCP are powered by SmartVID and a separate fixed 0.8V supply must be used for VCCL_HPS and filtered VCCPLLDIG_HPS.

Related Information

Intel Agilex 7 FPGAs and SoCs Device Data Sheet: F-Series and I-Series

1.8.2. Example 2—Intel Agilex 7 Devices (F-Tile and R-Tile)

Table 36. Power Supply Sharing Guidelines for Intel Agilex 7 Devices with F-Tile and R-Tile Transceivers

Example Requiring 12 Power Regulators

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	SmartVID(4), 0.8	± 3%	Switcher(5)	Share	Source VCC and VCCP from the same regulator, sharing the same voltage plane. You have the option to connect VCCL_HPS to the same regulator as VCC and VCCP when the power rails require the same voltage level. You may also connect the VCCPLLDIG_HPS power to the shared VCC, VCCP, and VCCL_HPS power planes with proper isolation filtering. For -4X devices, VCC and VCCP are powered by SmartVID and a separate fixed 0.8V supply must be used for VCCL_HPS and filtered VCCPLLDIG_HPS. When implementing a filtered supply topology, you must consider the IR drop across the filter. If you do not intend to utilize the HPS in the Intel Agilex 7 device, you must still provide power to these power supply pins. Do not leave the VCCL_HPS and VCCPLLDIG_HPS power supply pins floating or connected to GND.
VCCP						
VCCL_HPS						
VCCPLLDIG_HPS					Filter	
VCCH	2	0.8	± 3%	Switcher(5)	Share	Connect the VCC_HSSI_GXF to a dedicated 0.8-V power supply. When implementing a filtered supply topology, you must consider the IR drop across the filter.
VCC_HSSI_GXF						
VCCL_SDM						
VCCPLLDIG_SDM					Filter	

continued...

(4) For the SmartVID voltage range, refer to the *Intel Agilex 7 FPGAs and SoCs Device Data Sheet: F-Series and I-Series* .

(5) When using a switcher to supply these voltages, the switcher must be a low noise switcher as defined in note 4 of the *Notes to Intel Agilex 7 Pin Connection Guidelines*.

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC_HSSI_GXR	3	0.9	± 3%	Switcher(5)	Share	Connect VCC_HSSI_GXR and VCCH_SDM to a dedicated 0.9-V power supply.
VCCH_SDM(6)						
VCCE_PLL_GXR	4	1.0	± 2%	Linear	Share	Connect to a dedicated 1.0-V reference source.
VCC_DTS_GXR						
VCCERT_FGT_GXF	5	1.0	± 3%	Switcher(5) or Linear	Isolate	Connect to a dedicated 1.0-V power supply.
VCCERT1_FHT_GXF			± 2.5%	Switcher(5) or Linear	Isolate	
VCCERT2_FHT_GXF			± 2.5%	Linear	Isolate	
VCCRT_GXR	6	1.0	± 2.5%	Switcher(5)	Isolate	Connect to a dedicated power supply.
VCCED_GXR	7	0.9	± 3%	Linear	Isolate	Connect to a dedicated 0.9-V power supply.
VCCEHT_FHT_GXF	8	1.5	-2.5% to +2%	Linear	Isolate	Connect to a dedicated 1.5-V power supply.
VCCPT	9	1.8	± 3%	Switcher(5)	Share if 1.8 V	Connect VCCPT to a dedicated 1.8-V power supply. Connect VCCADC, VCCPLL_SDM, VCCPLL_HPS, VCCH_FGT_GXF, and VCCCLK_GXF to the same power plane with proper isolation filtering. Depending on the regulator capabilities, you have the option to share this supply with multiple Intel Agilex 7 devices. If you do not intend to utilize the HPS in the Intel Agilex 7 device, you must still provide power to the HPS power supply pins. When implementing a filtered supply topology, you must consider the IR drop across the filter.
VCCADC		1.8			Filter	
VCCPLL_SDM						
VCCPLL_HPS						
VCCCLK_GXF		1.8			Filter	
VCCH_FGT_GXF		1.8			Filter	
VCCH_GXR		1.8			Filter	

continued...

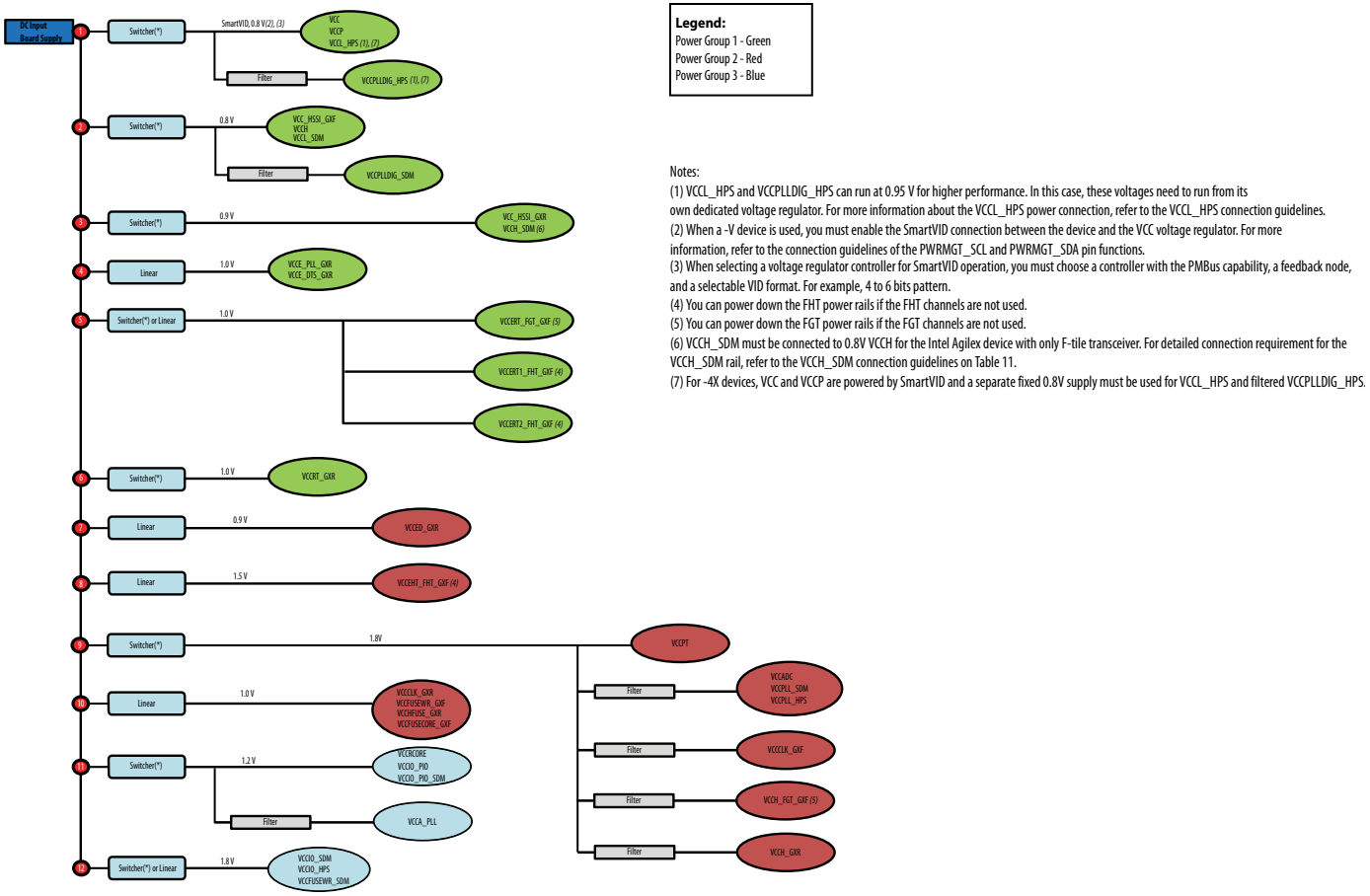
(6) VCCH_SDM must be connected to 0.8 V VCCH for the Intel Agilex 7 device with only F-tile transceiver. For detailed connection requirement for the VCCH_SDM rail, refer to the VCCH_SDM connection guideline on Table 11.

Power Pin Name	Regulator Group	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCCCLK_GXR	10	1.0	± 3%	Linear	Share	Connect to a dedicated 1.0-V power supply.
VCCFUSEWR_GXF						
VCCHFUSE_GXR						
VCCFUSECORE_GXF						
VCCRCORE	11	1.2	± 5%	Switcher(5)	Share	Connect to a dedicated 1.2-V power supply. When implementing a filtered supply topology, you must consider the IR drop across the filter.
VCCIO_PIO						
VCCIO_PIO_SDM						
VCCA_PLL					Filter	
VCCIO_SDM	12	1.8	± 5%Switcher(5) or Linear		Share	Connect VCCIO_SDM and VCCIO_HPS to a dedicated 1.8-V power supply.
VCCIO_HPS						
VCCFUSEWR_SDM					Share	A 1.8-V power supply is required on this pin if field-programming of the eFuses is required. If field-programming of the eFuses is not required, tie this pin to VCCIO_SDM or leave it unconnected (floating). Do not tie this pin to GND. If field-programming of the eFuses is required, Intel recommends using an adjustable regulator set to 1.8-V output when programming the eFuses.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Intel Agilex 7 device is provided in Figure 2 on page 71.

Figure 2. Example Power Supply Sharing Guidelines for Intel Agilex 7 Devices with F-Tile and R-Tile Transceivers

If an Intel Agilex 7 device without R-tile is used, you can ignore the R-tile power rails. If an Intel Agilex 7 device without F-tile is used, you can ignore the F-tile power rails.



Legend:
Power Group 1 - Green
Power Group 2 - Red
Power Group 3 - Blue

Notes:
(1) VCCL_HPS and VCCPLLDIG_HPS can run at 0.95 V for higher performance. In this case, these voltages need to run from its own dedicated voltage regulator. For more information about the VCCL_HPS power connection, refer to the VCCL_HPS connection guidelines.
(2) When a -V device is used, you must enable the SmartVID connection between the device and the VCC voltage regulator. For more information, refer to the connection guidelines of the PWRMGT_SCL and PWRMGT_SDA pin functions.
(3) When selecting a voltage regulator controller for SmartVID operation, you must choose a controller with the PMBus capability, a feedback node, and a selectable VID format. For example, 4 to 6 bits pattern.
(4) You can power down the FHT power rails if the FHT channels are not used.
(5) You can power down the FGT power rails if the FGT channels are not used.
(6) VCCH_SDM must be connected to 0.8V VCCH for the Intel Agilex device with only F-tile transceiver. For detailed connection requirement for the VCCH_SDM rail, refer to the VCCH_SDM connection guidelines on Table 11.
(7) For -4X devices, VCC and VCCP are powered by SmartVID and a separate fixed 0.8V supply must be used for VCCL_HPS and filtered VCCPLLDIG_HPS.

1.9. Notes to Intel Agilex 7 Device Family Pin Connection Guidelines

Note: Intel recommends that you create an Intel Quartus Prime design, enter your device I/O assignments, and compile the design. The Intel Quartus Prime software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Intel provides these guidelines only as recommendations. It is the responsibility of the designer to apply simulation results to the design to verify proper device functionality.

1. Use the Intel FPGA Power and Thermal Calculator to determine the preliminary current requirements for VCC and other power supplies. Use the Intel Quartus Prime Power Analyzer for the most accurate current requirements for this and other power supplies.
2. Power pins should not share breakout vias from the BGA. Each ball on the BGA needs to have its own dedicated breakout via. VCC must not share breakout vias.
3. For AC-coupled links, the AC-coupling capacitor can be placed anywhere along the channel. PCI Express (PCIe) protocol requires the AC-coupling capacitor to be placed on the transmitter side of the interface that permits adapters to be plugged and unplugged.
4. Low Noise Switching Regulator—defined as a switching regulator circuit encapsulated in a thin surface mount package containing the switch controller, power FETs, inductor, and other support components. The switching frequency is usually between 800 kHz and 1 MHz and has fast transient response. The switching frequency range is not an Intel requirement.
5. There are no dedicated PR_REQUEST, PR_ERROR, and PR_DONE pins. If required, you can use user I/O pins for these functions.
6. The device orientation is die view (bottom of chip view).
7. All I/O pins in a GPIO bank are configured as tri-stated with weak pull-up enabled during device power up (after VCC is fully powered up) and device configuration. During device power down, the I/O pin signals are measured between GND to VCCIO_PIO voltage level when the VCCIO_PIO and VCC power rails are powering down. All valid data transaction should start after the device enter user mode.

8. All dedicated configuration/JTAG, SDM, and SDM optional signal pins are in the undetermined state during device power up and power down. All I/O in the SDM pins are configured as defined in the *Intel Agilex 7 General-Purpose I/O User Guide: F-Series and I-Series* during device configuration.
9. All I/O pins in HPS banks are in the undetermined state during device power up and power down. All I/O in the HPS pins are configured as the Schmitt trigger input with 20-kΩ weak pull-up enabled after the device is powered up and during HPS or device configuration. All HPS data transaction should start after the device is fully powered up.
10. Input signals of all GPIO, HPS, and SDM I/O pins at any point during power up and power down should not exceed the I/O buffer power supply rail of the bank where the I/O pin resides in. If you use a pin in a GPIO bank with 1.5V VCCIO_PIO, the pin voltage must not exceed the VCCIO_PIO rail or 1.2V, whichever is lower.

Related Information

- Intel Agilex 7 Power Supply Sharing Guidelines on page 63
- Intel FPGA Power and Thermal Calculator User Guide
- Intel Agilex 7 General-Purpose I/O User Guide: F-Series and I-Series

1.10. Document Revision History for the Intel Agilex 7 Device Family Pin Connection Guidelines

Document Version	Changes
2023.04.03	• Added a footnote for the VCCH_SDM pin in Table: *Power Supply Sharing Guidelines for Intel Agilex 7 Devices with F-Tile and R-Tile Transceivers*. • Updated the *HPS_COLD_nRESET* signal description in Table: *SDM Optional Signal Pins*. • Updated the connection guidelines of the VCCH pin. • Updated the connection guidelines of the FGT[L,R]_RX_Q[0,1,2,3]_CH[0,1,2,3]P and FGT[L,R]_RX_Q[0,1,2,3]_CH[0,1,2,3]N pins. • Updated the connection guidelines of the VCCERT1_FHT_GXF[L,R] and VCCERT2_FHT_GXF[L,R] pins. • Updated Table: *Power Supply Sharing Guidelines for Intel Agilex 7 Devices with P-Tile and E-Tile Transceivers* and Table: *Power Supply Sharing Guidelines for Intel Agilex 7 Devices with F-Tile and R-Tile Transceivers* to combine the VCCFUSEWR_SDM with VCCIO_SDM and VCCIO_HPS rails.

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Document Version	Changes
	• Updated Table: *Power Supply Sharing Guidelines for Intel Agilex 7 Devices with F-Tile and R-Tile Transceivers* to combine the VCCERT_FGT_GXF with VCCERT1_FHT_GXF and VCCERT2_FHT_GXF rails. • Updated Figure: *Example Power Supply Sharing Guidelines for Intel Agilex 7 Devices with P-Tile and E-Tile Transceivers* and Figure: *Example Power Supply Sharing Guidelines for Intel Agilex 7 Devices with F-Tile and R-Tile Transceivers* to combine the VCCFUSEWR_SDM with VCCIO_SDM and VCCIO_HPS rails. • Updated Figure: *Example Power Supply Sharing Guidelines for Intel Agilex 7 Devices with F-Tile and R-Tile Transceivers* to combine the VCCERT_FGT_GXF with VCCERT1_FHT_GXF and VCCERT2_FHT_GXF rails.
2023.02.28	• Updated the pin description of the VCCRCORE pin. • Updated the connection guidelines of the VCCHFUSE_GXR[L,R] pins.
2023.02.20	• Updated the *R-Tile Transceiver Pins* section to include guidelines for the Intel Agilex™ 7 AGI041 device. • Updated the VCCFUSEWR_SDM notes in the following tables: — Table: *Power Supply Sharing Guidelines for Intel Agilex 7 Devices with P-Tile and E-Tile Transceivers* — Table: *Power Supply Sharing Guidelines for Intel Agilex 7 Devices with F-Tile and R-Tile Transceivers* • Updated product family name to "Intel Agilex 7". • Retitled the document from *Intel Agilex Device Family Pin Connection Guidelines* to *Intel Agilex 7 Device Family Pin Connection Guidelines*.
2022.09.22	• Updated the connection guidelines of the VCCBAT pin. • Updated the connection guidelines of the VCCL_HPS pin.
2022.09.06	Updated the connection guidelines of the VCCRCORE pin.
2022.07.20	Updated the *Optional/Dual-Purpose Configuration Pins* section.
2022.06.21	• Updated the connection guidelines of the VCCIO_PIO[3][A,B,C,D,E,F] pins. • Updated the connection guidelines of the REFCLK_GXP[L10A,L10C]_CH[0,2][p,n] pins. • Updated the connection guidelines of the I_PIN_PERST_N_GXF pin. • Updated the VCCL_HPS power supply voltage for the –4X and –4F speed grades in the connection guidelines of the VCCL_HPS pin. • Updated the following tables to include details on the –4X speed grade device for the VCCL_HPS and VCCPLLDIG_HPS: — Table: *Power Supply Sharing Guidelines for Intel Agilex Devices with P-Tile and E-Tile Transceivers*. — Table: *Power Supply Sharing Guidelines for Intel Agilex Devices with F-Tile and R-Tile Transceivers*. • Added note (5) in Figure: *Example Power Supply Sharing Guidelines for Intel Agilex Devices with P-Tile and E-Tile Transceivers*. • Updated note (6) and added note (7) in Figure: *Example Power Supply Sharing Guidelines for Intel Agilex Devices with F-Tile and R-Tile Transceivers*.
2022.04.20	Updated the connection guidelines of the REFCLK_FGT[L,R]_Q[2,3]_CH[8,9]P and REFCLK_FGT[L,R]_Q[2,3]_CH[8,9]N pins.

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Document Version	Changes
2022.04.15	• Updated the connection guidelines of the VCCBAT pin. • Removed the V_{CCBAT} power supply from the following examples: — Example 1—*Power Supply Sharing Guidelines for Intel Agilex Devices with P-Tile and E-Tile Transceivers* — Example 2—*Power Supply Sharing Guidelines for Intel Agilex Devices with F-Tile and R-Tile Transceivers*
2022.01.14	Updated the pin description and connection guidelines of the NAND_RB pin.
2021.11.08	• Added the *Pins Status for Intel Agilex Devices* section. • Updated the bank indexing of the following pins: — CLK_[T,B]_2[A,B,C,D,E,F]_[0:1][p,n] — CLK_[T,B]_3[A,B,C,D,E,F]_[0:1][p,n] — PLL_[2][A,B,C,D,E,F]_[T,B]_FB[0:1] — PLL_[3][A,B,C,D,E,F]_[T,B]_FB[0:1] — PLL_[2][A,B,C,D,E,F]_[T,B]_CLKOUT[0:1][p,n] — PLL_[3][A,B,C,D,E,F]_[T,B]_CLKOUT[0:1][p,n] — DIFF_RX[2][A,B,C,D,E,F][1:24][p,n] — DIFF_RX[3][A,B,C,D,E,F][1:24][p,n] — DIFF_TX[2][A,B,C,D,E,F][1:24][p,n] — DIFF_TX[3][A,B,C,D,E,F][1:24][p,n] • Updated the pin description of the following pins: — CLK_[T,B]_2[A,B,C,D,E,F]_[0:1][p,n] — CLK_[T,B]_3[A,B,C,D,E,F]_[0:1][p,n] — PLL_[2][A,B,C,D,E,F]_[T,B]_FB[0:1] — PLL_[3][A,B,C,D,E,F]_[T,B]_FB[0:1] — PLL_[2][A,B,C,D,E,F]_[T,B]_CLKOUT[0:1][p,n] — PLL_[3][A,B,C,D,E,F]_[T,B]_CLKOUT[0:1][p,n] — DIFF_RX[2][A,B,C,D,E,F][1:24][p,n] — DIFF_RX[3][A,B,C,D,E,F][1:24][p,n] — DIFF_TX[2][A,B,C,D,E,F][1:24][p,n] — DIFF_TX[3][A,B,C,D,E,F][1:24][p,n] — AVST_DATA[31:0] — AVST_READY(3A bank) — AVST_CLK(3A bank) — AVST_VALID(3A bank) • Updated the connection guidelines of the TCK pin.

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Document Version	Changes
	• Updated the pin description of the nSTATUS pin. • Updated the pin description and connection guidelines of the TEMPDIODE[1,3,4,6][p,n] pins. • Updated the connection guidelines of the VCCH_SDM pin. • Updated the connection guidelines of the VCCFUSEWR_SDM pin. • Updated the connection guidelines of the REFCLK_GXE[R9A]_CH[0:8][p,n] pins. • Updated the connection guidelines of the VCCH_GXP[L1,R1] pins. • Updated the SDM_IO pins in the AVST x16 configuration scheme for the CONF_DONE and INIT_DONE signals in Table: *SDM Optional Signal Pins*. • Updated the SDM_IO pins in the AVST x4, AVST x8, and AVST x32 configuration schemes for the nCATTRIP signal in Table: *SDM Optional Signal Pins*. • Updated the VCCRCORE pin name. • Updated the following pin names: — RCOMP_P_FHT_GXF — RCOMP_N_FHT_GXF — RCOMP_P_Q2_CH1_FGT_GXF — RCOMP_N_Q2_CH1_FGT_GXF • Updated Figure: *Example Power Supply Sharing Guidelines for Intel Agilex Devices with F-Tile and R-Tile Transceivers* to include a note for the VCCH_SDM rail. • Removed the *Appendix* section.
2021.10.29	• Added note to the *PWRMGT_SCL*, *PWRMGT_SDA*, and *PWRMGT_ALERT* signals in Table: *SDM Optional Signal Pins*. • Added new notes in the *Notes to Intel Agilex Device Family Pin Connection Guidelines* section.
2021.07.02	• Added the nCATTRIP signal to Table: *SDM Optional Signal Pins*. • Updated the connection guidelines of the VSIGP_[0,1] and VSIGN_[0,1] pins. • Updated the connection guidelines of the REFCLK_GXE(L8,R9)_CH[0:8][p,n] pins.
2021.06.02	• Updated the IO_AUX_RREF(10,12,20,22), IO_AUX_RREF[10,12,20,22]_P, and U[10,12,20]_P_IO_RESREF_0 pin names. • Updated the pin description of the IO_AUX_RREF(10,12,20,22), IO_AUX_RREF[10,12,20,22]_P, and U[10,12,20]_P_IO_RESREF_0 pins. • Updated the connection guidelines of the VCCH_SDM pin. • Updated the connection guidelines of the VCCH_FGT_GXF[L,R] and VCCERT_FGT_GXF[L,R] pins. • Updated the connection guidelines of the I_PIN_PERST_N_GXF pin. • Updated the supply tolerances of the VCCEHT_FHT_GXF and VCCERT_FGT_GXF pins in Table: *Power Supply Sharing Guidelines for Intel Agilex Devices with F-Tile and R-Tile Transceivers* . • Updated the VCCIO_PIO and VCCIO_PIO_SDM power rails in the following examples: — Example 1—*Power Supply Sharing Guidelines for Intel Agilex Devices with P-Tile and E-Tile Transceivers* — Example 2—*Power Supply Sharing Guidelines for Intel Agilex Devices with F-Tile and R-Tile Transceivers* • Removed the pin description and connection guidelines of the IO_PLL_REFCLK_[12A,12C,13A,13C]_GXF pins. • Removed F-series and I-series references.

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Document Version	Changes
2021.03.23	• Added the following sections: — *Intel Agilex F-Tile Pins* — *Intel Agilex R-Tile Pins* — *Appendix* • Updated Table: *SDM Pins* to include AS_nRST information for the SDM_IO15 pin. • Updated the connection guidelines for the following pins in Table: *Power Supply Pins*: — VCCIO_PIO_SDM — VCCPT — VCCR_CORE — VCCH — VCCIO_PIO[2][A,B,C,D] and VCCIO_PIO[3][A,B,C,D] • Updated the connection guidelines for the VCC_HSSI_GXE(L1,R1) pins in Table: *E-Tile Pins*. • Updated the LC filter reference for the VCCRT_GXE(L1,R1) pins to *AN 910: Intel Agilex Power Distribution Network Design Guidelines*. • Updated the pin descriptions for the following pins in Table: *P-Tile Pins*: — GXP[L10A,R11A]_RX_CH[19:0][p,n] — GXP[L10A,R11A]_TX_CH[19:0][p,n] — REFCLK_GXP[L10A,R11A]_CH[0,2][p,n] • Updated Figure: *Example Power Supply Sharing Guidelines for Intel Agilex F-Series Devices with P-Tile and E-Tile Transceivers*. • Updated note (1) to add reference for the VCCL_HPS connection guidelines in the following figures: — *Power Supply Sharing Guidelines for Intel Agilex F-Series Devices with P-Tile and E-Tile Transceivers* — *Power Supply Sharing Guidelines for Intel Agilex I-Series Devices with F-Tile and R-Tile Transceivers* — *Power Supply Sharing Guidelines for Intel Agilex ES Device (2486A)* • Removed the following sections: — *Intel Agilex H-Tile Pins* — *Example 2—Intel Agilex (P-Tile and H-Tile)* • Removed SDM_IO15 from ASx4 configuration scheme for the following signals in Table: *SDM Optional Signal Pins*: — CONF_DONE — INIT_DONE — CvP_CONFDONE — SEU_ERROR — HPS_COLD_nRESET — Direct to Factory Image

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Document Version	Changes
2020.12.03	• Added the *Intel Agilex H-Tile Pins* section. • Added the following power supply sharing guidelines: — *Example 2—Intel Agilex (P-Tile and H-Tile)* • Updated topic title *Example 1—Intel Agilex* to *Example 1—Intel Agilex (P-Tile and E-Tile)* for clarity. • Updated the pin description for nCONFIG in Table: *Dedicated Configuration/JTAG Pins—Preliminary*. • Updated the pin functions for all clock and PLL pins in Table: *Clock and PLL Pins—Preliminary*. • Updated the pin functions and description in Table:*Optional/Dual-Purpose Configuration Pins—Preliminary*. • Updated the pin descriptions for DIFF_RX and DIFF_TX in Table: *Differential I/O Pins—Preliminary*. • Updated Table: *Power Supply Pins—Preliminary*: — Updated the connection guidelines for VCCR_CORE and VCCA_PLL. — Updated the connection guidelines for VCCL_HPS and VCCIO_PIO. — Updated the connection guidelines for VCCIO_PIO[2][A,B,C,D] and VCCIO_PIO[3][A,B,C,D]. — Updated the pin description for VCCADC • Updated the connection guidelines for VREFP_ADC, VREFN_ADC, VSIGP_[0,1], and VSIGN_[0,1] in Table: *Voltage Sensor and Voltage Reference Pins—Preliminary*. • Updated Table: *E-Tile Pins—Preliminary*: — Updated the supported I/O standards for GXE(L8,R9)_RX_CH[0:23][p,n] and GXE(L8,R9)_TX_CH[0:23][p,n] from CML –56G PAM4 and 30G NRZ to 57.8G PAM4 and 28.9G NRZ. — Updated the pin description and connection guidelines of the REFCLK_GXE(L8,R9)(A,B,C)_CH[0:8][p,n] pins. • Added a note in the *P-Tile Pins* section to include details on the lane reversal and polarity inversion on the PCB. • Updated Table: *HPS Supply Pins*. • Updated the notes for VCCR_CORE and VCCA_PLL to clarify the VCCR_CORE pin must be tied to a 1.8-V power supply for Intel Agilex ES (2486A package) devices and 1.2-V power supply for Intel Agilex production devices and other Intel Agilex ES (except 2486A package) devices in the following tables and figures: — Table: *Power Supply Sharing Guidelines for Intel Agilex Device with P-Tile and E-Tile Transceivers—Preliminary* — Table: *Power Supply Sharing Guidelines for Intel Agilex Device with P-Tile and H-Tile Transceivers—Preliminary* • Replaced references to *Intel Agilex Platform Design Guide* with *AN 910: Intel Agilex Power Distribution Network Design Guidelines* for more details on decoupling recommendations for specific power rails.
2020.06.30	• Updated the connection guidelines of the TCK pin. • Updated the pin description of the nSTATUS pin. • Updated the pin description and connection guidelines of the nCONFIG pin. • Updated the connection guidelines of the VCCIO_PIO_SDM pin. • Updated the AVST x8, x16, and x32 configuration schemes for the *Direct to Factory Image* signal in the *SDM Optional Signal Pins* table. • Removed the SDMMC_CFG configuration pin functions and connection guidelines from the *Secure Device Manager (SDM) Pins* table.
2020.05.05	Updated the connection guidelines of the VCCFUSEWR_SDM pin.

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Document Version	Changes
2020.04.24	• Updated the voltage for VCCFUSEWR_SDM. • Updated the connection guidelines of the VSIGP_[0,1] and VSIGN_[0,1] pins. • Updated the pin function, pin description, and connection guidelines of the AVST_READY(3A bank) pin.
2020.02.04	Updated the connection guidelines of the VSIGP_[0,1] and VSIGN_[0,1] pins.
2020.01.23	• Changed the Early Power Estimator (EPE) tool name to Intel FPGA Power and Thermal Calculator. • Updated the VCCPGM power supply to the VCCIO_SDM power supply in the connection guidelines of the TMS and TDI pins. • Updated the pin description of the TCK, TMS, TDI, nSTATUS, nCONFIG, and OSC_CLK_1 pins. • Updated the pin description of the AVST_DATA[31:0] and AVST_READY(3A bank) pins. • Updated the pin names from SDM_MISSION_DATA[31:0], SDM_MISSION_CLK, and SDM_MISSION_DATA_VALID to AVST_DATA[31:0], AVST_CLK, and AVST_VALID. • Updated pin name I_PIN_PERST_N_U[10,20]_P to I_PIN_PERST_N_P. • Updated the I/O standard naming from 1.5V True Differential Signaling to True Differential Signaling. • Updated supported I/O standard from SSTL 1.2V to 1.2V LVCMOS for the AVST_READY(3A bank), AVST_CLK(3A bank), and AVST_VALID(3A bank) pins. • Updated the pin description of the DIFF_RX[2][A,B,C,D][1:24][p,n], DIFF_RX[3][A,B,C,D][1:24][p,n], DIFF_TX[2][A,B,C,D][1:24][p,n], and DIFF_TX[3][A,B,C,D][1:24][p,n] pins. • Updated the resistor value from 2kΩ to 2.8kΩ for the IO_AUX_RREF[10,20]_P pins. • Updated the pin description and connection guidelines of the VCCBAT pin. • Updated the pin description and connection guidelines of the VCCPT pin. • Updated the pin description and connection guidelines of the VCCR_CORE pin. • Updated the pin description of the VCCA_PLL pin. • Updated the connection guidelines of the DNU pins. • Updated the connection guidelines of the VCCIO_SDM pin. • Updated the pin function of the RREF_SDM pin. • Updated the pin description and connection guidelines of the REFCLK_GXE(L8,R9)_CH[0:8][p,n] pins. • Updated the connection guidelines of the GXP[L10A,R11A]_RX_CH[19:0][p,n] pins. • Updated the connection guidelines of the GXP[L10A,R11A]_TX_CH[19:0][p,n] pins. • Updated the connection guidelines of the REFCLK_GXP[L10A,R11A]_CH[0,2][p,n] pins. • Updated the resistor value from 200Ω to 169Ω of the U[10,20]_P_IORESREF_0 pins. • Updated the connection guidelines of the I_PIN_PERST_P pins. • Updated the connection guidelines of the VCCL_HPS pin. • Updated Table: *Power Supply Sharing Guidelines for Intel Agilex Device*. • Updated Figure: *Example Power Supply Sharing Guidelines for Intel Agilex Device*.

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Document Version	Changes
	• Added SDM_IO8 to AVST x16 and x32 for the CONF_DONE and INIT_DONE pins. • Added reference to the *External Memory Interface Pin Information for Intel Agilex Devices* in the *External Memory Interface Pins* section. • Added reference to the *E-Tile Transceiver PHY User Guide* in the *E-Tile Pins* section.
2019.06.10	Initial release.