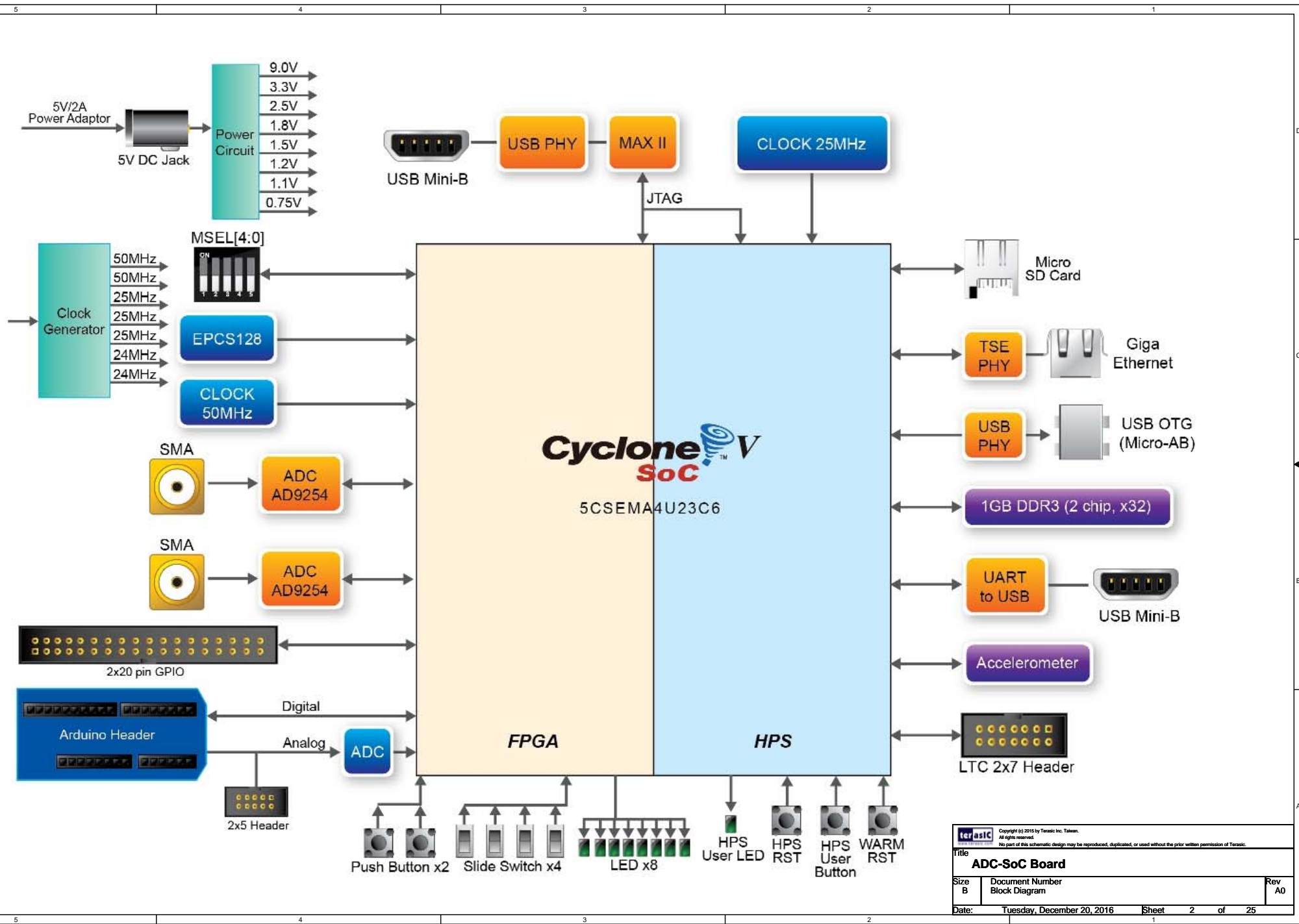
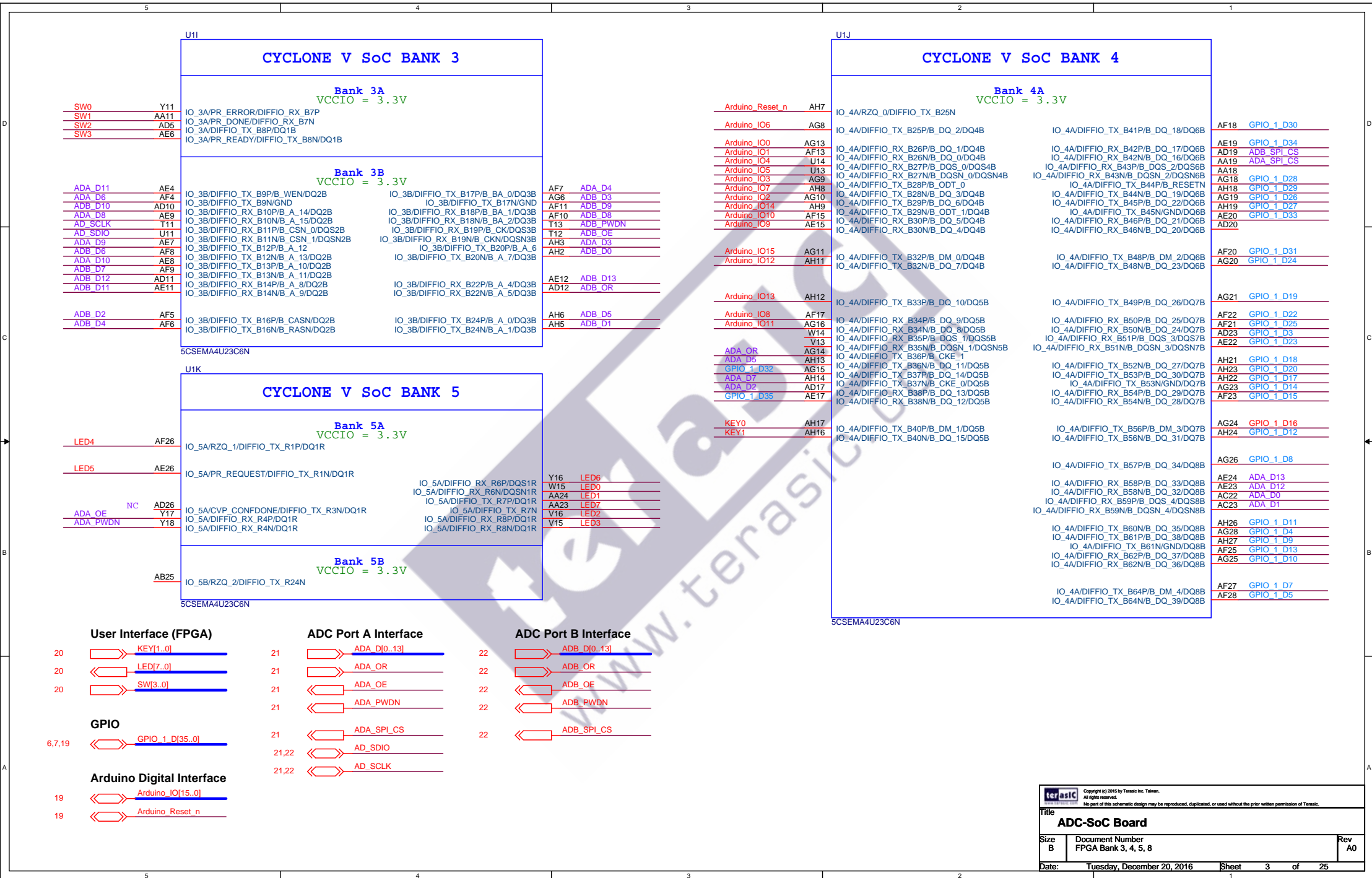


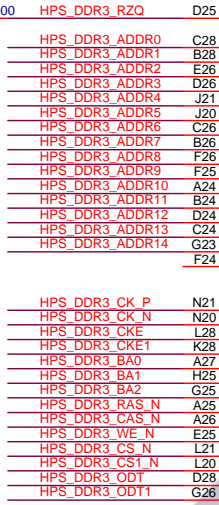
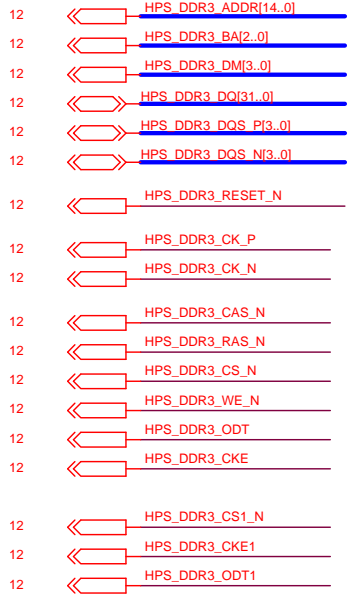
ADC-SoC Development Board

PAGE	CONTENT
01	Cover Page
02	Block Diagram
03	FPGA IO Bank3, 4, 5 and 8
04	FPGA IO Bank 6 (HPS DDR3)
05	FPGA IO Bank 7 (HPS Peripheral Device)
06	FPGA Clock In/Out and Clock Generator
07	FPGA Configuration and EPCS device
08	FPGA Power
09	FPGA Decoupling
10	USB Blaster II
11	JTAG Chain
12	HPS Peripheral : DDR3 SDRAM
13	HPS Peripheral : UART to USB and SD Card Socket
14	HPS Peripheral : USB OTG
15	HPS Peripheral : Gigabit Ethernet
16	HPS Peripheral : Accelerometer & LTC Expansion Header
17	HPS Peripheral : Reset Circuit, Button and LED
18	FPGA : ADC1 (LTC2308) for 8-channel Analog Expansion Header and Arduino Analog input
19	FPGA : GPIO, Analog and Arduino UNO Expansion Header
20	FPGA : Button, Switch and LED
21	FPGA : ADC A
22	FPGA : ADC B
23	Power - 1.1V, 5V
24	Power - 2.5V, 3.3V
25	Power - 1.2V, 1.5V, 1.8V, 9V





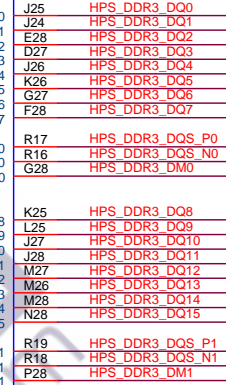
DDR3 Interface (HPS)



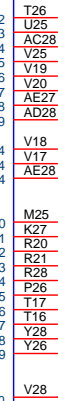
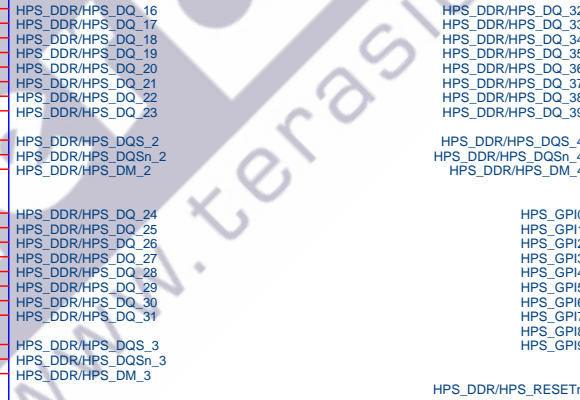
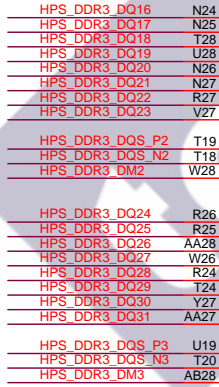
U1L

CYCLONE V SoC BANK 6 (HPS)

Bank 6A
VCCIO = 1.5V

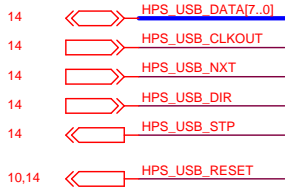


Bank 6B
VCCIO = 1.5V

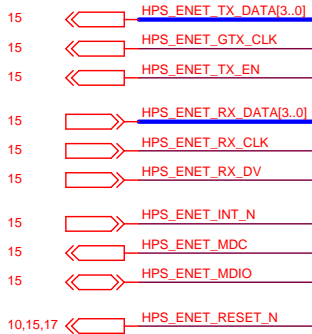


5CSEMA4U23C6N

UBS PHY Interface (ULPI)



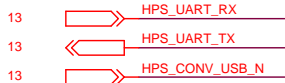
Ethernet PHY Interface (RGMII)



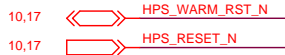
SD Card Interface



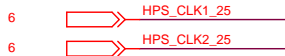
UART Interface



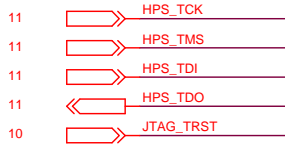
HPS Reset



HPS Clock



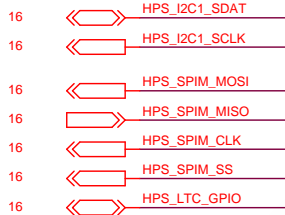
HPS JTAG INTERFACE



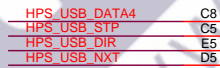
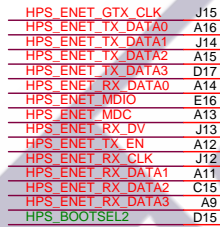
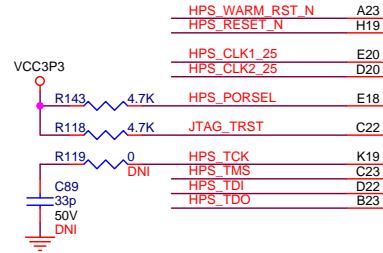
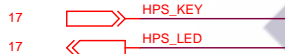
Accelerometer Interface



LTC Interface



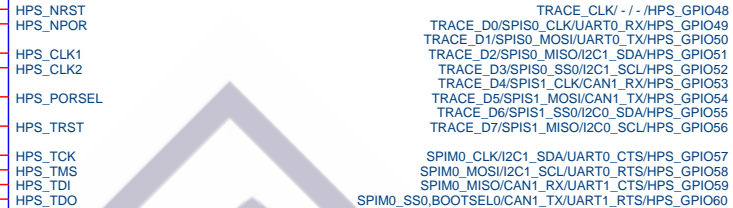
HPS Key and LED



U1M

CYCLONE V SoC BANK 7 (HPS)

Bank 7A
VCCIO = 3.3V



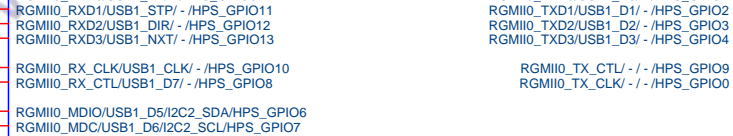
Bank 7B
VCCIO = 3.3V



Bank 7C
VCCIO = 3.3V

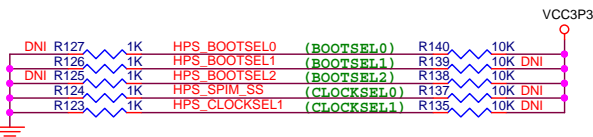


Bank 7D
VCCIO = 3.3V

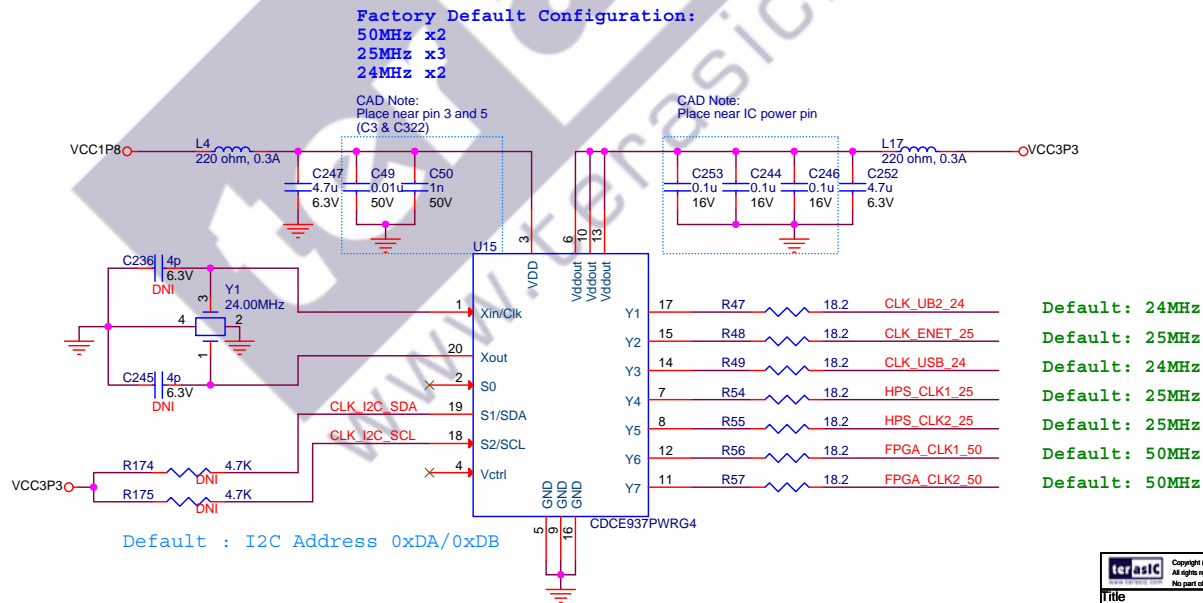
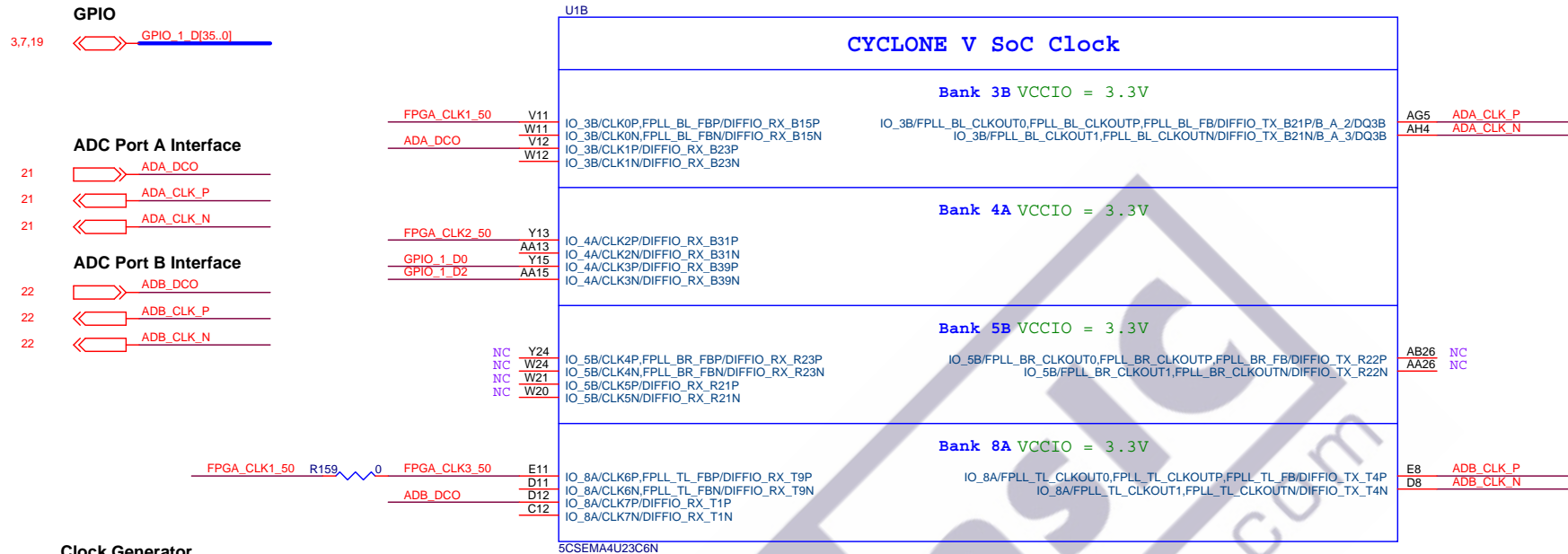


5CSEMA4U23C6N

Default Setting: BOOTSEL[2:0]=101 (Boot from SD CARD)
CLKSEL[1:0] =00



Title	
ADC-SoC Board	
Size	Document Number
B	FPGA Bank 7
Date:	Tuesday, December 20, 2016
Sheet	5 of 25
Rev	A0



FPGA JTAG INTERFACE



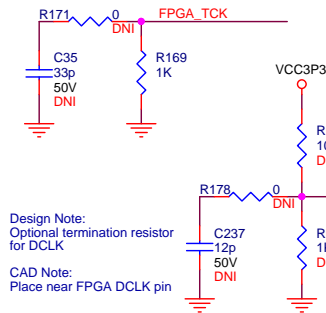
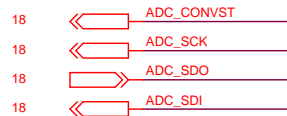
USB Blaster



GPIO

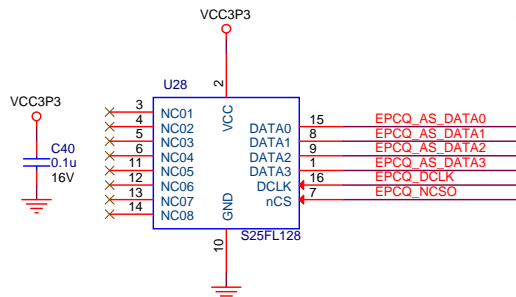
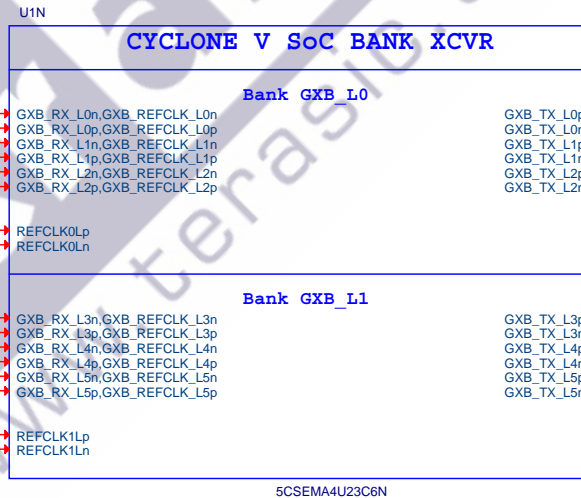
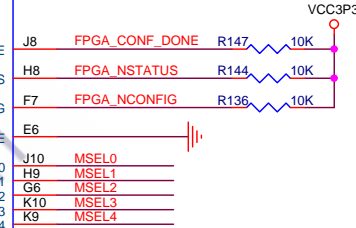
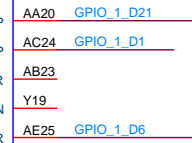
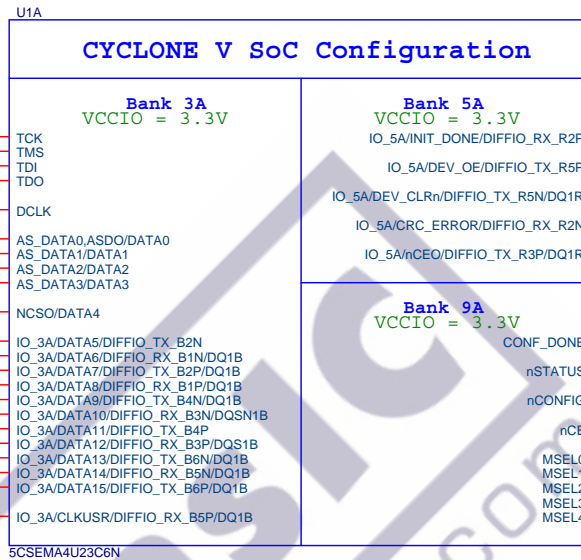


ADC

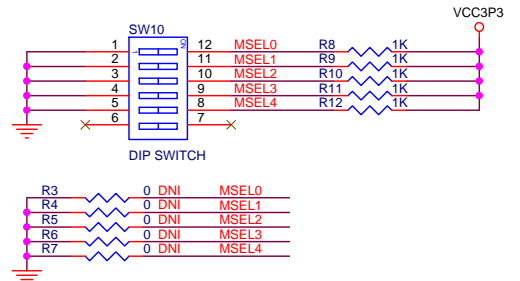


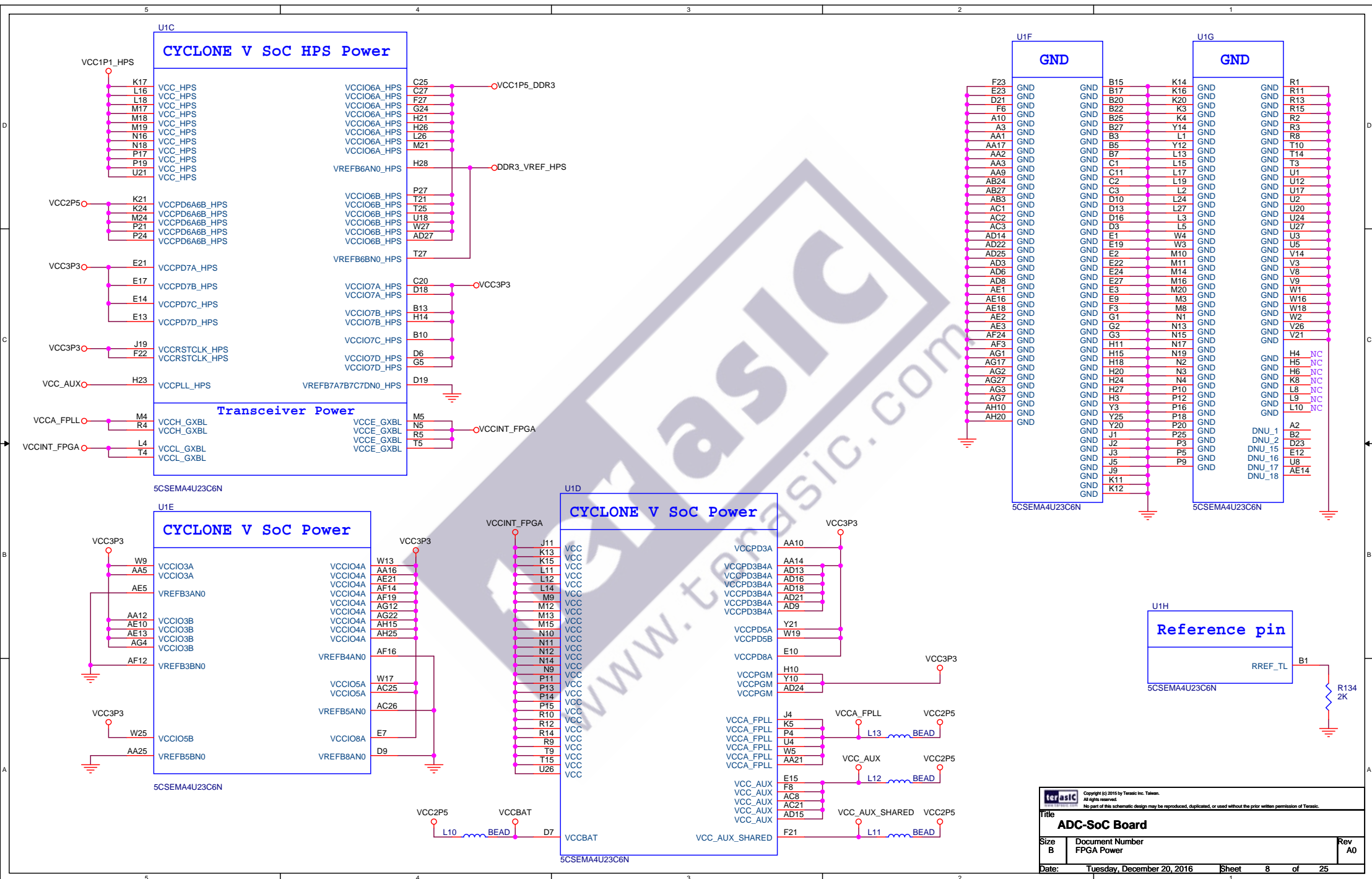
Design Note:
Optional termination resistor
for DCLK

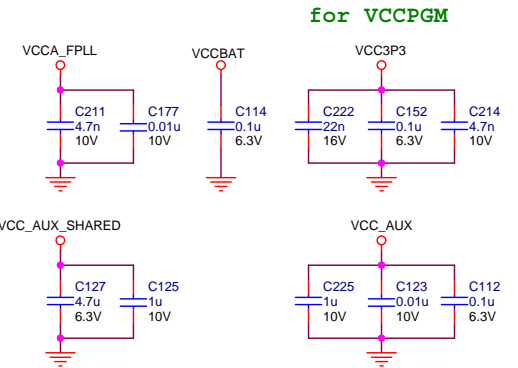
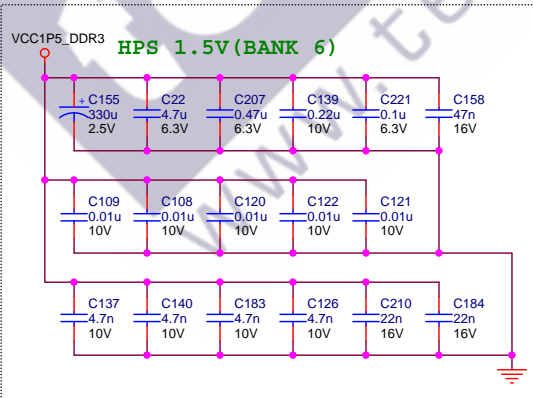
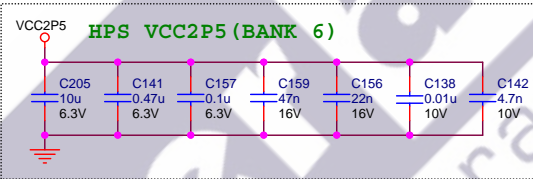
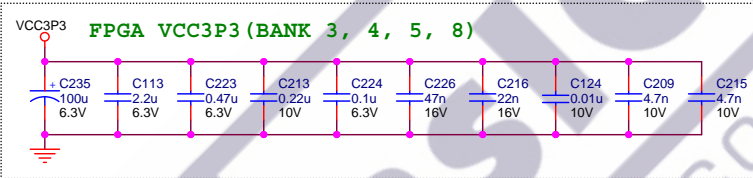
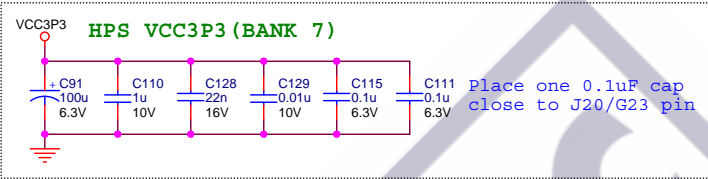
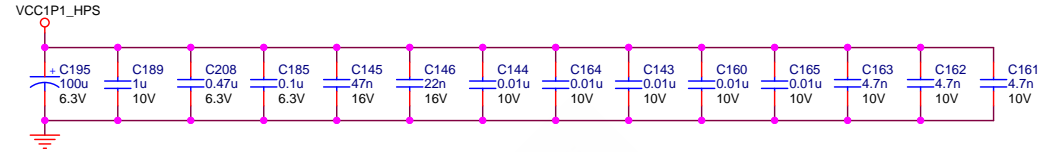
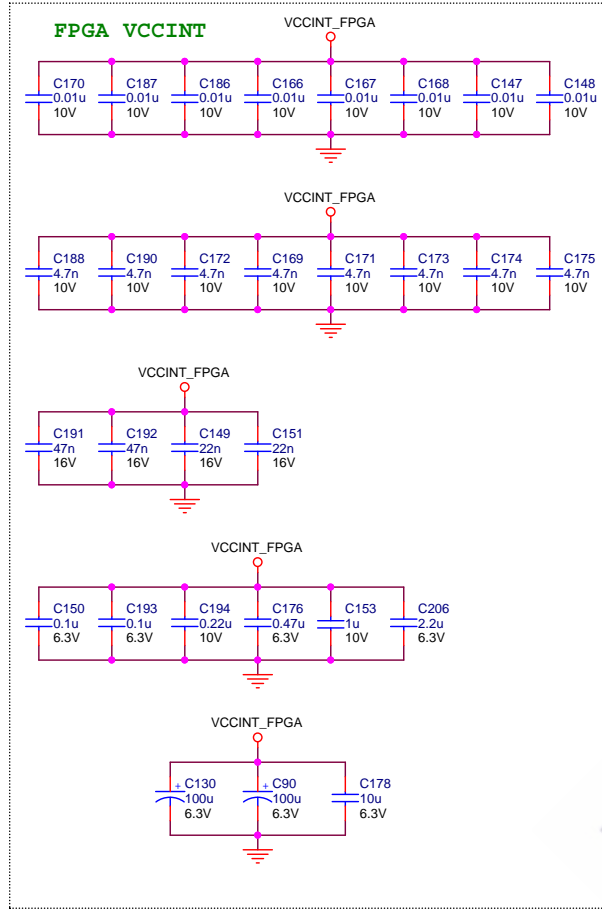
CAD Note:
Place near FPGA DCLK pin

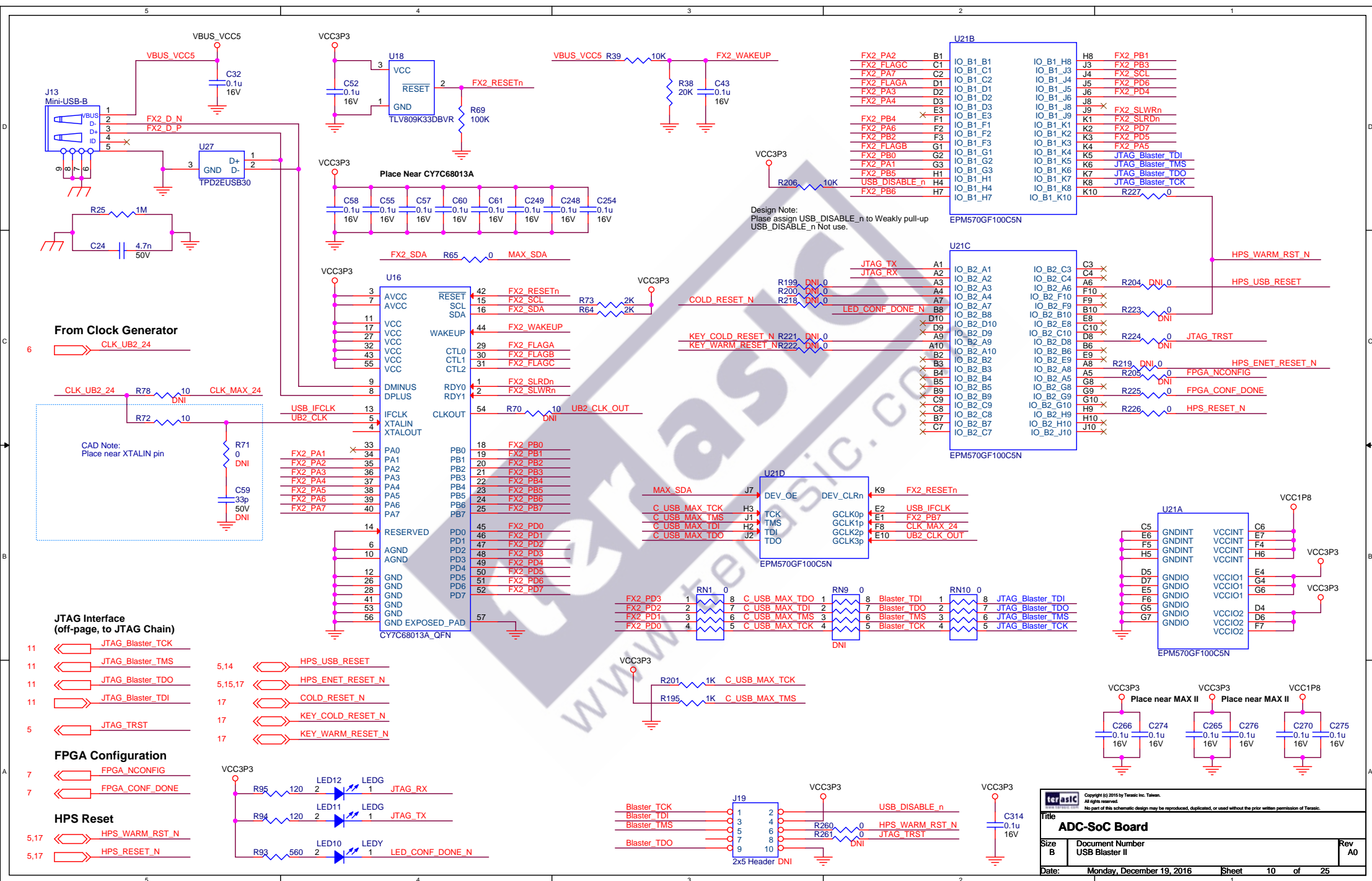


Default Setup MSEL[4:0] = 10010,
AS Fast Mode









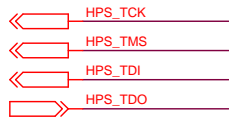
USB Blaster



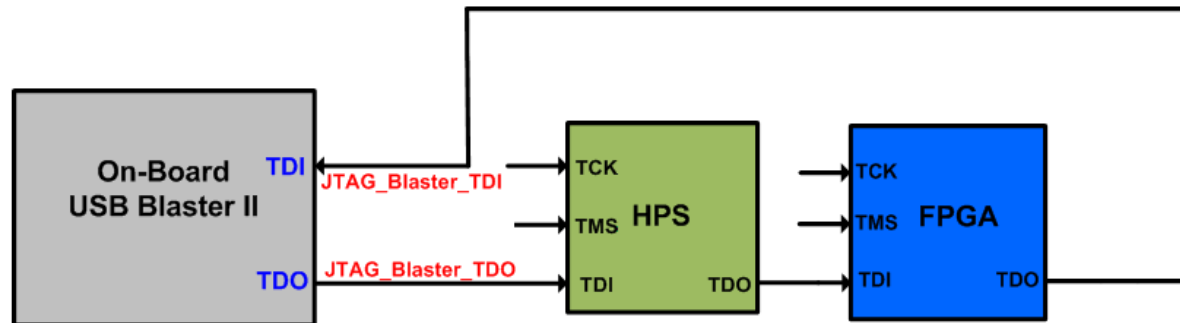
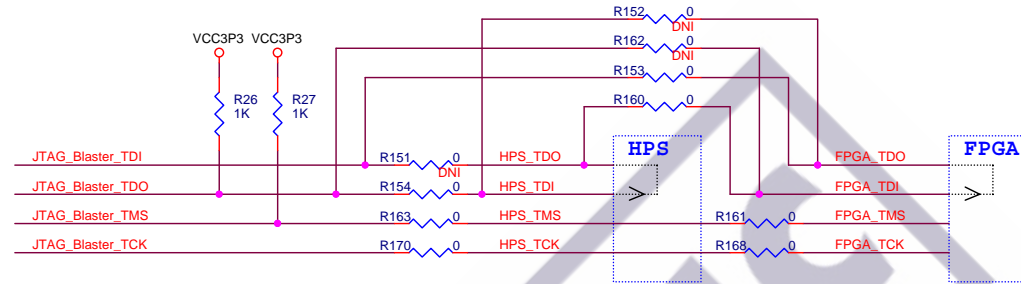
FPGA JTAG INTERFACE



HPS JTAG INTERFACE



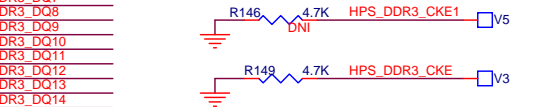
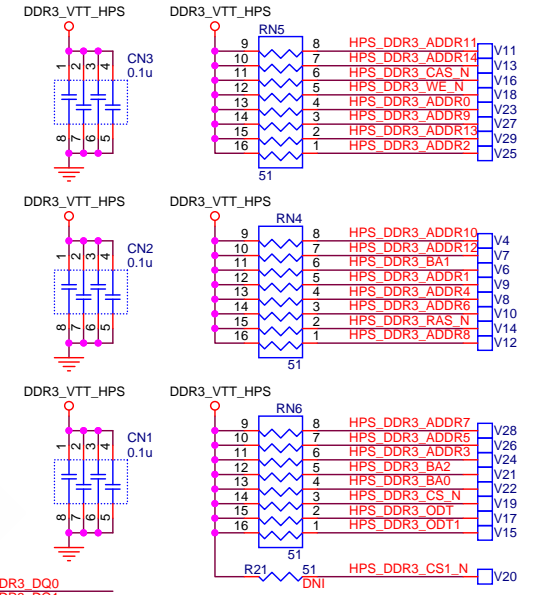
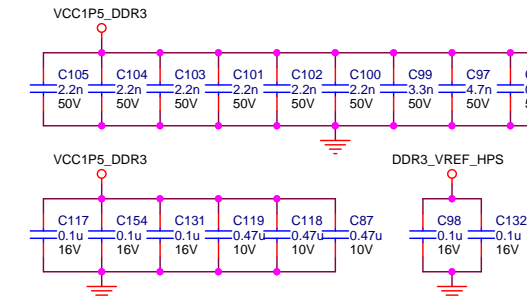
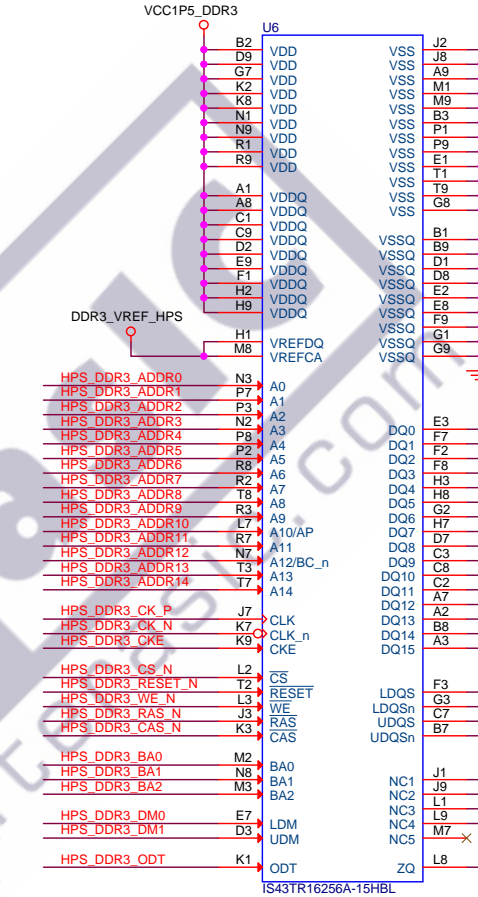
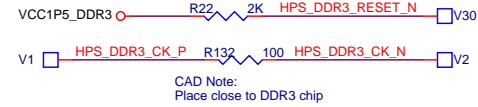
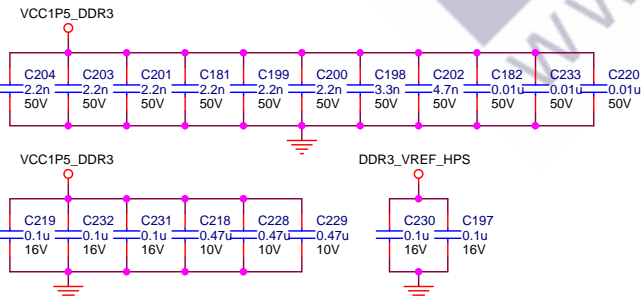
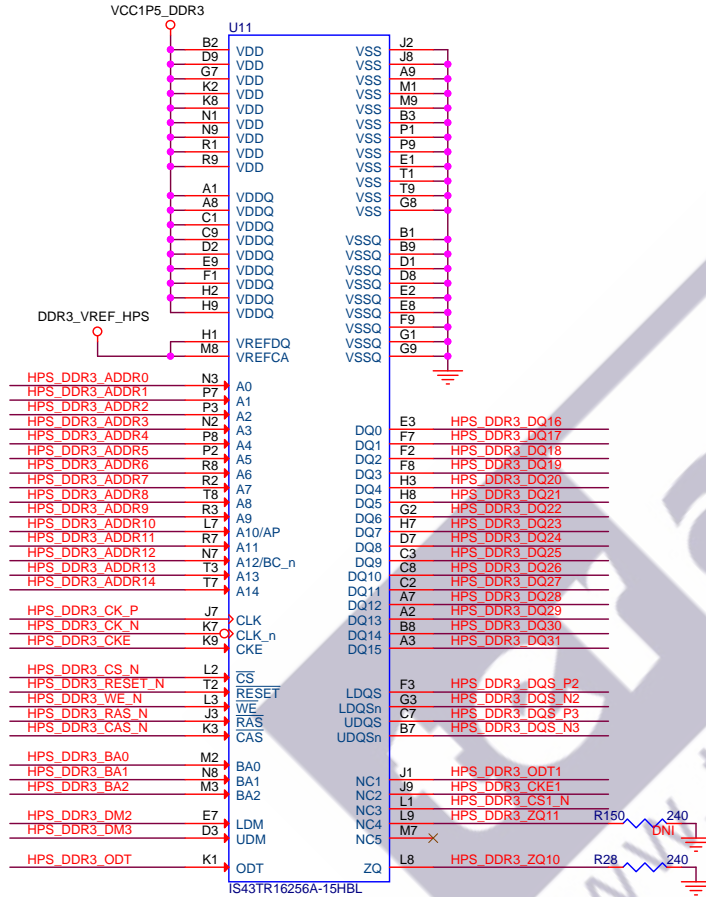
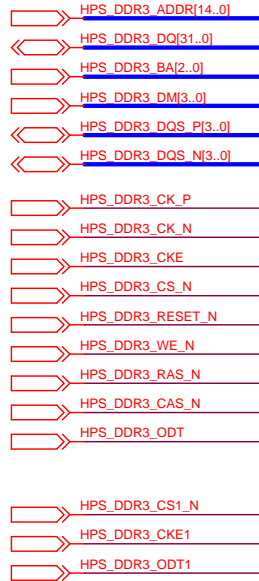
JTAG Chain



DDR3 Interface (HPS)

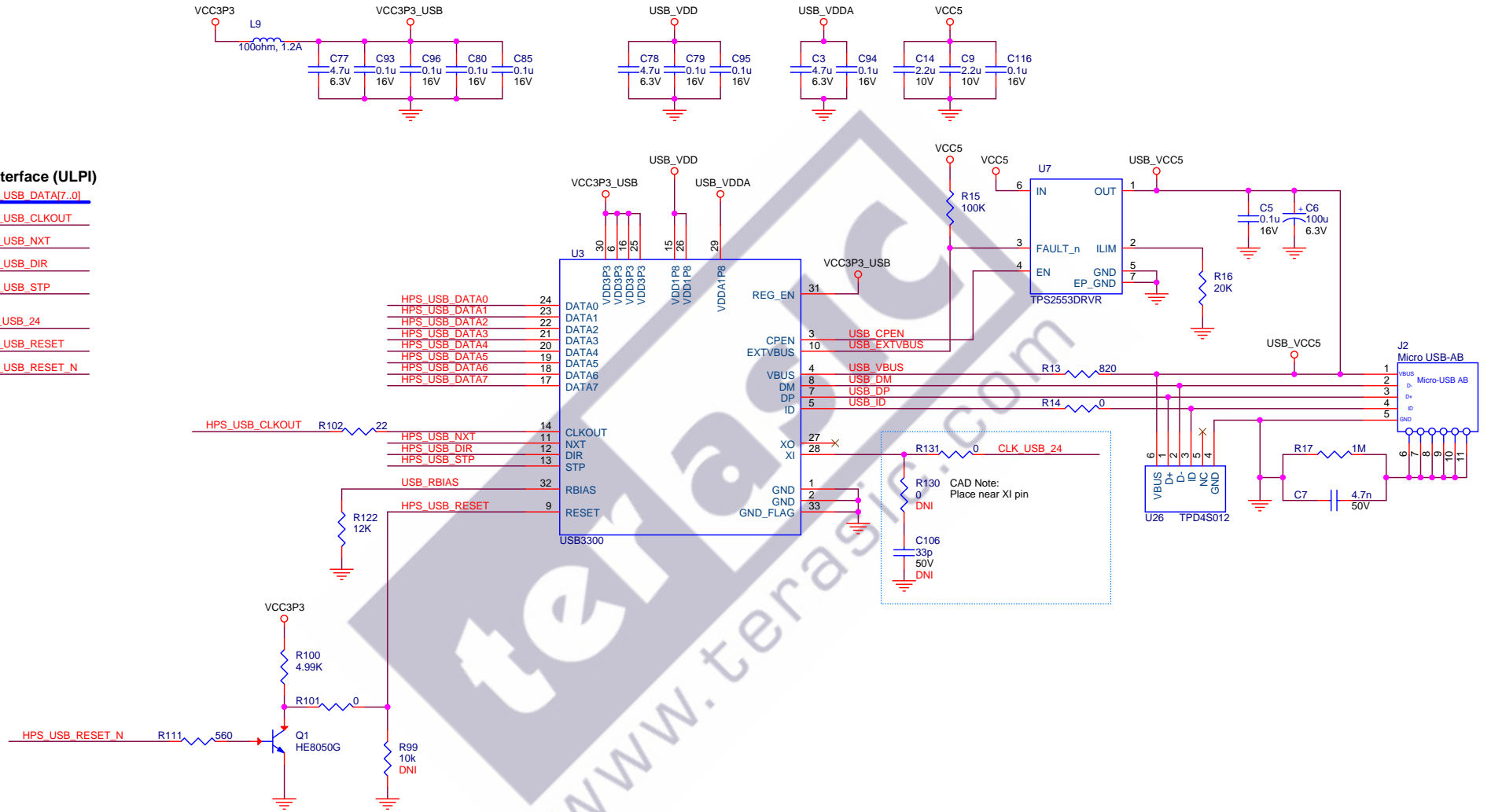
Note :
you can only swap the DQ signals
within x8 group (e.g. 0-7,8-15,16-23,24-31)
on the DDR3 chips

Note : you can swap the signals on the OCT resistor array
(include NC pin)

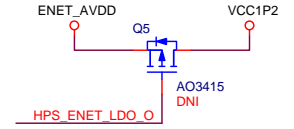
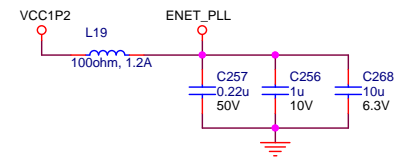
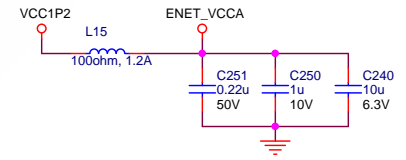
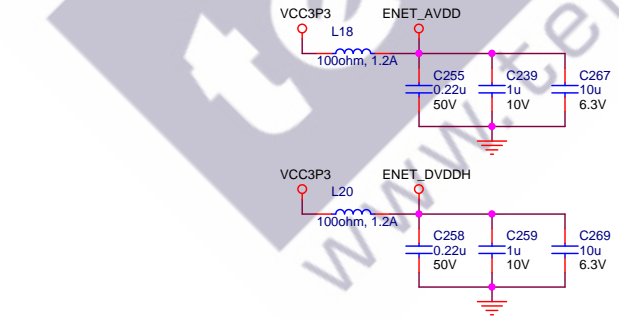
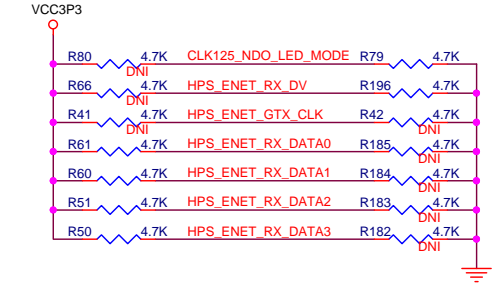
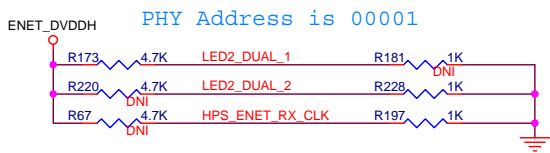
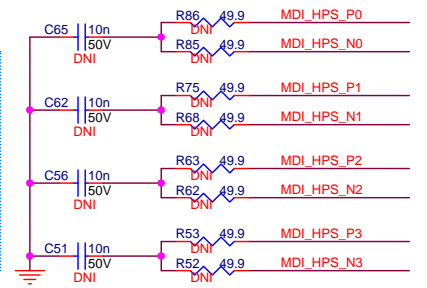
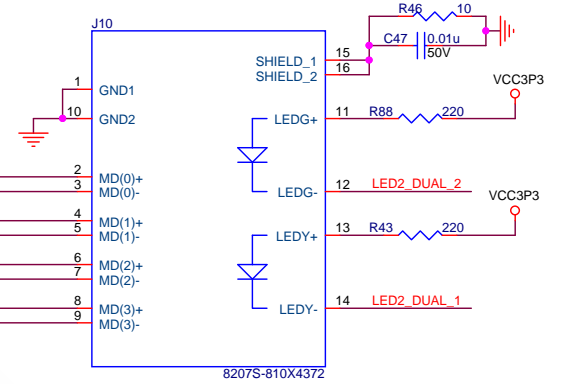
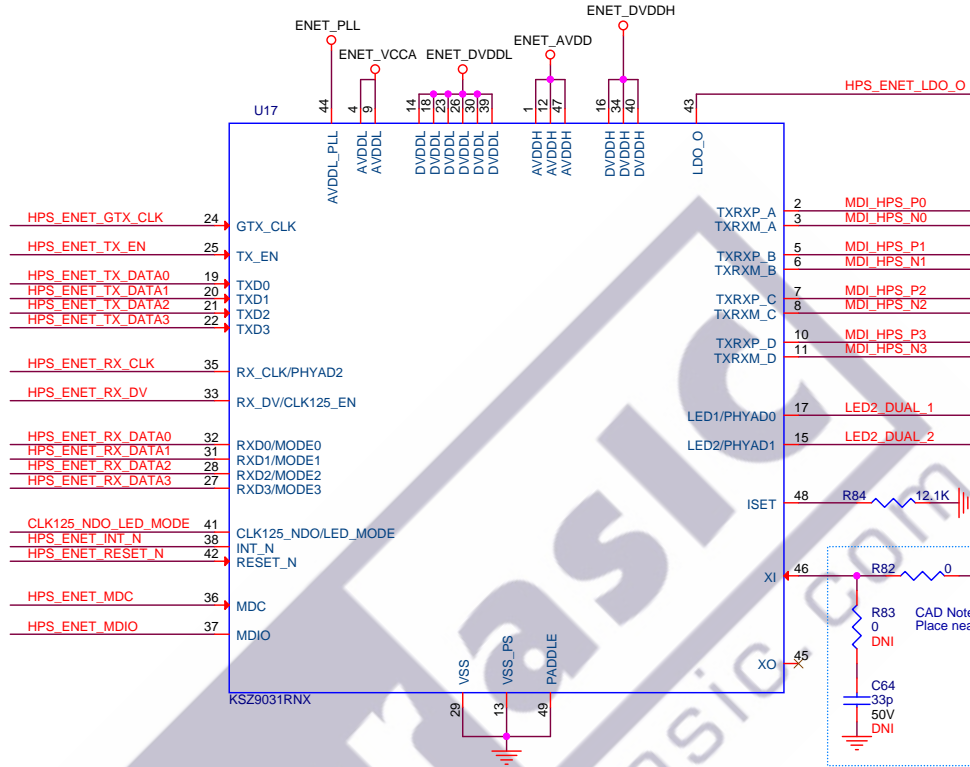
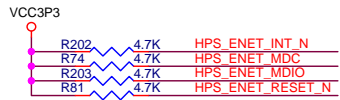
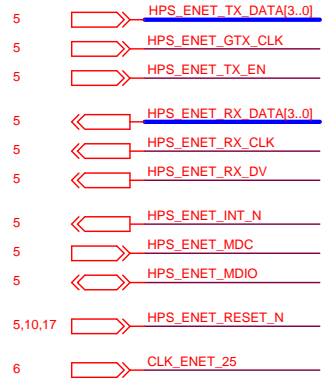


UBS PHY Interface (ULPI)

- 5 HPS_USB_DATA[7..0]
- 5 HPS_USB_CLKOUT
- 5 HPS_USB_NXT
- 5 HPS_USB_DIR
- 5 HPS_USB_STP
- 6 CLK_USB_24
- 5,10 HPS_USB_RESET
- 17 HPS_USB_RESET_N



Ethernet PHY Interface (RGMII)

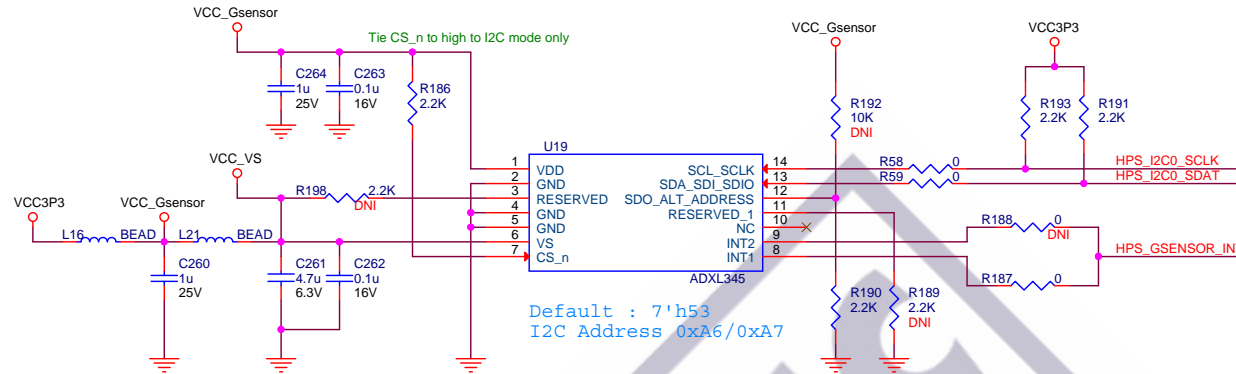


terasic			
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Title			
ADC-SoC Board			
Size	Document Number	Rev	
B	HPS : GigaBit Ethernet	A0	
Date:	Monday, December 19, 2016	Sheet	15 of 25

Digital Accelerometer

Accelerometer Interface

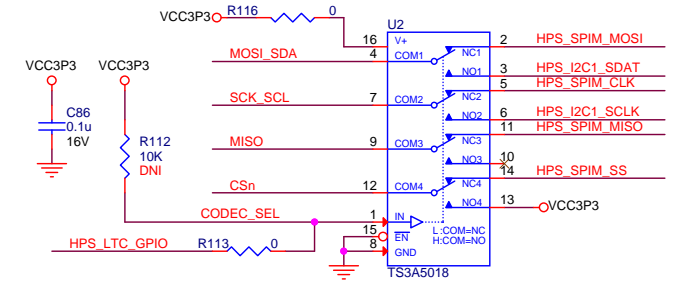
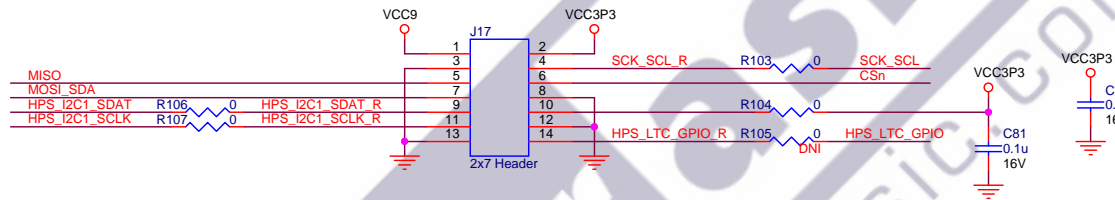
- HPS_I2C0_SDAT
- HPS_I2C0_SCLK
- HPS_GSENSOR_INT



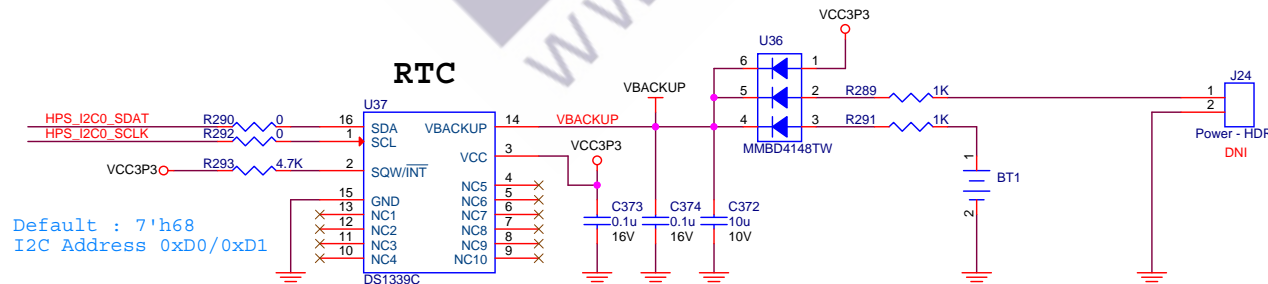
LTC 2x7 Connector

LTC Interface

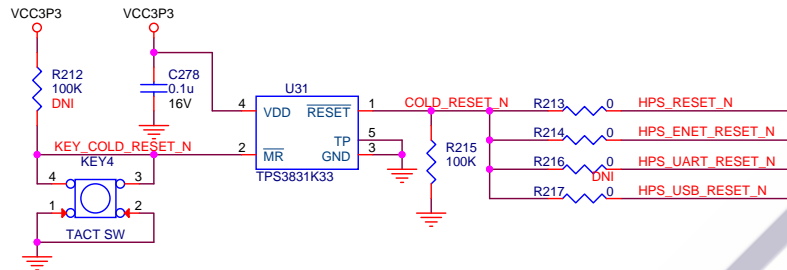
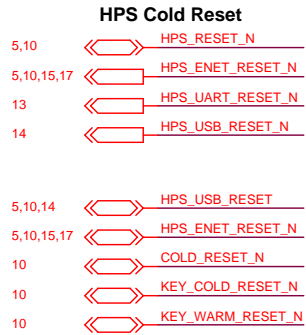
- HPS_I2C1_SDAT
- HPS_I2C1_SCLK
- HPS_SPIM_MOSI
- HPS_SPIM_MISO
- HPS_SPIM_CLK
- HPS_SPIM_SS
- HPS_LTC_GPIO



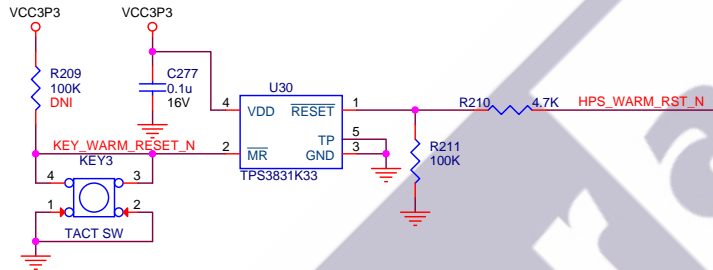
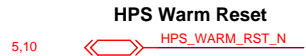
RTC



HPS Cold Reset



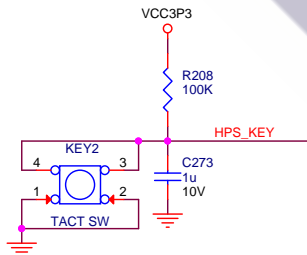
HPS Warm Reset



HPS Key and LED

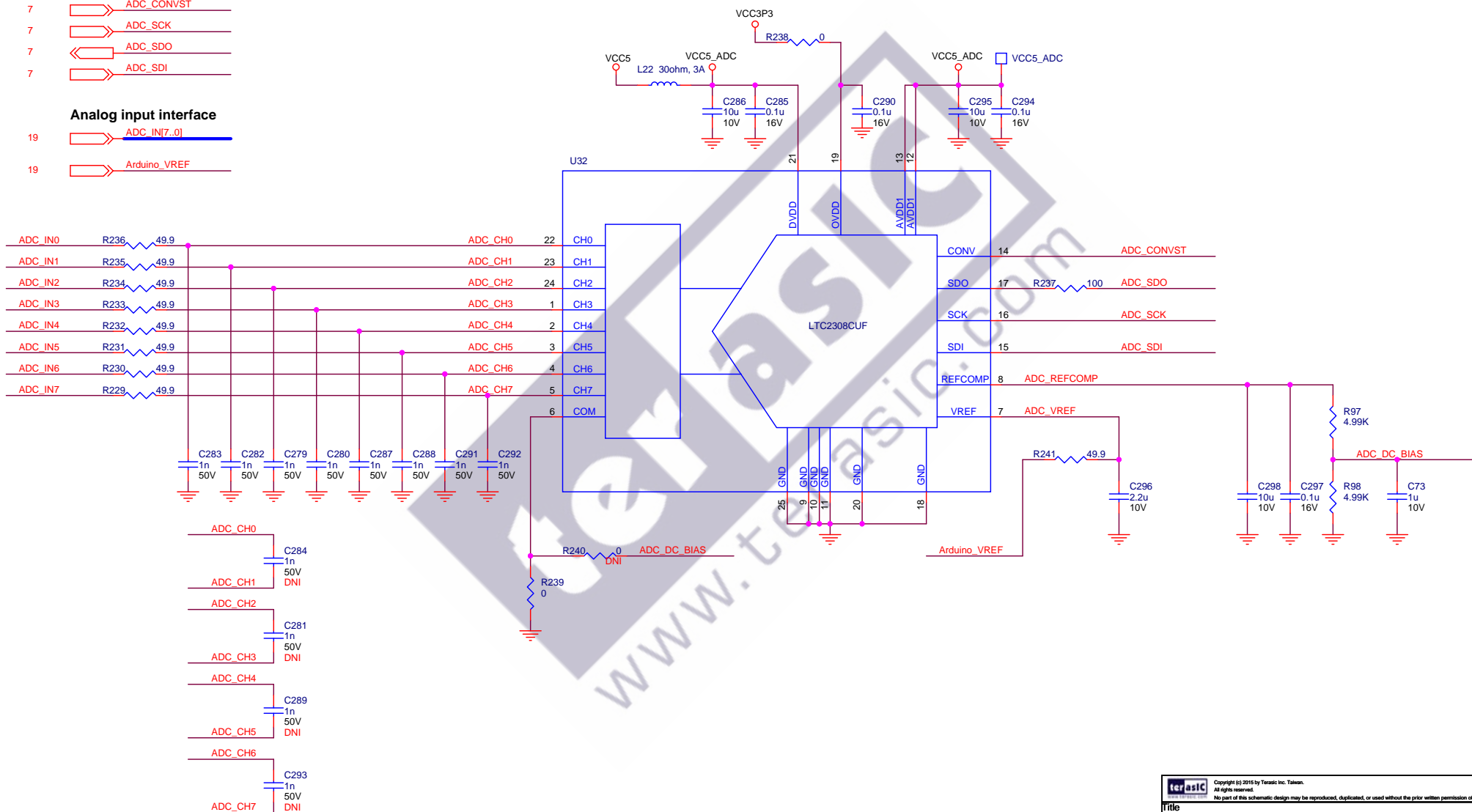
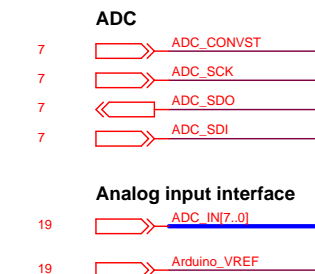


HPS User Button



HPS User LED





GPIO

3,6,7 << GPIO_1_D[35..0]

Arduino Digital Interface

3 << Arduino_IO[15..0]

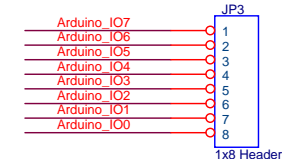
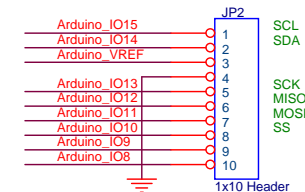
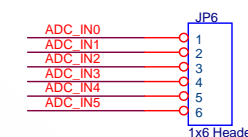
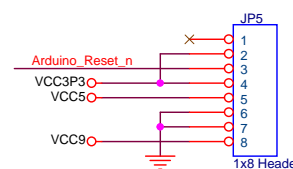
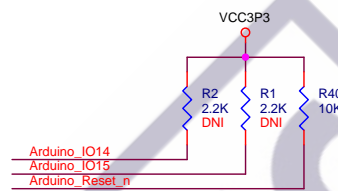
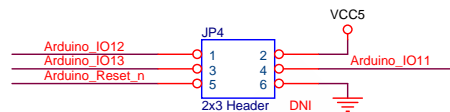
3 << Arduino_Reset_n

Analog input interface

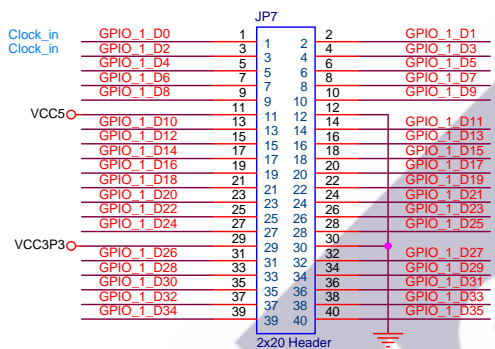
18 << ADC_IN[7..0]

18 << Arduino_VREF

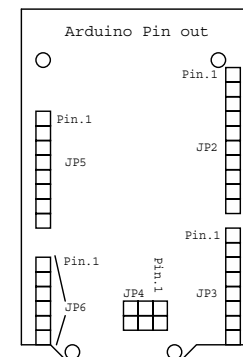
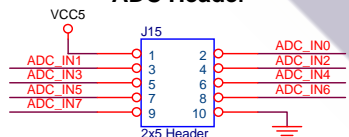
Arduino UNO Rev3



GPIO 1 Header



ADC Header



KEY

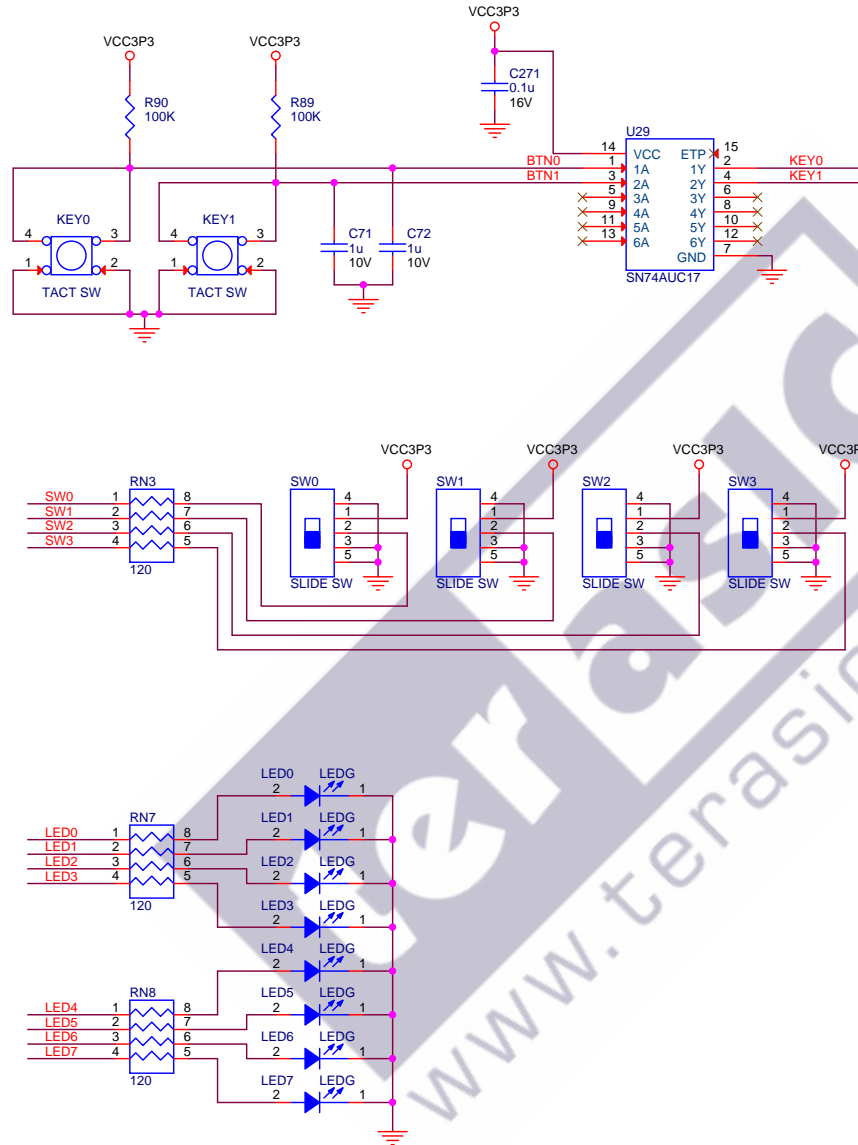
KEY[1..0]

SWITCH

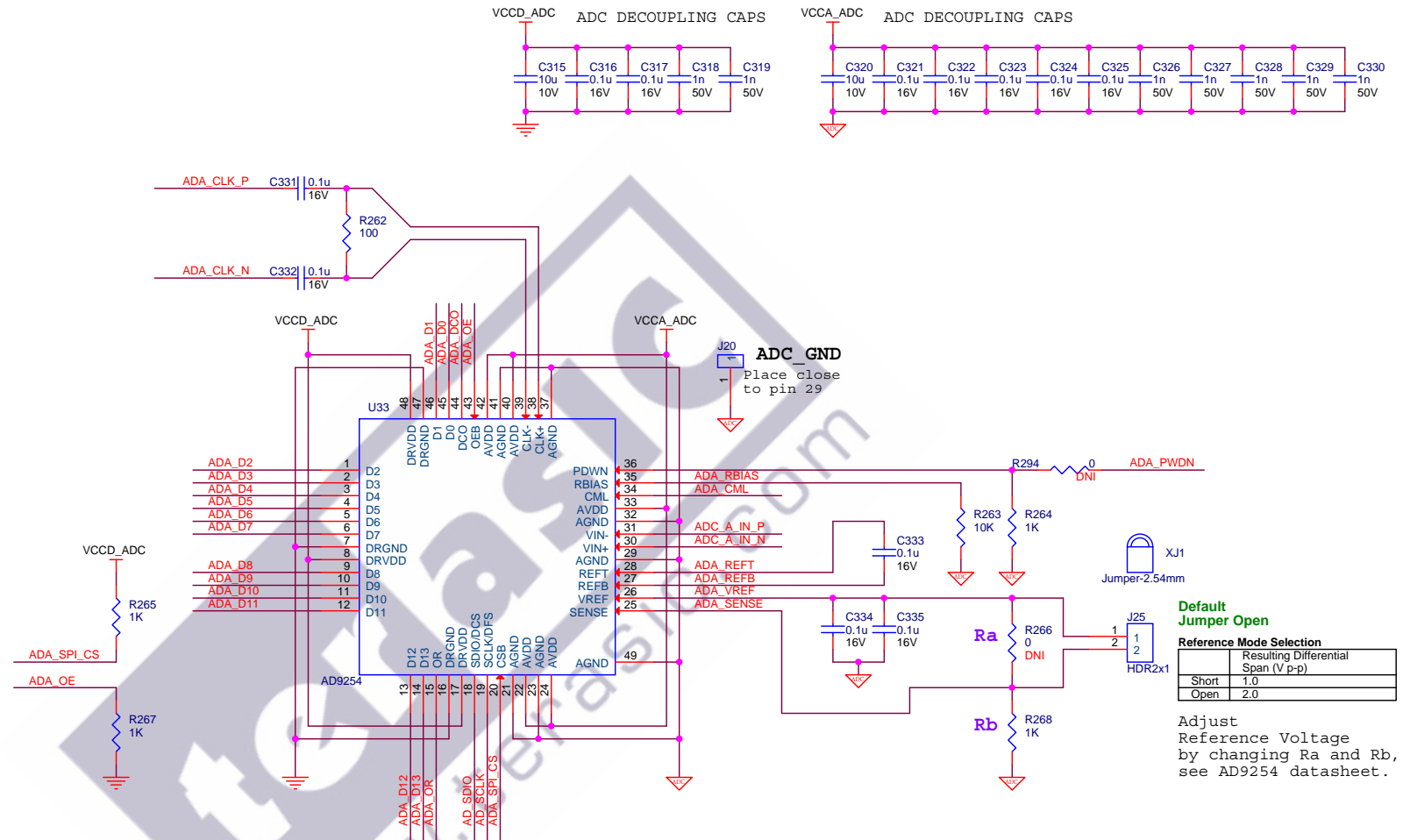
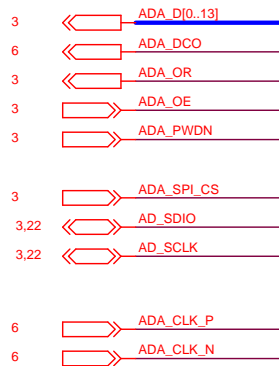
SW[3..0]

LED

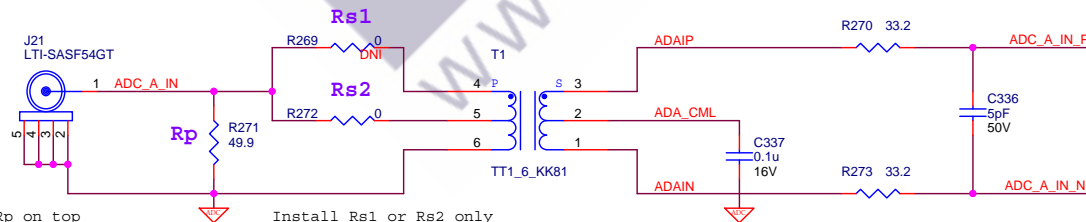
LED[7..0]



ADC Port A Interface



ADC CHANNEL A



Place Rp on top layer with untented vias so that it can be probed for testing purposes.

Install Rs1 or Rs2 only to experiment for the output swing and characteristics

Default Jumper Open

Reference Mode Selection

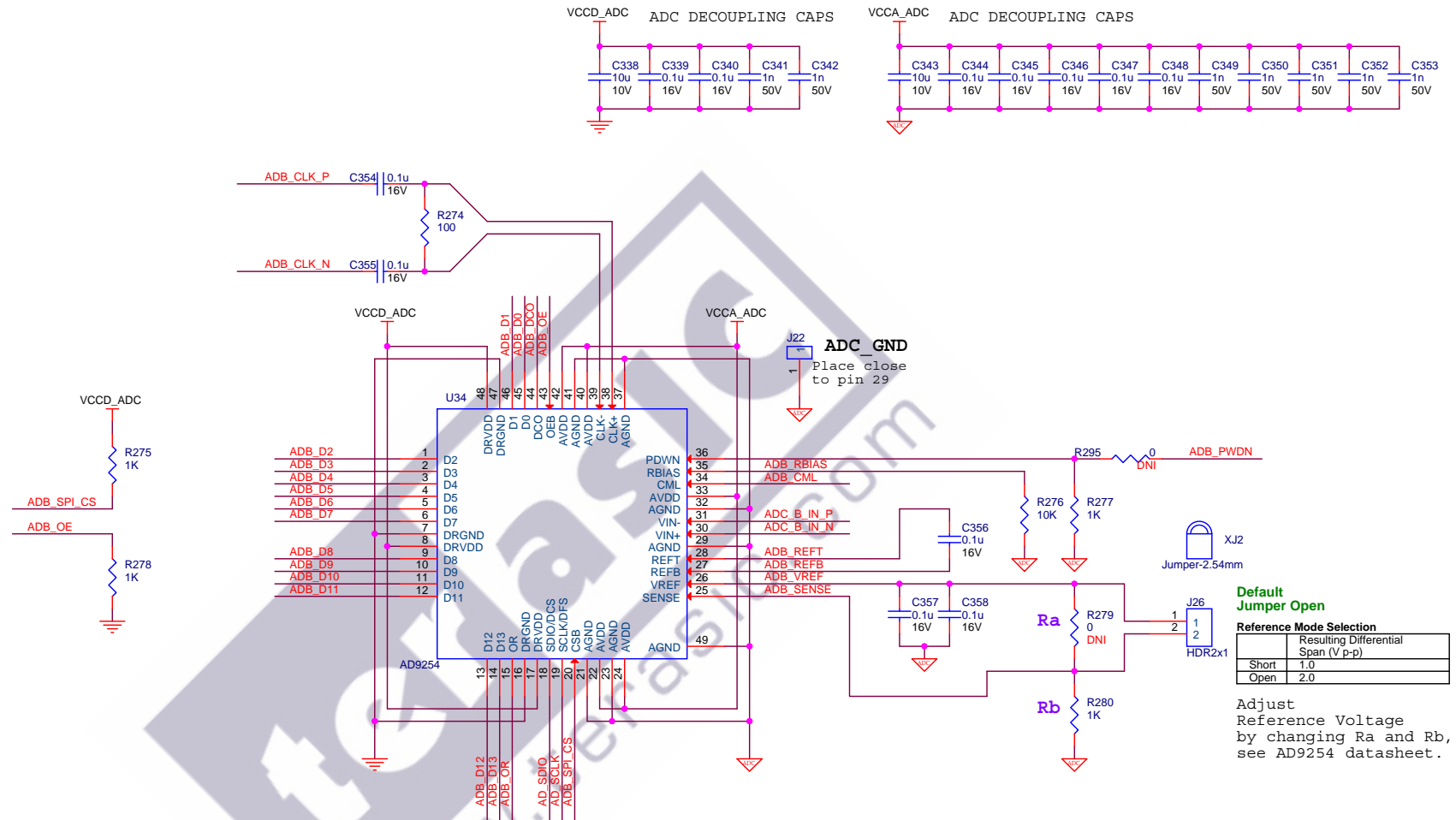
Resulting Differential Span (V p-p)
Short 1.0
Open 2.0

Adjust Reference Voltage by changing Ra and Rb, see AD9254 datasheet.

Analog to Digital Converter Channel A
14 Bit, 150 Ms/s, Analog Devices AD9254

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Title ADC-SoC Board			
Size B	Document Number Cover Page	Rev A0	
Date:	Monday, December 19, 2016	Sheet	21 of 25

3		ADB_D[0..13]
3		ADB_OR
3		ADB_OE
3		ADB_PWDN
3		ADB_SPI_CS
3,21		AD_SDIO
3,21		AD_SCLK
6		ADB_DCO
6		ADB_CLK_P
6		ADB_CLK_N



J23 LTI-SAS54GT

1 ADC_B_IN

2

3

4 P

5

6

TT1_6_KK81

ADBIP

ADB_CML

ADBIN

R281 0

R282 33.2

R283 0

R284 49.9

R285 33.2

R286 100k

C360 0.1u 16V

C359 5pF 50V

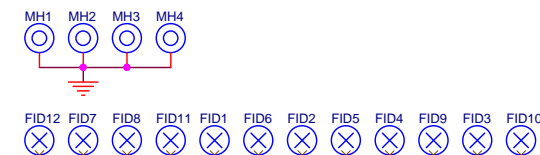
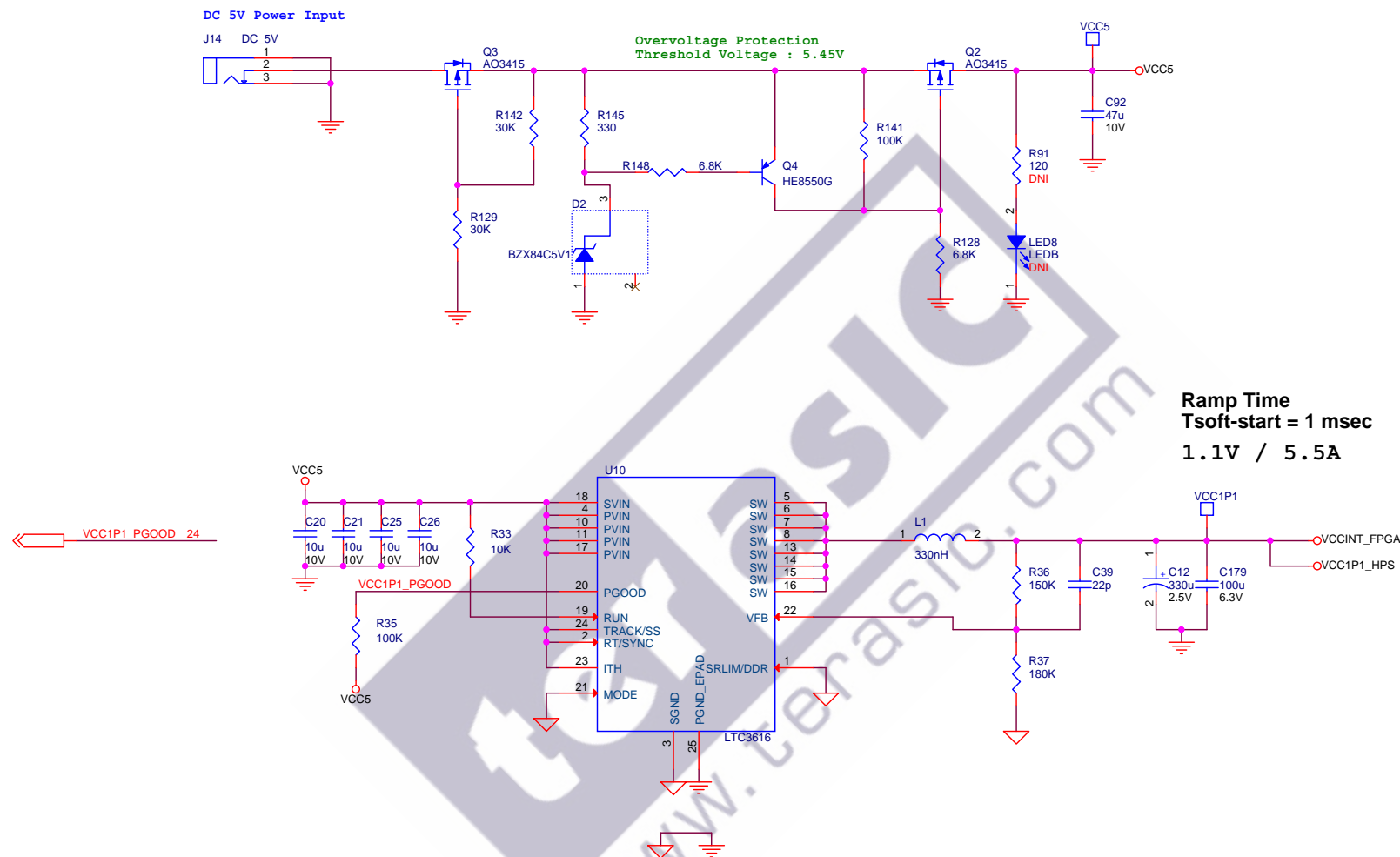
ADC_B_IN

ADC_B_IN_N

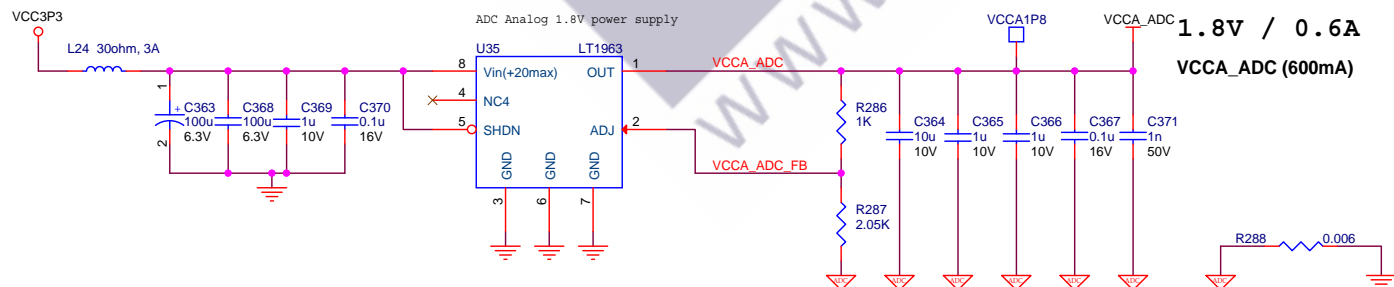
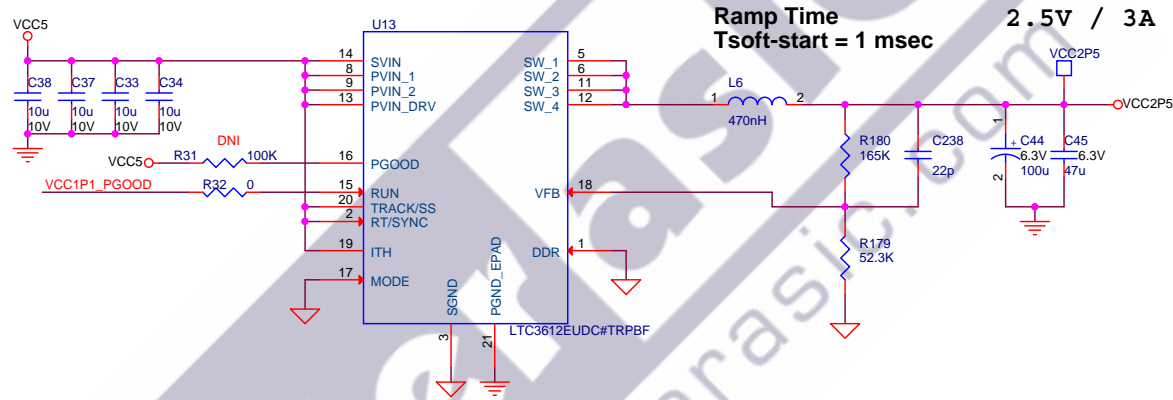
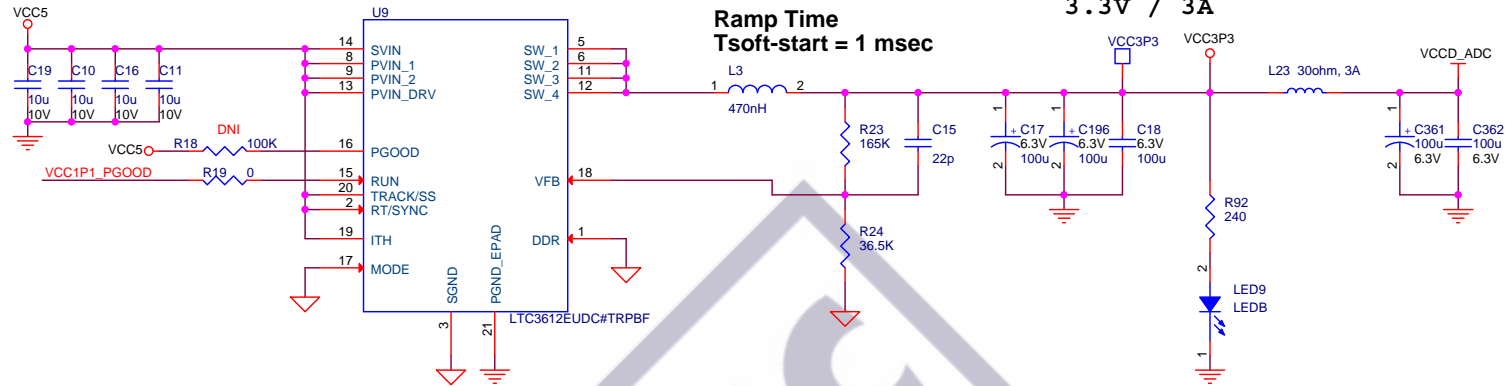
Install Rs1 or Rs2 only

Install Rs1 or Rs2 only
to experiment for the
output swing and
characteristics

Analog to Digital Converter Channel A
14 Bit, 150 Ms/s, Analog Devices AD9254A



VCC1P1_PGOOD 23



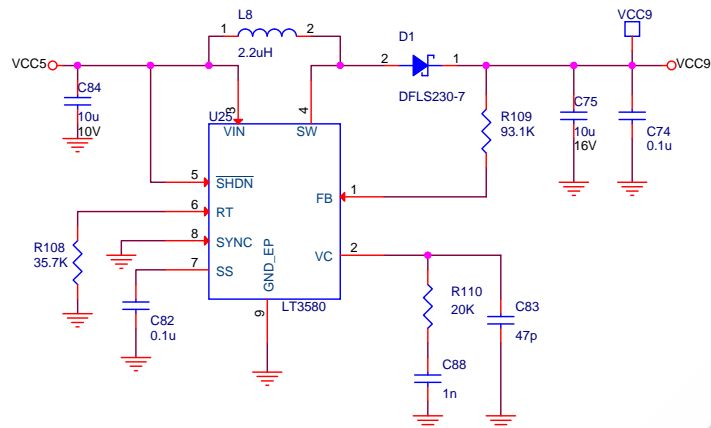
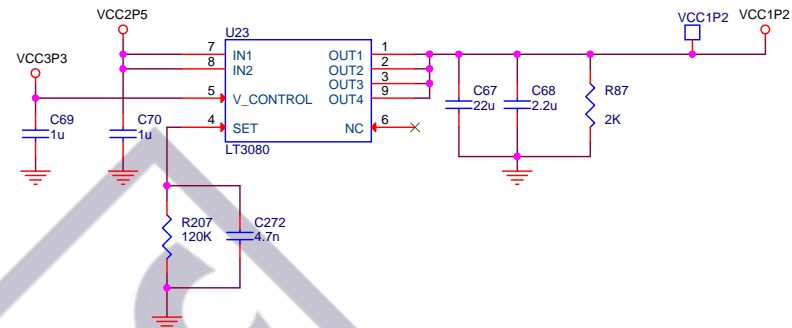
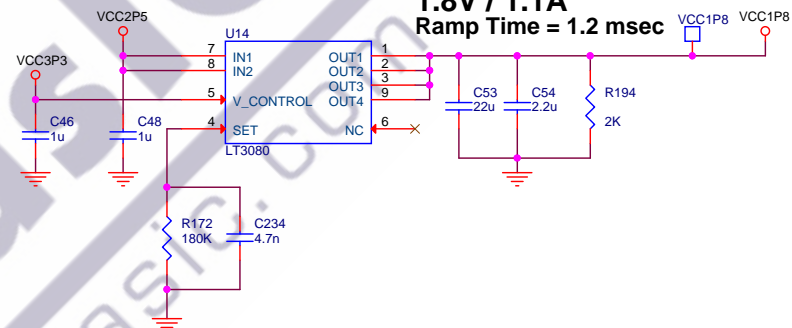
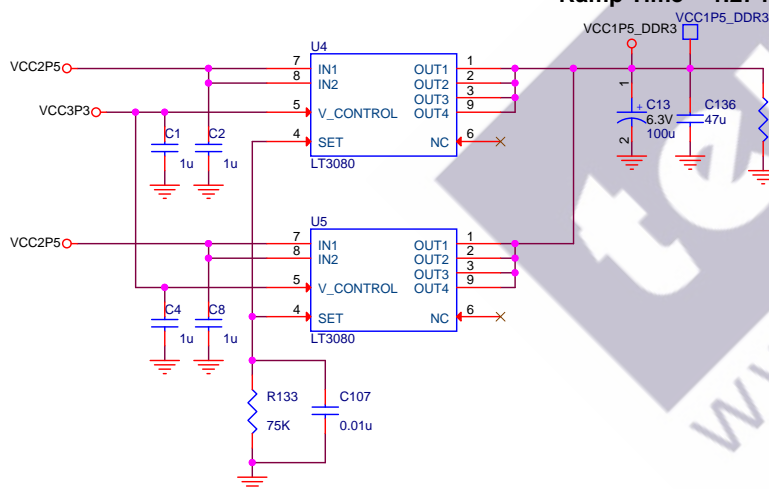
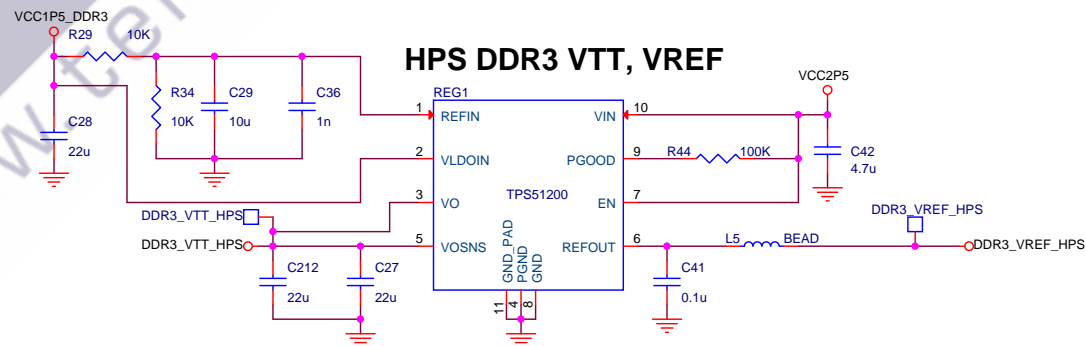
5

4

3

2

1

9V / 1A**1.2V / 1.1A****Ramp Time = 0.8msec****1.8V / 1.1A****Ramp Time = 1.2 msec****1.5V / 2.2A****Ramp Time = 1.27 msec****HPS DDR3 VTT, VREF**

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Title ADC-SoC Board		
Size B	Document Number Power - 1.2V, 1.5V, 1.8V, 9V	Rev A0
Date: Monday, December 19, 2016	Sheet 25	of 25