FPGA Mezzanine Card (FMC) Draft Standard

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Abstract

This standard describes FMC IO modules and introduces an electro-mechanical standard that creates a low overhead protocol bridge. This is between the front panel IO, on the mezzanine module, and an FPGA processing device on the carrier card, which accepts the mezzanine module.

FPGA is an acronym for "Field Programmable Gate Array" which is a semiconductor device that can have its logic functionality defined after it has been supplied to the field. Some devices can be one time programmable while others can be programmed many times with different functionality on each configuration.

FPGAs typically consist of an array of logic cells that implement small logical operations and are surrounded by peripheral I/O which can be programmed for different signaling standards. In some devices, there may be dedicated silicon for more advanced functions, such as multipliers, memory, processors, etc. Programmable interconnect within these devices enable linking of the logic cells, peripheral I/O and the optional dedicated functional blocks hence facilitating the functionality of the complete device.

Foreword

The purpose of this standard is to create an I/O mezzanine module, which works intimately with an FPGA processing device. The focus is to create a mezzanine module that minimizes the handling and formatting of the transceived data. The aims are to:

- Maximize data throughput
- Minimize latency
- Reduce FPGA design complexity
- Minimize system costs
- Reduce system overheads.

This standard takes a new approach on interface protocols by removing the need to inject protocol data into the raw data to be processed. It assumes that the FPGA has a unique closeness with the I/O mezzanine module. This enables modification of the FPGA to process the raw data formats that the module sources and sinks.

Although the key instigator for the data handling within this standard is the FPGA, it is not a prerequisite that an FPGA connects to the mezzanine module. However, the connected device must meet all the rules within this specification.

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The following people contributed to the development of this standard. Their participation is appreciated

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VSO and Other Standards

For further information on other standards from VSO, VME Product Directories, VME Handbooks, or general information on the VME market, please contact the VITA office at the address or telephone number on the front cover.

Change Bars

On document release, change bars will show revision changes.

Draft Summary

This is the preliminary draft standard. The original content of this draft standard was presented and agreed upon at the xxx VSO meeting. See the draft history for a summary list of the major changes to each draft.

Draft History

Draft No.	Date	Comments & Major Changes/Updates
D0.0	23 May, 2006	Preliminary Draft
D0.1	3 March 2007	Initial Draft for full review
D0.2	9 April 2007	Minor edits and appendix 1 added
D0.3	31 May 2007	Comments from Ballot included
D0.4	25 July 2007	Comments of Improvements from working group
D0.5	5 September 2007	Pin-out update, standoff change, double width 'notch', removed EPROM size, remove identification marks, removed 3.3V tolerant rule at power up
D0.6	13 September 2007	Dimensions for AMC and cPCI example, part numbers for connectors updated
D0.7	7 November 2007	Updates with comments from WG ballot
D0.8	22 November 2007	Finalized feedback from WG Ballot
D0.9	5 December 2007	Removed rules 5.18 and 5.19 from version 0.8
D0.10	21 December 2007	Removed reference to CLK0 and CLK1 for VREF pins.
D0.11	7 May 2008	Updates based on ANSI Ballot
D0.12	28 May 2008	Further updates based on ANSI Ballot and public review
D0.13	10 September 2008	Update following technical requests for updates
D0.14	17 September 2008	Updates from working group review
D0.15	8 December 2008	Initial updates from working group ballot
D0.16	18 February 2009	Final updates from working group
D0.17	25 March 2009	Added clarification regarding Vadj
D0.18	13 April 2009	Included Bidirectional clock support
D0.19	1 October 2009	Final edits following Ballot

Issues and Concerns to be Resolved

Following are some of the issues and concerns that need resolving before the final approval of this proposed standard:

None

1 Introduction

There is a greater need for different front panel IO functionality within systems in recent years. Typically, this front panel IO functionality was fixed on 3U or 6U form factor cards, or it was configured with PMC or XMC modules.

Previously, 3U and 6U form factor card design used a fixed front panel IO, which addressed a particular function. Changing the front panel IO functionality meant replacing the 3U or 6U cards.

PMC and XMC modules provided configurable front panel IO for 3U and 6U form factor cards. However, PMC and XMC modules use much of the 3U and 6U carrier card area.

This document provides a standard that describes a new IO mezzanine module. The module will connect to, but not be limited to, 3U and 6U form factor cards. The mezzanine module uses a smaller form factor compared with PMC or XMC modules. It assumes that it connects to an FPGA device or other device with reconfigurable IO capability.

1.1. Objectives

The objectives of this standard are to define:

- IO mezzanine modules, which connect to carrier cards
  - Supporting VME, VPX, VPX REDI, CompactPCI, CompactPCI Express, Advanced TCA, AMC, PCI and PCI Express Carriers, PXI and PXI Express Carriers.
- A family of high-speed connectors for IO mezzanine modules
  - Supporting up to 10 Gb/s transmission with adaptively equalized I/O
  - Supporting single ended and differential signaling up to 2 Gb/s
  - Numerous I/O available
- The electrical connectivity of the IO mezzanine module high-speed connector
  - Supporting a wide range of signaling standards
  - System configurable I/O functionality
  - FPGA intimacy
- The mechanical properties of the IO mezzanine module
  - Minimal size
  - Scalable from low end to high performance applications
  - Conduction and ruggedized support

1.2. FMC Overview

The FMC standard describes a versatile module, which can target a range of applications, environments, and markets. The specification defines a commercial grade version, which extends to cover a ruggedized conduction variant.

The specification of the double width modules helps applications that need additional carrier card bandwidth, greater front panel space, or a larger PCB area.

FPGAs provide a high pin count that can operate at many Gb/s. The latest connector technology is defined to maintain the high performance interface from the I/O on the mezzanine module, to the FPGA on the carrier card.

The FMC mezzanine module design minimizes design effort and resources. This can be seen through the removal of fixed protocols, minimal system support, and flexible pin allocation.

1.3. Standard Terminology

To clarify the requirements for compliance, many of the paragraphs in this standard are labeled with keywords. They indicate the type of information they contain. The keywords are:

> Rule
> Recommendation
> Suggestion
> Permission
> Observation

Any text not labeled with one of these keywords is descriptive. These are written in either a descriptive or a narrative style.

The keywords definitions are:

Rule <chapter>.<number>:
> Rules form the basic framework of this draft standard. They are expressed either in text form or in a figure, table, or drawing. All rules must be followed to ensure compatibility between card and backplane designs. All rules use the "shall" or "shall not" words to emphasize the importance of the rule. The "shall" or "shall not" words are reserved exclusively for stating rules in this draft standard and are not used for any other purpose.

Recommendation <chapter>.<number>:
> Designers are strongly advised to follow recommendations. They help to avoid poor performance or awkward problems. Recommendations in this standard are based on experience. They aim to guide designers to learn

quickly. All recommendations use the "should" or "should not" words to emphasize the importance of the recommendation. The "should" or "should not" words are reserved exclusively for stating recommendations in this draft standard and are not used for any other purpose.

Suggestion <chapter>.<number>:

A suggestion contains advice, which is helpful but not vital. The reader is encouraged to consider the advice. They help to make some design decisions, which are difficult until experience has been gained.

Permission <chapter>.<number>:

In some cases, a rule does not prohibit a certain design approach. However, the reader might wonder if their approach violates the spirit of the rule or might lead to some subtle problem. Permissions reassure the reader that a certain approach is acceptable and will cause no problems. All permissions use the "may" words to emphasize the importance of the permission. The lower-case "may" words are reserved exclusively for stating permissions in this draft standard and are not used for any other purpose.

Observation <chapter>.<number>:

Observations do not offer any specific advice. They usually follow naturally from a discussion. They spell out the implications of certain rules and bring attention to some items. They explain the reasoning behind certain rules.

1.4. FMC Definitions

FMC: FPGA Mezzanine Card

Board: Circuit card

CCA: Circuit Card Assembly

Carrier Card: A CCA that inserts into a carrier card (or backplane), which holds an FMC mezzanine module.

FMC Mezzanine Module: A PCB module that provides front panel IO for carrier cards.

FMC-RM: Ruggedized Conduction Cooled FMC IO Mezzanine Module

FMC-CM: Commercial Grade FMC IO Mezzanine Module

FMC -RC: Ruggedized Conduction Cooled FMC Carrier Card

FMC-CC: Commercial Grade FMC IO Carrier Card

Air cooled: A method of cooling active and passive components on a CCA using either natural free, or forced air convection

Conduction cooled: A method of cooling active and passive components on a CCA by using direct heat conduction.

Thermal Interface: Physical area allocated for direct mechanical contact to allow heat conduction from a lower level assembly to a higher-level assembly.

FPGA: Field Programmable Gate Array

HPC: High Pin Count Connector with 400 pins

LPC: Low Pin Count Connector with 160 pins

Pins: A physical mechanism to connect a signal between a carrier card and mezzanine module.

1.5. References

The following publications are for use with this standard.

The I^2C Bus Specification. Available from the Royal Philips Electronics web page at: http://www.semiconductors.philips.com/acrobat/various/I2C_BUS_SPECIFICATION_3.pdf

The following standards are available from the VMEbus International Trade Association. http://www.vita.com

ANSI/VITA-1-2002 VME64
ANSI/VITA-1.1-1997 VME64 Extensions
ANSI/VITA 20-2001 (R2005) Conduction Cooled PMC

The standard document for IPMI, Intelligent Platform Management interface, is at http://www.intel.com/design/servers/ipmi/

PCIMG standards are at http://www.picmg.org/

The following are available from their respective maintainers:

IEEE 1149.1-2001 Standard Test Access Port and Boundary-Scan Architecture

ISO 4527 Autocatalytic Nickel Phosphorus Coatings - Specification and Test Methods

ISO 7599 Anodizing of Aluminum and Its Alloys – General Specification for Anodic Oxide Coating on Aluminum

If any of the above standards are revised, use the revised standard unless it conflicts with this document.

1.6. Dimensions

All drawings use millimeters (mm) unless stated otherwise.

2 FMC Compliance

2.1. FMC Mezzanine Module's Minimum Features

Rule 2.1: To label a mezzanine module as FMC compliant, the IO mezzanine module shall comply with all appropriate requirements in this document.

Rule 2.2: Have provision for the mechanical constraints associated with the IO mezzanine modules.

Rule 2.3: If there are conflicts between this standard and a referenced standard or specification, this standard takes precedence.

2.2. FMC Carrier Card's Minimum Features

Rule 2.4: To label a carrier card as FMC compliant, the carrier card shall comply with all appropriate requirements in this document.

Rule 2.5: Provide a minimum of one FMC slot, which supports, as a minimum, the connector specification for a low pin count.

Rule 2.6: Have provision for the mechanical constraints associated with the carrier card.

Rule 2.7: If there are conflicts between this standard and a referenced standard or specification, this standard takes precedence.

3 FMC Mezzanine Module

3.1. Overview

This section of the specification describes the IO mezzanine module mechanical dimensions. The IO mezzanine module has two defined sizes that are referred to as a single width, and a double width module. The single width module has a width of 69mm and the double width module has a width of 139mm.
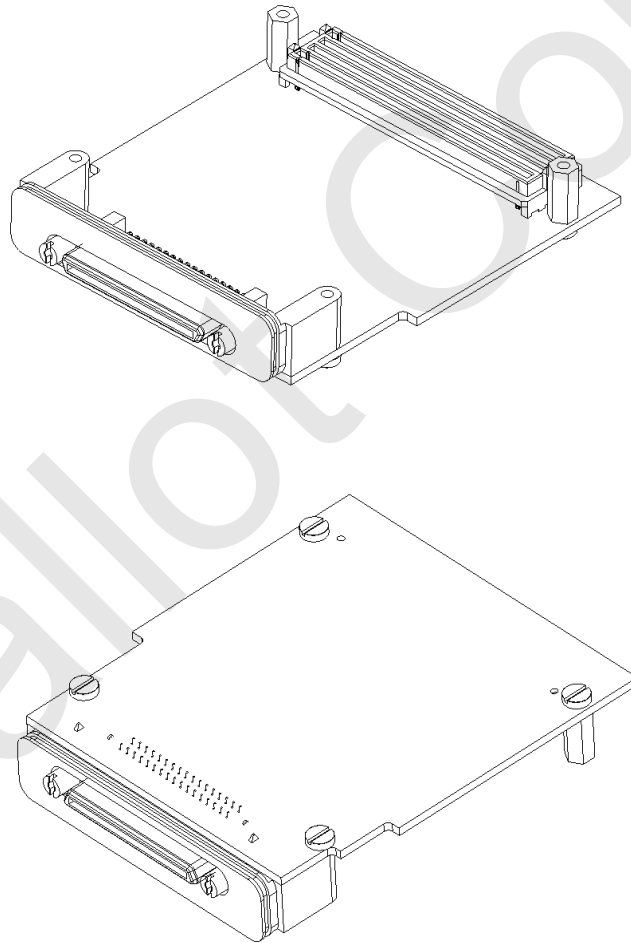
Figure 1.   Typical example of single width commercial grade FMC Module
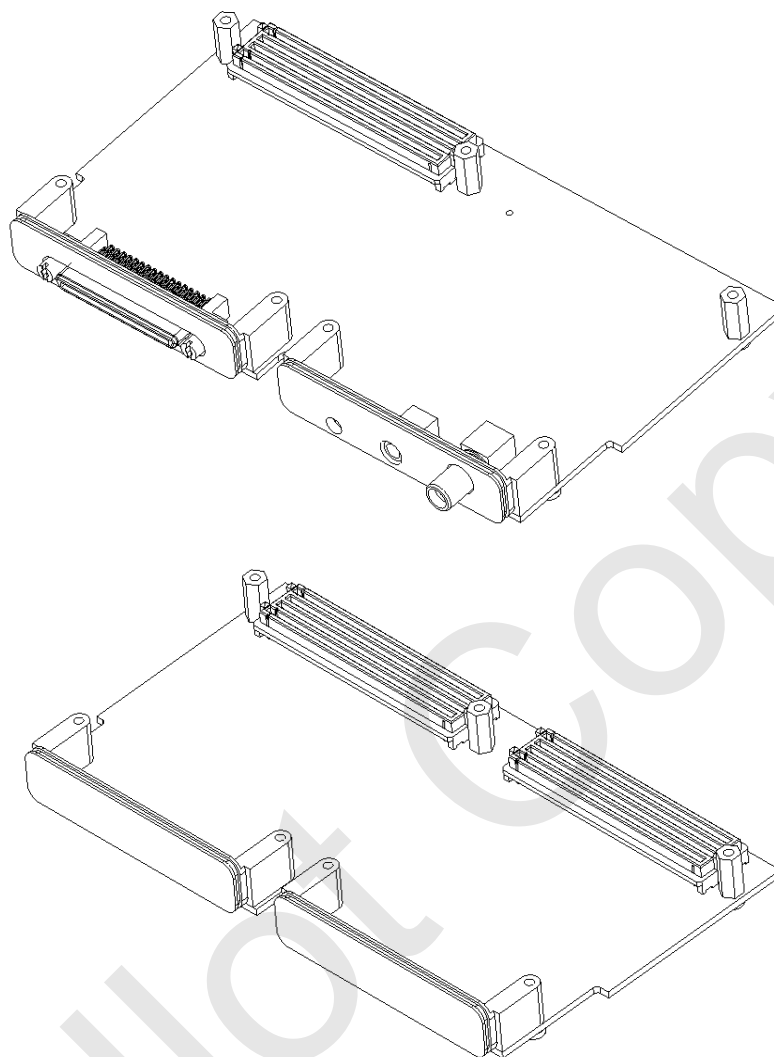
Figure 2.   Typical example of double width commercial grade FMC Module

The FMC mezzanine module uses a high-pin count 400 pin high-speed array connector, HPC. A mechanically compatible low-pin count, LPC, connector with 160 pins can also be used with any of the form factors detailed in this standard.

It is expected that the FMC will be used in a wide range of markets, environments, and carrier card form factors supporting a wide range of I/O interfaces. The standard describes options to create modules for operating in a range of environments from passively cooled to fully ruggedized conduction cooled.

For clarity in this document, Figure 3 provides definitions for the descriptors used.
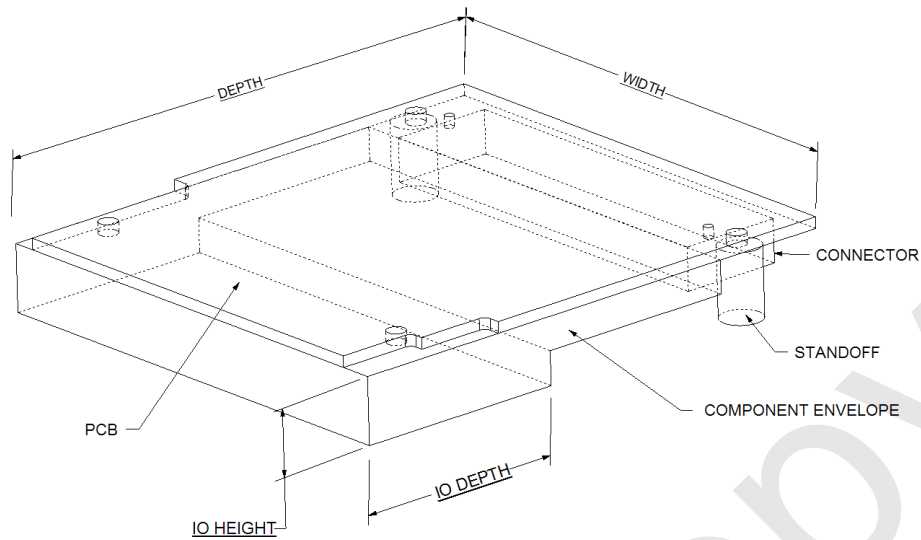
Figure 3.   Dimensional descriptors for FMC Mezzanine Module

The PCB side with the FMC connector mounted is described as side 1, the other side of the module's PCB is described as side 2.

The FMC Mezzanine module has three defined regions. This enables construction of different but compatible variants of the mezzanine module to suit the module's environment.
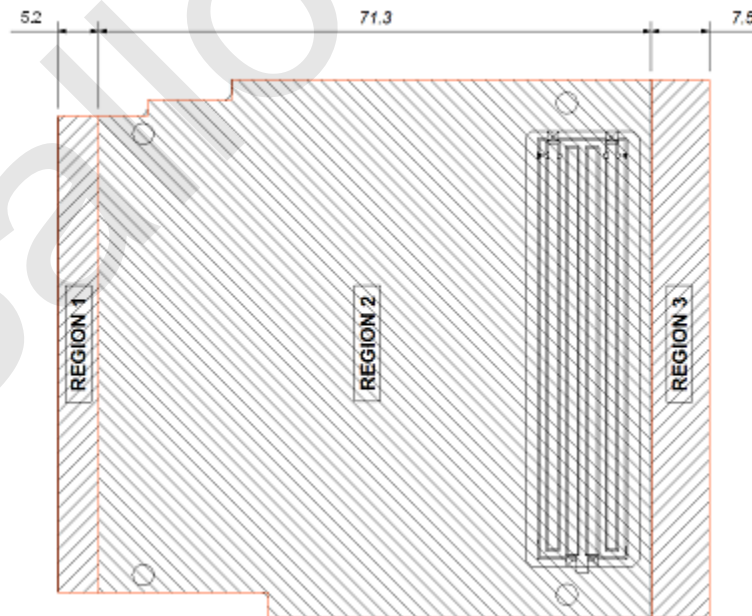
Figure 4.   PCB regions of Mezzanine module

The standard supports three combinations of these regions:

1. Regions 1 and 2 – Typically used on air cooled commercial grade carrier cards
2. Regions 2 and 3 – Typically used on ruggedized conduction cooled carrier cards
3. Regions 1, 2 and 3 – Typically used on ruggedized carrier cards needing region 1

This document describes the standard air cooled version of the mezzanine module that typically targets commercial grade applications. For environments that require conduction cooled and ruggedized capabilities, Section 3.5 defines additional constraints to be applied to support this capability.

3.2. Single Width Mezzanine Module

The single width FMC mezzanine module typically uses only regions 1 and 2. Figure 5 shows the mechanical dimensions of the air cooled non-rugged version of the mezzanine module.
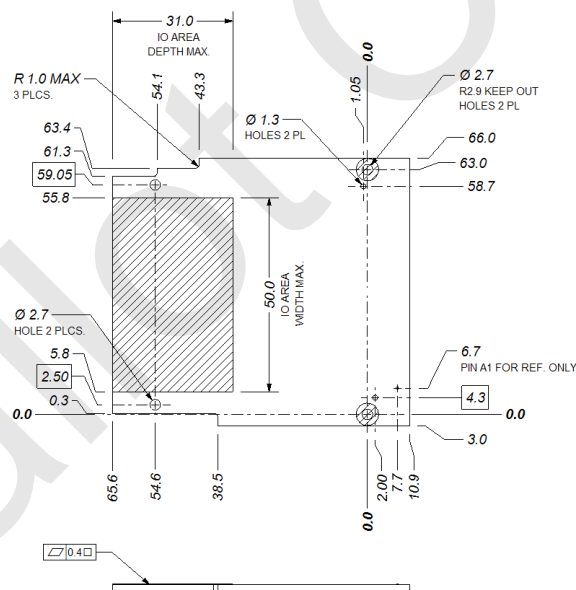
Figure 5.   Single Width Commercial Grade FMC Module Mechanical

Rule 3.1: Single width commercial grade modules shall meet the dimensions of Figure 5, with the option to add region 3 as defined in Figure 4 of the PCB, and the option to remove region 1 when no front panel I/O is required.

Rule 3.2: Single width modules shall have one connector, denoted as P1, between the mezzanine module and the carrier card.

Rule 3.3: The position of the connector P1 is highlighted in Figure 5 for commercial grade form factors.

3.3. Double Width Mezzanine Module

Figure 6 provides the mechanical dimension data for the double width FMC module.
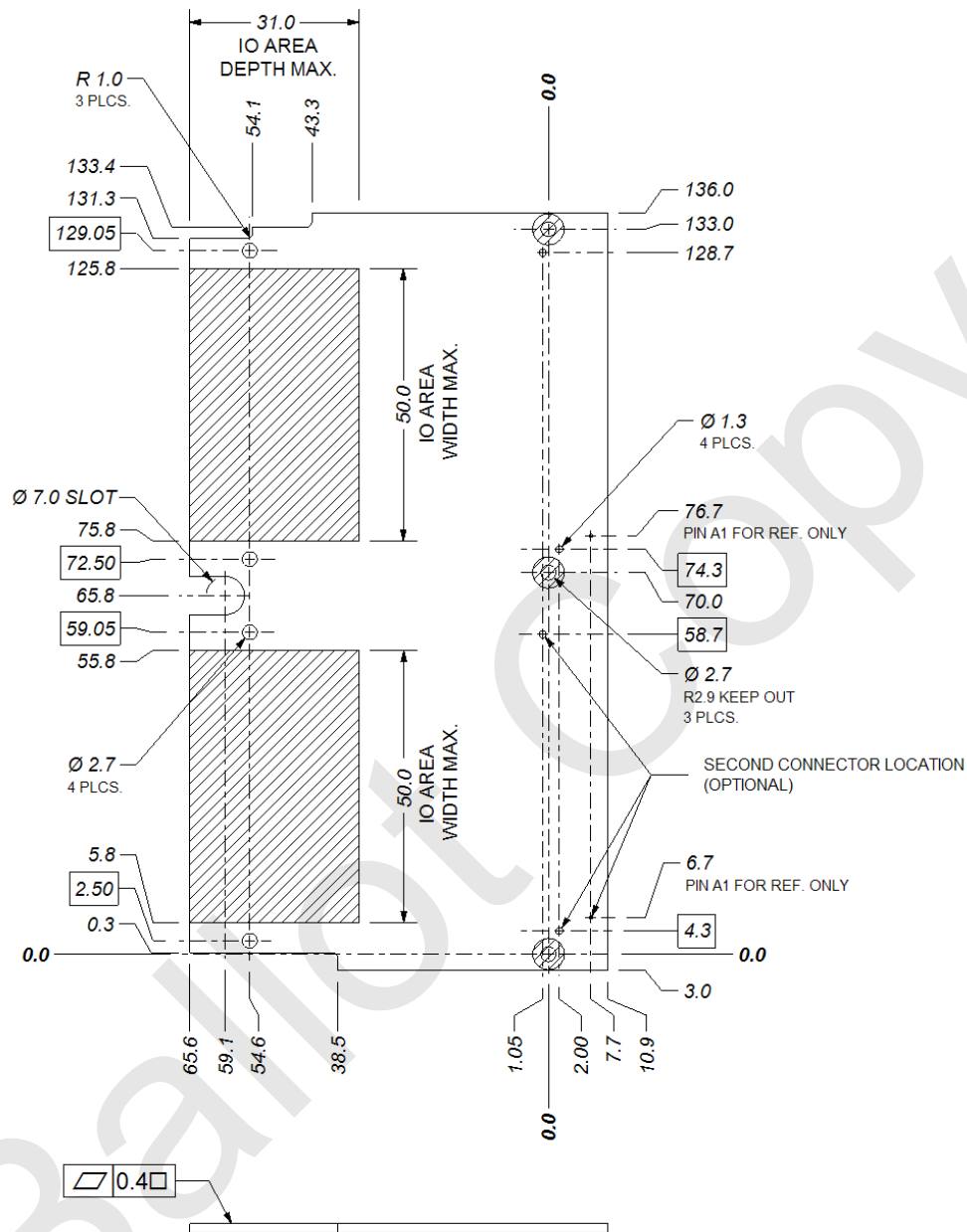
Figure 6.   Double Width Commercial Grade FMC Module Mechanical

Rule 3.4.: The connectors on a double width module shall be denoted as P1 for the primary and P2 for the secondary.

Rule 3.5: Double width commercial grade modules shall meet the dimensions of Figure 6

Rule 3.6: Double width modules shall have at least the P1 connector. A double width using the single connector is illustrated in Figure 7.

P1
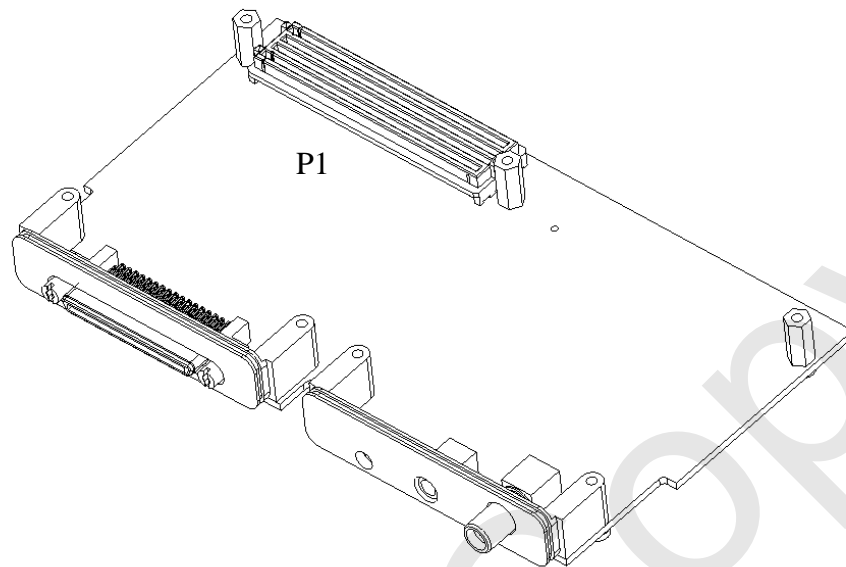
Figure 7.   Double width with only primary connector, P1

Permission 3.1: Double width modules may have two connectors P1 and P2. A double width module with two connectors populated is illustrated in Figure 8

P1

P2
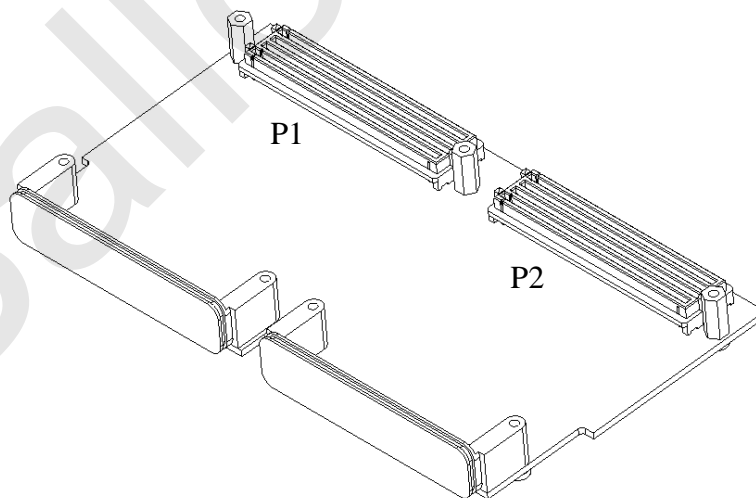
Figure 8.   Double width with both connectors, P1 and P2

Rule 3.7: The position of the connector P1 and the optional connector P2 is shown in Figure 8.

Recommendation 3.1: For double width modules with an HPC and an LPC connector, P1 should be the HPC connector. Carrier cards can be designed to reflect this priority.

Observation 3.1: Do not assume that the signals on the P1 and P2 are connected to the same FPGA. It is feasible that the signals on P1 connect to one FPGA and the signals on P2 connect to a different FPGA.

3.4. Connectors

Two versions of the electro-mechanically compatible connector can be used on commercial grade and conduction cooled form factors. The high-pin count connector has 400 contacts arranged in a 10x40 array. The low-pin count connector has 160 contacts and consists of two 2x40 rows of contacts within the 10x40 connector shell.

Rule 3.8: FMC carrier cards, which support the high-pin count connector, shall use connector type CC-HPC-10[1] or CC-HPC-10L[2].

Rule 3.9: FMC carrier cards, which support the low-pin count connector, shall use connector type CC-LPC-10[3] or CC-LPC-10L[4].

Rule 3.10: FMC IO mezzanine modules with a 10mm stacking height, which use the high-pin count connector, shall use connector type MC-HPC-10[5] or MC-HPC-10L[6].

Rule 3.11: FMC IO mezzanine modules with an 8.5mm stacking height, which use the high-pin count connector, shall use connector type MC-HPC-8.5[7] or MC-HPC-8.5L[8].

Rule 3.12: FMC IO mezzanine modules with a 10mm stacking height, which use the low-pin count connector, shall use connector type MC-LPC-10[9] or MC-LPC-10L[10].

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[1] CC-HPC-10 :   Samtec Part Number ASP-134486-01 or equivalent
[2] CC-HPC-10L: Samtec Part Number ASP-134485-01 or equivalent
[3] CC-LPC-10 :   Samtec Part Number ASP-134603-01 or equivalent
[4] CC-LPC-10L: Samtec Part Number ASP-127796-01 or equivalent
[5] MC-HPC-10 :   Samtec Part Number ASP-134488-01 or equivalent
[6] MC-HPC-10L: Samtec Part Number ASP-134487-01 or equivalent
[7] MC-HPC-8.5:   Samtec Part Number ASP-134602-01 or equivalent
[8] MC-HPC-8.5L: Samtec Part Number ASP-134601-01 or equivalent
[9] MC-LPC-10 :   Samtec Part Number ASP-134604-01 or equivalent
[10] MC-LPC-10L: Samtec Part Number ASP-127797-01 or equivalent

Rule 3.13: FMC IO mezzanine modules with an 8.5mm stacking height, which use the low-pin count connector, shall use connector type MC-LPC-8.5[11] or MC-LPC-8.5L[12].

Recommendation 3.2: Connector CC-HPC-10L should be used in place of CC-HPC-10 when a leaded process is required.

Recommendation 3.3: Connector CC-LPC-10L should be used in place of CC-LPC-10 when a leaded process is required.

Recommendation 3.4: Connector MC-HPC-10L should be used in place of MC-HPC-10 when a leaded process is required.

Recommendation 3.5: Connector MC-HPC-8.5L should be used in place of MC-HPC-8.5 when a leaded process is required.

Recommendation 3.6: Connector MC-LPC-10L should be used in place of MC-LPC-10 when a leaded process is required.

Recommendation 3.7: Connector MC-LPC-8.5L should be used in place of MC-LPC-8.5 when a leaded process is required.

Rule 3.14: The high-pin count, HPC, connectors shall have a possible 400 pins for signal assignment, arranged in a 10x40 array.

Rule 3.15: The low-pin count, LPC, connectors shall have a possible 160 pins for signal assignment, arranged in a two 2x40 arrays.

3.4.1. Variable stacking heights

The default stacking height for the mezzanine module is 10mm, however different stacking heights down to 8.5mm are allowed, but the component envelopes from side 1 shall be translated to the component envelope on side 2.

Figure 9 illustrates the extremes of the component envelopes for a maximum stacking height of 10mm and a minimum stacking height of 8.5mm.

Rule 3.16: Stacking heights from 8.5mm to 10mm shall be allowed

Rule 3.17: The stacking height shall be adjusted by changing only the connector on the mezzanine module.

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[11] MC-LPC-8.5:   Samtec Part Number ASP-134606-01 or equivalent
[12] MC-LPC-8.5L: Samtec Part Number ASP-134605-01 or equivalent

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Rule 3.18: Manufacturers of standard FMC carrier cards shall have no components greater than 8.5mm tall within the area that overlaps with region 3 of the module slot.
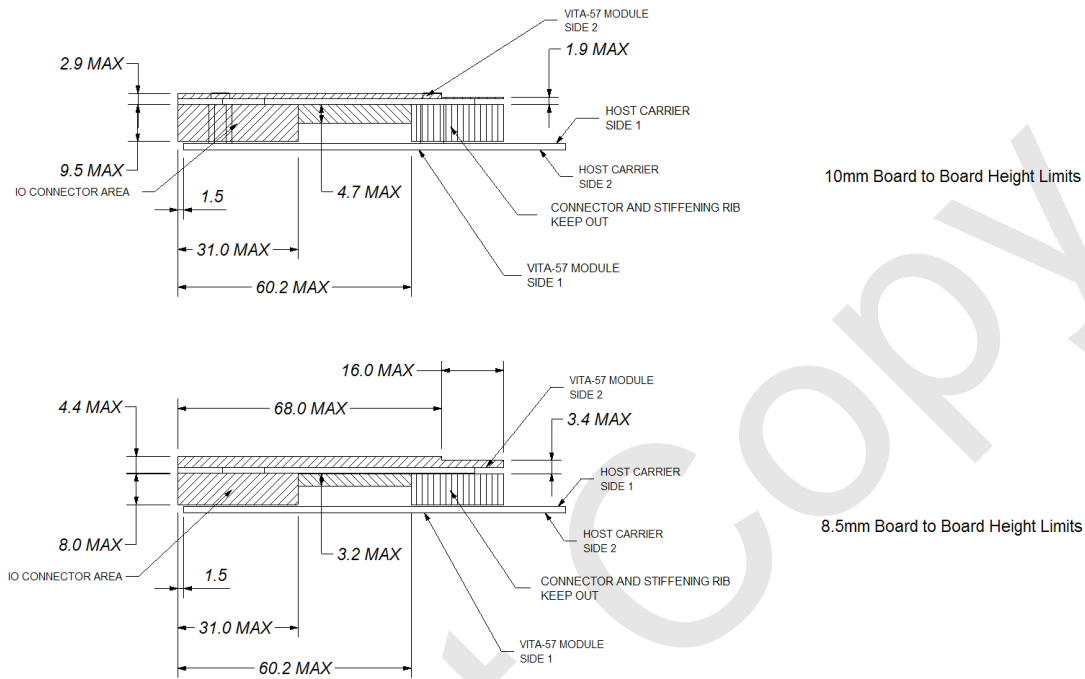
Figure 9.   Board to board height limits: 10mm and 8.5mm heights

Observation 3.2: The component envelope on side 2 is reduced by 16mm at the rear of the module. This allows the support of an FMC slot on mid-size AMC modules.

3.4.2. Ground connections

Rule 3.19: To prevent ground loop problems, the FMC front panel bezel shall be electrically isolated from the circuit ground on the mezzanine module.

Rule 3.20: Boards shall provide a minimum of 500Vdc and 1 MΩ of isolation between the FMC front panel bezel and the mezzanine circuit ground.

Rule 3.21: To prevent ground loop problems, the front panel of the FMC carrier card shall be electrically isolated from the circuit ground of the carrier card.

Rule 3.22: Boards shall provide a minimum of 500Vdc and 1 MΩ of isolation between the front panel of the carrier card and the carrier-card circuit ground.

Permission 3.2: More isolation may be required depending on system requirements.

Rule 3.23: The required standoffs located adjacent to P1 connector (and P2 connector on double width modules), shall be tied to the mezzanine module's chassis ground, or AC coupled to the mezzanine module's circuit ground, so that they do not float and create unwanted antennas.

Rule 3.24: The required standoffs located adjacent to P1 connector (and P2 connector on double width modules), shall be tied to the carrier card's chassis ground, or AC coupled to the carrier card's circuit ground, so that they do not float and create unwanted antennas.

Observation 3.3: If AC coupled to circuit ground the capacitor shall meet the requirements of Rule 3.20

Rule 3.25: All keying holes shall remain electrically isolated from the mezzanine module's circuit ground.

Rule 3.26: The FMC front panel bezel shall be attached to the carrier card chassis ground.

3.4.3. Connector Pads and Labeling

Figure 10 shows the connector pad layout that shall be used for the FMC connector present on a carrier card. Figure 11 shows the connector pad layout that shall be used for the FMC connector present on an IO mezzanine module. The alphanumeric grid labeling shown shall override any proprietary pin labeling conventions used by the connector manufacturer.
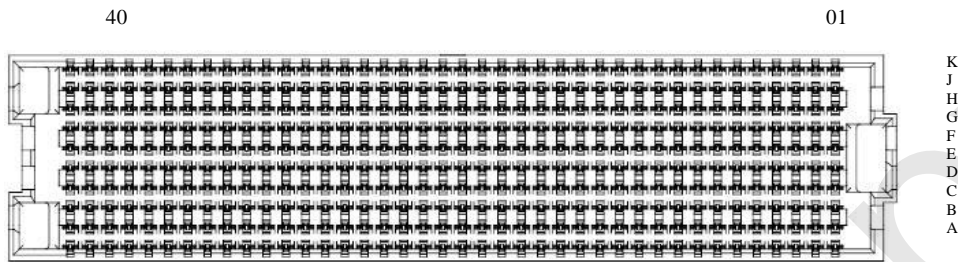
Figure 10. Carrier Card Connector Grid Labeling (Component Side View)
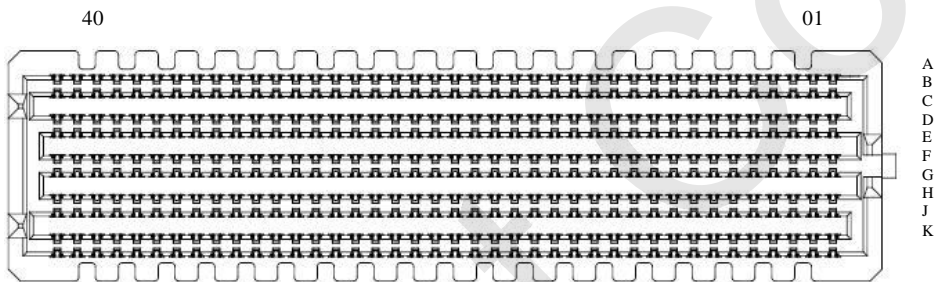
Figure 11. FMC Module Connector Grid Labeling (Component Side View)

3.4.4. Connector Assembly

Rule 3.27: Assembly of FMC connectors shall be within maximum tolerance, (MT), +/- 0.13 mm of true position (TP) in any axis parallel to the plane of the PCB.

Rule 3.28: For double width modules with P1 and P2 populated, MT is the total tolerance that is available for both connectors relative to a common reference point and is split evenly. Therefore, each connector has a maximum tolerance of +/- 0.065 mm of TP.

Rule 3.29: For carrier cards that accept double width modules, MT is the total tolerance that is available for both connectors relative to a common reference point and is split evenly. Therefore, each connector has a maximum tolerance of +/- 0.065 mm of TP.

Rule 3.30: MT shall be split evenly between the IO Mezzanine Module and the mating connector on the carrier card.

Rule 3.31: TP is defined as a point on the PCB near a connector, that the assembly equipment uses as a reference, to position the connectors before soldering.

Rule 3.32: The angular misalignment of any connector shall not exceed 0.066 degrees, or shall not exceed 0.065mm, along either the length or the width.

Rule 3.33: The solder thickness variation between the connector contacts and the solder-coated surfaces on the PCB shall not exceed 0.1mm. Excessive build up of solder under the connector contacts causes the connector to mount too high.

Observation 3.4: The rules within this section ensure that the maximum allowable misalignment between any two mating connectors is 0.13mm. Using a double width module, halves the tolerances to 0.065mm

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3.5. Conduction Cooled Mezzanine Modules

3.5.1. Single Width Module

The second form factor is a ruggedized conduction cooled form factor. This prepares the IO mezzanine module for use in harsher environments than those targeted by the commercial grade version of the standard.

Typical implementations of the PCB use only regions 2 and 3 as defined in Figure 4. Figure 12 illustrates an example of a ruggedized FMC mezzanine module that contains regions 2 and 3.

Figure 12. Typical example of single width conduction cooled FMC Module with primary and secondary thermal interfaces

Figure 13. Single Width Conduction Cooled FMC Module Mechanical
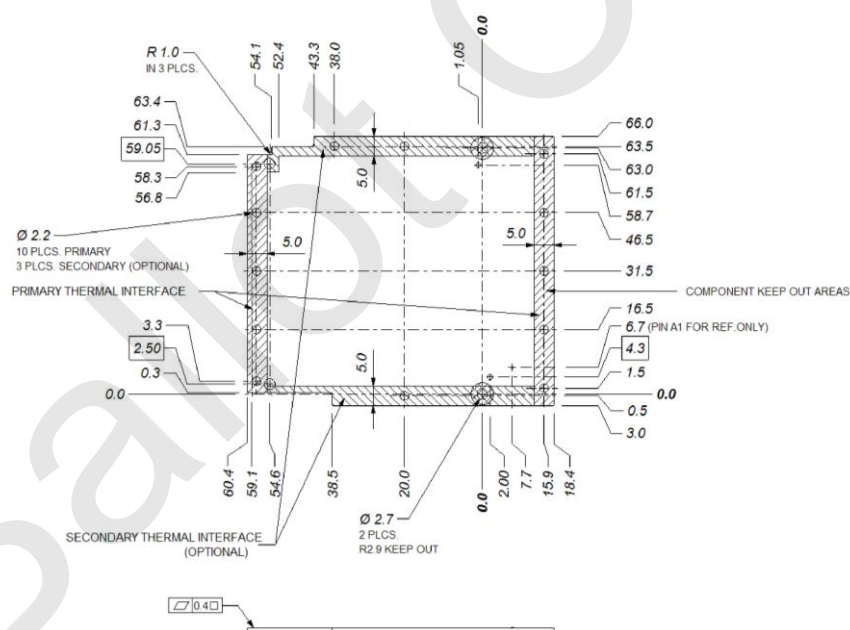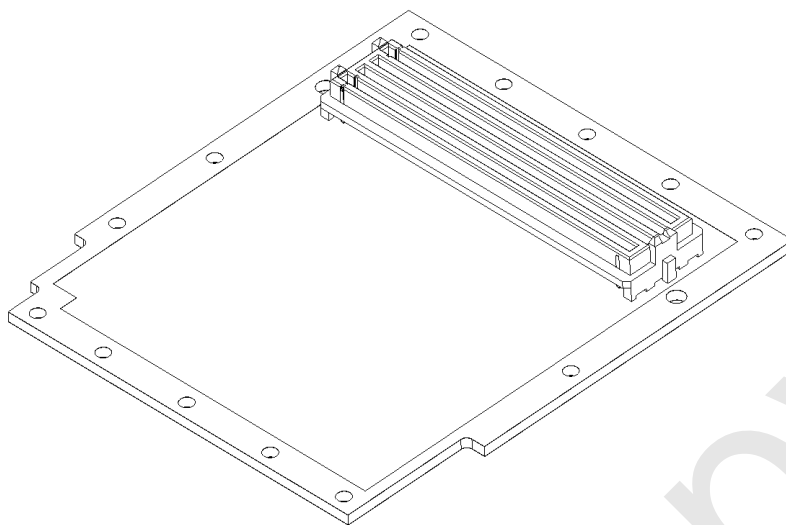
The thermal interfaces to the carrier card in the conduction cooled form factor cause minimum restriction to the mezzanine component area. This is achieved using the front panel and central stiffening bar areas, normally associated with conduction cooled assemblies. Additional thermal interfaces are optional to improve thermal performance, but they reduce the component area.

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Rule 3.34: Single width conduction cooled grade modules shall meet the dimensions of Figure 13 with the option of including region 1 as defined in Figure 4.

Rule 3.35: The position of the connector P1 is highlighted in Figure 13 by the positioning of pin A1 of the connector for conduction cooled form factors.

Rule 3.36: Conduction cooled mezzanine modules shall only have a stacking height of 10mm.

Rule 3.37: Any mezzanine module, conduction cooled or air cooled, that has a region 3 shall only have a stacking height of 10mm.

Rule 3.38: Conduction cooled ruggedized mezzanine modules shall be designed to fit on air cooled FMC carrier cards.

Permission 3.3: Conductors, for example, traces, pads, and via holes, located in FMC conduction cooled mezzanine module component keep out areas, should be electrically insulated to prevent electrical problems when interfacing to conductive surfaces. Solder mask and gasket pads are proven to be effective electrical insulation.

Observation 3.5: Optimal mechanical and thermal performance is obtained by using all screw fastening locations.

The commercial grade, form factor standard for the FMC mezzanine module defines a printed circuit board (PCB) profile that extends beyond the component boundary of a typical ruggedized VME and VPX carrier card. Therefore, the PCB length must be reduced by 5.25mm, by removing region 1, at the front panel to comply with IEEE 1101.2. In addition to this reduction at the front panel, the conduction-cooled form-factor extends by 7.5mm (region 3) at the rear of the module. This means the module can attach directly to the center rib located on VME and VPX carrier cards.

The reduction in length does not affect the bezel holes on the front panel. Therefore, compatibility with air cooled carrier card assemblies is maintained. Similarly, the carrier card zero-component-height and mezzanine module component I/O boundary areas are maintained. This means the mezzanine module artwork can accommodate front panel I/O as well as increased component heights. The position of the FMC front edge and main connector P1 are unchanged with respect to the front edge of the carrier card.

3.5.2. Double Width Module

A double width variant of the FMC conduction cooled mezzanine module is also defined.
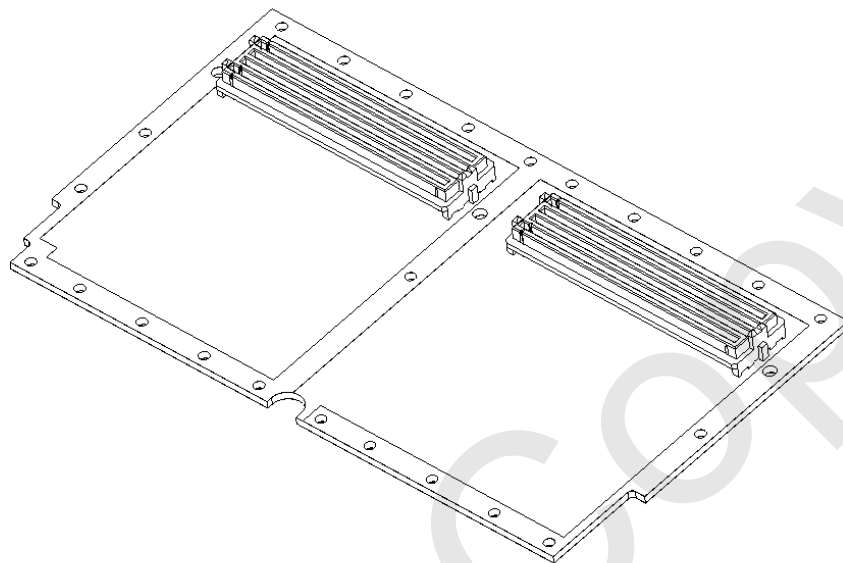
Figure 14. Example of double width conduction cooled FMC Module
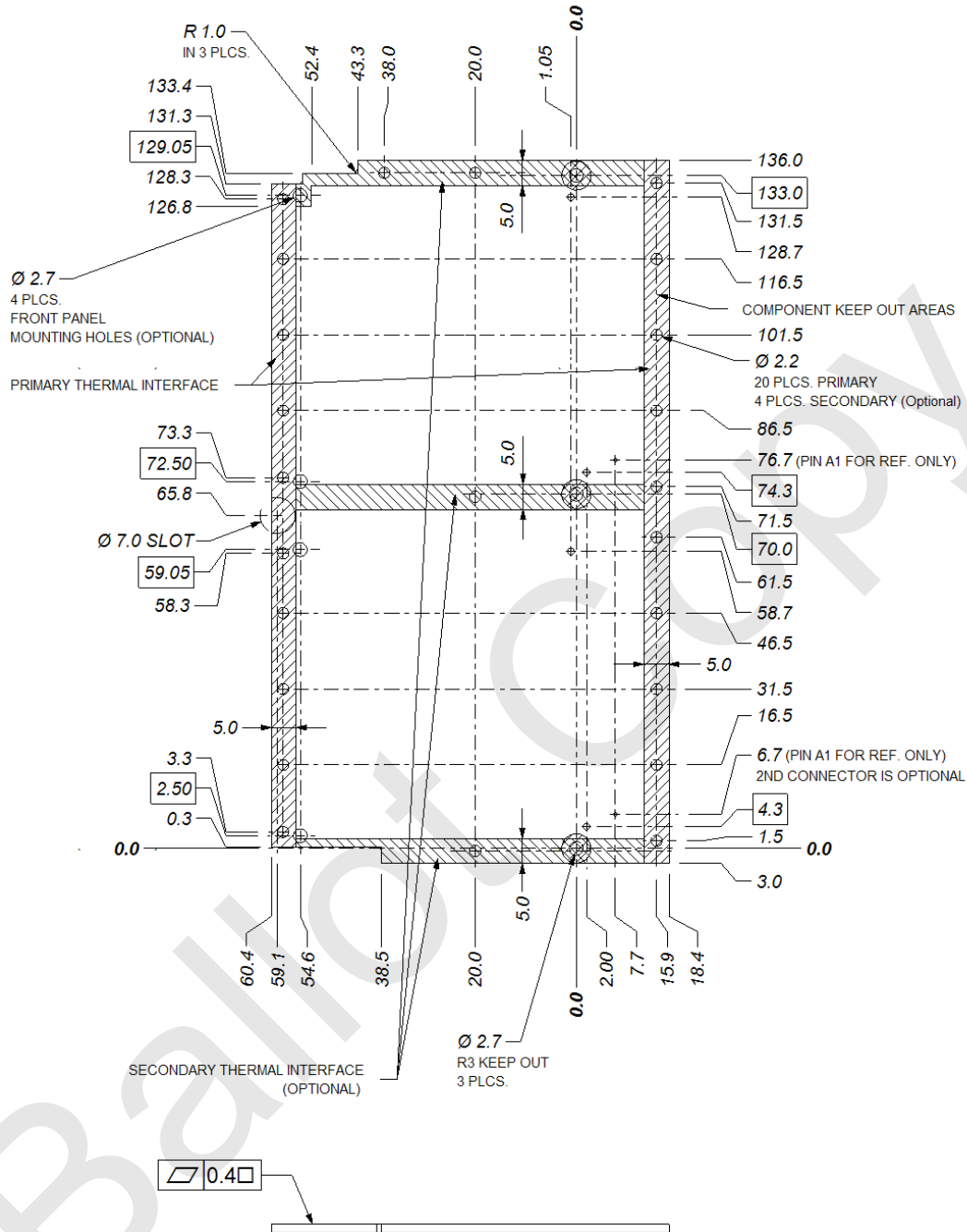
Figure 15. Double width Conduction Cooled FMC Mezzanine Module Mechanical

Rule 3.39: Double width conduction cooled grade modules shall meet the dimensions of Figure 15 with the option of including region 1 as defined in Figure 4.

3.5.3. Conduction Cooled

Permission 3.4: A conduction cooled carrier card may be designed with either fixed or removable primary ribs.

Permission 3.5: Conduction cooled carrier cards may provide a mechanism to allow fitting of an air cooled FMC.

Observation 3.6: The thermal and stiffening ribs on a conduction cooled host card protrude into the physical envelope of an air cooled FMC mezzanine module. For complete compatibility with air cooled FMC mezzanine modules, the ribs have to be removed.

Observation 3.7: Carrier cards requiring maximum compatibility with mezzanine modules should facilitate removal of the secondary ruggedization ribs.

Rule 3.40: Electrical ground returns shall not be made through the thermal interface.

3.5.4. Thermal Interfaces

Rule 3.41: Primary thermal interfaces shall be included on FMC mezzanine modules and carrier cards.

Permission 3.6: To improve thermal performance, secondary thermal interfaces may be added to a VITA mezzanine module on either or both sides of the module.

Rule 3.42: FMC Mezzanine modules using secondary thermal interfaces shall be designed for cooling from the primary interfaces and either of the secondary thermal interfaces located on its left or right extremity only. However, modules using secondary thermal interfaces shall have both right and left side interfaces.

Permission 3.7: For host cards designed with a single FMC site only, provision may be made for cooling from both the left and right secondary thermal interfaces for enhanced thermal performance.

Rule 3.43: Carrier card designs shall be capable of being configured to accommodate all possible thermal interfaces specified in this standard

Rule 3.44: Thermal conducting surfaces of both the mezzanine modules and the carrier card shall be straight, and have flatness of 0.002 mm per mm of

length or better. The surface roughness shall be RMS 0.65 μm (24 micro in) or better.

Observation 3.8: Flatness and surface finish are critical in attaining the best thermal impedance requirement.

Rule 3.45: The thermal conducting surfaces of both the mezzanine module and the carrier card shall be corrosion resistant or treated to resist corrosion.

Observation 3.9: Corrosion products on conduction clamping surfaces have been shown to substantially degrade thermal performance over time.

Permission 3.8: Aluminum structure may be sulphuric anodized and sealed to meet this rule, ref: ISO 7599.

Observation 3.10: Hard anodizing is not recommended as the hard oxide case substantially reduces heat transfer.

Permission 3.9: Aluminum structure may be electrolyses nickel plated to meet this rule, ref: ISO 4527.

3.5.5. Air cooled and conduction cooled compatibility

The principals of compatibility between air cooled and conduction cooled FMC modules with air cooled and conduction cooled carrier cards are similar to CCPMC described in the VITA 20 Conduction Cooled PMC standard.

The data within this standard is provided for completeness and to highlight two key differences. In particular, the permission to have region 1 available on conduction cooled mezzanine modules, and to allow front panel I/O from the mezzanine connector to the carrier card.

This leads to the six types of FMC that we need to consider for compatibility

1. Air cooled FMCs with front panel I/O
2. Air cooled FMCs without any front panel I/O (for example, memory expansion card)
3. Conduction cooled FMCs with front panel I/O
4. Conduction cooled FMCs without front panel I/O
5. Conduction cooled FMCs with region 1 and front panel I/O
6. Conduction cooled FMCs with region 1 and without front panel I/O

Other considerations are these three types of carrier cards:

1. Air cooled carrier cards
2. Conduction cooled carrier cards with fixed ribs
3. Conduction cooled carrier cards with removable ribs.

The following table describes compatibility between the FMC mezzanine modules and the carrier cards. "Fully compatible" means that the mezzanine module can be fitted on top of that carrier card without interference. The goal is that all conduction cooled mezzanine modules can be fitted on both air cooled and conduction cooled carrier cards. Also air cooled mezzanine modules can be fitted on conduction cooled carrier cards with removable ribs for use in a development environment.

	Air cooled FMC module with front panel I/O	Air cooled FMC module without front panel I/O	Conduction cooled FMC module without front panel I/O	Conduction cooled FMC module with front panel I/O	Conduction cooled FMC module with region 1 but without front panel I/O	Conduction cooled FMC module with region 1 but with front panel I/O
Air cooled host card	Fully Compatible	Fully Compatible	Fully Compatible	Fully Compatible	Fully Compatible	Fully Compatible
Conduction cooled host card (fixed rib)	Not Compatible	Not Compatible (note 1)	Fully Compatible (note 4)	Not Compatible (note 3) (note 4)	Not Compatible (note 1) (note 4)	Not Compatible (note 3) (note 4)
Conduction cooled host card (removable rib)	Lab Compatible (note 2)	Lab Compatible (note 2)	Fully Compatible (note 4)	Fully Compatible (note 3)	Fully Compatible (note 5)	Fully Compatible (note 3) (note 5)

Table 1.   Module and carrier card compatibility

Notes:
1. Air cooled mezzanine modules and conduction cooled modules with region 1 that do not have front panel I/O could be compatible with conduction cooled carrier cards with fixed ribs if components on the mezzanine module do not interfere with the stiffening ribs on the carrier card.
2. Although air cooled mezzanine modules can be fitted on conduction cooled carrier cards with removable ribs, these mezzanine modules may not have been designed to operate in a deployable environment. It is expected that this combination would only be used in a laboratory or prototyping environment.
3. Conduction cooled mezzanine modules with front panel I/O will require a modification to the front panel rib. This will affect thermal and structural performance.
4. Conduction cooled carrier cards may have to be configured to accept a specific conduction cooled mezzanine module, depending on use of optional thermal interfaces.
5. Conduction cooled carrier cards may have to be configured to accept a specific conduction cooled mezzanine module with region 1.

3.6. FMC Front Panel Bezel

The FMC front panel bezel has two basic parts: the bezel and the EMC gasket.

> **Permission 3.10:** The bezel of a FMC module may be used when the stiffener bar on the carrier card is not present; this is the typical use in commercial grade mezzanine modules.

> **Rule 3.46:** Each FMC Mezzanine module shall be designed to accommodate a bezel.

The main function of the front panel bezel is for the mounting of front panel I/O connectors and, if necessary, special indicators and switches. Since standard-size bezels are used, the FMC mezzanine module can fit into any host, which provides a FMC slot. Figure 16 shows the mechanical design of the FMC front panel bezel.

The two legs on the bezel also provide the standoffs for the front portion of the mezzanine card.

> **Rule 3.47:** The height of these legs shall be the same as the two standoffs used adjacent to the FMC connector.

> **Recommendation 3.8:** The standoffs adjacent to the FMC connector should use 4.5mm face to face hex standoffs, to allow for rotation of the standoffs

> **Observation 3.11:** The standoffs adjacent to the FMC connector can be 5mm face to face hex standoffs, however the standoffs will have to be correctly orientated.
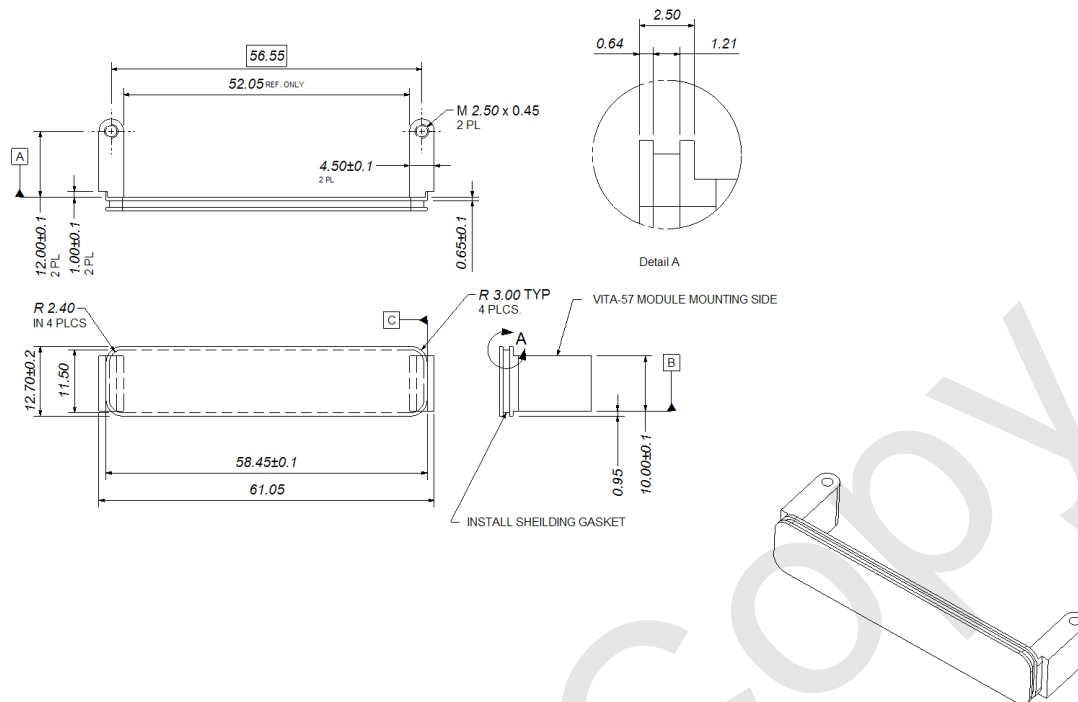
Figure 16. FMC Front Panel Bezel Mechanical Dimensions

If the FMC PCB is moved up or down within the FMC envelope, the bezel leg height needs to be adjusted accordingly. See Figure 9 for this relationship.

Rule 3.48: The center horizontal line of the FMC front panel bezel shall always be 5.4 mm above the host side 1 surface, for the 10 mm stacking height.

Observation 3.12: Note that if the FMC PCB is moved up or down, the FMC front panel bezel's centerline does not move. The bezel always maintains the same relationship with the host's side 1 surface and host front panel (face plate).

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3.6.1. FMC Mezzanine Module to Carrier Card relationship

It is very important to measure the fully assembled FMC Mezzanine modules. When the module is installed in a host FMC slot, it needs to match when providing I/O out of the front panel. Figure 17 illustrates the alignment parameters between the mezzanine module and the carrier card to ensure compatibility for providing I/O capability at the front panel of the carrier card.

Rule 3.49: When providing I/O out of the front panel of a FMC carrier card, the FMC mezzanine module's front panel bezel shall be aligned with the carrier card's FMC slot opening.

Observation 3.13: Due to tolerance build-up, this will not match. The mismatch may be as much as ±0.3 mm.

ONLY 10.00 SUPPORTED

3.75

Rugged board alignment

10.00 AND 8.00 SUPPORTED

5.00

1.50

Commercial board alignment
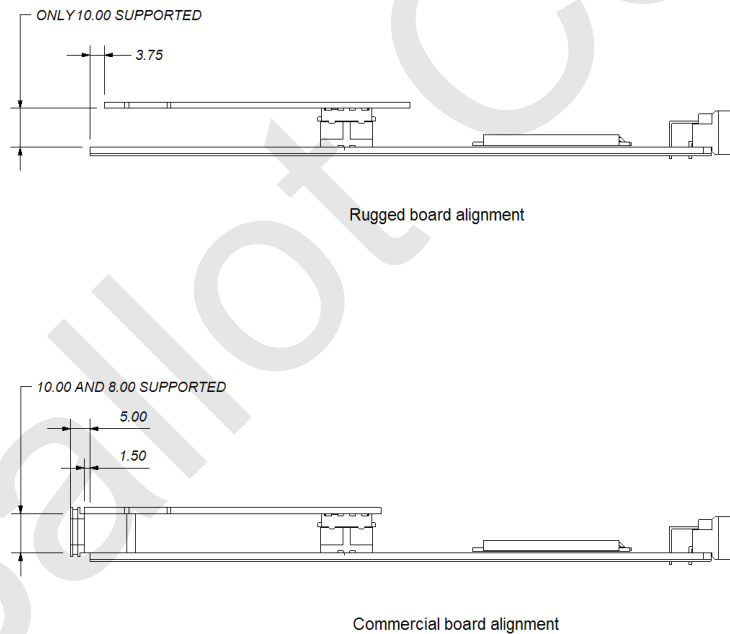
Figure 17. FMC Mezzanine Module to Carrier Card dimensions

Observation 3.14: The module to card positioning assumes that there is a 2mm front panel. If this is not case such as in AMC, then the carrier card designer should consider the position of the FMC slot to provide a flush front panel with the standard bezel.

4 FMC Carrier Card

4.1. Overview

An FMC carrier card provides slots that accept FMC Mezzanine modules. A typical 3U carrier card will be able to accept a single FMC mezzanine module located at the front panel. A typical 6U carrier card can support up to 3 single width FMC mezzanine modules, two of these slots can potentially accept one double width mezzanine module, see Figure 18. There is no requirement to have the maximum number of slots on a carrier card; this is left to the carrier card designer to specify the quantity of FMC slots required.
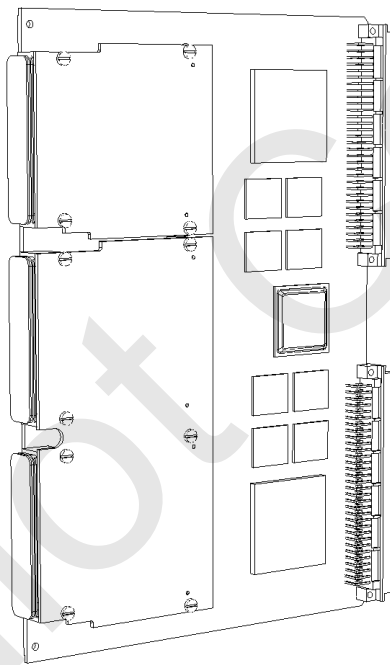
Figure 18. Typical 6U carrier card with double and single width module

Permission 4.1: If FMC carrier cards do not have the requirement to bring I/O out of its front panel the FMC may be placed freely on the carrier card.
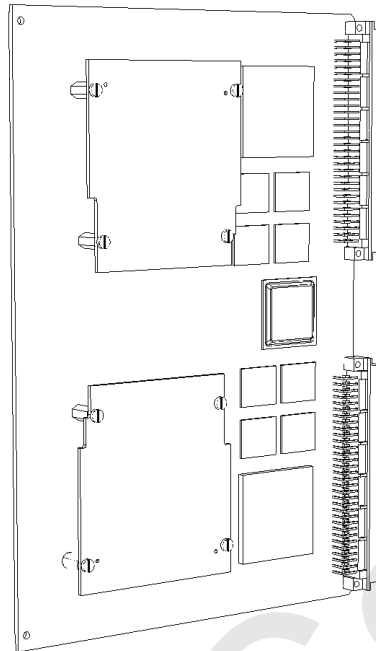
Figure 19. Example of 6U carrier with no external mezzanine I/O

Typically, carrier cards are designed for air cooled or conduction cooled environments. Figure 20 illustrates a 6U commercial grade carrier card loaded with three single commercial grade FMC mezzanine modules. Whereas Figure 21 illustrates a ruggedized carrier card loaded with three single width ruggedized conduction cooled mezzanine modules.
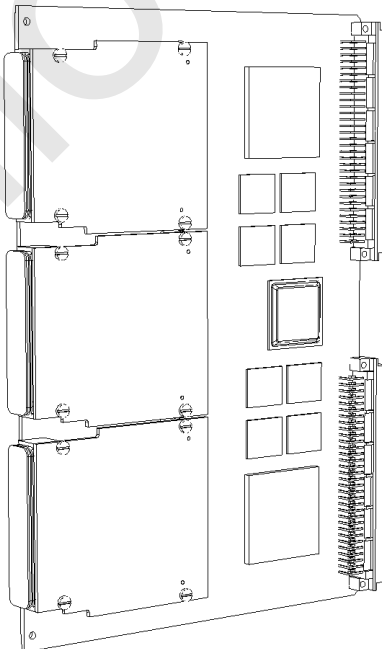
Figure 20. Typical 6U carrier card loaded with three single width commercial mezzanine modules
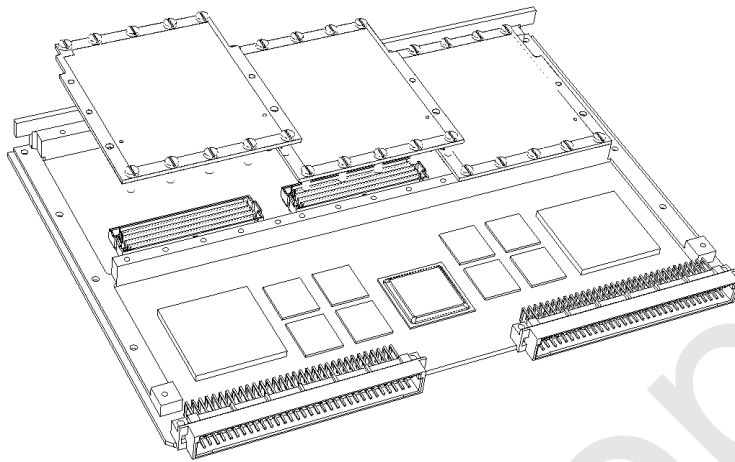
Figure 21. Typical 6U ruggedized carrier card loaded with three single width ruggedized mezzanine modules

An example of two single width FMC modules or one double width module on a cPCI carrier card is illustrated in Figure 22 with dimensions that provide for the front panel bezel to be flush with the carrier card's front panel.
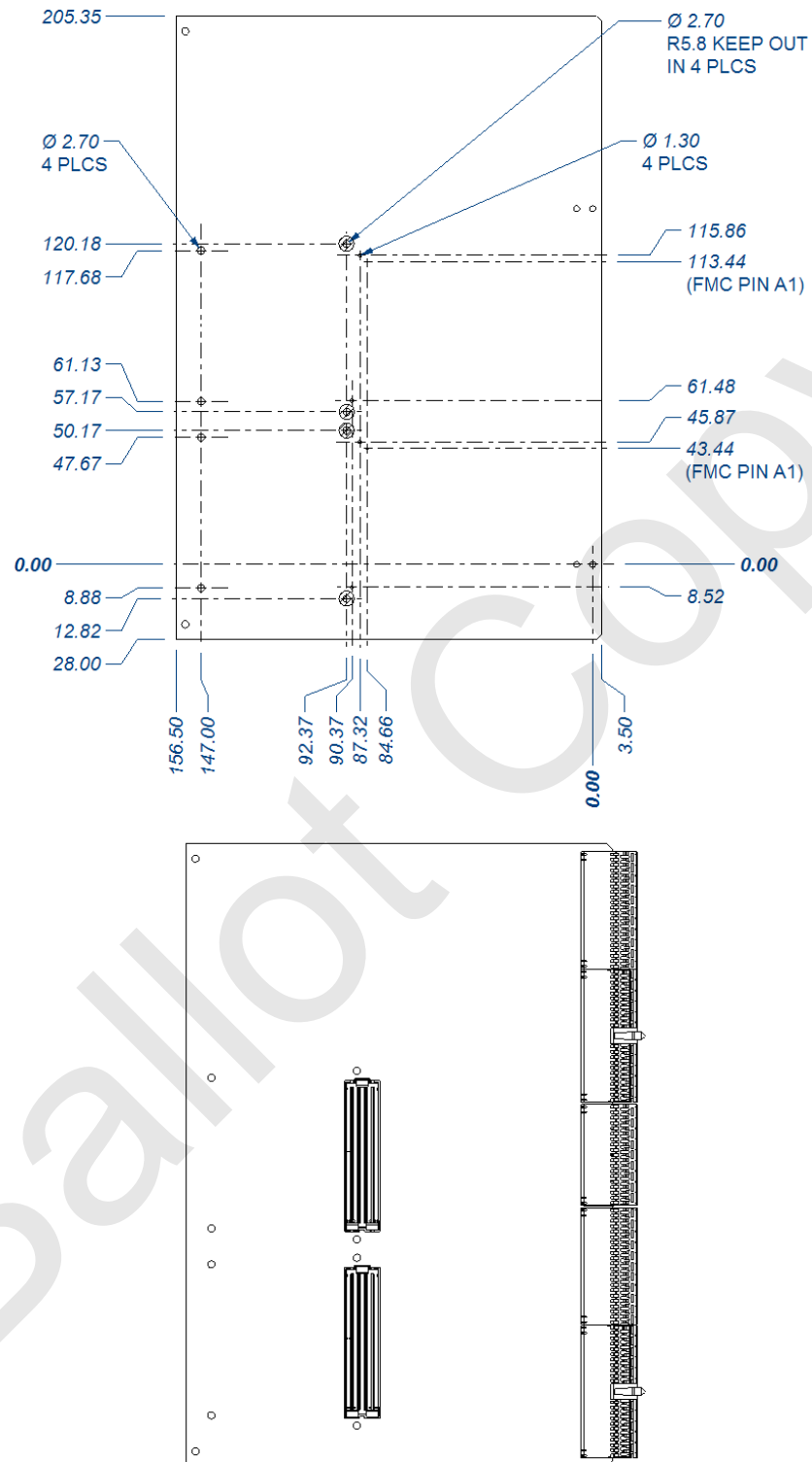
Figure 22. Dimensions of cPCI carrier card example with two FMC sites

Other examples of FMC solutions are illustrated below. Figure 23 shows a FMC mounted on 3U cPCI carrier followed by two options of an FMC mounted on an AMC carrier.
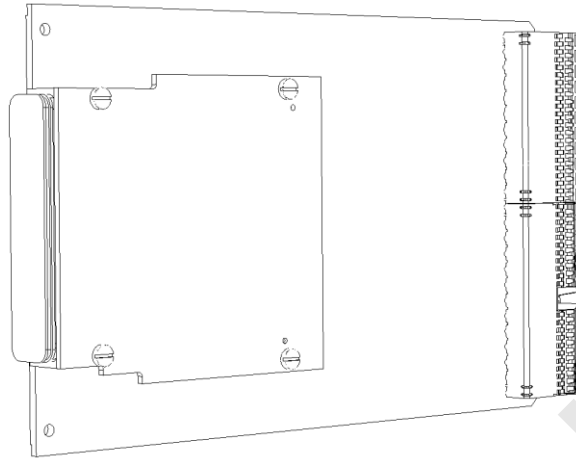
Figure 23. Example of 3U cPCI carrier with single with FMC Module

When positioning the FMC module site on an AMC carrier card there are several options available since the FMC front panel bezel is defined to be 2mm deep, while AMC carrier cards typically use a narrower front plate.

One option is to have the front of the FMC front panel bezel flush with the front panel of the AMC carrier; this would require a recess in the AMC carrier card. Figure 24 provides an example of the location of the FMC site on an AMC carrier card for this scenario.

Ø 2.70
2 PLCS

Ø 2.70
R2.9 KEEP OUT
2 PLCS

30.70
29.75
28.20
26.38

0.00

0.00

INSIDE OF FRONT PANEL

28.00
28.35
31.50
32.30

Ø 1.30
2 PLCS

178.60
167.41

112.79
110.81
107.77

0.00
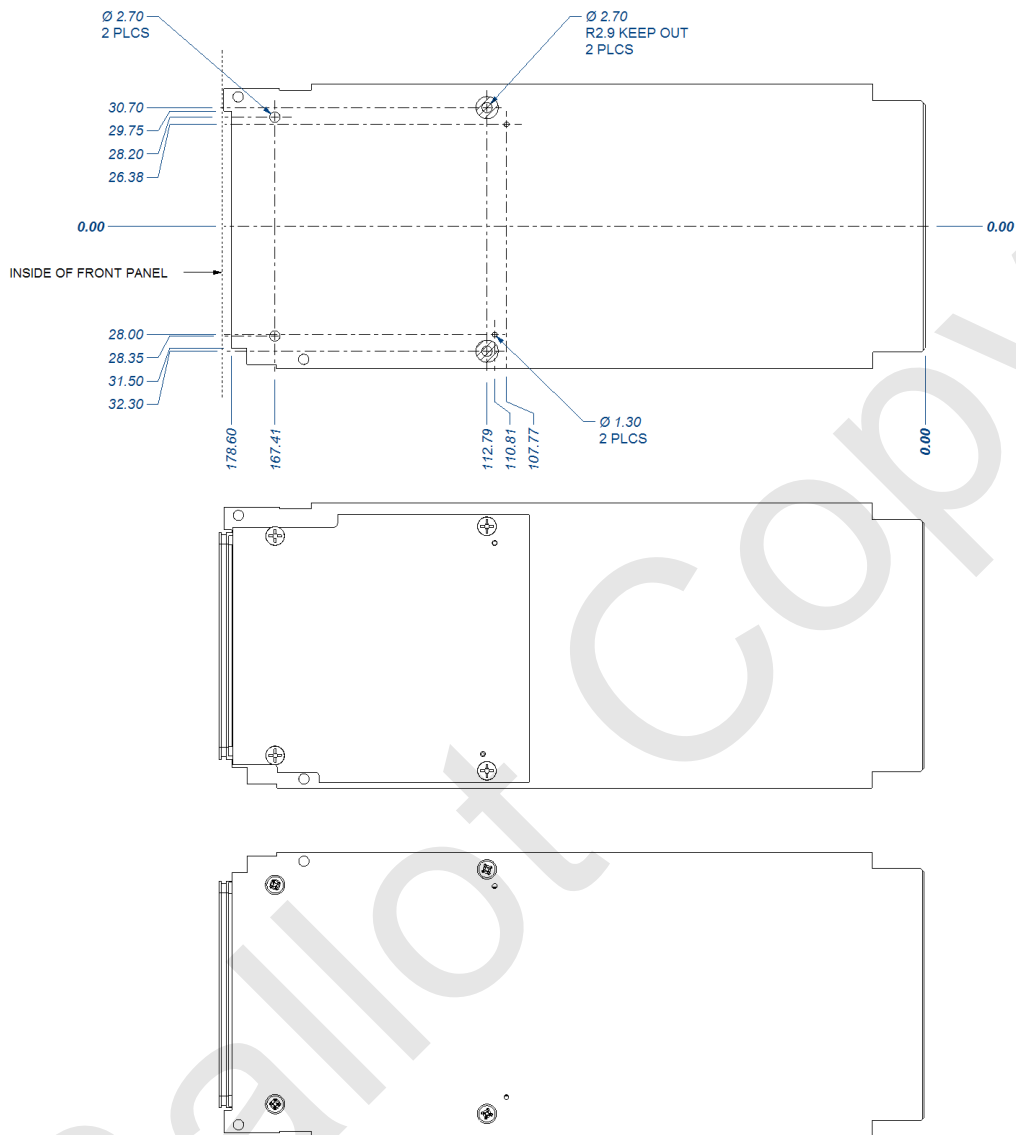
Figure 24. Dimensions of AMC with one FMC site and flush bezel

An alternative example of placing the FMC site on an AMC carrier card is shown in Figure 25. In this case, the rear of the FMC bezel and the AMC faceplate will be flush, and hence the front of the FMC front panel bezel will protrude if it is thinner than 2mm.
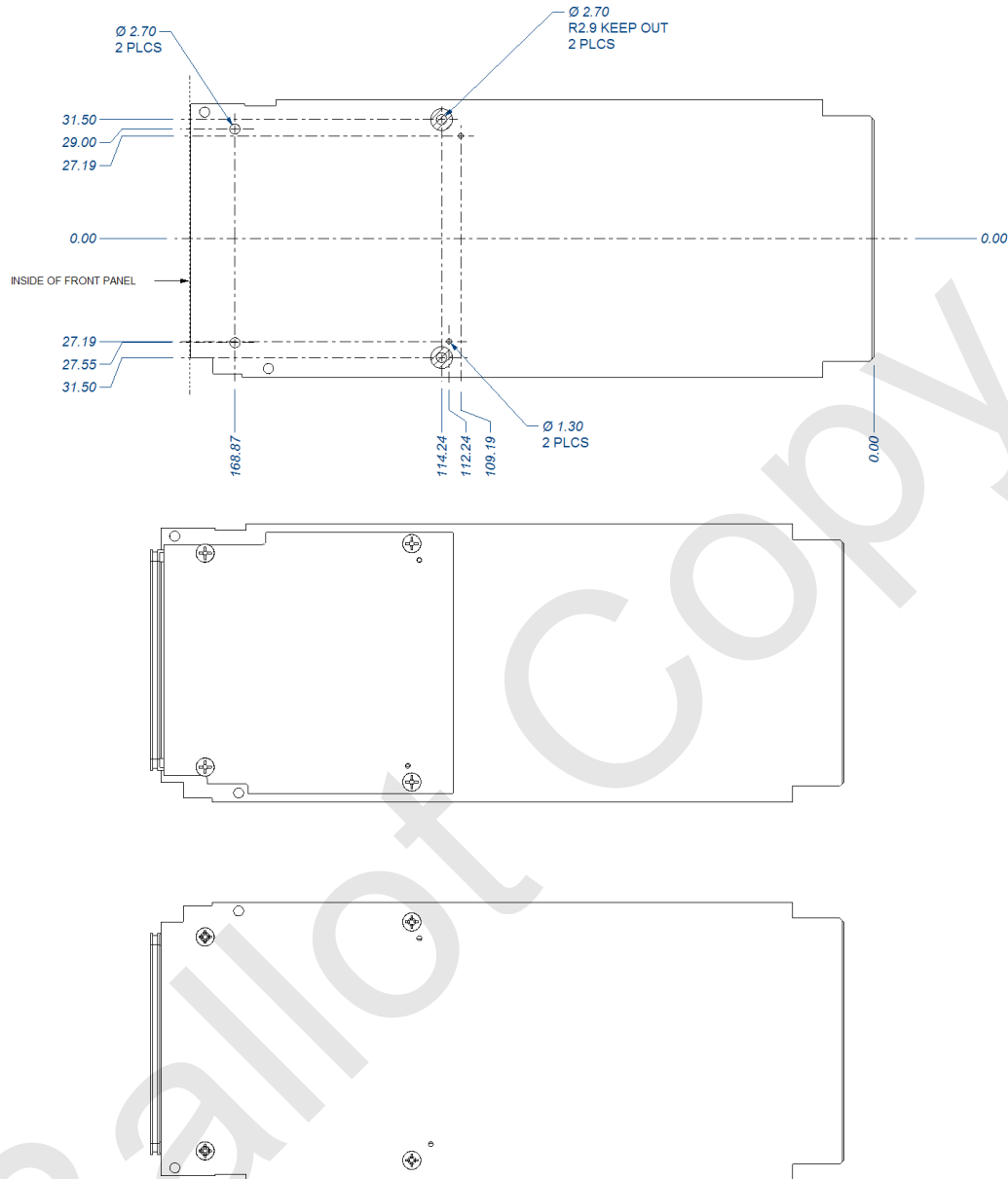
Figure 25. Dimensions of AMC with one FMC site and no recess

4.1.1. Carrier Card side 1 component height

Permission 4.2: Carrier card designers may place components under the mezzanine module slot.

Rule 4.1: The maximum component height on the carrier card under the modules component area is 4.7mm for 10mm stacking height reducing to 3.2mm for 8.5mm stacking height

Rule 4.2: No components shall be placed on side 1 of the carrier card in the I/O area of the FMC mezzanine module.

Observation 4.1: When traces or vias are used in this I/O area, they shall be insulated to prevent shorting, should mezzanine I/O components touch the host PCB in this area.

5 Connector Pin Assignments

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND
2	GND	CLK3_BIDIR_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_BIDIR_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_BIDIR_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	CLK2_BIDIR_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND

LPC Connector   LPC Connector   LPC Connector   LPC Connector

Table 2.   Signal Definitions for high-pin count connector

	K	J	H	G	F	E	D	C	B	A
1	NC	NC	VREF_A_M2C	GND	NC	NC	PG_C2M	GND	NC	NC
2	NC	NC	PRSNT_M2C_L	CLK1_M2C_P	NC	NC	GND	DP0_C2M_P	NC	NC
3	NC	NC	GND	CLK1_M2C_N	NC	NC	GND	DP0_C2M_N	NC	NC
4	NC	NC	CLK0_M2C_P	GND	NC	NC	GBTCLK0_M2C_P	GND	NC	NC
5	NC	NC	CLK0_M2C_N	GND	NC	NC	GBTCLK0_M2C_N	GND	NC	NC
6	NC	NC	GND	LA00_P_CC	NC	NC	GND	DP0_M2C_P	NC	NC
7	NC	NC	LA02_P	LA00_N_CC	NC	NC	GND	DP0_M2C_N	NC	NC
8	NC	NC	LA02_N	GND	NC	NC	LA01_P_CC	GND	NC	NC
9	NC	NC	GND	LA03_P	NC	NC	LA01_N_CC	GND	NC	NC
10	NC	NC	LA04_P	LA03_N	NC	NC	GND	LA06_P	NC	NC
11	NC	NC	LA04_N	GND	NC	NC	LA05_P	LA06_N	NC	NC
12	NC	NC	GND	LA08_P	NC	NC	LA05_N	GND	NC	NC
13	NC	NC	LA07_P	LA08_N	NC	NC	GND	GND	NC	NC
14	NC	NC	LA07_N	GND	NC	NC	LA09_P	LA10_P	NC	NC
15	NC	NC	GND	LA12_P	NC	NC	LA09_N	LA10_N	NC	NC
16	NC	NC	LA11_P	LA12_N	NC	NC	GND	GND	NC	NC
17	NC	NC	LA11_N	GND	NC	NC	LA13_P	GND	NC	NC
18	NC	NC	GND	LA16_P	NC	NC	LA13_N	LA14_P	NC	NC
19	NC	NC	LA15_P	LA16_N	NC	NC	GND	LA14_N	NC	NC
20	NC	NC	LA15_N	GND	NC	NC	LA17_P_CC	GND	NC	NC
21	NC	NC	GND	LA20_P	NC	NC	LA17_N_CC	GND	NC	NC
22	NC	NC	LA19_P	LA20_N	NC	NC	GND	LA18_P_CC	NC	NC
23	NC	NC	LA19_N	GND	NC	NC	LA23_P	LA18_N_CC	NC	NC
24	NC	NC	GND	LA22_P	NC	NC	LA23_N	GND	NC	NC
25	NC	NC	LA21_P	LA22_N	NC	NC	GND	GND	NC	NC
26	NC	NC	LA21_N	GND	NC	NC	LA26_P	LA27_P	NC	NC
27	NC	NC	GND	LA25_P	NC	NC	LA26_N	LA27_N	NC	NC
28	NC	NC	LA24_P	LA25_N	NC	NC	GND	GND	NC	NC
29	NC	NC	LA24_N	GND	NC	NC	TCK	GND	NC	NC
30	NC	NC	GND	LA29_P	NC	NC	TDI	SCL	NC	NC
31	NC	NC	LA28_P	LA29_N	NC	NC	TDO	SDA	NC	NC
32	NC	NC	LA28_N	GND	NC	NC	3P3VAUX	GND	NC	NC
33	NC	NC	GND	LA31_P	NC	NC	TMS	GND	NC	NC
34	NC	NC	LA30_P	LA31_N	NC	NC	TRST_L	GA0	NC	NC
35	NC	NC	LA30_N	GND	NC	NC	GA1	12P0V	NC	NC
36	NC	NC	GND	LA33_P	NC	NC	3P3V	GND	NC	NC
37	NC	NC	LA32_P	LA33_N	NC	NC	GND	12P0V	NC	NC
38	NC	NC	LA32_N	GND	NC	NC	3P3V	GND	NC	NC
39	NC	NC	GND	VADJ	NC	NC	GND	3P3V	NC	NC
40	NC	NC	VADJ	GND	NC	NC	3P3V	GND	NC	NC

LPC Connector   LPC Connector   LPC Connector   LPC Connector

Table 3.   Signal Definitions for low-pin count connector

Rule 5.1: Signal assignment for high-pin count connector shall be defined as shown in Table 2.

Rule 5.2: Signal assignment for low-pin count connector shall be defined as shown in Table 3.

Observation 5.1: Rows A through to Row K are associated with the high-pin count connectors.

Observation 5.2: Rows C, D, G, and H are the only rows associated with the low-pin count connectors.

Observation 5.3: Signal names with 'C2M' indicate that the signal is driven by the carrier card and received by the IO mezzanine module

Observation 5.4: Signal names with 'M2C' indicate that the signal is driven by the IO mezzanine module and received by the carrier card

Observation 5.5: Signal names with 'BIDIR' indicate that the signal can be driven by the IO mezzanine module or by the carrier card

Observation 5.6: The postfix '_P' on a differential signal pairs, indicates the positive component of a differential signal

Observation 5.7: The postfix '_N' on a differential signal pairs, indicates the negative component of a differential signal

Observation 5.8: The postfix '_L' on a single ended signal, 'PRSNT_M2C_L' and 'TRST_L' indicate that these are active low signals.

Recommendation 5.1: Signals with a '_CC' postfix should be used as the preferred signals for clocks in source synchronous applications and should be connected to pins on the FPGA, which are identified for this purpose.

LA[00..33]_P, LA[00..33]_N – User defined signals on Bank A located on the LPC and HPC.

HA[00..23]_P, HA[00..23]_N - User defined signals on Bank A located on the HPC.

HB[00..21]_P, HB[00..21]_N - User defined signals on Bank B located on the HPC.

CLK[0..1]_M2C_P, CLK[0..1]_M2C_N – Differential pairs that are assigned for clock signals, which are driven from the IO Mezzanine Module to the carrier card.

CLK[2..3]_BIDIR_P, CLK[2..3]_BIDIR_N – Differential pairs that are assigned for clock signals, which are driven either by the IO Mezzanine Module or the carrier card.

CLK_DIR – Used to determine whether the mezzanine module or the carrier card is the driver for CLK[2..3].

GBTCLK0_M2C_P, GBTCLK0_M2C_N, GBTCLK1_M2C_P, GBTCLK1_M2C_N – A differential pair shall be used as a reference clock for the DP data signals.

DP[0..9]_M2C_P, DP[0..9]_M2C_N, DP[0..9]_C2M_P, DP[0..9]_C2M_N - These signals form 10 multi-gigabit transceiver data pairs.

GA[0..1] - These signals provide geographical addressed of the module and are used for I2C channel select.

VREF_A_M2C – This is the reference voltage associated with the signaling standard used by the bank A data pins, LAxx and HAxx. If the signaling standard on Bank A does not require a reference voltage then this pin can be left unconnected

VREF_B_M2C – This is the reference voltage associated with the signaling standard used by the bank B data pins, HBxx. If the signaling standard on Bank B does not require a reference voltage then this pin can be left unconnected

VIO_B_M2C – This voltage is generated by the Mezzanine module and is used as the main voltage to power the IO banks on the FPGA that interface to the Bank B IO pins of the connector

3P3VAUX - A 3.3V auxiliary power supply.

VADJ – These pins carry an adjustable voltage level power from the carrier to the IO Mezzanine module.

3P3V – These pins carry 3.3V power from the carrier to the IO Mezzanine module.

12P0V – These pins carry 12V power from the carrier to the IO Mezzanine module.

TRST_L - JTAG Reset. This signal provides asynchronous initialization of the TAP controller on the IO Mezzanine module.

TCK - JTAG Clock. This signal provides an independent clock reference for TAP controller operation.

TMS - JTAG Mode Select. This signal shall provide state control of the TAP controller on the IO Mezzanine module.

TDI - JTAG Data In. This signal provides for serial writes of test data and instructions into the IO Mezzanine module.

TDO - JTAG Data Out. This signal provides for serial writes of test data and instructions out of the IO Mezzanine module.

PRSNT_M2C_L - Module present signal. This signal allows the carrier to determine whether an IO Mezzanine module is present.

PG_C2M – Power Good Carrier Card. This signal asserts high by the carrier card when power supplies, VADJ, 12P0V, 3P3V, are within tolerance.

PG_M2C – Power Good Mezzanine. This signal asserts high by the mezzanine module when power supplies, VIO_B_M2C, VREF_A_M2C, VREF_B_M2C, are within tolerance.

SCL – System Management I2C serial clock. This signal provides a clock reference to the IO Mezzanine module from the carrier card for a two-wire serial management bus.

SDA - System Management I2C serial data. This signal provides a data line for a two-wire serial management bus.

RES0, RES1 – These are reserved pins and are left unconnected by the IO Mezzanine module and the carrier card.

GND – This is signal ground

5.1. User Defined Pins

This specification defines the number of pins available for user defined signaling interfacing between the carrier card and the IO mezzanine module. By using the programmable flexibility of FPGA I/O, it is expected that the user defined pins can support both differential and single ended signaling. This enables the reuse of pins for different I/O standards and aids in minimizing the size of the physical connector required. The intent of this specification is to define the number of user defined pins supported by both the high-pin and low pin-count connectors.

The user defined pins are

LA[00..33]_P, LA[00..33]_N - These signals are arranged as differential pairs with signals having the '_P' postfix representing the positive component and signals with '_N' postfix representing the negative component.

HA[00..23]_P, HA[00..23]_N - These signals are arranged as differential pairs with signals having the '_P' postfix representing the positive component and signals with '_N' postfix representing the negative component.

HB[00..21]_P, HB[00..21]_N - These signals are arranged as differential pairs with signals having the '_P' postfix representing the positive component and signals with '_N' postfix representing the negative component.

Rule 5.3: Pins with a LA or HA prefix shall use the signaling standard associated with 'Bank A' and can use the reference voltage on pin 'VREF_A_M2C'.

Rule 5.4: Pins with a HB prefix shall use the signaling standard associated with 'Bank B' and can use the reference voltage on pin 'VREF_B_M2C'.

Rule 5.5: Pins with a L prefix shall have connector contacts populated in the low-pin and high-pin count connectors.

Rule 5.6: Pins with a H prefix shall have connector contacts populated only in the high-pin count connector.

Rule 5.7: The high-pin count connector shall support 160 single-ended user defined signals; or 80 differential user defined signals.

Rule 5.8: The low-pin count connector shall support 68 single-ended user defined signals; or 34 differential user defined signals.

Rule 5.9: The FMC User Defined signals in Bank A shall tolerate signal levels from -300mV to VADJ + 300mV.

Rule 5.10: Neither the carrier nor the mezzanine module shall generate signals outside the range of -300mV to VADJ + 300mV signal levels on the user defined signals in Bank A.

Rule 5.11: The FMC User Defined signals in Bank B shall tolerate signal levels from -300mV to VIO_B_M2C + 300mV.

Rule 5.12: Neither the carrier nor the mezzanine module shall generate signals outside the range of -300mV to VIO_B_M2C + 300mV signal levels on the user defined signals in Bank B.

Rule 5.13: A minimum of no user defined signals shall be supported by this standard.

Rule 5.14: A maximum of 160 user defined signals shall be supported this standard.

Permission 5.1: Any number of user defined pins may be connected on the FMC module or FMC carrier card.

Rule 5.15: The user defined signals on Bank A shall be assigned starting with the lowest ordinal in the LA group and used in ascending order. This will be followed by signals with the lowest ordinal in the HA group and used in ascending order.

Rule 5.16: The user defined signals on Bank B shall be assigned starting with the lowest ordinal in the HB group and used in ascending order.

Rule 5.17: If an odd number of signals are assigned in Bank A or Bank B then the '_P' signal shall be populated in preference to the '_N' signal.

Permission 5.2: Bank A and Bank B may be populated independently.

Permission 5.3: To maximize signal integrity, the LA signals should be fully populated and then HA and HB should be populated in the same ratio of their maximum.

Recommendation 5.3: When signals are routed differentially each pair should provide a differential impedance of 100Ω +/- 10%

Recommendation 5.4: When signals are routed single ended each signal should provide an impedance of 50Ω +/- 10%

Observation 5.9: To maximize compatibility between mezzanine modules and carrier cards, the LVDS and LVTTL signaling standards should be the preferred choice.

Observation 5.10: To maximize the performance of data buses located on the user defined pins, the skew between user defined pins should be keep to a minimum. The skew should be less that 10% of the targeted unit interval, UI for the data rates on the pins. Table 4 provides examples of times for targeted data rates.

Targeted Data Rate	10% UI (in pico seconds)
100 Mbps	1000
200 Mbps	500
500 Mbps	200
1.0 Gbps	100
1.5 Gbps	66
2.0 Gbps	50

Table 4.   Examples of UI times for targeted data rates

Unused user defined pins may be connected to ground to improved signal integrity.

> **Permission 5.4:** Application specific signals may be connected to higher ordinal pins on any of the LA, HA or HB banks that are not included as general user defined signals, provided they meet the voltage requirements for the associated bank. The number of available user defined signals shall not include the application specific signals in their count.

5.2. Differential Reference Clocks

There are four reference clocks, which have a bus between the carrier card and the IO mezzanine module. The clocks can have two configuration;

1. When 'CLK_DIR' is connected to 'GND' or unconnected on the mezzanine module, then **CLK[0..1]_M2C_P, CLK[0..1]_M2C_N, CLK[2..3]_BIDIR_P, CLK[2..3]_BIDIR_N** are four differential pairs that are assigned for clock signals, which are driven from the IO Mezzanine Module to the carrier card.
2. When 'CLK_DIR' is connected to '3P3V' via a 10KΩ pull up resistor on the mezzanine module, then **CLK[0..1]_M2C_P, CLK[0..1]_M2C_N** are two differential pairs that are assigned for clock signals, which are driven from the IO Mezzanine Module to the carrier card, and, **CLK[2..3]_BIDIR_P, CLK[2..3]_BIDIR_N** two differential pairs that are assigned for clock signals, which are driven from the carrier card to the IO Mezzanine Module.

> **Observation 5.11:** CLK0_M2C, CLK1_M2C, are defined in the high-pin count and low-pin count connectors

> **Observation 5.12:** CLK2_BIDIR, CLK3_BIDIR, are defined in the high-pin count connector

> **Rule 5.18:** Clocks, CLK0_M2C, CLK1_M2C shall be driven by the IO Mezzanine module and received by the carrier card.

Rule 5.19: Clocks, CLK2_BIDIR, CLK3_BIDIR shall be driven by the IO Mezzanine module and received by the carrier card when CLK_DIR is connected to GND or unconnected by the mezzanine module.

Rule 5.20: Clocks, CLK2_BIDIR, CLK3_BIDIR shall be driven by the carrier card and received by the IO Mezzanine module when CLK_DIR is connected via a 10KΩ pull up resistor to 3P3V by the mezzanine module.

Rule 5.21: CLK[0..3] shall be assigned starting with the lowest ordinal and used in ascending order when CLK_DIR is connected to GND or unconnected..

Rule 5.22: CLK[0..1]_M2C shall be assigned to clocks driving from the mezzanine module to the carrier card starting with the lowest ordinal and used in ascending order when CLK_DIR is connected via a 10KΩ pull up resistor to 3P3V by the mezzanine module.

Rule 5.23: CLK[2..3]_BIDIR shall be assigned to clocks driving from the carrier card to the mezzanine module starting with the lowest ordinal and used in ascending order when CLK_DIR is connected via a 10KΩ pull up resistor to 3P3V by the mezzanine module.

Rule 5.24: CLK[0..3] shall use the LVDS signaling standard.

Rule 5.25: All CLK signals shall be connected to differential logical '0' by the driving source when not connected to a signal. The '_P' signal shall connect to '0' and the '_N' signal shall connect to '1'.

Rule 5.26: Clock traces shall provide a differential impedance of 100Ω +/- 10%

Rule 5.27: The differential length mismatch on each differential clock pair shall be a maximum 11ps.

Rule 5.28: The maximum period jitter on CLK[0..3] shall be 1ns.

Rule 5.29: The maximum cycle to cycle jitter on CLK[0..3] shall be +/- 150ps

Recommendation 5.5: CLK[0..1]_M2C (and CLK[2..3]_BIDIR when carrier cards support the configuration of CLK_DIR connected to GND or unconnected) signals should be connected to optimal pins on the FPGA device residing on the carrier card, such as dedicated clock pins.

Recommendation 5.6: If a mezzanine module has a need for a particular clock performance, then it should be generated locally on the mezzanine module.

Rule 5.30: CLK_DIR shall be implemented as a LVTTL signal

Rule 5.31: The Carrier card shall provide a 100KΩ pull-down resister on CLK_DIV signals to GND.

Rule 5.32: The Mezzanine module shall connected CLK_DIR to GND or leave unconnected when it is driving a clock on either CLK2_BIDIR or CLK3_BIDIR to the carrier card.

Rule 5.33: The Mezzanine module shall connected CLK_DIR via a 10KΩ pull up resistor to 3P3V when it requires the carrier card to drive a clock on either CLK2_BIDIR or CLK3_BIDIR to the mezzanine module
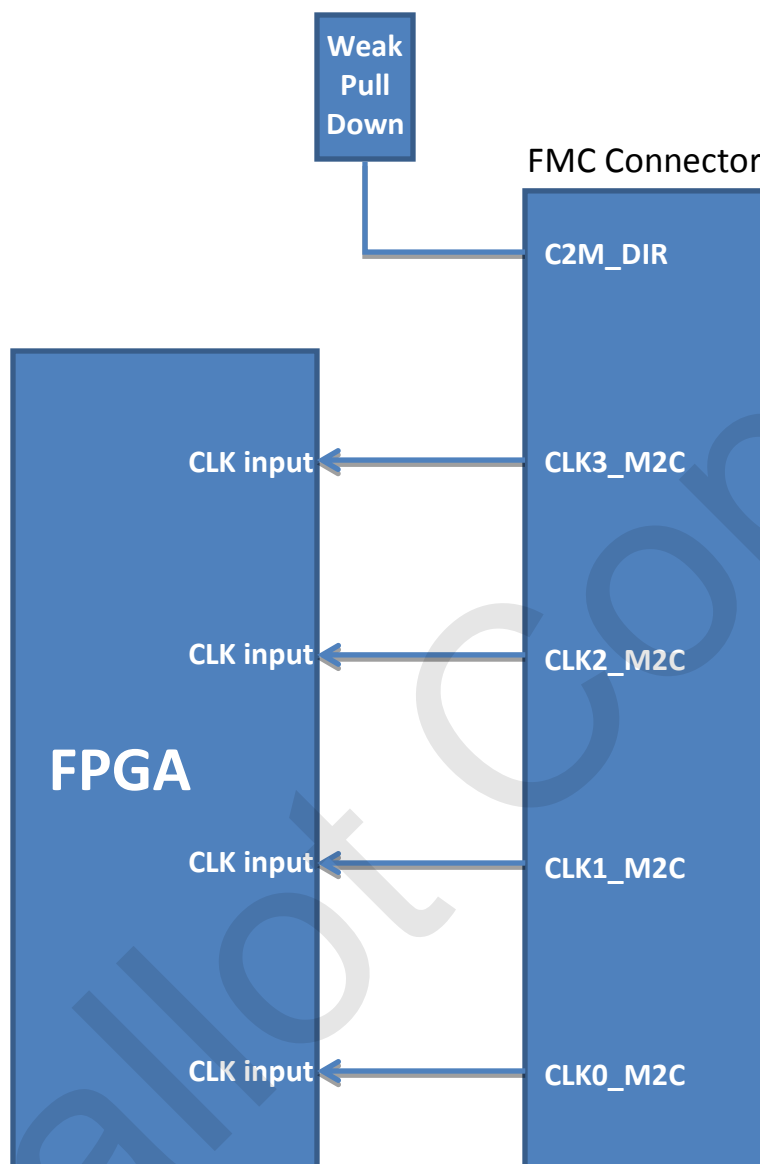
Figure 26. Illustration of carrier card only supporting 4 receiving clocks
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VITA 57.1-2009/D0.19   10/01/09
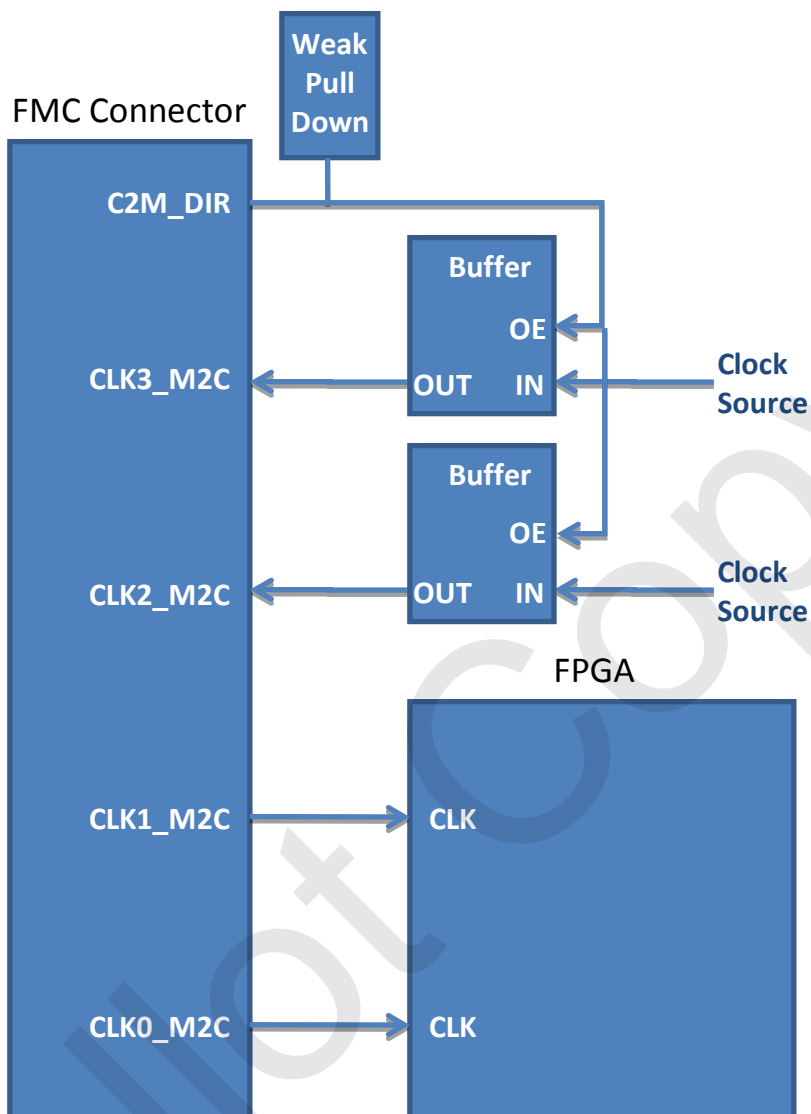
Figure 27. Illustration of carrier card supporting 2 receiving and 2 driving clocks
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5.3. Gigabit Interface

This specification defines the use of a multi-gigabit interface between the carrier card and the IO mezzanine module. The intent of this specification is to support multi-gigabit interfaces up to 10Gb/s. The gigabit interface signals are identified by the signals with 'DP' prefix and the associated reference clocks for use with the DP signals have a prefix of 'GBTCLK'.

5.3.1. Gigabit Data Signals

DP[0..9]_M2C_P, DP[0..9]_M2C_N - These signals are arranged as differential pairs with signals having the '_P' postfix representing the positive component and signals with '_N' postfix representing the negative component.

DP[0..9]_C2M_P, DP[0..9]_C2M_N - These signals are arranged as differential pairs with signals having the '_P' postfix representing the positive component and signals with '_N' postfix representing the negative component.

> **Rule 5.34:** The DP[0..9]_M2C are driven from the IO mezzanine module to the carrier card.

> **Rule 5.35:** DP[0..9]_M2C shall be connected to the adaptively equalized IO transceiver receiver inputs on the FPGA of the carrier card

> **Rule 5.36:** The DP[0..9]_C2M are driven from the carrier card to the IO mezzanine module.

> **Rule 5.37:** DP[0..9]_C2M shall be connected to the adaptively equalized IO transceiver transmitter outputs on the FPGA of the carrier card

> **Rule 5.38:** The FPGA I/O pins connected to DP[0..9]_C2M and DP[0..9]_M2C shall be able to accommodate situations when they are left unconnected on the mezzanine module.

> **Observation 5.13:** To improve signal integrity, unused DP[0..9]_M2C differential pairs may be connected to differential logic '0', where the '_P' signal shall connect to '0' and the '_N' signal shall connect to '1'.

> **Rule 5.39:** The multi-gigabit transceiver data signals, DP, are arranged as differential pairs with signals having the '_P' postfix representing the positive component and signals with '_N' postfix representing the negative component.

> **Rule 5.40:** All DP[0..9]_C2M signals shall be connected directly to the pins of the FPGA device on the carrier card. No other components shall be connected to these signals on the carrier card.

> **Rule 5.41:** All DP[0..9]_M2C signals shall be connected directly to the pins of the FPGA device on the carrier card. No other components shall be connected to these signals on the carrier card.

Rule 5.42: If AC coupling is required for DP[0..9]_M2C, DP[0..9]C2M signals, this shall be provided on the mezzanine module.

Rule 5.43: The four-gigabit data pins with the same ordinal value shall makeup a complementary transceiver pair.

Rule 5.44: Only gigabit data pins with an ordinal value of '0' are available on the low-pin count connector.

Rule 5.45: A single gigabit interface consists of a transmit differential pair, and a receive differential pair, with the direction referenced to the FPGA on the carrier card.

Observation 5.14: The DP[0..9]_C2M differential pairs connect to the transmitters of the FPGA on the carrier card.

Observation 5.15: The DP[0..9]_M2C differential pairs connect to the receivers of the FPGA on the carrier card.

Rule 5.46: A minimum of no separate gigabit interfaces shall be supported by this standard.

Rule 5.47: A maximum of ten separate gigabit interfaces shall be supported by this standard.

Rule 5.48: Carrier cards shall support the gigabit interfaces in the following groups – 0x, 1x, 2x, 4x, 8x, 10x.

Rule 5.49: The gigabit interfaces shall be assigned starting with the pair with the lowest ordinal and used in ascending order

Rule 5.50: The differential peak-to-peak voltage on the DP[0..9] signals shall not exceed 1V.

Rule 5.51: Gigabit data pairs traces shall provide a differential impedance of 100Ω +/- 10%

Rule 5.52: The differential length mismatch on each differential data pair shall 1ps.

Observation 5.16: To operate at speed greater than 3.125 Gb/s, stub elimination is necessary.

Observation 5.17: The size of the AC coupling for the DP[0..9] signals are not specified as it will be application specific, however capacitances ranging from 75nF to 200nF are typically recommended.

Permission 5.5: Each DP pair may have a different value for their AC coupling.

5.3.2. Gigabit reference clocks

To support the multi-gigabit IO interfaces a reference clock is typically required that is used to determine the data transfer rates.

GBTCLK0_M2C_P, GBTCLK0_M2C_N – A differential pair that is assigned for a clock signal, which is driven from the IO Mezzanine Module to the carrier card. This signal will be used as a reference clock for the DP data signals.

GBTCLK1_M2C_P, GBTCLK1_M2C_N – A differential pair that is assigned for a clock signal, which is driven from the IO Mezzanine Module to the carrier card. This signal will be used as a reference clock for the DP data signals.

Rule 5.53: The IO mezzanine module shall provide the reference clocks, GBTCLK, for the gigabit interface. These clocks shall be bused as a differential pair.

Rule 5.54: The reference clocks, GBTCLK, shall use the LVDS signaling standard.

Rule 5.55: The reference clocks, GBTCLK, shall be tied to logical '0' when not in use. The '_P' signal shall be tied to '0' and the '_N' signal shall be tied to '1'.

Rule 5.56: If only one GBTCLK is connected then this shall be GBTCLK0_M2C.

Observation 5.18: The low-pin count connector only has GBTCLK0_M2C available.

Rule 5.57: Clock traces shall provide a differential impedance of 100Ω +/- 10%

Rule 5.58: The differential length mismatch on each differential clock pair shall 11ps.

Recommendation 5.7: The maximum peak to peak jitter on the clocks should be +/-40ps.

Suggestion 5.1: GBTCLK signals may be connected to dedicated clock pins on the FPGA device on the carried card that are associated with the multi-gigabit data pairs

5.4. JTAG Signals

This standard allows the use of signals required to implement Test Access Port and Boundary Scan Architecture, also known as JTAG, specified in IEEE1149.1. The complete specification of these signals is beyond the scope of this document; for additional information on JTAG signaling and usage, please see appropriate specification.

The definitions of the JTAG signals are highlighted in Table 5.

Signal Name	Description
TDI	Test Data Input to IO mezzanine module
TDO	Test Data Output from IO mezzanine module
TMS	Test Mode Select input to IO mezzanine module
TCK	Test Clock input to IO mezzanine module
TRST_L	Test Reset input to IO mezzanine module

Table 5.   JTAG Signal definition

Rule 5.59: The carrier card shall ensure that an independently buffered TCK shall be input to each IO mezzanine module.

Rule 5.60: The mezzanine module card shall only have one load on the TMS signal.

Rule 5.61: The carrier card shall connect TDI directly to TDO, if the FMC module is not plugged into carrier card

Rule 5.62: The FMC module shall connect TDI to TDO, if the module does not use the JTAG interface.

Rule 5.63: For double width modules the carrier card shall connect the TDI on P2 to TDO on P2 if no connector is present

Rule 5.64: For double width modules the FMC module shall connect TDI of P2 to TDO of P2, if the module does not use the JTAG interface.

Rule 5.65: For double width modules the FMC module shall treat the JTAG interfaces on each of P1 and P2 as independent JTAG chain. Hence the JTAG path entry of TDI on P1 shall route back through TDO of P1 and the JTAG path entry of TDI on P2 shall route back through TDO of P2.

Suggestion 5.2: PRSNT_M2C_L should be used to detect the presence of the module and used to control the switching of the TDI signal that would normally connect to the IO Mezzanine module directly to the TDO signal, thus bypassing the module and keeping the JTAG chain intact

Observation 5.19: JTAG support is optional on compliant IO mezzanine modules.

Rule 5.66: The FMC JTAG signals require LVTTL (3.3V) levels on the JTAG signals.

Rule 5.67.: The carrier shall not drive signals onto the JTAG signals to the IO Mezzanine module that exceed LVTTL levels.

Rule 5.68: The IO Mezzanine Module shall not drive signals to the carrier card that exceed LVTTL levels.

5.5. I2C Bus Signals

This standard allows the use of signals required to implement the I2C bus specification. The complete specification of these signals is beyond the scope of this document; for additional information on I2C signaling and usage, please see appropriate specification. Two pins SCL and SDA are allocated for I2C.

The definition of the I2C Bus signals are highlighted in Table 6

Signal Name	Description
SDA	Bi-directional serial data
SCL	Clock

Table 6.   I2C Bus signals

Rule 5.69: The IO mezzanine module shall provide an onboard EEPROM, which shall interface with the I2C bus signals.

Observation 5.20: The EEPROM shall be used to store information pertaining to the characteristics of the IO mezzanine module.

Rule 5.70: The EEPROM will be powered by the signal 3P3VAUX.

Rule 5.71: On double width mezzanine modules, the non-volatile storage device will be connected to the I2C bus on the P1 connector.

Rule 5.72: On double width mezzanine modules, the non-volatile storage device on P1 connector's I2C bus shall contain data pertaining to setting for P2 connector if populated.

Rule 5.73: On double width mezzanine modules, devices shall not be placed on the I2C bus located on P2.

5.5.1. IPMI Support

The FMC mezzanine module shall provide hardware definition information that may be read by an external controller using IPMI commands and I2C serial bus transactions. The mezzanine module shall support the I2C link on pins SDA and SCL and optionally support the base IPMI commands defined in the PICMG 2.9 specification.

Rule 5.74: Data fields provided by the IPMI resource on the mezzanine module shall include the minimum records defined in the Platform Management FRU Information Storage Definition V1.0.

Rule 5.75: The EEPROM shall include the BOARD_INFO area for identification of the mezzanine module.

Rule 5.76: The mezzanine module description data shall be stored in a non-volatile memory resource on the mezzanine module.

Rule 5.77: For FMC-specific MultiRecords, the MultiRecord's header (see ISD section 16.1) shall specify OEM record type 0xFA (see ISD section 16.2.1). The Manufacturer ID field of the Multirecord's data portion (see ISD section 18.7) shall specify VITA's Organizationally Unique Identifier (OUI), 0x0012A2

Field	Byte Offset	Bit Location	Length	Description
Subtype	0	7:4	4 bits	0 for main definition type
Version	0	3:0	4 bits	0 for current version
Module Size	1	7:6	2 bits	0b00 = single width, 0b01 = double width
P1 Connector size	1	5:4	2 bits	0b00 = LPC, 0b01 = HPC
P2 Connector size	1	3:2	2 bits	0b00 = LPC, 0b01 = HPC, 0b11 = not fitted
Clock Direction	1	1	1 bit	Defines direction of CLKx_BIDIR 0b0 = from Mezzanine to Carrier 0b1 = from Carrier to Mezzanine
reserved	1	0	1 bit	= 0b0
P1 Bank A Number Signals	2	7:0	8 bits	= number needed
P1 Bank B Number Signals	3	7:0	8 bits	= number needed
P2 Bank A Number Signals	4	7:0	8 bits	= number needed
P2 Bank B Number Signals	5	7:0	8 bits	= number needed
P1 GBT Number Transceivers	6	7:4	4 bits	= number needed
P2 GBT Number Transceivers	6	3:0	4 bits	= number needed
Max Clock for TCK	7	7:0	8 bits	= clock in MHz

Table 7.   Subtype 0: Base Definition (fixed length and mandatory)

Rule 5.78: A multi-record 'DC Output' shall be included for the VIO_B_M2C, VREF_A_M2C, VREF_B_M2C power supplies

Rule 5.79: A multi-record 'DC Load' shall be included for the VADJ, 3P3V, 12P0V, VIO_B_M2C power supplies

Rule 5.80: When the VADJ can support a range of voltage levels, then the VADJ 'DC Load' multi-record shall use the minimum and maximum fields to indicate the voltage ranges supported and the 'Voltage Required' field shall indicate the preferred voltage.

DC Output Record	Connector	Record Type	Output Number	Description
VADJ	P1	LOAD	0	Mandatory
3P3V	P1	LOAD	1	Mandatory
12P0V	P1	LOAD	2	Mandatory
VIO_B_M2C	P1	OUTPUT	3	Mandatory
VREF_A_M2C	P1	OUTPUT	4	Mandatory
VREF_B_M2C	P1	OUTPUT	5	Mandatory
VADJ	P2	LOAD	6	Mandatory for double width with P2 fitted, n/a for Single Width
3P3V	P2	LOAD	7	Mandatory for double width with P2 fitted, n/a for Single Width
12P0V	P2	LOAD	8	Mandatory for double width with P2 fitted, n/a for Single Width
VIO_B_M2C	P2	OUTPUT	9	Mandatory for double width with P2 fitted, n/a for Single Width
VREF_A_M2C	P2	OUTPUT	10	Mandatory for double width with P2 fitted, n/a for Single Width
VREF_B_M2C	P2	OUTPUT	11	Mandatory for double width with P2 fitted, n/a for Single Width

Table 8.   DC Load and DC Output Multi-record Definitions

Field	Byte Offset	Bit Location	Length	Description
Subtype	0	7:4	4 bits	1 for I2C device definition subtype
Version	0	3:0	4 bits	0 for current version
Device String	1..N/8		N bits	Device address / name strings, see below

Table 9.   Subtype 1: I2C Device Definition (variable length and optional)

The device string portion of this MultiRecord subtype consists of 6-bit ASCII text as defined in the ISD. The string is divided into one or more I2C device records. Each device record consists of one or more address characters followed by one or more bytes of device name.

Address characters use the characters 0x01 through 0x0F, indicating I2C addresses with the most significant bits corresponding to 0b0000 through 0b1111, skipping the Serial EEPROM address of 0b1010. Address characters may not be used within the device name. If the same device is used multiple times, it may be indicated by multiple address characters prior to the device name.

The device name consists of the characters '0' through '9' and 'A' through 'Z'. The interpretation of the device name is outside the scope of this standard. It is recommended that the most basic form of the device part number be used, without information such as package type, temperature range, or speed grade.

For example, if the FMC module has a single I2C controller at address 0b0000nnn, it would have the subtype 1 string "!CTLR". If an FMC module had two temperature sensors at addresses 0b0011nnn and 0b0100nnn along with the above controller, it could have the subtype 1 string "!CTLR$%LM75".

5.6. Geographic Addresses

These signals enable the FMC carrier card to address specific FMC slots that share an IPMI I2C bus.

Rule 5.81: A mezzanine module shall use GA0 and GA1 to determine the address of the non-volatile storage device EEPROM devices and optional devices. The address decoding shall follow the addresses outlined in Table 10.

GA[0..1]	I2C Address for serial EEPROM	I2C Addresses for Optional Devices
00	0b101 0000	0bxxx xx00
01	0b101 0001	0bxxx xx01
10	0b101 0010	0bxxx xx10
11	0b101 0011	0bxxx xx11

Table 10. I2C Address decoding

Observation 5.21: Table 10 assumes that the most significant bit is transmitted first.

Observation 5.22: GA[0] is connected to Address bit [1] and GA[1] is connected to Address bit[0].

Rule 5.82: The carrier card shall provide a unique code on GA[0..1] for all FMC slots that share an IPMI I2C bus.

Rule 5.83: The carrier card shall connect the GA[0] and GA[1] directly to either the 3V3PAUX supply or GND signal.

Rule 5.84: Optional Devices shall not use the address spaces assigned to the serial EEPROM.

Observation 5.23: The mezzanine module may want to put a current limiting resistor on GA[0] and GA[1] signals.

5.7. IO Mezzanine Module Present

This standard uses the **PRSNT_M2C_L** signal, for a carrier card to successfully detect that an IO mezzanine module is installed.

Rule 5.85: The IO mezzanine module shall connect this signal to GND.

Rule 5.86: For double width modules, if the mezzanine module populates P2 then the mezzanine module shall connect the PRSNT_M2C_L on the P2 connector to GND.

Rule 5.87: The carrier card shall analyze the PRSNT_M2C_L signal to identify whether an IO mezzanine module is installed.

5.8. Power Good Signals

The signals, **PG_M2C and PG_C2M**, indicate whether the power signals listed in Table 11 or Table 12 are all within tolerance to ensure a stable system for operation.

Rule 5.88: PG_M2C and PG_C2M shall be implemented as LVTTL signals

Rule 5.89: The Carrier card shall provide a 10KΩ pull-up resister on each of PG_M2C and PG_C2M signals to 3P3V.

Rule 5.90: A carrier card shall drive PG_C2M low when the power signals VADJ, 3P3V, 12P0V, and 3P3AUX do not meet specification. When these signals meet specification, the carrier card shall drive PG_C2M high.

Rule 5.91: A HPC mezzanine module shall drive PG_M2C low when the power signals VREF_A_M2C, VREF_B_M2C, VIO_B_M2C do not meet specification. When these signals meet specification, the mezzanine module card shall drive PG_M2C high.

Observation 5.24: Mezzanine modules and carrier cards should implement appropriate measures to handle when power supplies go out of specification during operation

Rule 5.92: Double width mezzanine modules that populate the P2 connector shall have a PG_M2C signal for the power supply signals local to the P2 connector.

Observation 5.25: The PG_C2M and PG_M2C signals on the P1 and P2 connectors operate independently and represent the status of the power signals local to the connector. Double width mezzanine modules designers need to ensure that PG_C2M and PG_M2C on P1 and PG on P2, both assert high before all supplies to the module are within tolerance.

Rule 5.93: For double width mezzanine modules, VADJ on the P1 and P2 connector shall be independent supplies

Rule 5.94: 3P3V and 12P0V shall share a common power rail on the carrier card for double width slots for P1 and P2 connectors

Permission 5.6: VIO_B_M2C on P1 and P2 connectors of double width modules may be a common supply rail.

Permission 5.7: VREF_A_M2C on P1 and P2 connectors of double width modules may be a common supply rail.

Permission 5.8: VREF_B_M2C on P1 and P2 connectors of double width modules may be a common supply rail.

Observation 5.26: When VIO_B_M2C, VREF_A_M2C and VREF_B_M2C are common supply rails they must be capable of supplying the maximum current on both the P1 and P2 connectors.

5.9. Reserved Signals

This specification identifies reserved pins of the connector with signal RES0 and RES1.

Rule 5.95: These pins are reserved for future use, and therefore, shall be left un-connected.

5.10. Power Supply Requirements

This specification provides for three main power supply voltages, VADJ, 3P3V and 12P0V, as defined in Table 11 and Table 12. It is the intent of the specification that these be maintained as separate delivery paths. The voltages shall be supplied from the carrier

card to the IO mezzanine module. It is also the intent of this specification that primary power to the module is provided by some combination of main three power supply voltages.

Voltage Supply	Allowable Voltage Range	No Pins	Max Amps	Tolerance	Max Capacitive Load
VADJ	0 – 3.3V	4	4	+/- 5%	1000 uF
VIO_B_M2C	0 – VADJ	2	1.15	+/- 5%	500 uF
VREF_A_M2C	0 – VADJ	1	1mA	+/- 2%	10 uF
VREF_B_M2C	0 – VIO_B_M2C	1	1mA	+/- 2%	10 uF
3P3VAUX	3.3V	1	20mA	+/- 5%	150 uF
3P3V	3.3V	4	3	+/- 5%	1000 uF
12P0V	12V	2	1	+/- 5%	1000 uF

Table 11. Power Supply Voltages for HPC connector

Voltage Supply	Allowable Voltage Range	No Pins	Max Amps	Tolerance
VADJ	0 – 3.3V	2	2	+/- 5%
VIO_B_M2C	NC	0	0	n/a
VREF_A_M2C	0 – VADJ	1	1mA	+/- 2%
VREF_B_M2C	NC	0	0	n/a
3P3VAUX	3.3V	1	20mA	+/- 5%
3P3V	3.3V	4	3	+/- 5%
12P0V	12V	2	1	+/- 5%

Table 12. Power Supply Voltages for LPC connector

VADJ is provided on the FMC connector to simplify the power management on the FMC module so that the limited space on the module can be fully used for the I/O functionality and to minimize any noise that would come from a power supply onboard the module. With the wide range of I/O that may exist on a FMC module, it is difficult to specify a single universal voltage that would not need conversion to suit the devices on the modules. Therefore, this flexible mechanism of obtaining a preconditioned power source from the carrier card and defined by the IPMI provides a powerful feature for simplified system design.

Rule 5.96: IO mezzanine modules shall use the appropriate combination of the main three power supply voltages, VADJ, 3P3V, 12P0V, to accommodate the design requirements.

Recommendation 5.8: For carrier cards to obtain maximum compatibility with FMC modules, carrier cards should have provision for maximum current for each supply as define in Table 11 and Table 12.

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Rule 5.97: Carrier card vendors shall include in their product information the current that can be supplied on the 12P0V, 3P3V, VADJ and 3P3VAUX supplies.

Rule 5.98: Carrier card vendors shall include in their product information the available voltages that can be supplied on the VADJ supplies.

Rule 5.99: Module vendors shall include in their product information the current that can be supplied on the VIO_B_M2C, VREF_A_M2C, VREF_B_M2C supplies.

Rule 5.100: Module vendors shall include in their product information the voltage that is required on the VADJ supply.

Rule 5.101: Module vendors shall include in their product information the voltage can be supplied on each of the VIO_B_M2C, VREF_A_M2C, VREF_B_M2C supplies.

Rule 5.102: Carrier card vendors shall include in their product information the current that will be used on the VIO_B_M2C, VREF_A_M2C, VREF_B_M2C supplies.

Rule 5.103: Module vendors shall include in their product information the current that will be used on the 12P0V, 3P3V, VADJ, and 3P3VAUX supplies.

Rule 5.104: Mezzanine modules shall not dissipate more than 10W. More than 10W may be generated onboard the mezzanine module provided the system is capable of dissipating the power generated.

Rule 5.105: Module vendors shall include in their product information the maximum heat dissipated by the module.

Permission 5.9: Carrier cards may provide less than the specified currents and support lower than 10W of thermal dissipation provided that this is clearly identified in the product information

Rule 5.106: A total of four pins shall be allocated to VADJ supply voltage on the high pin count connector

Rule 5.107: A total of two pins shall be allocated to VADJ supply voltage on the low pin count connector

Rule 5.108: A total of four pins shall be allocated to 3P3V supply voltage

Rule 5.109: A total of two pins shall be allocated to 12P0V supply voltage

Observation 5.27: The FMC high-speed connector has a pin current rating of 2.7A. However, this specification will use a derated factor of 1A.

Recommendation 5.9: IO mezzanine modules **should** include an internal power supply control system that holds the module in reset until the input voltages are stable for a suitable interval. For many system applications, this time will be 200-500 milliseconds.

5.11.   Power Sequencing

Observation 5.28: Carriers may provide power with arbitrary rise time and sequencing between different power supplies.

Rule 5.110: Carriers and mezzanines shall consider power to be stable once all power supplies are within tolerances.

Rule 5.111: The 3P3V, 12P0V, and VADJ power supplies must all be monotonic during rise time.

5.12.   3.3V Auxiliary Supply

3P3VAUX - A 3.3V auxiliary power supply is available for IO Mezzanine module use. 3P3VAUX is not intended to provide primary power to the module but rather to accommodate system management functionality which might need to operate even if the onboard power conversion circuitry fails

Rule 5.112: Carrier cards shall provide 3.3V on this pin. Carrier cards may use its 3.3V AUX or the main 3.3V of the carrier card to service this pin

Rule 5.113: The 3P3VAUX power supply must be monotonic during rise time.

Observation 5.29: 3P3VAUX may be present to the mezzanine module when no other voltages are present.

Observation 5.30: 3P3VAUX and 3P3V should not share common paths on the mezzanine module to avoid a false current path when mezzanine is switched off.

5.13. IO Reference Voltage

This specification provides for a reference voltage to source from the IO mezzanine module to the carrier card. It is the intention of this specification to facilitate IO standards used by the module, which require a reference voltage. The complete specification of these IO standards is beyond the scope of this document; for additional information please see appropriate specification

VREF_A_M2C – This is the reference voltage associated with the signaling standard used by the bank A data pins.

VREF_B_M2C – This is the reference voltage associated with the signaling standard used by the bank B data pins.

> **Rule 5.114:** LAxx and HAxx, user defined pins and also the CLK[0..2]_M2C signals shall use VREF_A_M2C as the reference voltage if required for their signaling standard

> **Permission 5.10:** If the signaling standard on Bank A does not require a reference voltage then the mezzanine module may leave VREF_A_M2C unconnected

> **Rule 5.115:** HBxx, user defined pins and also the CLK3_M2C signals shall use VREF_B_M2C as the reference voltage if required for their signaling standard

> **Permission 5.11:** If the signaling standard on Bank B does not require a reference voltage then the mezzanine module may leave VREF_B_M2C unconnected.

> **Rule 5.116:** The carrier card must connect the VREF pins to the appropriate pins of the FPGA device, which shall be interfacing with the IO mezzanine module.

> **Permission 5.12:** If the carrier card does not support any signaling standards requiring a VREF voltage, then the corresponding VREF pin for either Bank A or Bank B or both Banks may be left unconnected on the carrier card.

5.14. IO Bank Supply Voltage

This specification provides for a supply voltage that is generated by the mezzanine module and is passed to the carrier card by the VIO_B_M2C pins to be used to drive the main power supply for the IO signals connected to Bank B of the FMC connector.

Rule 5.117: The VIO_B_M2C power supplies shall be monotonic.

Rule 5.118: VIO_B_M2C shall meet the limits specified in Table 11

Rule 5.119: When using 3P3V or 12P0V or VADJ to generate VIO_B_M2C, VIO_B_M2C shall be within tolerance 20 millisecond after the supply rail used is within tolerance

Observation 5.31: When generating VIO_B_M2C from 3P3V or 12P0V, VIO_B_M2C must not exceed VADJ.

Rule 5.120: VIO_B_M2C shall be capable of supplying sufficient current for all the signal pins used on Bank B.

Rule 5.121: User defined signals on Bank A shall use the VADJ voltage as the IO power voltage.

Rule 5.122: If the carrier card cannot provide the VADJ requested by the mezzanine module then this voltage is considered to be out of tolerance and the carrier card shall drive the PG low.

Rule 5.123: The carrier card shall obtain the value required for the VADJ from the non-volatile storage device located on the mezzanine card and set VADJ to this value. If the carrier card can not set the required voltage then VADJ is set to 0V or is isolated from the power source.

Permission 5.13: VADJ may be used for other purposes beyond its use for Bank A IO supply voltage.

Permission 5.14: VADJ may be used to source VIO_B_M2C directly or indirectly.

Permission 5.15: In closed systems where the VADJ for an FMC module is known a-priori to a carrier card. The carrier card may bypass Rule 5.115.

Observation 5.32: Configuration of VADJ requires a level of infrastructure to be in place for normal operation. During development and in prototyping set-ups the interrogation and configuration infrastructure may not be fully operationally, therefore, in these environments developers should understand the activity of VADJ as the voltages levels may be different to those requested by the mezzanine module.

6 Electrical Requirements

6.1. Multi-standard Signal Banks

This standard supports the use of multiple signaling standards between the two FMC I/O banks, Bank A and Bank B, and within each of these I/O banks, provided that there is no conflict within a bank between, the VADJ and VREF_A_M2C for bank A and VIO_B_M2C and VREF_B_M2C for bank B, requirements of the signaling standards being used

Rule 6.1: There shall be no conflict between the VCCIO and VREF requirements for different IO signaling standards required by the mezzanine module from signals within the same bank

Recommendation 6.1: A HPC mezzanine module using signaling standards with differing VIO and VREF requirements can split these requirements between the signaling banks providing two different sets of signals with differing VIO and VREFs.

Observation 6.1: If there is a requirement for more than two such sets of signaling standards, the mezzanine module can use level translation to bring the signaling within the specifications for VIO and VREF for one of the signal banks

6.1.1. Supported Signaling Standards

Observation 6.2: Mezzanine modules and carrier cards should use the values of VADJ/VIO_B_M2C and VREF_A_M2C/VREF_B_M2C given in Table 13 to provide the required signaling standard on the LA*, HA*, HB*, CLK0 and CLK1 signals.

Signaling Standard Required	VADJ / VIO_B_M2C	VREF_A_M2C / VREF_B_M2C
LVTTL	3.3	n/a
LVCMOS33	3.3	n/a
LVCMOS25	2.5	n/a
LVCMOS18	1.8	n/a
LVCMOS15	1.5	n/a
SSTL2 Class 1	2.5	1.25
SSTL2 Class 2	2.5	1.25
SSTL18 Class 1	1.8	0.9
SSTL18 Class 2	1.8	0.9
HSTL18 Class 1	1.8	0.9
HSTL18 Class 2	1.8	0.9
HSTL18 Class 3	1.8	1.1
HSTL18 Class 4	1.8	1.1
HSTL Class 1	1.5	0.75
HSTL Class 2	1.5	0.75
HSTL Class 3	1.5	0.9
HSTL Class 4	1.5	0.9
LVDS	2.5	n/a
LVPECL	2.5	n/a

Table 13.   Supply and Reference Voltages for signaling standards

Observation 6.3: This is not an exhaustive list of the potential signaling standards that may be supported.

Table 14.

6.1.2. Compatibility and interoperability

The following sections outline the provision for multiple IO banks supporting IO standards with differing VIO and VREF requirements. Guidance for the implementation of the '_CC' pins is also provided. The Standard supports a maximum of 1 bank on the LPC connector and 2 banks on the HPC connector.

6.1.2.1. IO, VIO and VREF Grouping

Rule 6.2: IO signals designated LAxx_y and HAxx_y shall be associated with the IO reference voltage VREF_A_M2C.

Rule 6.3: IO signals designated HBxx_y shall be associated with the IO reference voltage VREF_B_M2C.

Rule 6.4: IO signals designated LAxx_y and HAxx_y shall be driven by the common VADJ supply.

Rule 6.5: IO signals designated HBxx_y shall be driven by the common VIO_B_M2C supply.

6.1.2.2. VADJ and VIO_B_M2C

Rule 6.6: The module shall identify its VADJ Voltage requirements to the carrier by the non-volatile EPROM

Rule 6.7: The carrier card shall utilize VADJ as the supply voltage to the FPGA to provide the signaling standards on LAxx_y and HAxx_y signals.

Rule 6.8: The carrier card shall utilize VIO_B_M2C as the supply voltage to the FPGA to provide the signaling standards on HBxx_y signals.
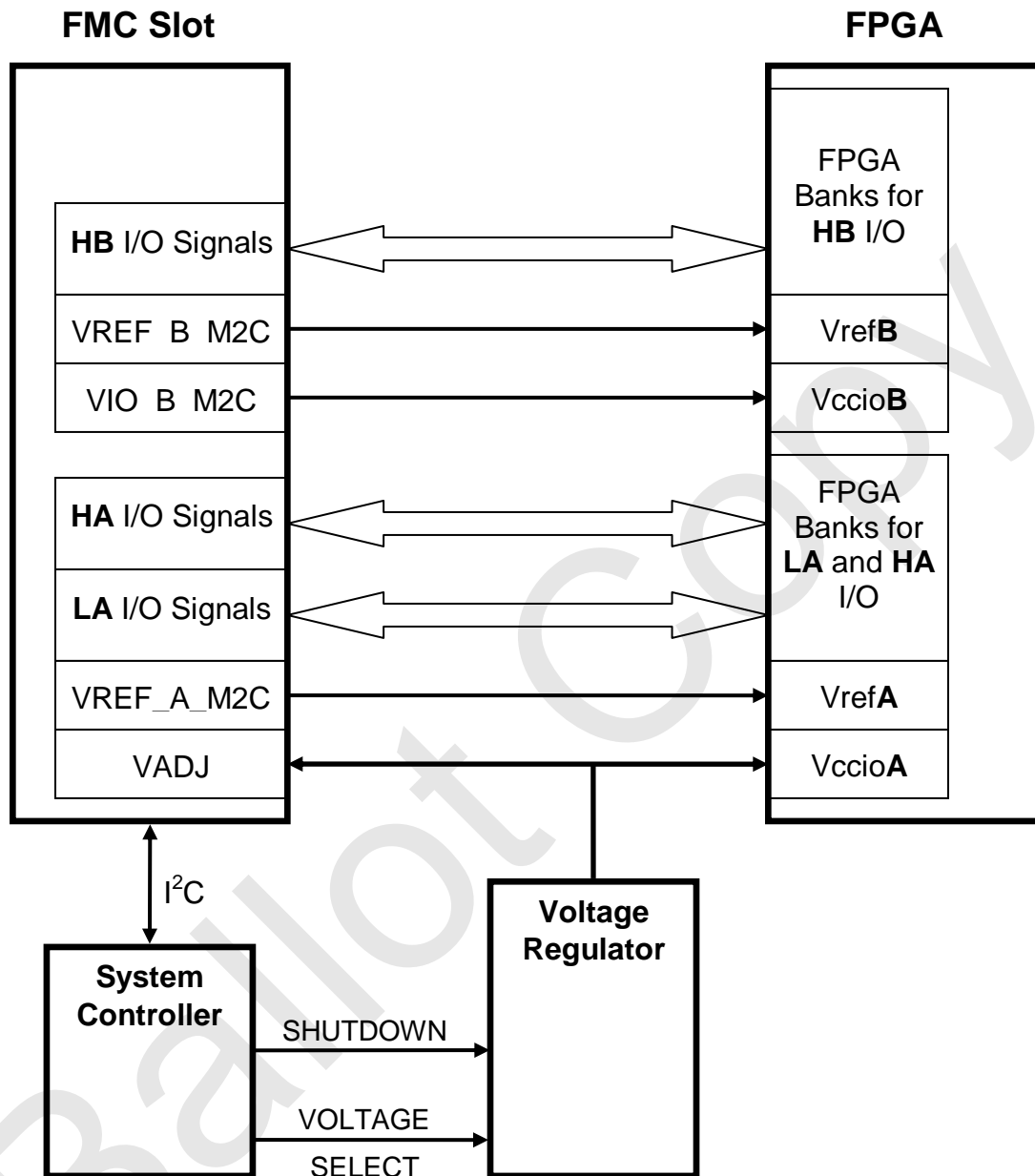
Figure 28. Illustration of I/O Voltage implementation

Figure 28 illustrates an example how the voltages that are associated with the I/O signaling can be implemented. VREF_B_M2C, VIO_B_M2C and VREF_A_M2C are generated by the mezzanine module and can use any available supply present provided all the rules within this standard are adhered too. Typically, these voltages from the mezzanine module will be generated using the VADJ power supply.

VADJ is a flexible supply voltage to meet the requirements of a range of signaling standards and to track the trend of decreasing voltage levels in use. This flexibility requires additional functionality to interrogate the setting for the VADJ and to set an appropriate value. These tasks would be carried out by a system controller which could be implemented in a CPU, standalone FPGA or within the FPGA connected to the FMC slot for example. The typical steps to set up VADJ that would be required for the illustration in Figure 28 are;

1. Power down VADJ until value found by asserting the 'SHUTDOWN' signal
2. Read I^2C non-volatile memory on mezzanine module
3. Determine voltage requested for VADJ from the 'Voltage Required' field in the VADJ DC Load record.
4. If the 'Voltage Required' can not be set on the voltage regulator, then select a value between the 'Minimum voltage' and 'Maximum voltage' fields in the VADJ DC Load record.
5. If the voltage regulator can not be configured to provide a voltage in the range from the minimum to maximum values, then the 'SHUTDOWN' signal remains asserted. Otherwise, setup the voltage regulator to the appropriate voltage output value with the 'VOLTAGE SELECT' signals and deassert the 'SHUTDOWN' signal.

After the VADJ has been enabled, the System Controller should monitor the power good signals, PG_M2C and PG_C2M, until they have both been asserted to ensure that the mezzanine module is within operating tolerances.

6.1.2.3. _CC signals and associated I/O signals

As different FPGAs can have varying relationships between their '_CC' type signals and their I/O signals within a bank, this section proposes a recommendation on the affinity of '_CC' signals to particular I/O signals.

Recommendation 6.1: Carrier cards should connect the primary _CC signal shown in Table 15 to the FPGA so that it can be used with the preferred I/O signals.

Recommendation 6.2: Carrier cards should connect the secondary _CC signal shown in Table 15 to the FPGA so that it can be used with the preferred I/O signals.

Recommendation 6.3: When the primary _CC signal can not be used with the full range of preferred I/O signals, the primary _CC should use the lower ordinal signals and the secondary _CC should use the upper ordinal signals

Primary _CC Signal	Preferred I/O Signals	Secondary _CC Signal
LA00	LA01 – LA16	LA01
LA17	LA18 – LA33	LA18
HA00	HA01 – HA16	HA01
HA17	HA18 – HA23	HA18
HB00	HB01 – HB16	HB06
HB17	HB18 – HB21	n/a

Table 15. Recommended _CC signal association to I/O signals

Check No.	Description	Response
1	Does CC have sufficient pins connected on bank LA for MM	Yes ___, No ___
2	Does CC FPGA support the signaling standards needed on bank LA	Yes ___, No ___
3	Does CC have sufficient pins connected on bank HA for MM	Yes ___, No ___
4	Does CC FPGA support the signaling standards needed on bank HA	Yes ___, No ___
5	Does CC have sufficient pins connected on bank HB for MM	Yes ___, No ___
6	Does CC FPGA support the signaling standards needed on bank HB	Yes ___, No ___
7	Does CC have sufficient Gigabit channels connected for MM	Yes ___, No ___
8	Does CC FPGA support the data rates needed on GBT transceivers	Yes ___, No ___
9	If MM is double width, does the CC have a double width slot	Yes ___, No ___
10	If MM is double width and has a P2 connector, does the CC has a P2 connector	Yes ___, No ___
11	If MM is double width, does CC P2 connector have sufficient pins connected on bank LA	Yes ___, No ___
12	If MM is double width, does CC P2 connector have sufficient pins connected on bank HA	Yes ___, No ___
13	If MM is double width, does CC P2 connector have sufficient pins connected on bank HB	Yes ___, No ___
14	If MM is double width and P1 and P2 connections need to go to the same FPGA on the CC, does the CC support this	Yes ___, No ___
15	If a high pin count connector is needed, does CC have high pin count connector	Yes ___, No ___
16	Does the CC have enough current on 3P3V power rail	Yes ___, No ___
17	Does the CC have enough current on 12P0V power rail	Yes ___, No ___
18	Can the CC provide the voltage requested on VADJ	Yes ___, No ___
19	Can the CC provide the current requested on VADJ	Yes ___, No ___
20	Can the MM provide sufficient current on VIO_B_M2C power rail for the CC	Yes ___, No ___
21	Is the minimum speed of the JTAG clock from the CC is lower than MM max speed	Yes ___, No ___
22	Do the trace lengths of the data lines on the CC meet the skew requirements	Yes ___, No ___
23	Do the trace lengths of the data lines on the MM meet the skew requirements	Yes ___, No ___
24	For air cooled and conduction cooled systems, does the CC and MM satisfy the compatibility table in section 3.5.5	Yes ___, No ___

25	If MM supplies CLK[0..3]_M2C then are they connected to appropriate pins on CC FPGA	Yes ___, No ___
25	If MM requires CC to supply clocks on CLK[2..3]_BIDIR does the carrier card have this capability	Yes ___, No ___
26	If the recommended data pins for clocking in source synchronous applications, postfix of 'CC', are used, are they connected to appropriate pins on the CC FPGA	Yes ___, No ___
27	If MM supplies GBTCLK0 and/or GBTCLK1 then are they connected to appropriate pins on CC FPGA	Yes ___, No ___
28	Can the CC and MM combination provide sufficient cooling	Yes ___, No ___