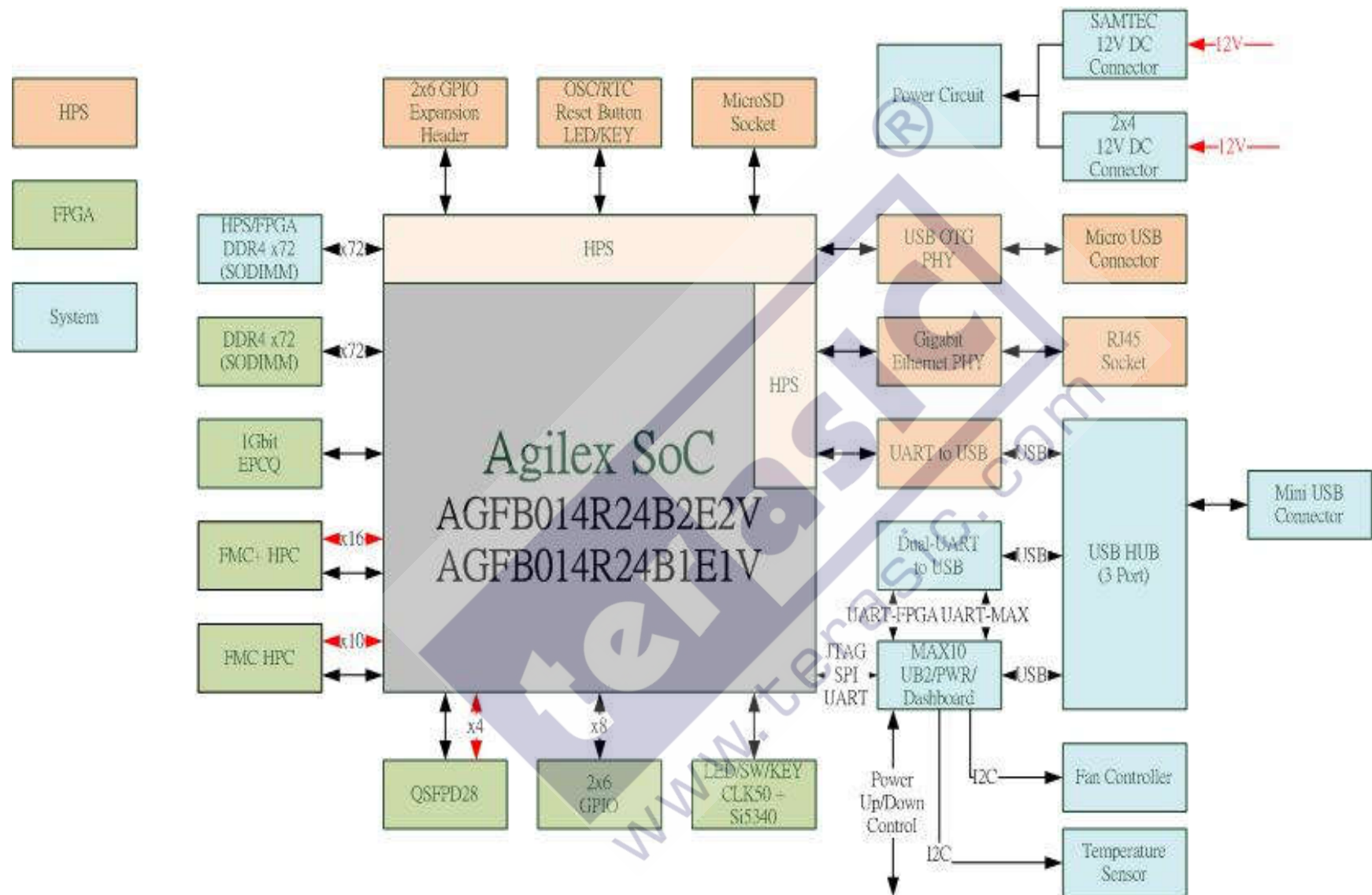


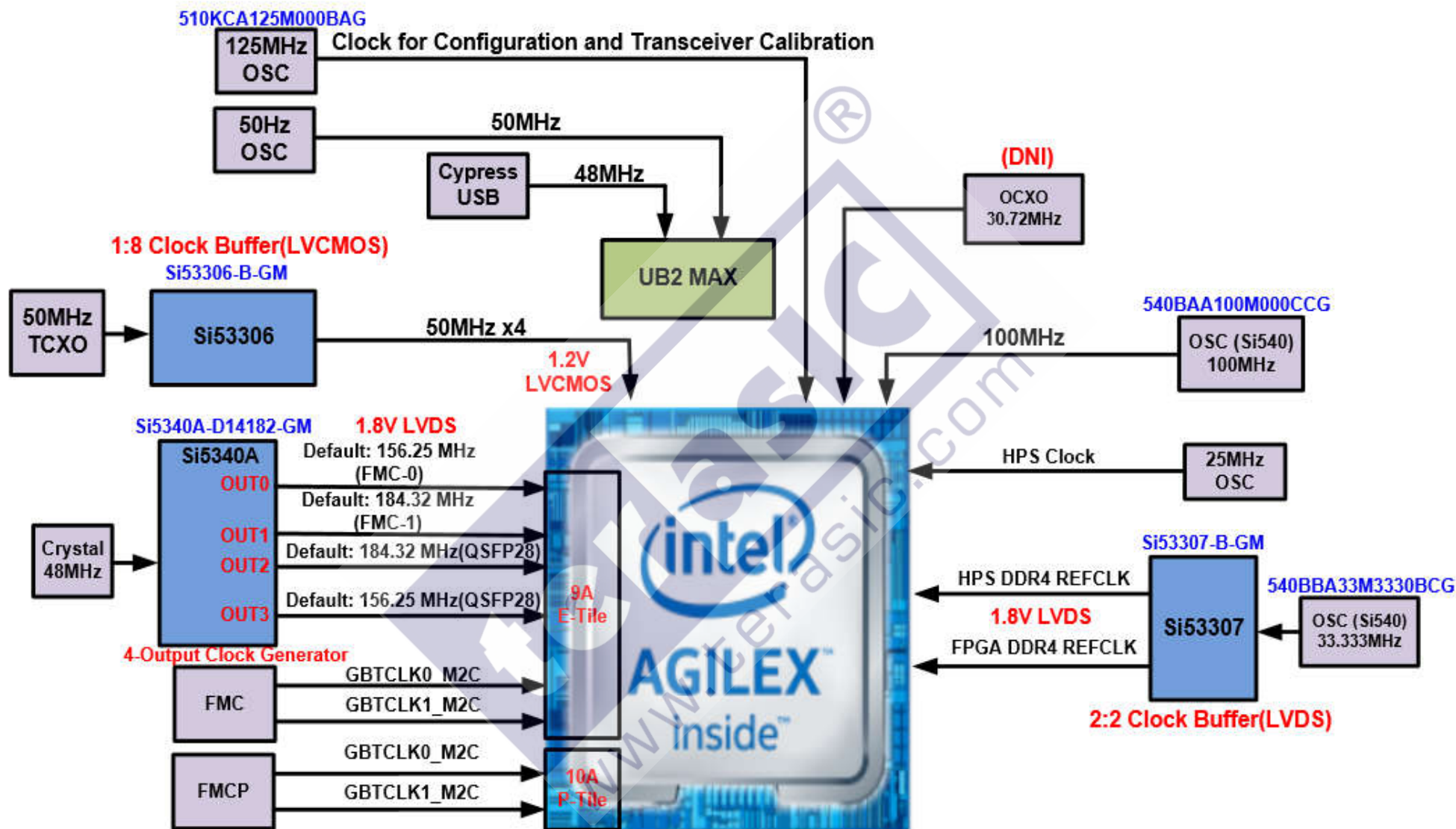
# Agilex SOM Board

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10	FPGA Bank 2C	39	HPS: SD Card, RTC, HPS 2x6 GPIO
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12	FPGA Bank 2A	41	FAN Control and Temperature Monitor
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16	FPGA Bank 3A	45	Power - 3.3V and 0.9V
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18	FPGA Bank 9A E-tile	47	Power - 0.8V, 1.1V, 1.8V
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20	FPGA Configuration	49	Power - 1.8V, 2.5V, 5V
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22	FPGA Power 2	51	Power - Power-Down Discharge
23	FPGA GND 1		
24	FPGA GND 2		
25	FPGA NC/DNU		
26	FPGA Decoupling 1		
27	FPGA Decoupling 2		
28	FPGA Decoupling 3		
29	DDR4 SO-DIMM A		

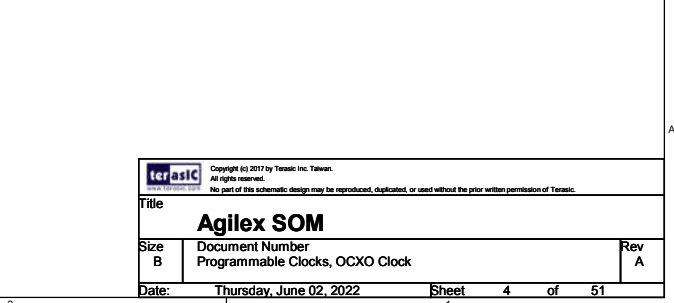
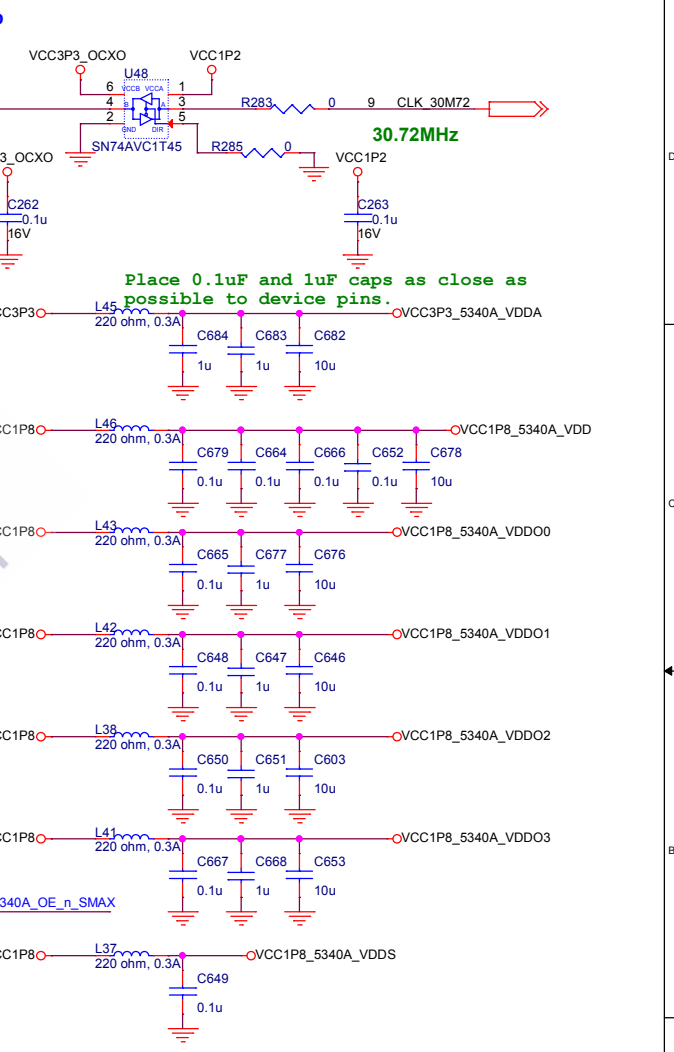
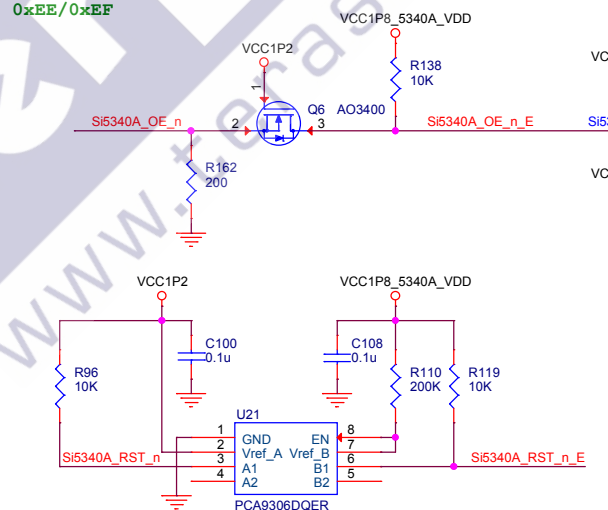
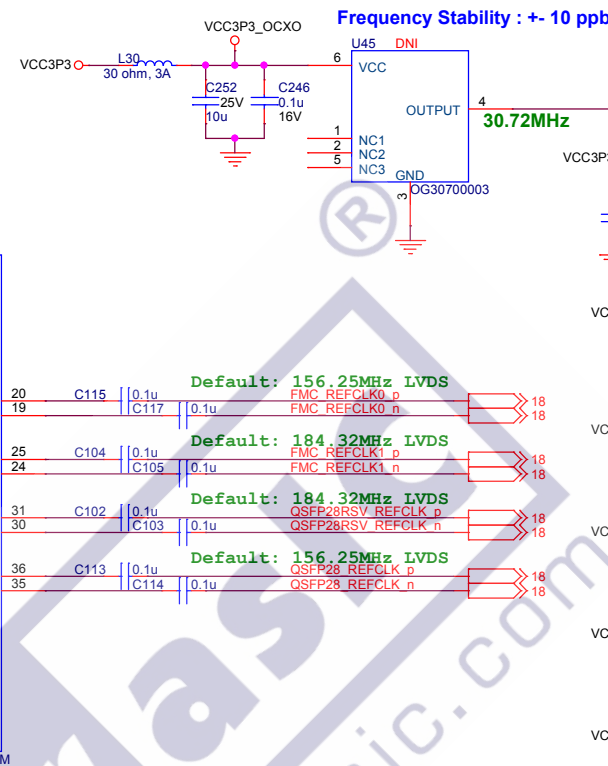
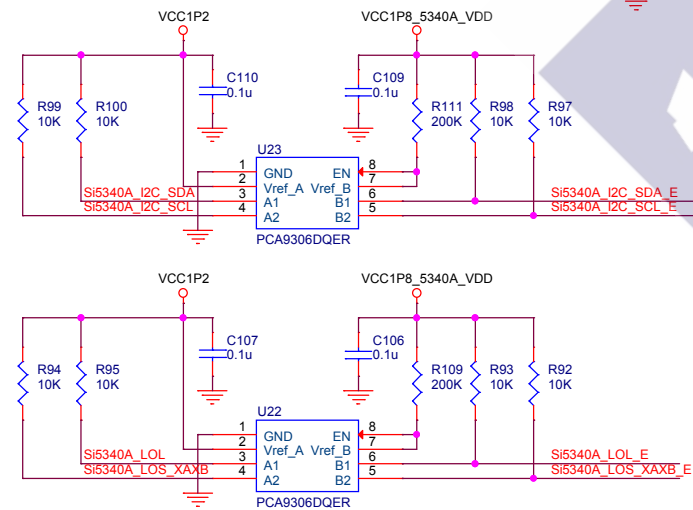
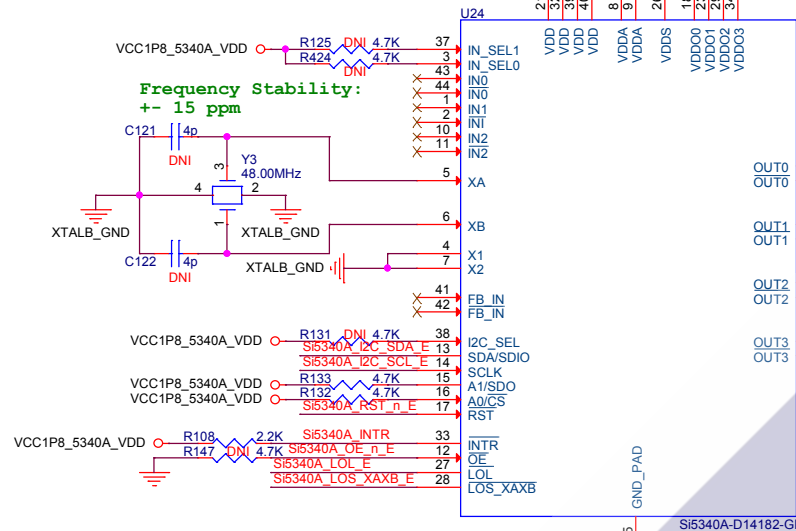
Block Diagram



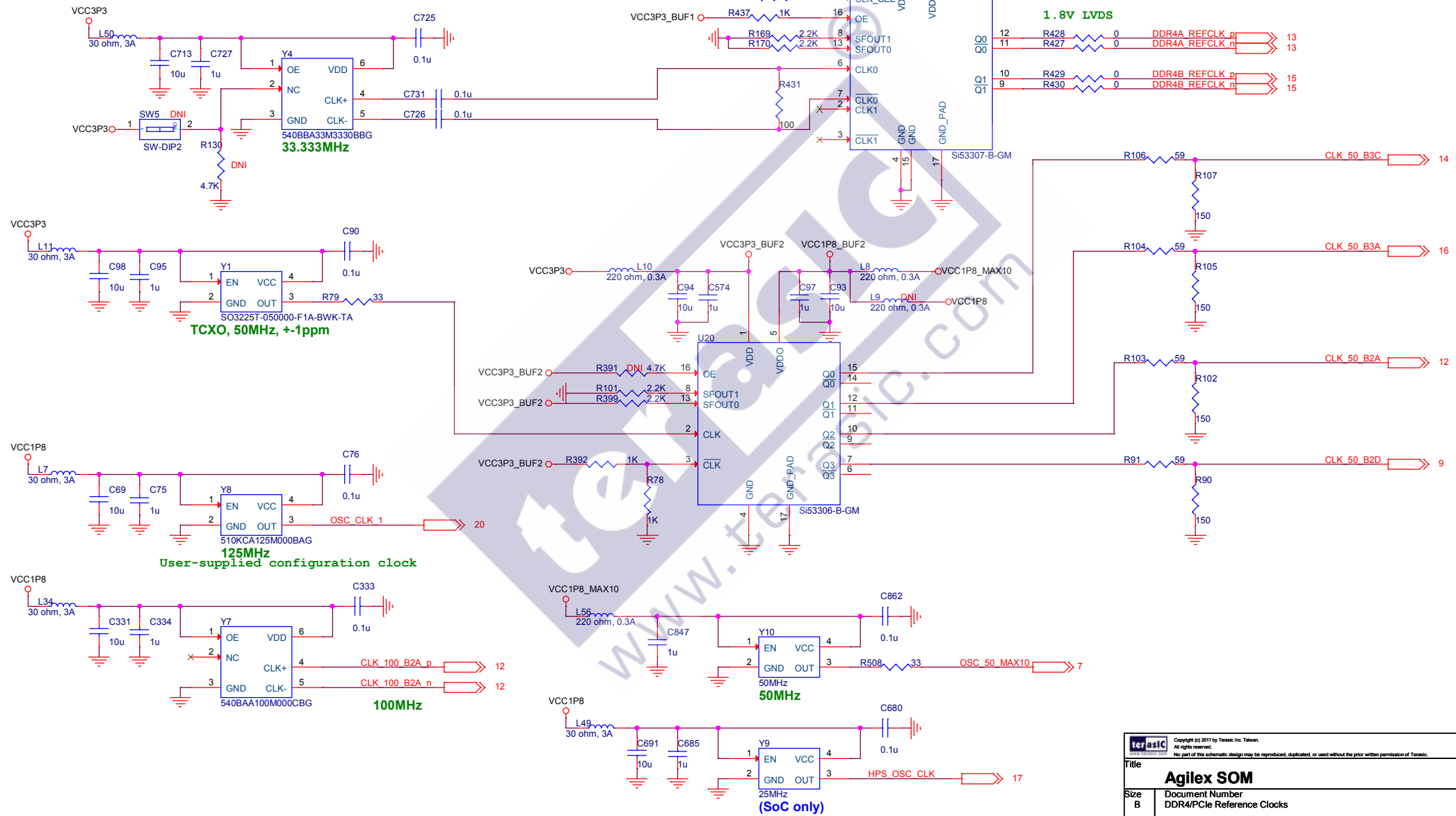
# Clock Tree



SI5340A\_I2C\_SDA 14  
 SI5340A\_I2C\_SCL 14  
 SI5340A\_RST\_n 14  
 SI5340A\_OE\_n 14  
 SI5340A\_LOL 14  
 SI5340A\_LOS\_XAXB 14



Title <b>Agilex SOM</b>		
Size B	Document Number Programmable Clocks, OCXO Clock	Rev A
Date:	Thursday, June 02, 2022	Sheet 4 of 51





## FPGA Temperature Control and Monitor (by System MAX)

TEMP\_I2C\_SCL 41  
TEMP\_I2C\_SDA 41

## FPGA/UB2 MAX SPI

INFO\_SPI\_SCLK 16  
INFO\_SPI\_CS\_n 16  
INFO\_SPI\_MOSI 16  
INFO\_SPI\_MISO 16

## FPGA UART to USB

AG\_UART\_RX 14  
AG\_UART\_TX 14  
AG\_UART\_CTS 14  
AG\_UART\_RTS 14

AG\_UART\_RX\_E 40  
AG\_UART\_TX\_E 40  
AG\_UART\_CTS\_E 40  
AG\_UART\_RTS\_E 40

FMCP\_PRSNLT\_M2C\_L 32

FMC\_PRSNLT\_M2C\_L 33

LTM4700\_FAULT\_n 46

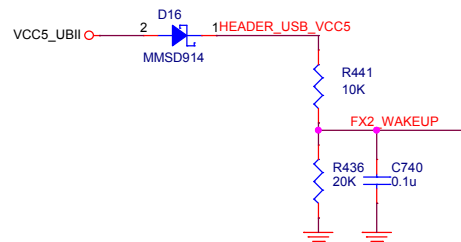
USB\_CLK 7

FX2\_RESETrn 7,40

## FPGA Power Enable Signal

46,51 GROUP1\_PWR\_VCC\_EN  
47,49,51 GROUP2\_PWR\_EN  
48,50,51 GROUP3\_PWR\_EN

# On Board USB BLASTER II 1



AG\_UART\_RX D1  
AG\_UART\_TX C2  
AG\_UART\_CTS E3  
AG\_UART\_RTS E4  
INFO\_SPI\_SCLK C1  
INFO\_SPI\_CS\_n B1  
INFO\_SPI\_MOSI F1  
INFO\_SPI\_MISO E1

POWER\_LEDG F4  
LTM4700\_FAULT\_n C4  
POWER\_LEDH H2  
FMCP\_PRSNLT\_M2C\_L H3

MAX10 10M08SCU169C8G

FX2\_FLAGG L5  
FX2\_PA1 M4  
FX2\_FLAGB L4  
FX2\_PA5 M5  
FX2\_FLAGA K5  
FX2\_PA3 N4  
FX2\_PB8 J5  
FX2\_PA7 N5  
FX2\_PA2 N6  
FX2\_PA4 N7  
FX2\_PA6 M7  
FX2\_PD4 N8  
FX2\_PB5 J6  
FX2\_PD5 M8  
FX2\_PB7 K6  
FX2\_PD7 M9  
FX2\_SDA J7  
FX2\_PA0 K7  
FX2\_SLRDn M13  
FX2\_PB1 N10  
FX2\_PB4 M12  
FX2\_PB6 N9  
FX2\_PB2 M11  
FX2\_PB0 L11  
FX2\_SCL J8  
FX2\_SLWRn K8  
FX2\_PB3 M10  
FX2\_L10 L10

MAX10 10M08SCU169C8G

FX2\_FLAGG L5  
FX2\_PA1 M4  
FX2\_FLAGB L4  
FX2\_PA5 M5  
FX2\_FLAGA K5  
FX2\_PA3 N4  
FX2\_PB8 J5  
FX2\_PA7 N5  
FX2\_PA2 N6  
FX2\_PA4 N7  
FX2\_PA6 M7  
FX2\_PD4 N8  
FX2\_PB5 J6  
FX2\_PD5 M8  
FX2\_PB7 K6  
FX2\_PD7 M9  
FX2\_SDA J7  
FX2\_PA0 K7  
FX2\_SLRDn M13  
FX2\_PB1 N10  
FX2\_PB4 M12  
FX2\_PB6 N9  
FX2\_PB2 M11  
FX2\_PB0 L11  
FX2\_SCL J8  
FX2\_SLWRn K8  
FX2\_PB3 M10  
FX2\_L10 L10

MAX10 10M08SCU169C8G

FX2\_FLAGG L5  
FX2\_PA1 M4  
FX2\_FLAGB L4  
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FX2\_PA3 N4  
FX2\_PB8 J5  
FX2\_PA7 N5  
FX2\_PA2 N6  
FX2\_PA4 N7  
FX2\_PA6 M7  
FX2\_PD4 N8  
FX2\_PB5 J6  
FX2\_PD5 M8  
FX2\_PB7 K6  
FX2\_PD7 M9  
FX2\_SDA J7  
FX2\_PA0 K7  
FX2\_SLRDn M13  
FX2\_PB1 N10  
FX2\_PB4 M12  
FX2\_PB6 N9  
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FX2\_PB0 L11  
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FX2\_PB3 M10  
FX2\_L10 L10

MAX10 10M08SCU169C8G

FX2\_FLAGG L5  
FX2\_PA1 M4  
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FX2\_PA3 N4  
FX2\_PB8 J5  
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FX2\_PA2 N6  
FX2\_PA4 N7  
FX2\_PA6 M7  
FX2\_PD4 N8  
FX2\_PB5 J6  
FX2\_PD5 M8  
FX2\_PB7 K6  
FX2\_PD7 M9  
FX2\_SDA J7  
FX2\_PA0 K7  
FX2\_SLRDn M13  
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FX2\_PB4 M12  
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FX2\_PB3 M10  
FX2\_L10 L10

MAX10 10M08SCU169C8G

FX2\_FLAGG L5  
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FX2\_PA3 N4  
FX2\_PB8 J5  
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FX2\_PA2 N6  
FX2\_PA4 N7  
FX2\_PA6 M7  
FX2\_PD4 N8  
FX2\_PB5 J6  
FX2\_PD5 M8  
FX2\_PB7 K6  
FX2\_PD7 M9  
FX2\_SDA J7  
FX2\_PA0 K7  
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MAX10 10M08SCU169C8G

FX2\_FLAGG L5  
FX2\_PA1 M4  
FX2\_FLAGB L4  
FX2\_PA5 M5  
FX2\_FLAGA K5  
FX2\_PA3 N4  
FX2\_PB8 J5  
FX2\_PA7 N5  
FX2\_PA2 N6  
FX2\_PA4 N7  
FX2\_PA6 M7  
FX2\_PD4 N8  
FX2\_PB5 J6  
FX2\_PD5 M8  
FX2\_PB7 K6  
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FX2\_PB6 N9  
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FX2\_L10 L10

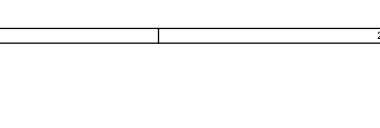
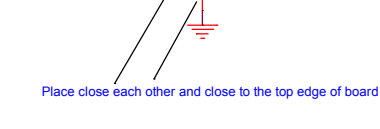
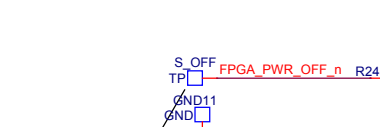
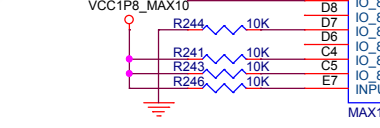
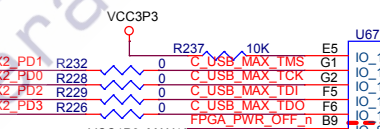
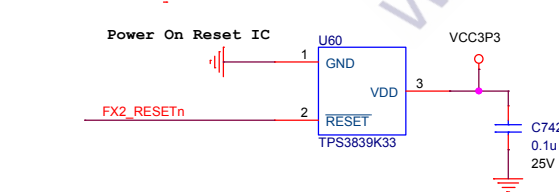
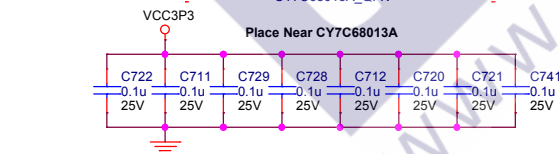
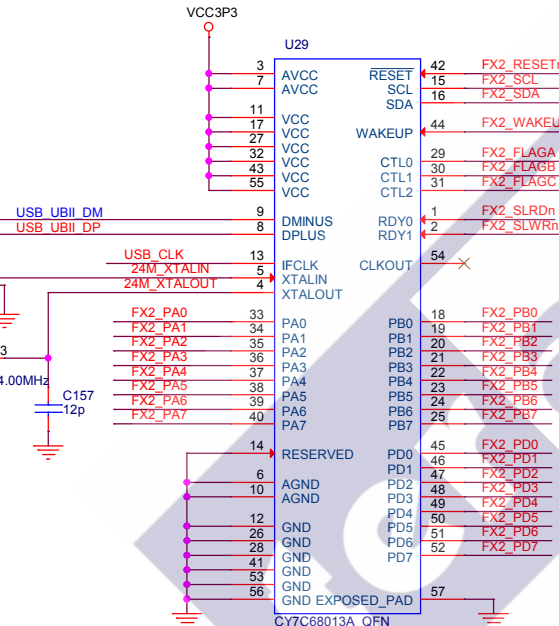
MAX10 10M08SCU169C8G

FX2\_FLAGG L5  
FX2\_PA1 M4  
FX2\_FLAGB L4  
FX2\_PA5 M5  
FX2\_FLAGA K5  
FX2\_PA3 N4  
FX2\_PB8 J5  
FX2\_PA7 N5  
FX2\_PA2 N6  
FX2\_PA4 N7  
FX2\_PA6 M7  
FX2\_PD4 N8  
FX2\_PB5 J6  
FX2\_PD5 M8  
FX2\_PB7 K6  
FX2\_PD7 M9  
FX2\_SDA J7  
FX2\_PA0 K7  
FX2\_SLRDn M13  
FX2\_PB1 N10  
FX2\_PB4 M12  
FX2\_PB6 N9  
FX2\_PB2 M11  
FX2\_PB0 L11  
FX2\_SCL J8  
FX2\_SLWRn K8  
FX2\_PB3 M10  
FX2\_L10 L10

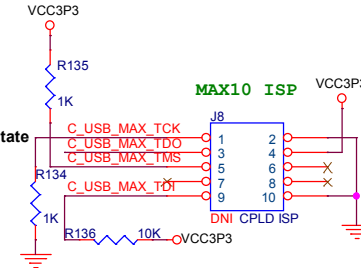
MAX10 10M08SCU169C8G

FX2\_FLAGG L5  
FX2\_PA1 M4  
FX2\_FLAGB L4  
FX2\_PA5 M5  
FX2\_FLAGA K5  
FX2\_PA3 N4  
FX2\_PB8 J5  
FX2\_PA7 N5  
FX2\_PA2 N6  
FX2\_PA4 N7  
FX2\_PA6 M7  
FX2\_PD4 N8  
FX2\_PB5 J6  
FX2\_PD5 M8  
FX2\_PB7 K6  
FX2\_PD7 M9  
FX2\_SDA J7  
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FX2\_SLRDn M13  
FX2\_PB1 N10  
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FX2\_SCL J8  
FX2\_SLWRn K8  
FX2\_PB3 M10  
FX2\_L10 L10

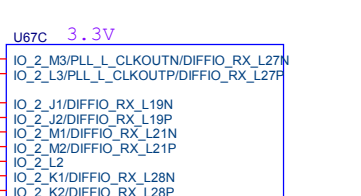
MAX10 10M08SCU169C8G



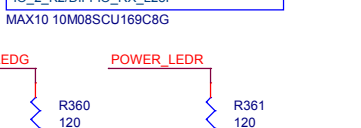
UB2 doesn't drive S10  
if FPGA\_PWRGD is low  
(UB2 bank 5/6/8 IOs are tri-state  
if FPGA\_PWRGD is low)



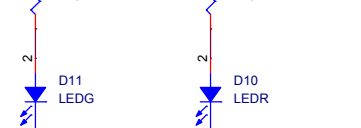
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GROUP2\_PWR\_EN L3  
GROUP3\_PWR\_EN J1  
AG\_UART\_RX E J2  
AG\_UART\_TX E M1  
AG\_UART\_CTS E M2  
AG\_UART\_RTS E L2  
TEMP\_I2C\_SCL K1  
TEMP\_I2C\_SDA K2



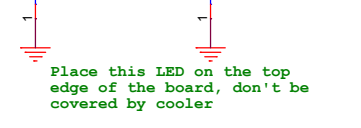
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GROUP2\_PWR\_EN L3  
GROUP3\_PWR\_EN J1  
AG\_UART\_RX E J2  
AG\_UART\_TX E M1  
AG\_UART\_CTS E M2  
AG\_UART\_RTS E L2  
TEMP\_I2C\_SCL K1  
TEMP\_I2C\_SDA K2



GROUP1\_PWR\_VCC\_EN M3  
GROUP2\_PWR\_EN L3  
GROUP3\_PWR\_EN J1  
AG\_UART\_RX E J2  
AG\_UART\_TX E M1  
AG\_UART\_CTS E M2  
AG\_UART\_RTS E L2  
TEMP\_I2C\_SCL K1  
TEMP\_I2C\_SDA K2



GROUP1\_PWR\_VCC\_EN M3  
GROUP2\_PWR\_EN L3  
GROUP3\_PWR\_EN J1  
AG\_UART\_RX E J2  
AG\_UART\_TX E M1  
AG\_UART\_CTS E M2  
AG\_UART\_RTS E L2  
TEMP\_I2C\_SCL K1  
TEMP\_I2C\_SDA K2



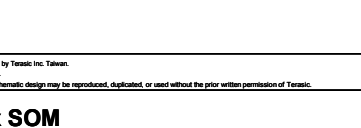
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GROUP2\_PWR\_EN L3  
GROUP3\_PWR\_EN J1  
AG\_UART\_RX E J2  
AG\_UART\_TX E M1  
AG\_UART\_CTS E M2  
AG\_UART\_RTS E L2  
TEMP\_I2C\_SCL K1  
TEMP\_I2C\_SDA K2



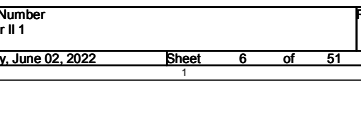
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GROUP2\_PWR\_EN L3  
GROUP3\_PWR\_EN J1  
AG\_UART\_RX E J2  
AG\_UART\_TX E M1  
AG\_UART\_CTS E M2  
AG\_UART\_RTS E L2  
TEMP\_I2C\_SCL K1  
TEMP\_I2C\_SDA K2



GROUP1\_PWR\_VCC\_EN M3  
GROUP2\_PWR\_EN L3  
GROUP3\_PWR\_EN J1  
AG\_UART\_RX E J2  
AG\_UART\_TX E M1  
AG\_UART\_CTS E M2  
AG\_UART\_RTS E L2  
TEMP\_I2C\_SCL K1  
TEMP\_I2C\_SDA K2



GROUP1\_PWR\_VCC\_EN M3  
GROUP2\_PWR\_EN L3  
GROUP3\_PWR\_EN J1  
AG\_UART\_RX E J2  
AG\_UART\_TX E M1  
AG\_UART\_CTS E M2  
AG\_UART\_RTS E L2  
TEMP\_I2C\_SCL K1  
TEMP\_I2C\_SDA K2



GROUP1\_PWR\_VCC\_EN M3  
GROUP2\_PWR\_EN L3  
GROUP3\_PWR\_EN J1  
AG\_UART\_RX E J2  
AG\_UART\_TX E M1  
AG\_UART\_CTS E M2  
AG\_UART\_RTS E L2  
TEMP\_I2C\_SCL K1  
TEMP\_I2C\_SDA K2



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Title	Agilex SOM	
Size	Document Number	Rev
B	USB Blaster II 1	A
Date:	Thursday, June 02, 2022	Sheet 6 of 51

## Agilex Configuration Setting

FPGA nCONFIG	20
FPGA nSTATUS	20
FPGA CONF_DONE	20

### FAN Control Interface

FAN I2C_SCL	41
FAN I2C_SDA	41
FAN_ALERT_n	41

### 12V Power Monitor Interface

PM I2C_SCL	44
PM I2C_SDA	44
PM_ALERT_N	44

### 50MHz CLK

OSC_50_MAX10	5
--------------	---

### 48MHz CLK

USB_CLK	6
---------	---

### System MAX UART to USB

MAX_UART_RX	40
MAX_UART_TX	40
MAX_UART_CTS	40
MAX_UART_RTS	40

### HPS JTAG Interface (To HPS)

HPS_JTAG_TCK	17
HPS_JTAG_TMS	17
HPS_JTAG_TDI	17
HPS_JTAG_TDO	17

### HPS Reset

HPS_COLD_RESET_N	42
SYS_HPS_RST_n	20,36,37,38

### ADC

ADC_CS_n	44
ADC_SDO	44
ADC_SCLK	44

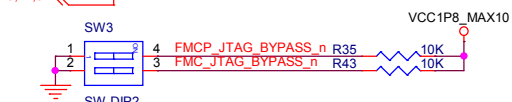
### FX2 RESETn

FX2_RESETn	6,40
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### Agilex JTAG Interface (To Agilex)

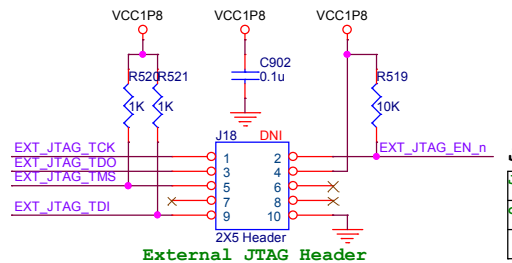
AG_JTAG_TCK	20
AG_JTAG_TMS	20
AG_JTAG_TDI	20
AG_JTAG_TDO	20

### GROUP1\_PWR\_VCCCH\_EN



### Default bypass two FMC JTAG

ON = JTAG Bypass  
OFF = JTAG Enable



### JTAG Master Select

JTAG Master	EXT_JTAG_EN_n
on-board UB2	High
EXT JTAG	Low

## On Board USB BLASTER II 2

### U67F 1.8V

VCC_CORE_PG	F12
VCC0P9_VCCCH_PG	E12
VCC1P8_VCCIO_PG	C13
AG_JTAG_TCK	F8
AG_JTAG_TDO	B12
VCC1P8_PG	E9
AG_JTAG_TMS	B11
VCC0P8_VCCCL_SDM_PG	C12
VCC1P1_VCCCH_GXE_PG	B13
VCC2P5_VCCCLK_GXE_PG	C11
VCC1P2_PG	A12
AG_JTAG_TDI	E10
VCC1P8_FUSEWR_SDM_PG	D9
VCC3P3_PG	D12
CPU_RST_1P8	D11

MAX10 10M08SCU169C8G

### U67E 3.3V

MAX_UART_RX	K10
MAX_UART_TX	K11
MAX_UART_CTS	J10
MAX_UART_RTS	L12
PM I2C_SCL	K12
PM I2C_SDA	L13
CPU_RST_1P8	J12
PM_ALERT_N	J12
FAN I2C_SCL	J9
FAN I2C_SDA	J13
FAN_ALERT_n	H10
FMCP_JTAG_TDI	H13
FMCP_JTAG_TMS	H9
FMCP_JTAG_TDO	G13
FMCP_JTAG_TCK	H8
FMCP_JTAG_TDI	G12

MAX10 10M08SCU169C8G

MAX 10 instant mode has power ramp up requirement

### U67H

GROUP1_PWR_VCCCH_EN	G5
USB_CLK	H6
FMC_JTAG_TMS	H5
FMC_JTAG_TDO	H4
FMC_JTAG_TCK	N2
FX2_RESETn	N3
FPGA_nCONFIG	G9
FPGA_nSTATUS	G10
OSC_50_MAX10	F13
FPGA_CONF_DONE	E13
HPS_COLD_RESET_N	F9
SYS_HPS_RST_n	F10
LTM4700_EN_NO_PL	H1
L1	L1
N11	N11
K13	K13
VCCIO_FMC_HAB_PG	D13
B7	B7

MAX10 10M08SCU169C8G

### FMC+ JTAG Interface

FMCP_JTAG_TCK	32
FMCP_JTAG_TMS	32
FMCP_JTAG_TDI	32
FMCP_JTAG_TDO	32

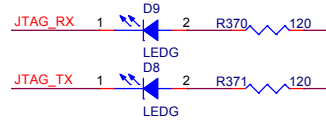
### FMC JTAG Interface

FMC_JTAG_TCK	33
FMC_JTAG_TMS	33
FMC_JTAG_TDI	33
FMC_JTAG_TDO	33

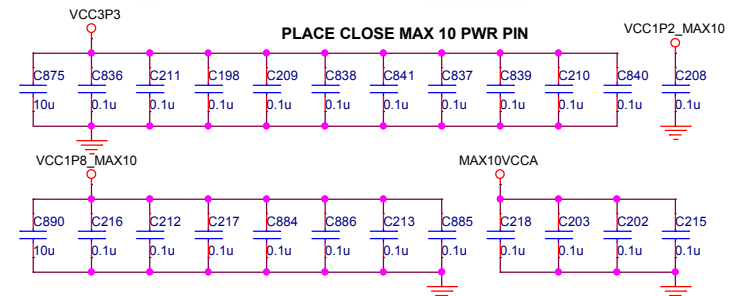
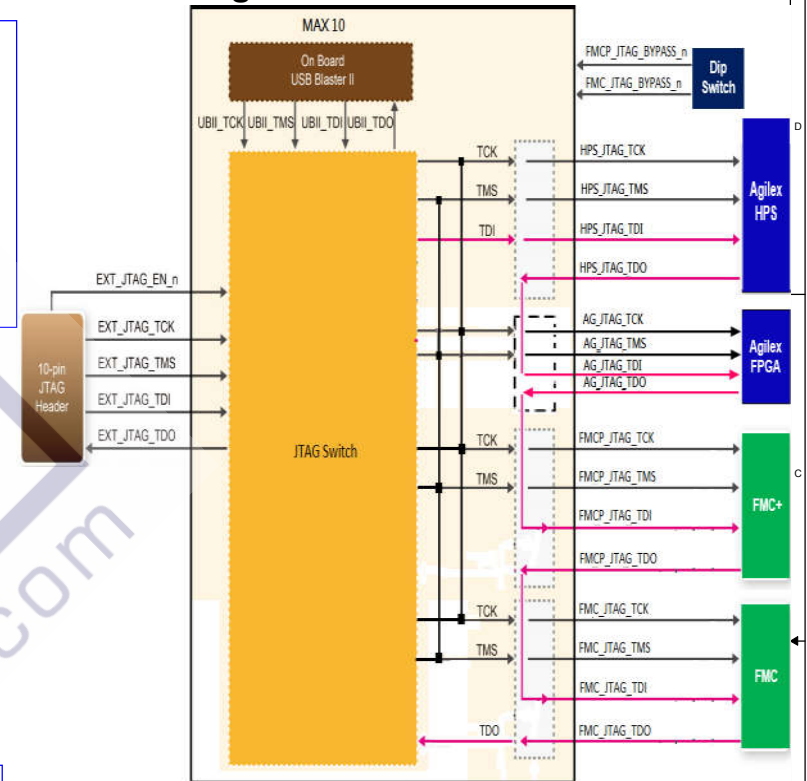
### U67A

VCCIO1A_F2	F2
VCCIO1B_G3	G3
VCCIO2_K3	K3
VCCIO2_J3	L8
VCCIO3_L8	L7
VCCIO3_L7	L6
VCCIO5_J11	J11
VCCIO5_H11	H11
VCCIO6_G11	G11
VCCIO6_F11	F11
VCCIO8_C8	C8
VCCIO8_C7	C7
VCCIO8_C6	C6
VCCA3_D3	D3
VCCA1_K4	K4
VCCA2_M4	M4
VCCA3_D4	D4
VCCA4_K9	K9
VCC_ONE_H7	H7
VCC_ONE_G8	G8
VCC_ONE_G6	G6
VCC_ONE_F7	F7

MAX10 10M08SCU169C8G



## Agilex SOM JTAG Chain

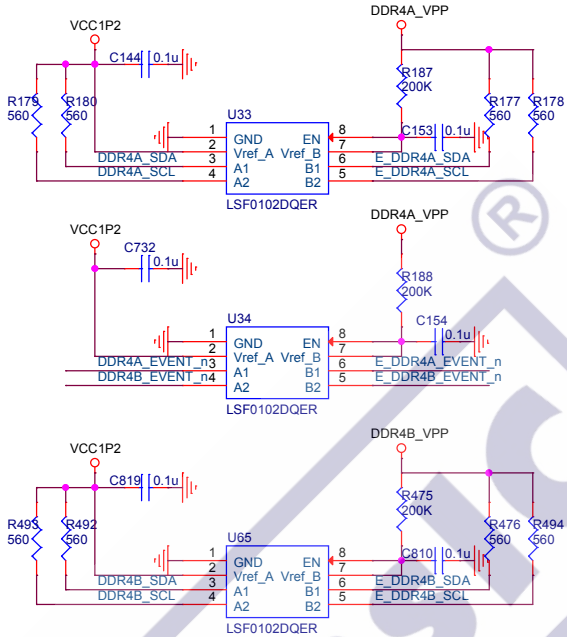
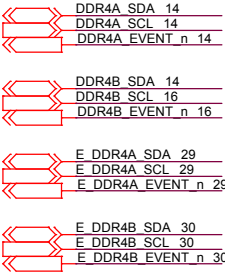


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### Agilex SOM

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SO-DIMM A/B SPD Interface





# FPGA Bank - 2D

U15B

FMC\_LA\_n29 CF3  
FMC\_LA\_p29 CH3  
FMC\_LA\_n23 CE4  
FMC\_LA\_p23 CG4  
FMC\_LA\_n22 CF5  
FMC\_LA\_p22 CH5  
FMC\_LA\_n26 CE6  
FMC\_LA\_p26 CG6  
FMC\_LA\_n33 CF7  
FMC\_LA\_p33 CH7  
FMC\_LA\_n28 CE8  
FMC\_LA\_p28 CG8  
FMC\_LA\_n25 CK3  
FMC\_LA\_p25 CM3  
FMC\_LA\_n21 CL4  
FMC\_LA\_p21 CN4  
FMC\_LA\_n31 CK5  
FMC\_LA\_p31 CM5  
FMC\_LA\_n24 CL6  
FMC\_LA\_p24 CN6  
FMC\_LA\_n27 CK7  
FMC\_LA\_p27 CM7  
CLK\_30M72 CN8  
FMC\_CLK\_M2C\_n0 CE10  
FMC\_CLK\_M2C\_p0 CG10  
FMC\_LA\_n30 CF11  
FMC\_LA\_p30 CH11  
CE12  
CG12  
CF13  
CH13  
CE14  
CG14  
CF15  
CH15  
CL10  
CN10  
CK11  
CM11  
CL12  
CN12  
CK13  
CM13  
CL14  
CN14  
CK15  
CM15

FMC\_LA\_n32  
FMC\_LA\_p32

FMC\_CLK3\_BIDIR\_n  
FMC\_CLK3\_BIDIR\_p  
FMC\_RES0

FMC\_SDA  
FMC\_SCL

FMC\_CLK3\_BIDIR\_p\_33  
FMC\_CLK3\_BIDIR\_n\_33

FMC\_CLK2\_BIDIR\_n  
FMC\_CLK2\_BIDIR\_p

AGFB014R24B1E1V

BOT TOP

Bank 2D vccio = 1.2v

RX\_2D1n IO, LVDS2D\_1N, DQ0  
RX\_2D1p IO, LVDS2D\_1P, DQ0  
TX\_2D1n IO, LVDS2D\_2N, DQ0  
TX\_2D1p IO, LVDS2D\_2P, DQ0  
RX\_2D2n IO, LVDS2D\_3N, DQ0  
RX\_2D2p IO, LVDS2D\_3P, DQ0  
TX\_2D2n IO, LVDS2D\_4N, DQ0  
TX\_2D2p IO, LVDS2D\_4P, DQ0  
RX\_2D3n IO, LVDS2D\_5N, DQ0  
RX\_2D3p IO, LVDS2D\_5P, DQ0  
TX\_2D3n IO, LVDS2D\_6N, DQ0  
TX\_2D3p IO, LVDS2D\_6P, DQ0  
RX\_2D4n IO, LVDS2D\_7N, DQ0  
RX\_2D4p IO, LVDS2D\_7P, DQ0  
TX\_2D4n IO, LVDS2D\_8N, DQ0  
TX\_2D4p IO, LVDS2D\_8P, DQ0  
RX\_2D5n IO, LVDS2D\_9N, DQ0  
RX\_2D5p IO, LVDS2D\_9P, DQ0  
TX\_2D5n IO, PLL\_2D\_T\_CLKOUT1N, LVDS2D\_10N, DQS1  
TX\_2D5p IO, PLL\_2D\_T\_CLKOUT1P, PLL\_2D\_T\_CLKOUT1, PLL\_2D\_T\_FB1, LVDS2D\_10P, DQS1  
RX\_2D6n IO, LVDS2D\_11N, DQ1  
RX\_2D6p IO, RZQ\_T\_2D, LVDS2D\_11P, DQ1  
TX\_2D6n IO, CLK\_T\_2D\_1N, LVDS2D\_12N, DQ1  
TX\_2D6p IO, CLK\_T\_2D\_1P, LVDS2D\_12P, DQ1  
RX\_2D7n IO, CLK\_T\_2D\_0N, LVDS2D\_13N, DQ2  
RX\_2D7p IO, CLK\_T\_2D\_0P, LVDS2D\_13P, DQ2  
TX\_2D7n IO, LVDS2D\_14N, DQ2  
TX\_2D7p IO, LVDS2D\_14P, DQ2  
RX\_2D8n IO, PLL\_2D\_T\_CLKOUT0N, LVDS2D\_15N, DQ2  
RX\_2D8p IO, PLL\_2D\_T\_CLKOUT0P, PLL\_2D\_T\_CLKOUT0, PLL\_2D\_T\_FB0, LVDS2D\_15P, DQ2  
TX\_2D8n IO, LVDS2D\_16N, DQS2  
TX\_2D8p IO, LVDS2D\_16P, DQS2  
RX\_2D9n IO, LVDS2D\_17N, DQ2  
RX\_2D9p IO, LVDS2D\_17P, DQ2  
TX\_2D9n IO, LVDS2D\_18N, DQ2  
TX\_2D9p IO, LVDS2D\_18P, DQ2  
RX\_2D10n IO, LVDS2D\_19N, DQ3  
RX\_2D10p IO, LVDS2D\_19P, DQ3  
TX\_2D10n IO, LVDS2D\_20N, DQ3  
TX\_2D10p IO, LVDS2D\_20P, DQ3  
RX\_2D11n IO, LVDS2D\_21N, DQ3  
RX\_2D11p IO, LVDS2D\_21P, DQ3  
TX\_2D11n IO, LVDS2D\_22N, DQS3  
TX\_2D11p IO, LVDS2D\_22P, DQS3  
RX\_2D12n IO, LVDS2D\_23N, DQ3  
RX\_2D12p IO, LVDS2D\_23P, DQ3  
TX\_2D12n IO, LVDS2D\_24N, DQ3  
TX\_2D12p IO, LVDS2D\_24P, DQ3

CT3 FMC\_GA0  
CV3 FMC\_GA1  
CR4 FMC\_LA\_n13  
CU4 FMC\_LA\_p13  
CT5 FMC\_LA\_n20  
CV5 FMC\_LA\_p20  
CU6 FMC\_LA\_n4  
CR6 FMC\_LA\_p4  
CT7 FMC\_LA\_n18  
CV7 FMC\_LA\_p18  
CR8 FMC\_LA\_n17  
CU8 FMC\_LA\_p17  
CT1 FMC\_LA\_n14  
CV1 FMC\_LA\_p14  
CY3 FMC\_LA\_n9  
DA4 FMC\_LA\_p9  
CY5 FMC\_LA\_n10  
DB5 FMC\_LA\_p10  
DA6 FMC\_LA\_n1  
DC6 FMC\_LA\_p1  
CY7 FMC\_LA\_n16  
DB7 FMC\_LA\_p16  
DA8 CLK\_50\_B2D  
CR10 FMC\_LA\_n0  
CU10 FMC\_LA\_p0  
CT11 FMC\_LA\_n15  
CV11 FMC\_LA\_p15  
CR12  
CU12  
CT13 FMC\_LA\_n2  
CV13 FMC\_LA\_p2  
CR14 FMC\_LA\_n6  
CU14 FMC\_LA\_p6  
CT15 FMC\_LA\_n19  
CV15 FMC\_LA\_p19  
DA10 FMC\_LA\_n3  
DC10 FMC\_LA\_p3  
CY11 FMC\_LA\_n5  
DB11 FMC\_LA\_p5  
DA12 FMC\_LA\_n8  
DC12 FMC\_LA\_p8  
CY13 FMC\_LA\_n7  
DB13 FMC\_LA\_p7  
DA14 FMC\_LA\_n12  
DC14 FMC\_LA\_p12  
CY15 FMC\_LA\_n11  
DB15 FMC\_LA\_p11

CLK\_30M72 4


FMC\_RES0\_33  
FMC\_SDA\_33  
FMC\_SCL\_33  
FMC\_GA1\_0\_33

FMC\_CLK3\_BIDIR\_p\_33  
FMC\_CLK3\_BIDIR\_n\_33  
FMC\_CLK2\_BIDIR\_p\_33  
FMC\_CLK2\_BIDIR\_n\_33

FMC\_LA\_p13\_0\_33  
FMC\_LA\_n13\_0\_33  
FMC\_CLK\_M2C\_n1\_0\_10\_33  
FMC\_CLK\_M2C\_p1\_0\_10\_33

FMC\_HA\_p13\_0\_10\_33  
FMC\_HA\_n13\_0\_10\_33  
FMC\_HB\_p13\_0\_10\_33  
FMC\_HB\_n13\_0\_10\_33

CLK\_50\_B2D 5

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Title		
Agilex SOM		
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FMC LA p[33..0]\_9,33  
FMC LA n[33..0]\_9,33  
FMC HA p[23..0]\_33  
FMC HA n[23..0]\_33  
FMC HB p[21..0]\_33  
FMC HB n[21..0]B3  
FMC CLK\_M2C\_n[1..0]9,33  
FMC CLK\_M2C\_n[1..0]9,33

FMC HA n11 CF17  
FMC HA p11 CH17  
FMC HA n10 CE18  
FMC HA p10 CG18  
FMC HA n20 CF19  
FMC HA p20 CH19  
FMC HA n15 CE20  
FMC HA p15 CG20  
FMC HA n13 CF21  
FMC HA p13 CH21  
FMC HA n8 CE22  
FMC HA p8 CG22  
FMC HA n16 CK17  
FMC HA p16 CM17  
FMC HA n6 CL18  
FMC HA p6 CN18  
FMC HA n7 CK19  
FMC HA p7 CM19  
FMC HA n0 CL20  
FMC HA p0 CN20  
FMC HA n22 CK21  
FMC HA p22 CH21  
FMC HA n23 CL22  
FMC HA p23 CN22  
FMC HA n1 CE24  
FMC HA p1 CG24  
FMC HA n4 CF25  
FMC HA p4 CH25  
FMC HA n13 CE26  
FMC HA p13 CG26  
FMC HA n12 CF27  
FMC HA p12 CH27  
FMC HA n14 CE28  
FMC HA p14 CH28  
FMC HA n19 CF29  
FMC HA p19 CH29  
FMC HA n9 CL24  
FMC HA p9 CN24  
FMC HA n2 CK25  
FMC HA p2 CM25  
FMC HA n5 CL26  
FMC HA p5 CN26  
FMC HA n17 CK27  
FMC HA p17 CM27  
FMC HA n3 CL28  
FMC HA p3 CN28  
FMC HA n21 CK29  
FMC HA p21 CM29

U15C

IO, LVDS2C\_25N, DQ12RX\_2C13n  
IO, LVDS2C\_25P, DQ12RX\_2C13p  
IO, LVDS2C\_26N, DQ12TX\_2C13n  
IO, LVDS2C\_26P, DQ12TX\_2C13p  
IO, LVDS2C\_27N, DQ12RX\_2C14n  
IO, LVDS2C\_27P, DQ12RX\_2C14p  
IO, LVDS2C\_28N, DQSN12TX\_2C14n  
IO, LVDS2C\_28P, DQS12 TX\_2C14p  
IO, LVDS2C\_29N, DQ12 RX\_2C15n  
IO, LVDS2C\_29P, DQ12 RX\_2C15p  
IO, LVDS2C\_30N, DQ12 TX\_2C15n  
IO, LVDS2C\_30P, DQ12 TX\_2C15p  
IO, LVDS2C\_31N, DQ13 RX\_2C16n  
IO, LVDS2C\_31P, DQ13 RX\_2C16p  
IO, LVDS2C\_32N, DQ13 TX\_2C16n  
IO, LVDS2C\_32P, DQ13 TX\_2C16p  
IO, LVDS2C\_33N, DQ13 RX\_2C17n  
IO, LVDS2C\_33P, DQ13 RX\_2C17p  
IO, PLL\_2C\_B\_CLKOUT1N, LVDS2C\_34N, DQSN13TX\_2C17n  
IO, PLL\_2C\_B\_CLKOUT1P, PLL\_2C\_B\_CLKOUT1, PLL\_2C\_B\_FB1, LVDS2C\_34P, DQS13TX\_2C17p  
IO, LVDS2C\_35N, DQ13 RX\_2C18n  
IO, RZQ\_B\_2C, LVDS2C\_35P, DQ13 RX\_2C18p  
IO, CLK\_B\_2C\_1N, LVDS2C\_36N, DQ13TX\_2C18n  
IO, CLK\_B\_2C\_1P, LVDS2C\_36P, DQ13TX\_2C18p  
IO, CLK\_B\_2C\_0N, LVDS2C\_37N, DQ14 RX\_2C19n  
IO, CLK\_B\_2C\_0P, LVDS2C\_37P, DQ14 RX\_2C19p  
IO, LVDS2C\_38N, DQ14 TX\_2C19n  
IO, LVDS2C\_38P, DQ14TX\_2C19p  
IO, PLL\_2C\_B\_CLKOUT0N, LVDS2C\_39N, DQ14RX\_2C20n  
IO, PLL\_2C\_B\_CLKOUT0P, PLL\_2C\_B\_CLKOUT0, PLL\_2C\_B\_FB0, LVDS2C\_39P, DQ14RX\_2C20p  
IO, LVDS2C\_40N, DQSN14TX\_2C20n  
IO, LVDS2C\_40P, DQS14 TX\_2C20p  
IO, LVDS2C\_41N, DQ14 RX\_2C21n  
IO, LVDS2C\_41P, DQ14 RX\_2C21p  
IO, LVDS2C\_42N, DQ14 TX\_2C21n  
IO, LVDS2C\_42P, DQ14 TX\_2C21p  
IO, LVDS2C\_43N, DQ15RX\_2C22n  
IO, LVDS2C\_43P, DQ15 RX\_2C22p  
IO, LVDS2C\_44N, DQ15 TX\_2C22n  
IO, LVDS2C\_44P, DQ15 TX\_2C22p  
IO, LVDS2C\_45N, DQ15 RX\_2C23n  
IO, LVDS2C\_45P, DQ15 RX\_2C23p  
IO, LVDS2C\_46N, DQSN15TX\_2C23n  
IO, LVDS2C\_46P, DQS15 TX\_2C23p  
IO, LVDS2C\_47N, DQ15 RX\_2C24n  
IO, LVDS2C\_47P, DQ15RX\_2C24p  
IO, LVDS2C\_48N, DQ15TX\_2C24n  
IO, LVDS2C\_48P, DQ15TX\_2C24p

BOT TOP

Bank 2C VCCIO = VCCIO\_FMC\_HAB (1.2 or 1.5V)

AGFB014R24B1E1V

RX\_2C1n IO, LVDS2C\_1N, DQ8  
RX\_2C1p IO, LVDS2C\_1P, DQ8  
TX\_2C1n IO, LVDS2C\_2N, DQ8  
TX\_2C1p IO, LVDS2C\_2P, DQ8  
RX\_2C2n IO, LVDS2C\_3N, DQ8  
RX\_2C2p IO, LVDS2C\_3P, DQ8  
TX\_2C2n IO, LVDS2C\_4N, DQSN8  
TX\_2C2p IO, LVDS2C\_4P, DQSN8  
RX\_2C3n IO, LVDS2C\_5N, DQ8  
RX\_2C3p IO, LVDS2C\_5P, DQ8  
TX\_2C3n IO, LVDS2C\_6N, DQ8  
TX\_2C3p IO, LVDS2C\_6P, DQ8  
RX\_2C4n IO, LVDS2C\_7N, DQ9  
RX\_2C4p IO, LVDS2C\_7P, DQ9  
TX\_2C4n IO, LVDS2C\_8N, DQ9  
TX\_2C4p IO, LVDS2C\_8P, DQ9  
RX\_2C5n IO, LVDS2C\_9N, DQ9  
RX\_2C5p IO, LVDS2C\_9P, DQ9  
TX\_2C5n IO, PLL\_2C\_T\_CLKOUT1N, LVDS2C\_10N, DQSN9  
TX\_2C5p IO, PLL\_2C\_T\_CLKOUT1P, PLL\_2C\_T\_CLKOUT1, PLL\_2C\_T\_FB1, LVDS2C\_10P, DQSN9  
RX\_2C6n IO, LVDS2C\_11N, DQ9  
RX\_2C6p IO, RZQ\_T\_2C, LVDS2C\_11P, DQ9  
TX\_2C6n IO, CLK\_T\_2C\_1N, LVDS2C\_12N, DQ9  
TX\_2C6p IO, CLK\_T\_2C\_1P, LVDS2C\_12P, DQ9  
RX\_2C7n IO, CLK\_T\_2C\_0N, LVDS2C\_13N, DQ10  
RX\_2C7p IO, CLK\_T\_2C\_0P, LVDS2C\_13P, DQ10  
TX\_2C7n IO, LVDS2C\_14N, DQ10  
TX\_2C7p IO, LVDS2C\_14P, DQ10  
RX\_2C8n IO, PLL\_2C\_T\_CLKOUT0N, LVDS2C\_15N, DQ10  
RX\_2C8p IO, PLL\_2C\_T\_CLKOUT0P, PLL\_2C\_T\_CLKOUT0, PLL\_2C\_T\_FB0, LVDS2C\_15P, DQ10  
TX\_2C8n IO, LVDS2C\_16N, DQSN10  
TX\_2C8p IO, LVDS2C\_16P, DQSN10  
RX\_2C9n IO, LVDS2C\_17N, DQ10  
RX\_2C9p IO, LVDS2C\_17P, DQ10  
TX\_2C9n IO, LVDS2C\_18N, DQ10  
TX\_2C9p IO, LVDS2C\_18P, DQ10  
RX\_2C10n IO, LVDS2C\_19N, DQ11  
RX\_2C10p IO, LVDS2C\_19P, DQ11  
TX\_2C10n IO, LVDS2C\_20N, DQ11  
TX\_2C10p IO, LVDS2C\_20P, DQ11  
RX\_2C11n IO, LVDS2C\_21N, DQ11  
RX\_2C11p IO, LVDS2C\_21P, DQ11  
TX\_2C11n IO, LVDS2C\_22N, DQSN11  
TX\_2C11p IO, LVDS2C\_22P, DQSN11  
RX\_2C12n IO, LVDS2C\_23N, DQ11  
RX\_2C12p IO, LVDS2C\_23P, DQ11  
TX\_2C12n IO, LVDS2C\_24N, DQ11  
TX\_2C12p IO, LVDS2C\_24P, DQ11

CT17 FMC HB n5  
CV17 FMC HB p5  
CR18 FMC HB n14  
CU18 FMC HB p14  
CT19 FMC HB n9  
CV19 FMC HB p9  
CR20 FMC HB n16  
CU20 FMC HB p16  
CT21 FMC HB n11  
CV21 FMC HB p11  
CR22 FMC HB n20  
CU22 FMC HB p20  
CY17 FMC HB n3  
DB17 FMC HB p3  
DA18 FMC HB n12  
DC18 FMC HB p12  
CY19  
DB19  
DA20 FMC HB n0  
DC20 FMC HB p0  
CY21 FMC HB n7  
DB21 FMC HB p7  
DA22 FMC CLK\_M2C\_n1  
DC22 FMC CLK\_M2C\_p1  
CR24 FMC HB n1  
CU24 FMC HB p1  
CT25 FMC HB n8  
CV25 FMC HB p8  
CR26 FMC HB n19  
CU26 FMC HB p19  
CT27 FMC HB n17  
CV27 FMC HB p17  
CR28 FMC HB n21  
CU28 FMC HB p21  
CT29 FMC HB n10  
CV29 FMC HB p10  
DA24 FMC HB n13  
DC24 FMC HB p13  
CY25 FMC HB n6  
DB25 FMC HB p6  
DA26 FMC HB n15  
DC26 FMC HB p15  
CY27 FMC HB n4  
DB27 FMC HB p4  
DA28 FMC HB n18  
DC28 FMC HB p18  
CY29 FMC HB n2  
DB29 FMC HB p2

FMCP\_HA\_n7 CF43  
FMCP\_HA\_p7 CH43  
FMCP\_HA\_n8 CE42  
FMCP\_HA\_p8 CG42  
FMCP\_HA\_n9 CF41  
FMCP\_HA\_p9 CH41  
FMCP\_HA\_n2 CE40  
FMCP\_HA\_p2 CG40  
FMCP\_HA\_n5 CF39  
FMCP\_HA\_p5 CH39  
FMCP\_HA\_n10 CE38  
FMCP\_HA\_p10 CG38  
FMCP\_HA\_n13 CK43  
FMCP\_HA\_p13 CM43  
FMCP\_HA\_n6 CL42  
FMCP\_HA\_p6 CN42  
FMCP\_HA\_n11 CK41  
FMCP\_HA\_p11 CM41  
FMCP\_HA\_n0 CL40  
FMCP\_HA\_p0 CN40  
FMCP\_HA\_n18 CK39  
FMCP\_HA\_p18 CM39  
FMCP\_HA\_n12 CL38  
FMCP\_HA\_p12 CN38  
FMCP\_HA\_n1 CE36  
FMCP\_HA\_p1 CG36  
FMCP\_HA\_n4 CF35  
FMCP\_HA\_p4 CH35  
FMCP\_HA\_n3 CE34  
FMCP\_HA\_p3 CG34  
FMCP\_HA\_n23 CF33  
FMCP\_HA\_p23 CH33  
FMCP\_HA\_n20 CE32  
FMCP\_HA\_p20 CG32  
FMCP\_HA\_n21 CF31  
FMCP\_HA\_p21 CH31  
FMCP\_HA\_n14 CL36  
FMCP\_HA\_p14 CN36  
FMCP\_HA\_n15 CK35  
FMCP\_HA\_p15 CM35  
FMCP\_HA\_n18 CL34  
FMCP\_HA\_p18 CN34  
FMCP\_HA\_n19 CK33  
FMCP\_HA\_p19 CM33  
FMCP\_HA\_n22 CL32  
FMCP\_HA\_p22 CN32  
FMCP\_HA\_n17 CK31  
FMCP\_HA\_p17 CM31

U15D

IO, LVDS2B\_25N, DQ20RX\_2B13n  
IO, LVDS2B\_25P, DQ20RX\_2B13p  
IO, LVDS2B\_26N, DQ20TX\_2B13n  
IO, LVDS2B\_26P, DQ20TX\_2B13p  
IO, LVDS2B\_27N, DQ20RX\_2B14n  
IO, LVDS2B\_27P, DQ20RX\_2B14p  
IO, LVDS2B\_28N, DQSN20TX\_2B14n  
IO, LVDS2B\_28P, DQSN20 TX\_2B14p  
IO, LVDS2B\_29N, DQ20RX\_2B15n  
IO, LVDS2B\_29P, DQ20RX\_2B15p  
IO, LVDS2B\_30N, DQ20TX\_2B15n  
IO, LVDS2B\_30P, DQ20TX\_2B15p  
IO, LVDS2B\_31N, DQ21RX\_2B16n  
IO, LVDS2B\_31P, DQ21RX\_2B16p  
IO, LVDS2B\_32N, DQ21TX\_2B16n  
IO, LVDS2B\_32P, DQ21TX\_2B16p  
IO, LVDS2B\_33N, DQ21RX\_2B17n  
IO, LVDS2B\_33P, DQ21RX\_2B17p  
IO, PLL\_2B\_B\_CLKOUT1N, LVDS2B\_34N, DQSN2TX\_2B17n  
IO, PLL\_2B\_B\_CLKOUT1P, PLL\_2B\_B\_CLKOUT1, PLL\_2B\_B\_FB1, LVDS2B\_34P, DQSN2TX\_2B17p  
IO, LVDS2B\_35N, DQ21RX\_2B18n  
IO, RZQ\_B\_2B, LVDS2B\_35P, DQ21RX\_2B18p  
IO, CLK\_B\_2B\_1N, LVDS2B\_36N, DQ21TX\_2B18n  
IO, CLK\_B\_2B\_1P, LVDS2B\_36P, DQ21TX\_2B18p  
IO, CLK\_B\_2B\_0N, LVDS2B\_37N, DQ22RX\_2B19n  
IO, CLK\_B\_2B\_0P, LVDS2B\_37P, DQ22RX\_2B19p  
IO, LVDS2B\_38N, DQ22TX\_2B19n  
IO, LVDS2B\_38P, DQ22TX\_2B19p  
IO, PLL\_2B\_B\_CLKOUT0N, LVDS2B\_39N, DQ22RX\_2B20n  
IO, PLL\_2B\_B\_CLKOUT0P, PLL\_2B\_B\_CLKOUT0, PLL\_2B\_B\_FB0, LVDS2B\_39P, DQ22RX\_2B20p  
IO, LVDS2B\_40N, DQSN22TX\_2B20n  
IO, LVDS2B\_40P, DQSN22 TX\_2B20p  
IO, LVDS2B\_41N, DQ22 RX\_2B21n  
IO, LVDS2B\_41P, DQ22 RX\_2B21p  
IO, LVDS2B\_42N, DQ22TX\_2B21n  
IO, LVDS2B\_42P, DQ22TX\_2B21p  
IO, LVDS2B\_43N, DQ23RX\_2B22n  
IO, LVDS2B\_43P, DQ23RX\_2B22p  
IO, LVDS2B\_44N, DQ23TX\_2B22n  
IO, LVDS2B\_44P, DQ23TX\_2B22p  
IO, LVDS2B\_45N, DQ23 RX\_2B23n  
IO, LVDS2B\_45P, DQ23 RX\_2B23p  
IO, LVDS2B\_46N, DQSN23TX\_2B23n  
IO, LVDS2B\_46P, DQSN23 TX\_2B23p  
IO, LVDS2B\_47N, DQ23RX\_2B24n  
IO, LVDS2B\_47P, DQ23RX\_2B24p  
IO, LVDS2B\_48N, DQ23TX\_2B24n  
IO, LVDS2B\_48P, DQ23TX\_2B24p

BOT

TOP


Bank 2B VCCIO = 1.2V

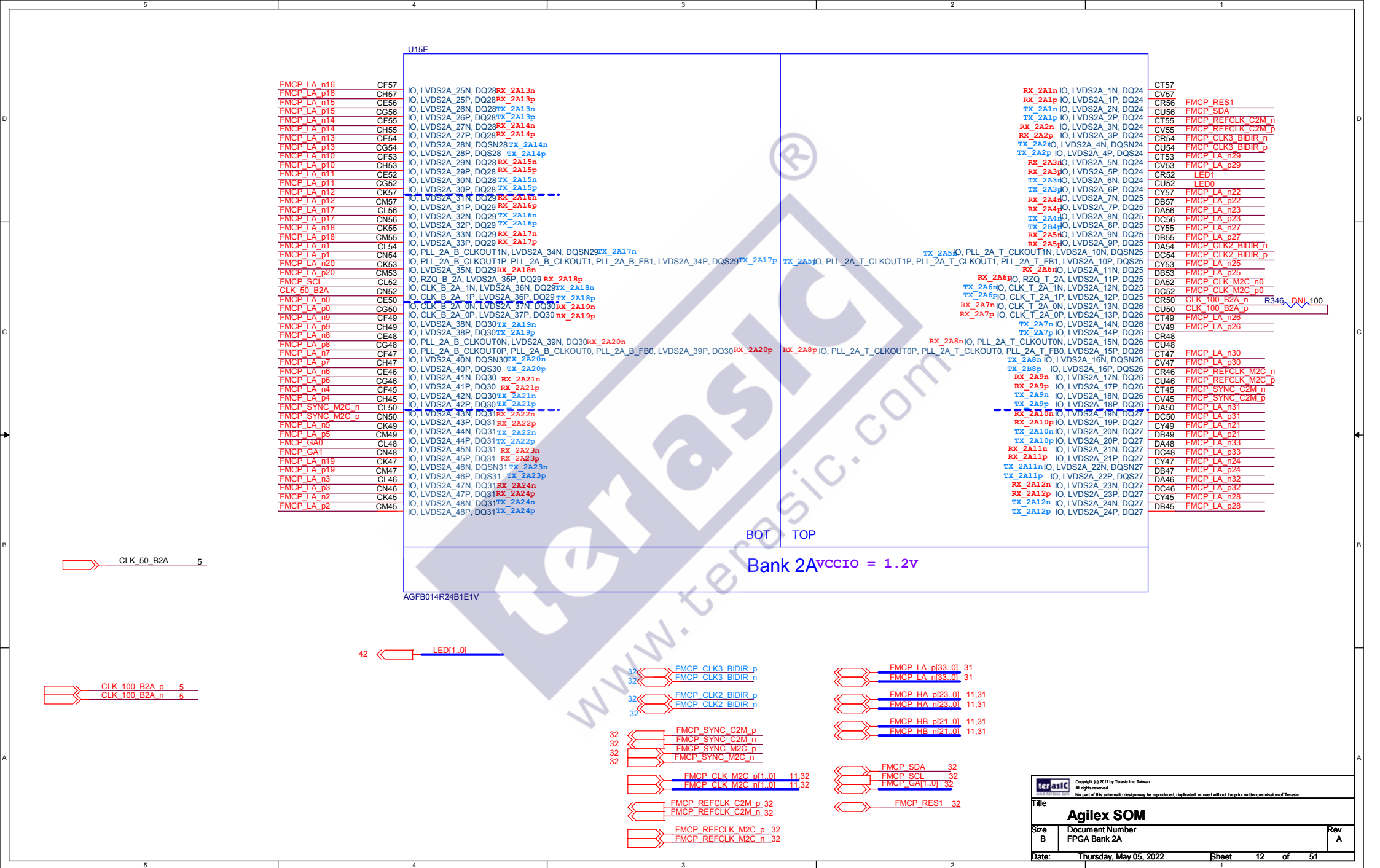
AGFB014R24B1E1V

FMCP\_CLK\_M2C\_n11\_01 12\_32  
FMCP\_CLK\_M2C\_n11\_01 12\_32  
FMCP\_HA\_n23\_01 31  
FMCP\_HA\_n23\_01 31  
FMCP\_HB\_n21\_01 31  
FMCP\_HB\_n21\_01 31

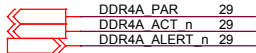
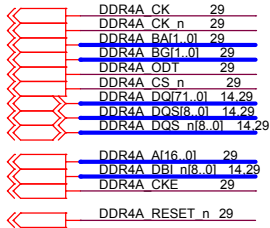
RX\_2B1n IO, LVDS2B\_1N, DQ16  
RX\_2B1p IO, LVDS2B\_1P, DQ16  
TX\_2B1n IO, LVDS2B\_2N, DQ16  
TX\_2B1p IO, LVDS2B\_2P, DQ16  
RX\_2B2n IO, LVDS2B\_3N, DQ16  
RX\_2B2p IO, LVDS2B\_3P, DQ16  
TX\_2B2n IO, LVDS2B\_4N, DQSN16  
TX\_2B2p IO, LVDS2B\_4P, DQSN16  
RX\_2B3n IO, LVDS2B\_5N, DQ16  
RX\_2B3p IO, LVDS2B\_5P, DQ16  
TX\_2B3n IO, LVDS2B\_6N, DQ16  
TX\_2B3p IO, LVDS2B\_6P, DQ16  
RX\_2B4n IO, LVDS2B\_7N, DQ17  
RX\_2B4p IO, LVDS2B\_7P, DQ17  
TX\_2B4n IO, LVDS2B\_8N, DQ17  
TX\_2B4p IO, LVDS2B\_8P, DQ17  
RX\_2B5n IO, LVDS2B\_9N, DQ17  
RX\_2B5p IO, LVDS2B\_9P, DQ17  
TX\_2B5n IO, PLL\_2B\_T\_CLKOUT1N, LVDS2B\_10N, DQSN17  
TX\_2B5p IO, PLL\_2B\_T\_CLKOUT1P, PLL\_2B\_T\_CLKOUT1, PLL\_2B\_T\_FB1, LVDS2B\_10P, DQSN17  
RX\_2B6n IO, RZQ\_T\_2B, LVDS2B\_11P, DQ17  
RX\_2B6p IO, RZQ\_T\_2B, LVDS2B\_11P, DQ17  
TX\_2B6n IO, CLK\_T\_2B\_1N, LVDS2B\_12N, DQ17  
TX\_2B6p IO, CLK\_T\_2B\_1P, LVDS2B\_12P, DQ17  
RX\_2B7n IO, CLK\_T\_2B\_0N, LVDS2B\_13N, DQ18  
RX\_2B7p IO, CLK\_T\_2B\_0P, LVDS2B\_13P, DQ18  
TX\_2B7n IO, LVDS2B\_14N, DQ18  
TX\_2B7p IO, LVDS2B\_14P, DQ18  
RX\_2B8n IO, PLL\_2B\_T\_CLKOUT0N, LVDS2B\_15N, DQ18  
RX\_2B8p IO, PLL\_2B\_T\_CLKOUT0P, PLL\_2B\_T\_CLKOUT0, PLL\_2B\_T\_FB0, LVDS2B\_15P, DQ18  
TX\_2B8n IO, LVDS2B\_16N, DQSN18  
TX\_2B8p IO, LVDS2B\_16P, DQSN18  
RX\_2B9n IO, LVDS2B\_17N, DQ18  
RX\_2B9p IO, LVDS2B\_17P, DQ18  
TX\_2B9n IO, LVDS2B\_18N, DQ18  
TX\_2B9p IO, LVDS2B\_18P, DQ18  
RX\_2B10n IO, LVDS2B\_19N, DQ19  
RX\_2B10p IO, LVDS2B\_19P, DQ19  
TX\_2B10n IO, LVDS2B\_20N, DQ19  
TX\_2B10p IO, LVDS2B\_20P, DQ19  
RX\_2B11n IO, LVDS2B\_21N, DQ19  
RX\_2B11p IO, LVDS2B\_21P, DQ19  
TX\_2B11n IO, LVDS2B\_22N, DQSN19  
TX\_2B11p IO, LVDS2B\_22P, DQSN19  
RX\_2B12n IO, LVDS2B\_23N, DQ19  
RX\_2B12p IO, LVDS2B\_23P, DQ19  
TX\_2B12n IO, LVDS2B\_24N, DQ19  
TX\_2B12p IO, LVDS2B\_24P, DQ19

CT43 FMCP\_HB\_n9  
CV43 FMCP\_HB\_p9  
CR42 FMCP\_HB\_n20  
CU42 FMCP\_HB\_p20  
CT41 FMCP\_HB\_n5  
CV41 FMCP\_HB\_p5  
CR40 FMCP\_HB\_n16  
CU40 FMCP\_HB\_p16  
CT39 FMCP\_HB\_n3  
CV39 FMCP\_HB\_p3  
CR38 FMCP\_HB\_n12  
CU38 FMCP\_HB\_p12  
CY43 FMCP\_HB\_n7  
DB43 FMCP\_HB\_p7  
DA42 FMCP\_HB\_n2  
DC42 FMCP\_HB\_p2  
CY41 FMCP\_HB\_n13  
DB41 FMCP\_HB\_p13  
DA40 FMCP\_HB\_n0  
DC40 FMCP\_HB\_p0  
CV39 FMCP\_HB\_n11  
DB39 FMCP\_HB\_p11  
DA38 FMCP\_CLK\_M2C\_n1  
DC38 FMCP\_CLK\_M2C\_p1  
CR36 FMCP\_HB\_n1  
CU36 FMCP\_HB\_p1  
CT35 FMCP\_HB\_n8  
CV35 FMCP\_HB\_p8  
CR34  
CU34  
CT33 FMCP\_HB\_n6  
CV33 FMCP\_HB\_p6  
CR32 FMCP\_HB\_n18  
CU32 FMCP\_HB\_p18  
CT31 FMCP\_HB\_n17  
CV31 FMCP\_HB\_p17  
DA36 FMCP\_HB\_n19  
DC36 FMCP\_HB\_p19  
CY35 FMCP\_HB\_n14  
DB35 FMCP\_HB\_p14  
DA34 FMCP\_HB\_n15  
DC34 FMCP\_HB\_p15  
CY33 FMCP\_HB\_n4  
DB33 FMCP\_HB\_p4  
DA32 FMCP\_HB\_n21  
DC32 FMCP\_HB\_p21  
CY31 FMCP\_HB\_n10  
DB31 FMCP\_HB\_p10

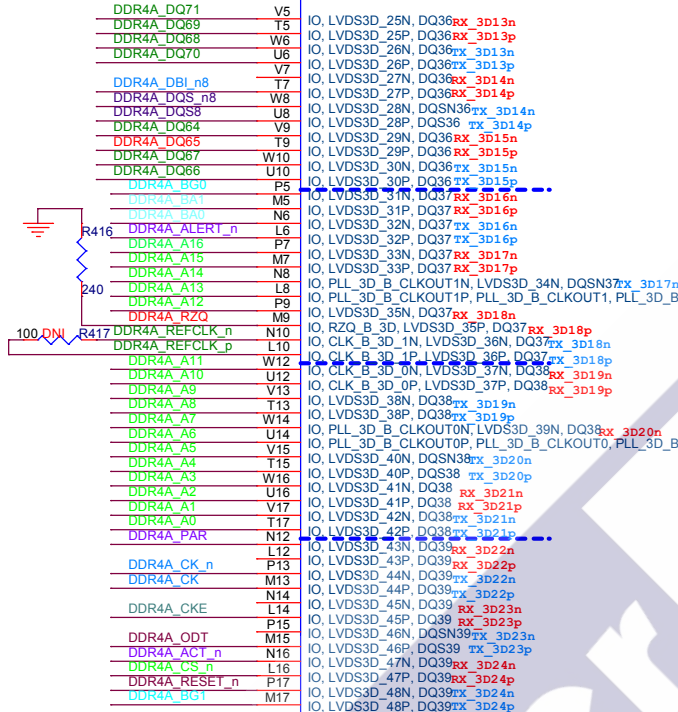
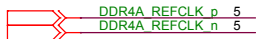
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Title <b>Agilex SOM</b>		
Size B	Document Number FPGA Bank 2B	Rev A
Date:	Friday, May 27, 2022	Sheet 11 of 51



## DDR4 SO-DIMM A



RAS\_n is a multiplexed function with A16  
CAS\_n is a multiplexed function with A15  
WE\_n is a multiplexed function with A14

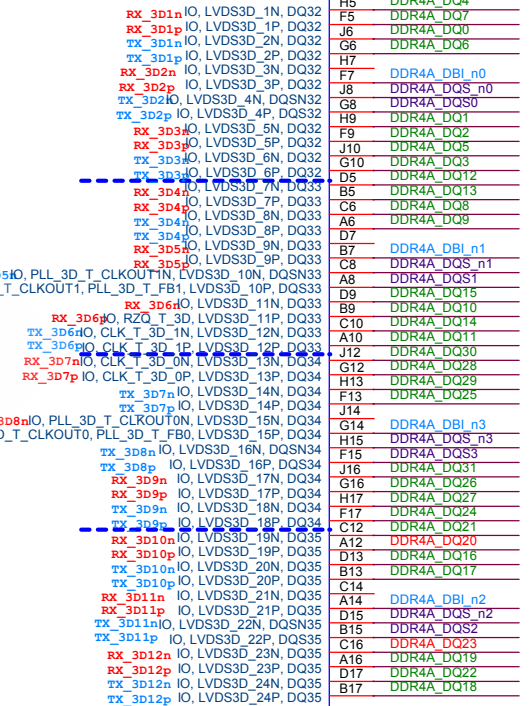


U15F

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BOT TOP

Bank 3D VCCIO = 1.2V





DDR4A CK	13.29
DDR4A CK n	13.29
DDR4A BA[1..0]	13.29
DDR4A BG[1..0]	13.29
DDR4A ODT	13.29
DDR4A CS n	13.29
DDR4A DQ[71..0]	13.29
DDR4A DQS[8..0]	13.29
DDR4A DQS n[8..0]	13.29
DDR4A A[16..0]	13.29
DDR4A DBI n[8..0]	13.29
DDR4A RESET	13.29
DDR4A CESE n	13.29

DDR4A PAR	13,29
DDR4A ACT n	13,29
DDR4A ALERT n	13,29

DDR4A EVENT	n	8
DDR4A SDA		8
DDR4A SCL		8

RAS\_n is a multiplexed function with A16  
CAS\_n is a multiplexed function with A15  
WE\_n is a multiplexed function with A14

CLK 50 B3C 5

AG UART RX	6
AG UART TX	6
AG UART CTS	6
AG UART RTS	6

DDR4B\_SDA 8

DDR4A_DQ41	V19	IO, LVDS3C_25N, DQ44RX_3C13n
DDR4A_DQ45	T19	IO, LVDS3C_25P, DQ44RX_3C13p
DDR4A_DQ43	W20	IO, LVDS3C_26N, DQ44RX_3C13n
DDR4A_DQ44	U20	IO, LVDS3C_26P, DQ44TX_3C13p
	V21	IO, LVDS3C_27N, DQ44RX_3C14n
DDR4A_DBI_n5	T21	IO, LVDS3C_27P, DQ44RX_3C14p
DDR4A_DQS_n5	W22	IO, LVDS3C_28N, DQSN44RX_3C14n
DDR4A_DQS5	U22	IO, LVDS3C_28P, DQSN44TX_3C14p
DDR4A_DQ46	T23	IO, LVDS3C_29N, DQ44RX_3C15n
DDR4A_DQ47	V23	IO, LVDS3C_29P, DQ44RX_3C15p
DDR4A_DQ47	W24	IO, LVDS3C_30N, DQ44TX_3C15n
DDR4A_DQ42	U24	IO, LVDS3C_30P, DQ44TX_3C15p
DDR4A_DQ35	P19	IO, LVDS3C_31N, DQ45RX_3C16n
DDR4A_DQ38	M19	IO, LVDS3C_31P, DQ45RX_3C16p
DDR4A_DQ32	N20	IO, LVDS3C_32N, DQ45TX_3C16n
DDR4A_DQ36	L20	IO, LVDS3C_32P, DQ45TX_3C16p
	P21	IO, LVDS3C_33N, DQ45RX_3C17n
DDR4A_DBI_n4	M21	IO, LVDS3C_33P, DQ45RX_3C17p
DDR4A_DQS_n4	N22	IO, PLL_3C_B_CLKOUT1N, LVDS3C_34N, DQSN45X_3C17n
DDR4A_DQS4	L22	IO, PLL_3C_B_CLKOUT1P, PLL_3C_B_CLKOUT1, PLL_3C_B
DDR4A_DQ38	P23	IO, LVDS3C_35N, DQ45RX_3C18n
DDR4A_DQ33	M23	IO, RZQ_B_3C, LVDS3C_35P, DQ45RX_3C18p
DDR4A_DQ34	N24	IO, CLK_B_3C_1N, LVDS3C_36N, DQ45TX_3C18n
DDR4A_DQ37	L24	IO, CLK_B_3C_1P, LVDS3C_36P, DQ45TX_3C18p
DDR4A_DQ50	W26	IO, CLK_B_3C_1N, LVDS3C_37N, DQ46RX_3C19n
DDR4A_DQ55	U26	IO, CLK_B_3C_1P, LVDS3C_37P, DQ46RX_3C19p
DDR4A_DQ54	V27	IO, LVDS3C_38N, DQ46RX_3C19n
DDR4A_DQ52	T27	IO, LVDS3C_38P, DQ46TX_3C19p
	W28	IO, PLL_3C_B_CLKOUTN, LVDS3C_39N, DQ48RX_3C20n
DDR4A_DQBI_n6	U28	IO, PLL_3C_B_CLKOUT1P, PLL_3C_B_CLKOUT0, PLL_3C_B
DDR4A_DQS_n6	V29	IO, LVDS3C_40N, DQSN48TX_3C20n
DDR4A_DQS6	T29	IO, LVDS3C_40P, DQSN48TX_3C20p
DDR4A_DQ48	W30	IO, LVDS3C_41N, DQ46RX_3C21n
DDR4A_DQ51	V31	IO, LVDS3C_41P, DQ46RX_3C21p
DDR4A_DQ53	T31	IO, LVDS3C_42N, DQ46TX_3C21n
DDR4A_DQ58	N26	IO, LVDS3C_42P, DQ46TX_3C21p
DDR4A_DQ57	L26	IO, LVDS3C_43N, DQ47RX_3C22n
DDR4A_DQ59	P27	IO, LVDS3C_43P, DQ47RX_3C22p
DDR4A_DQ80	M27	IO, LVDS3C_44N, DQ47TX_3C22n
	N28	IO, LVDS3C_44P, DQ47TX_3C22p
DDR4A_DBI_n7	L28	IO, LVDS3C_45N, DQ47RX_3C23n
DDR4A_DQS_n7	P29	IO, LVDS3C_45P, DQ47RX_3C23p
DDR4A_DQ57	M29	IO, LVDS3C_46N, DQSN47TX_3C23n
DDR4A_DQ62	N30	IO, LVDS3C_46P, DQSN47TX_3C23p
DDR4A_DQ56	L30	IO, LVDS3C_47N, DQ47TX_3C24n
DDR4A_DQ63	P31	IO, LVDS3C_47P, DQ47RX_3C24p
DDR4A_DQ61	M31	IO, LVDS3C_48N, DQ47TX_3C24n
		IO, LVDS3C_48P, DQ47TX_3C24p


[BOT](#) | [TOP](#)

Bank 3C  $V_{CCIO} = 1.2V$

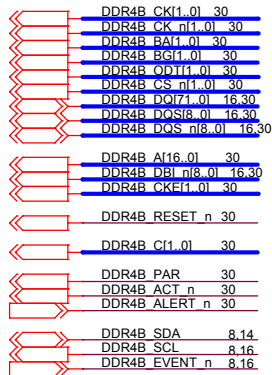
AGFB014R24B1E1V

QSPI28	MOD_SEL_n	35
QSPI28	RST_n	35
QSPI28	SCL	35
QSPI28	SDA	35
QSPI28	LP_MODE	35
QSPI28	INTERRUPT_n	35
QSPI28	MOD_PRS_n	35

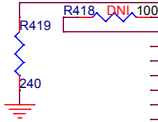
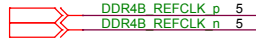
	Si5340A_I2C_SDA	4
	Si5340A_I2C_SCL	4
	Si5340A_RST_n	4
	Si5340A_OE_n	4
	Si5340A_LOL	4
	Si5340A_LOS_XAXB	4

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Title			
	<b>Agilex SOM</b>		
Size	Document Number	B	Rev
	FPGA Bank 3C		A
Date:	Thursday, May 05, 2022	Sheet	14 of 51

## DDR4 SO-DIMM B



RAS\_n is a multiplexed function with A16  
CAS\_n is a multiplexed function with A15  
WE\_n is a multiplexed function with A14



DDR4B_CK_n1	V45
DDR4B_CK1	T45
	W44
	U44
	V43
	T43
	W42
	U42
	V41
	T41
DDR4B_C1	W40
DDR4B_C0	U40
DDR4B_B00	P45
DDR4B_BA1	M45
DDR4B_BA0	N44
DDR4B_ALERT_n	L44
DDR4B_A16	P43
DDR4B_A15	M43
DDR4B_A14	N42
DDR4B_A13	L42
DDR4B_A12	P41
DDR4B_RZ0	M41
DDR4B_REFCLK_n	N40
DDR4B_REFCLK_p	L40
DDR4B_A11	W38
DDR4B_A10	U38
DDR4B_A9	V37
DDR4B_A8	T37
DDR4B_A7	W36
DDR4B_A6	U36
DDR4B_A5	V35
DDR4B_A4	T35
DDR4B_A3	W34
DDR4B_A2	U34
DDR4B_A1	V33
DDR4B_A0	T33
DDR4B_PAR	N38
DDR4B_CS_n1	L38
DDR4B_CK_n0	P37
DDR4B_CK0	M37
DDR4B_CKE1	N36
DDR4B_CKE0	L36
DDR4B_ODT1	P35
DDR4B_ODT0	M35
DDR4B_ACT_n	N34
DDR4B_CS_n0	L34
DDR4B_RESET_n	P33
DDR4B_BG1	M33

U15H

AGFB014R24B1E1V

[BOT](#)
[TOP](#)

[TOP](#)

Bank 3B  $V_{CCIO} = 1.2V$

```

RX 3b1n IO, LVDS3B 1N, DQ48
RX 3b1p IO, LVDS3B 1P, DQ48
TX 3b1n IO, LVDS3B 2N, DQ48
TX 3b1p IO, LVDS3B 2P, DQ48
RX 3b2n IO, LVDS3B 3N, DQ48
RX 3b2p IO, LVDS3B 3P, DQ48
TX 3b2n IO, LVDS3B 4N, DQ54
TX 3b2p IO, LVDS3B 4P, DQ54
RX 3b3n IO, LVDS3B 5N, DQ48
RX 3b3p IO, LVDS3B 5P, DQ48
TX 3b3n IO, LVDS3B 6N, DQ48
TX 3b3p IO, LVDS3B 6P, DQ48
RX 3b4n IO, LVDS3B 7N, DQ49
RX 2b4n IO, LVDS3B 7P, DQ49
TX 3b4n IO, LVDS3B 8N, DQ49
TX 3b4p IO, LVDS3B 8P, DQ49
RX 3b5n IO, LVDS3B 9N, DQ49
RX 3b5p IO, LVDS3B 9P, DQ49
CLKOUT1N, LVDS3B 10N, DQ54N
CLKOUT1P, LVDS3B 10P, DQ54N
RX 3b6n IO, LVDS3B 11N, DQ49
HO, RZQ, TX FB0, LVDS3B 11P, DQ49
CLK T 3b1N, LVDS3B 12N, DQ49
CLK T 3b1P, LVDS3B 12P, DQ49
CLK T 3b0N, LVDS3B 13N, DQ50
CLK T 3b0P, LVDS3B 13P, DQ50
TX 3b7n IO, LVDS3B 14N, DQ50
TX 3b7p IO, LVDS3B 14P, DQ50
TX CLKOUT0N, LVDS3B 15N, DQ50
PLT 3b1 T FB0, LVDS3B 15P, DQ50
RX 3b8n IO, LVDS3B 16N, DQ50
RX 3b8p IO, LVDS3B 16P, DQ50
RX 3b9n IO, LVDS3B 17N, DQ50
RX 3b9p IO, LVDS3B 17P, DQ50
TX 3b9n IO, LVDS3B 18N, DQ50
TX 3b9p IO, LVDS3B 18P, DQ50
RX 3b10n IO, LVDS3B 19N, DQ51
RX 3b10p IO, LVDS3B 19P, DQ51
TX 3b10n IO, LVDS3B 20N, DQ51
TX 3b10p IO, LVDS3B 20P, DQ51
RX 3b11n IO, LVDS3B 21N, DQ51
RX 3b11p IO, LVDS3B 21P, DQ51
TX 3b11n IO, LVDS3B 22N, DQ51
TX 3b11p IO, LVDS3B 22P, DQ51
RX 3b12n IO, LVDS3B 23N, DQ51
RX 3b12p IO, LVDS3B 23P, DQ51
TX 3b12n IO, LVDS3B 24N, DQ51
TX 3b12p IO, LVDS3B 24P, DQ51

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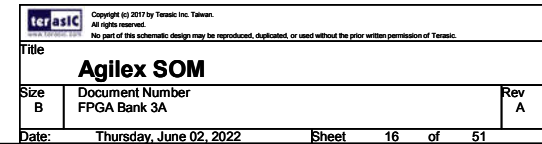
F45	DDR4B D09
H45	DDR4B D013
J44	DDR4B D015
G44	DDR4B D010
H43	
F43	DDR4B DBI_n1
J42	DDR4B D0S_n1
G42	DDR4B D08
F41	DDR4B D08
F41	DDR4B D014
J40	DDR4B D012
G40	DDR4B D011
D45	DDR4B D018
B45	DDR4B D022
C44	DDR4B D020
A44	DDR4B D019
D43	
B43	DDR4B DBI_n2
C42	DDR4B D0S_n2
C42	DDR4B D0S2
D41	DDR4B D023
B41	DDR4B D016
C40	DDR4B D021
A40	DDR4B D017
J38	DDR4B D05
G38	DDR4B D02
H37	DDR4B D03
F37	DDR4B D06
J36	
G36	DDR4B DBI_n0
C36	DDR4B D0S_n0
F35	DDR4B D0S0
J34	DDR4B D07
G34	DDR4B D07
H33	DDR4B D04
F33	DDR4B D00
C38	DDR4B D031
A38	DDR4B D024
D37	DDR4B D028
B37	DDR4B D027
C36	
D35	DDR4B DBI_n3
D35	DDR4B D0S_n3
B35	DDR4B D0S3
C34	DDR4B D025
A34	DDR4B D030
D33	DDR4B D026
B33	DDR4B D029

DDR4B CK1[0]	15.30
DDR4B CK n[1:0]	15.30
DDR4B BA[1:0]	15.30
DDR4B BG[1:0]	15.30
DDR4B OD[1:0]	15.30
DDR4B CS n[1:0]	15.30
DDR4B OD[7:1]	15.30
DDR4B DQSIB n[0]	15.30
DDR4B DQS n[6:0]	15.30
DDR4B A[16:0]	15.30
DDR4B DBI n[6:0]	15.30
DDR4B CKE[1:0]	15.30
DDR4B RESET n	15.30
DDR4B C1[0]	15.30
DDR4B PAR	15.30
DDR4B ACT n	15.30
DDR4B ALERT n	15.30

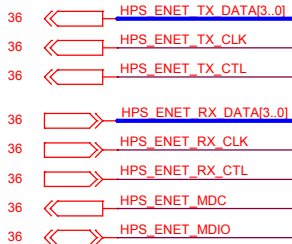
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INFO SPI CS <sub>n</sub>	6
INFO SPI MOSI	6
INFO SPI MISO	6

[AGFB014R24B1E1V](#)

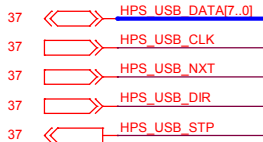
Bank 3A  $V_{CCIO} = 1.2V$



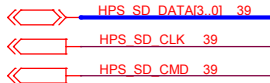
### Ethernet PHY Interface (RGMII)



### UBS PHY Interface (ULPI)



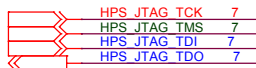
### SD Card Interface



### HPS 25MHz Clock



### HPS JTAG Interface



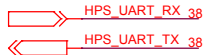
### HPS User Button



### HPS User LED



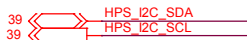
### UART Interface



### HPS GPIO



### HPS I2C Interface (RTC)



## FPGA Bank - HPS

U15J

HPS\_USB\_CLK AH5  
HPS\_USB\_STP AD1  
HPS\_USB\_DIR AG6  
HPS\_USB\_DATA0 AB1  
HPS\_USB\_DATA1 AG4  
HPS\_USB\_NXT AD3  
HPS\_USB\_DATA2 AF5  
HPS\_USB\_DATA3 AC2  
HPS\_USB\_DATA4 AF1  
HPS\_USB\_DATA5 AB3  
HPS\_USB\_DATA6 AF3  
HPS\_USB\_DATA7 AA2  
HPS\_ENET\_TX\_CLK AC4  
HPS\_ENET\_RX\_CTL V1  
HPS\_ENET\_RX\_CLK AA4  
HPS\_ENET\_TX\_CTL T1  
HPS\_ENET\_TX\_DATA0 AD5  
HPS\_ENET\_TX\_DATA1 P1  
HPS\_ENET\_RX\_DATA0 AF7  
HPS\_ENET\_RX\_DATA1 M1  
HPS\_ENET\_TX\_DATA2 AF9  
HPS\_ENET\_TX\_DATA3 W2  
HPS\_ENET\_RX\_DATA2 AB5  
HPS\_ENET\_RX\_DATA3 U2  
HPS\_LED AC6  
HPS\_KEY H1  
HPS\_UART\_TX AA6  
HPS\_UART\_RX F1  
HPS\_GPIO4 AD7  
HPS\_OSC\_CLK N2  
HPS\_I2C\_SDA AB7  
HPS\_I2C\_SCL L2  
HPS\_JTAG\_TCK AC8  
HPS\_JTAG\_TMS J2  
HPS\_JTAG\_TDI AA8  
HPS\_JTAG\_TDO G2  
HPS\_SD\_DATA0 AD9  
HPS\_SD\_CMD V3  
HPS\_SD\_CLK AB9  
HPS\_SD\_DATA1 T3  
HPS\_SD\_DATA2 AC10  
HPS\_SD\_DATA3 P3  
HPS\_GPIO0 AD11  
HPS\_GPIO1 M3  
HPS\_GPIO2 AC12  
HPS\_GPIO3 H3  
HPS\_ENET\_MDIO AD13  
HPS\_ENET\_MDC F3

AH19  
AJ20

HPS\_IOA\_1, GPIO0\_IO0, SPIM0\_SS1\_N, SPIS0\_CLK, UART0\_CTS\_N, NAND\_ADQ0, USB0\_CLK, SDMMC\_CCLK  
HPS\_IOA\_2, GPIO0\_IO1, SPIM1\_SS1\_N, SPIS0\_MOSI, UART0\_RTS\_N, NAND\_ADQ1, USB0\_STP, SDMMC\_CMD  
HPS\_IOA\_3, GPIO0\_IO2, SPIS0\_SS0\_N, UART0\_TX, I2C1\_SDA, NAND\_WE\_N, USB0\_DIR, SDMMC\_DATA0  
HPS\_IOA\_4, GPIO0\_IO3, SPIS0\_MISO, UART0\_RX, I2C1\_SCL, NAND\_RE\_N, USB0\_DATA0, SDMMC\_DATA1  
HPS\_IOA\_5, GPIO0\_IO4, SPIM0\_CLK, UART1\_CTS\_N, I2C0\_SDA, NAND\_WP\_N, USB0\_DATA1, SDMMC\_DATA2  
HPS\_IOA\_6, GPIO0\_IO5, SPIM0\_MOSI, UART1\_RTS\_N, I2C0\_SCL, NAND\_ADQ2, USB0\_NXT, SDMMC\_DATA3  
HPS\_IOA\_7, GPIO0\_IO6, SPIM0\_MISO, MDIO2\_MDIO, UART1\_TX, I2C\_EMAC2\_SDA, NAND\_ADQ3, USB0\_DATA2, SDMMC\_DATA4  
HPS\_IOA\_8, GPIO0\_IO7, SPIM0\_SS0\_N, MDIO2\_MDC, UART1\_RX, I2C\_EMAC2\_SCL, NAND\_CLE, USB0\_DATA3, SDMMC\_DATA5  
HPS\_IOA\_9, GPIO0\_IO8, SPIM1\_CLK, SPIS1\_CLK, MDIO1\_MDIO, I2C\_EMAC1\_SDA, NAND\_ADQ4, USB0\_DATA4, SDMMC\_DATA6  
HPS\_IOA\_10, GPIO0\_IO9, SPIM1\_MOSI, SPIS1\_MOSI, MDIO1\_MDC, I2C\_EMAC1\_SCL, NAND\_ADQ5, USB0\_DATA5, SDMMC\_DATA7  
HPS\_IOA\_11, GPIO0\_IO10, SPIM1\_MISO, SPIS1\_SS0\_N, MDIO0\_MDIO, I2C\_EMAC0\_SDA, NAND\_ADQ6, USB0\_DATA6  
HPS\_IOA\_12, GPIO0\_IO11, SPIM1\_SS0\_N, SPIS1\_MISO, MDIO0\_MDC, I2C\_EMAC0\_SCL, NAND\_ADQ7, USB0\_DATA7  
HPS\_IOA\_13, GPIO0\_IO12, NAND\_ALE, USB1\_CLK, EMAC0\_TX\_CLK  
HPS\_IOA\_14, GPIO0\_IO13, NAND\_RB, USB1\_STP, EMAC0\_TX\_CTL  
HPS\_IOA\_15, GPIO0\_IO14, NAND\_CE\_N, USB1\_DIR, EMAC0\_RX\_CLK  
HPS\_IOA\_16, GPIO0\_IO15, USB1\_DATA0, EMAC0\_RX\_CTL  
HPS\_IOA\_17, GPIO0\_IO16, NAND\_ADQ8, USB1\_DATA1, EMAC0\_TXD0  
HPS\_IOA\_18, GPIO0\_IO17, NAND\_ADQ9, USB1\_NXT, EMAC0\_TXD1  
HPS\_IOA\_19, GPIO0\_IO18, NAND\_ADQ10, USB1\_DATA2, EMAC0\_RXD0  
HPS\_IOA\_20, GPIO0\_IO19, SPIM1\_SS1\_N, NAND\_ADQ11, USB1\_DATA3, EMAC0\_RXD1  
HPS\_IOA\_21, GPIO0\_IO20, SPIM1\_CLK, SPIS0\_CLK, UART0\_CTS\_N, I2C1\_SDA, NAND\_ADQ12, USB1\_DATA4, EMAC0\_TXD2  
HPS\_IOA\_22, GPIO0\_IO21, SPIM1\_MOSI, SPIS0\_MOSI, UART0\_RTS\_N, I2C1\_SCL, NAND\_ADQ13, USB1\_DATA5, EMAC0\_TXD3  
HPS\_IOA\_23, GPIO0\_IO22, SPIM1\_MISO, SPIS0\_SS0\_N, UART0\_TX, I2C0\_SDA, NAND\_ADQ14, USB1\_DATA6, EMAC0\_RXD2  
HPS\_IOA\_24, GPIO0\_IO23, SPIM1\_SS0\_N, SPIS0\_MISO, UART0\_RX, I2C0\_SCL, NAND\_ADQ15, USB1\_DATA7, EMAC0\_RXD3  
HPS\_IOB\_1, GPIO1\_IO0, SPIM1\_CLK, UART0\_CTS\_N, NAND\_ADQ0, EMAC1\_TX\_CLK  
HPS\_IOB\_2, GPIO1\_IO1, SPIM1\_MOSI, UART0\_RTS\_N, NAND\_ADQ1, EMAC1\_TX\_CTL  
HPS\_IOB\_3, GPIO1\_IO2, SPIM1\_MISO, UART0\_TX, I2C0\_SDA, NAND\_WE\_N, EMAC1\_RX\_CLK  
HPS\_IOB\_4, GPIO1\_IO3, SPIM1\_SS0\_N, UART0\_RX, I2C0\_SCL, NAND\_RE\_N, EMAC1\_RX\_CTL  
HPS\_IOB\_5, GPIO1\_IO4, SPIM1\_SS1\_N, SPIS1\_CLK, UART1\_CTS\_N, NAND\_WP\_N, EMAC1\_TXD0  
HPS\_IOB\_6, GPIO1\_IO5, SPIS1\_MOSI, UART1\_RTS\_N, NAND\_ADQ2, EMAC1\_TXD1  
HPS\_IOB\_7, GPIO1\_IO6, SPIS1\_SS0\_N, UART1\_TX, I2C1\_SDA, NAND\_ADQ3, EMAC1\_RXD0  
HPS\_IOB\_8, GPIO1\_IO7, SPIS1\_MISO, UART1\_RX, I2C1\_SCL, NAND\_CLE, EMAC1\_RXD1  
HPS\_IOB\_9, GPIO1\_IO8, JTAG\_TCK, SPIS0\_CLK, MDIO2\_MDIO, I2C\_EMAC2\_SDA, NAND\_ADQ4, EMAC1\_TXD2  
HPS\_IOB\_10, GPIO1\_IO9, JTAG\_TMS, SPIS0\_MOSI, MDIO2\_MDC, I2C\_EMAC2\_SCL, NAND\_ADQ5, EMAC1\_TXD3  
HPS\_IOB\_11, GPIO1\_IO10, JTAG\_TDO, SPIS0\_SS0\_N, MDIO0\_MDIO, I2C\_EMAC0\_SDA, NAND\_ADQ6, EMAC1\_RXD2  
HPS\_IOB\_12, GPIO1\_IO11, JTAG\_TDI, SPIS0\_MISO, MDIO0\_MDC, I2C\_EMAC0\_SCL, NAND\_ADQ7, EMAC1\_RXD3  
HPS\_IOB\_13, GPIO1\_IO12, I2C1\_SDA, NAND\_ALE, SDMMC\_DATA0, EMAC2\_TX\_CLK  
HPS\_IOB\_14, GPIO1\_IO13, I2C1\_SCL, NAND\_RB, SDMMC\_CMD, EMAC2\_TX\_CTL  
HPS\_IOB\_15, GPIO1\_IO14, UART1\_TX, NAND\_CE\_N, SDMMC\_CCLK, EMAC2\_RX\_CLK  
HPS\_IOB\_16, GPIO1\_IO15, UART1\_RX, SDMMC\_DATA1, EMAC2\_RX\_CTL  
HPS\_IOB\_17, GPIO1\_IO16, UART1\_CTS\_N, NAND\_ADQ8, SDMMC\_DATA2, EMAC2\_TXD0  
HPS\_IOB\_18, GPIO1\_IO17, SPIM0\_SS1\_N, UART1\_RTS\_N, NAND\_ADQ9, SDMMC\_DATA3, EMAC2\_TXD1  
HPS\_IOB\_19, GPIO1\_IO18, SPIM0\_MISO, MDIO1\_MDIO, I2C\_EMAC1\_SDA, NAND\_ADQ10, SDMMC\_DATA4, EMAC2\_RXD0  
HPS\_IOB\_20, GPIO1\_IO19, SPIM0\_SS0\_N, MDIO1\_MDC, I2C\_EMAC1\_SCL, NAND\_ADQ11, SDMMC\_DATA5, EMAC2\_RXD1  
HPS\_IOB\_21, GPIO1\_IO20, SPIM0\_CLK, SPIS1\_CLK, I2C\_EMAC2\_SDA, NAND\_ADQ12, SDMMC\_DATA6, EMAC2\_TXD2  
HPS\_IOB\_22, GPIO1\_IO21, SPIM0\_MOSI, SPIS1\_MOSI, I2C\_EMAC2\_SCL, NAND\_ADQ13, SDMMC\_DATA7, EMAC2\_TXD3  
HPS\_IOB\_23, GPIO1\_IO22, SPIM0\_MISO, SPIS1\_SS0\_N, MDIO0\_MDIO, I2C\_EMAC0\_SDA, NAND\_ADQ14, EMAC2\_RXD2  
HPS\_IOB\_24, GPIO1\_IO23, SPIM0\_SS0\_N, SPIS1\_MISO, MDIO0\_MDC, I2C\_EMAC0\_SCL, NAND\_ADQ15, EMAC2\_RXD3

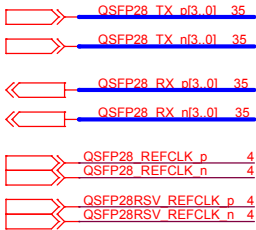
AGFB014R24B1E1V

HPS IO VCCIO = 1.8V

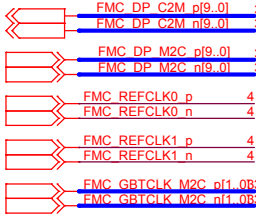
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Agilex SOM		
Size	Document Number	Rev
B	FPGA Bank HPS	A
Date:	Thursday, May 05, 2022	Sheet 17 of 51



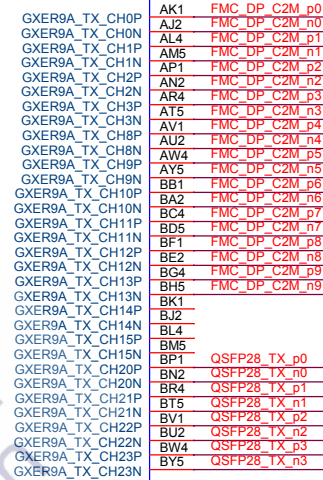
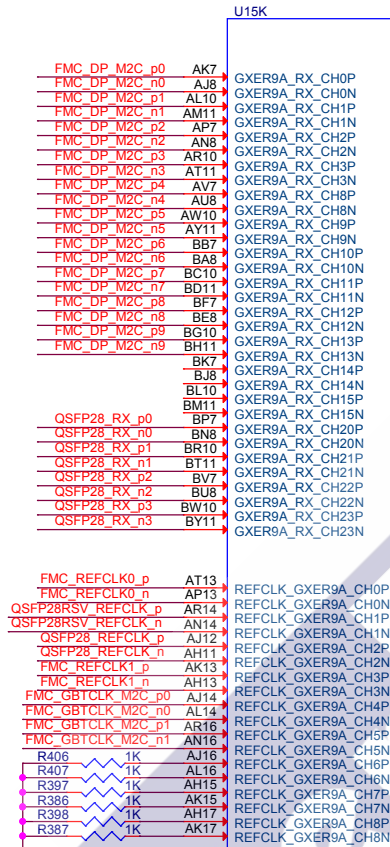
# QSFP28 Transceivers



## On-board FMC Port Transceivers

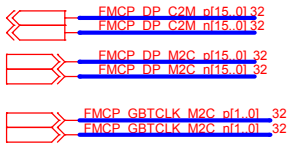


## FPGA Temperature diode

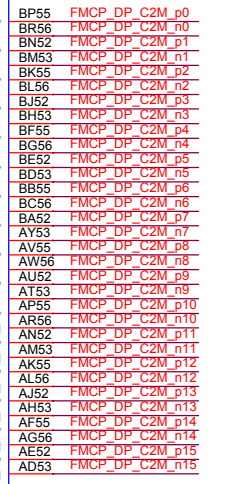
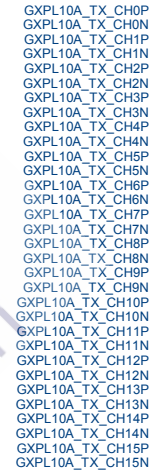
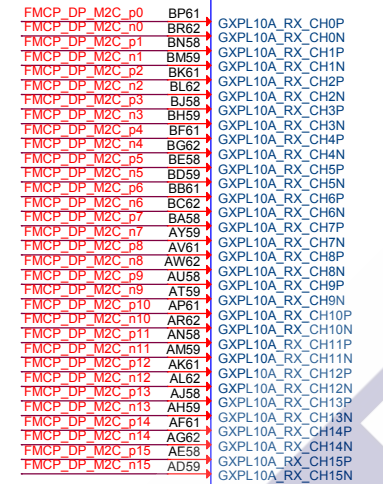




PCIe Transceiver

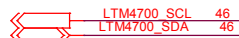
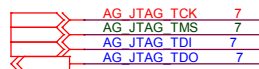


FPGA Temperature diode

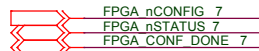


Bank 10A

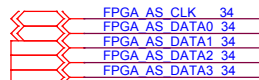
## Agilex JTAG Interface



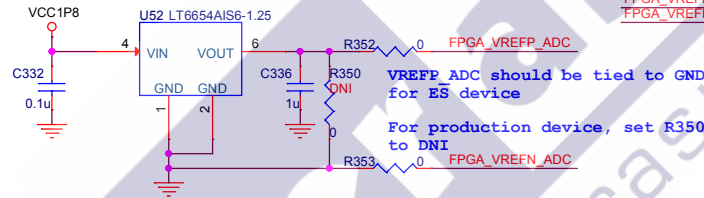
## FPGA AVSTX16 Configuration



## FPGA AS Configuration

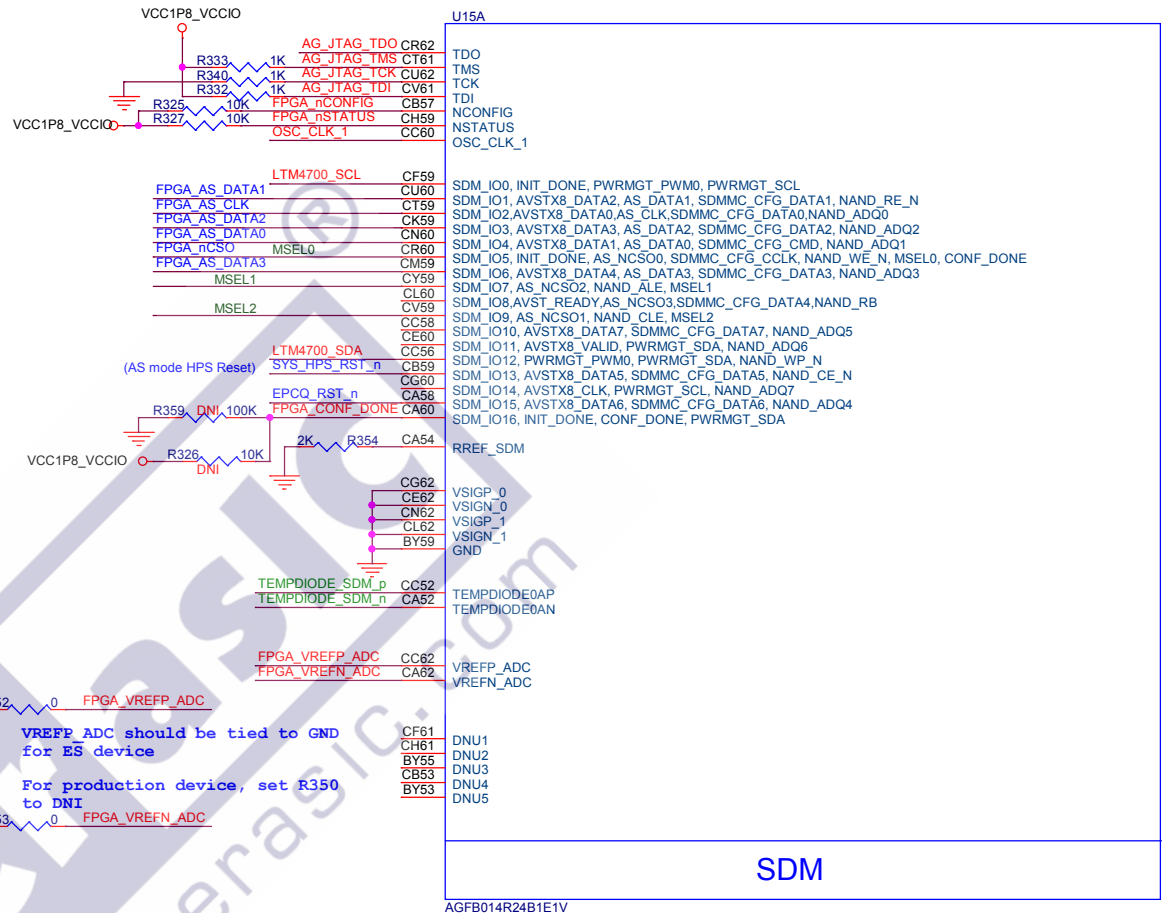
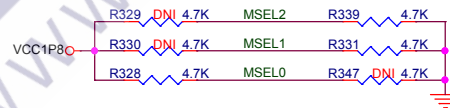


## FPGA Temperature diode



Default Setting:  
MSEL[2:0] = 001b, AS (Fast mode – for CvP)

MSEL[2..0]



SDM

AGFB014R24B1E1V

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Title	
Agilex SOM	
Size	Document Number
B	FPGA Configuration
Date:	Thursday, June 02, 2022
Sheet	20 of 51
Rev	A

Diagram illustrating the pin connections for the AGFB014R24B1E1V component, showing various power and control pins and their associated signals.

**Top Section (Pins 1-10):**

- VCC0P9\_VCCCH\_O
- BR20
- BP19
- BK19
- BH19
- BD19
- BB19
- AY19
- AW20
- AU20

**Middle Section (Pins 11-15):**

- VCC1P1\_VCCCH\_GXE
- BP17
- BM17
- BK17
- BB17
- AY17

**Bottom Section (Pins 16-25):**

- VCC0P9\_VCCRT\_GXE
- BP15
- BN14
- BM15
- BL14
- BK15
- BJ14
- BG14
- BE14
- BC14
- BB15
- BA14
- AY15
- AW14
- AV15

**Bottom Section (Pins 26-27):**

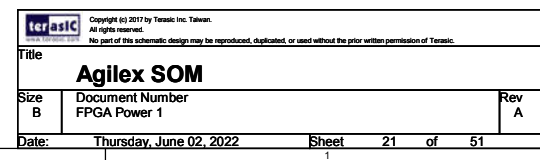
- VCC0P9\_VCCRTPLL\_GXE
- BG16
- BE16

**Bottom Right:**

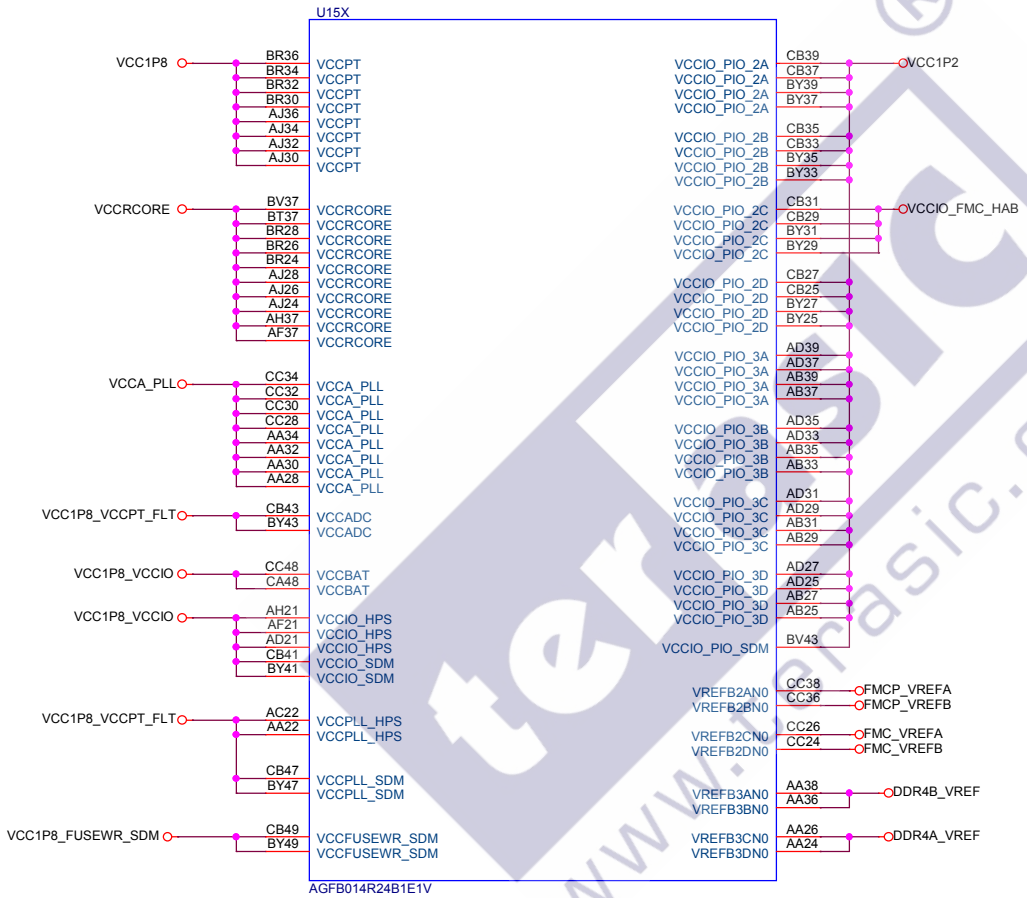
AGFB014R24B1E1V

**Legend:**

- 45 VSENSEP\_VCC0P9\_VCCCH
- 45 VSENSEN\_VCC0P9\_VCCCH



FPGA Power 2

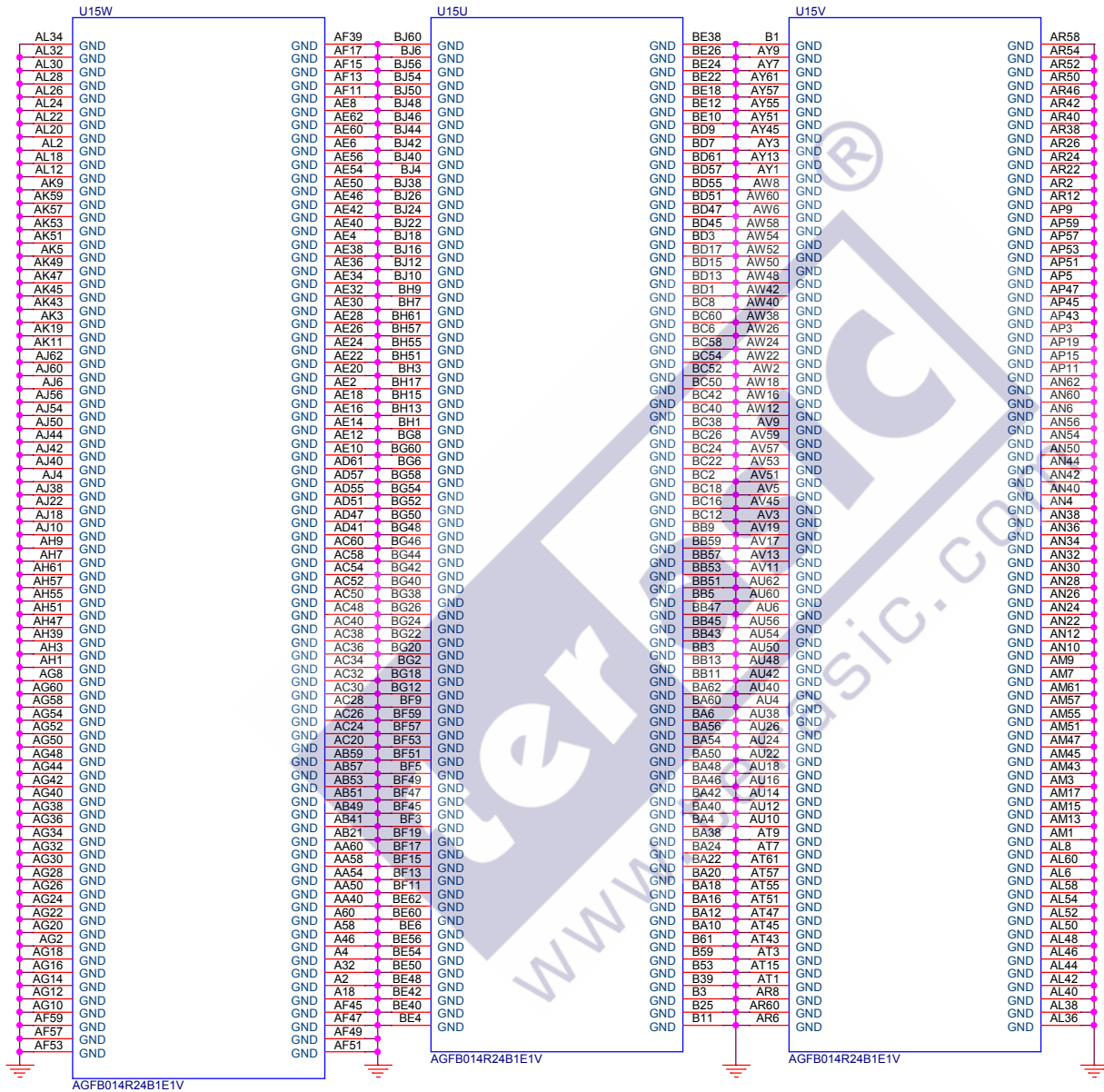


# FPGA GND 1

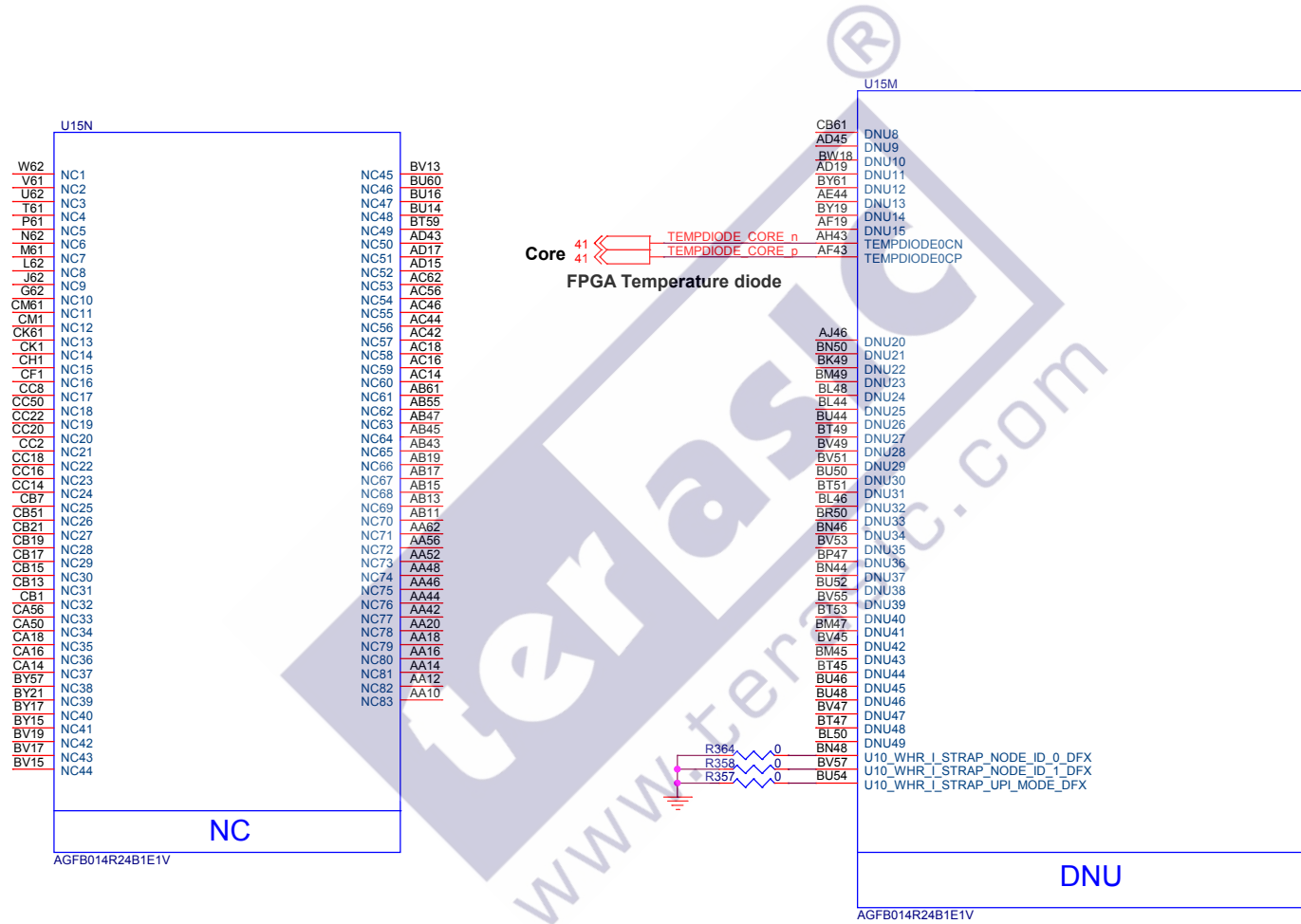


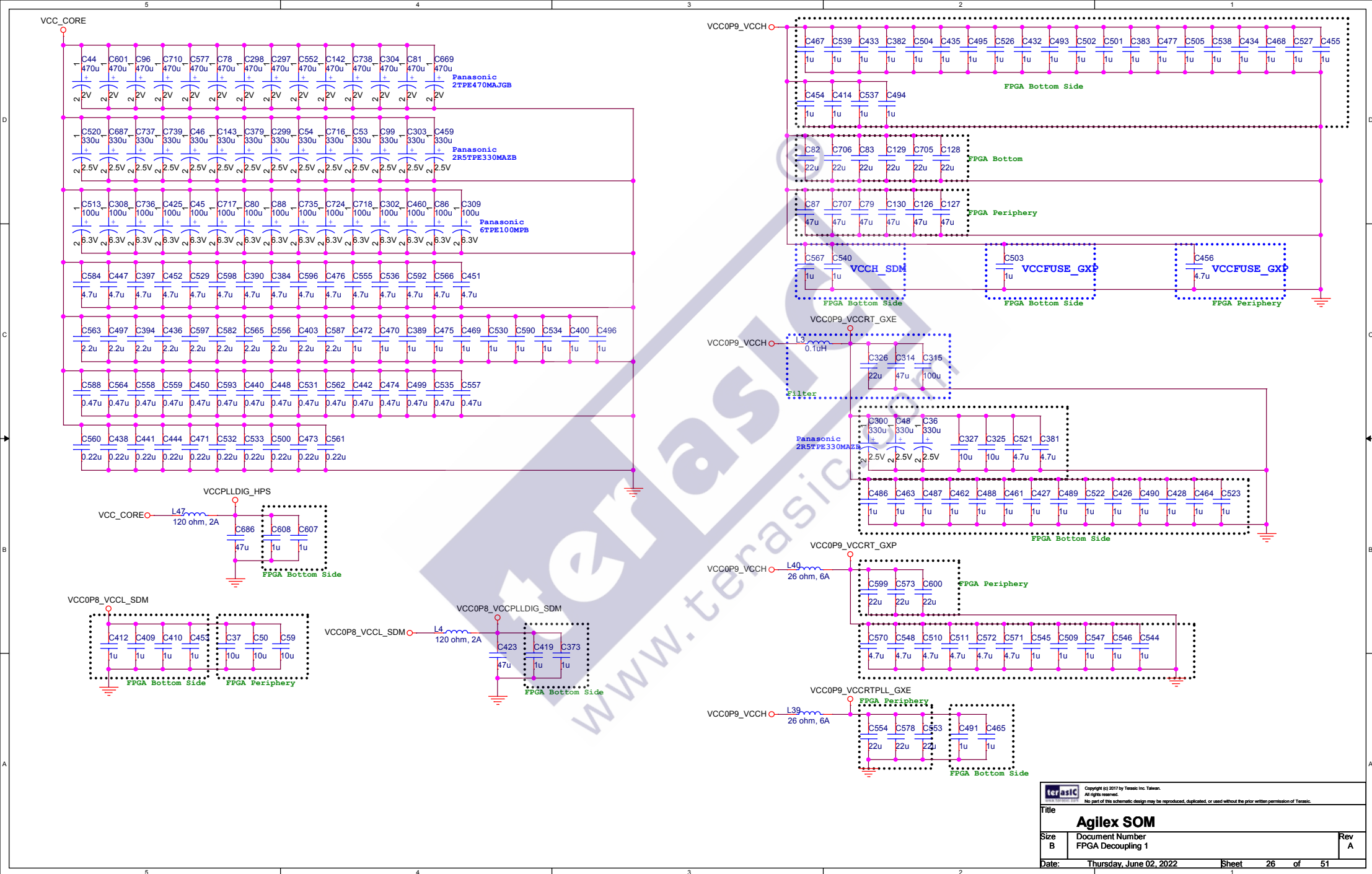


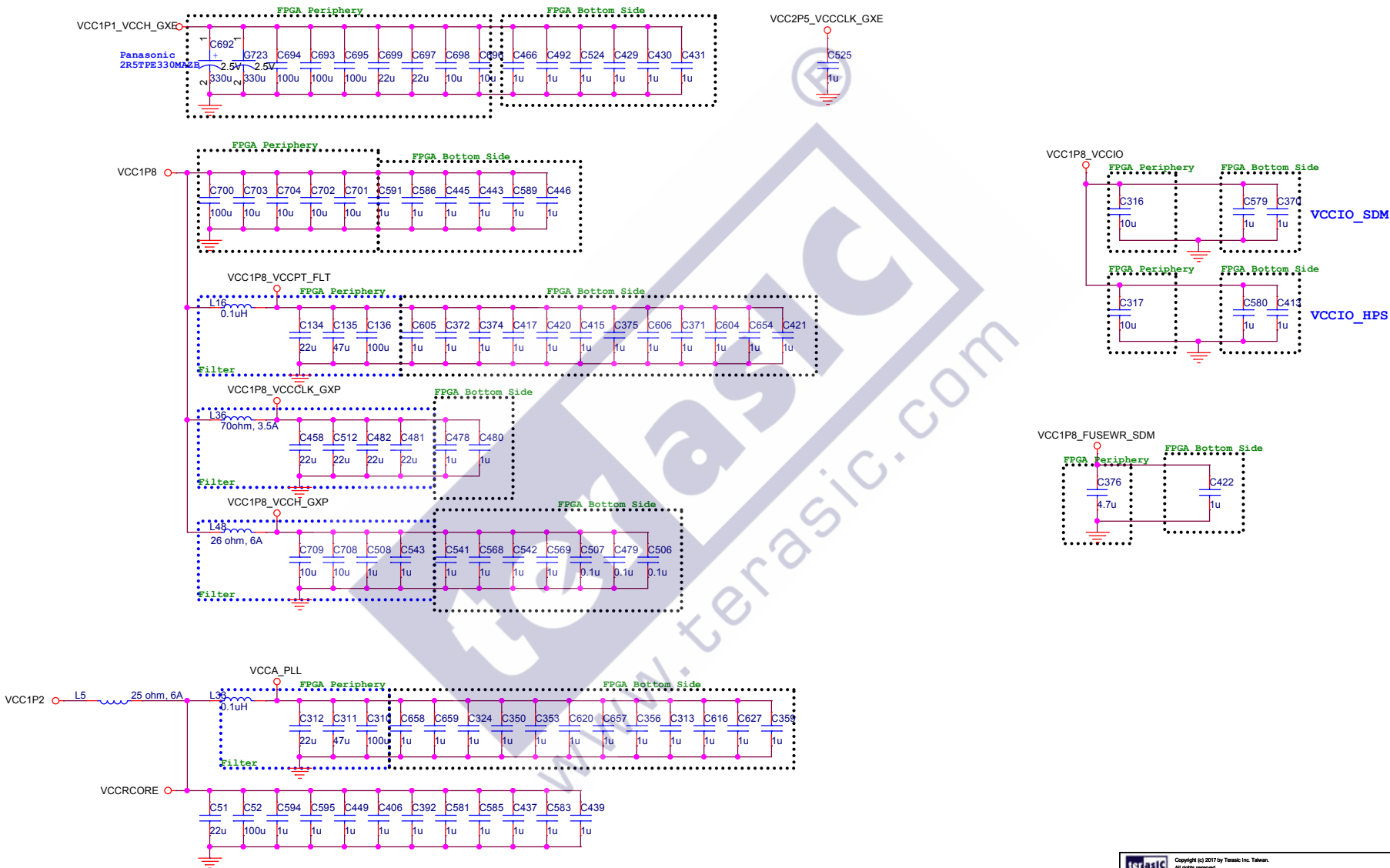
# FPGA GND 2



# FPGA NC/DNU

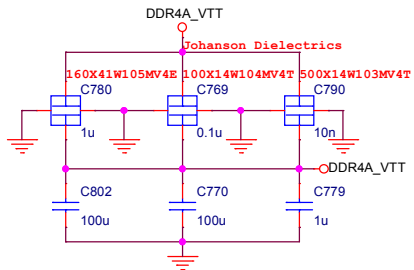
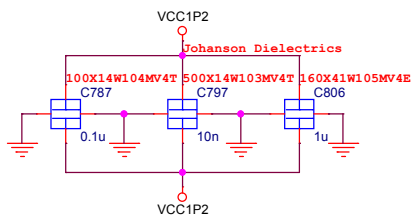
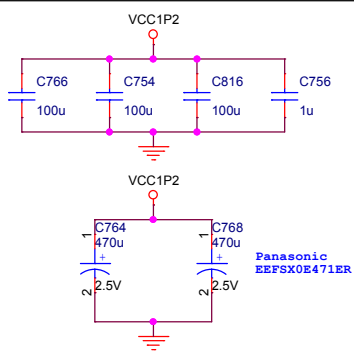








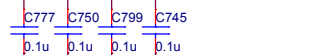
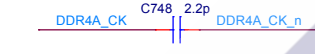




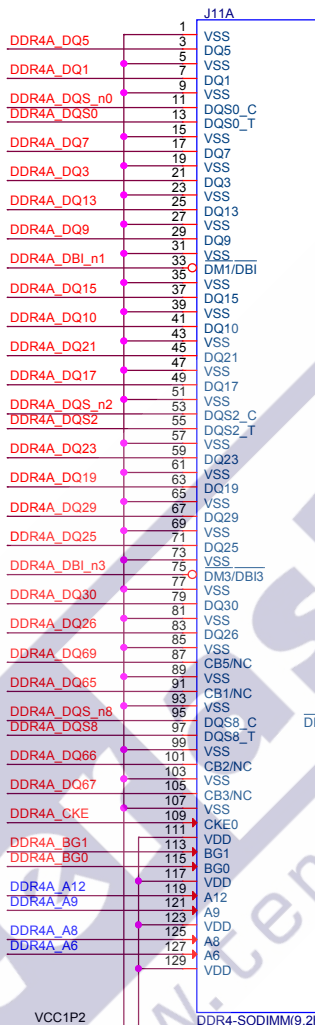
## DDR4A SO-DIMM

DDR4A CK	13
DDR4A CK_n	13
DDR4A BA[1..0]	13
DDR4A BG[1..0]	13
DDR4A ODT	13
DDR4A CS_n	13
DDR4A DQ[71..0]	13,14
DDR4A DQS[18..0]	13,14
DDR4A DQS_n[18..0]	13,14
DDR4A A[16..0]	13
DDR4A DBI_n[8..0]	13,14
DDR4A CKE	13
DDR4A RESET_n	13
DDR4A PAR	13
DDR4A ACT_n	13
DDR4A ALERT_n	13
E_DDR4A_SDA	8
E_DDR4A_SCL	8
E_DDR4A_EVENT_n	8

RAS\_n is a multiplexed function with A16  
CAS\_n is a multiplexed function with A15  
WE\_n is a multiplexed function with A14

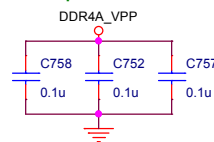


Place near the pins of DDR4 SO-DIMM

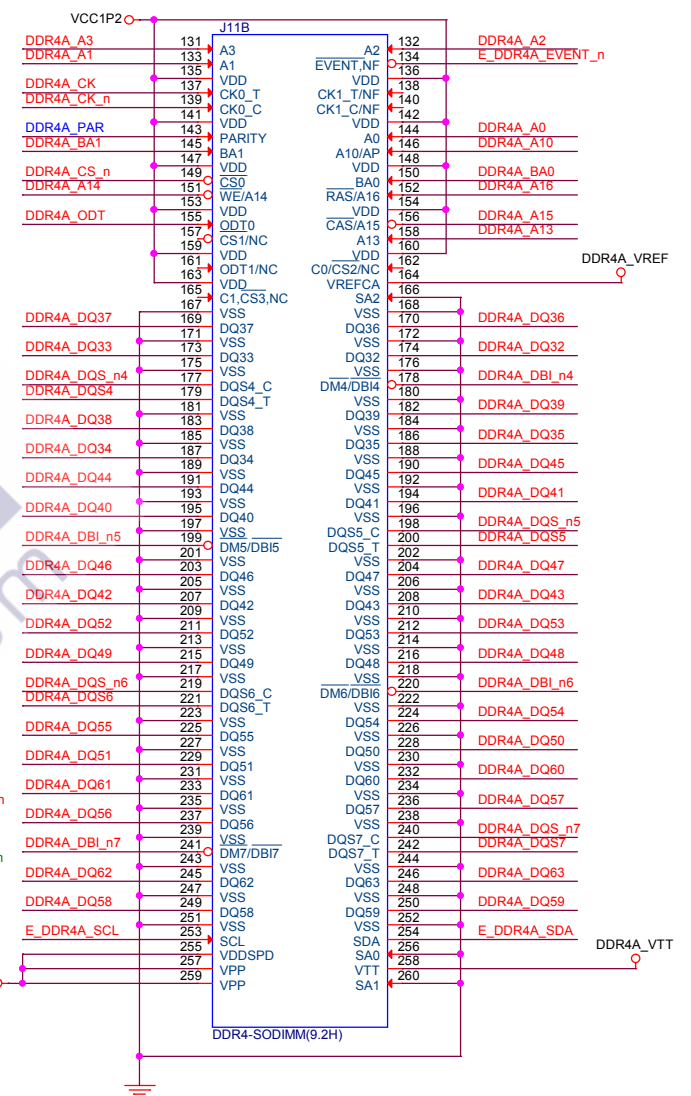
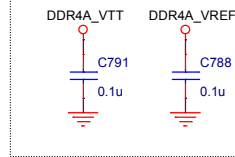


VPP\_DDR4 = 2.5V  
VTT\_DDR4 = 0.6V  
VREF\_DDR4 = 0.6V

Place near the pins of DDR4 SO-DIMM



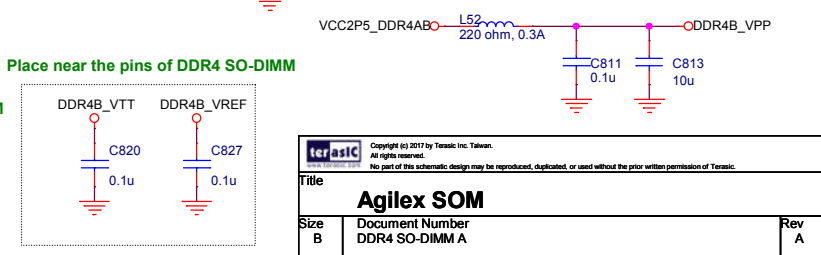
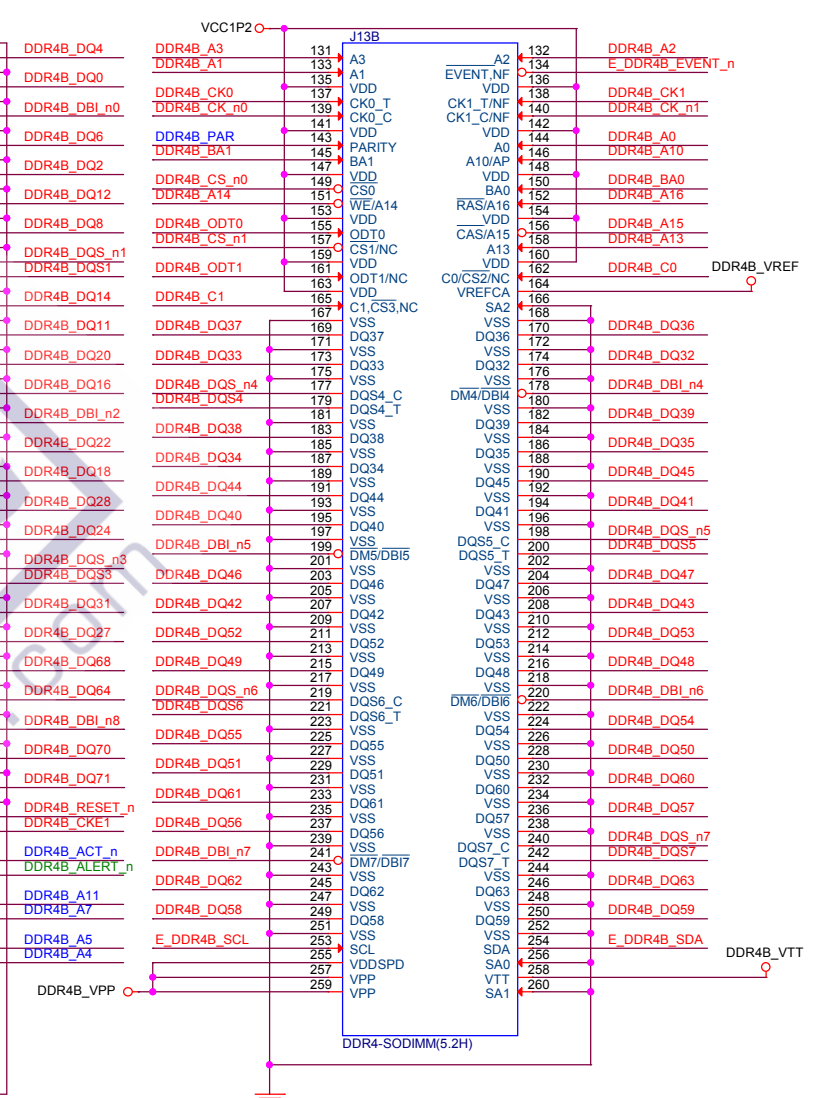
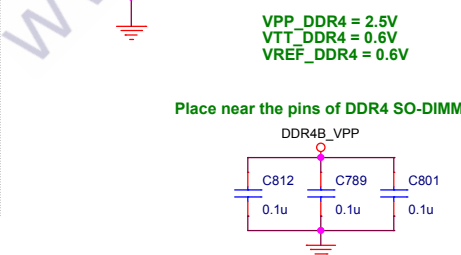
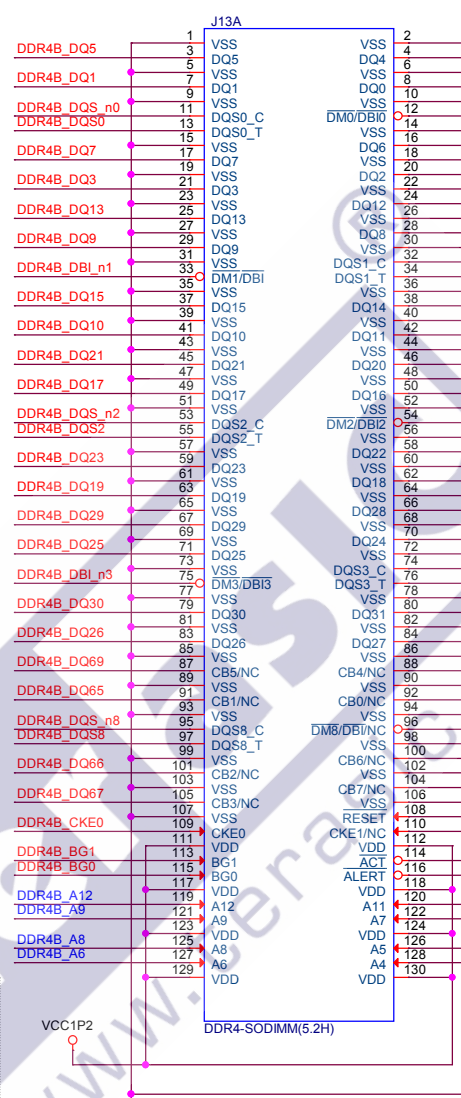
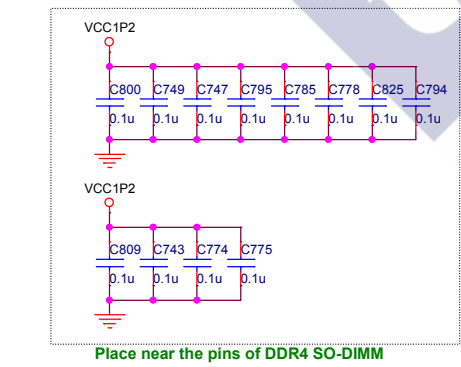
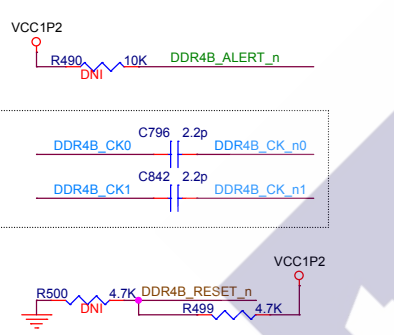
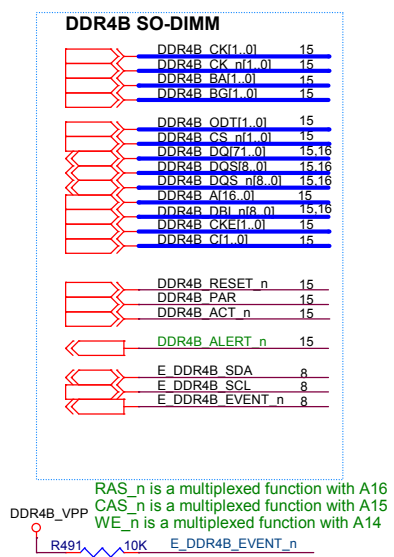
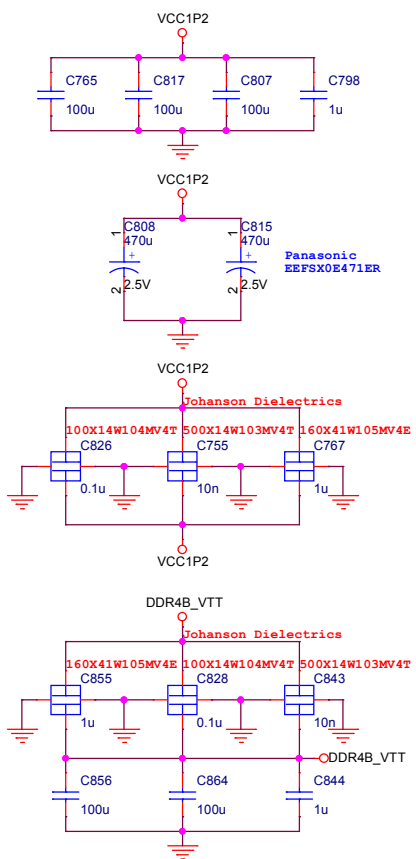
Place near the pins of DDR4 SO-DIMM



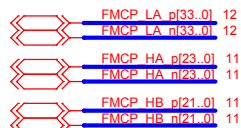
VCC2P5\_DDR4AB L51 220 ohm, 0.3A



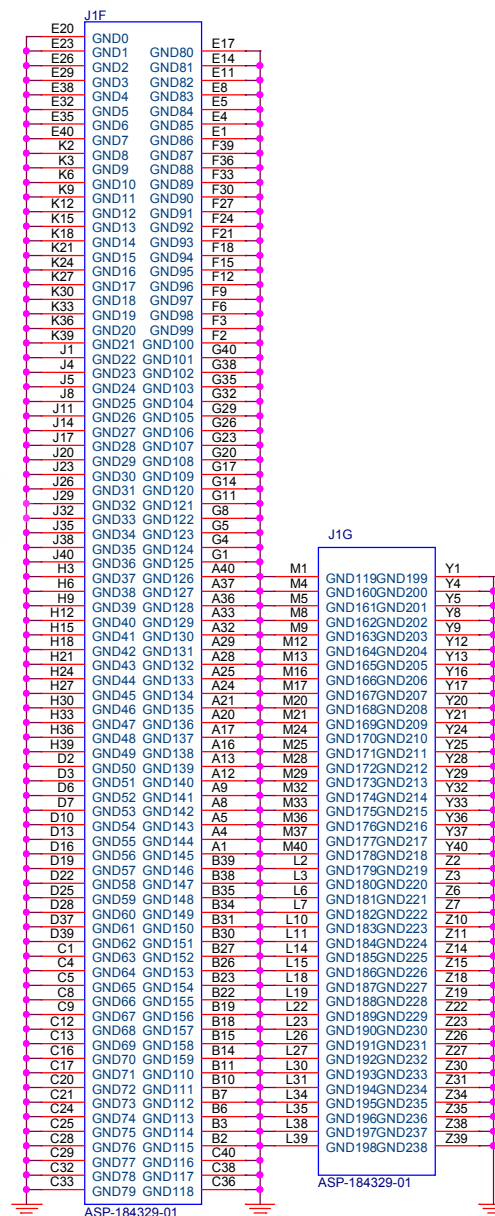
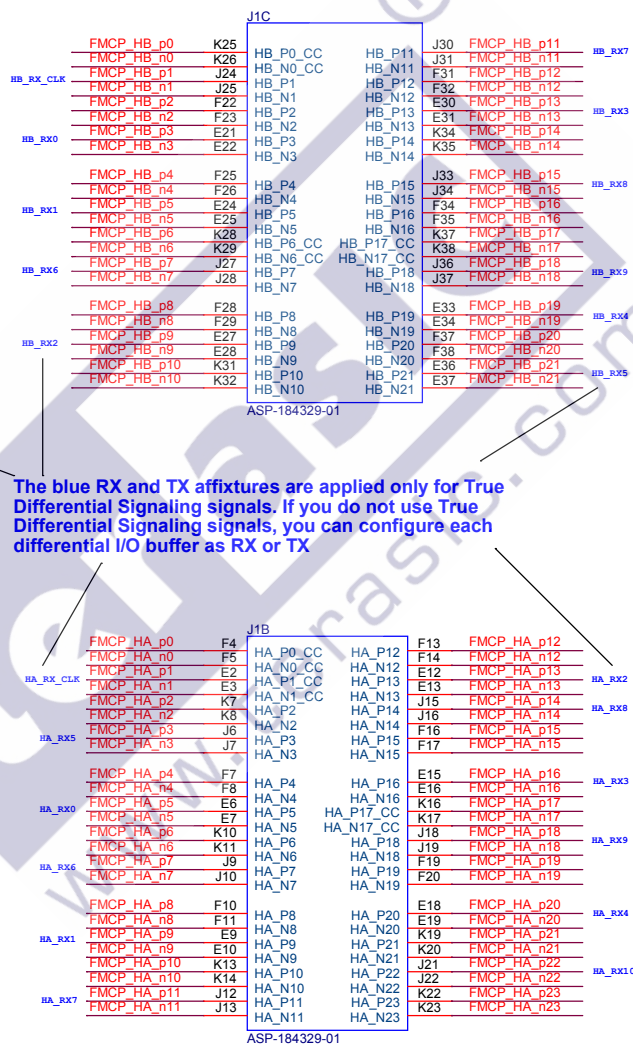
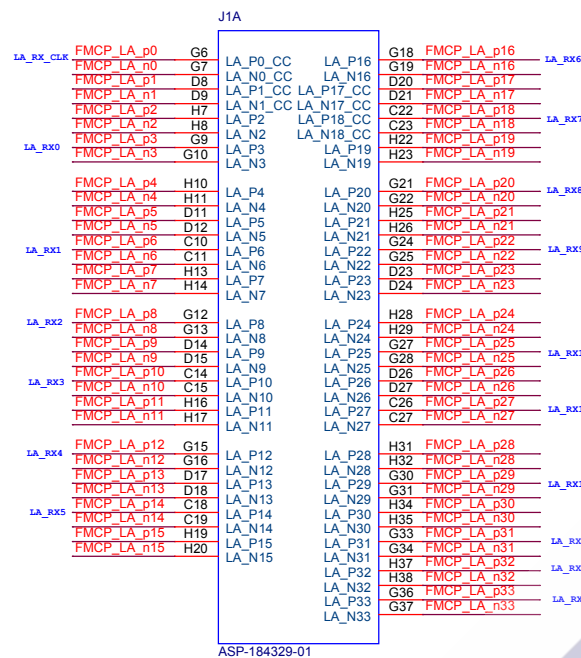
Agilex SOM		
Size B	Document Number DDR4 SO-DIMM B	Rev A
Date:	Thursday, June 02, 2022	Sheet 29 of 51



## FMC PORT INTERFACE(HPC)

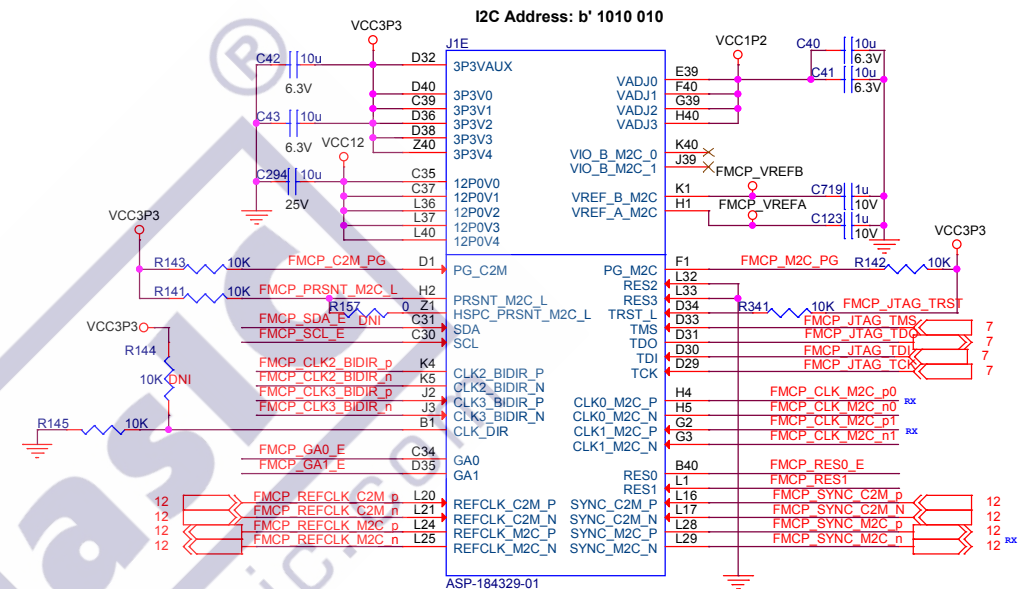
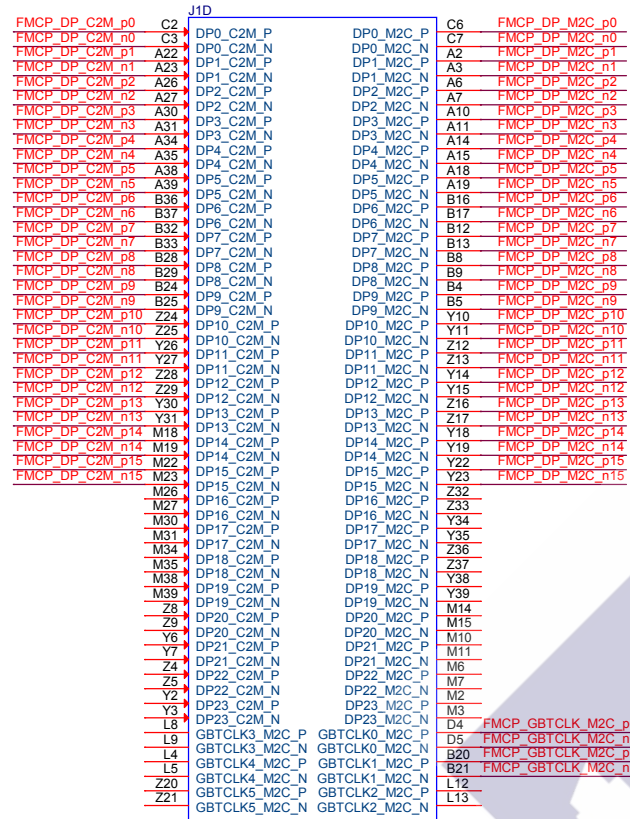


## FMC+ 1

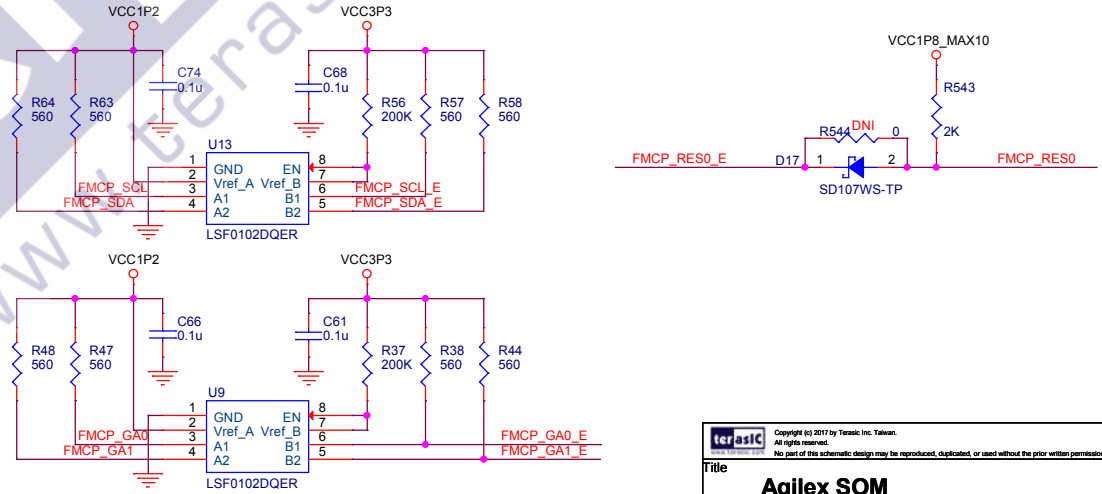


The blue RX and TX affixtures are applied only for True Differential Signaling signals. If you do not use True Differential Signaling signals, you can configure each differential I/O buffer as RX or TX

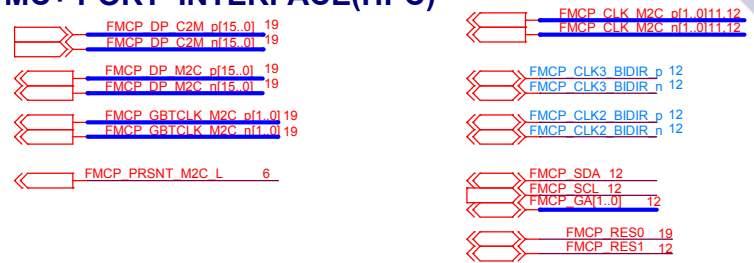
## FMC+ 2




**Translation Up need pull up resistor**



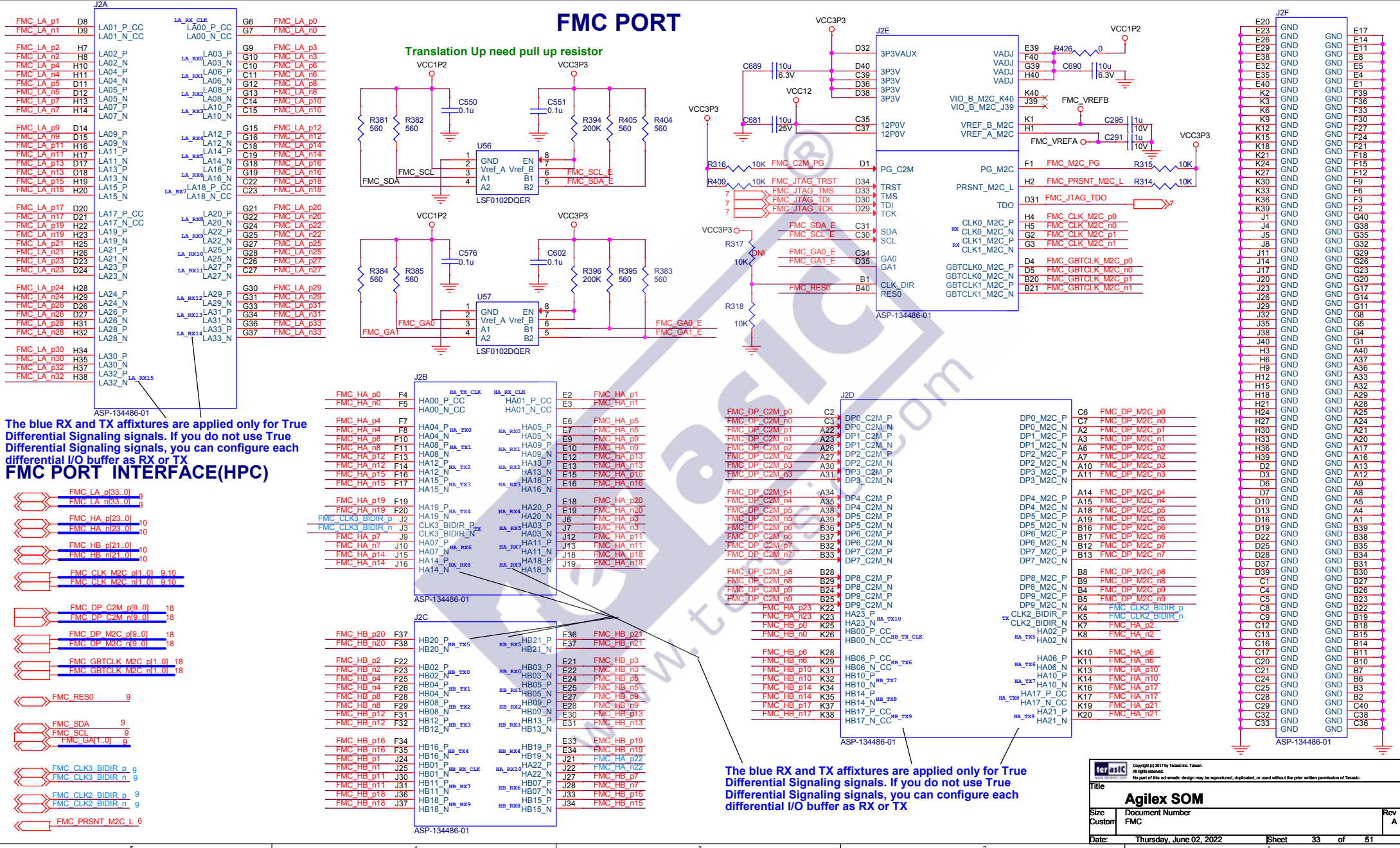
## FMC+ PORT INTERFACE(HPC)



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Title		<b>Agilex SOM</b>	
Size B	Document Number FMC+ 2		Rev A
Date: <b>Thursday, June 02, 2022</b>		Sheet <b>32</b>	of <b>51</b>



## FMC PORT



The blue RX and TX affixtures are applied only for True Differential Signaling signals. If you do not use True Differential Signaling signals, you can configure each differential I/O buffer as RX or TX

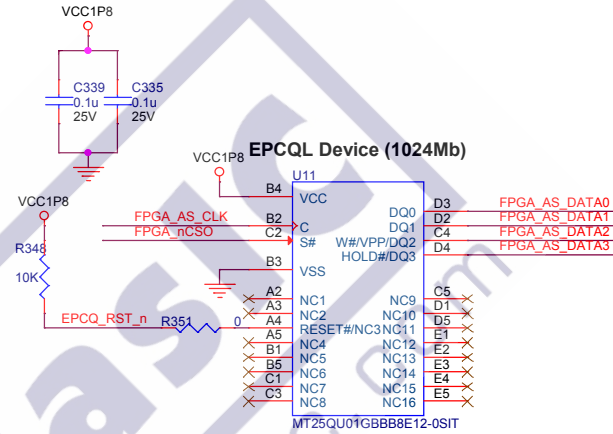
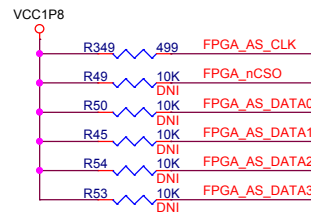


# FPGA AS Mode Configuration

FPGA AS DATA0	20
FPGA AS DATA1	20
FPGA AS DATA2	20
FPGA AS DATA3	20

FPGA AS CLK	20
FPGA nCSO	20

EPCQ\_RST\_n 7.20



# QSFP28 Port A Transceivers

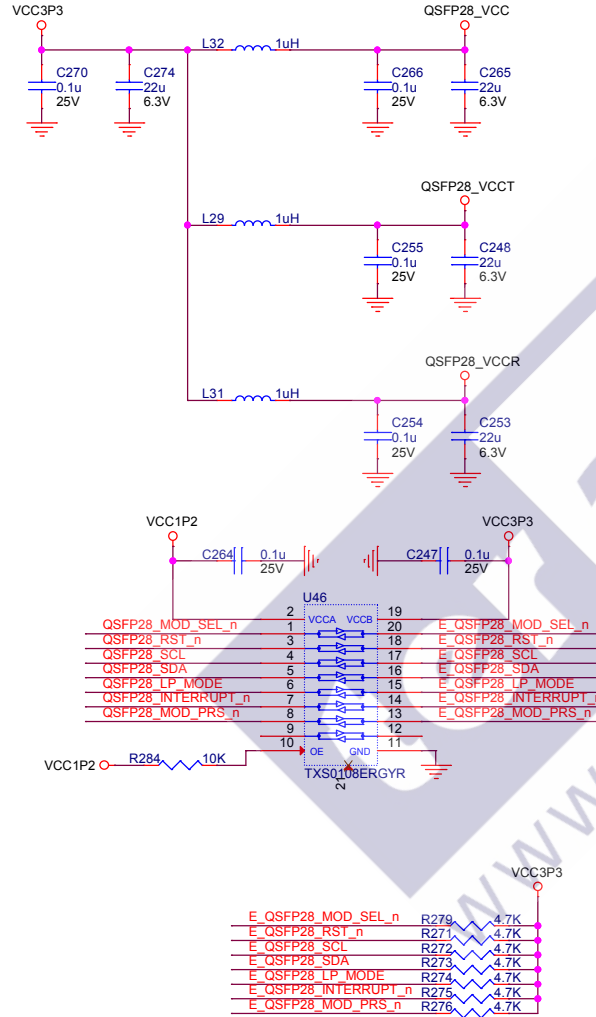
QSFP28\_TX\_p[3..0] 18  
QSFP28\_TX\_n[3..0] 18

QSFP28\_RX\_p[3..0] 18  
QSFP28\_RX\_n[3..0] 18

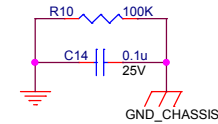
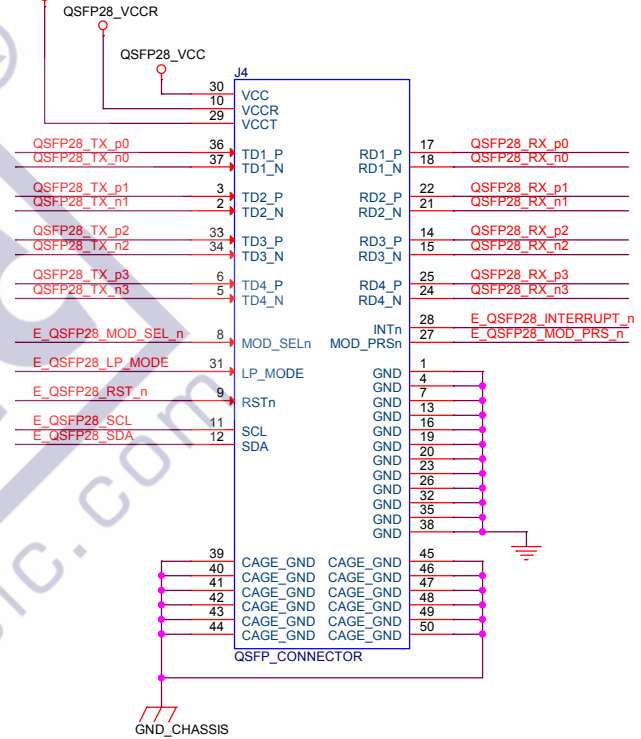
## QSFP28A Control Interface

QSFP28\_MOD\_SEL\_n 14  
QSFP28\_RST\_n 14  
QSFP28\_SCL 14  
QSFP28\_SDA 14  
QSFP28\_LP\_MODE 14  
QSFP28\_INTERRUPT\_n 14  
QSFP28\_MOD\_PRS\_n 14

NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.  
NOTE 2: Assuming that the SFP RD 100-ohm termination on the Host Board FPGA device will be implemented via the on-chip termination circuit.  
NOTE 3: DC blocking capacitors are in the module for RX and TX.  
NOTE 4: 1uH inductors should have a DC Resistance of less than 0.1-ohm.



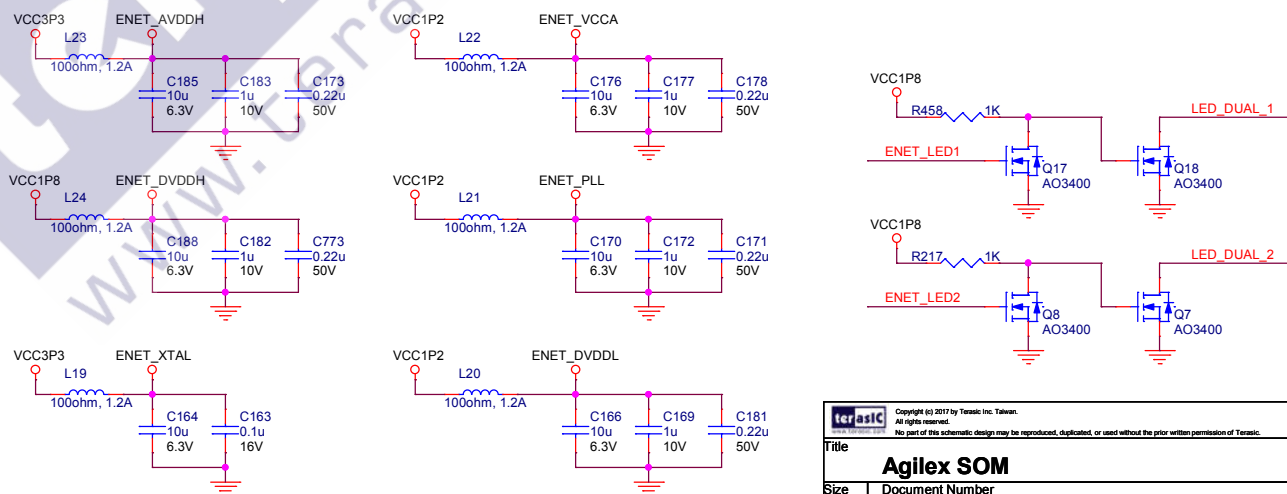
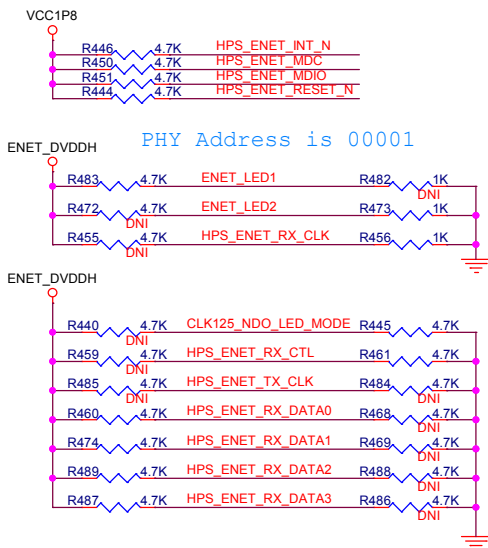
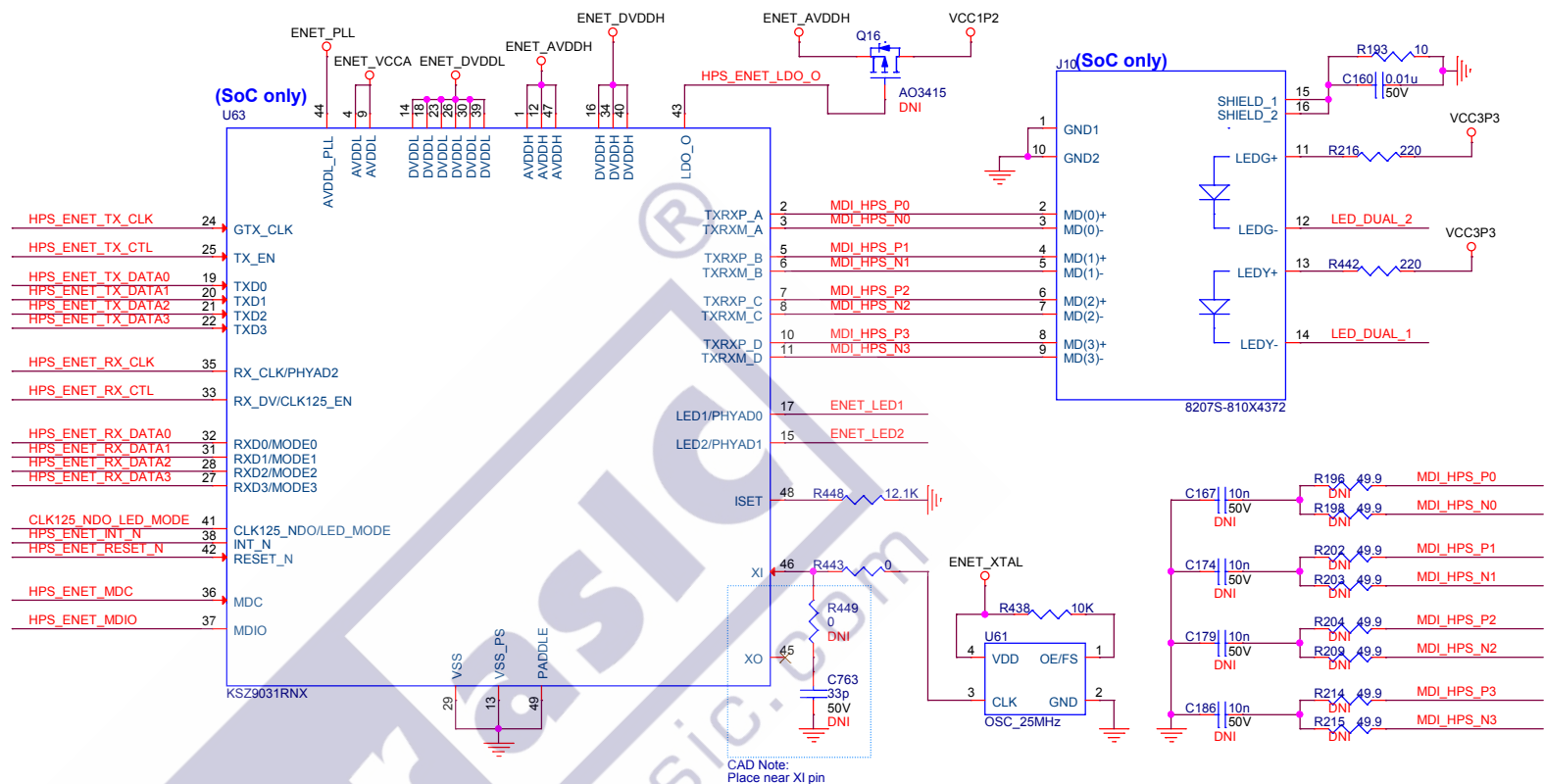
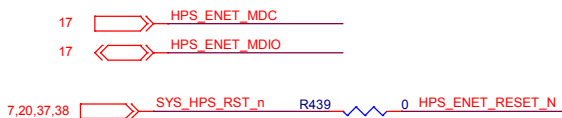
## QSFP28\_VCCCT




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Title		
Agilex SOM		
Size	Document Number	Rev
B	QSFP28	A
Date:	Thursday, June 02, 2022	Sheet 35 of 51

Diagram illustrating the HPS ENET TX and RX signals:

- TX Signals (Output):**
  - HPS\_ENET\_TX\_DATA[3..0]
  - HPS\_ENET\_TX\_CLK
  - HPS\_ENET\_TX\_CTL
- RX Signals (Input):**
  - HPS\_ENET\_RX\_DATA[3..0]
  - HPS\_ENET\_RX\_CLK
  - HPS\_ENET\_RX\_CTL

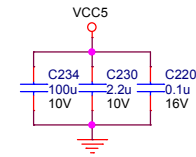
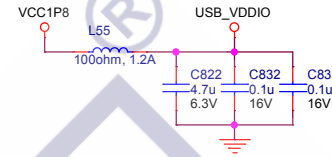
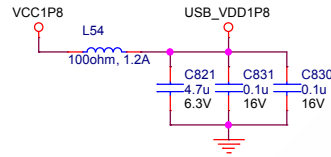
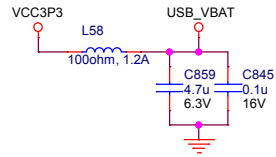


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<b>Title</b> <div style="text-align: center; font-size: 1.5em; font-weight: bold;">Agilex SOM</div>			
<b>Size</b> B	<b>Document Number</b> HPS - Gagabit Ethernet (SoC only)		<b>Rev</b> A
<b>Date:</b>	Thursday, June 02, 2022	Sheet	36 of 51

# UBS PHY Interface (ULPI)

17 << HPS\_USB\_DATA[7:0]  
 17 << HPS\_USB\_CLK  
 17 << HPS\_USB\_NXT  
 17 << HPS\_USB\_DIR  
 17 << HPS\_USB\_STP

CAD Note:  
Place near power pin



7,20,36,38 << SYS\_HPS\_RST\_n R496 0 HPS\_USB\_RESET\_N

(SoC only)

HPS\_USB\_DATA0  
 HPS\_USB\_DATA1  
 HPS\_USB\_DATA2  
 HPS\_USB\_DATA3  
 HPS\_USB\_DATA4  
 HPS\_USB\_DATA5  
 HPS\_USB\_DATA6  
 HPS\_USB\_DATA7

HPS\_USB\_CLK

HPS\_USB\_NXT  
 HPS\_USB\_DIR  
 HPS\_USB\_STP

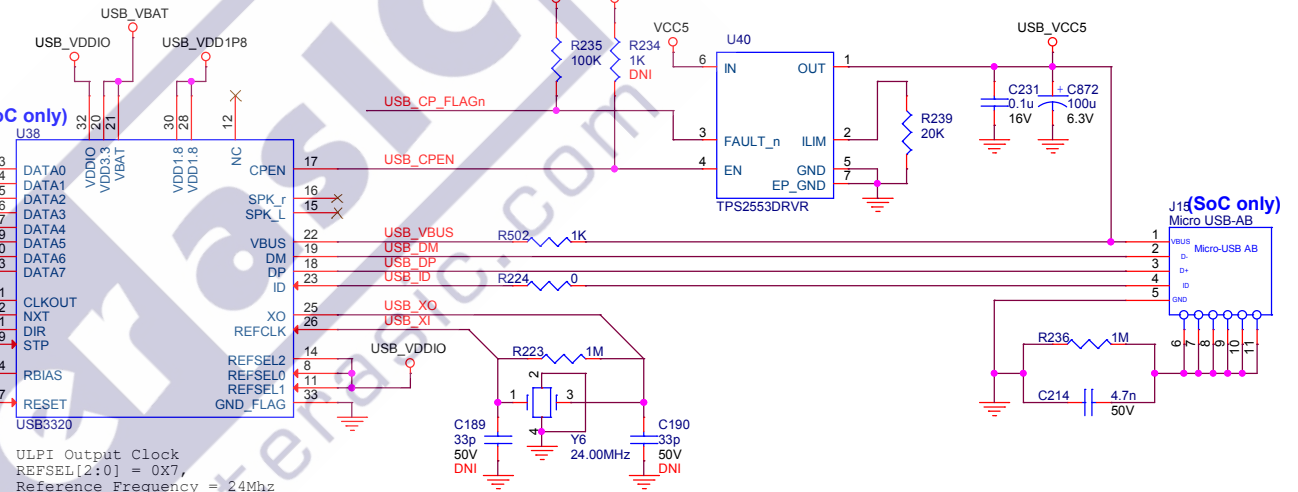
USB\_RBIAS

USB\_RESET\_PHY

HPS\_USB\_RESET\_N

Place Rbias as close as possible to USB3320  
 The nominal voltage at RBIAS is 0.8V +/- 10%

RESETB must be held low  
 until the VDD18 and VDDIO supplies are stable



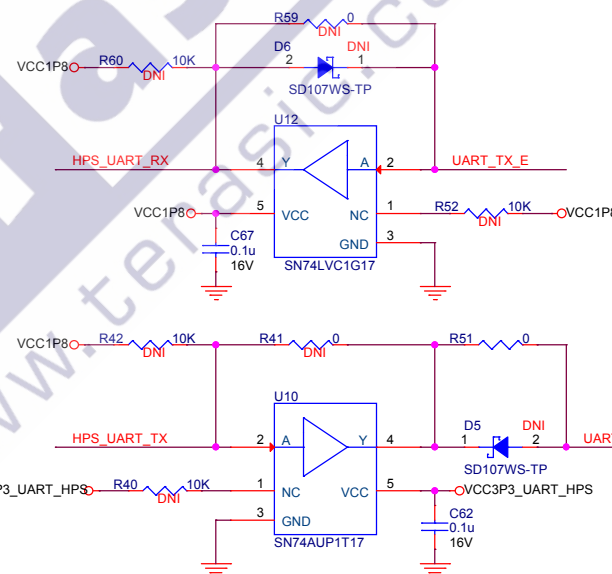
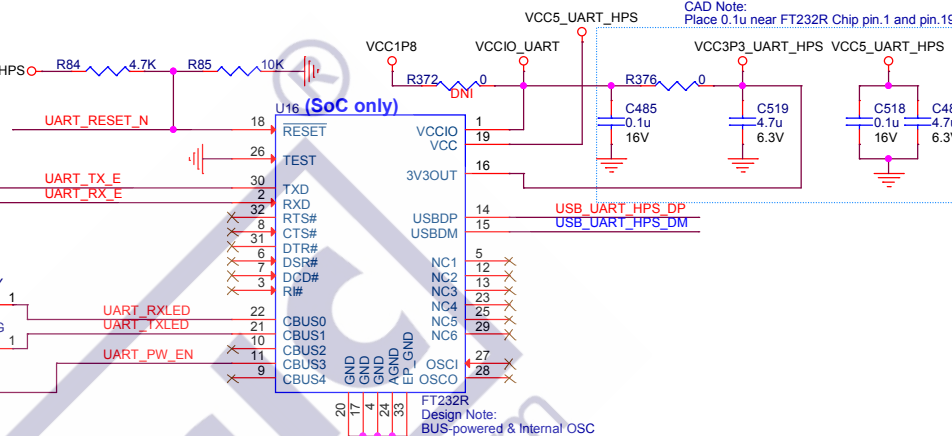
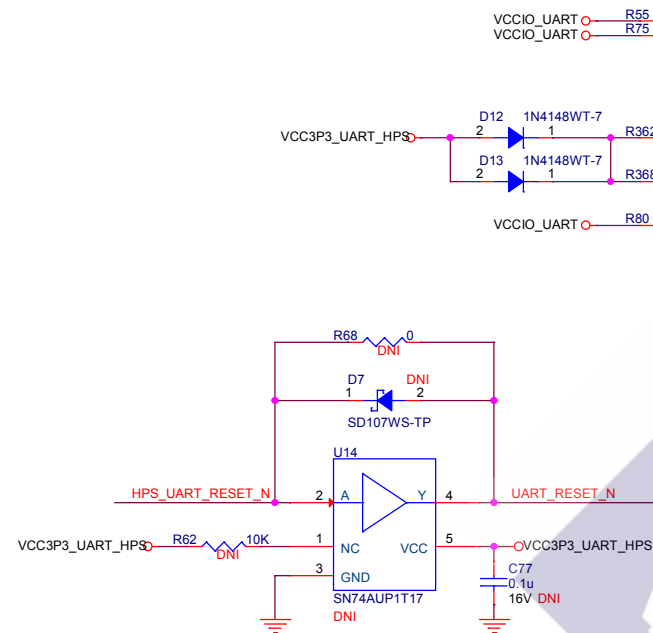
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Title		
Agilex SOM		
Size	Document Number	Rev
B	HPS: USB OTG (SoC only)	A
Date:	Thursday, June 02, 2022	Sheet 37 of 51

# UART Interface

HPS\_UART\_RX 17  
HPS\_UART\_TX 17

USB\_UART\_HPS\_DP 40  
USB\_UART\_HPS\_DM 40

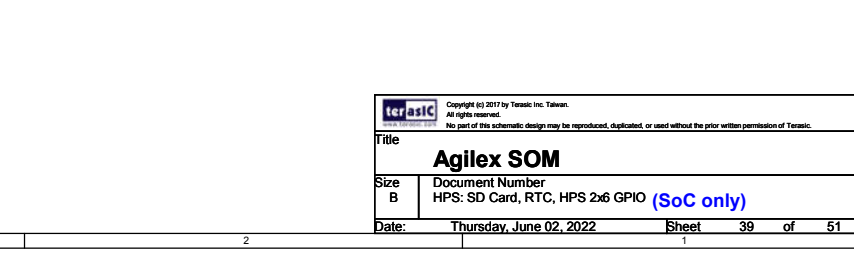
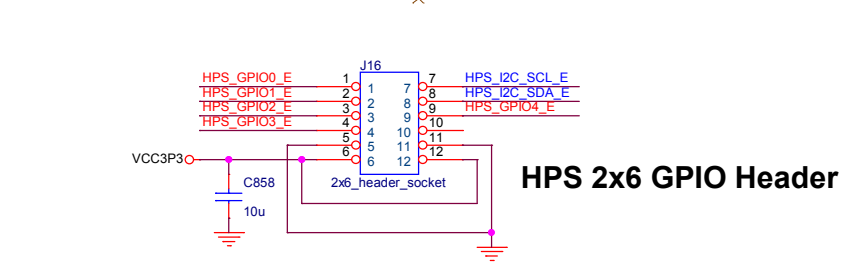
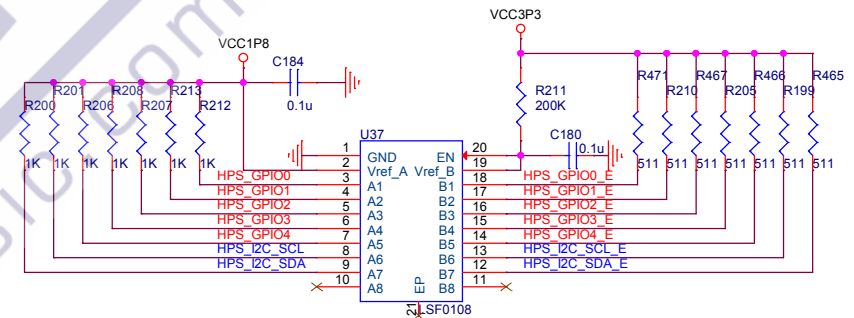
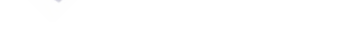
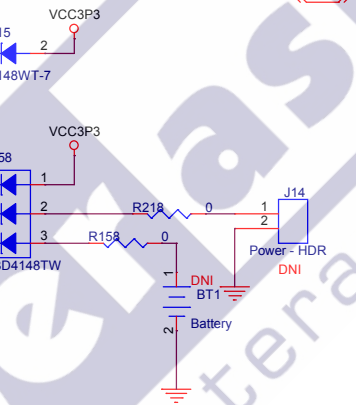
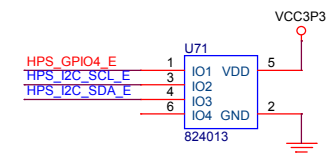
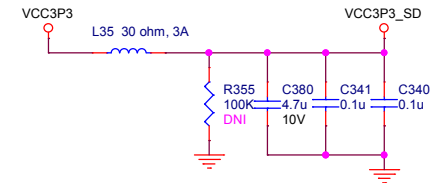
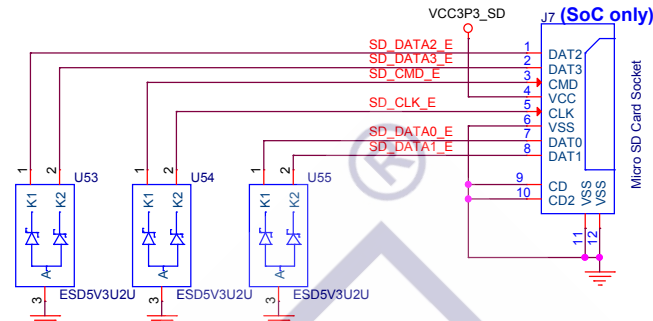
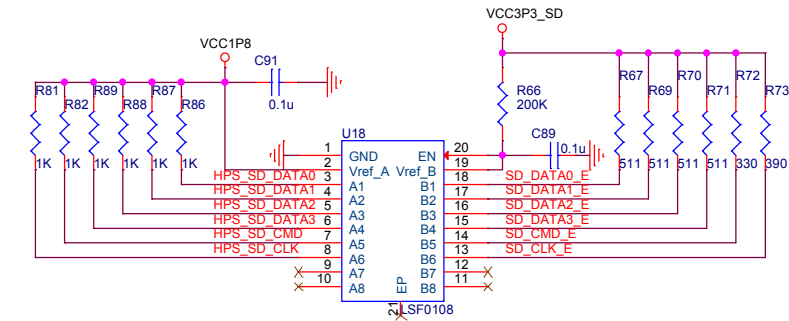
7,20,36,37 SYS\_HPS\_RST\_n R65 0 HPS\_UART\_RESET\_N



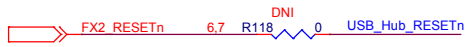
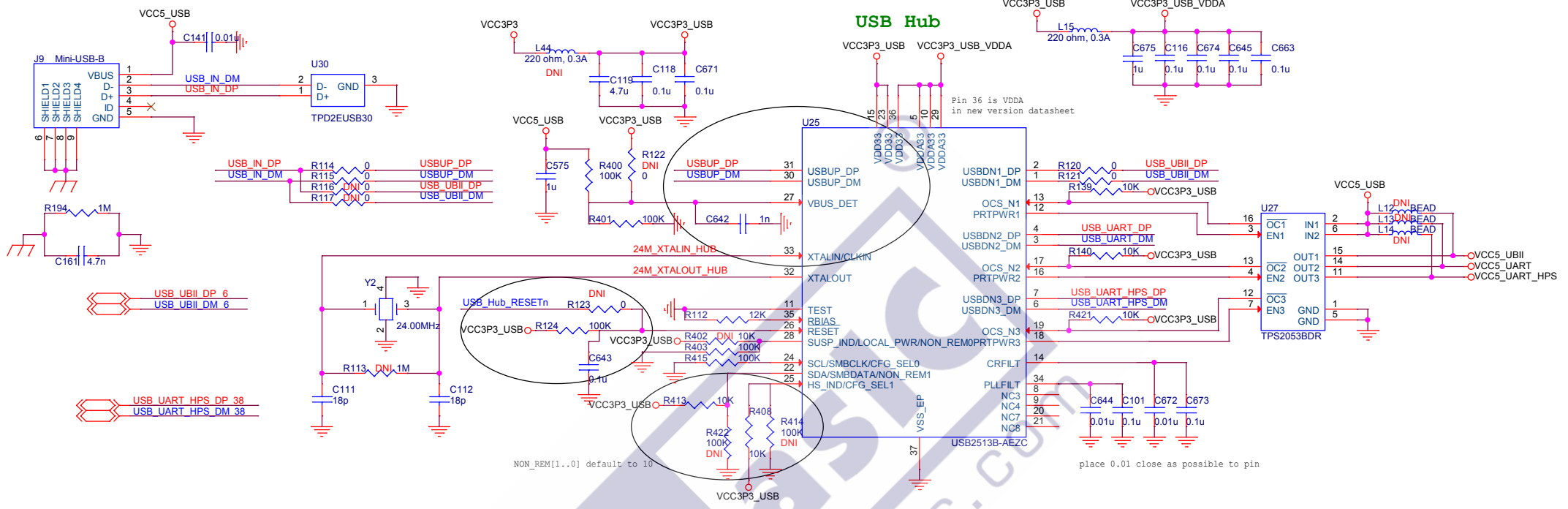
CAD Note:  
Place 0.1u near FT232R Chip pin.1 and pin.19

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Title		
Agilex SOM		
Size	Document Number	Rev
B	HPS: UART to USB (SoC only)	A
Date:	Thursday, June 02, 2022	Sheet 38 of 51

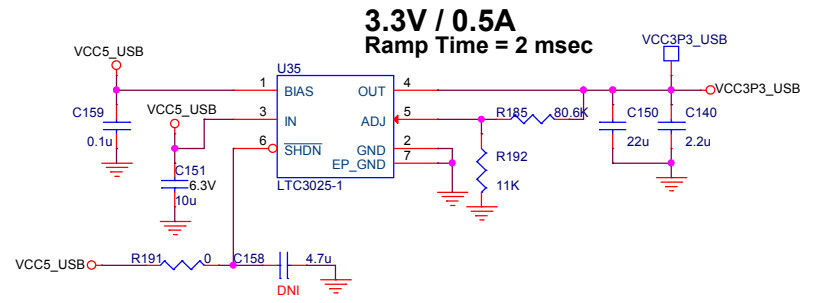
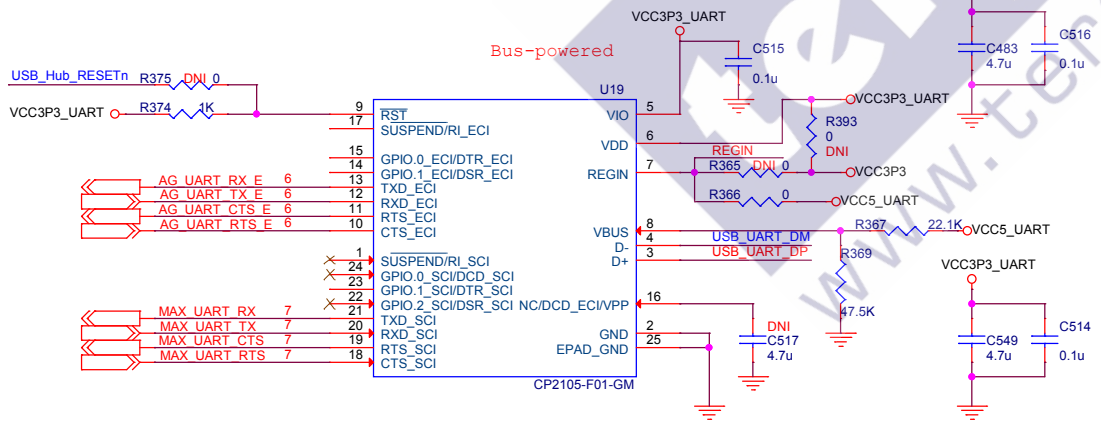




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Title	<b>Agilex SOM</b>	
Size B	Document Number HPS: SD Card, RTC, HPS 2x6 GPIO (SoC only)	Rev A
Date:	Thursday, June 02, 2022	Sheet 39 of 51

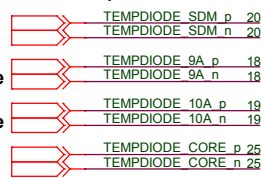


### Uart to USB

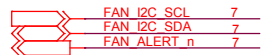


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Title		
Agilex SOM		
Size B	Document Number USB Hub, USB to Dual UART	Rev A
Date:	Thursday, June 02, 2022	Sheet 40 of 51

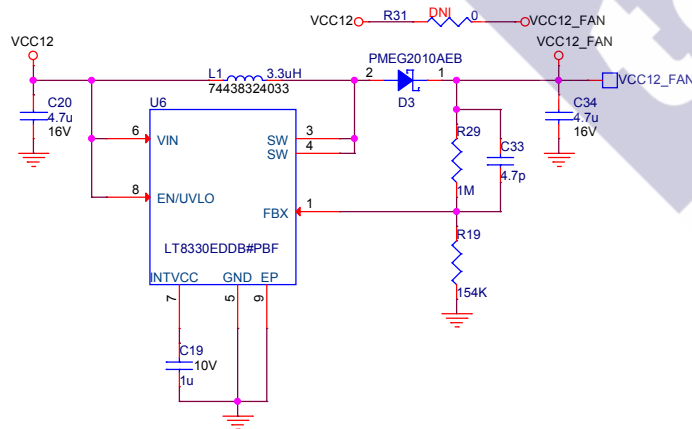
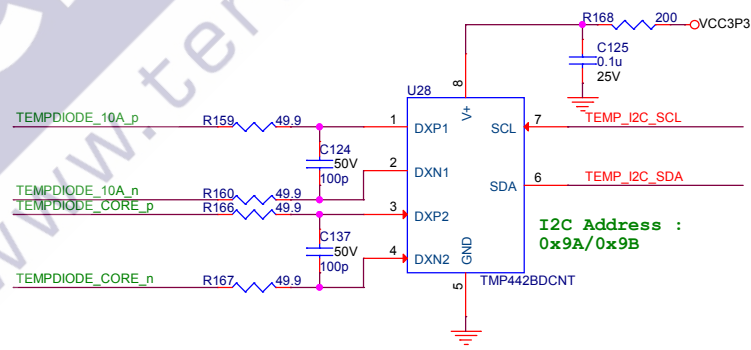
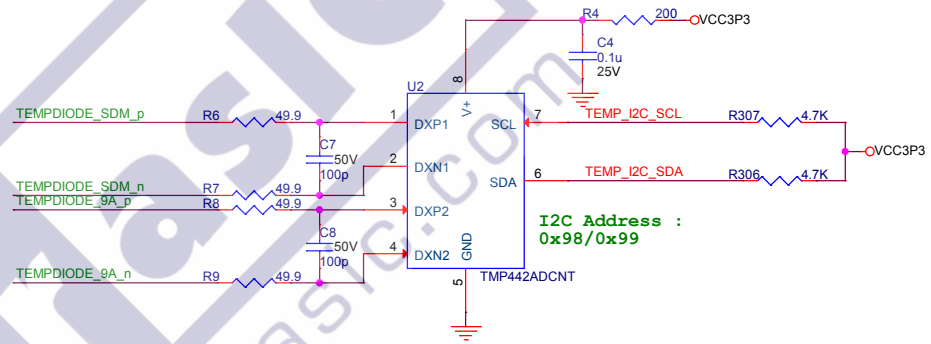
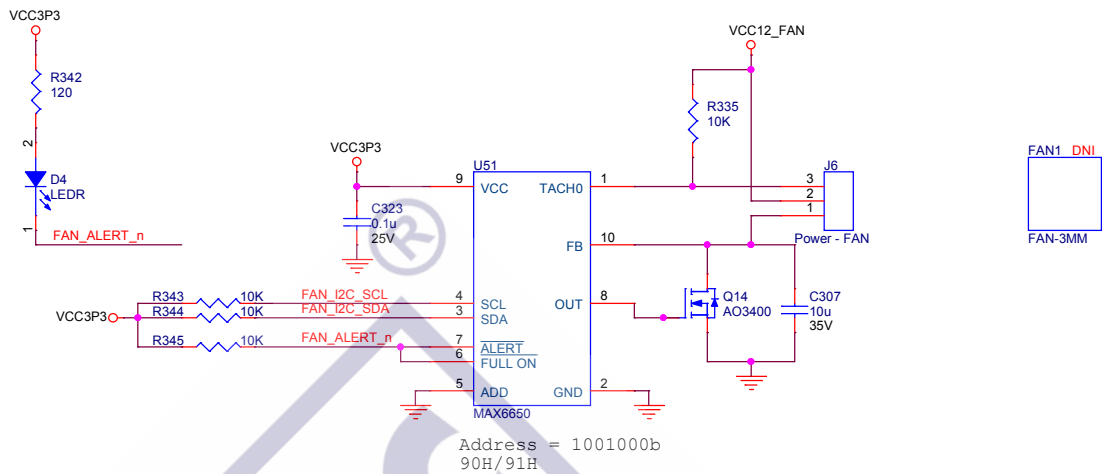
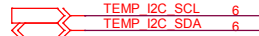
# FPGA Temperature diode



# FAN Control Interface



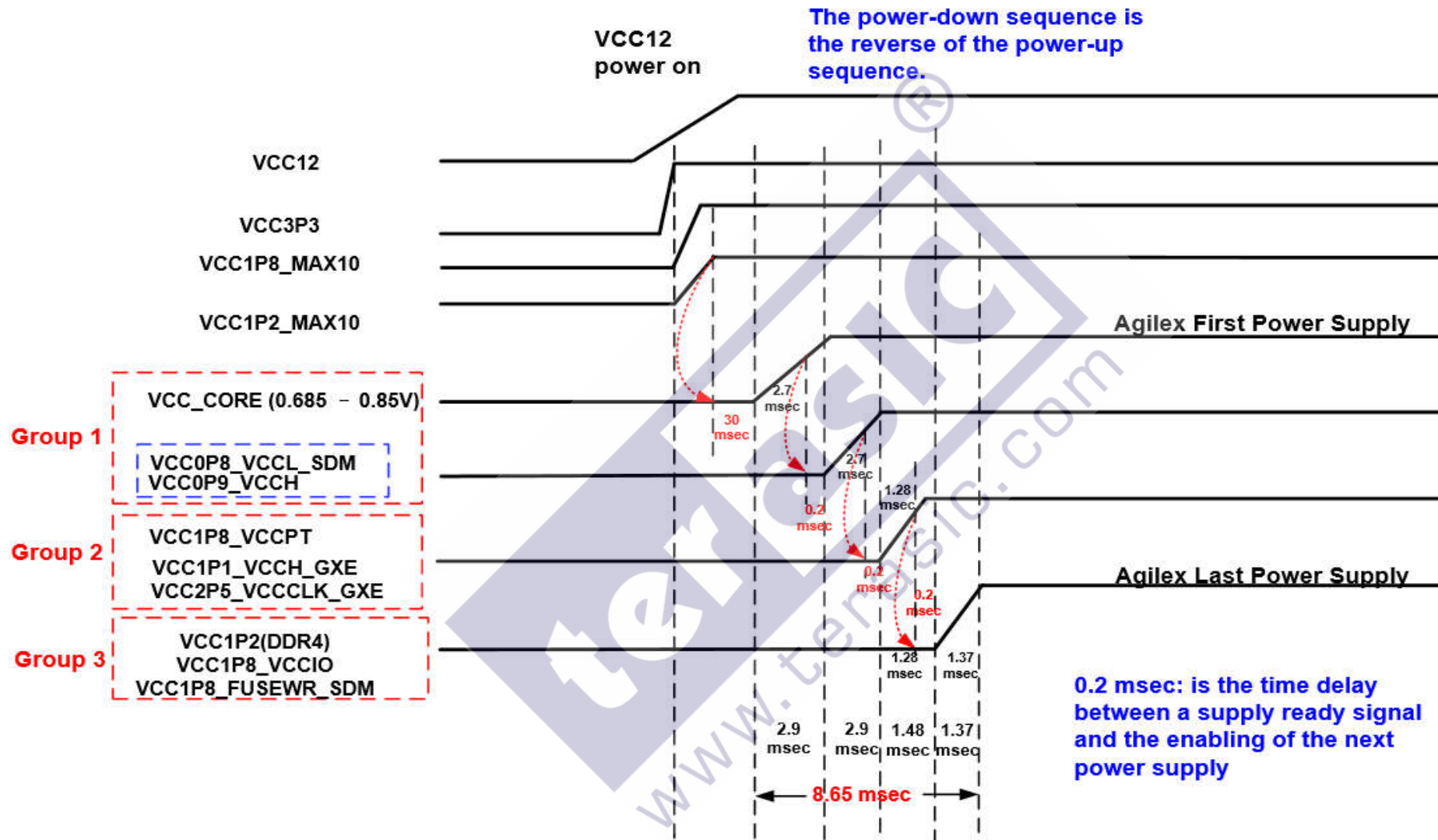
# FPGA Temperature Control and Monitor (by System MAX)



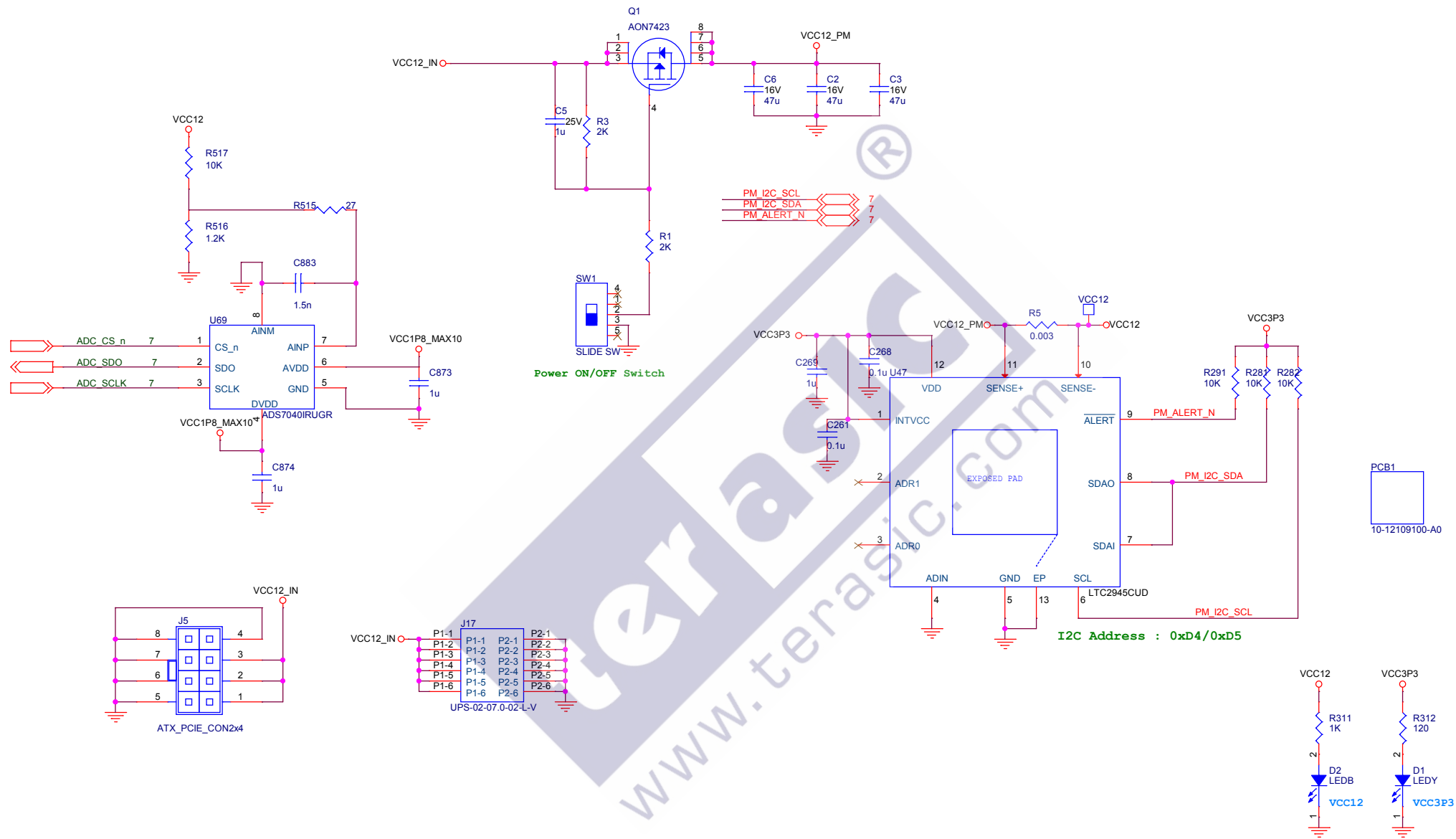
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Title		
Agilex SOM		
Size	Document Number	Rev
B	FAN Control and Temperature Monitor	A
Date:	Thursday, June 02, 2022	Sheet 41 of 51



# Agilex Power-up Sequence Design Diagram

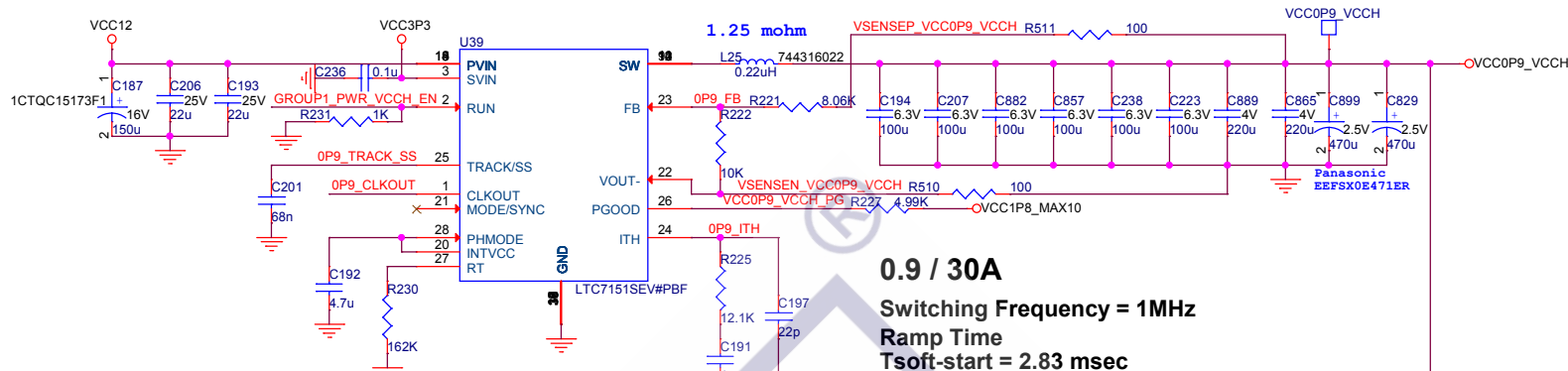






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Title		
Agilex SOM		
Size	Document Number	Rev
B	Power - 12 V Power Input, Power Monitor, ADC	A
Date:	Thursday, June 02, 2022	Sheet 44 of 51

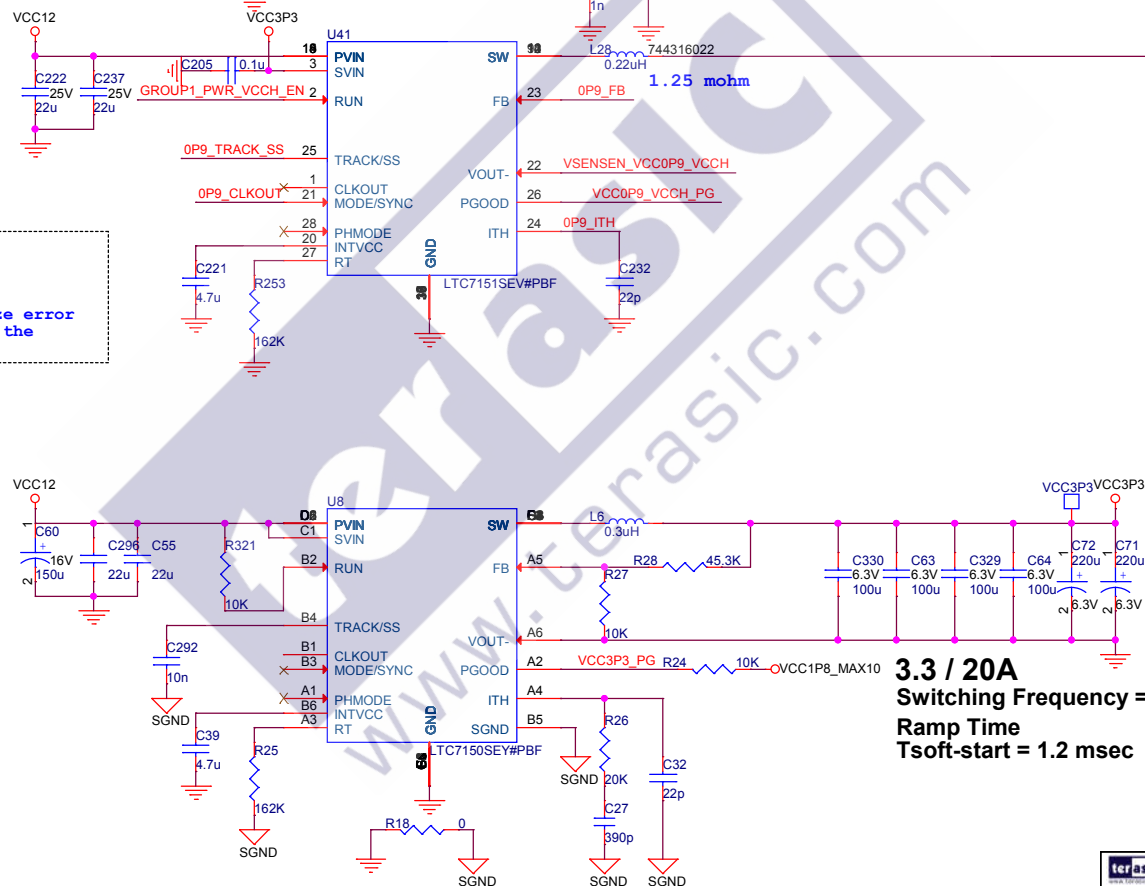
GROUP1\_PWR\_VCCH\_EN 7,47,51  
VCC0P9\_VCCH\_PG 7  
VCC3P3\_PG 7



**0.9 / 30A**  
Switching Frequency = 1MHz  
Ramp Time  
Tsoft-start = 2.83 msec

VSENSEP\_VCC0P9\_VCCH 21  
VSENSEN\_VCC0P9\_VCCH 21

Connect the point near the load in order to minimize error incurred by voltage drop across the metal trace of the board

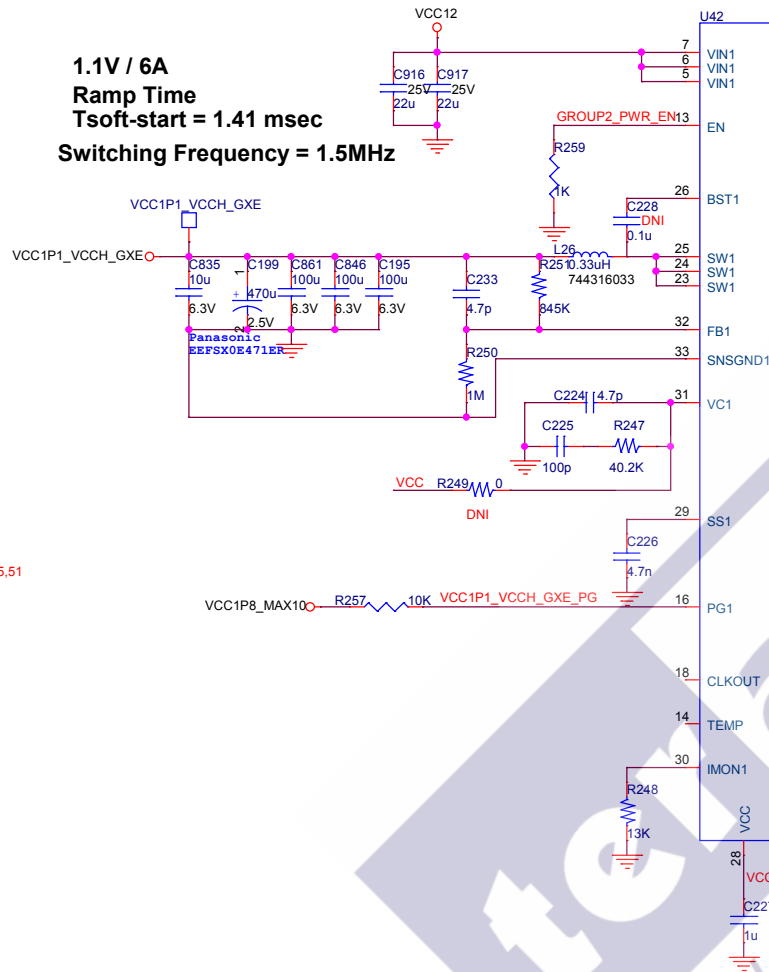


**3.3 / 20A**  
Switching Frequency = 1MHz  
Ramp Time  
Tsoft-start = 1.2 msec

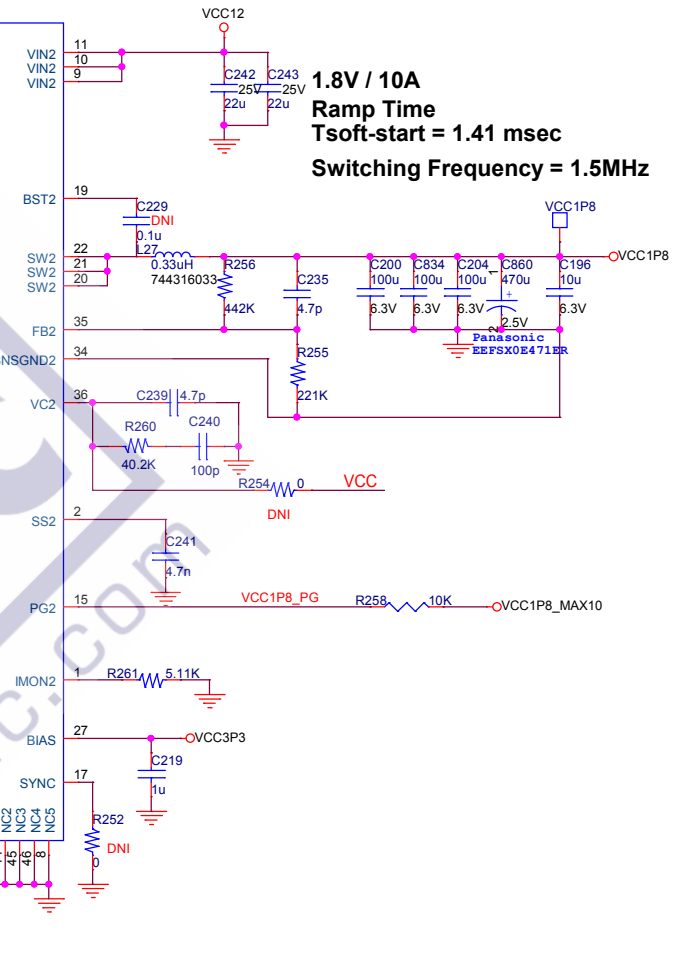
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Title		
Agilex SOM		
Size	Document Number	Rev
B	Power - 3.3V and 0.9V	A
Date:	Thursday, June 02, 2022	Sheet 45 of 51



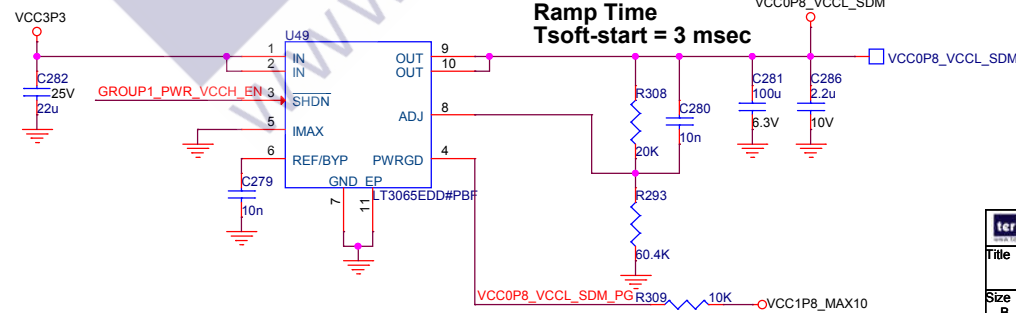
**1.1V / 6A**  
**Ramp Time**  
**Tsoft-start = 1.41 msec**  
**Switching Frequency = 1.5MHz**



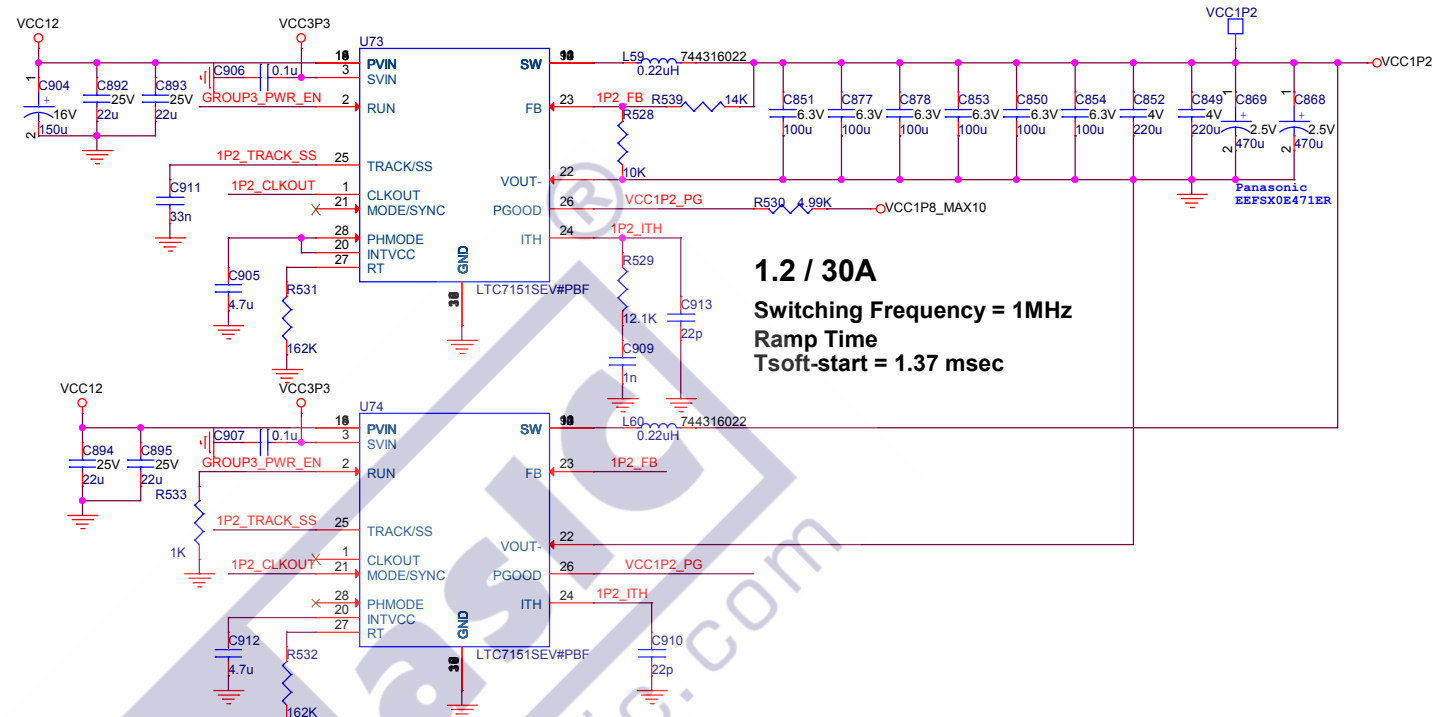
**1.8V / 10A**  
**Ramp Time**  
**Tsoft-start = 1.41 msec**  
**Switching Frequency = 1.5MHz**



**0.8V / 0.5A**  
**Ramp Time**  
**Tsoft-start = 3 msec**



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Title		
<b>Agilex SOM</b>		
Size	Document Number	Rev
B	Power - 0.8V, 1.1V, 1.8V	A
Date:	Thursday, June 02, 2022	Sheet 47 of 51

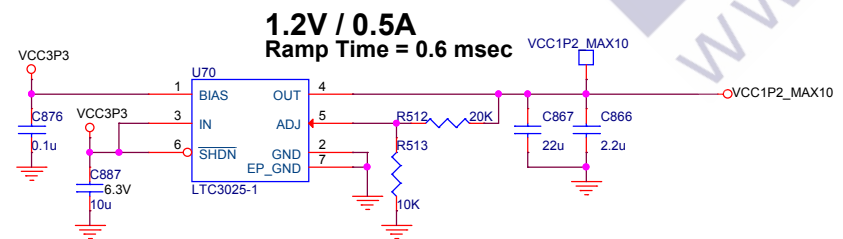
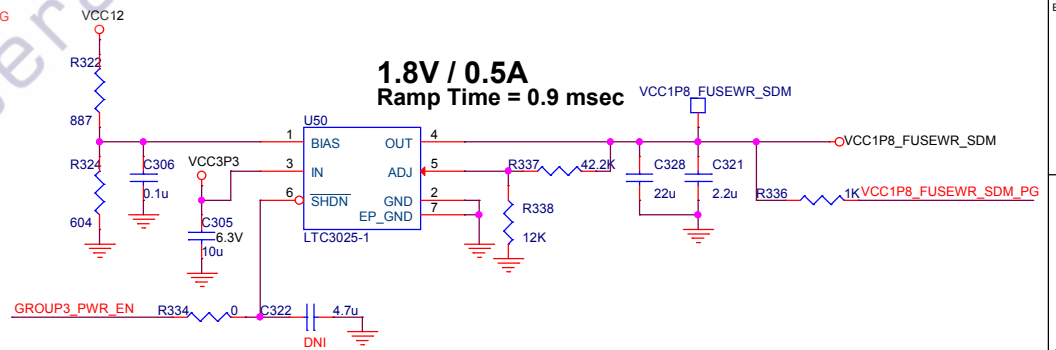
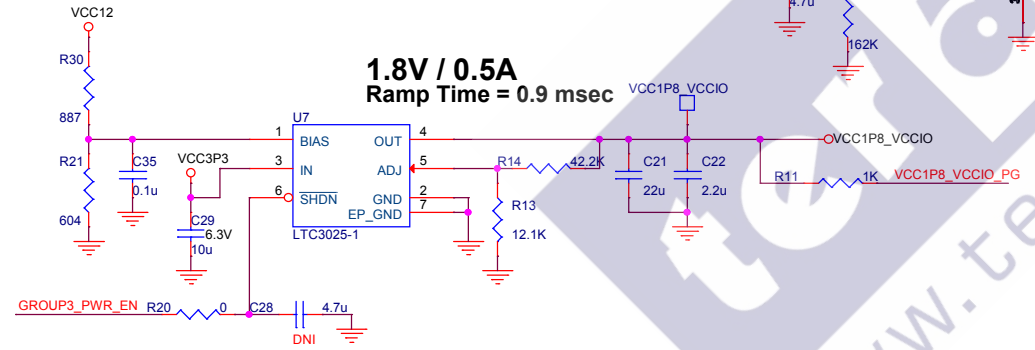


6.50,51 GROUP3\_PWR\_EN

7 VCC1P2\_PG

7 VCC1P8\_VCCIO\_PG

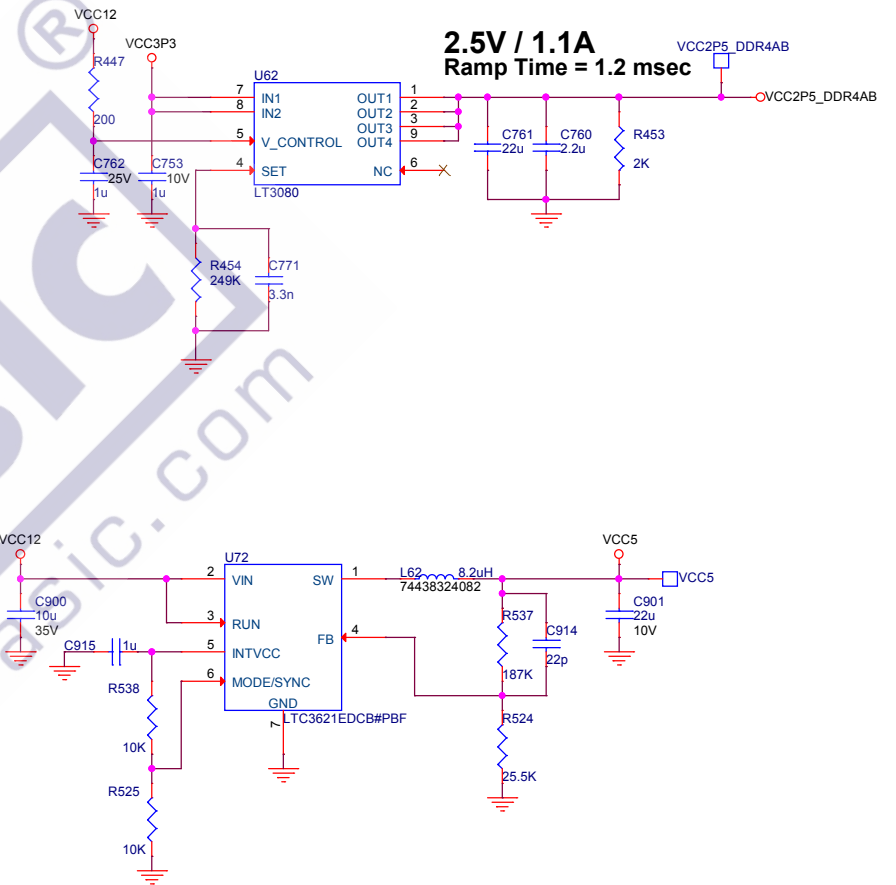
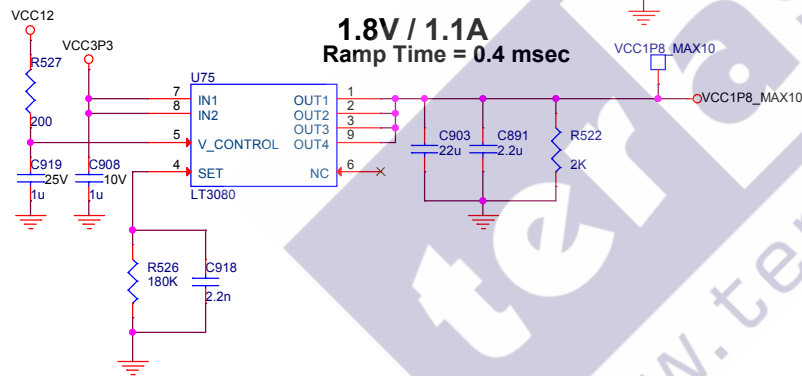
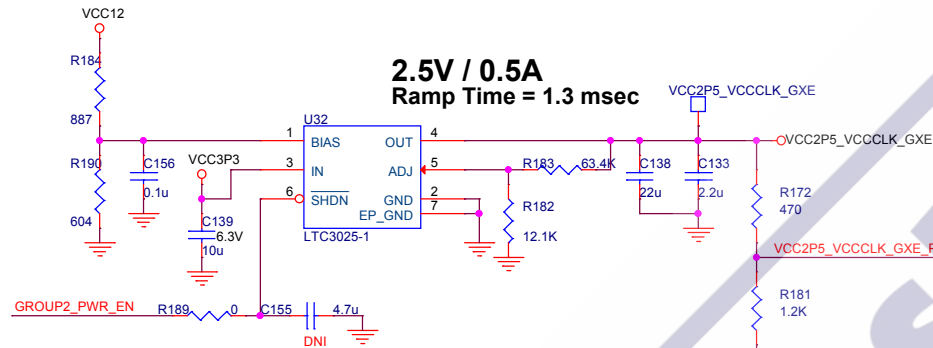
7 VCC1P8\_FUSEWR\_SDM\_PG






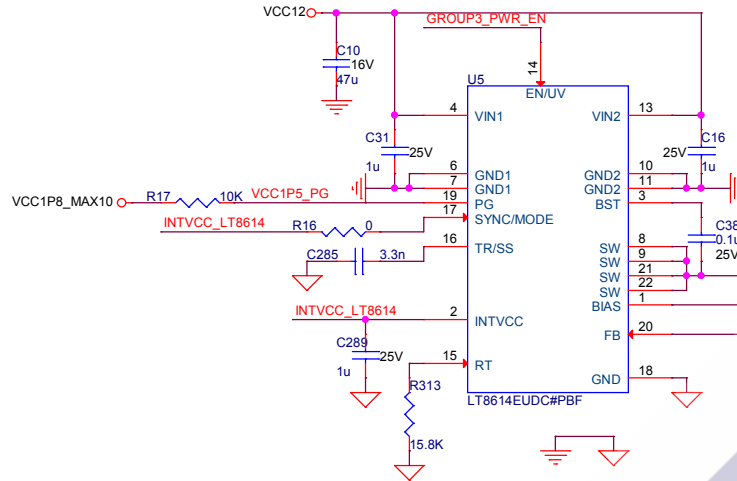
GROUP2\_PWR\_EN 6.47.51

VCC2P5\_VCCCLK\_GXE\_PG 7

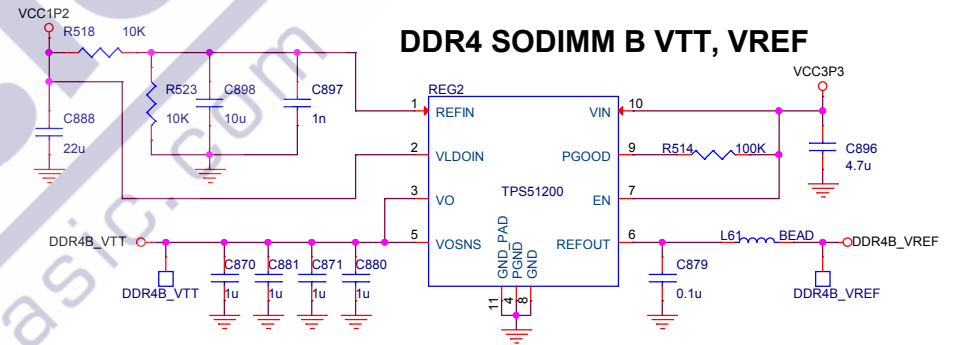
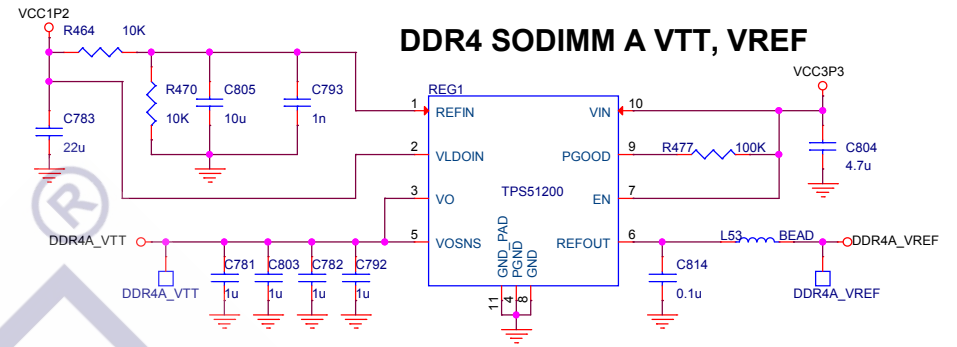


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Title			
Agilex SOM			
Size	Document Number		Rev
B	Power - 1.8V, 2.5V, 5V		A
Date:	Thursday, June 02, 2022	Sheet	49 of 51

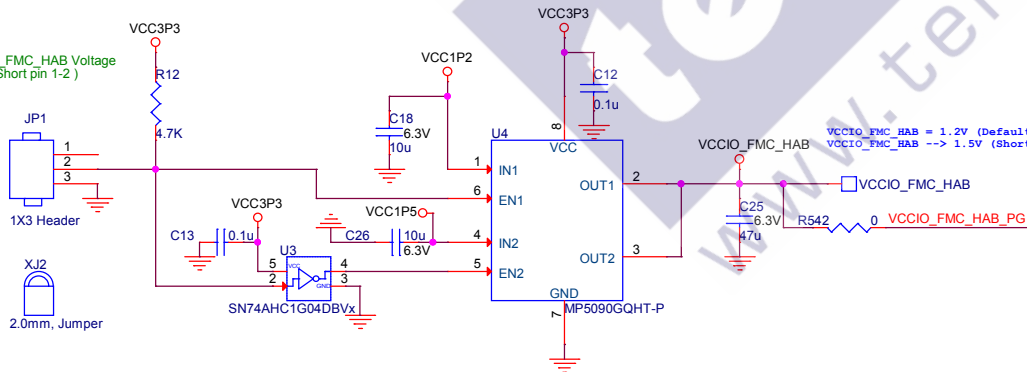
6,48,51 → GROUP3\_PWR\_EN  
7 → VCCIO\_FMC\_HAB\_PG



**1.5V / 4A**  
Ramp Time  
Tsoft-start = 1.46 msec  
Switching Frequency = 2.2MHz



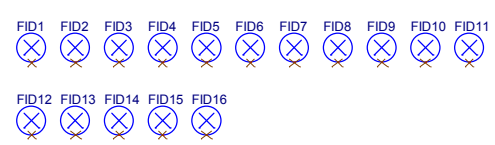
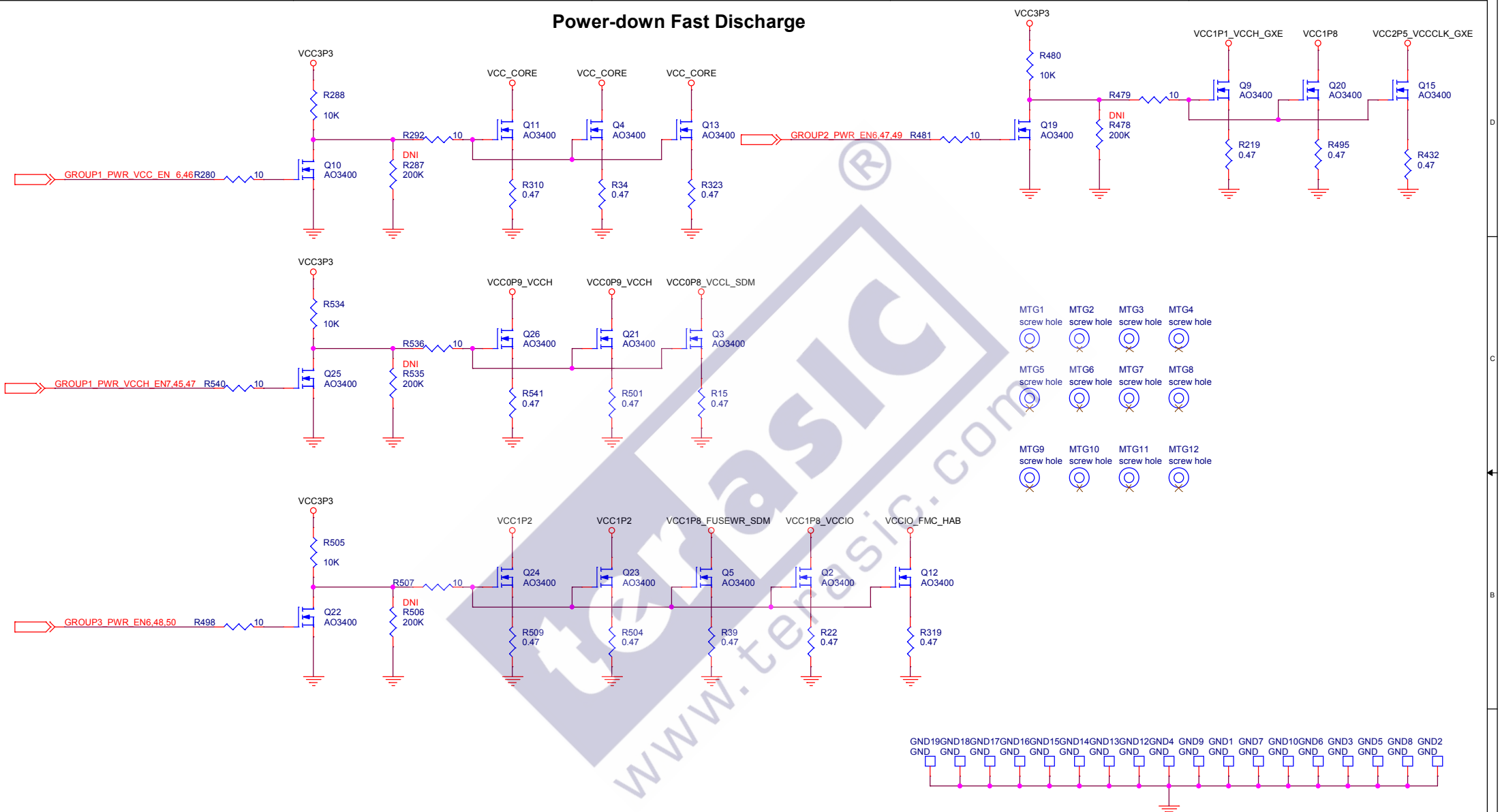
JP3 Set VCCIO\_FMC\_HAB Voltage  
Default : 1.2V (Short pin 1-2)  
1-2 : 1.2V  
2-3 : 1.5V



VCCIO\_FMC\_HAB = 1.2V (Default Setting, Short JP3-1/2)  
VCCIO\_FMC\_HAB --> 1.5V (Short JP3-2/3)

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# Power-down Fast Discharge



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