

## 32 kHz TO 156.25 MHz CMOS MEMS OSCILLATOR

### Features

- Wide frequency range: 32 kHz to 125 MHz, 130.25 to 156.25 MHz
- Multiple stability options:  $\pm 20$ ,  $\pm 30$ ,  $\pm 50$  ppm
- LVCMOS/LVTTL output
- Low phase jitter: 1.0 ps rms (typ)
- Low period jitter: 1.1 ps rms (typ)
- Continuous supply voltage range: +1.71 V to +3.63 V
- Low power: 1.77 mA (typ)
- No internal PLL
- Output enable
- Selectable power management options including: fast start, low power, and sleep
- User selectable  $T_R/T_F$  options: 0.7, 1.3, 2.5, 5, 10 ns (typ)
- Glitchless start and stop
- High PSRR
- Excellent short-term stability, long-term aging
- Significantly lower FIT rate than quartz XOs
- Industry standard footprint: 2x2.5, 3.2x5, 5x7 mm
- RoHS compliant, Pb-free
- Short lead times: <2 weeks
- $-40$  to  $+85$  °C,  $-20$  to  $+70$  °C options

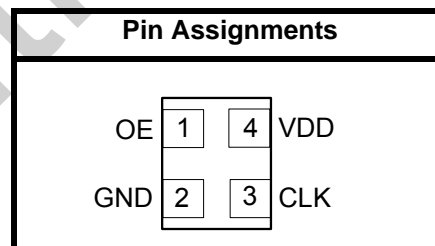
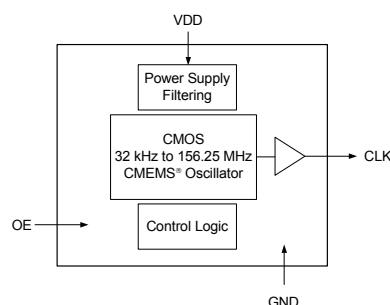
### Applications

- Portable media players
- Digital cameras
- Digital camcorders
- Handheld gaming consoles
- Portable storage
- Portable medical devices
- Office automation
- Networking/Communications
- Embedded
- Industrial

### Description

The Si501 MEMS XO utilizes Silicon Laboratories' CMEMS<sup>®</sup> technology to provide frequencies from 32 kHz to 156.25 MHz. Unlike traditional crystal oscillators that require a custom crystal for each unique frequency, the Si501's CMEMS<sup>®</sup> based silicon oscillator technology is capable of producing any frequency across its operating range. CMEMS<sup>®</sup> eliminates the use of crystals, enhancing reliability and improving immunity to shock and vibration. In addition, the Si501 provides superior supply noise rejection, simplifying low jitter clock generation in noisy environments. The Si501 is individually factory-configured and production-tested to guarantee performance and reliability. The Si501 is available with short 2-week lead times.

### Functional Block Diagram



Patents pending

## 1. Electrical Specifications

**Table 1. Recommended Operating Conditions**
 $V_{DD}$  = 1.71 to 3.63 V,  $T_A$  = -40 to 85 °C, unless otherwise specified

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage <sup>1</sup>	$V_{DD}$		1.71	—	3.63	V
Dynamic Supply Current	$I_{DD1}$	$C_L$ = 4 pF, 3.3 $V_{DD}$ , $F_{CLK}$ = 1.0 MHz Low power option	—	1.77	TBD	mA
		$C_L$ = 4 pF, 3.3 $V_{DD}$ , $F_{CLK}$ = 156.25 MHz Low power option	—	6.5	TBD	
		$C_L$ = 4 pF, 3.3 $V_{DD}$ , $F_{CLK}$ = 1.0 MHz Low jitter option	—	4.2	TBD	
		$C_L$ = 4 pF, 3.3 $V_{DD}$ , $F_{CLK}$ = 156.25 MHz Low jitter option	—	8.9	TBD	
Static Supply Current <sup>2</sup>	$I_{DD2}$	OE = STOP, $F_{CLK}$ = 1 MHz Output disabled	—	1.74	TBD	mA
		OE = DOZE Output disabled Oscillator in low power mode	—	740	TBD	
		OE = SLEEP Output disabled Oscillator turned off	—	—	1	
Input High Voltage <sup>3</sup>	$V_{IH}$	OE pin	0.70 x $V_{DD}$	—	—	V
Input Low Voltage <sup>3</sup>	$V_{IL}$	OE pin	—	—	0.30 x $V_{DD}$	V
OE Internal Pull Up/Down Resistor <sup>3</sup>	$R_I$		—	50	—	k $\Omega$
Operating Temperature	$T_A$	Extended commercial grade	-20	—	70	°C
		Industrial grade	-40	—	85	

**Notes:**

1. The supply voltage range is continuous from 1.71 to 3.63 V.
2. The Si501 supports various power management orderable options. See Ordering Guide section for details.
3. Active high and active low polarity OE options available. See Ordering Guide section for details.

**Table 2. Output Clock Frequency Characteristics**V<sub>DD</sub>=1.71 to 3.6 V, T<sub>A</sub>= -40 to 85 °C, unless otherwise specified.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency Range	F <sub>CLK</sub>		0.032	—	125	MHz
			130.25	—	156.25	
Total Stability*	F <sub>STAB</sub>	T <sub>A</sub> = −20 to 70 °C	−20	—	+20	ppm
		T <sub>A</sub> = −20 to 70 °C, −40 to 85 °C	−30	—	+30	
		T <sub>A</sub> = −20 to 70 °C, −40 to 85 °C	−50	—	+50	
Startup Time	T <sub>SU</sub>	Start time to 1st clock. See Figure 4 for more details.	—	—	5	ms
Resume Time	T <sub>RUN</sub>	From sleep mode	—	—	5	ms
		From doze mode	—	—	2.55	
		From stop mode	—	—	1.5 x T <sub>CLK</sub> + 35	ns
Output Disable Time	T <sub>D</sub>	To sleep/doze mode, from output running	—	—	225	μs
		Stop	—	—	1.5 x T <sub>CLK</sub> + 35	ns
<b>*Note:</b> Factory configurable. Stability budget consists of initial tolerance, operating temperature range, rated power supply voltage change, load change, aging (10 yr aging at 40°C), shock and vibration.						

**Table 3. Output Clock Levels and Symmetry** $V_{DD}=1.71$  to  $3.63V$ ,  $T_A=-40$  to  $85^{\circ}C$ , unless otherwise specified

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
CMOS Output Logic High	$V_{OH}$	1 <sup>st</sup> ordering option code: A and H $I_{OH} = -4$ mA	$0.90 \times V_{DD}$	—	—	V
CMOS Output Logic Low	$V_{OL}$	1 <sup>st</sup> ordering option code: A and H $I_{OL} = +4$ mA	—	—	$0.10 \times V_{DD}$	V
CMOS Rise/Fall Time*	$T_R / T_F$	1 <sup>st</sup> ordering option code: A and H	TBD	0.7	TBD	ns
		1 <sup>st</sup> ordering option code: B and J $Z_O=50\Omega@1.8V$	TBD	1.3	TBD	
		1 <sup>st</sup> ordering option code: C and K $Z_O=50\Omega@2.5V$	TBD	1.3	TBD	
		1 <sup>st</sup> ordering option code: D and L $Z_O=50\Omega@3.3V$	TBD	1.3	TBD	
		1 <sup>st</sup> ordering option code: E and M	TBD	2.5	TBD	
		1 <sup>st</sup> ordering option code: F and N	TBD	5	TBD	
		1 <sup>st</sup> ordering option code: G and P	TBD	10	TBD	
Duty Cycle	DC	Drive strength selected such that 20/80% ( $T_R$ and $T_F$ ) <10% of period	45	50	55	%

**\*Note:**  $C_L=15$  pF, 20/80%

**Table 4. Output Clock Jitter and Phase Noise**V<sub>DD</sub>=1.71 to 3.63 V, T<sub>A</sub>=−40 to 85 °C, unless otherwise specified.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Phase Jitter <sup>1</sup>	$\phi$	3.3 V F <sub>OFFSET</sub> =1.875 MHz to F <sub>CLK</sub> /2 Low Jitter Option 1 <sup>st</sup> ordering option code: H	—	1.0	TBD	ps rms
		3.3 V F <sub>OFFSET</sub> =1.875 MHz to F <sub>CLK</sub> /2 Low Power Option 1 <sup>st</sup> ordering option code: A		2.4	TBD	
Period Jitter <sup>2</sup>	J <sub>PRMS</sub>	3.3 V Low Jitter Option 1 <sup>st</sup> ordering option code: H	—	1.1	TBD	ps rms
		3.3 V Low Power Option 1 <sup>st</sup> ordering option code: A	—	2.4	TBD	
Period Jitter <sup>2</sup>	J <sub>PPKPK</sub>	3.3 V Low Jitter Option 10K samples 1 <sup>st</sup> ordering option code: H	—	TBD	TBD	ps pk-pk
		3.3 V Low Power Option 10K samples 1 <sup>st</sup> ordering option code: A	—	TBD	TBD	
Additive RMS Jitter Due to External Power Supply Noise <sup>3</sup>	J <sub>PSR</sub>	10 kHz sinusoidal noise	—	TBD	—	ps rms
		100 kHz sinusoidal noise	—	TBD	—	
		500 kHz sinusoidal noise	—	TBD	—	
		1 MHz sinusoidal noise	—	TBD	—	

**Notes:**

1. Applies to output frequencies: 100, 106.25, 125, 148.35165, 148.5, 150, 155.52, 156.25 MHz.
2. Applies to output frequencies: 74.17582, 74.25, 75, 77.76, 106.25, 125, 148.35165, 148.5, 150, 155.52, 156.25 MHz.
3. F<sub>CLK</sub> = 156.25 MHz. Increase in jitter on output clock due to +50 mVpp sine wave noise added to VDD = 3.3 V. Refer to AN491. 1<sup>st</sup> ordering option code: A or H, T<sub>R</sub>/T<sub>F</sub>=0.7 ns.

Table 5. Environmental Compliance and Package Information

Parameter	Test Condition
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Temperature cycle	JESD22, Method A104
Resistance to solder heat	MIL-STD-883, Method 2036
Moisture sensitivity level	3
Contact pads	TBD

Table 6. Thermal Conditions

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance Junction to Ambient	$\theta_{JA}$	5x7 mm <sup>2</sup> , still air	TBD	°C/W
		3.2x5 mm <sup>2</sup> , still air	TBD	
		2x2.5 mm <sup>2</sup> , still air	TBD	

Table 7. Absolute Maximum Limits<sup>1</sup>

Parameter	Symbol	Rating	Unit
Maximum Operating Temperature	$T_{MAX}$	85	°C
Storage Temperature	$T_S$	–55 to +125	°C
Supply Voltage	$V_{DD}$	–0.5 to +3.8	V
Input Voltage	$V_{IN}$	–0.5 to $V_{DD}$ +0.3V	V
ESD Sensitivity (JESD22-A114)	HBM	2000	V
ESD Sensitivity (CDM)	CDM	500	V
Soldering Temperature (Pb-free profile) <sup>2</sup>	$T_{PEAK}$	260	°C
Soldering Temperature at $T_{PEAK}$ (PB-free profile) <sup>2</sup>	$T_P$	20–40	s
Maximum Junction Temperature	$T_J$	125	°C
<b>Notes:</b> <ol style="list-style-type: none"> <li>Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.</li> <li>The device is compliant with JEDEC J-STD-020.</li> </ol>			

## 2. Typical Applications Circuit

### 2.1. Fast Rise/Fall Time with Series Termination Resistor Eliminated

1st ordering option codes: B, C, D, J, K, and L

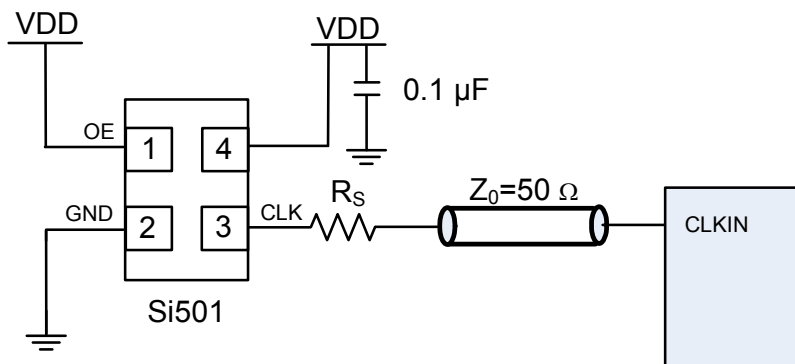


Figure 1. Si501 with Series Termination Resistor Eliminated

### 2.2. Fast Rise/Fall Time with Series Termination Resistor

1st ordering option codes: A and H

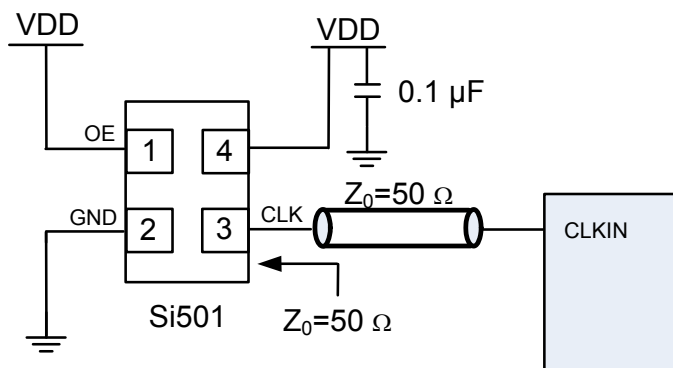


Figure 2. Si501 with Series Termination Resistor

### 2.3. Slow Rise/Fall Time (EMI Reduction)

1st ordering option codes: E, F, G, M, N, and P

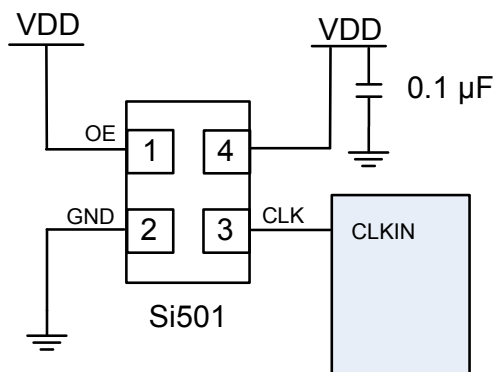


Figure 3. Si501 with Slow Rise/Fall Time

## 3. Functional Description

### 3.1. AC Waveforms

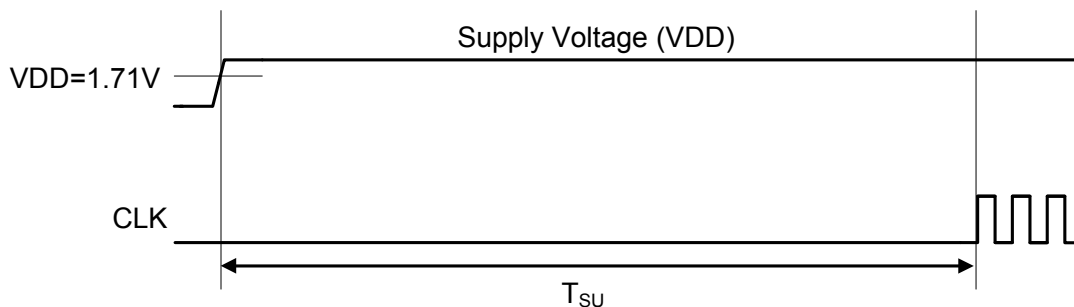


Figure 4. Power On Time

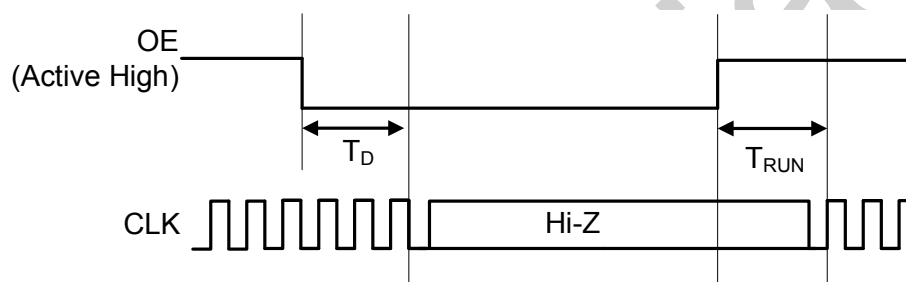


Figure 5. AC Waveform

### 3.2. Output Enable, Power-Down, and Wake Time

Table 8. Output Enable and Power Mode

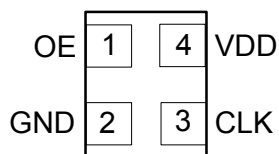
Power Mode	Output Disable State	Internal Oscillator State	Maximum Wake Time	Maximum CLK Disable Time
Stop	Hi-Z	On	$1.5 \times T_{CLK} + 35 \text{ ns}$	$1.5 \times T_{CLK} + 35 \text{ ns}$
Doze	Hi-Z	On (Low power mode)	2.55 ms	225 $\mu\text{s}$
Sleep	Hi-Z	Off	5 ms	225 $\mu\text{s}$

#### Notes:

1. If OE changes value, the new value must stay stable for the maximum duration of the event the OE change invoked (T<sub>RUN</sub> time for different modes).
2.  $T_{CLK} = 1/F_{CLK}$



## 4. Pin Descriptions



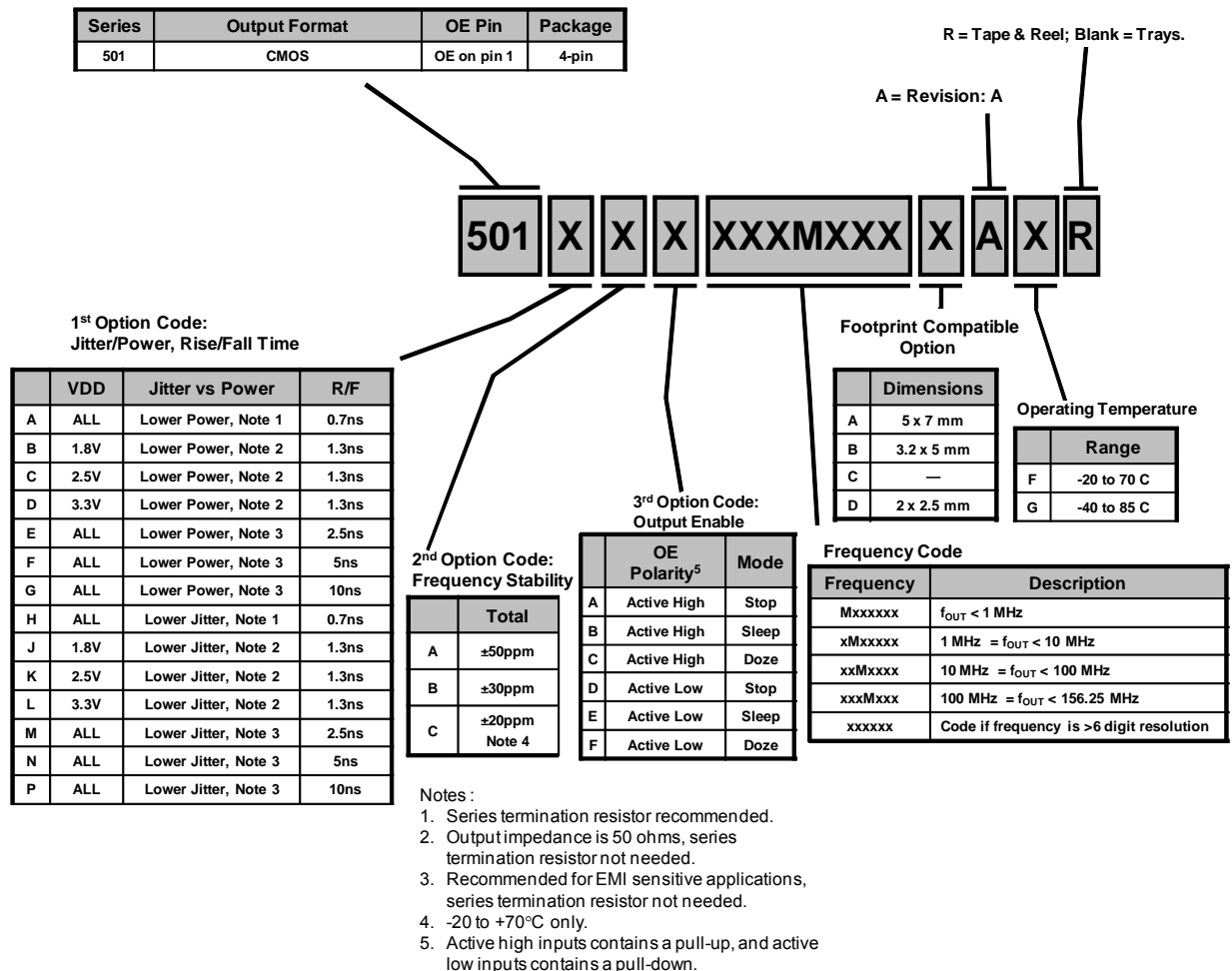
**Figure 6. Si501**

**Table 9. Pin Description**

Pin	Name	Function
1	OE	Output enable. When OE is disabled, the output enters into Hi-Z after completing the last cycle glitch-free. When OE is enabled, the output is active. OE supports multiple factory-customized power-down options including stop, doze, and sleep. Active high and active low options are available. See the Ordering Guide section for details.
2	GND	Ground.
3	CLK	Output clock.
4	V <sub>DD</sub>	Power supply. Bypass with a 0.1μF capacitor placed as close to the V <sub>DD</sub> pin as possible.

## 5. Ordering Guide

The Si501 supports a wide variety of configuration options including frequency, stability, jitter/power, rise/fall time, and multiple power-down states. Specific device configurations are programmed at time of shipment. Configurations can be specified using the Part Number Configuration chart below. A web-based utility will be available to simplify device customization. The Si501 CMEMS<sup>®</sup> XO series is supplied in industry-standard, RoHS compliant, lead-free 5x7, 3.2x5, and 2x2.5 mm footprints. Tape and reel packaging is an ordering option.



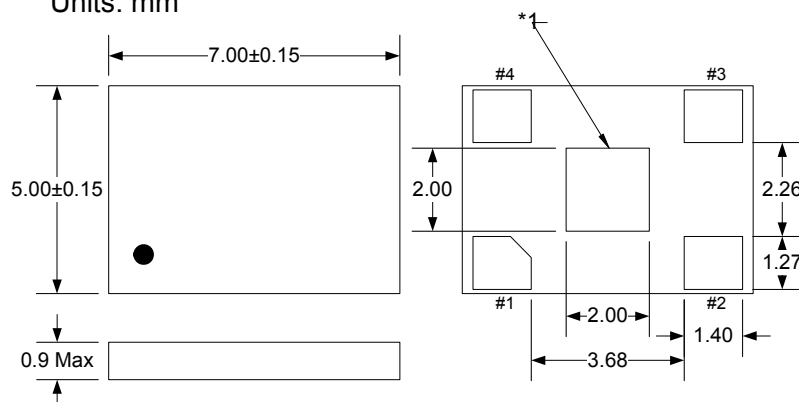
**Figure 7. Part Number Syntax**

Example of an orderable part number: 501AAA156M250AAGR represents a -40 to +85°C, 1.8 to 3.3V, 156.25 MHz ± 50 ppm 5 x 7 mm LVCMOS MEMS XO with active high output enable.

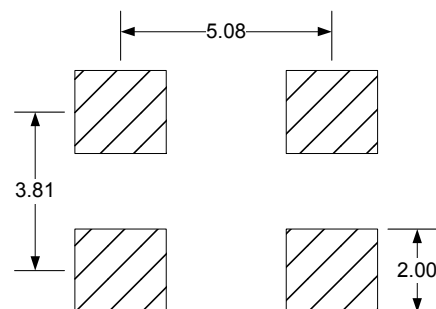
## 6. Package Outline

### Package Dimensions:

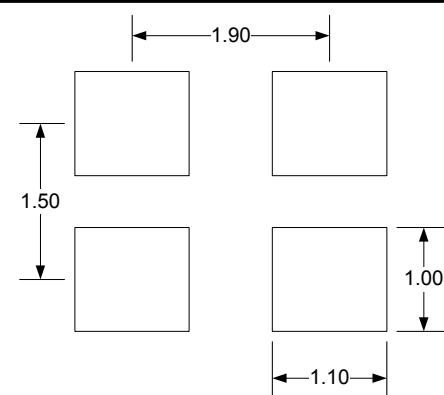
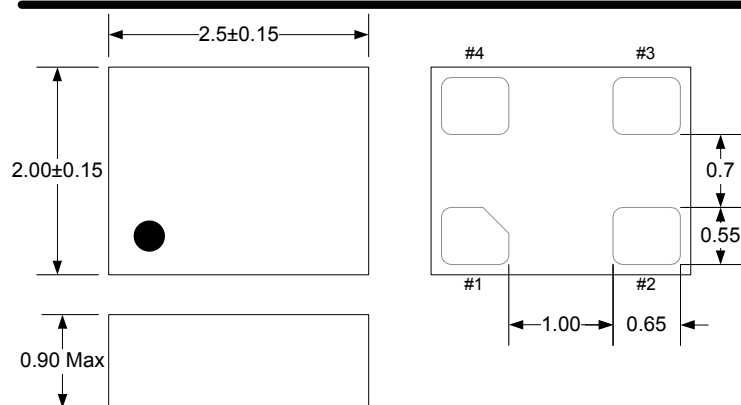
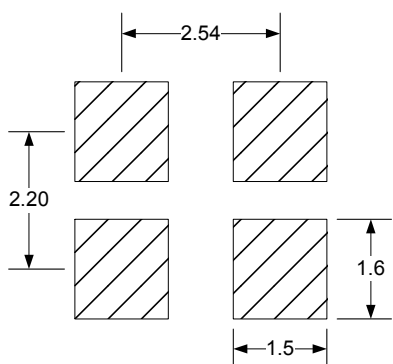
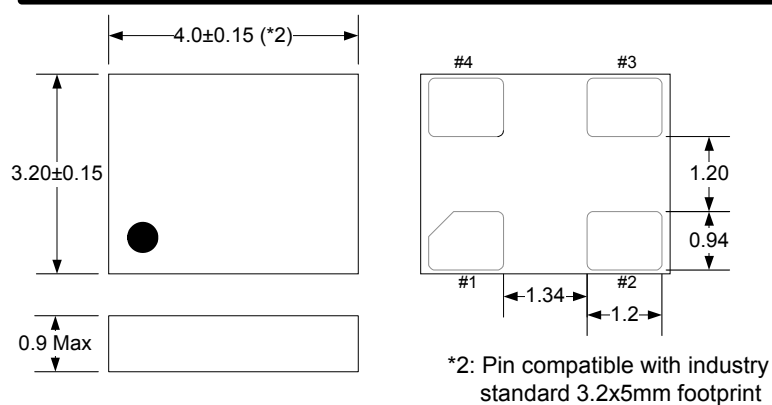
Units: mm



Recommended Land Pattern:

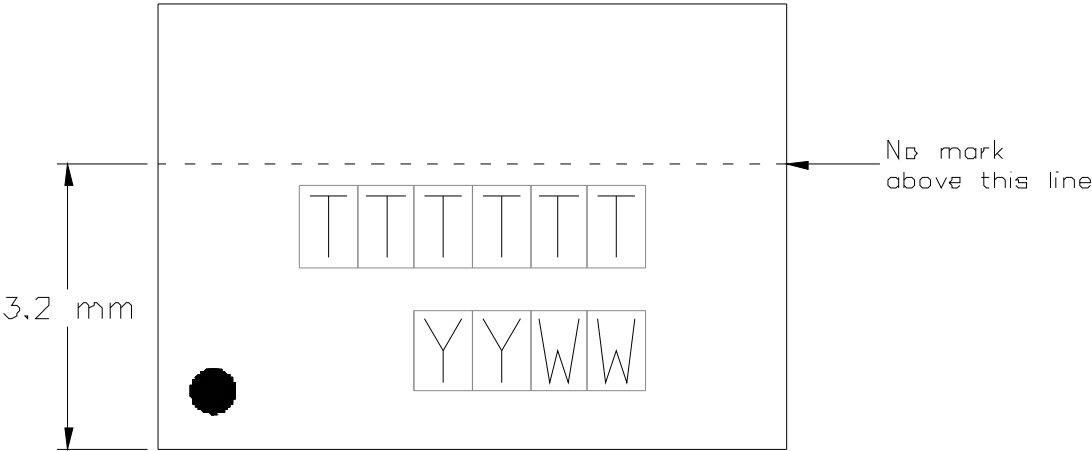


\*1:Float die paddle. Floating die paddle does not affect performance or functionality.



7. Top Markings

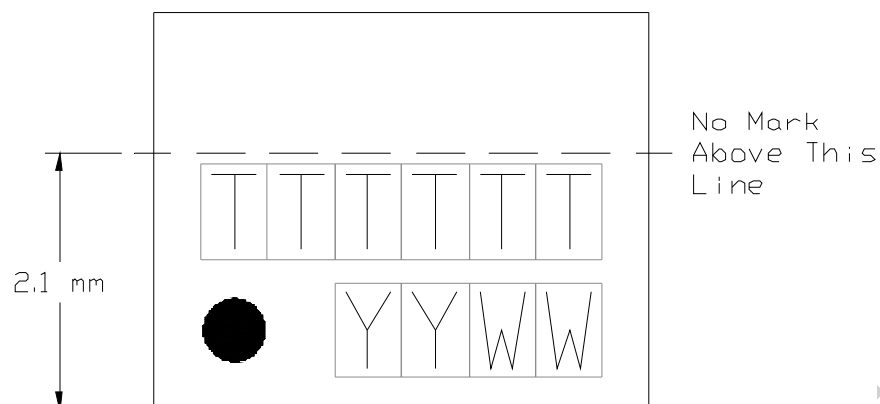
7.1. 7.0 x 5.0 Top Marking



7.2. 7.0 x 5.0 Top Marking Explanation

<b>Mark Method:</b>	Laser	
<b>Font Size:</b>	2.0 Point (28 mils) Right-Justified	
<b>Line 1 Marking:</b>	TTTTTT=Mfg Code	Manufacturing Code from the Assembly Purchase Order form.
<b>Line 2 Marking</b>	Circle=0.5 mm Diameter Lower-Left Justified	Pin 1 Identifier
	YY=Year WW=Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the assembly release.

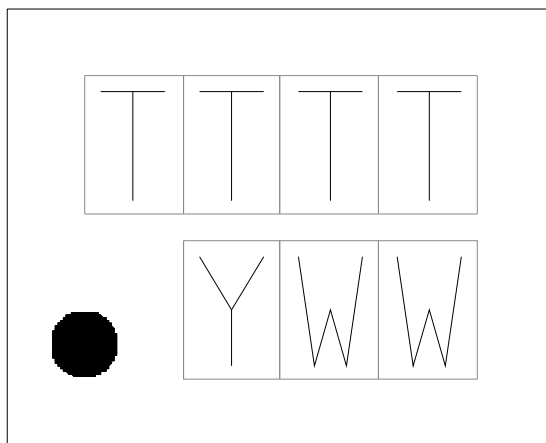
### 7.3. 3.2 x 4.0 Top Marking



### 7.4. 3.2 x 4.0 Top Marking Explanation

<b>Mark Method:</b>	Laser	
<b>Font Size:</b>	0.60mm Right-Justified	
<b>Line 1 Marking:</b>	TTTTTT=Trace Code	Manufacturing Code from the Assembly Purchase Order form.
<b>Line 2 Marking:</b>	Circle=0.5 mm Diameter Left-Justified	Pin 1 Indicator
	YY=Year WW=Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the build date.

## 7.5. 2.0 x 2.5 Top Marking



## 7.6. 2.0 x 2.5 Top Marking Explanation

<b>Mark Method:</b>	Laser	
<b>Font Size:</b>	0.50 mm Right-Justified	
<b>Line 1 Marking:</b>	TTTT=Trace Code	Last 4 digits of Manufacturing Code from the Assembly Purchase Order form.
<b>Line 2 Marking:</b>	Circle=0.3mm Diameter Left-Justified	Pin 1 Indicator
	Y=Year WW=Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the build date.

**NOTES:**

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## CONTACT INFORMATION

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