

U14-4

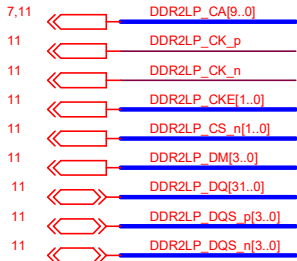
CYCLONE V GX BANK 3

Bank 3B VCCIO = 1.2V

GND	T9	IO_3B/DIFFIO_TX_B9P/DQ2B	IO_3B/DIFFIO_TX_B17P/DQ3B	V10	SW6
SW4	W11	IO_3B/DIFFIO_TX_B9N/GND	IO_3B/DIFFIO_TX_B17N/GND	V9	GND
SW8	Y11	IO_3B/DIFFIO_RX_B10P/DQ2B	IO_3B/DIFFIO_RX_B18P/DQ3B	AD8	
DDR2LP_CS_n0	R11	IO_3B/DIFFIO_RX_B10N/DQ2B	IO_3B/DIFFIO_RX_B18N/DQ3B	AE8	
DDR2LP_CS_n1	T11	IO_3B/DIFFIO_RX_B11P/DQS2B/B_CSN_0	IO_3B/DIFFIO_RX_B19P/DQS3B/B_CK	N10	DDR2LP_CK_p
SW5	AB10	IO_3B/DIFFIO_RX_B11N/DQSN2B/B_CSN_1	IO_3B/DIFFIO_RX_B19N/DQSN3B/B_CKN	P10	DDR2LP_CK_n
SW7	AC10	IO_3B/DIFFIO_TX_B12P	IO_3B/DIFFIO_TX_B20P/B_CA_6	AE9	DDR2LP_CA6
SW0	AC9	IO_3B/DIFFIO_TX_B12N/DQ2B	IO_3B/DIFFIO_TX_B20N/DQ3B/B_CA_7	AF9	DDR2LP_CA7
SW3	AC8	IO_3B/DIFFIO_TX_B13P/DQ2B			
DDR2LP_CA8	AB12	IO_3B/DIFFIO_TX_B13N/DQ2B	IO_3B/DIFFIO_RX_B22P/DQ3B/B_CA_0	U10	DDR2LP_CA4
DDR2LP_CA9	AB11	IO_3B/DIFFIO_RX_B14N/DQ2B/B_CA_8	IO_3B/DIFFIO_RX_B22N/DQ3B/B_CA_5	U11	DDR2LP_CA5
		IO_3B/DIFFIO_RX_B14N/DQ2B/B_CA_9			
ADC_SDO	W10	IO_3B/DIFFIO_TX_B16P/DQ2B	IO_3B/DIFFIO_TX_B24P/DQ3B/B_CA_0	AE6	DDR2LP_CA0
ADC_SDI	Y10	IO_3B/DIFFIO_TX_B16N/DQ2B	IO_3B/DIFFIO_TX_B24N/DQ3B/B_CA_1	AF6	DDR2LP_CA1

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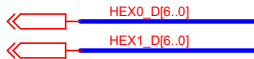
LPDDR2 Interface



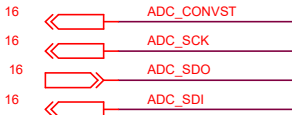
SWITCH



7-SEGMENT



ADC Interface



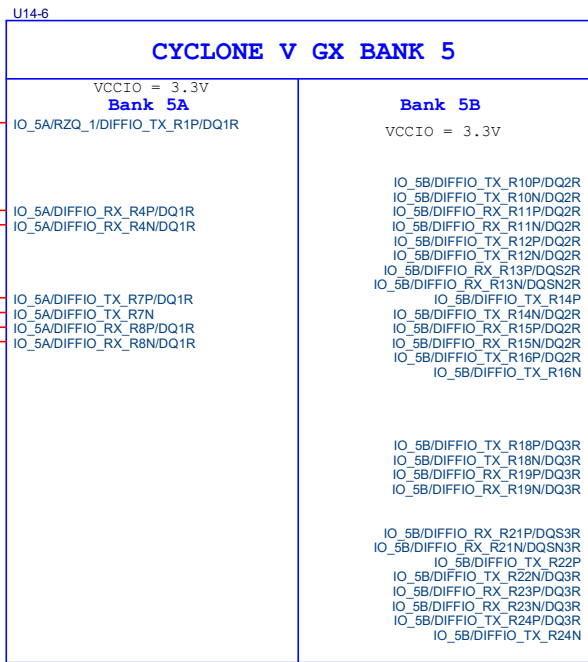
U14-5

CYCLONE V GX BANK 4

Bank 4A VCCIO = 1.2V

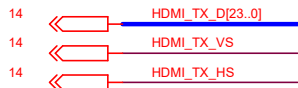
IO_4A/RZQ_0/DIFFIO_TX_B25N	IO_4A/DIFFIO_TX_B25P/DQ4B/B_DQ_2	IO_4A/DIFFIO_TX_B41P/DQ6B/B_DQ_18	AC18	DDR2LP_DQ18
		IO_4A/DIFFIO_TX_B41N/GND	AD17	GND
		IO_4A/DIFFIO_RX_B42P/DQ6B/B_DQ_17	AD17	DDR2LP_DQ17
		IO_4A/DIFFIO_RX_B42N/DQ6B/B_DQ_16	AD16	DDR2LP_DQ16
		IO_4A/DIFFIO_RX_B43P/DQ6B/B_DQ_2	V15	DDR2LP_DQS_p2
		IO_4A/DIFFIO_RX_B43N/DQ6B/B_DQSN_2	W15	DDR2LP_DQS_n2
		IO_4A/DIFFIO_TX_B44P/B_RESETN	AE19	SW9
		IO_4A/DIFFIO_TX_B44N/DQ6B/B_DQ_19	AF19	DDR2LP_DQ19
		IO_4A/DIFFIO_TX_B45P/DQ6B/B_DQ_22	AF21	DDR2LP_DQ22
		IO_4A/DIFFIO_TX_B45N/DQ6B/GND	AF22	GND
		IO_4A/DIFFIO_RX_B46P/DQ6B/B_DQ_21	AB17	DDR2LP_DQ21
		IO_4A/DIFFIO_RX_B46N/DQ6B/B_DQ_20	AC17	DDR2LP_DQ20
		IO_4A/DIFFIO_RX_B47P/GND	T17	GND
		IO_4A/DIFFIO_RX_B47N/GND	U17	GND
		IO_4A/DIFFIO_TX_B48P/DQ6B/B_DM_2	AE20	DDR2LP_DM2
		IO_4A/DIFFIO_TX_B48N/DQ6B/B_DQ_23	AE21	DDR2LP_DQ23
			AC20	DDR2LP_DQ26
			AD20	GND
			AE16	DDR2LP_DQ25
			AE15	DDR2LP_DQ24
			W16	DDR2LP_DQS_p3
			W17	DDR2LP_DQS_n3
			AD22	GND
			AD21	DDR2LP_DQ27
			AD23	DDR2LP_DQ30
			AE23	GND
			AF17	DDR2LP_DQ29
			AF16	DDR2LP_DQ28
			U15	GND
			U16	GND
			AE24	DDR2LP_DM3
			AF23	DDR2LP_DQ31
			AE25	HEX1_D4
			AF24	HEX1_D6
			Y18	HEX0_D6
			AA18	HEX1_D0
			V17	HEX0_D1
			W17	HEX0_D2
			AD26	HEX1_D1
			AE26	HEX1_D3
			AB19	HEX1_D2
			AC19	HEX1_D5
			Y20	HEX0_D4
			Y19	HEX0_D5
			V19	HEX0_D0
			W18	HEX0_D3
			AB22	ADC_CONVST
			AA21	ADC_SCK

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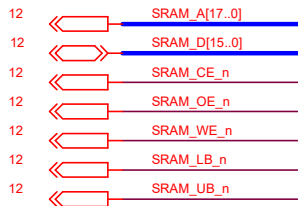


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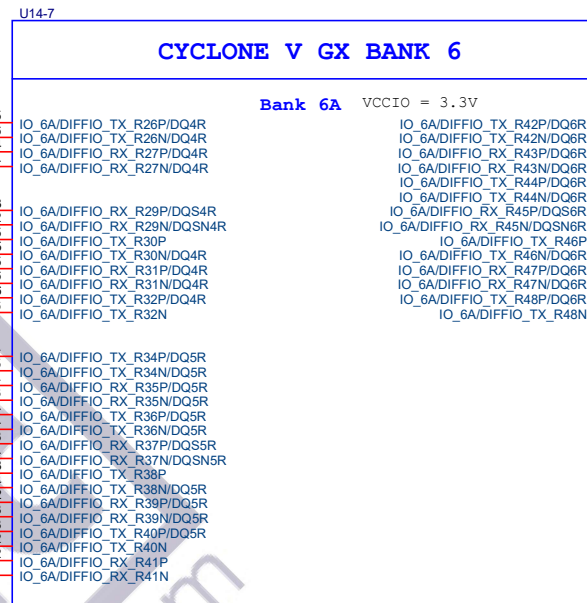
HDMI TX



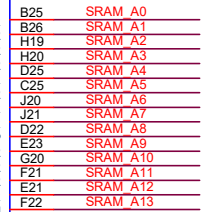
SRAM



GPIO



5CGXFC5C6F27C7N



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CYCLONE V GX BANK 7

Bank 7A VCCIO = 2.5V

IO_7A/RZQ_2/DIFFIO_TX_T40N

HSMC RX p4 H15
HSMC RX n4 J16
HSMC TX p11 C23
HSMC TX n11 C22
HSMC RX p16 B24
HSMC RX n16 A24
HSMC TX p13 A23
HSMC TX n13 A22
HSMC RX p2 H18
HSMC RX n2 H17
HSMC TX p7 B22
HSMC TX n7 A21
HSMC RX p15 D21
HSMC RX n15 D20
HSMC TX p16 B21
HSMC TX n16 B20
HSMC RX p6 G16
HSMC RX n6 G17

IO_7A/DIFFIO_RX_T1P/GND
IO_7A/DIFFIO_RX_T1N/GND
IO_7A/DIFFIO_TX_T2P/DQ1T/T_DM_4
IO_7A/DIFFIO_TX_T2N/DQ1T/T_DM_39
IO_7A/DIFFIO_RX_T3P/DQ1T/T_DQ_37
IO_7A/DIFFIO_RX_T3N/DQ1T/T_DQ_36
IO_7A/DIFFIO_TX_T4P/DQ1T/T_DQ_38
IO_7A/DIFFIO_TX_T4N/DQ1T/GND
IO_7A/DIFFIO_RX_T5P/DQS1T/T_DQS_4
IO_7A/DIFFIO_RX_T5N/DQSN1T/T_DQSN_4
IO_7A/DIFFIO_TX_T6P/GND
IO_7A/DIFFIO_TX_T6N/DQ1T/T_DQ_35
IO_7A/DIFFIO_RX_T7P/DQ1T/T_DQ_33
IO_7A/DIFFIO_RX_T7N/DQ1T/T_DQ_32
IO_7A/DIFFIO_TX_T8P/DQ1T/T_DQ_34
IO_7A/DIFFIO_TX_T8N/GND
IO_7A/DIFFIO_RX_T9P/GND
IO_7A/DIFFIO_RX_T9N/GND

HSMC TX p5 C20
HSMC TX n5 B19
HSMC RX p14 E20
HSMC RX n14 E19
HSMC TX p15 C19
HSMC TX n15 C18
HSMC RX p5 J12
HSMC RX n5 J11
HSMC CLKOUT p1 A19
HSMC CLKOUT n1 A18
HSMC RX p13 D18
HSMC RX n13 D17
HSMC CLKOUT p2 A17
HSMC CLKOUT n2 A16
HSMC D1 H14
HSMC D3 H13

5CGXFC5C6F27C7N

HSMC Interface

HSMC TX p[16..0]
HSMC TX n[16..0]
HSMC RX p[16..0]
HSMC RX n[16..0]
HSMC D[3..0]

HSMC Clock output

HSMC_CLKOUT_p[2..1]
HSMC_CLKOUT_n[2..1]

IO_7A/DIFFIO_TX_T18P/DQ3T/T_DM_2
IO_7A/DIFFIO_TX_T18N/DQ3T/T_DQ_23
IO_7A/DIFFIO_RX_T19P/DQ3T/T_DQ_21
IO_7A/DIFFIO_RX_T19N/DQ3T/T_DQ_20
IO_7A/DIFFIO_TX_T20P/DQ3T/T_DQ_22
IO_7A/DIFFIO_TX_T20N/DQ3T/GND
IO_7A/DIFFIO_RX_T21P/DQS3T/T_DQS_2
IO_7A/DIFFIO_RX_T21N/DQSN3T/T_DQSN_2
IO_7A/DIFFIO_TX_T22P/T_RESETN
IO_7A/DIFFIO_RX_T22N/DQ3T/T_DQ_19
IO_7A/DIFFIO_RX_T23P/DQ3T/T_DQ_17
IO_7A/DIFFIO_RX_T23N/DQ3T/T_DQ_16
IO_7A/DIFFIO_TX_T24P/DQ3T/T_DQ_18
IO_7A/DIFFIO_TX_T24N/GND

IO_7A/DIFFIO_TX_T26P/DQ4T/T_DM_1
IO_7A/DIFFIO_TX_T26N/DQ4T/T_DQ_15
IO_7A/DIFFIO_RX_T27P/DQ4T/T_DQ_13
IO_7A/DIFFIO_RX_T27N/DQ4T/T_DQ_12
IO_7A/DIFFIO_TX_T28P/DQ4T/T_DQ_14
IO_7A/DIFFIO_TX_T28N/DQ4T/T_CKE_0
IO_7A/DIFFIO_RX_T29P/DQS4T/T_DQS_1
IO_7A/DIFFIO_RX_T29N/DQSN4T/T_DQSN_1
IO_7A/DIFFIO_TX_T30P/T_CKE_1
IO_7A/DIFFIO_TX_T30N/DQ4T/T_DQ_11
IO_7A/DIFFIO_RX_T31P/DQ4T/T_DQ_9
IO_7A/DIFFIO_RX_T31N/DQ4T/T_DQ_8
IO_7A/DIFFIO_TX_T32P/DQ4T/T_DQ_10
IO_7A/DIFFIO_TX_T32N/GND

IO_7A/DIFFIO_TX_T34P/DQ5T/T_DM_0
IO_7A/DIFFIO_TX_T34N/DQ5T/T_DQ_7
IO_7A/DIFFIO_RX_T35P/DQ5T/T_DQ_5
IO_7A/DIFFIO_RX_T35N/DQ5T/T_DQ_4
IO_7A/DIFFIO_TX_T36P/DQ5T/T_DQ_6
IO_7A/DIFFIO_TX_T36N/DQ5T/T_ODT_1
IO_7A/DIFFIO_RX_T37P/DQS5T/T_DQS_0
IO_7A/DIFFIO_RX_T37N/DQSN5T/T_DQSN_0
IO_7A/DIFFIO_TX_T38P/T_ODT_0
IO_7A/DIFFIO_TX_T38N/DQ5T/T_DQ_3
IO_7A/DIFFIO_RX_T39P/DQ5T/T_DQ_1
IO_7A/DIFFIO_RX_T39N/DQ5T/T_DQ_0
IO_7A/DIFFIO_TX_T40P/DQ5T/T_DQ_2

C17 HSMC TX p14
B17 HSMC TX n14
E18 HSMC RX p8
F18 HSMC RX n8
A14 HSMC TX p12
B14 HSMC TX n12
L12 HSMC RX p3
K11 HSMC RX n3
B15 HSMC TX p6
C15 HSMC TX n6
C14 HSMC RX p11
D15 HSMC RX n11
A8 HSMC TX p9
A9 HSMC TX n9

C9 HSMC TX p1
B9 HSMC TX n1
E16 HSMC RX p12
D16 HSMC RX n12
D10 HSMC TX p2
C10 HSMC TX n2
N12 HSMC RX p0
M12 HSMC RX n0
B10 HSMC TX p4
A11 HSMC TX n4
F16 HSMC RX p9
E15 HSMC RX n9
E10 HSMC TX p0
E11 HSMC TX n0

B12 HSMC TX p10
A13 HSMC TX n10
G12 HSMC RX p7
F12 HSMC RX n7
A12 HSMC TX p3
B11 HSMC TX n3
M11 HSMC RX p1
L11 HSMC RX n1
C13 HSMC TX p8
C12 HSMC TX n8
E13 HSMC RX p10
D13 HSMC RX n10
D11 HSMC D0

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CYCLONE V GX BANK 8

Bank 8A VCCIO = 2.5V

IO_8A/DIFFIO_TX_T42P/DQ6T/T_CA_0
IO_8A/DIFFIO_TX_T42N/DQ6T/T_CA_1
IO_8A/DIFFIO_RX_T43P/DQ6T/T_CA_4
IO_8A/DIFFIO_RX_T43N/DQ6T/T_CA_5

IO_8A/DIFFIO_RX_T45P/DQS6T/T_CK
IO_8A/DIFFIO_RX_T45N/DQSN6T/T_CKN
IO_8A/DIFFIO_TX_T46P/T_CA_6
IO_8A/DIFFIO_TX_T46N/DQ6T/T_CA_7
IO_8A/DIFFIO_RX_T47P/DQ6T
IO_8A/DIFFIO_RX_T47N/DQ6T
IO_8A/DIFFIO_TX_T48P/DQ6T
IO_8A/DIFFIO_TX_T48N/GND

IO_8A/DIFFIO_TX_T50P/DQ7T
IO_8A/DIFFIO_TX_T50N/DQ7T
IO_8A/DIFFIO_RX_T51P/DQ7T/T_CA_8
IO_8A/DIFFIO_RX_T51N/DQ7T/T_CA_9
IO_8A/DIFFIO_TX_T52P/DQ7T
IO_8A/DIFFIO_TX_T52N/DQ7T
IO_8A/DIFFIO_RX_T53P/DQS7T/T_CSN_0
IO_8A/DIFFIO_RX_T53N/DQSN7T/T_CSN_1
IO_8A/DIFFIO_TX_T54P
IO_8A/DIFFIO_TX_T54N/DQ7T
IO_8A/DIFFIO_RX_T55P/DQ7T
IO_8A/DIFFIO_RX_T55N/DQ7T
IO_8A/DIFFIO_TX_T56P/DQ7T
IO_8A/DIFFIO_TX_T56N/GND

F6 LEDR1
G6 LEDR2
K8 LEDR7
J8 LEDR4
G7 LEDR3
F7 LEDR0
K10 LEDR6
J10 LEDR9
H7 LEDR8
J7 LEDR5
L7 LEDG0
K6 LEDG1
D8 LEDG2
E9 LEDG3

5CGXFC5C6F27C7N

Audio CODEC

AUD_XCK
AUD_BCLK
AUD_DACDAT
AUD_DACLCK
AUD_ADCCAT
AUD_ADCLCK

LED

LEDR[9..0]
LEDG[7..0]

UART to USB

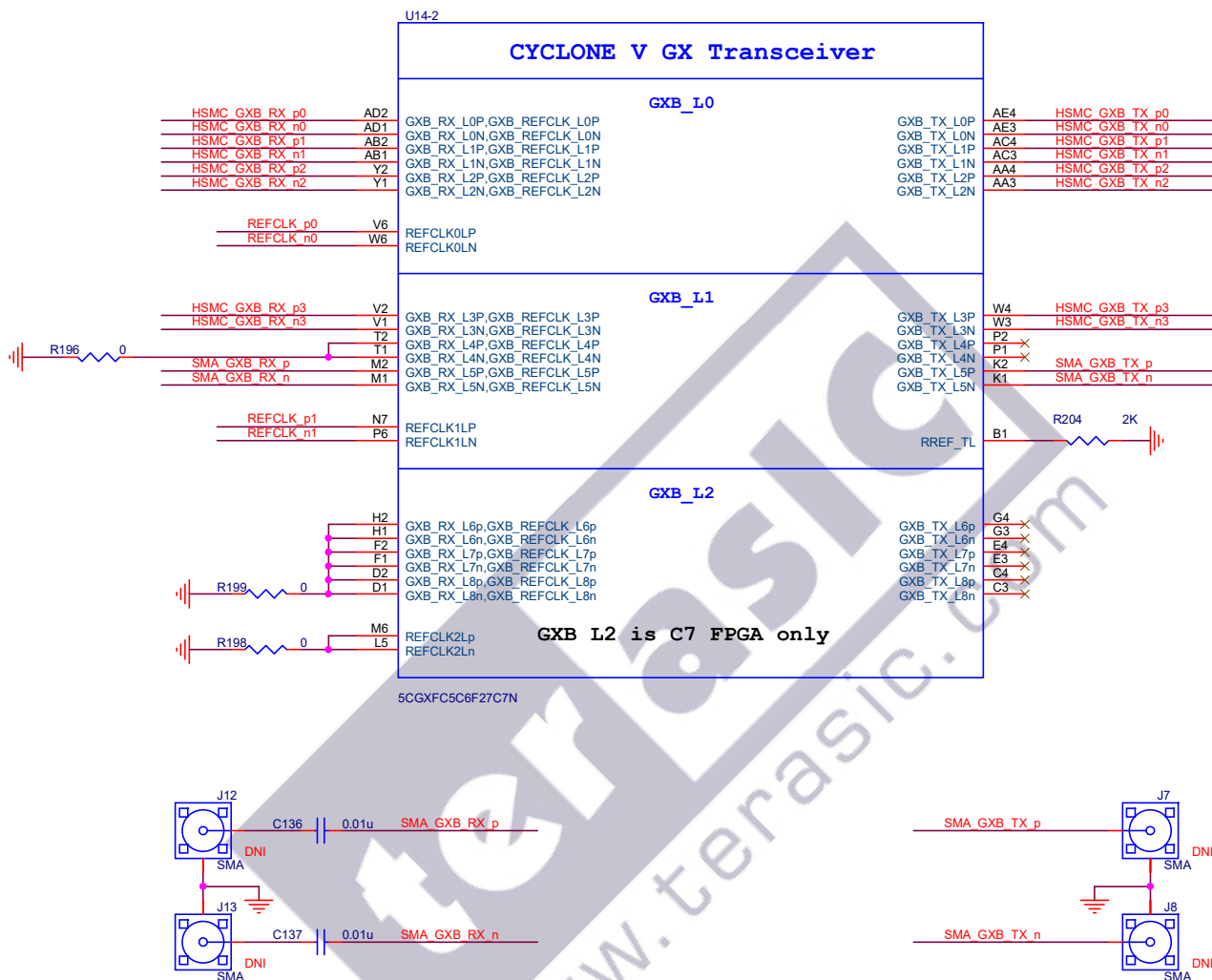
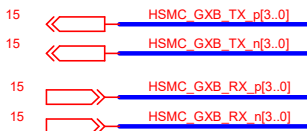
UART_RX
UART_TX

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Title					
Cyclone V GX Starter Kit					
Size	Document Number				Rev
B	FPGA BANK 7 & 8				B
Date:	Wednesday, August 14, 2013		Sheet	5	of 23

XCVR Reference Clock



HSMC Transceiver



GXB L2 is C7 FPGA only

5CGXFC5C6F27C7N

LPDDR2



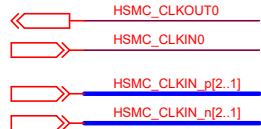
KEY



GPIO (CLOCK IN/OUT)



HSMC Clock



XCVR Reference Clock



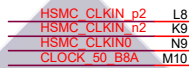
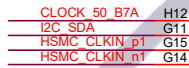
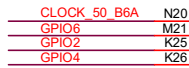
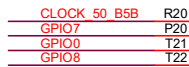
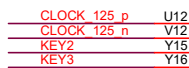
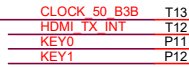
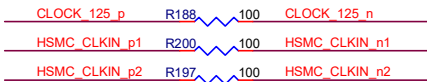
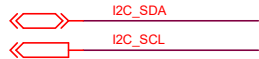
HDMI TX



GPIO



I2C Interface



U14-3

CYCLONE V GX Clock

Bank 3B VCCIO = 1.2V

IO_3B/CLK0P,FPLL_BL_FBP/DIFFIO_RX_B15P
IO_3B/CLK0N,FPLL_BL_FBN/DIFFIO_RX_B15N
IO_3B/CLK1P/DIFFIO_RX_B23P
IO_3B/CLK1N/DIFFIO_RX_B23N

AF7 DDR2LP_CA2
AF8 DDR2LP_CA3

Bank 4A VCCIO = 1.2V

IO_4A/CLK2P/DIFFIO_RX_B31P
IO_4A/CLK2N/DIFFIO_RX_B31N
IO_4A/CLK3P/DIFFIO_RX_B39P
IO_4A/CLK3N/DIFFIO_RX_B39N

Bank 5B VCCIO = 3.3V

IO_5B/FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTP,FPLL_BR_FB/DIFFIO_TX_R20P/DQ3R
IO_5B/FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTN/DIFFIO_TX_R20N/DQ3R

Y25 HDMI_TX_CLK
Y26 HDMI_TX_DE

Bank 6A VCCIO = 3.3V

IO_6A/FPLL_TR_CLKOUT0,FPLL_TR_CLKOUTP,FPLL_TR_FB/DIFFIO_TX_R28P/DQ4R
IO_6A/FPLL_TR_CLKOUT1,FPLL_TR_CLKOUTN/DIFFIO_TX_R28N/DQ4R

F26 GPIO16
G26 GPIO18

Bank 7A VCCIO = 2.5V

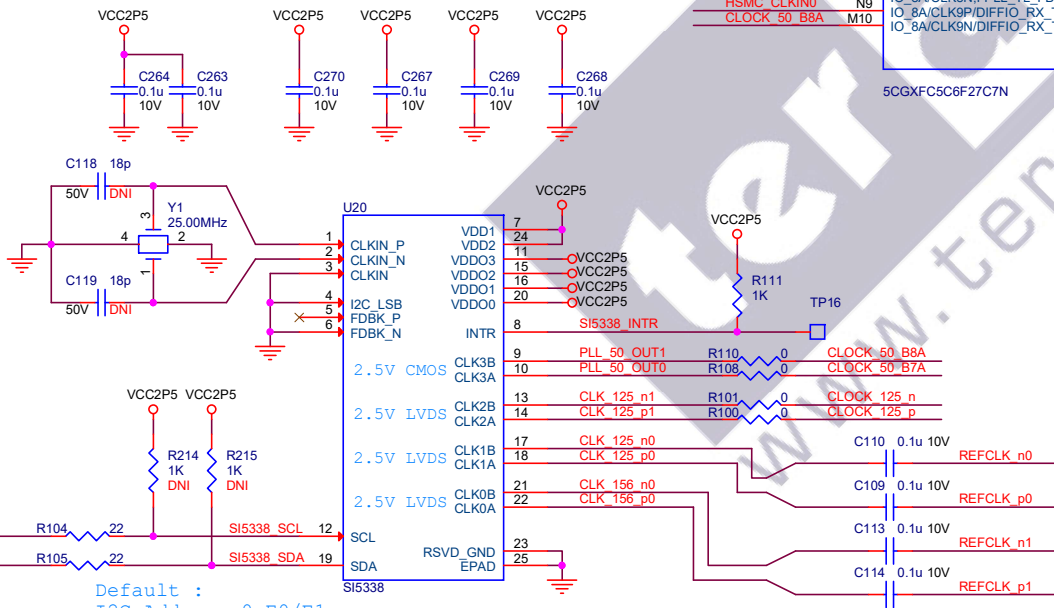
IO_7A/CLK10P/DIFFIO_RX_T33P
IO_7A/CLK10N/DIFFIO_RX_T33N
IO_7A/CLK11P/DIFFIO_RX_T25P
IO_7A/CLK11N/DIFFIO_RX_T25N

Bank 8A VCCIO = 2.5V

IO_8A/FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTP,FPLL_TL_FB/DIFFIO_TX_T44P/DQ6T/CA_2
IO_8A/FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTN/DIFFIO_TX_T44N/DQ6T/CA_3

A7 HSMC_CLKOUT0
B7 I2C_SCL

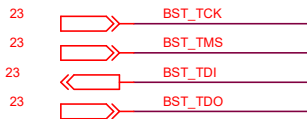
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Default :
I2C Address 0xE0/E1

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Title Cyclone V GX Starter Kit		
Size B	Document Number FPGA Clock	Rev B
Date: Friday, November 15, 2013	Sheet 7	of 23

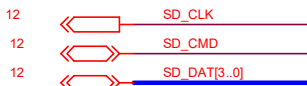
USB Blaster



CPU_RESET



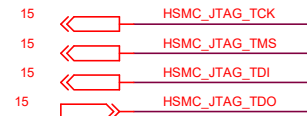
Micro SD Card



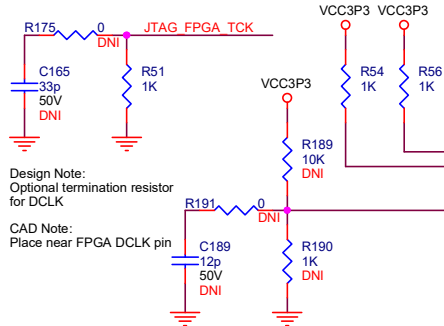
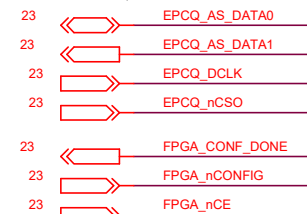
GPIO



HSMC JTAG



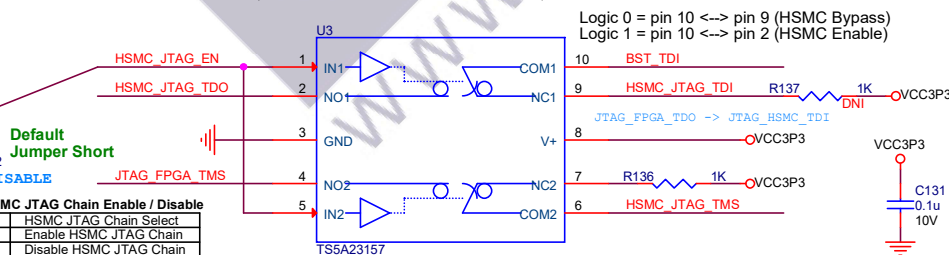
EPCQ Interface



Design Note:
Optional termination resistor
for DCLK

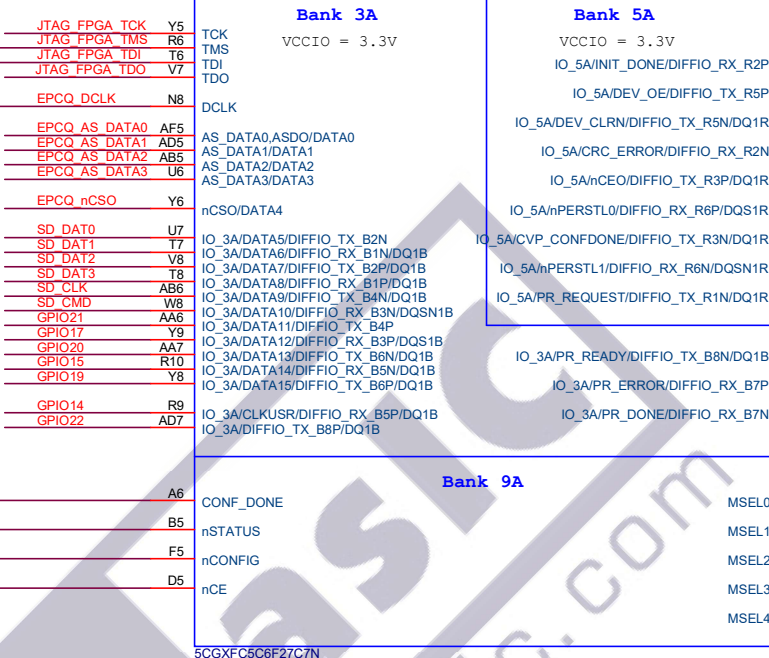
CAD Note:
Place near FPGA DCLK pin

LOW --> NC to/from COM = ON and NO to/from COM = OFF
HIGH --> NC to/from COM = OFF and NO to/from COM = ON

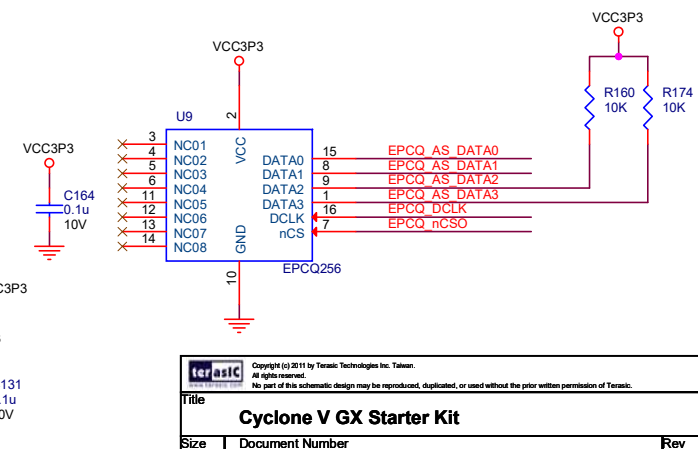


JP2	HSMC JTAG Chain Enable / Disable
Open	Enable HSMC JTAG Chain
Short	Disable HSMC JTAG Chain

CYCLONE V GX Configuration

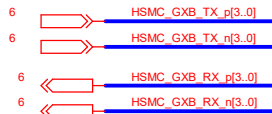


MSEL Settings : MSEL[4:0] = 10010
Active serial (AS)(x1 and x4),
no compression, no security, fast POR

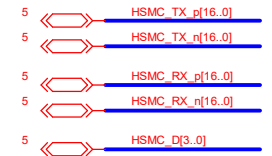


Title Cyclone V GX Starter Kit		
Size B	Document Number FPGA Configuration and JTAG	Rev B
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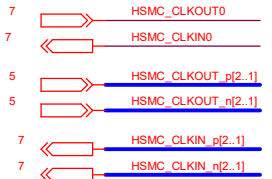
HSMC Transceiver



HSMC Interface



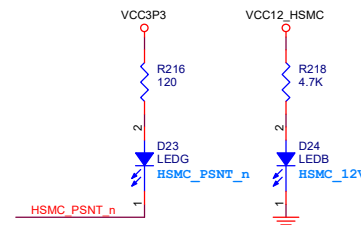
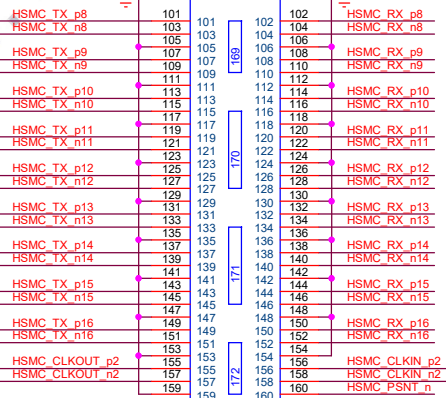
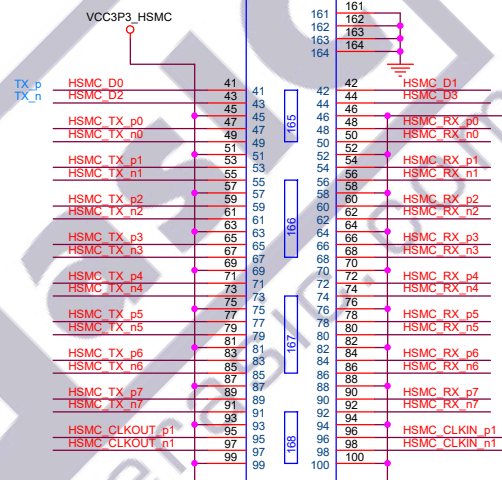
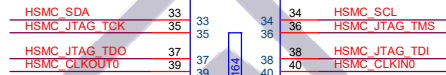
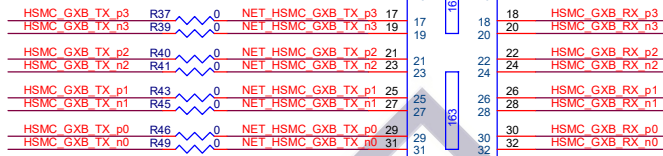
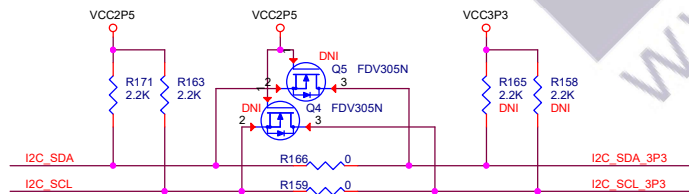
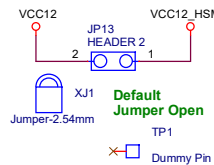
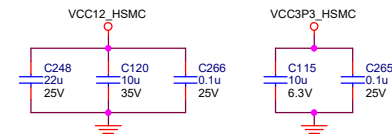
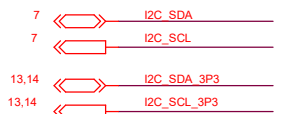
HSMC Clock

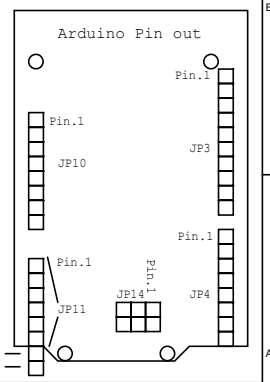
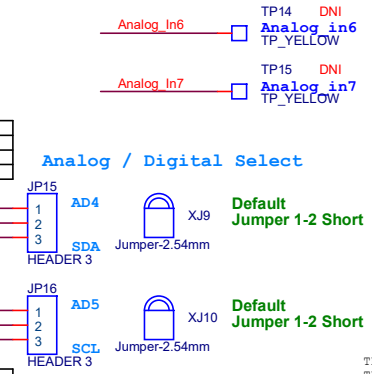
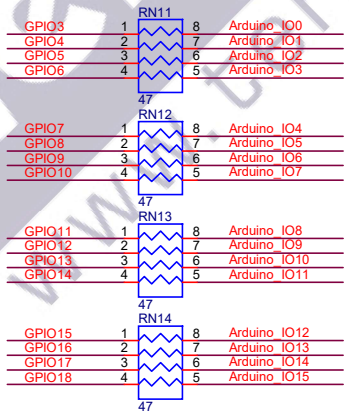
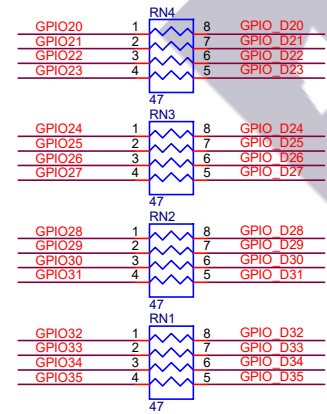
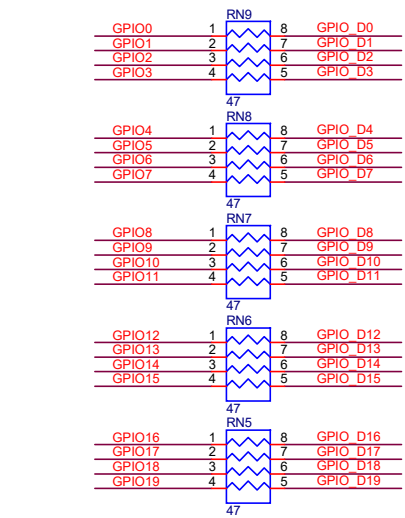
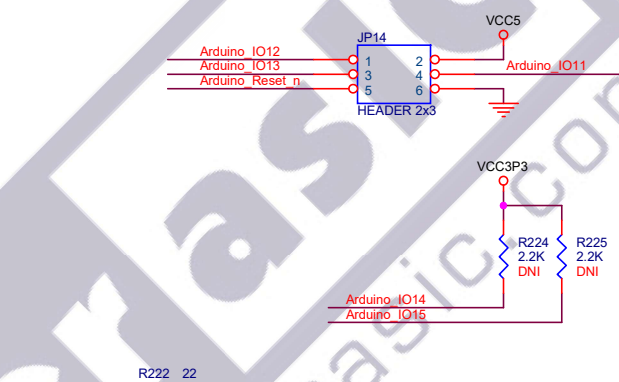
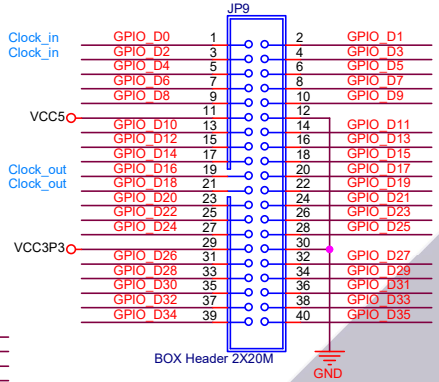
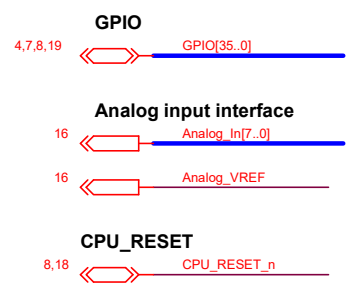
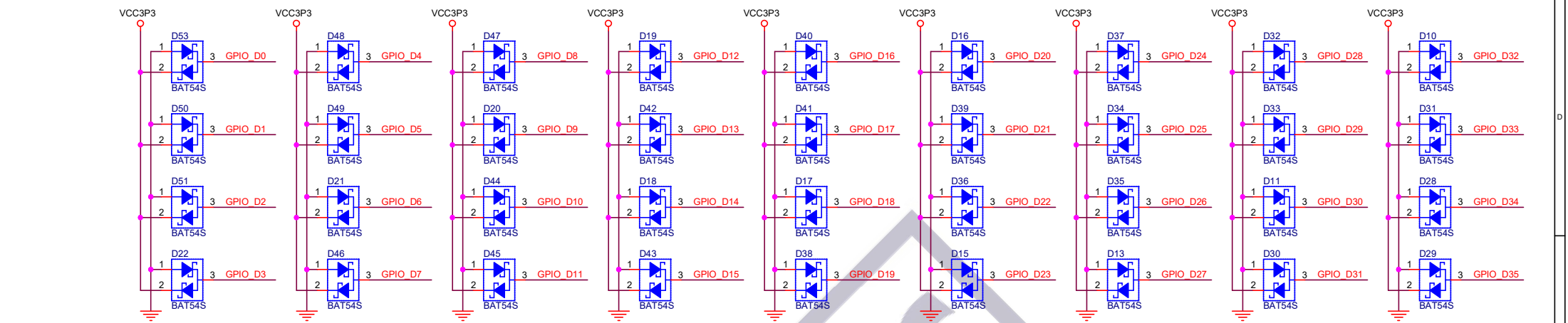


HSMC JTAG



I2C Interface

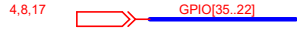




7-Segment



7-Segment (share GPIO[35..22])



LED

