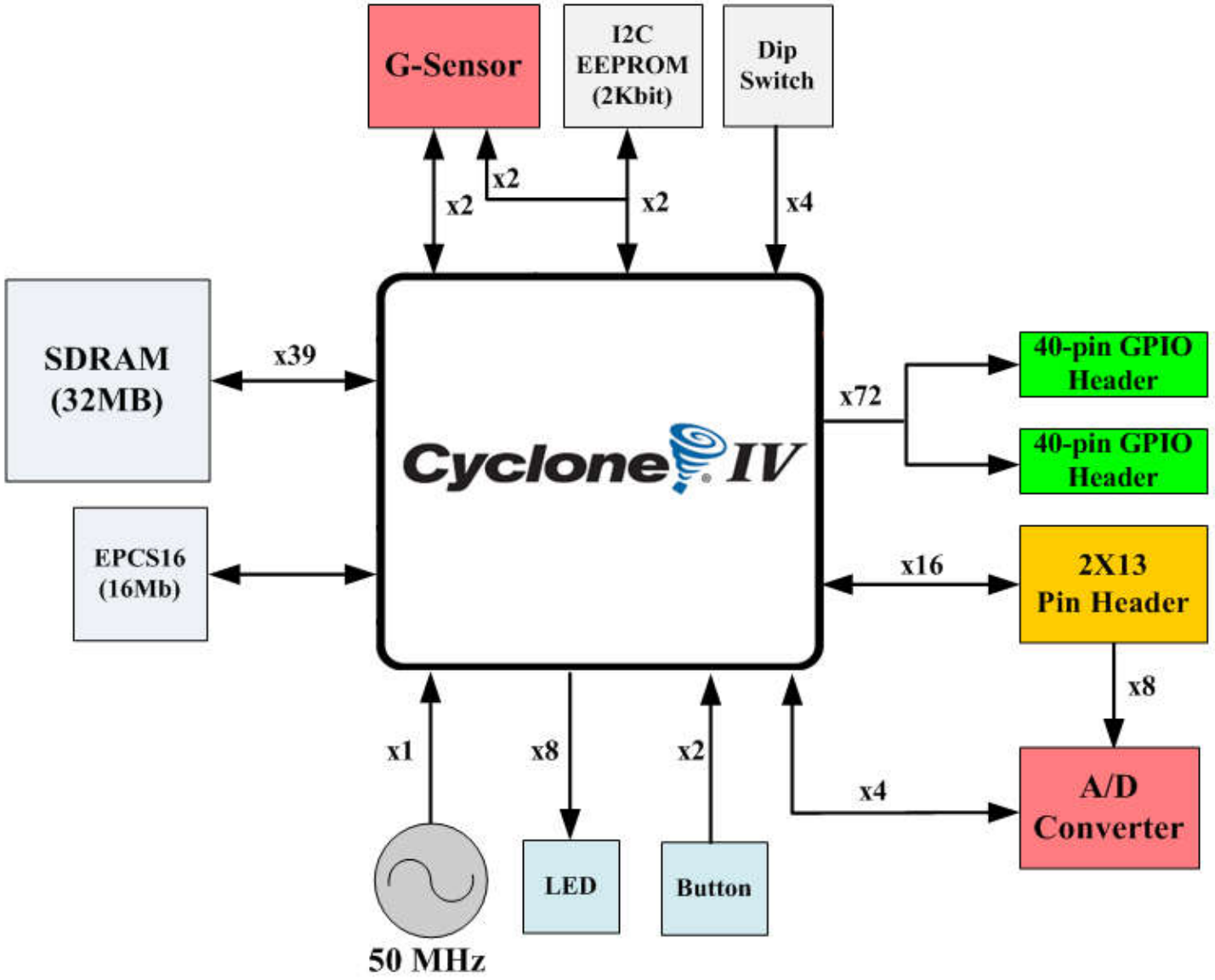
ALTERA Cyclone IV Development & Education Board (DE0-Nano)

Title: **DE0-Nano Board**

Size	Document Number	Rev
B	COVER PAGE	F

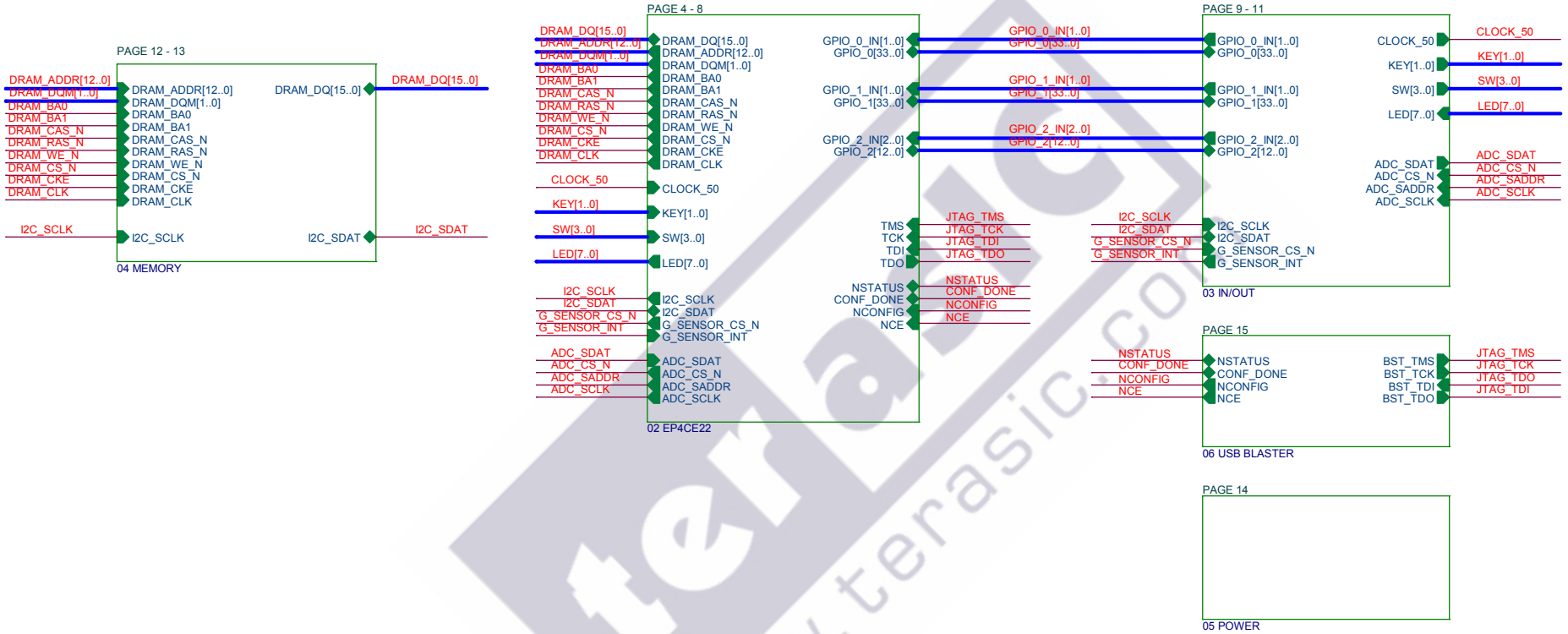
Date: Monday, May 15, 2017 Sheet 1 of 15



Title: **DE0-Nano Board**

Size	Document Number	Rev
B	PLACEMENT	F

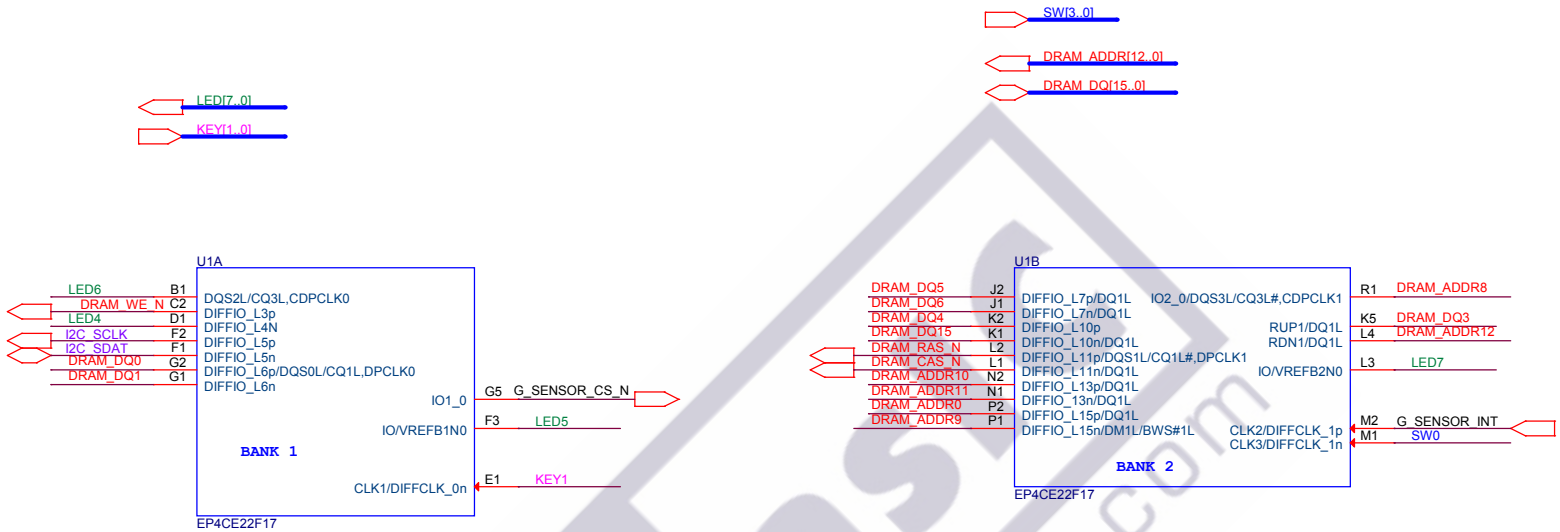
Date: Monday, May 15, 2017 Sheet 2 of 15



Title: **DE0-Nano Board**

Size	Document Number	Rev
B	TOP	F

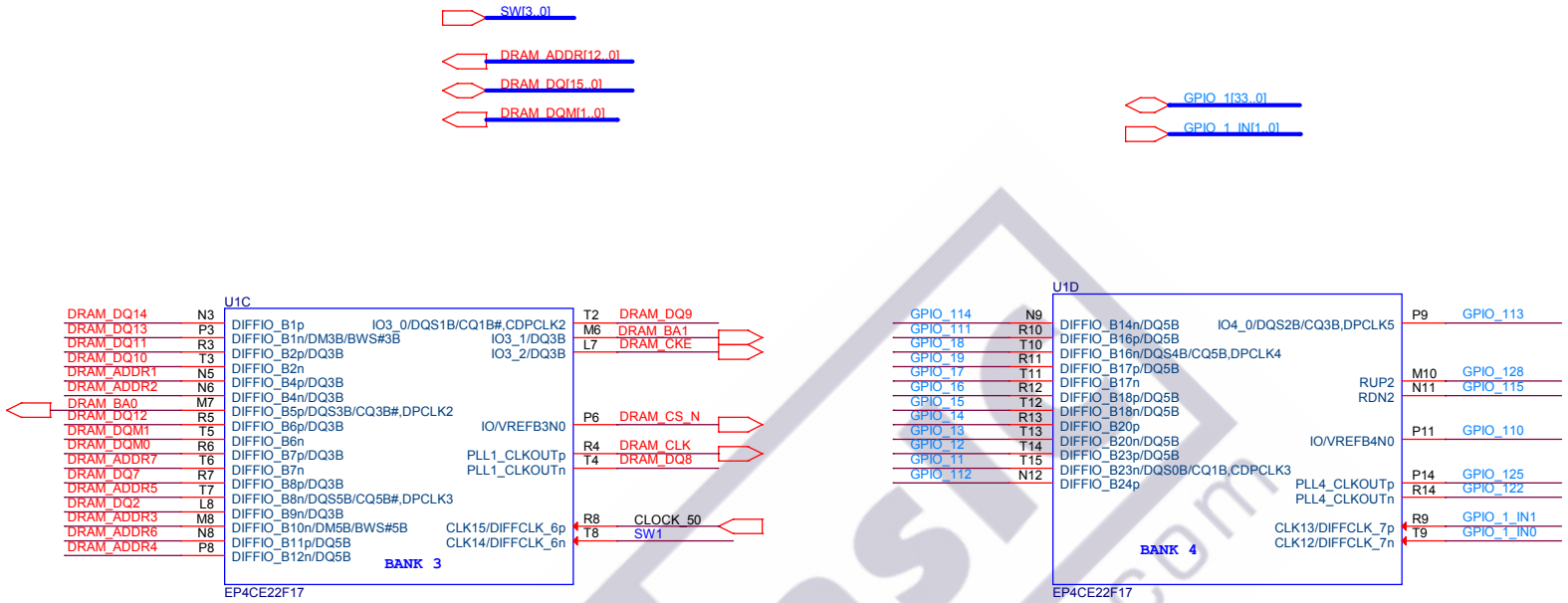
Date: Monday, May 15, 2017 Sheet 3 of 15



Title
DE0-Nano Board

Size	Document Number	Rev
B	EP4CE22 BANK1 & BANK2	F

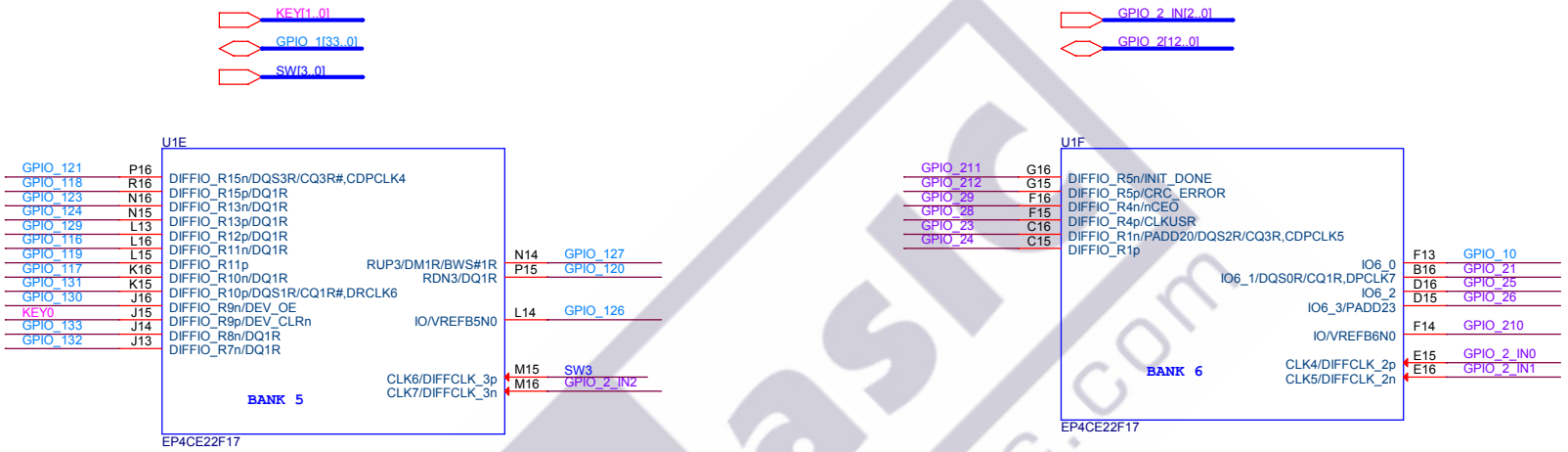
Date: Monday, May 15, 2017 Sheet 4 of 15



Title: **DE0-Nano Board**

Size	Document Number	Rev
B	EP4CE22 BANK3 & BANK4	F

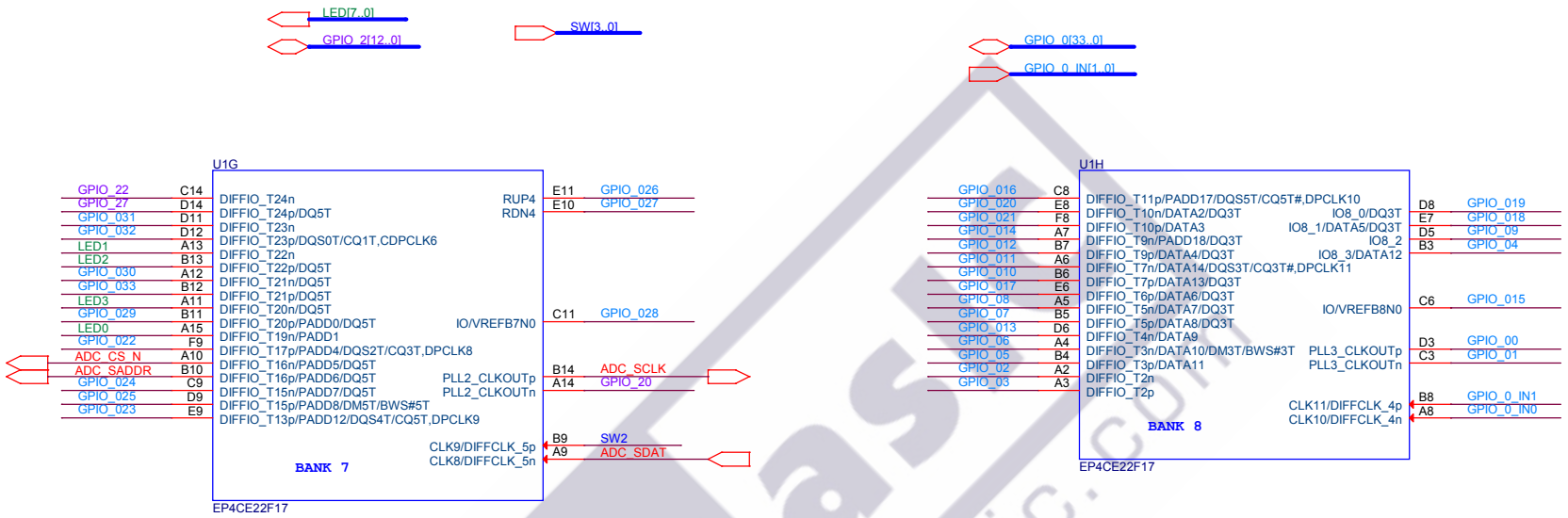
Date: Monday, May 15, 2017 Sheet 5 of 15



Title
DE0-Nano Board

Size	Document Number	Rev
B	EP4CE22 BANK5 & BANK6	F

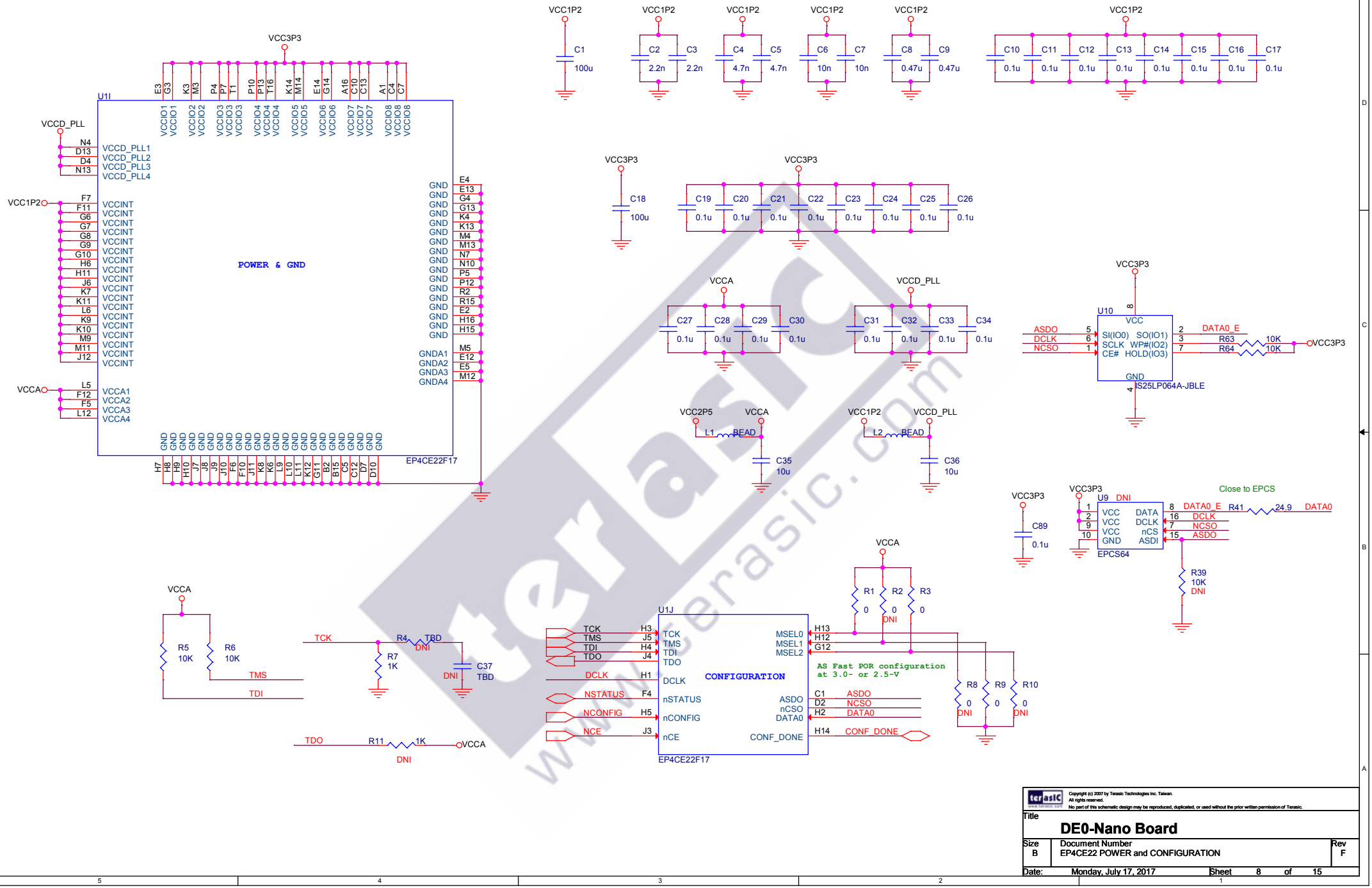
Date: Monday, May 15, 2017 Sheet 6 of 15



Title: **DE0-Nano Board**

Size	Document Number	Rev
B	EP4CE22 BANK7 & BANK8	F

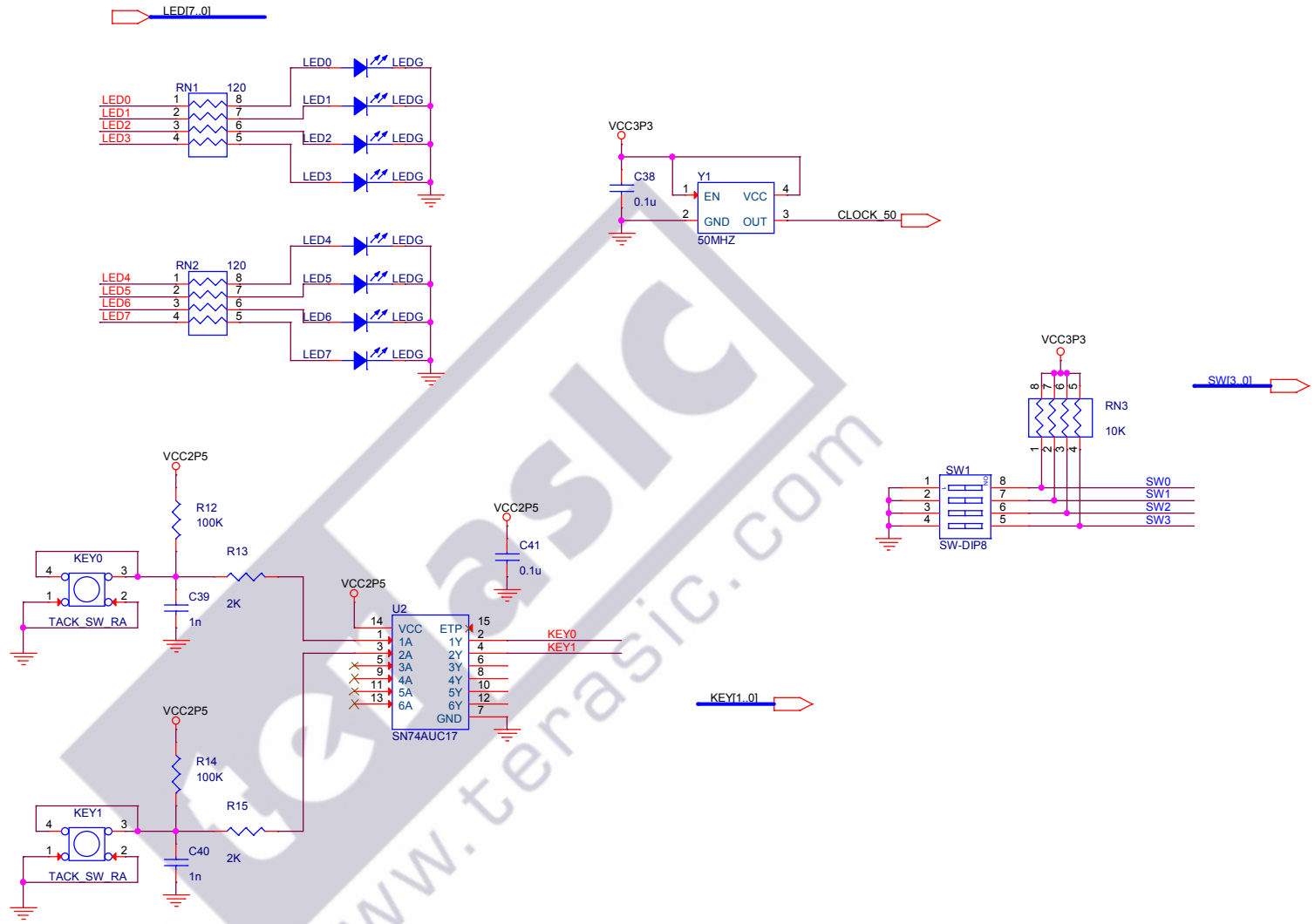
Date: Monday, May 15, 2017 Sheet 7 of 15



Title: **DE0-Nano Board**

Size	Document Number	Rev
B	EP4CE22 POWER and CONFIGURATION	F

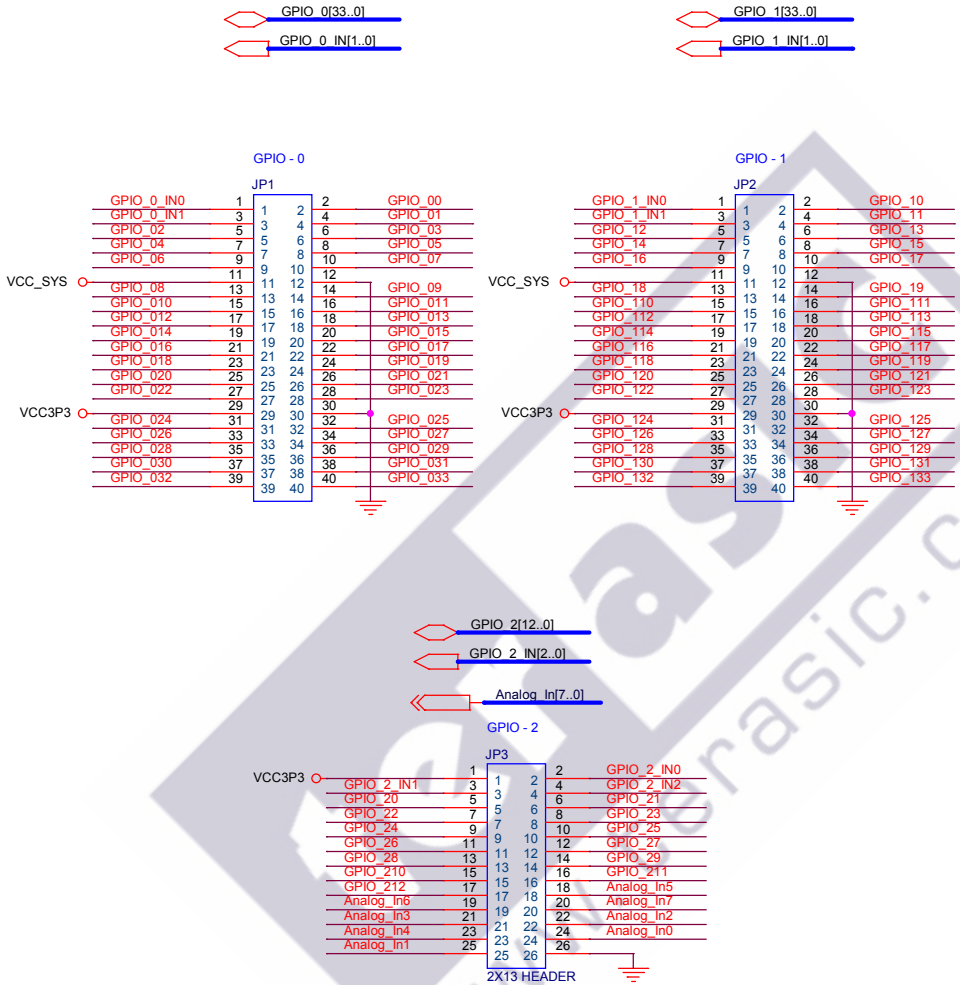
Date: Monday, July 17, 2017 Sheet 8 of 15



Title
DE0-Nano Board

Size	Document Number	Rev
B	CLOCK & LED & BUTTON & SWITCH	F

Date: Monday, May 15, 2017 Sheet 9 of 15

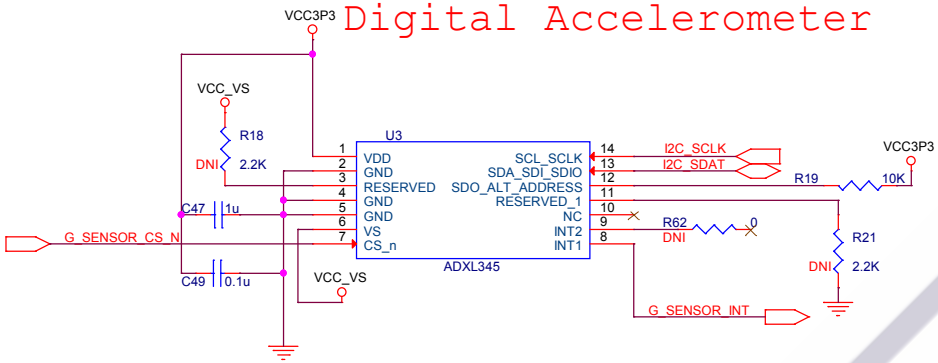


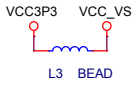
Title: **DE0-Nano Board**

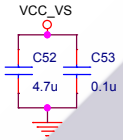
Size	Document Number	Rev
B	GPIOs & 2X13 Header	F

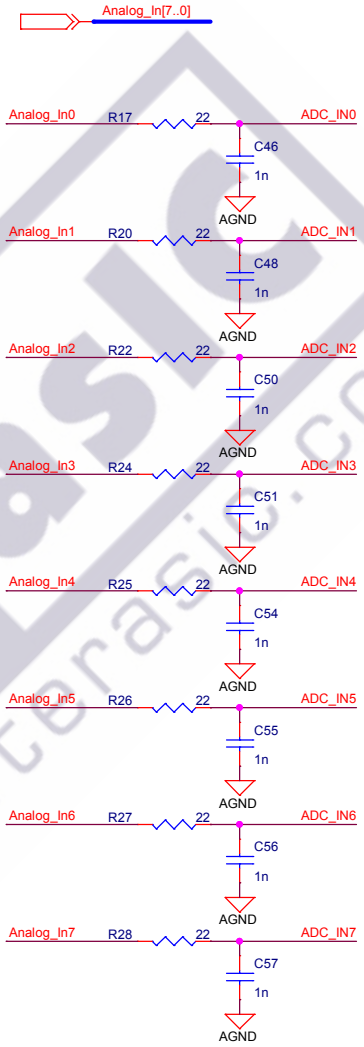
Date: Monday, May 15, 2017 Sheet 10 of 15

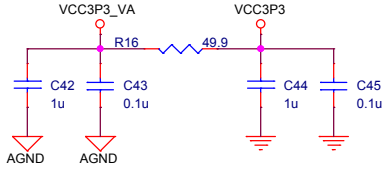
Digital Accelerometer

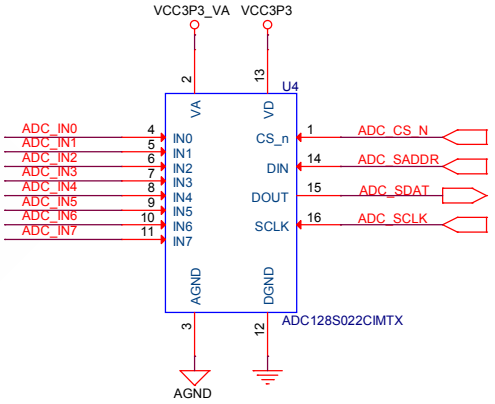


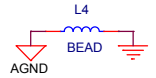








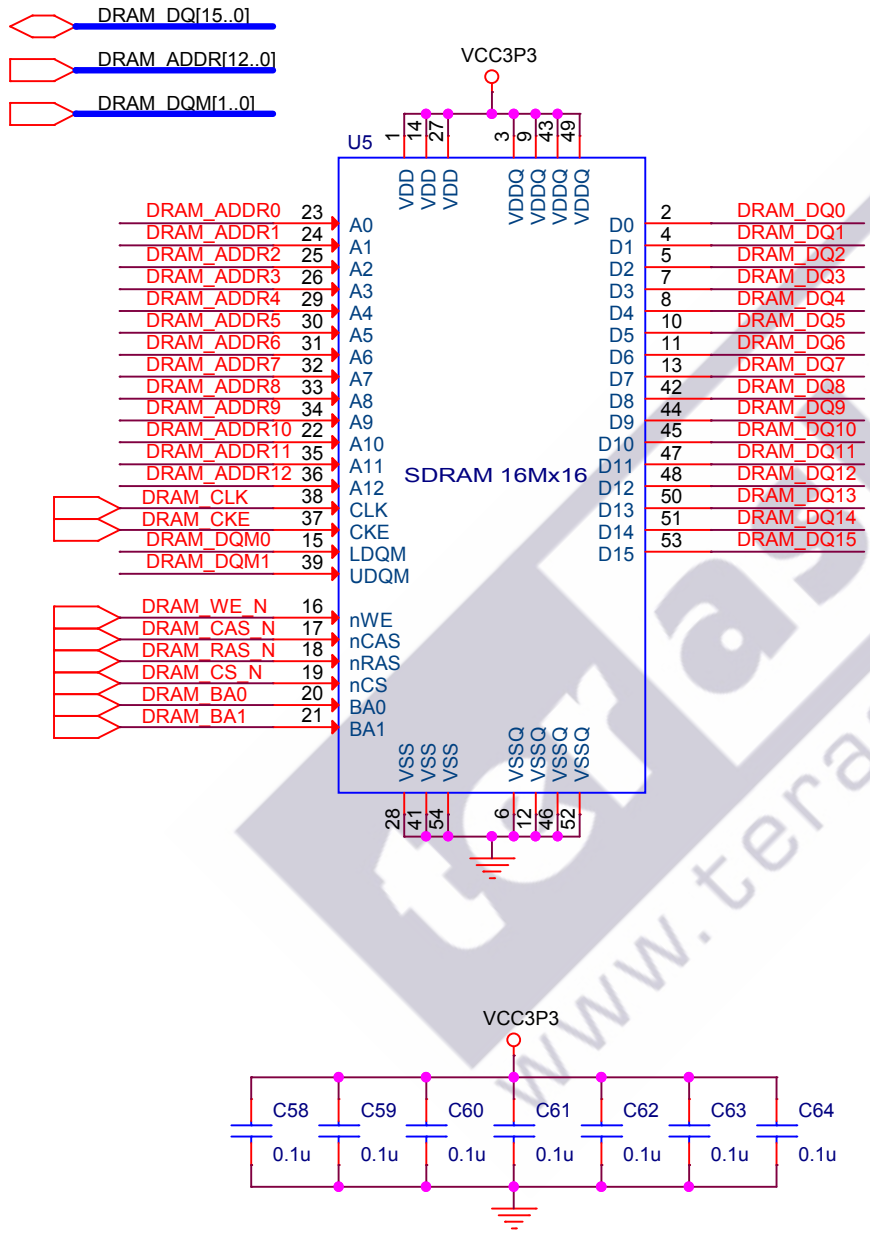




Title: **DE0-Nano Board**

Size	Document Number	Rev
B	G-Sensor & ADC	F

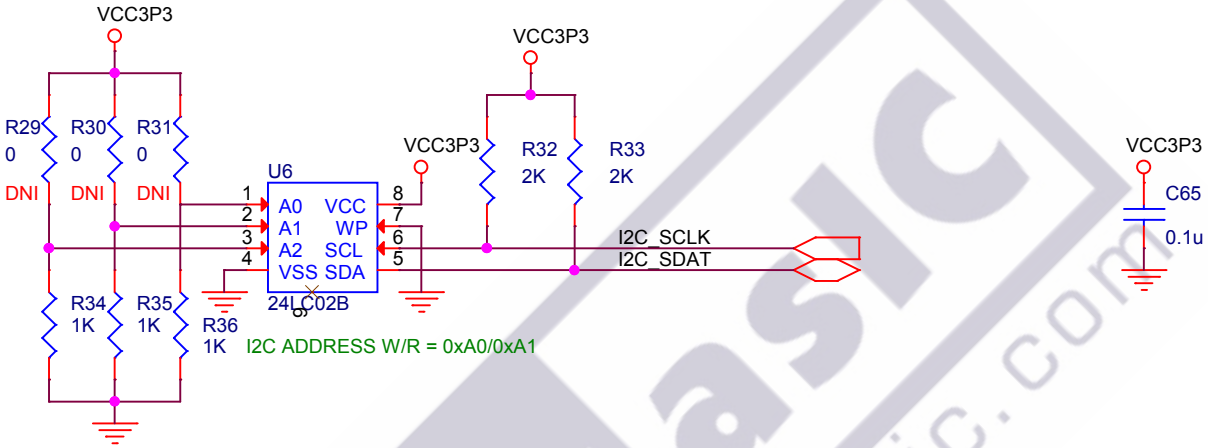
Date: Monday, May 15, 2017 Sheet 11 of 15



Title
DE0-Nano Board

Size	Document Number	Rev
A	SDRAM	F

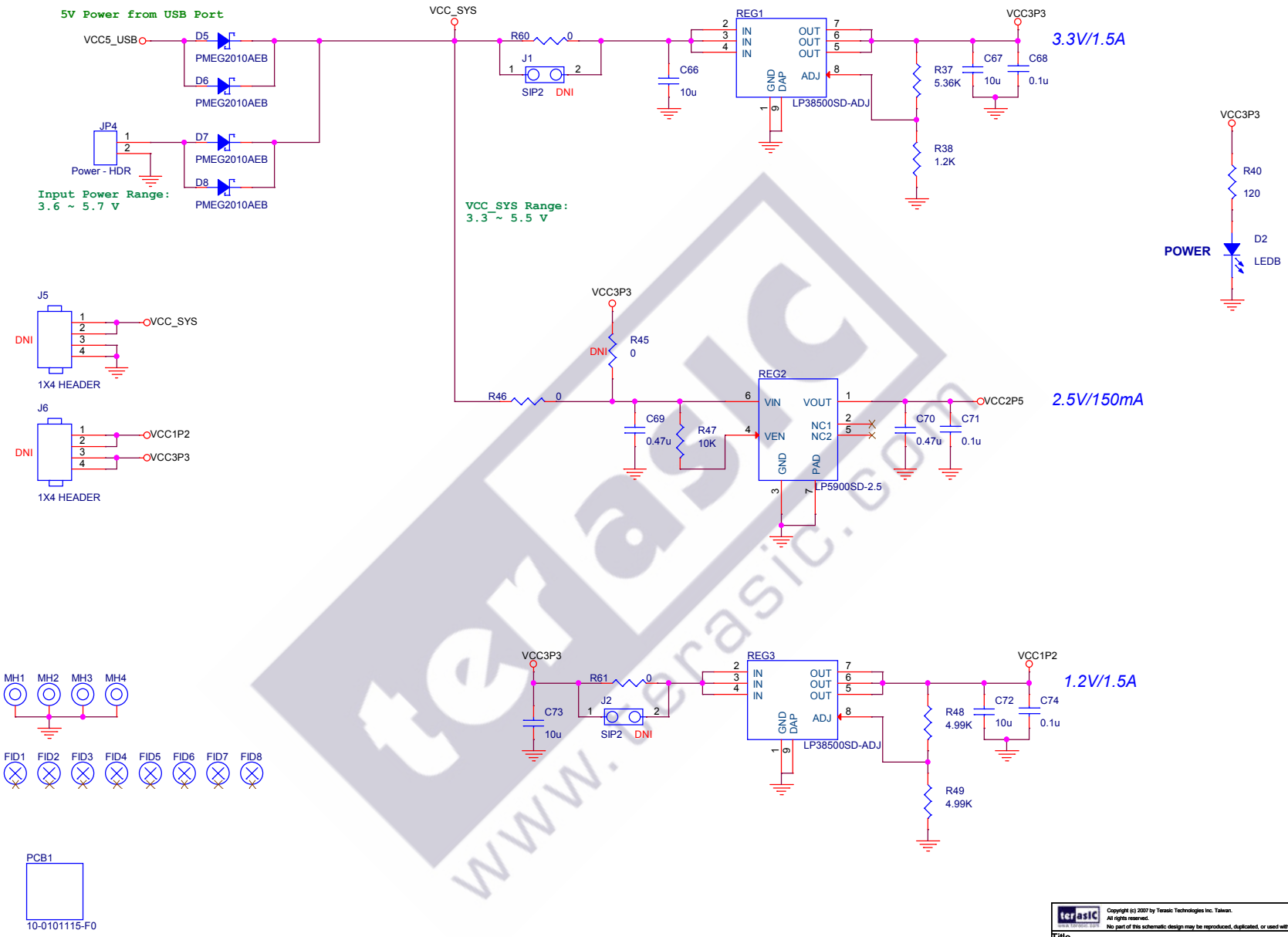
Date: Monday, May 15, 2017 Sheet 12 of 15



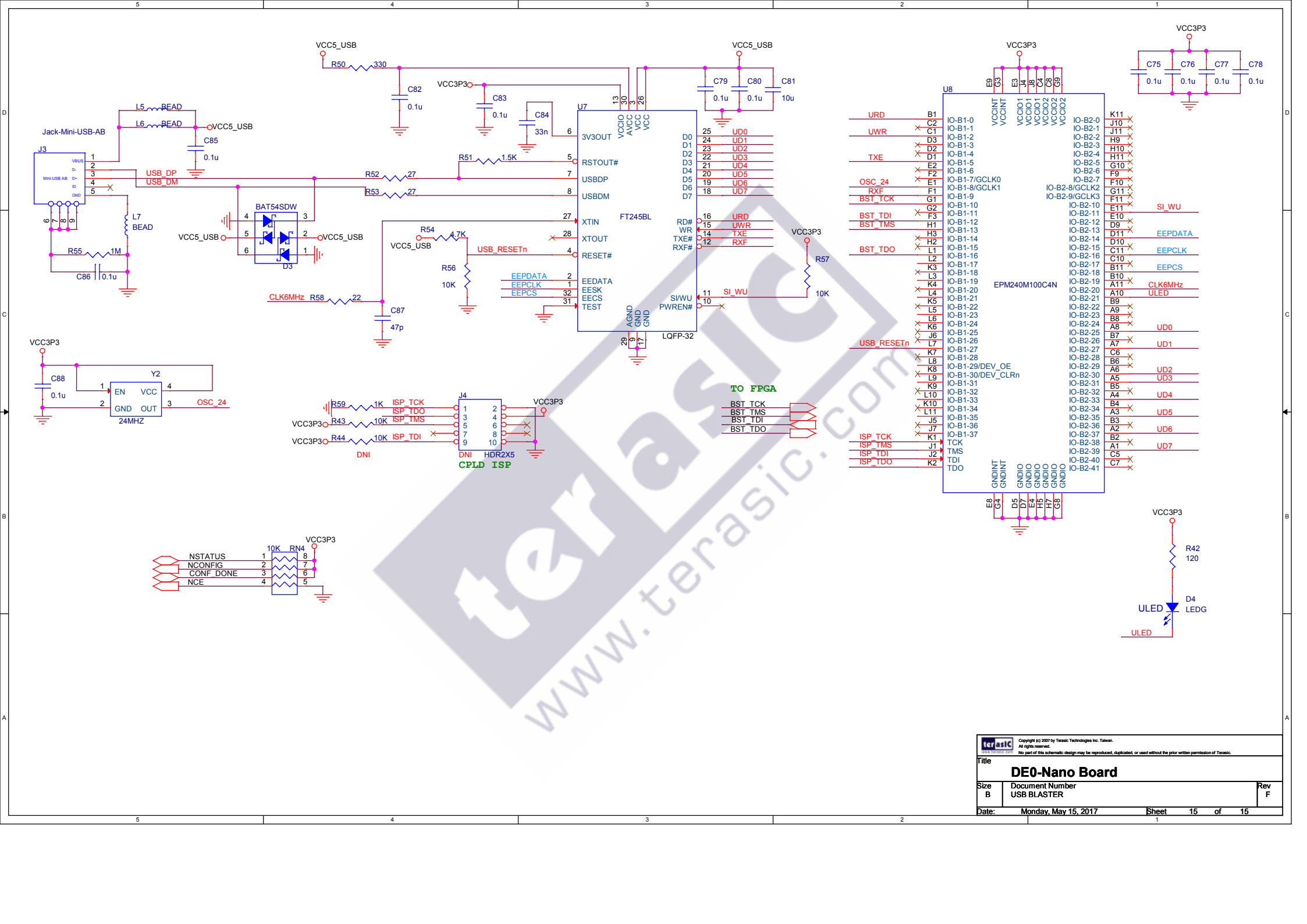
Title: **DE0-Nano Board**

Size	Document Number	Rev
A	EEPROM	F

Date: Monday, May 15, 2017 Sheet 13 of 15



Title	**DE0-Nano Board**	
Size B	Document Number 1.2V & 2.5V & 3.3V	Rev F
Date: Monday, May 15, 2017	Sheet 14 of 15	


Jack-Mini-USB-AB
J3
L5 BEAD
L6 BEAD
VCC5_USB
C85 0.1u
USB_DP
USB_DM
L7 BEAD
R55 1M
C86 0.1u
BAT54SDW
D3
R50 330
C82 0.1u
C83 0.1u
C84 33n
VCC3P3
U7
FT245BL
3V3OUT
RSTOUT#
USBDP
USBDM
XTIN
XTOUT
RESET#
EEDATA
EESK
EECS
TEST
VCCIO
AVCC
VCC
AGND
GND
LQFP-32
R51 1.5K
R52 27
R53 27
R54 4.7K
R56 10K
USB_RESETn
CLK6MHz
R58 22
C87 47p
EEPDATA
EEPCLK
EEPCS
D0 D1 D2 D3 D4 D5 D6 D7
UD0 UD1 UD2 UD3 UD4 UD5 UD6 UD7
RD# WR TXE# RXF#
URD UWR TXE RXF
SI/WU PWREN#
SI_WU
R57 10K
C79 0.1u
C80 0.1u
C81 10u
C88 0.1u
Y2
EN VCC GND OUT
24MHZ
OSC_24
R59 1K ISP_TCK
ISP_TDO
R43 10K ISP_TMS
R44 10K ISP_TDI
DNI
J4
HDR2X5
CPLD ISP
TO FPGA
BST_TCK
BST_TMS
BST_TDI
BST_TDO
NSTATUS
NCONFIG
CONF_DONE
NCE
10K RN4
U8
EPM240M100C4N
URD
UWR
TXE
OSC_24
RXF
BST_TCK
BST_TDI
BST_TMS
BST_TDO
USB_RESETn
ISP_TCK
ISP_TMS
ISP_TDI
ISP_TDO
TCK
TMS
TDI
TDO
VCCINT
VCCIO1
VCCIO2
GNDINT
GNDIO
IO-B1-0 IO-B1-1 IO-B1-2 IO-B1-3 IO-B1-4 IO-B1-5 IO-B1-6
IO-B1-7/GCLK0
IO-B1-8/GCLK1
IO-B1-9 IO-B1-10 IO-B1-11 IO-B1-12 IO-B1-13 IO-B1-14 IO-B1-15 IO-B1-16 IO-B1-17 IO-B1-18 IO-B1-19 IO-B1-20 IO-B1-21 IO-B1-22 IO-B1-23 IO-B1-24 IO-B1-25 IO-B1-26 IO-B1-27 IO-B1-28
IO-B1-29/DEV_OE
IO-B1-30/DEV_CLRn
IO-B1-31 IO-B1-32 IO-B1-33 IO-B1-34 IO-B1-35 IO-B1-36 IO-B1-37
IO-B2-0 IO-B2-1 IO-B2-2 IO-B2-3 IO-B2-4 IO-B2-5 IO-B2-6 IO-B2-7
IO-B2-8/GCLK2
IO-B2-9/GCLK3
IO-B2-10 IO-B2-11 IO-B2-12 IO-B2-13 IO-B2-14 IO-B2-15 IO-B2-16 IO-B2-17 IO-B2-18 IO-B2-19 IO-B2-20 IO-B2-21 IO-B2-22 IO-B2-23 IO-B2-24 IO-B2-25 IO-B2-26 IO-B2-27 IO-B2-28 IO-B2-29 IO-B2-30 IO-B2-31 IO-B2-32 IO-B2-33 IO-B2-34 IO-B2-35 IO-B2-36 IO-B2-37 IO-B2-38 IO-B2-39 IO-B2-40 IO-B2-41
SI_WU
EEPDATA
EEPCLK
EEPCS
CLK6MHz
ULED
UD0 UD1 UD2 UD3 UD4 UD5 UD6 UD7
C75 C76 C77 C78 0.1u
R42 120
D4 LEDG
ULED
Copyright (c) 2007 by Terasic Technologies Inc. Taiwan.
All rights reserved.
No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.
Title
DE0-Nano Board
Size B
Document Number
USB BLASTER
Rev F
Date: Monday, May 15, 2017
Sheet 15 of 15