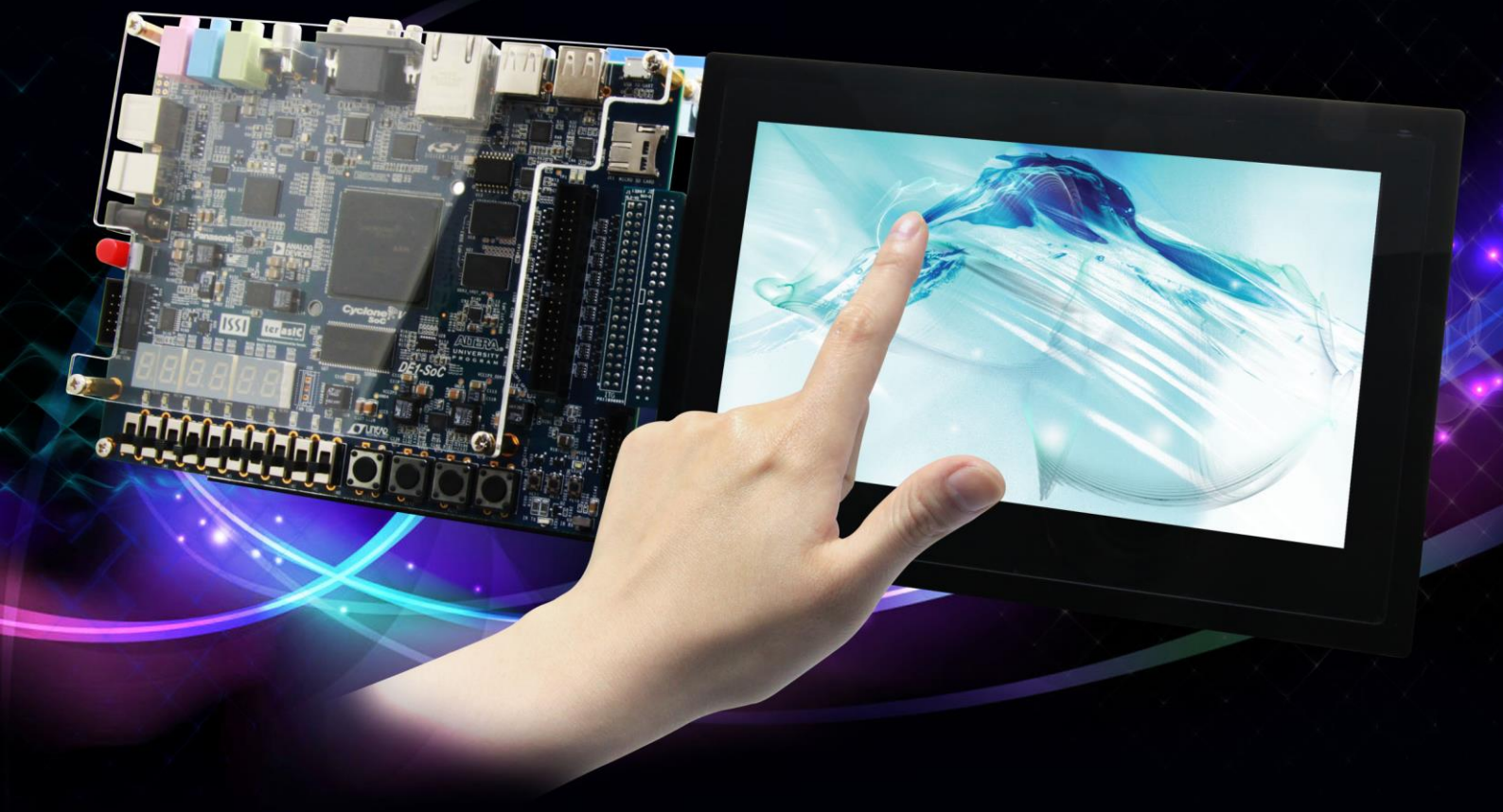
DE1-SoC-MTL

User Manual



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Chapter 1

Introduction

The DE1-SoC-MTL Development Kit is a comprehensive design environment with everything embedded developers need to create processing-based systems. The DE1-SoC-MTL delivers an integrated platform including hardware, design tools, Intellectual Property (IP), and reference designs for developing embedded software and hardware platforms in a wide range of applications. The fully integrated kit allows developers to rapidly customize their processor and IP to best suit their specific application. The DE1-SoC-MTL features a DE1-SoC development board targeting Altera Cyclone® V SX SoC FPGA, as well as a capacitive LCD multimedia color touch panel which natively supports multi-touch gestures.

The all-in-one embedded solution offered on the DE1-SoC-MTL, in combination of a LCD touch panel and digital image module, provides embedded developers the ideal platform for multimedia applications with unparallel processing performance. Developers can benefit from the use of FPGA-based embedded processing system such as mitigating design risk and obsolescence, design reuse, lowering bill of material (BOM) costs by integrating powerful graphics engines within the FPGA.

For SoC reference design in Linux for touch-screen display, please refer to the "Programming Guide for Touch-Screen Display" document in the System CD of DE1-SoC-MTL.

Figure 1-1 shows a photo of DE1-SoC-MTL.

Figure 1-1 The DE1-SoC-MTL platform

1.1 Key Features

The key features of this kit are listed below:

- **Cyclone V SX SoC—5CSEMA5F31C6N**
  - Dual-core ARM Cortex-A9 (HPS)
  - 85K programmable logic elements
  - 4,450 Kbits embedded memory
  - 6 fractional PLLs
  - 2 hard memory controllers

- **Configuration Sources**
  - Quad serial configuration device – EPCQ256 for the FPGA
  - On-board USB Blaster II (normal type B USB connector)

- **Memory Devices**
  - 64MB (32Mx16) SDRAM for the FPGA
  - 1GB (2x256MBx16) DDR3 SDRAM for the HPS
  - microSD card socket for the HPS

- **Peripherals**
  - Two port USB 2.0 Host (ULPI interface with USB type A connector)
  - UART to USB (USB Mini B connector)
  - 10/100/1000 Ethernet
  - PS/2 mouse/keyboard
  - IR emitter/receiver
  - I2C multiplexer

- **Connectors**
  - Two 40-pin expansion headers
  - One 10-pin ADC input header
  - One LTC connector (one Serial Peripheral Interface (SPI) master ,one I2C bus, and one GPIO interface)

- **Display**
  - 24-bit VGA DAC

- **Audio**
  - 24-bit CODEC, line-in, line-out, and microphone-in jacks

- **Video Input**
  - TV decoder (NTSC/PAL/SECAM) and Video-in connector

- **ADC**
  - Fast throughput rate: 1 MSPS
  - Channel number: 8
  - Resolution: 12-bit
  - Analog input range : 0 ~ 2.5 V or 0 ~ 5V by selecting the RANGE bit in the control register

- **Switches, Buttons and LEDs**
  - 5 user keys (4 for the FPGA and 1 for the HPS)
  - 10 user switches for the FPGA
  - 11 user LEDs (10 for the FPGA and 1 for the HPS)
  - 2 HPS reset buttons (HPS_RESET_n and HPS_WARM_RST_n)
  - Six 7-segment displays

- **Sensor**
  - G-sensor for the HPS

- **Power**
  - 12V DC input

- **Capacitive LCD Touch Screen**
  - Equipped with an 7-inch Amorphous-TFT-LCD (Thin Film Transistor Liquid Crystal Display) module
  - Module composed of LED backlight

- Support 24-bit parallel RGB interface
- Convert the X/Y coordination of touch point to its corresponding digital data via the touch controller.

Table 1-1 shows the general physical specifications of the touch-screen (Note*).

Table 1-1 General physical specifications of the LCD

Item	*Specification*	*Unit*
LCD size	7-inch (Diagonal)	-
Resolution	800 x3(RGB) x 480	dot
Dot pitch	0.1926(H) x0.1790 (V)	mm
Active area	154.08 (H) x 85.92 (V)	mm
Module size	164.9(H) x 100.0(V) x 5.7(D)	mm
Surface treatment	Glare	-
Color arrangement	RGB-stripe	-
Interface	Digital	-

Note: For more information about the LCD touch panel and CMOS sensor module, please refer to their datasheets in the System CD.

1.2 About the Kit

The kit includes everything users need to run the demonstrations and develop custom designs, as shown in Figure 1-2.

Figure 1-2 Contents of DE1-SoC-MTL kit package

1.3 Power On Test

The 8GB micrSD card included in the kit is pre-programmed with LXDE Linux desktop. Users can perform a power on test from the microSD card. The procedures to perform the power on test are:

1. Please make sure the microSD card is inserted to the microSD card socket (J11) onboard.
2. Set MSEL[4:0] = 00000, as shown in **Figure 1-3**.
3. Plug in a USB keyboard to the USB host on the DE1-SoC board.
4. Plug in the 12V DC power supply to the DE1-SoC board.
5. Power on the DE1-SoC board.
6. When a login prompt appears on the LCD display, as shown in **Figure 1-4**, scroll down form the keyboard and selected the "More…" then press ENTER.
7. Type "root" and press ENTER.
8. Type 'terasic" and press ENTER.
9. The LXDE Desktop will appear on the LCD display.
10. Use the touch-screen to select the system menu, as shown in **Figure 1-5**.

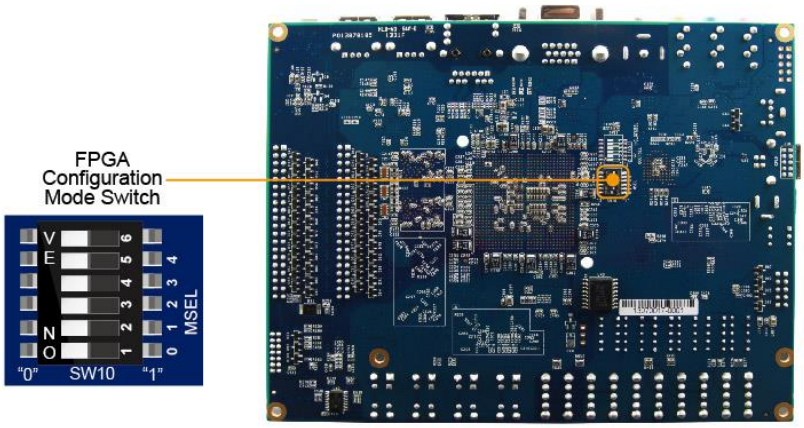

Figure 1-3 MSEL[4:0] = 00000

Figure 1-4 LXDE login prompt

Figure 1-5 LXDE desktop on DE1-SoC-MTL platform

1.4 System CD and Linux BSP

The DE1-SoC-MTL System CD contains the touch-screen documentations and supporting materials, including the user manual, reference designs, touch-screen IP and license, and device datasheets.

Users can download the System CD form the link: http://cd-de1-soc-mtl.terasic.com. This site also provides the Linux image files for creating a bootable microSD card. Table 1-1 shows the contents of DE1-SoC-MTL System CD. For the system CD of DE1-SoC mainboard, users can download it from the link: http://cd-de1-soc.terasic.com.

Table 1-1 Contents of DE1-SoC-MTL System CD

Folder Name	*Description*
Datasheet	Specifications for major components on the touch-screen display module
Demonstrations	FPGA and SoC design examples
IP	Encrypted touch controller
License	IP license of the touch controller
Manual	Including user manual and software programming guide
Schematic	Schematic of the touch-screen display module

1.5 Setup License for Terasic Multi-touch IP

To utilize the multi-touch panel in a Quartus II project, the Terasic Multi-touch IP is required. There will be error messages if the license file is not added before compiling projects using Terasic Multi-touch IP. The license file is located at:

DE1-SoC-MTL System CD\License\license_multi_touch.dat

There are two ways to setup the license. One way is to add the license file (license_multi_touch.dat) in Quartus II, as shown in Figure 1-6.

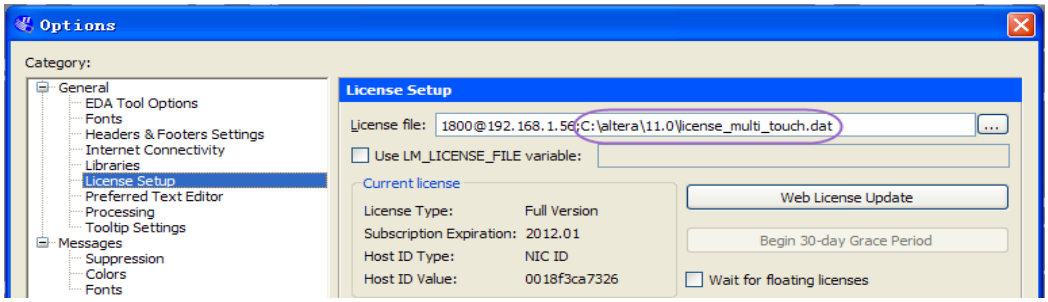

Figure 1-6 License setup

The other way is to add license content to the existing license file. The procedures are listed below:

1. Use Notepad or other text editing software to open the file license_multi_touch.dat.
2. The license file contains the FEATURE lines, which are required to license the IP Cores, as shown in Figure 1-3.
3. Open your Quartus II license.dat file in a text editor.

4. Copy everything under the license_multi_touch.dat and paste it to the end of your Quartus II license file. Note: Do NOT delete any FEATURE lines from the Quartus II license file.
5. Save the Quartus II license file.

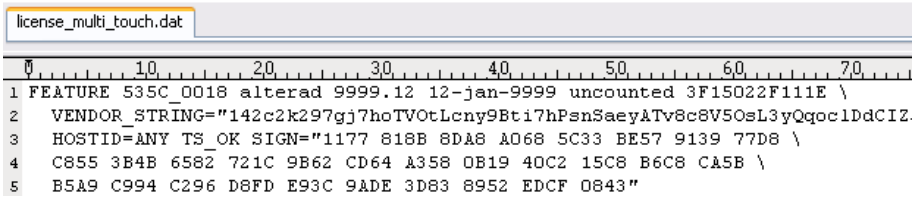

Figure 1-3 Contents of license_multi_touch.dat

1.6 Getting Help

Here is the contact information should you encounter any problem:

- **Terasic Technologies**
- **Tel: +886-3-575-0880**
- **Email: support@terasic.com**

Chapter 2

Architecture

This chapter provides information regarding the features and architecture of DE1-SoC-MTL. The kit is composed of DE1-SoC mainboard and MTL (Multi-Touch LCD) module. The MTL module is connected to a 2x20 GPIO expansion header on DE1-SoC board through an ITG (IDE to GPIO) adaptor. For more information about the DE1-SoC mainboard, please refer to the user manual in DE1-SoC System CD, which can be download from the link: http://cd-de1-soc.terasic.com.

2.1 Layout and Components

Figure 2-1 and Figure 2-2 show photos of DE1-SoC-MTL. It depicts the layout of the board and indicates the locations of connectors and key components.

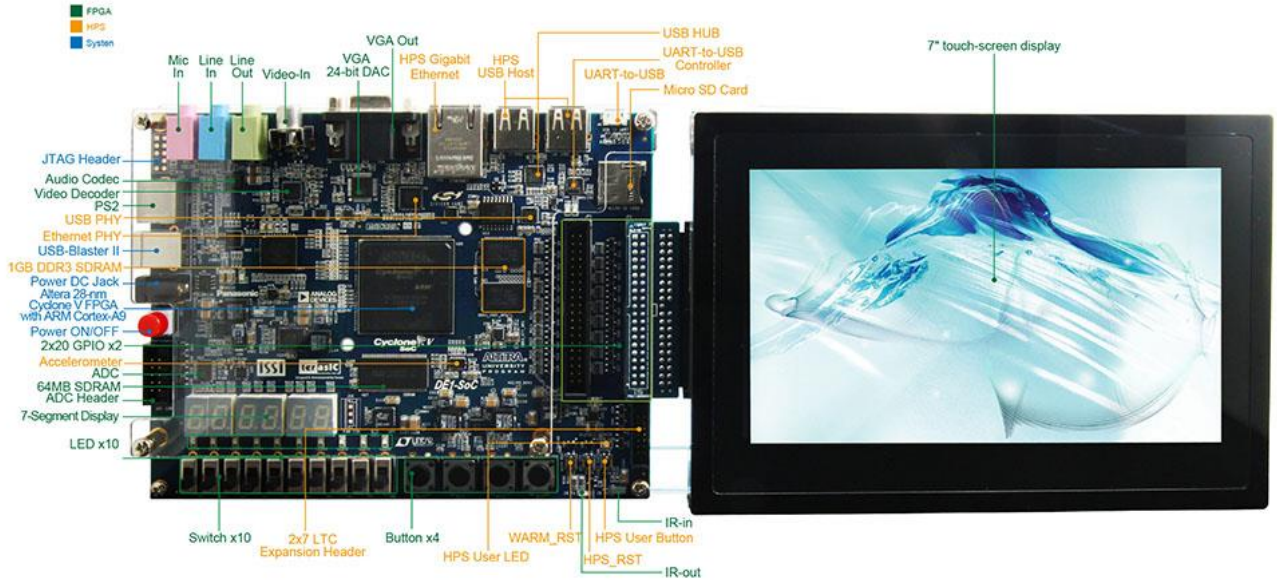

Figure 2-1 DE1-SoC-MTL (top view)

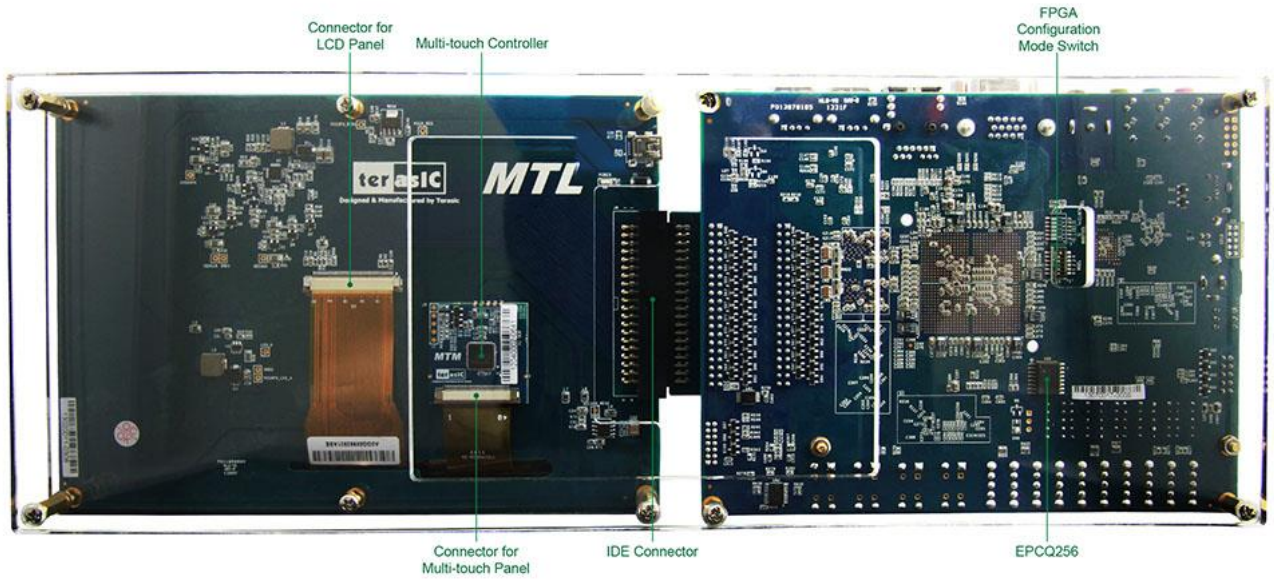

Figure 2-2 DE1-SoC-MTL (bottom view)

2.2 Block Diagram

Figure 2-3 shows the block diagram of MTL module. The IDE connector bridges all the wires from the peripherals to the FPGA through an ITG adapter.

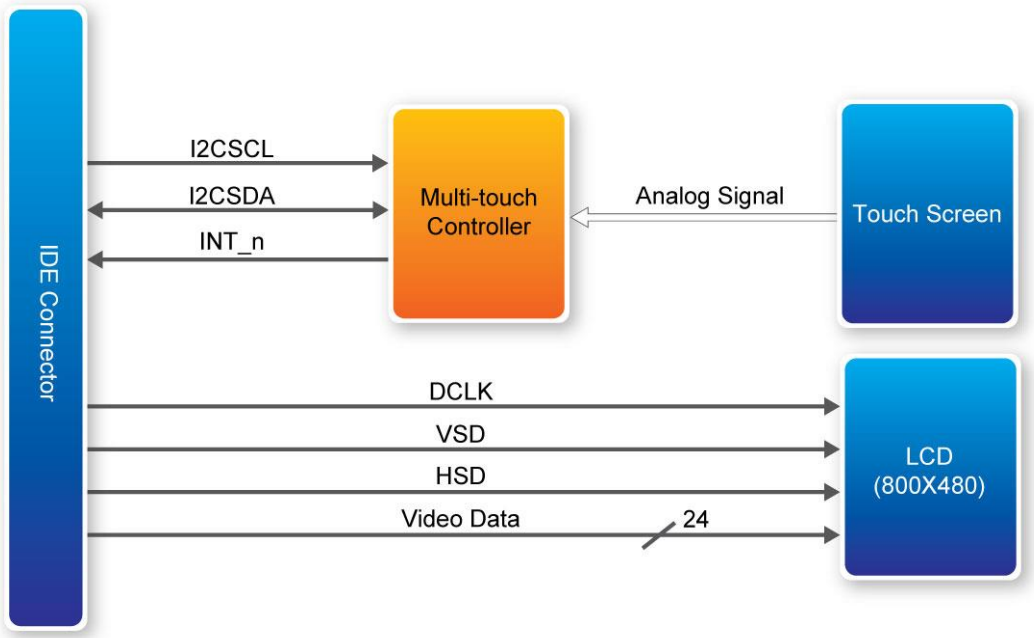

Figure 2-3 Block diagram of MTL

Figure 2-4 illustrates the connection of MTL to Terasic FPGA board.

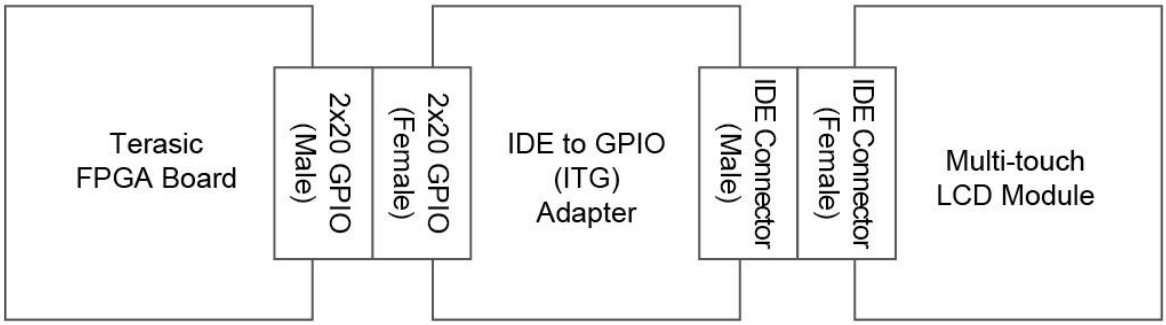

Figure 2-4 Connection Diagram of MTL Kit with Terasic FPGA boards

2.3 ITG Adapter

The IDE to GPIO (ITG) adapter is designed to remap IDE pins to GPIO pins.

Component and Layout

Figure 2-5 and Figure 2-6 show the top and bottom view of ITG adapter, respectively.

The J1 connector is used to connect the FPGA board. The J2 connector is used to interface with the IDE cable.

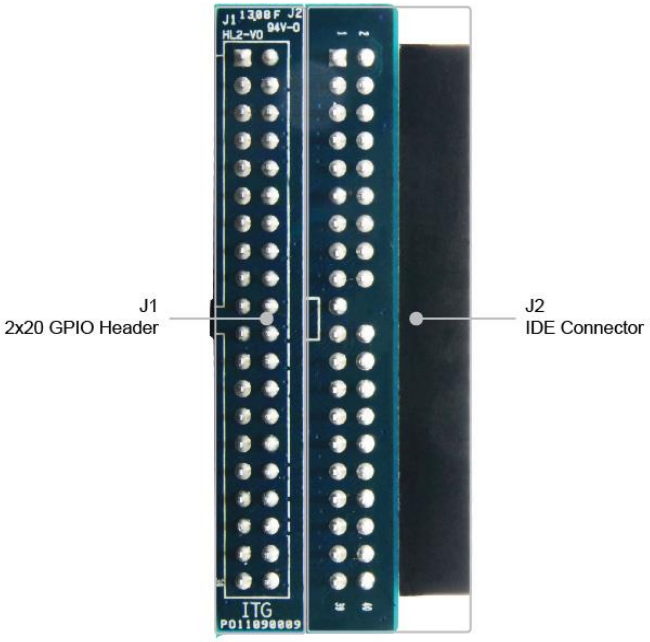

Figure 2-5 ITG adapter (top view)

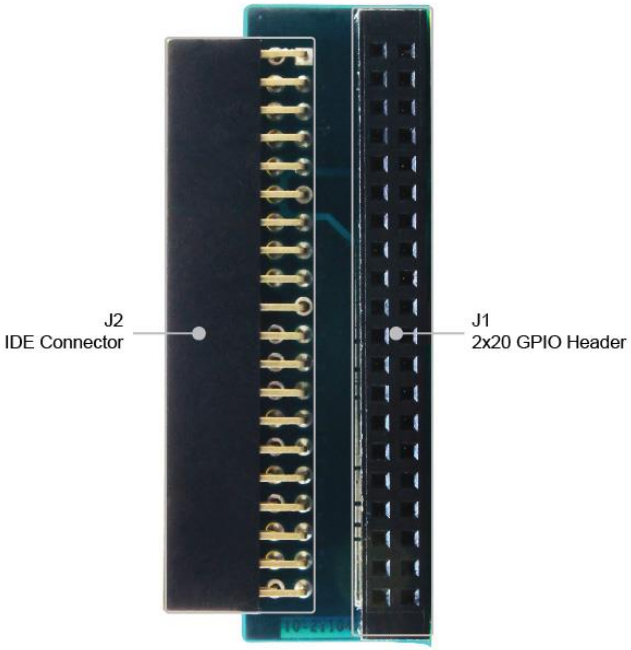

Figure 2-6 ITG adapter (bottom view)

Chapter 3

Using DE1-SoC-MTL

This chapter provides information on how to control the Multi-touch LCD Module (MTL) hardware, which includes the definition of 2x20 GPIO interface, LCD control, and multi-touch control signals.

3.1 Using FPGA

The DE1-SoC-MTL is composed of DE1-SoC SoC development board and 7" touch panel daughter card. The DE1-SoC SoC development board with the FPGA device is considered as the main part. The DE1-SoC user manual and CD are available at:

http://cd-de1-soc.terasic.com

3.2 Pin Definition of 2x20 GPIO Connector

The 2x20 GPIO female connector directly connects to the 2x20 GPIO male connector on the Terasic FPGA development boards. **Figure 3-1** shows the signal names of the 2x20 GPIO from the ITG adapter.

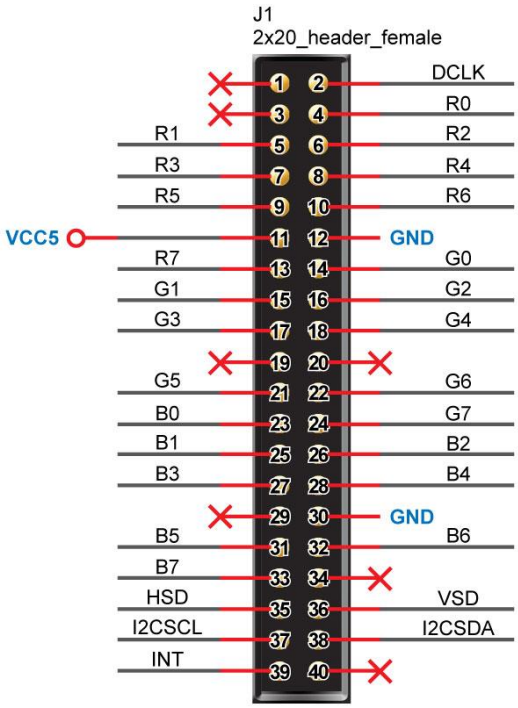

Figure 3-1 Signals of 2x20 GPIO connector

Table 3-1 shows the recommended pin assignments for the 2x20 GPIO pins in Quartus II.

Table 3-1 Recommended Pin Assignments of 2x20 GPIO in Quartus II

Pin Numbers	*Pin Name*	*Direction*	*IO Standard*
1	-	-	-
2	MTL_DCLK	Output	3.3-V LVTTL
3	-	-	-
4	MTL_R[0]	Output	3.3-V LVTTL
5	MTL_R[1]	Output	3.3-V LVTTL
6	MTL_R[2]	Output	3.3-V LVTTL
7	MTL_R[3]	Output	3.3-V LVTTL
8	MTL_R[4]	Output	3.3-V LVTTL
9	MTL_R[5]	Output	3.3-V LVTTL
10	MTL_R[6]	Output	3.3-V LVTTL
11	-	-	-
12	-	-	-
13	MTL_R[7]	Output	3.3-V LVTTL
14	MTL_G[0]	Output	3.3-V LVTTL
15	MTL_G[1]	Output	3.3-V LVTTL
16	MTL_G[2]	Output	3.3-V LVTTL
17	MTL_G[3]	Output	3.3-V LVTTL

18	MTL_G[4]	Output	3.3-V LVTTL
19	-	-	-
20	-	-	-
21	MTL_G[5]	Output	3.3-V LVTTL
22	MTL_G[6]	Output	3.3-V LVTTL
23	MTL_B[0]	Output	3.3-V LVTTL
24	MTL_G[7]	Output	3.3-V LVTTL
25	MTL_B[1]	Output	3.3-V LVTTL
26	MTL_B[2]	Output	3.3-V LVTTL
27	MTL_B[3]	Output	3.3-V LVTTL
28	MTL_B[4]	Output	3.3-V LVTTL
29	-	-	-
30	-	-	-
31	MTL_B[5]	Output	3.3-V LVTTL
32	MTL_B[6]	Output	3.3-V LVTTL
33	MTL_B[7]	Output	3.3-V LVTTL
34	-	-	-
35	MTL_HSD	Output	3.3-V LVTTL
36	MTL_VSD	Output	3.3-V LVTTL
37	MTL_TOUCH_I2C_SCL	Output	3.3-V LVTTL
38	MTL_TOUCH_I2C_SDA	Inout	3.3-V LVTTL
39	MTL_TOUCH_INT_n	Input	3.3-V LVTTL
40	-	-	-

3.3 Using LCD

The LCD features 800x480 pixel resolution and runs at 33 MHz pixel rate. There is no configuration required to drive the LCD. The timing specification is defined as in the **Table 3-2**.

Table 3-2 LCD Timing Specifications

Item	*Typical Value*	*Unit*
Pixel Rate	33	MHz
Horizontal Period	1056	Pixel
Horizontal Pulse Width	30	Pixel
Horizontal Back Porch	16	Pixel
Horizontal Front Porch	210	Pixel
Horizontal Valid	800	Pixel
Vertical Period	525	Line
Vertical Pulse Width	13	Line
Vertical Back Porch	10	Line
Vertical Front Porch	22	Line
Vertical Valid	480	Line

3.4 Using Terasic Multi-touch IP

Terasic Multi-touch IP is provided for developers to retrieve user inputs, including multi-touch gestures and single-touch. The file name of this IP is **i2c_touch_config** and it is encrypted. To compile projects with this IP, users need to setup its license first. For license setup, please refer to Chapter 1 of this document. The license file is located at:

MTL System CD\License\license_multi_touch.dat

The IP decodes I2C information and outputs coordinates and gesture information. The inputs and outputs of this IP module is shown below:

```
module i2c_touch_config  (
            // Host Side
            iCLK,
            iRSTN,
            iTRIG,
            oREADY,
            oREG_X1,
            oREG_Y1,
            oREG_X2,
            oREG_Y2,
            oREG_TOUCH_COUNT,
            oREG_GESTURE,
            // I2C Side
            I2C_SCLK,
            I2C_SDAT
);
```

The purpose of signals for this IP is described in **Table 3-3.** The IP requires a 50 MHz signal as a reference clock to the **iCLK** pin and system reset signal to the **iRSTN**. **iTRIG**, The signals of **I2C_SCLK**, and **IC2_SDAT** pins should be connected to the MTL_TOUCH_INT_n, MTL_TOUCH_I2C_SCL, and MTL_TOUCH_I2C_DAT signals in the 2x20 GPIO header, respectively. When the **oREADY** rises, it indicates touch activity, and the associated information can be collected from the oREG_X1, oREG_Y1, oREG_X2, oREG_Y2, oREG_TOUCH_COUNT, and oREG_GESTURE pins.

When touch activity occurs, the control application should check whether the value of oREG_GESTURE matches a pre-defined gesture ID defined in **Table 3-3**. If it is not a gesture, it indicates a single-touch has occurred and the relative X/Y coordinates can be derived from oREG_X1 and oREG_Y1.

Table 3-3 Definition of Terasic Multi-touch IP Signals

Pin Name	*Direction*	*Description*
iCLK	Input	Connect to 50MHz clock
iRSTN	Input	Connect to system reset signal
iTRIG	Input	Connect to interrupt pin of touch IC
oREADY	Output	Triggered when the data of following six

		outputs are valid
oREG_X1	Output	10-bit X coordinate of first touch point
oREG_Y1	Output	9-bit Y coordinate of first touch point
oREG_X2	Output	10-bit X coordinate of second touch point
oREG_Y2	Output	9-bit Y coordinate of second touch point
oREG_TOUCH_COUNT	Output	2-bit touch count. Valid value is 0, 1, or 2.
oREG_GESTURE	Output	8-bit gesture ID (See Table 3-4)
I2C_SCLK	Output	Connect to I2C clock pin of touch IC
I2C_SDAT	Inout	Connect to I2C data pin of touch IC

The gestures and IDs supported are shown in **Table 3-4**.

Table 3-4 Gestures and Its IDs

Gesture	*ID (hex)*
One Point Gesture	
North	0x10
North-East	0x12
East	0x14
South-East	0x16
South	0x18
South-West	0x1A
West	0x1C
North-West	0x1E
Rotate Clockwise	0x28
Rotate Anti-clockwise	0x29
Click	0x20
Double Click	0x22
Two Point Gesture	
North	0x30
North-East	0x32
East	0x34
South-East	0x36
South	0x38
South-West	0x3A
West	0x3C
North-West	0x3E
Click	0x40
Zoom In	0x48
Zoom Out	0x49

Note: The Terasic IP Multi-touch IP can also be found under the \IP folder in the system CD, as well as the reference designs.

Chapter 4

Linux BSP

This chapter describes how to use the Linux BSP (Board Support Package) provide by Terasic. Users can develop touch-screen GUI program easily with the BPS even without support from Linux X Window.

4.1 Board Support Package

Figure 4-1 shows the block diagram of Linux BSP for DE1-SoC-MTL kit. The BPS incudes three major parts:

- Linux image files
- Quartus project
- QT library and touch-screen library

The Linux image files are implemented on HPS/ARM and the Quartus project is implemented on FPGA/Qsys. The Linux image files include the pre-built Linux system. Users can create a Linux bootable microSD card with the image files. The Quartus project includes the controller for VGA display and the touch-screen controller for touch-screen panel.

The BSP includes not only precompiled QT library and touch-screen library in the Linux image files, but also the document that show how to cross-compile these libraries, as well as to develop touch-screen GUI program based on these libraries.

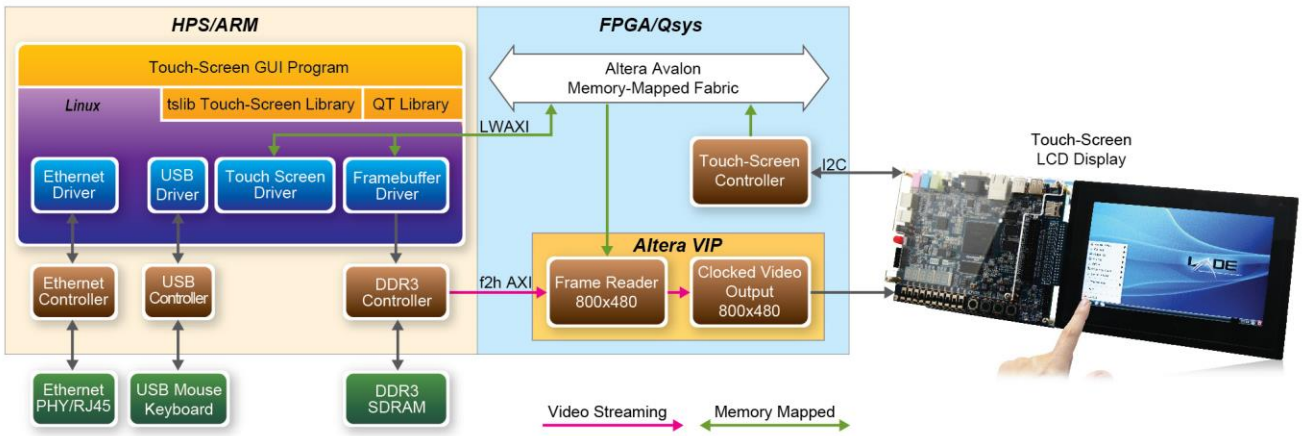

Figure 4-1 Block diagram of Linux BSP for DE1-SoC-MTL kit

4.2 Linux Image Files

Two Linux image files below are provided for DE1-SoC-MTL.

- Linux console with frame buffer
- LXDE desktop

These Linux image files are available from the link: http://cd-de1-soc-mtl.terasic.com. Developers can use a tool named **Win32 Disk Imager** to write the image file into a microSD card. For details about how to create a bootable microSD card or booting Linux from the DE1-SoC board, please refer to the chapter 5 of DE1-SoC_Getting_Started_Guide.pdf, which is included in the DE1-SoC System CD, which is available from the link: http://cd-de1-soc.terasic.com.

Linux Console

Figure 4-2 shows a screenshot of Linux console with frame buffer. The console is displayed on the LCD touch panel. A microSD card with minimal 4GB capacity is required.

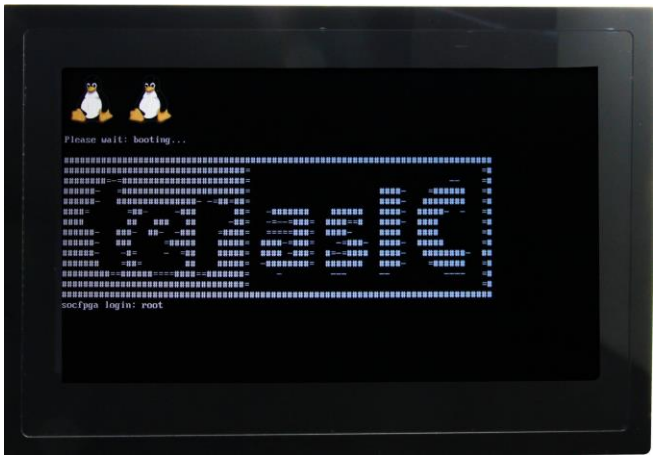

Figure 4-2 Screenshot of Linux console

This Linux image file also includes the QT library and touch-screen library for users to develop touch-screen GUI program based on these two libraries.

To execute the **ts_test** demo included in the touch-screen library,

1. Type "cd /usr/loca/tslib-altera-soc/bin" and press Enter
2. Type "./ts-test" and press Enter to launch, as shown in Figure 4-3.

To execute the **affine** demo included in the QT library,

1. Type "cd /usr/local/qt-4.8.5-tslib-altera-soc/demos/affine" and press Enter
2. Type "./affine -qws" and press Enter launch, as shown in Figure 4-4.

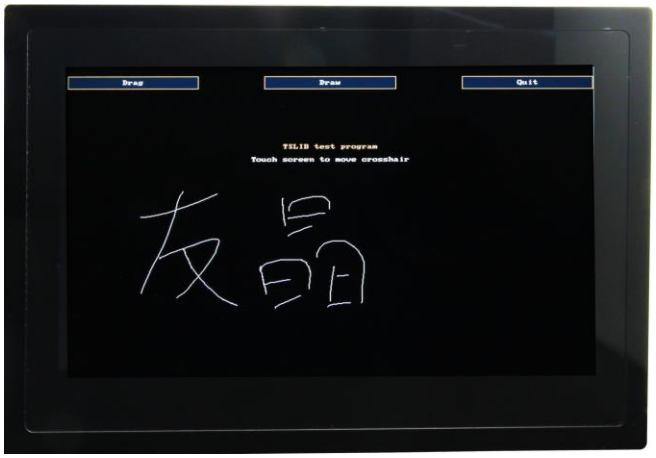

Figure 4-3 Touch-screen ts-test demo

Figure 4-4 QT affine demo

LXDE Desktop

Figure 4-5 shows a screenshot of LXDE desktop after login. The LXDE desktop is displayed on the LCD touch panel. This image file also includes the QT library and touch-screen library. To perform this demo, users need to enter the terminal without Linux X Window by pressing “CTRL+ALT+F1” or “CTRL+ALT+F2”. Press “CTRL+ALT+F7” to return to the LXDE desktop.

Figure 4-5 Screenshot of LXDE desktop

4.3 Quarts Project

The Quartus project is designed based on Altera Qsys tool. There are three major parts:

- VGA display
- Touch-screen
- HPS component

The VGA display part is designed to display the Linux console or desktop on the LCD touch panel. Altera Video and Image Processing (VIP) suite is used to implement this function. The Linux frame buffer driver fills up the DDR3 with data to be displayed, and the VIP frame-reader component reads the data from the DDR3 in a DMA manner. The video data is streamed into the VIP Clocked Video Output component. Finally, the VIP Clocked Video Output component drives the VGA DAC chip to display the video data.

A customized component developed by Terasic in Qsys is used to communicate with the touch-screen panel. The component interfaces with the touch-screen panel through I2C-like protocol, and reports the status of touch-screen panel through a parallel bus.

The HPS component acts as a bridge between ARM and FPGA. Program running on ARM can communicate with FPGA through memory-mapped interface. The Quartus project is located under the folder “Demonstrations/SoC/MTL_HPS” in the DE1-SoC-MTL system CD.

4.4 QT and Touch-screen Libraries

Users can develop touch-screen GUI program based on the QT and touch-screen libraries. For more information, please refer to the document “**Software Development Guide for touch-screen display.pdf**” included in the DE1-SoC-MTL system CD. The precompiled libraries can be found from the folder “Demonstrations/SoC/Libraries” in the DE1-SoC-MTL system CD.

Chapter 5

Painter Demonstration

This chapter shows how to implement a painter demo on the Multi-touch LCD module based on Altera Qsys tool and the Video and Image Processing (VIP) suite. It demonstrates how to use multi-touch gestures and single-touch resolution. The GUI of this demonstration is controlled by the program in Nios II.

5.1 Operation Description

Figure 5-1 shows the Graphical User Interface (GUI) of Painter demo. The GUI is classified into four separate areas: Painting Area, Gesture Indicator, Clear Button, and Color Palette. Users can select a color from the color palette and start painting in the paint area. If a gesture is detected, the associated gesture symbol will be shown in the gesture area. To clear the painting area, click the "Clear" button.

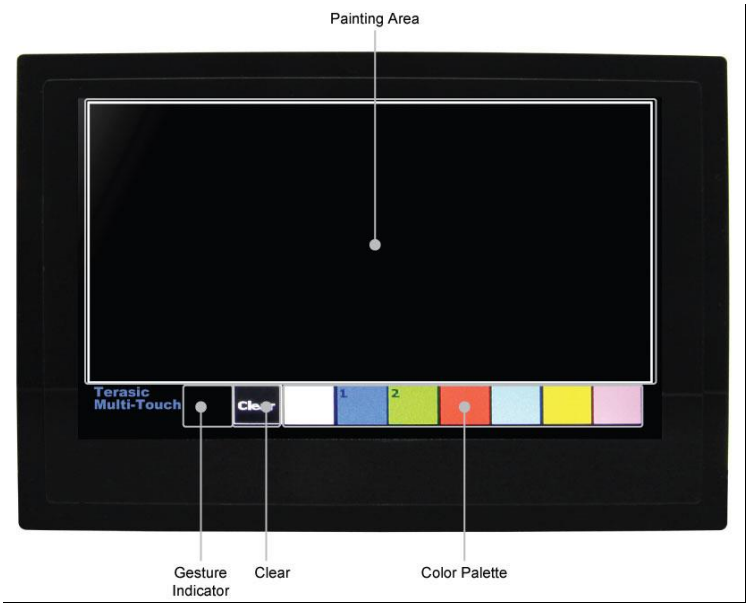

Figure 5-1 GUI of Painter Demo

Figure 5-2 shows the single-finger painting of canvas area.

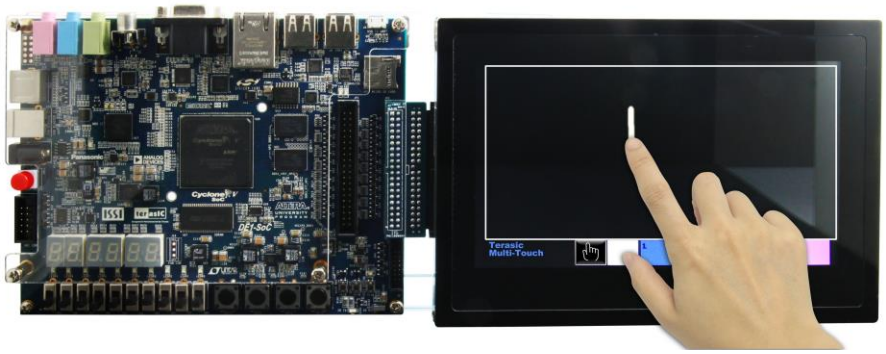

Figure 5-2 Single-finger painting

Figure 5-3 shows the counter-clockwise rotation gesture.

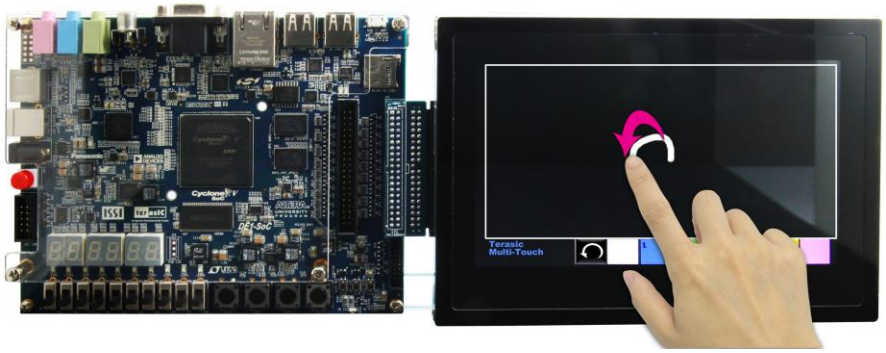

Figure 5-3 Counter-clockwise rotation gesture

Figure 5-4 shows the zoom-in gesture.

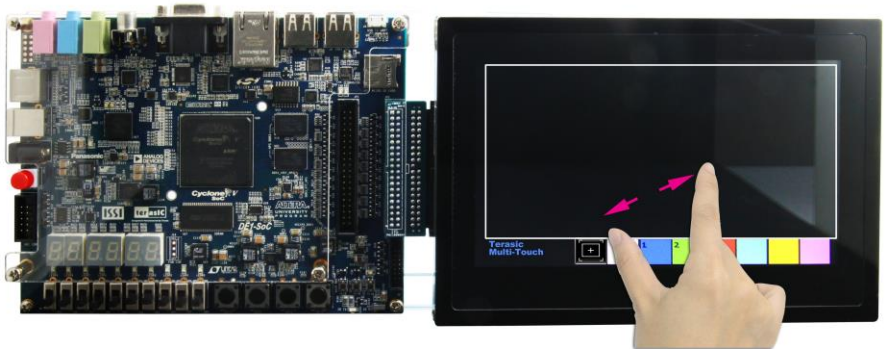

Figure 5-4 Zoom-in gesture

5.2 System Description

For LCD display processing, the reference design is developed based on Altera's Video and Image Processing (VIP) suite. The Frame Reader VIP is used for reading data to be displayed from the associated video memory, and the VIP Video Out is used to display the video data. The data is drawn by the Nios II processor according to user input.

For multi-touch processing, Terasic memory-mapped IP is used to retrieve user input, including multi-touch gestures and single-touch coordinates. For more information about this IP, please refer to the Chapter 3 of this document. Note: the license for this IP must be installed before compiling the Quartus II project including this encrypted component.

Figure 5-5 shows the system generic block diagram of painter demonstration.

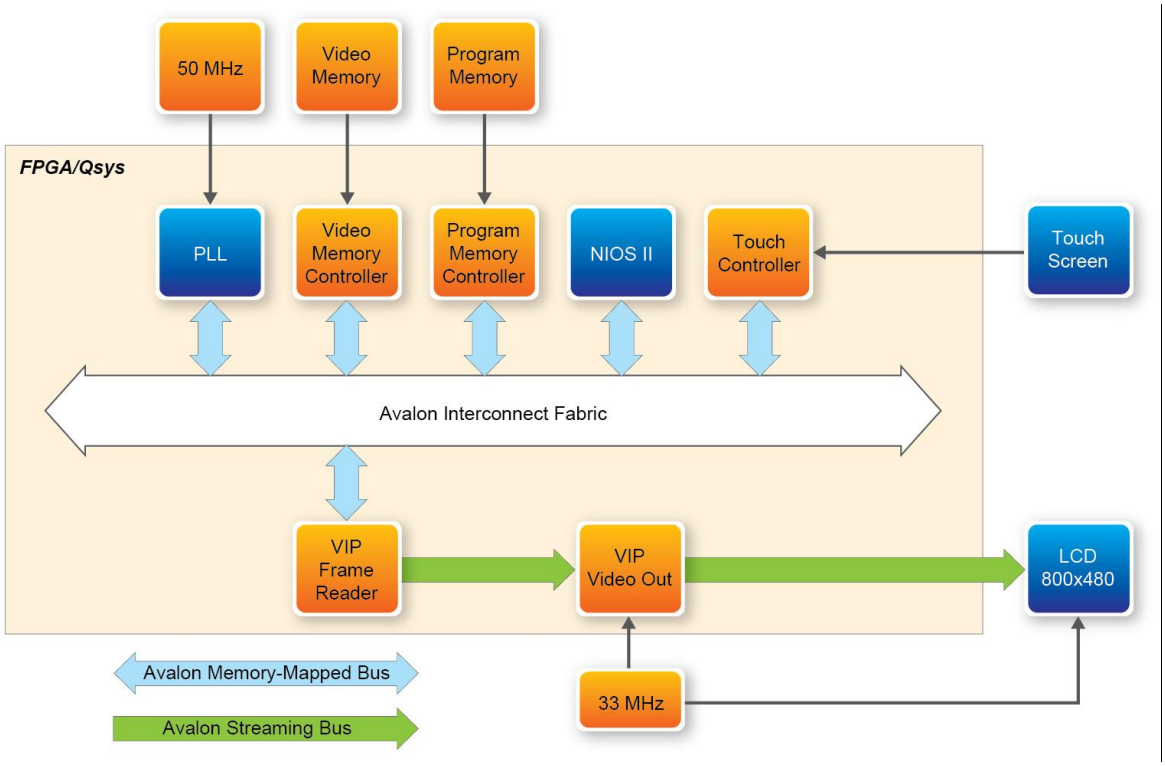

Figure 5-5 System block diagram of painter demonstration

5.3 Demonstration Setup

Please follow the procedures below to setup the demonstration:

1. Connect the DE1-SoC-MTL USB-Blaster II USB port to the PC USB Port with a USB Cable.
2. Power on the DE1-SoC-MTL.
3. Please make sure Quartus II v13.0 has been installed on the host PC.
4. Copy the folder \Demonstrations\FPGA\DE1_SoC_MTL_PAINTER\demo_batch from the DE1-SoC-MTL system CD to the host PC.
5. Execute "DE1_SoC_MTL_PAINTER.bat".
6. The painter GUI will show up on the LCD panel.

5.4 Demonstration Source Code

The locations of this demonstration source code are shown in **Table 5-1.** Note: The project is built under Quartus II v13.0. Both Altera VIP license and Terasic Multi-touch IP license are required to rebuild the project.

Table 5-1 Locations of Painter Demonstration Source Code

Project	*Location*
Quartus II	Demonstrations\FPGA\DE1_SoC_MTL_PAINTER
Nios II	Demonstrations\FPGA\DE1_SoC_MTL_PAINTER\software

Chapter 6

Appendix

6.1 Revision History

Version	Change Log
V1.0	Initial Version (Preliminary)

6.2 Copyright Statement