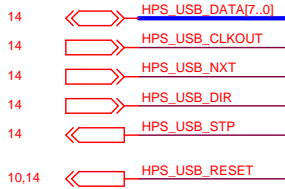
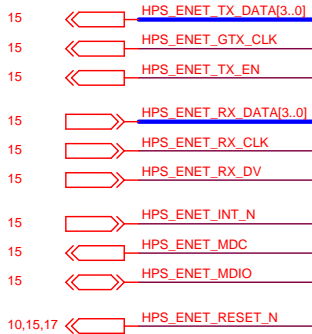


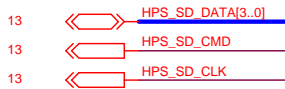
UBS PHY Interface (ULPI)



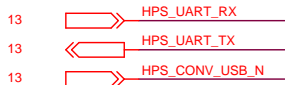
Ethernet PHY Interface (RGMII)



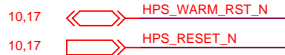
SD Card Interface



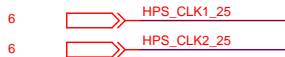
UART Interface



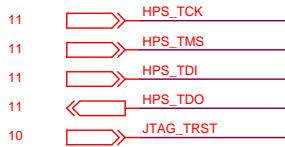
HPS Reset



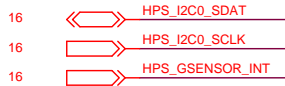
HPS Clock



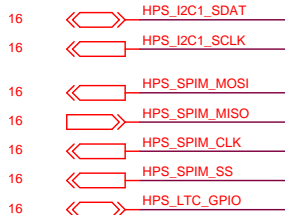
HPS JTAG INTERFACE



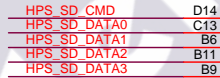
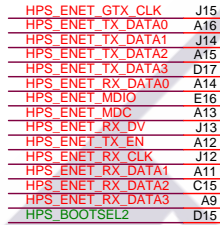
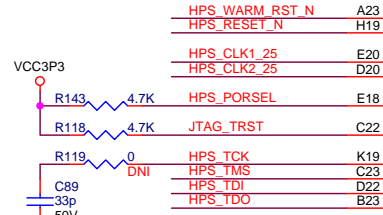
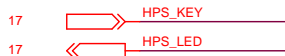
Accelerometer Interface



LTC Interface



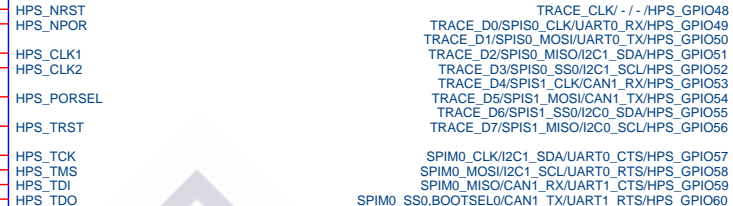
HPS Key and LED



U1M

CYCLONE V SoC BANK 7 (HPS)

Bank 7A
VCCIO = 3.3V



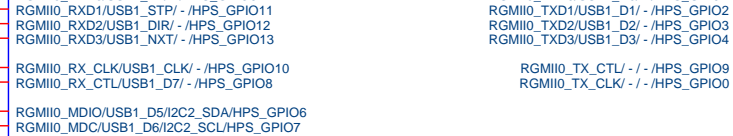
Bank 7B
VCCIO = 3.3V



Bank 7C
VCCIO = 3.3V

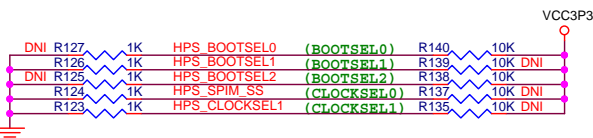


Bank 7D
VCCIO = 3.3V

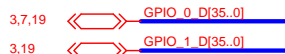


5CSEBA6U2317

Default Setting: BOOTSEL[2:0]=101 (Boot from SD CARD)
CLKSEL[1:0] =00



GPIO



User Interface (FPGA)



FPGA_CLK1_50 V11
 GPIO_0_D25 W11
 GPIO_0_D0 V12
 GPIO_0_D2 W12

FPGA_CLK2_50 Y13
 GPIO_0_D34 AA13
 GPIO_1_D0 Y15
 GPIO_1_D2 AA15

SW0 Y24
 SW1 W24
 SW2 W21
 SW3 W20

FPGA_CLK1_50 R159 0
 FPGA_CLK3_50 E11
 GPIO_0_D3 D11
 GPIO_0_D18 D12
 GPIO_0_D18 C12

CYCLONE V SoC Clock

Bank 3B VCCIO = 3.3V

IO_3B/CLK0P,FPLL_BL_FBP/DIFFIO_RX_B15P
 IO_3B/CLK0N,FPLL_BL_FBN/DIFFIO_RX_B15N
 IO_3B/CLK1P/DIFFIO_RX_B23P
 IO_3B/CLK1N/DIFFIO_RX_B23N

AG5 HDMI_TX_CLK
 AH4 HDMI_TX_D18

Bank 4A VCCIO = 3.3V

IO_4A/CLK2P/DIFFIO_RX_B31P
 IO_4A/CLK2N/DIFFIO_RX_B31N
 IO_4A/CLK3P/DIFFIO_RX_B39P
 IO_4A/CLK3N/DIFFIO_RX_B39N

Bank 5B VCCIO = 3.3V

IO_5B/CLK4P,FPLL_BR_FBP/DIFFIO_RX_R23P
 IO_5B/CLK4N,FPLL_BR_FBN/DIFFIO_RX_R23N
 IO_5B/CLK5P/DIFFIO_RX_R21P
 IO_5B/CLK5N/DIFFIO_RX_R21N

AB26 GPIO_0_D31
 AA26 GPIO_0_D33

Bank 8A VCCIO = 3.3V

IO_8A/CLK6P,FPLL_TL_FBP/DIFFIO_RX_T9P
 IO_8A/CLK6N,FPLL_TL_FBN/DIFFIO_RX_T9N
 IO_8A/CLK7P/DIFFIO_RX_T1P
 IO_8A/CLK7N/DIFFIO_RX_T1N

E8 GPIO_0_D1
 D8 GPIO_0_D4

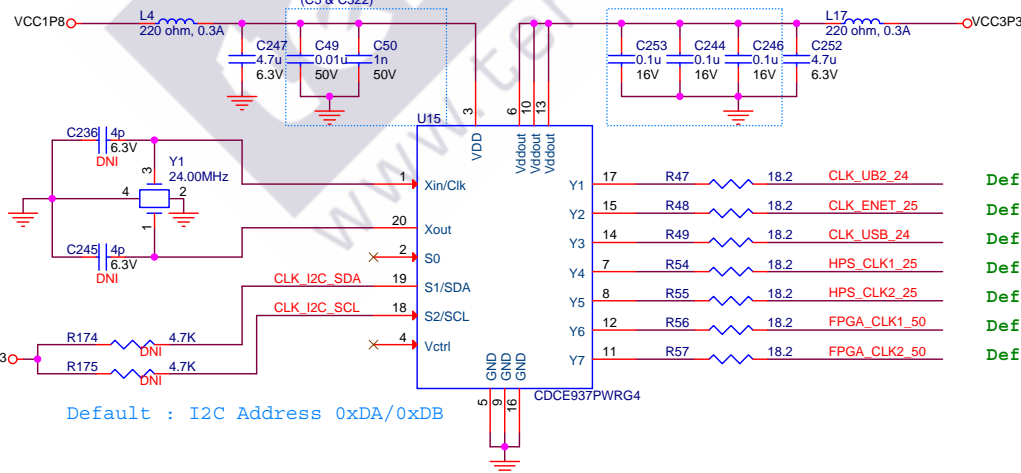
5CSEBA6U2317

Factory Default Configuration:

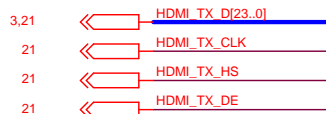
50MHz x2
 25MHz x3
 24MHz x2

CAD Note:
 Place near pin 3 and 5
 (C3 & C322)

CAD Note:
 Place near IC power pin



HDMI TX



Default: 24MHz
 Default: 25MHz
 Default: 24MHz
 Default: 25MHz
 Default: 25MHz
 Default: 50MHz
 Default: 50MHz

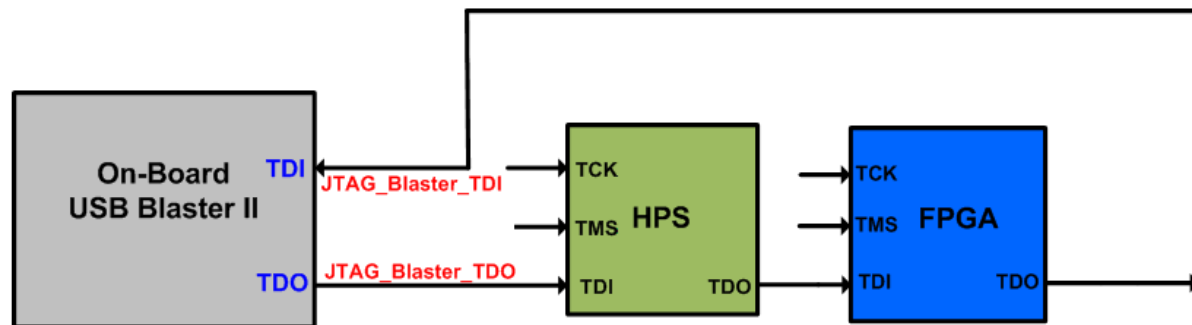
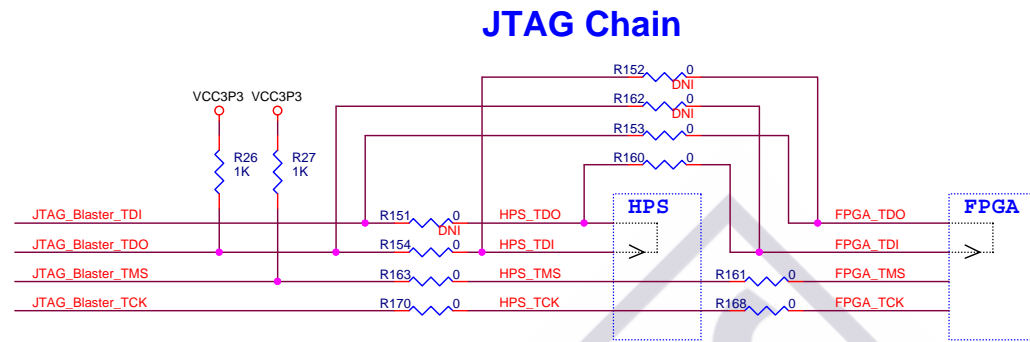
Diagram showing the JTAG Blaster pins:

- JTAG Blaster_TCK
- JTAG Blaster_TMS
- JTAG Blaster_TDO
- JTAG Blaster_TDI

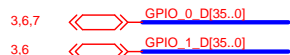
Diagram showing four JTAG pins connected to a device:

- FPGA_TCK
- FPGA_TMS
- FPGA_TDI
- FPGA_TDO

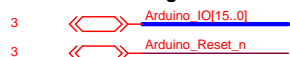
HPS_TCK
 HPS_TMS
 HPS_TDI
 HPS_TDO



GPIO



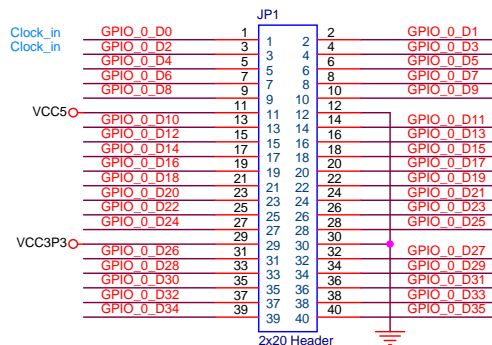
Arduino Digital Interface



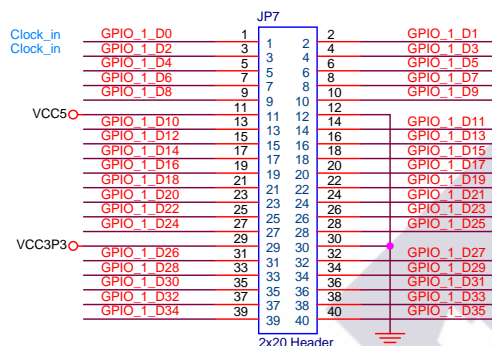
Analog input interface



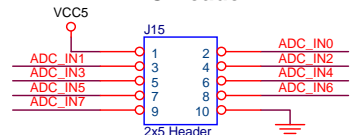
GPIO 0 Header



GPIO 1 Header



ADC Header



Arduino UNO Rev3

