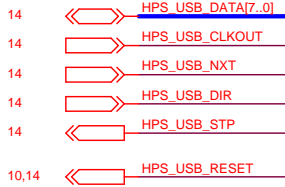
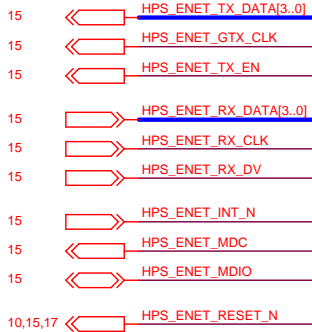


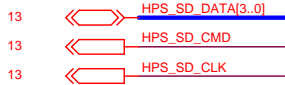
UBS PHY Interface (ULPI)



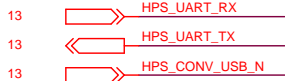
Ethernet PHY Interface (RGMII)



SD Card Interface



UART Interface



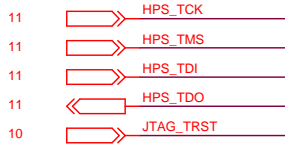
HPS Reset



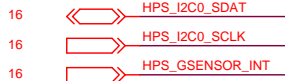
HPS Clock



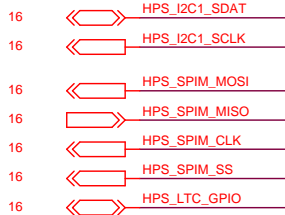
HPS JTAG INTERFACE



Accelerometer Interface



LTC Interface



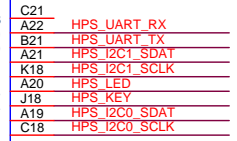
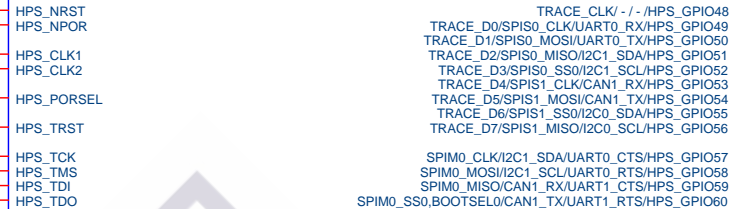
HPS Key and LED



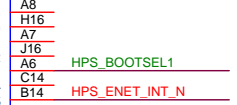
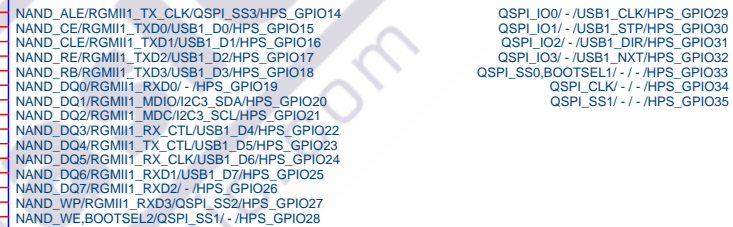
U1M

CYCLONE V SoC BANK 7 (HPS)

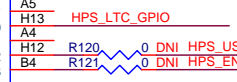
Bank 7A
VCCIO = 3.3V



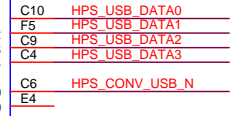
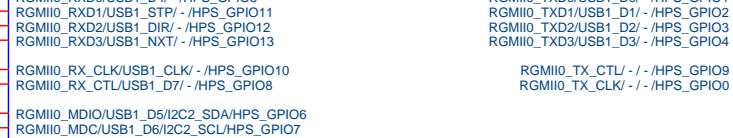
Bank 7B
VCCIO = 3.3V



Bank 7C
VCCIO = 3.3V

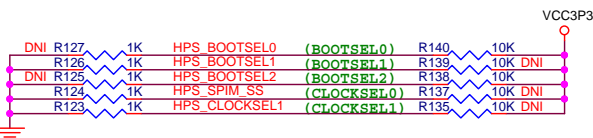


Bank 7D
VCCIO = 3.3V

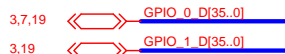


5CSEBA6U2317N

Default Setting: BOOTSEL[2:0]=101 (Boot from SD CARD)
CLKSEL[1:0] =00



GPIO



User Interface (FPGA)



FPGA_CLK1_50 V11
GPIO_0_D25 W11
GPIO_0_D0 V12
GPIO_0_D2 W12

FPGA_CLK2_50 Y13
GPIO_0_D34 AA13
GPIO_1_D0 Y15
GPIO_1_D2 AA15

SW0 Y24
SW1 W24
SW2 W21
SW3 W20

FPGA_CLK1_50 R159 0
FPGA_CLK3_50 E11
GPIO_0_D3 D11
GPIO_0_D16 D12
GPIO_0_D18 C12

CYCLONE V SoC Clock

Bank 3B VCCIO = 3.3V

IO_3B/CLK0P,FPLL_BL_FBP/DIFFIO_RX_B15P
IO_3B/CLK0N,FPLL_BL_FBN/DIFFIO_RX_B15N
IO_3B/CLK1P/DIFFIO_RX_B23P
IO_3B/CLK1N/DIFFIO_RX_B23N

IO_3B/FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTP,FPLL_BL_FB/DIFFIO_TX_B21P/B_A_2/DQ3B
IO_3B/FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTN/DIFFIO_TX_B21N/B_A_3/DQ3B

AG5 HDMI_TX_CLK
AH4 HDMI_TX_D18

Bank 4A VCCIO = 3.3V

IO_4A/CLK2P/DIFFIO_RX_B31P
IO_4A/CLK2N/DIFFIO_RX_B31N
IO_4A/CLK3P/DIFFIO_RX_B39P
IO_4A/CLK3N/DIFFIO_RX_B39N

Bank 5B VCCIO = 3.3V

IO_5B/CLK4P,FPLL_BR_FBP/DIFFIO_RX_R23P
IO_5B/CLK4N,FPLL_BR_FBN/DIFFIO_RX_R23N
IO_5B/CLK5P/DIFFIO_RX_R21P
IO_5B/CLK5N/DIFFIO_RX_R21N

Bank 8A VCCIO = 3.3V

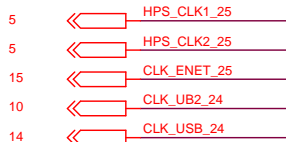
IO_8A/CLK6P,FPLL_TL_FBP/DIFFIO_RX_T9P
IO_8A/CLK6N,FPLL_TL_FBN/DIFFIO_RX_T9N
IO_8A/CLK7P/DIFFIO_RX_T1P
IO_8A/CLK7N/DIFFIO_RX_T1N

IO_8A/FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTP,FPLL_TL_FB/DIFFIO_TX_T4P
IO_8A/FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTN/DIFFIO_TX_T4N

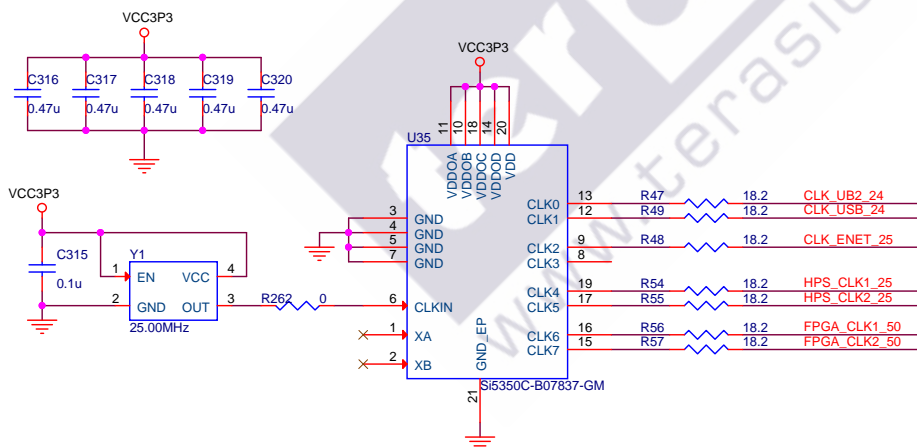
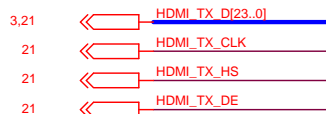
AB26 GPIO_0_D31
AA26 GPIO_0_D33

E8 GPIO_0_D1
D8 GPIO_0_D4

Clock Generator



HDMI TX



Default: 24MHz
Default: 24MHz

Default: 25MHz

Default: 25MHz
Default: 25MHz

Default: 50MHz
Default: 50MHz



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Title

DE10-Nano Board

Size

B

Document Number

FPGA Clock and Clock Generator

Rev

C0

Date:

Wednesday, August 30, 2017

Sheet

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of

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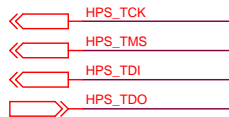
USB Blaster



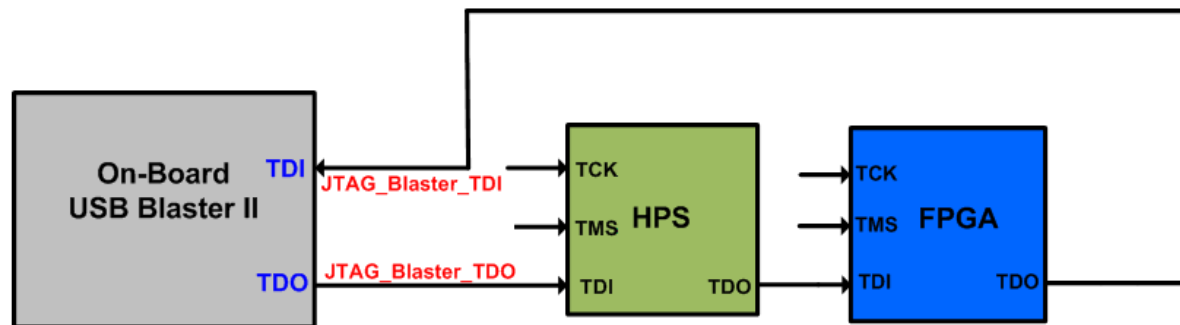
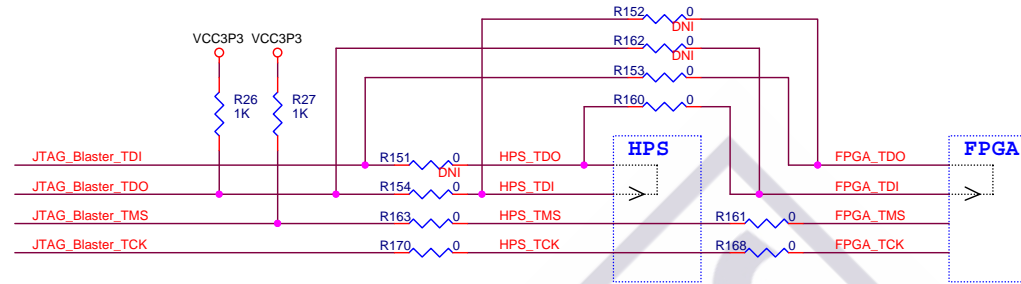
FPGA JTAG INTERFACE



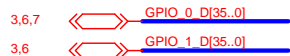
HPS JTAG INTERFACE



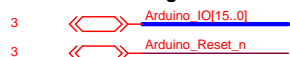
JTAG Chain



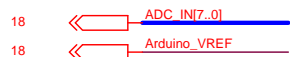
GPIO



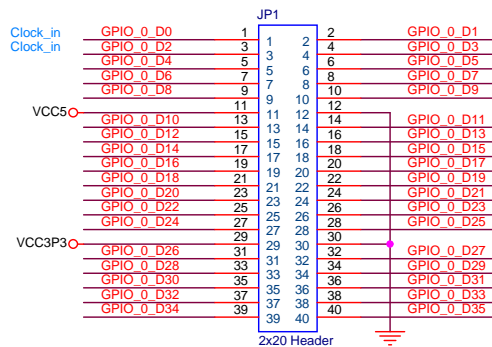
Arduino Digital Interface



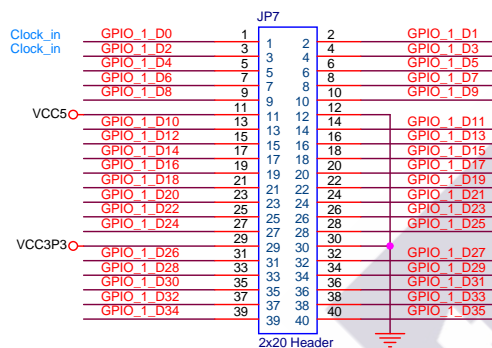
Analog input interface



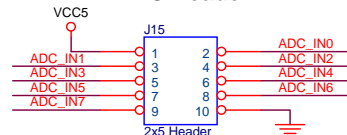
GPIO 0 Header



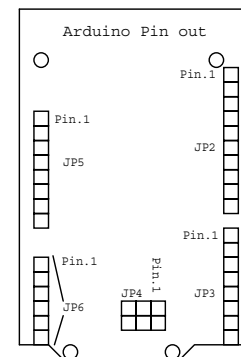
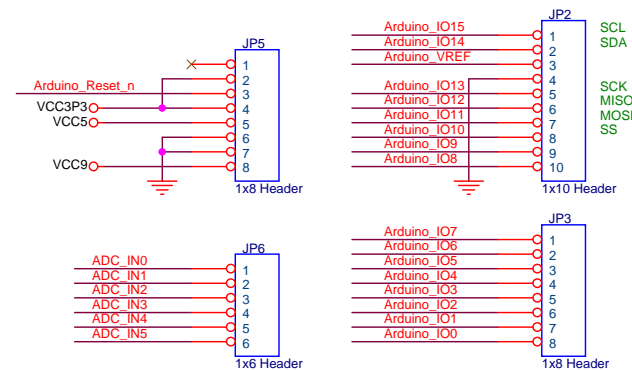
GPIO 1 Header



ADC Header



Arduino UNO Rev3



KEY

KEY[1..0]

SWITCH

SW[3..0]

LED

LED[7..0]

