Confidential

Smartcoder（AU6805）

Specifications

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Pre release version

Preliminary

R E V I S I O N S

No.	DATE	PAGES	DESCRIPTION	DS'D	CH'D	APP'D
1	14. 6. 4	P11,P13,P31,P32	Error correction			

ED'N No. . .

DS' D	DATE	MODEL No.	TITLE
CH' D	'14. 4.16	AU6805	Smartcoder（AU6805） Specifications
APP' D			

DWG NO.	3	4	5	6	7	8	9	10	11	12	SHEET
S P	C	0	0	0	6	3	0	W	0	0	1/39

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Edition No.

1 Scope

This specification document applies to R/D(Resolver/Digital) Conversion IC which is mountable on vehicles(automobiles, trains and so on), uses the time-proven R/D Conversion method "Digital Tracking Method" and provides a low-cost and reliable angle(absolute value) detection system designed to accompany with amplitude modulation method brushless resolver(BRX).

2 Related Document(Referential Drawing)

Attended Figure.3 AU6805 Package Outline Figure

3 Requirements

3.1 Function and Performances

3.1.1 Concept/Feature

- Digital Tracking Method consists of Digital Signal Processing hardware, sustains and improves the conversion performance(resolution, accuracy, tracking speed, noise immunity, etc.) which is equivalent of AU6803 Twin-PLL method, and achieve a low price.
- Capable of building an absolute angle detection system with safety and high reliability by enhancing the failure detection function and incorporating a built-in self-test (BIST) function for the R/D conversion and a failure detection function.
- Simple to use. (All-in-one design; eliminates phase adjustment of exciting signal (i.e. allowable phase angle: ±45 degrees), and others).
- Quality capable of enduring vehicle-mount applications.

3.1.2 Functional Composition

R/D conversion functional composition of Digital Tracking Method refers to Figure 1 Function Configuration Diagram.

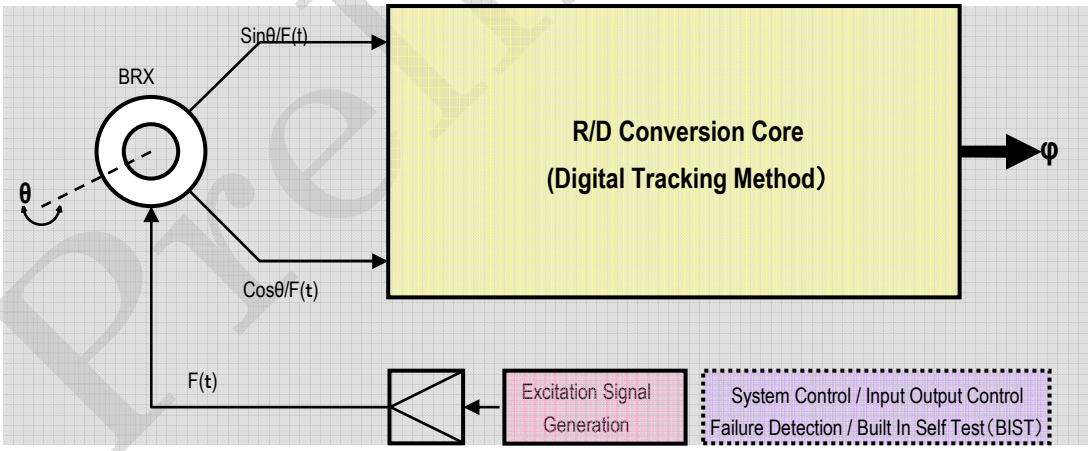

Figure 1 Function Configuration Diagram

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The internal constitution of Digital Tracking R/D conversion IC is shown in Figure 2.

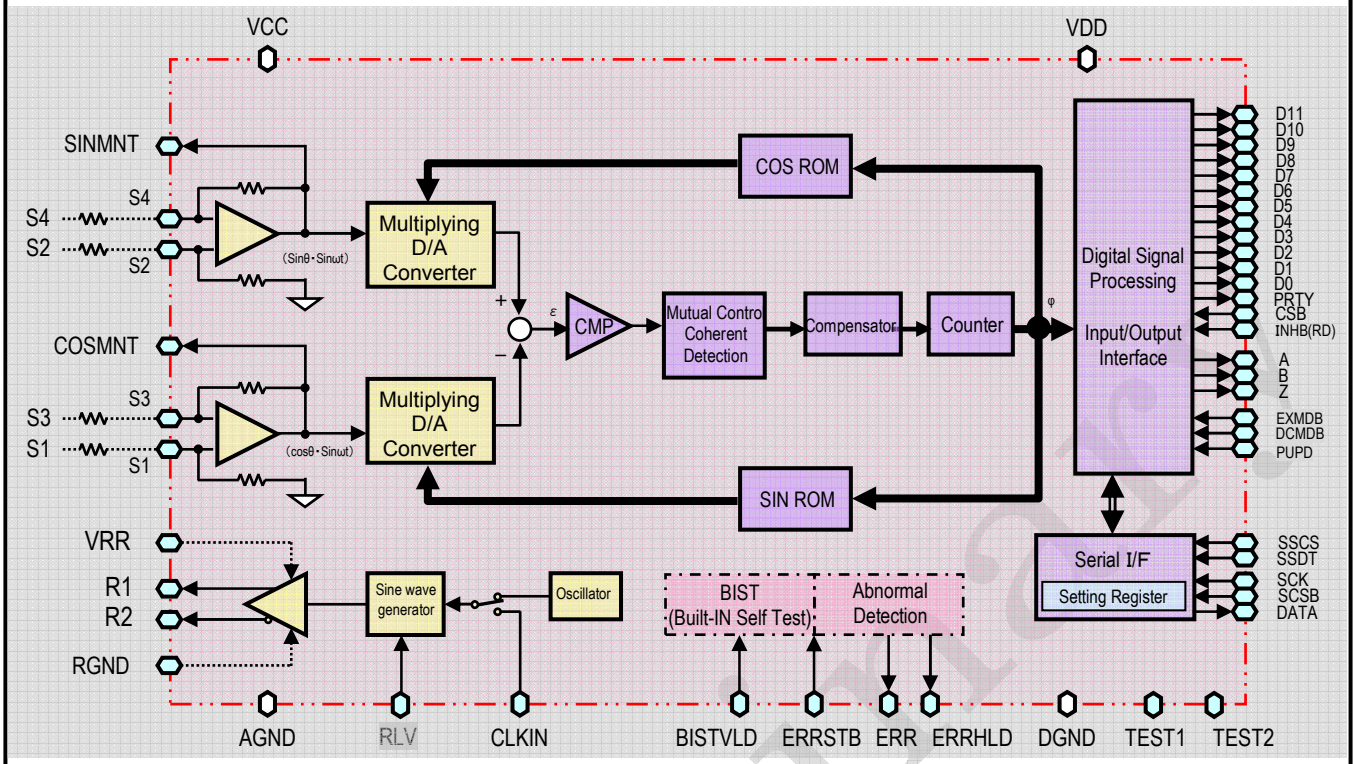

Figure 2.Internal Constitution

3.1.3 Major Functions

(1) R/D Conversion Function

The Digital Tracking Method has a function to convert resolver signal(analogue signal) to 12 bit resolution digital data.

(2) Exciting Signal Output(R1, R2) Generator Function

It has the function to output Sine-wave exciting signal able to excite resolver directly.

This function is able to select the current exciting mode to excite resolver directly from an exciting amplifier embedded internal IC or to excite resolver through current buffer outside after converting voltage output by resistance between R1 terminal and R2 one, and the exciting mode to exciting resolver through current buffer outside after converting voltage output by resistance between R1 terminal and R2 one as written above. The setting method refers to Table 2.

This is an effective method, for improving the S/N ratio for noise immunity, associated with the magnetic leakage flux from the motor, to boost the excitation voltage through an external buffer amplifier, as mentioned in Section 5.3,

(Note 1) Short-circuit of R1 and R2 terminal to GND and power-supply line(VRR, VCC, VDD and etc.) may cause damage. When the waveform between R1 and R2 needs to be checked, observe it as the difference of each waveform of R1 and R2. Never connect the GND of probe directly to the R1 or R2 terminal.

(Note 2) This function is available at H level of both EXMDB and DCMDB.

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(3) Failure Detection Function

It has the function to monitor and detect resolver signal abnormality and IC itself abnormality(R/D conversion function, etc.) This function is independent from R/D conversion and doesn't constrain R/D conversion output with or without failure detection result. Also, failure detection result output in ERR and ERRHLD terminals. The detection contents are as follow;

A) Resolver signal abnormality: Detect the disturbance in the resolver signal balance such as exciting line(R1, R2) disconnection(including loose connection), exciting signal down(exciting signal output circuit down, short circuit between line, etc.), shot circuit between signal line(S1-S3, S2-S4), or rare short circuit of resolver winding wire and so on.

B) Resolver signal disconnection: Detect resolver signal(S1-S4) line disconnection (including loose connection) in full angle range by the DC-bias method.

C) R/D conversion abnormality: Monitor error deviation of R/D conversion loop and detect operation abnormality R/D conversion function(IC itself).

D) Abnormal High Temperature inside IC: It is detected, when the inside temperature exceeds approximately 150 ˚C.

(4) Built-In Self Test(BIST) Function

This converter has a built-in self test function that generates an intentional simulated signal input inside the R/D converter IC by setting the BIST command (BISTVLD) terminal and observes the output signal to the simulated signal input to determine the validity of operation. The details of the diagnosis are described below.

A) Angle Conversion BIST: Run Built-In Self Test(BIST) for R/D conversion function and set 0°, 45°or 270°(electric angle) as resolver signal.

B) Failure Detection BIST: Run Built-In Self Test(BIST) of failure Detection function shown in C) as follows;

- ■ Resolver signal abnormal detection BIST: "Resolver signal abnormality" detect function Built-In Self Test
- ■ Resolver signal disconnection detection BIST**:** "Resolver signal disconnection" detect function Built-In Self Test
- ■ Conversion abnormality BIST: "R/D conversion abnormality" detect function Built-In Self Test

Each output operates on BIST for a trial signal.
Also, be sure to reset error(refer to Figure 17) after Built-In Self Test(BIST).

(5) Serial input setting function

You can change setting register content shown in Table 1 with serial input. Setting register is 12 bit register built in IC to set functional usage environment like IC operating conditions of R/D conversion IC and default value below is automatically set without setting with serial input.

Serial input setting operation waveform is shown in Figure 3.After "SSDT" setting input once set fronting setting register serially in "SCK" input falling when "SSCS" input is active("L" level), set setting register at "SSCS" input start-up and update system(setting change).Until system is updated, normal system setting condition is maintained, all settings are reset by power discontinuity or system reset(reboot).Also, on Built-In Self Test(BIST) and special mode, by "BISTVLD" input, you can control on/off of Built-In Self Test(BIST) operation setting or special mode setting in BIT(BIT No.7-10).

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(Note 1) The contents of the setting register set in this paragraph and the following paragraph (6) are to be periodically checked through the serial output (Settings of [10] & [11]). The "SSCS" input terminal should be connected to the power supply (VDD) when the serial input is not set.
(Note 2)Do not perform serial input set sequence during 5ms after start up or reset(reboot).

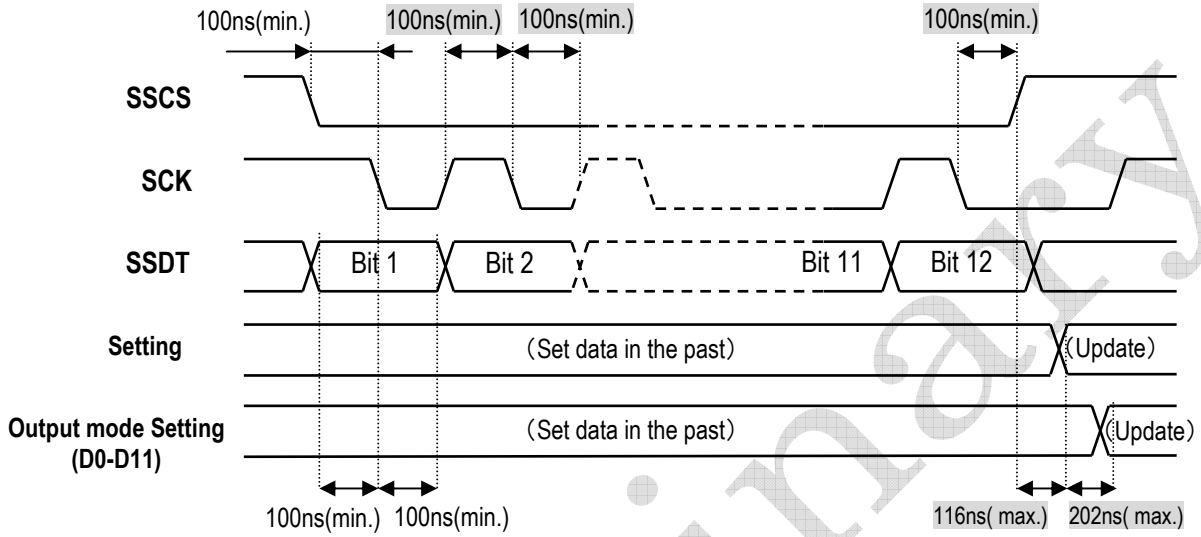

Figure 3. Serial Input Setting operation waveform

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Table 1 Serial Input "Setting Resister" Contents

BIT No.	Item	Set Contents		
1	Output Mode Setting (D0-D11)	[0]: absolute-value(φ1-φ12) Parallel Angle Data [1]: equivalent Encoder Pulse(A,B,Z,U,V,W)		
2	Excitation Signal Operation Clock Selection	[0]: Internal Oscillator [1]: External Clock Input		
3 4	Serial Output Mode Setting [BIT 4,3]	[00]: absolute-value(φ1-φ12) Angle Data [01]: equivalent Encoder Pulse(A,B,Z,U,V,W) [10]:Serial Callback(Setting Resister Confirmation [11]: Failure Detection / BIST(Built In Self Test) Result		
5 6	Loop Gain Setting [BIT 6,5]		Loop Gain Setting Group A [BIT 11] = [0]	Loop Gain Setting Group B [BIT 11] = [1]
		[00]	Fixed Value(1) (Bandwidth 800Hz(typ.) equiv.)	Fixed Value(5) Bandwidth 1,000Hz(typ.)equiv.
		[01]	Fixed Value(2) (Bandwidth 2,000Hz(typ.) equiv.)	Fixed Value(6) Bandwidth 500Hz(typ.)equiv.
		[10]	Fixed Value(3) (Bandwidth 2,500Hz(typ.) equiv.)	Fixed Value(7) Bandwidth 200Hz(typ.)equiv.
		[11]	Fixed Value(4) (Bandwidth 1,500Hz(typ.) equiv.)	Loop Gain Automatic Adjuster (Automatic Change between bandwidth 220Hz-460KHz(typ.))
7 8 9 10	BIST(Built In Self Test) Setting & Special Mode Setting [BIT 10,9,8,7]	[0000]:BISTVLD(Input) Invalid [0001]:Reserved(Do Not Use) [0010]:Reserved(Do Not Use) [0011]:Reserved(Do Not Use) [0100]:Reserved(Do Not Use) [0101]:Angle Conversion BIST: Ordered Angle1(0°) [0110]:Angle Conversion BIST: Ordered Angle 2(45°) [0111]:Angle Conversion BIST: Ordered Angle 3(270°) [1000]:Reserved(Do Not Use) [1001]:Failure Detection BIST: Failure Detection BIST Of Resolver Signal [1010]:Failure Detection BIST: Disconnection Detection BIST of Resolver Signal(COS Side) [1011]:Failure Detection BIST: Disconnection Detection BIST of Resolver Signal(SIN Side) [1100]:Failure Detection BIST: Conversion Abnormality BIST [1101]:System Reset(Re-Boot) [1110]:Serial Absolute-Value Output16 BIT Mode [1111]:Reserved(Do Not Use)		
11	Loop Gain Setting Group Selection	[0]: Group A(* Refer to Loop Gain Setting[BIT 6,5]) [1]: Group B(*Refer to Loop Gain Setting[BIT 6,5])		
12	Thresholds Setting For Resolver Signal Abnormality	[0]:0.1xVCC [Vp-p] [1]:0.14xVCC [Vp-p]		

(Note) Setting default value is [0] in all BIT except requirement described in the next(6).

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(6) Default Value Setting Function

It has the function to detect voltage level as input terminal in power-on or system reset(reboot) with addition pull-up resistance(10kΩ) or pull-down resistance 10kΩ to output terminal and set setting register to the default value shown in Table 2.

Table 2 Default Value Set Contents

Terminal No	Signal Name	Set Item	Pull-up Register(10kΩ)	Pull-down Register(10kΩ)	Register to be set
39	ERRHLD	Output Mode Setting(D0-D11)	Absolute Parallel Angle Data(φ1-φ12)	Encoder equivalent Pulse (A,B,Z,U,V,W)	Bit 1
41	ERR	Exciting Signal Operation Clock Selection	Internal Oscillator Selection	External Clock Input	Bit 2
44	Z	Exciting Mode Setting	Current Excitation Mode (VMD="0")	Voltage Excitation Mode (VMD="1")	Incapable of serial setting

(7) R/D Conversion Data(parallel) Output Function

It has the function to select output terminal(D0-D11) to absolute parallel output mode or encoder equivalent pulse output mode with "Output Mode Setting" of Setting register BIT NO.1.

Output Signal Format is shown in Table 3.

Table 3 Output Signal Format(D0-D11)

Output	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11
Absolute-value Output Mode Setting[0]	LSB φ12	φ11	φ10	φ9	φ8	φ7	φ6	φ5	φ4	φ3	φ2	MSB φ1
Pulse Output Mode Setting[1]	Encoder Equivalent Pulse						-	ERR	ERR HLD	ERR CD1	ERR CD2	ERR CD3
	A	B	Z	U	V	W						

Two types of output mode is able to select by bus I/F control signal(CSB) below.

- ✧ Parallel Bus Interface Mode
- ✧ Parallel I/O Interface Mode(standalone)

Also, "ERR CD1-3" in the table shows failure contents as error code and details are shown in Table 4.When some errors occur, only higher-priority error codes are shown and the error codes area cleared in the "ERRHLD" output by error reset input("ERRSTB").

Table 4 Error Code List(Failure Detection Result)

ERR CD3	ERR CD2	ERR CD1	Error Contents(Failure Detection Result)	Priority	Note
0	0	0	Normal	-	No Error
0	0	1	Resolver Signal Abnormality	3	
0	1	0	Disconnection Detection BIST of Resolver Signal(COS Side)	1	
0	1	1	Disconnection Detection BIST of Resolver Signal(SIN Side)	2	
1	0	0	R/D Conversion Abnormality	4	
1	0	1	(Undefined)	-	
1	1	0	Anomalous Warmth of internal IC(about over 150°)	5	
1	1	1	Error Mask on start-up(After Reset Release)	-	Refer to Fig.19

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(8) Encoder Equivalent Pulse Output Function

IC has output function to convert R/D converting absolute value angle data to Encoder equivalent pulse by logical transform below. Encoder equivalent pulse output may have a gap for absolute value angle data on resolver rotation direction because of inserted 1bit hysteresis circuit for chattering eliminator.

Moreover, A, B and Z have independent output terminal and can output constantly.

- ✧ Output phase: A, B, Z, U, V, W
- ✧ Number of pulses (A, B): 1,024 P/T(electrical angle)

Operation Waveform of encoder equivalent pulse output is shown in Figure 4.

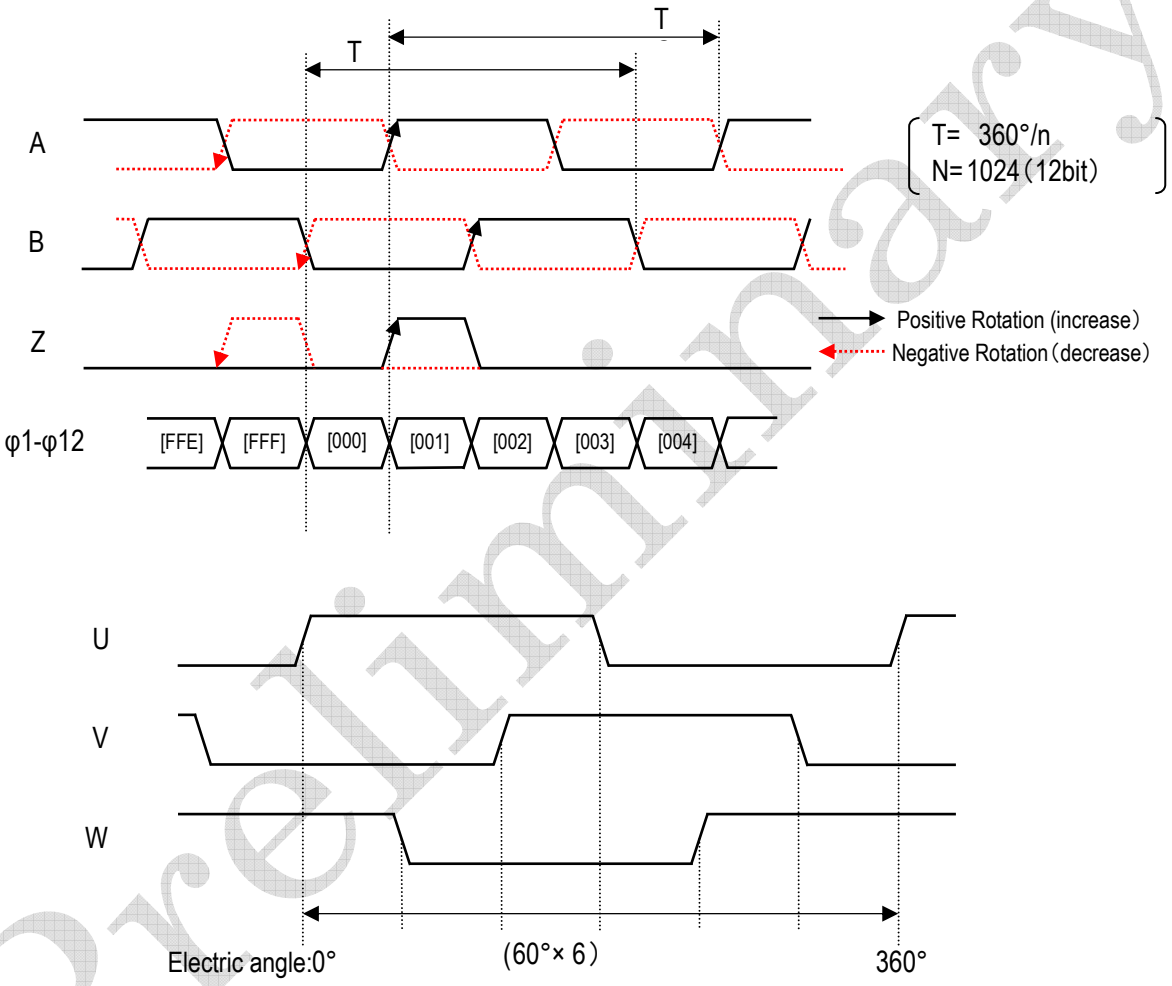

Figure 4. Operation Waveform of Encoder Equivalent Pulse

(Note) The pulses equivalent to an encoder may chatter at the edge of switching in some operating conditions. Note that the phase difference between A and B pulses and the width of pulses, etc. may be significantly disarranged. For purposes of preventing accumulation of angle error caused by chattering and electronic noise, etc., use a reversible counter on the signal processor side if using both A and B pulses.

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(9) Serial Output Function

This converter has a function that transmits the signal shown in Table 5 in serial by setting the serial output mode in the setting register Bit Nos. 3 & 4. The "DATA" output transmits the latest information in serial format with synchronization to the external clock ("SCK") at the time when "SCSB" input falls down.

Note that it is possible to recognize the present position with some error especially in case of using the pulse output equivalent to an encoder, because the time required transmitting all bits in this serial output may generate some dead time in the control system.

Moreover, serial output becomes in absolute output 16 BIT mode regardless of setting resister BIT No.4, 3 in case of operating in "serial absolute output 16BIT mode(special one

Table 5 Serial Output Signal Contents

Serial Output Mode Setting [BIT 4,3]	"DATA" Output BIT NO.															
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**
Absolute-Value Output Mode Setting [00]	LSB φ12	φ11	φ10	φ9	φ8	φ7	φ6	φ5	φ4	φ3	φ2	MSB φ1	PRTY	0	0	PRTY2
Pulse Output Mode Setting [01]	Encoder equivalent Pulse						-	ERR	ERR HLD	ERR CD1	ERR CD2	ERR CD3	PRTY	1	0	PRTY2
	A	B	Z	U	V	W										
Serial Callback Setting [10]	Serial Setting Register Contents												PRTY	0	1	PRTY2
	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7	BIT 8	BIT 9	BIT10	BIT11	BIT12				
Built In Self Test (BIST) Result Setting [11]	Default Setting		BIST CD1	BIST CD2	BIST CD3	BIST CD4	On BIST	VMD	ERR HLD	ERR CD1	ERR CD2	ERR CD3	PRTY	1	1	PRTY2
	BIT 1	BIT 2														
Absolute-value Output 16 BIT Mode [--](Special)	LSB φ16	φ15	φ14	φ13	φ12	φ11	φ10	φ9	φ8	φ7	φ6	φ5	φ4	φ3	φ2	MSB φ1

Operation Waveform of serial output is shown in Figure 5.

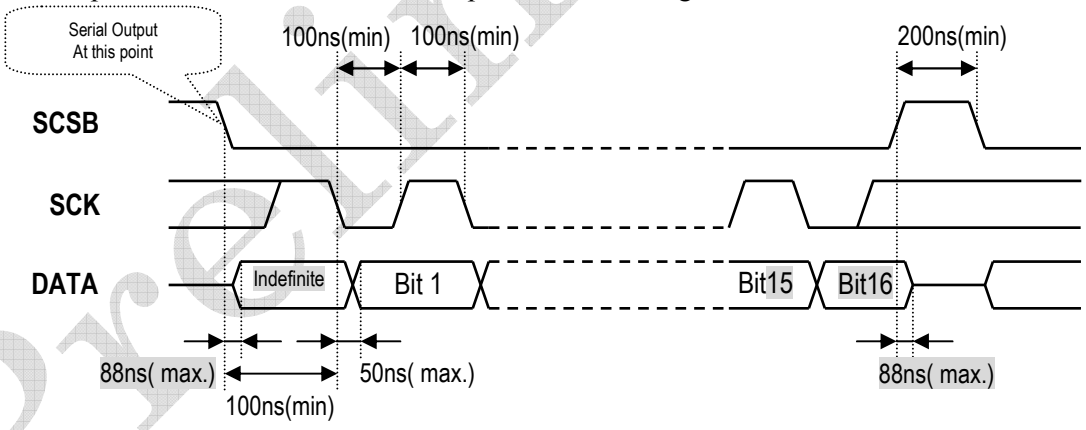

Figure 5. Operation Waveform of serial output

"BIST CD1-4" in Table 5 shows Built-In Self Test(BIST) result(contents) with codes. Please refer to Table 6 in details. You can monitor setting condition of setting register every BIT with serial callback and make sure that serial input setting is correct.

(Note 1) If SCSB is applied continuously ("L level"), it output same data every 16 clock of SCK input repeatedly.

(Note 2) Covered signals in INHB (RD) might be held (fixed) in case of falling SCSB within 58 ns after rising edge of INHB (RD) input.

(Note 3) Do not run serial output sequence within 5 ms after power up or system reset(reboot).

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Table 6 Built In Self Test(BIST Result Contents

BIST CD4	BIST CD3	BIST CD2	BIST CD1	Built In Self Test(BIST) Result Contents	Note
0	0	0	0	(Default Value)	Except On BIST
0	0	0	1	-	
0	0	1	0	-	
0	0	1	1	-	
0	1	0	0	-	
0	1	0	1	Match BIST Ordered Angle1(0°)	Match Range: within ±1.4°
0	1	1	0	Match BIST Ordered Angle2(045°)	Match Range: within ±1.4°
0	1	1	1	Match BIST Ordered Angle3(270°)	Match Range: within ±1.4°
1	0	0	0	-	
1	0	0	1	Resolver Signal Abnormal Detection BIST Normal Operation	
1	0	1	0	Disconnection Detection BIST of Resolver Signal(COS Side) Normal Operation	
1	0	1	1	Disconnection Detection BIST of Resolver Signal(SIN Side) Normal Operation	
1	1	0	0	Conversion Abnormality BIST Normal Operation	
1	1	0	1	-	
1	1	1	0	-	
1	1	1	1	BIST Abnormality or Special Mode Operation	

(10) Exciting Signal Source Select Function

Resolver excitation of external oscillator has the function of R/D conversion with internal exciting output shown in(2) above with R1, R2 input/output select terminal(EXMDB)

⚠1 (Note) Please input external exciting signal to R1 and R2 terminal, in case of set external clock input mode (EXMDB=L) with Serial Input Setting Function.

(11) Using Sensor Select Function

Though originally resolver signal(K•sinθ•sinωt, K•cosθ•sinωt) contains exciting components(sinωt), this IC is able to function effectively to input even DC resolver signal(E•sinθ, E•cosθ) without exciting components if setting using sensor select terminal(DMCDB).

It is able to input DC resolver signal to resolver signal input circuit to set DCMDB terminal to L level.

(Note 1).Exciting component extraction function is disabled it DC resolver signal selection.
(Note 2).EXMDB setting is priority at L level of both EXMDB and DCMDB.

(12) Output Data Error Detection Function

It has the function to output vertical parity as 1 bit even parity(PRTY2) to parallel output data(D0-D11) in(7) above and serial output data(BIT1-BIT12) in(9) above.

It has the function to output vertical parity as 1 bit even parity(PRTY2) to serial output data(BIT1-BIT15).

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3.1.4 R/D Conversion Capability

R/D conversion capability is shown in Table 7.

Table 7 R/D Conversion Capability

No.	Item	Specification		Note
1	Conversion Method	Digital Tracking method(negative feedback control)		
2	Resolution	**4,096(=2^{12})**		Division number per electric angle rotation
3	Conversion Accuracy	**±4** LSB		Absolute error of the electrical angle input in a stationary state, (12bit corresponding value.)
4	Settling Time		**Loop Gain Setting**	
		42 ms(typ.)	Fixed Value(1)(Bandwidth 800Hz)	Electric angle 180°input step Setting range: within ±8LSB
		17 ms(typ.)	Fixed Value(2)(Bandwidth2,000Hz)	
		14 ms(typ.)	Fixed Value(3)(Bandwidth2,500Hz)	
		24 ms(typ.)	Fixed Value(4)(Bandwidth1,500Hz)	
		35 ms(typ.)	Fixed Value(5)(Bandwidth1,000Hz)	
		69 ms(typ.)	Fixed Value(6)(Bandwidth 500Hz)	
		170 ms(typ.)	Fixed Value(7)(Bandwidth 200Hz)	
		1.5 ms(typ.)	Auto-tuning	
5	Maximum Angular Velocity	**240,000** min^{-1}	Loop Gain Fixed Value Setting	Angular velocity range capable of tracking in the electrical angle
		120,000 min^{-1}	Loop Gain Auto-tuning Setting	
		15,000 min^{-1}	Serial Absolute Value Output 16BIT Setting	
6	Maximum Angular Acceleration		**Loop Gain Setting**	Angular acceleration range capable of tracking in the electrical angle
		230,000 rad/s^2(typ.)	Fixed Value(1)(Bandwidth 800Hz)	
		1,110,000 rad/s^2(typ.)	Fixed Value②(Bandwidth2,000Hz)	
		1,370,000 rad/s^2(typ.)	Fixed Value③(Bandwidth2,500Hz)	
		800,000 rad/s^2(typ.)	Fixed Value④(Bandwidth1,500Hz)	
		290,000 rad/s^2(typ.)	Fixed Value⑤(Bandwidth1,000Hz)	
		70,000 rad/s^2(typ.)	Fixed Value⑥(Bandwidth 500Hz)	
		7,000 rad/s^2(typ.)	Fixed Value⑦(Bandwidth 200Hz)	
		3,000,000 rad/s^2(typ.)	Auto-tuning,	
7	Responsibility	**±0.2** °(max.)/10,000 min^{-1}		Electrical angle output in constant angular velocity Response Lag(**3.3μS**equiv.)
8	Stability Time on Start-up	**20** ms(max.)		Output stability time on start-up(within ±8LSB during rest)

(Note) R/D conversion capability specified in Table 7 assumes conditions as follows.

1. Exciting component phase difference of resolver signal input waveform(SINMNT, COSMNT terminal waveform) for resolver exciting signal's basic waveform(discharge waveform between R1-R2 terminals) is as follows in use internal excitation output(EXMDB=H).
   - Current excitation mode (VMD="0"): +90°±45°
   - Voltage excitation mode (VMD="1"): 0°±45°

2. Exciting component phase difference of resolver signal input waveform(SINMNT, COSMNT terminal waveform) for resolver exciting signal's basic waveform(discharge waveform between R1-R2 terminals) is within ±45° in use external oscillator(EXMDB=L).

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3.1.5 Input/Output Signal

Input/Output signal list is shown in Table 8 and pin alignment is shown in Figure 6.

Table 8 Input/Output Signal List(Pin Alignment)

No.	Name	Type	Note	No.	Name	Type	Note
1	EXMDB	D/I	External exciting signal source mode	25	D11	D/O(BUS)	ERRCD3/φ1
2	DCMDB	D/I	DC resolver mode	26	D10	D/O(BUS)	ERRCD2/φ2
3	RLV	D/I	Exciting current selection	27	D9	D/O(BUS)	ERRCD1/φ3
4	VCC	-	Analog power-supply	28	D8	D/O(BUS)	ERRHLD/φ4
5	SINMNT	A/O	SIN monitor	29	D7	D/O(BUS)	ERR/φ5
6	COSMNT	A/O	COS monitor	30	D6	D/O(BUS)	- /φ6
7	AGND	-	Analog GND	31	D5	D/O(BUS)	W phase/φ7
8	S3	A/I	S3 input	32	D4	D/O(BUS)	V phase/φ8
9	S1	A/I	S1 input	33	D3	D/O(BUS)	U phase/φ9
10	S2	A/I	S2 input	34	D2	D/O(BUS)	Z phase/φ10
11	S4	A/I	S4 input	35	D1	D/O(BUS)	B phase/φ11
12	RGND	-	Exciting amplifier GND	36	D0	D/O(BUS)	A phase/φ12
13	R2	A/O(I)	Exciting output R2	37	VDD	-	Digital power-supply
14	VRR	-	Exciting amplifier power-supply	38	INHB(RD)	D/I	inhibit
15	R1	A/O(I)	Exciting output R1	39	ERRHLD	D/O(I)	Error(keeping)
16	BISTVLD	D/I	BIST execute control	40	ERRSTB	D/I	Error reset
17	CLKIN	D/I	Clock input	41	ERR	D/O(I)	Error output
18	SSDT	D/I	Serial setting data	42	A	D/O	A phase pulse output
19	SSCS	D/I	Serial setting CS	43	B	D/O	B phase pulse output
20	DATA	D/O(BUS)	Serial data	44	B	D/O(I)	Z
21	SCSB	D/I	Serial CSB	45	CSB	D/I	Chip select
22	PRTY	D/O(BUS)	parity	46	PUPD	D/I	Parallel absolute value update switch
23	SCK	D/I	Serial clock	47	TEST1	D/I	(Test mode setting)
24	DGND	-	Digital GND	48	TEST2	D/I	(Test mode setting)

(Note 1) ”No.” is equal to terminal(pin) no.
(Note 2) Signal types are below.

- ✧ A/I: Analog Input
- ✧ A/O: Analog Output
- ✧ A/O(I): Analog Output(Input/Output switch in control terminal input)
- ✧ D/ I : Digital Input
- ✧ D/O: Digital Output
- ✧ D/O(I): Digital Output(internal input addition)
- ✧ D/O(BUS):Digital Output(3-STATE output)

(Note 3) No.47 TEST1 signal and No.48 TEST2signal have no direct involvement in operation and shunt TEST1to digital power supply(VDD), TEST2 to digital GND(DGND) under normal conditions. Each terminal is pulled-up or pulled-down inside without any connection.

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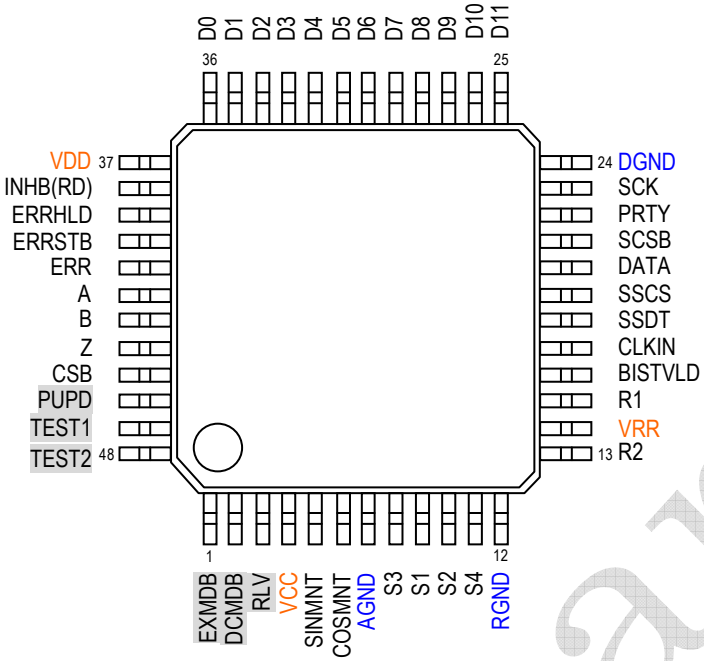


Figure 6.Pin Alignment

Input signal polarity is shown in Table 9.

Table 9.Input Signal Polarity

Pin No.	Signal Name	Signal Function	Signal Polarity		Note
19	SSCS	Chip Select Signal For Serial Input Setting	High	SSDT Input Reception Invalid	
			Low	SSDT Input Reception Valid	
21	SCSB	Serial Data(DATA) Output Status Control Input	High	High-Z	
			Low	Output Effective	
45	CSB	D0-D11 and PRTY Output Status Control Input	High	High-Z	
			Low	Output Effective	
38	INHB(RD)	Hold(fixed) Input of Intended Signal Output(Refer to Note)	High	Signal Through	
			Low	Hold(fixed)	
40	ERRSTB	Reset Input of ERRHLD Output and Error Code ERR CD1-3	High	Hold	
			Low	Clear Hold status	
16	BISTVLD	Built-in Self Test(BIST) Function, Special mode Operation Able/Disable Control Input	High	Non-executable	Normal Operation
			Low	Executable	
1	EXMDB	Input/Output Changeover of R1,R2	High	Exciting Current Output	
			Low	Exciting Signal External Input	
2	DCMDB	Sensor Used Selection	High	Resolver Used	
			Low	DC Resolver	Hall IC etc.
3	RLV	Exciting Current Selection	High	Exciting Current 10mArms.(typ)	
			Low	Exciting Current 20mArms.(typ)	
46	PUPD	Parallel Absolute Value Output Update Time Changeover	High	Update Frequency 25MHz(typ.)	
			Low	Update Frequency 12.5MHz(typ.)	

(Note) INHB(RD) signal function is valid in output signal below.

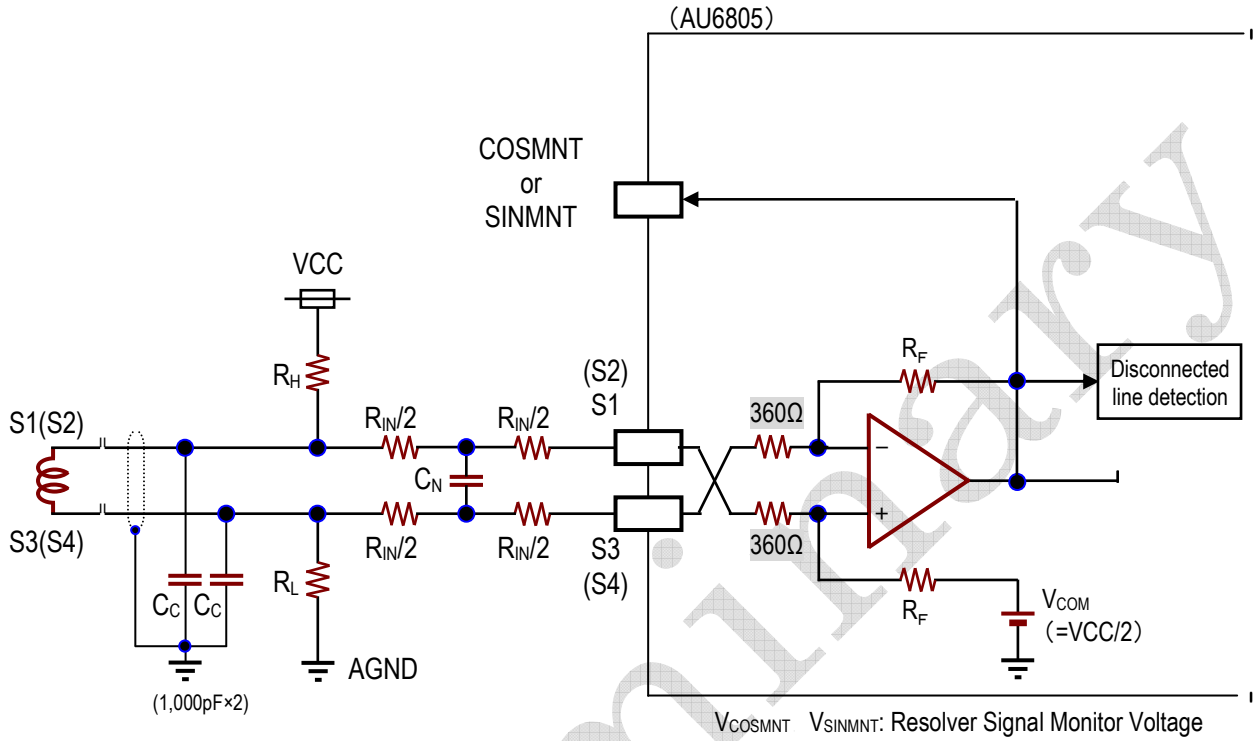
- Parallel Output(D0-D11) and PRTY
  - Absolute Value Output Mode: φ1-φ12, PRTY
  - Pulse Output Mode: U, V, W, ERR, ERRHLD, ERRCD1-3
- Serial Output
  - Absolute Value Output Mode: φ1-φ12, PRTY
  - Pulse Output Mode: U, V, W, ERR, ERRHLD, ERRCD1-3
  - Built-In Self Test(BIST) Result: ERRHLD, ERRCD1-3
  - Absolute value output 16BIT Mode(Special Mode): φ1-φ16

Edition No.

Preliminary

3.1.6 Input/Output Circuit(Exclude Protection Circuit)

(1) Resolver Signal Input(Differential) Circuit <S1-S3, S2-S4> and Monitor Output
Equivalent circuit of Resolver signal input(differential) circuit <S1-S3, S2-S4> and monitor output is shown in Figure 7.



VCOSMNT VSINMNT: Resolver Signal Monitor Voltage
VCOM Reference voltage Internal IC (=VCC/2)
Rf 21kΩ±20% (Relative accuracy : ±1%)

(Note 1) Tolerance range [%] of input resistance (R_{IN}) has impact to conversion accuracy[LSB].0.3% is equivalent to 1LSB.

(Note 2) Except the tolerance of input resistances and the performance of Resolver itself, the variation of monitor output voltages (V_{SINMNT} & V_{COSMNT}) is within ±20 % when Resolver is directly excited by the exciting output (R1 & R2) of this IC.

Figure 7. Resolver Signal Input (Differential) Circuit

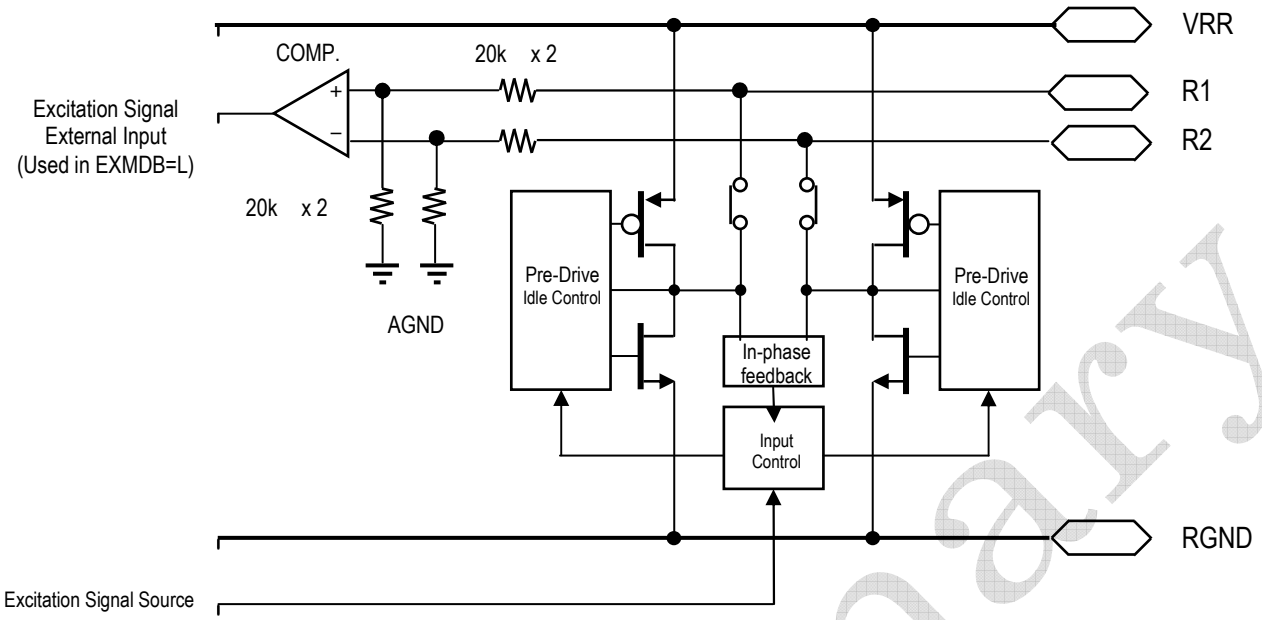
<Constant Setting Method>

- **R_{IN}**: Resolver signal level
  V_{COSMNT} or **V_{SINMNT} =(V_{IN}) ×(R_F/(R_{IN}+360Ω))≈2-3** [Vp-p](recommended value)
  (However, V_{IN} means signal output voltage [Vp-p] between resolver terminals, **R_{IN}≥2**[kΩ])
- **R_H** and **R_L**: Determine resistance value within 80-100% of calculated value below.
  1. **R_H≈{(VCC-V_{COM})/(12.5×10^{-6})}-R_{IN}** (V_{COM}=VCC/2[V])
  2. **R_L≈{V_{COM}/(12.5×10^{-6})}- R_{IN}** (V_{COM}=VCC/2[V])

Preliminary

(2) Resolver Exciting Input/Output Circuit<R1, R2>

Resolver exciting input/output circuit is shown in Figure 8.



(Note) As the measures for eliminating noise from the exciting output terminals (R1 & R2), it is effective to insert a serial resistor to the extent of allowable resistance and a subsequent Schottky diode with low impedance to the exciting output circuit especially in order to clamp any negative surge voltage.

Figure 8.Resolver Exciting Input/Output Equivalent Circuit

Preliminary

(3) Digital Input Circuit

Digital Input Equivalent Circuit is shown in Figure 9 and 10.

Covered signal: SSDT, SSCS, SCSB, SCK, CSB, INHB(RD), ERRSTB, CLKIN, BISTVLD, EXMDB, DCMDB, RLV, PUPD, TEST1

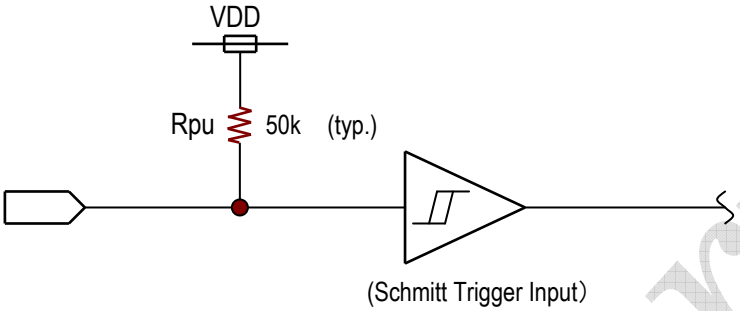


Figure 9. Digital Input Equivalent Circuit(Internal Pull-up Terminal)

< Intended signal: TEST2>

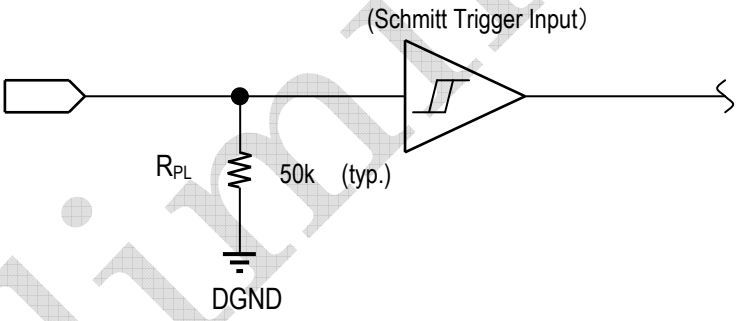


Figure 10. Digital Input Equivalent Circuit(Internal Pull-down Terminal)

(4) Digital Output Equivalent Circuit<A, B>

Digital output equivalent circuit is shown in Figure 11.

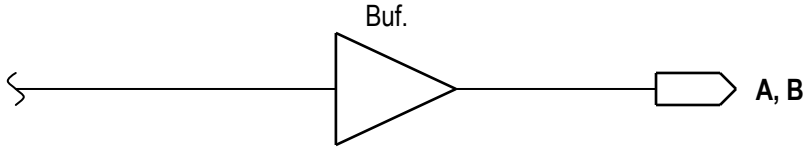


Figure 11.Digital Output Equivalent Circuit

Preliminary

(5) Digital Input/Output Circuit Construction<ERRHLD, ERR, Z>
Digital input/output circuit construction is shown in Figure 12.

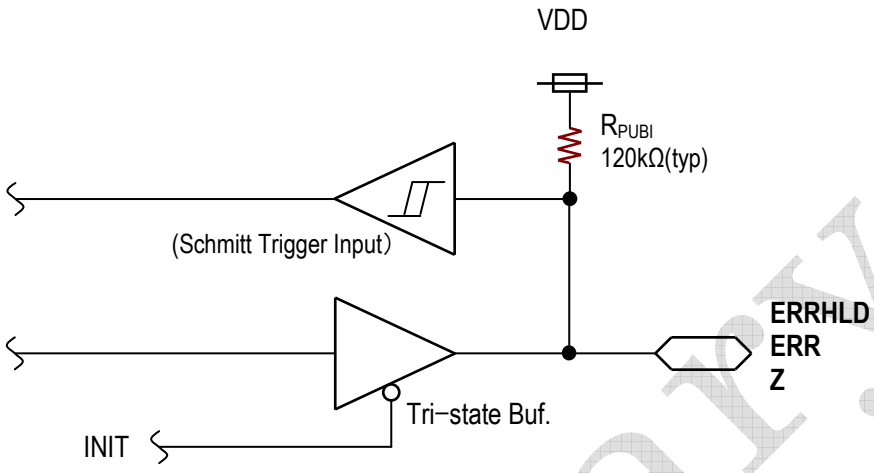


Figure 12.Digital Input/Output Equivalent Circuit

(6) Bus Interface Circuit
Bus interface equivalent circuit is shown in Figure 13.
<Intended signal: D0-D11, PRTY>

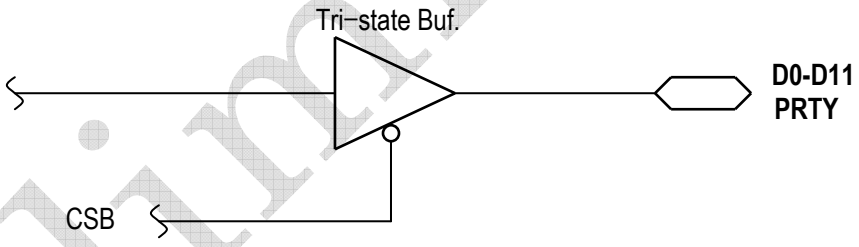


Figure 13.Bus Interface Equivalent Circuit

(7) Serial DATA Signal Output Circuit
Serial DATA signal output equivalent circuit is shown in Figure 14.

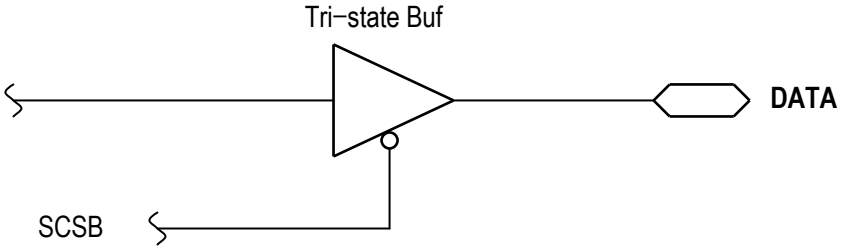


Figure 14.Serial DATA Signal Output Equivalent Circuit

Preliminary

3.1.7 Electrical Properties

(1) Resolver Exciting Output(**R1, R2**)

- Output Waveform: Sine wave current output
- Frequency: 10kHz±**30**%(in internal clock operation),
  (clock frequency)/1000[Hz](in external clock operation)
- Output Current: **10**mArms.±**30**%(in RLV=H),
  20mArms.±**30**%(in RLV=L)
- Load Impedance: **200**Ω(max.)(in RLV=H)
  100Ω(max.)(in RLV=L)

(2) Resolver signal monitor output(**SINMNT**, **COSMNT**)

- Frequency: as same as resolver signal input frequency
- Maximum Output Voltage Range: **3.8**Vp-p(min.) (center runout: COM potential)
- Load Impedance: **20**kΩ(min.)

(3) Internal Clock

- Internal Digital Part CLK: **50**MHz±**30**%

(4) Threshold Internal Setting Value for Angle Conversion BIST Judgment

Judgment threshold internal setting value for Angle conversion BIST is shown in Table 10.

Table 10 Judgment Threshold Internal Setting Value for Angle Conversion BIST

Angle Conversion BIST Contents	Setting threshold	Constant In Detection
Angle Conversion BIST Ordered Angle 1(0°)	**±1.4°** (8 bit accuracy)	**10** ms(max.)
Angle Conversion BIST Ordered Angle 2(45°)		
Angle Conversion BIST Ordered Angle 3(270°)		

Preliminary

(5) Internal Setting Value of Failure Detection Judgment Threshold Value
Internal setting value of failure detection judgment threshold value is shown in Table 11.

Table 11 Internal Setting Value of Failure Detection Judgment Threshold Value

Failure Detection Contents		Setting Threshold Value	Detection Time [ms]
Resolver Signal Abnormality (Monitor Output Amplitude Voltage (Note)1)	Setting Resister [BIT12]=[0]	0.1 VCC±5%[Vp-p]	**0.5**(max.)
	Setting Resister [BIT12]=[1]	0.14 VCC±5%[Vp-p]	
	Relative deviation between range	0.04 VCC±5%[Vp-p]	
Resolver Signal Disconnection (DC-Bias Method) (DC level variation of monitor output voltage V_{SINMNT} - V_{COM} or V_{COSMNT} - V_{COM} Refer to 3.1.6(1) Input/Output Circuit Figure (Note 2))	Except setting as follows	0.08 VCC±5%[V_{DC}]	**10**(max.)
	DCMDB=L And EXMDB=H	0.35 VCC±5% V_{DC}	
R/D Conversion Abnormality (Excessive Control Deviation) (Internal Control Deviation(ε) Recognition Level As Too much(Note3))	High side	0.55 VCC±5%[V_{DC}]	(Note)4
	Low side	0.45 VCC±5%[V_{DC}]	

(Note 1) If both SINMNT and COSMNT become less than threshold, it is judged as abnormal.
(Note 2) If DC Level variation become more than threshold, it is judged as abnormal.
(Note 3) If error deviation is more than threshold in the High side or less than one in the Low side, it is recognized as excessive.
(Note 4) if control variation recognition rate as too much is more than 50% as around 5.9 ms, it is judged as abnormal.(It is equivalent that around 15°(typ.) is R/D output angle gap for resolver signal angle about threshold.)
(Note 5) When abnormality duration is shorter than detection time, it is incapable to detect.

Preliminary

(6) Absolute Maximum Rating

Absolute Maximum rating is shown in Table 12.

Table 12 Absolute Maximum Rating

Item	Symbol	Terminal	Absolute Maximum Rating	Unit
Power-supply Voltage	VDD	VDD	**-0.3 - +6.5**	V
	VCC	VCC	**-0.3 - +6.5**	V
	VRR	VRR	**-0.3 - +6.5**	V
Voltage Difference Between Voltage Source(Note 1)	VCC–VRR	VCC, VRR	**-0.3 - +0.3**	V
Voltage Difference Between GND	AGND-RGND	AGND, RGND	**-0.1 - +0.1**	V
	RGND-DGND	RGND, DGND	**-0.1 - +0.1**	V
	DGND-AGND	DGND, AGND	**-0.1 - +0.1**	V
Input Voltage Range	VIN_d	Digital Input/Output Terminal (PIN 1-3, 16-48)	**-0.3 - VDD+0.3**	V
	VIN_a1	Analog Input/Output Terminal1(PIN 5 - 11)	**-0.3 - VCC+0.3**	V
	VIN_a2	Analog Input/Output Terminal2(PIN 13 15)	**-0.3 - VRR+0.3**	V

(Note 1.Including power on time, power off time)

(7) Digital Signal Input/Output

■ Recommended Operating Range

Recommended operating range of digital signal is shown in Table 13.

Table 13 Digital Signal Recommended Operating Range(VDD=5V±10%, Ta=-40°-+125°)

Item	Symbol	Min.	Typ.	Max.	Unit
High Level Input Voltage	V_{IH}	**0.8VDD**		**VDD**	V
Low Level Input Voltage	V_{IL}	**0**		**0.2VDD**	V
Input Rise Time	TRI	**0**		**1.0**	ms
Input Fall Time	T I	**0**		**1.0**	ms
External CLK Input Frequency	F_{CLK}	**7**	**10**	**13**	MHz
External CLK Duty	D_{CLK}	**40**		**60**	%
Serial Clock (SCK) Input Frequency	F_{SCK}			**5**	MHz

Preliminary

■ DC Property

Digital signal DC property is shown in Table 14.

Table 14 DC Property (VDD=5V±10%, Ta=-40°-+125°)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
hysteresis Voltage	V_H		**0.36**			V
Input Pull-up Impedance	R_{PU}		**30**	**50**	**85**	kΩ
Input Pull-down Impedance	R_{PL}		**30**	**50**	**85**	kΩ
Pull-up Impedance	R_{PUBI}		**72**	**120**	**200**	kΩ
Input Leak Current	I_L	V_I=D ND			**-200**	μA
High Level Output Voltage	V_{OH}	I_{OH}=0mA	**VDD-0.1**			V
Low Level Output Voltage	V_{OL}	I_{OL}=0mA			**0.1**	V
High Level Output Current	I_{OH}	V_{OH}=VDD-0.5V	**-4**			mA
Low Level Output Current	I_{OL}	V_{OL}=0.5V	**4**			mA

(Note) Input Leak Current has "-" direction.

■ AC Property

Digital signal of AC property is shown in Table 15.

Table 15 AC Property(VDD=5V±10%, Ta=-40°-+125°)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Rise Time	TR	C_L=15pF			**6**	ns
Output Fall Time	T	C_L=15pF			**6**	ns

(Note) Output rise time/Output fall time means time required for 0.2VDD-0.8VDD zone.

Preliminary

■ Timing Chart

a) Bus Control Timing

Bus control timing in "PUPD=1" is shown in Figure 15.

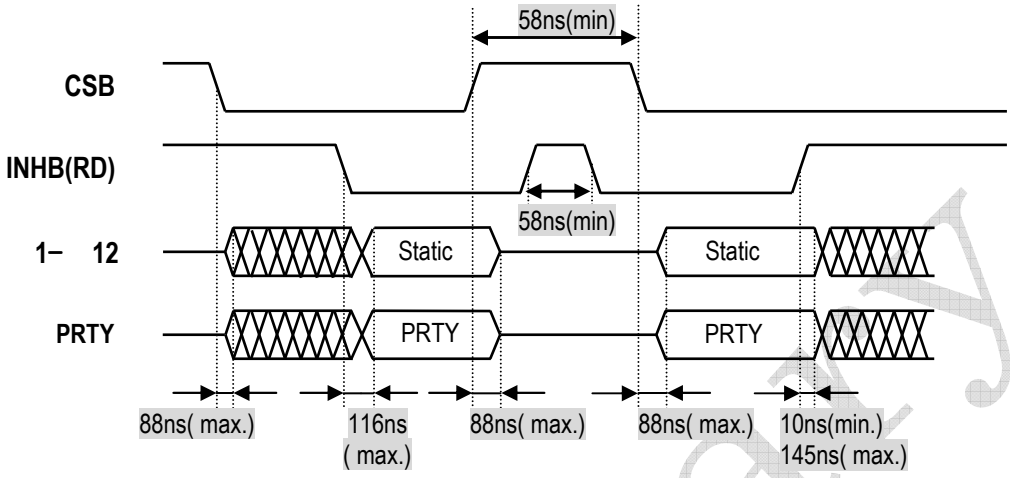


Figure 15. Parallel and Parity Output Operating Waveform In "PUPD=1"

Bus control timing in "PUPD=0" is shown in Figure 16.

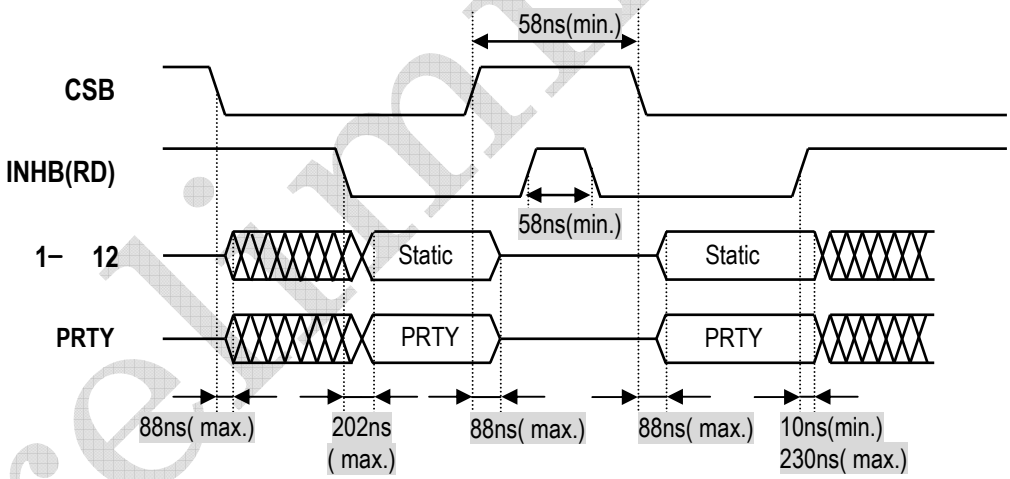


Figure 16. Parallel and Parity Output Operating Waveform In "PUPD=0"

Preliminary

b) Error Reset Timing

Error reset timing is shown in Figure 17.

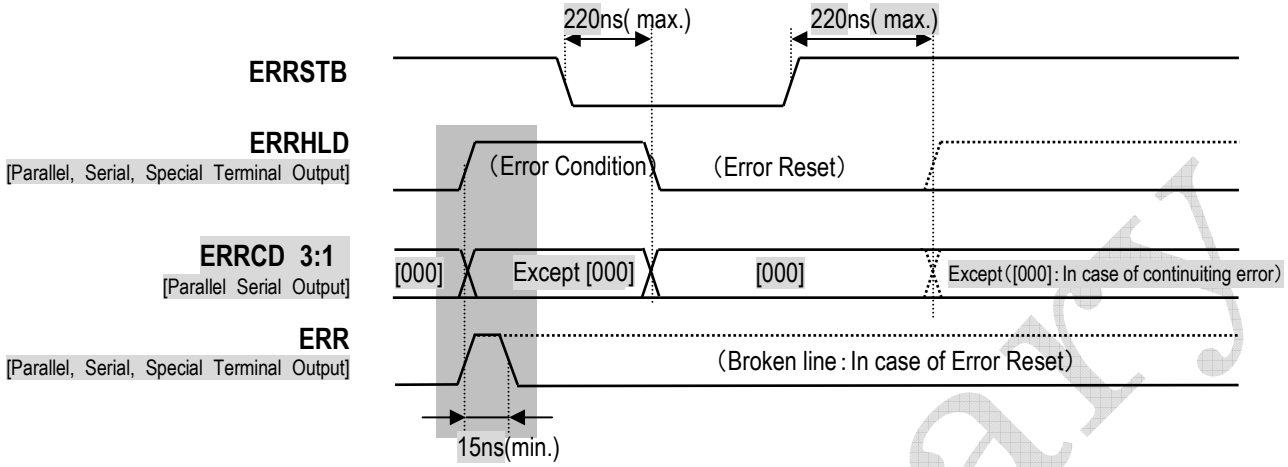
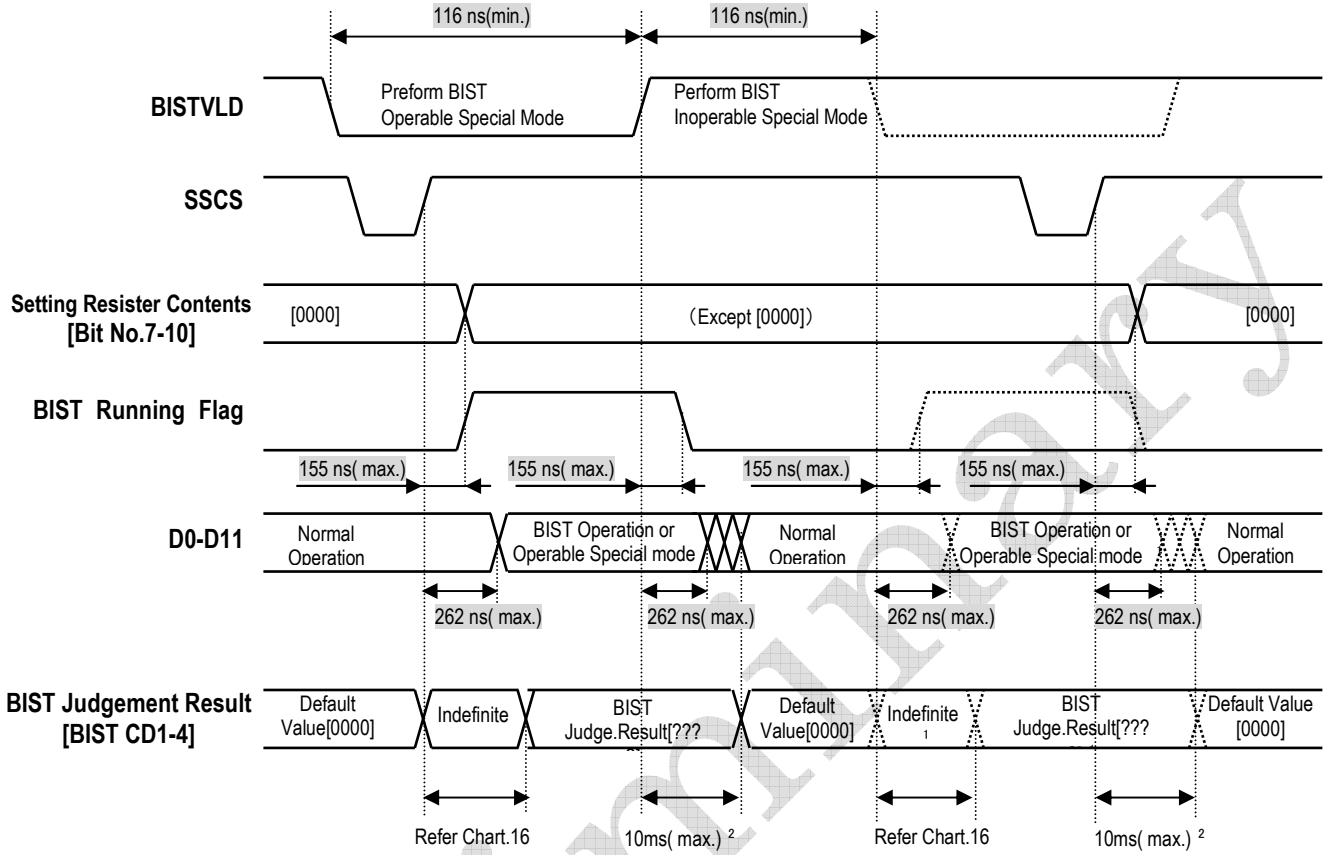


Figure 17. Error Output Operating Waveform

(Note 1) Please use ERRHLD output after the error is reset by ERRSTB input certainly. If ERRHLD output error cannot be reset, eliminate true error factor.
(Note 2) Parallel and serial signal output is covered in INHB(RD).
(Note 3) Sequence specified in Figure 5 is necessary to load signal related serial output error.

Preliminary

(8) Built-In Self Test(BIST), Special Mode Operating Sequence
Built-in Self Test(BIST) and special mode operating sequence is shown in Figure 18.



*1: Broken line means BISTVLD=L except setting resister [Bit No.7-10]=[0000]
*2: less 120,000min^{-1} (electric angle)

(Note) Don't run serial input/output sequence in 116ns before/after BISTVLD polar change.

Figure 18. Built-In Self Test (BIST), Special Mode Operating Sequence

Built-In Self Test(BIST) and special mode can run only during "BISTVLD" input is capable to run as "Low" and Built-In Self Test(BIST) and special mode in setting register. In addition, system reset can issue when SSCS=H.

Preliminary

Built-In Self Test(BIST) judgment result is output as BIST code(BIST CD1-BIST CD4) in serial output during the time. BIST Judgment Time is shown in Table 16.

Table 16 BIST Judgment Time

Judgment Item	Judgment Time	Note
Angle Conversion BIST	10ms max	Time Until BIST Judgment Result is Settling
Resolver Signal Abnormal Detection BIST	0.5ms max..	
Disconnection Detection BIST of Resolver Signal	1ms max..	
Conversion Abnormality BIST	10ms max..	

(9) Power ON/OFF Sequence

Power On operating sequence is shown in Figure 19.

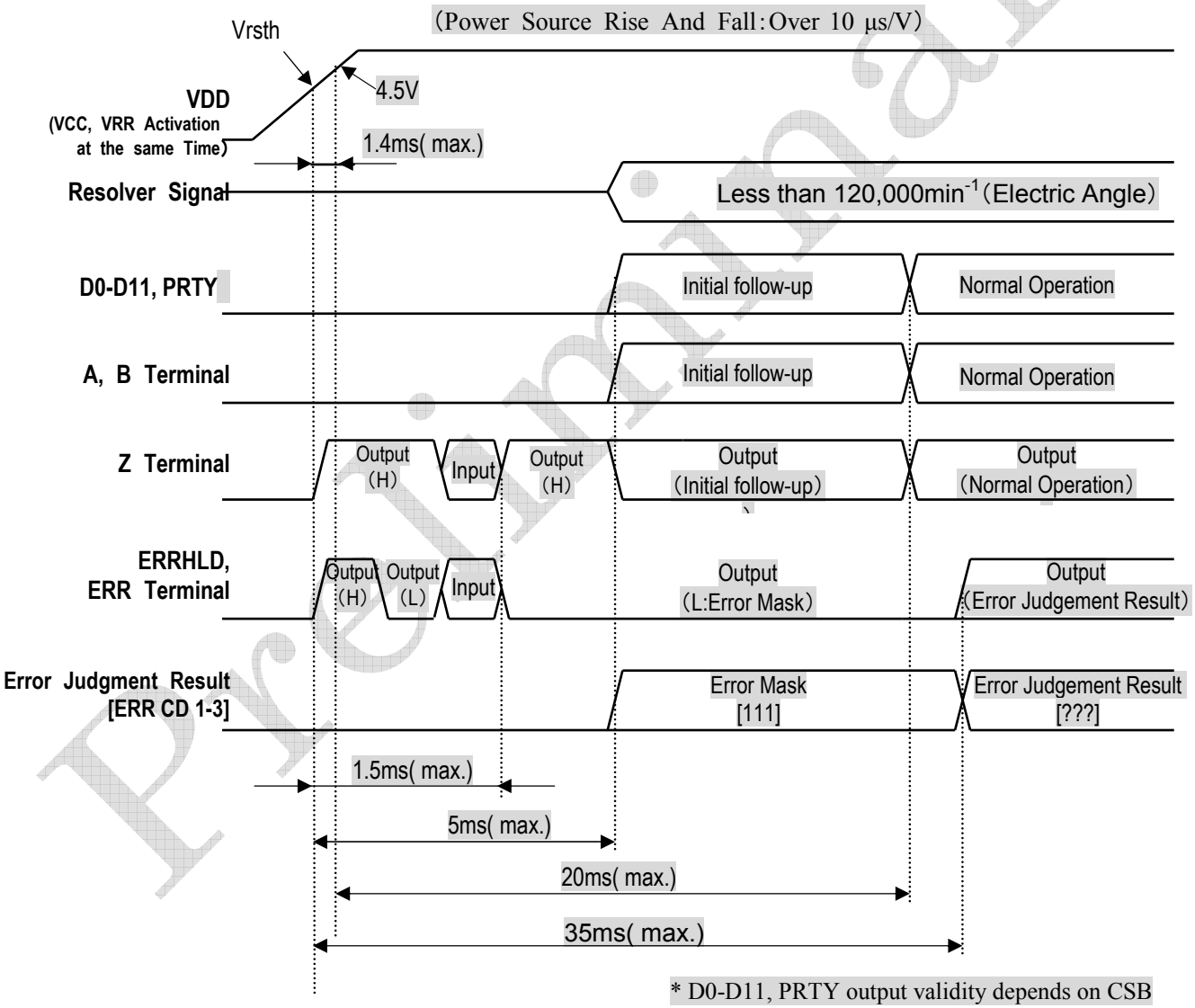


Figure 19.Power ON Operating Sequence

Preliminary

Power Off operating sequence is shown in Figure 20.

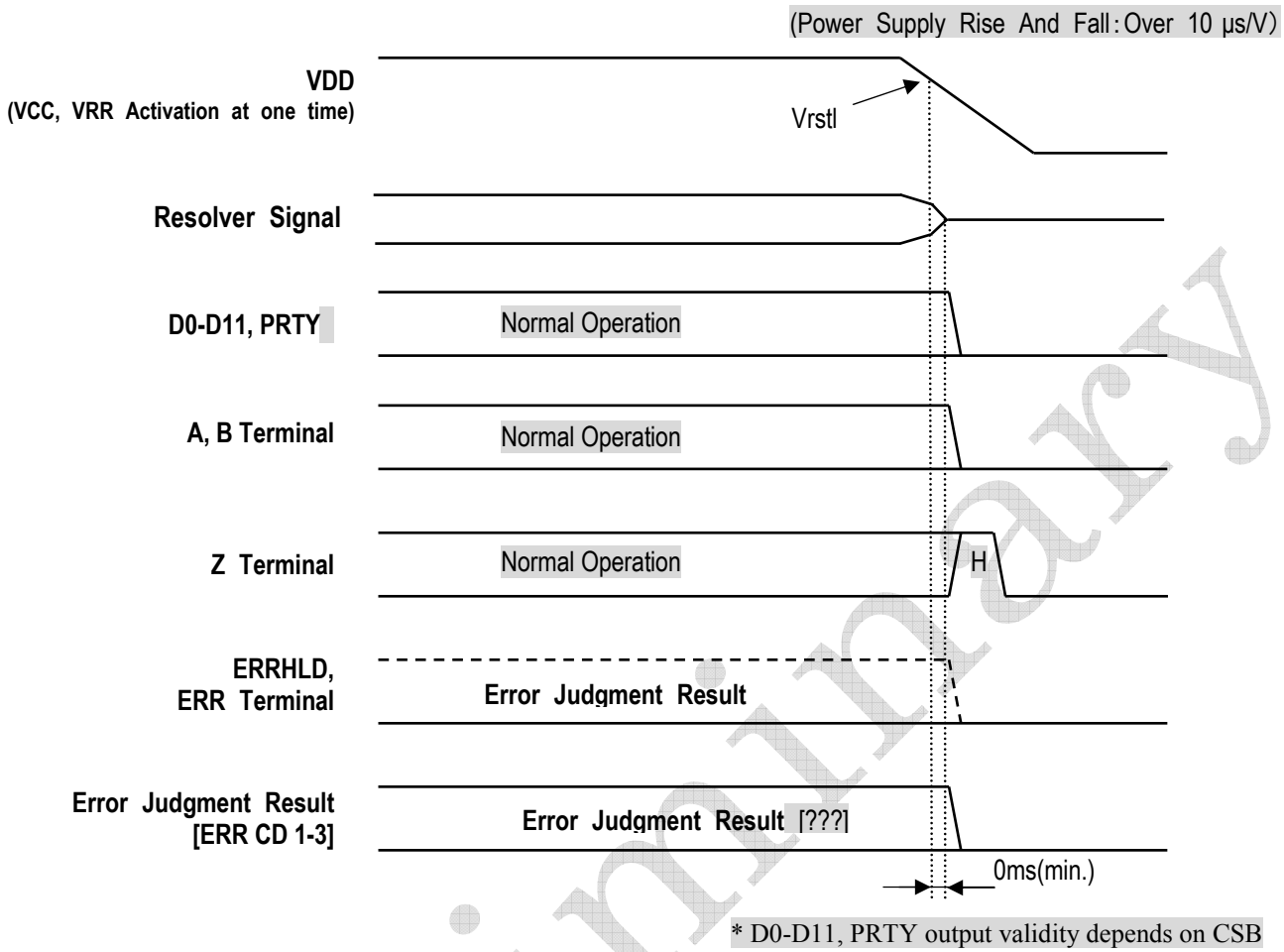


Figure 20.Power OFF Operating Sequence

(Note) Three types of power supply, "VCC" for analog, "VDD" for digital, and "VRR" for excitation should be turned on or off simultaneously, when the power supply is switched on or off.

When the power supply is turned on and the voltage value of VCC exceeds the reset releasing voltage, Vrsth shown in Table 17, the reset is released and its operation starts, and then the error code becomes [111] (Error mask when starting). When the power supply is turned off, if the voltage value of VCC reduces below the reset voltage Vrstl shown in Table 17, it becomes reset and the operation stops or goes to the end.

Table 17 Reset Voltage Specification

Code	Specification Value [V]			Note
	Min.	Typ.	Max.	
Vrsth	**3.4**		**4.4**	Reset Release Voltage
Vrstl	**3.2**		**4.2**	Reset Voltage
Vrhys		**0.2**		Hysteresis Width

Preliminary

Also internal reset signal timing is shown in Figure 21 and Table 18.

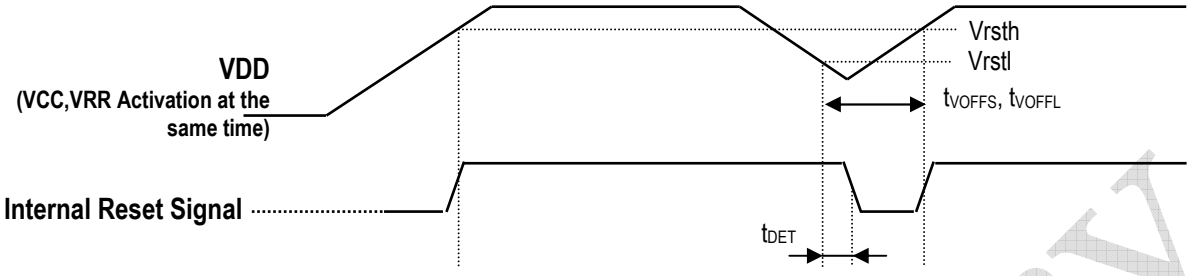


Figure 21. Internal Reset Signal Operating Waveform

Table 18 Internal Reset Signal Timing Specification

Code	Specification Value[ms]			Note
	Min.	Typ.	Max.	
T_{DET}	**0.5**		**3.0**	Relay Delay Time
T_{VOFFS}			**0.5**	Reset Disable VDD Decreasing Time((Note 1)
T_{VOFFL}	**3.0**			Rest Enable VDD Decreasing Time(Note 2)

(Note 1) Maximum VDD Decreasing Time with reset
(Note 2) Minimum VDD Decreasing Time with reset

3.1.8 Required Electric Power Supply

(1) Power-supply Voltage: DC+**5**V±**10**%(VCC, VDD, VRR)
(2) Consumption Current: Refer to Table 19. Each value means the internal current consumption, when the exciting current is contained, and there is no load in the digital output.

Table 19 Maximum Consumption Current

RLV="H"	RLV="L"
45mA	**65**mA

Preliminary

3.2 Physical Feature

(1) Outside Dimension: **7*7*1.5t** [mm] LQFP(Refer to Attended Figure 2.Package Outline Figure.)
(2) Pin Alignment: **0.5** mm pitch, 48 pin
(3) Weight: **0.2**g(Typ.)

3.3 Environment Resistance

(1) Operation Temperature(Ambient Temperature): **-40°** to **+125°**
Do not exceed maximum power.
(2) Storage Temperature: **-65°**to **+150°**(before implementation) 1
(Note) Normal strage must be followed by moisture-proof packaging specifications.
(3) Degree of humidity: **90**%RH max..(without be dewing)
(Note 1) Environmental performance on the basis of normal use condition(2 6)
(Note 2) Follow the storage conditions of moisture-proof packaging specification prior to implementation.
(4) Maximum Power Dissipation (P) 3 0 W
(5) Package Thermal Resistance ( ) 63.6 W 4- er o r 6.2 114.3 t1.6

Preliminary

4 Quality Assurance

4.1 Warranty of Products

The warranty period for R/D Converter IC (AU6805) is one year after shipping, with the exception of conditions caused by disassembling, changing, reassembling, misusing, or other intention or fault by the customer. Failed products, due to workmanship, within this one year term will be replaced at no charge.

AU6805 is a semi-conductor integrated circuit (i.e. electronic device) with a high grade quality level suitable for use in automobiles, trains, etc. and is designed for units involving direct control and safety of transportation equipment.

The predicted mean time between failures (MTBF) is considerably long, but the failure rate is not zero. Therefore, the customer is to assume this responsibility, considering the possibility of failure, and to design multilple back-up measures within the equipment or system to avoid a serious system failure.

If you have any questions or concerns, we respond in good faith even though out of warranty.

Preliminary

4.2 Reliability Test

Reliability Test (AEC-Q100 equivalent) referred to Table 20 Reliability Test Contents is applied to establish product quality.

Table 21 Reliability Test Contents

Test Item	Test Conditions	No. of lot	Sample size / lot	Test Time	Note
Preconditioning (PC)	Over JEDEC LEVEL3 (J-STD-020C) (JESD22-A113)	-	-	------	Applied before THB, TC, AC
High Temperature Storage Life (HTSL)	+150°	1	45	2,000 Hr	
High Temperature Operating Life (HTOL)	+125°(5.5V)	3	77	1,000 Hr (2000Hr only in 1lot)	
Temperature-Humidity-Bias (THB)	+85°/ 85%RH (5.5V)	3	77	1,000 Hr (2000Hr only in 1lot)	
Autoclave (AC)	+121° / 15psig ⚠1	3	77	96 Hr (500Hr only in 1lot)	
Temperature Cycling (TC)	-65° / +150° Hold 20 minutes	3	77	500 Cyc (1,000Cyc only in 1lot)	
Latch-Up(LU)	AEC-Q100-004	1	6	-------	
Solderability(SD)	After burn-in J ESD22-B102	1	15	-------	
Wire Bond Pull (WBP)	MIL-STD883 Method 2011	1	5 (30 bond)	-------	
	Minimumu pull strength after TC = 3grams.	1	5 (12 bond)	-------	
Wire Bond Share (WBS)	AEC-Q100-001	1	5 (30 bond)	-------	
Physical dimensions (PD)	JESD22-B100 or B108	3	10	-------	
Electrical Distributions (ED)	AEC-Q100-009	3(each condition)	30(each condition)	-------	
Early Life Failure Rate (ELFR)	+125°(5.5V)	3	800	-------	
Lead Integrity	Tensile 1N 30S 1 time bend±15°1time (JESD 22-B105)	1	22	-------	

Table 21. Electrostatic Discharge Test

Test Item	Test Conditions	No. of lot	Sample size / lot	Note
Human Body Model (HBM)	Start Applied Voltage:±50V Step Voltage:±50V-±200V (AEC-Q100-002)	1	6/ Each voltage level	
Machine Model (MM)	Start Applied Voltage:±0.5KV Step Voltage:±0.5KV-±2KV (AEC-Q100-003)	1	6/ Each voltage level	
Charged Device Model (CDM)	Start Applied Voltage:±0.25KV Step Voltage:0.25KV-±0.75KV (AEC-Q100-011)	1	3/ Each voltage level	

Preliminary

5 Application Note

5.1 Input/Output Interface Circuit

The practical examples of circuit for application are shown in the separate application notes as references. These practical examples show only an idea to materializing the basic functions (i.e. interfaces), and the determination of constants such as the value of resistors, etc. and addition of functions such as the protection of input/output circuits, etc. should be considered depending on the individual application.

5.2 System Setting(IC Operating Environment Equipment)

(1) Considerations in power-supply line design method

Please set bypass capacitors(0.1μF) individually between every power-supply terminal(VRR-RGND, VCC-AGND, VDD-DGND) as close as possible to this IC, when power-supply line is designed.

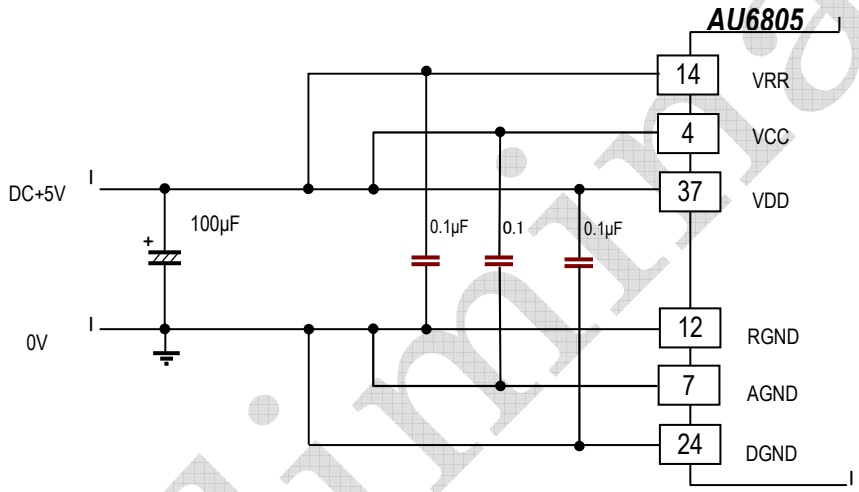


Figure 22. Power-supply Line Design Method

Preliminary

5.3 Measure against Noise

Especially in case of using resolver as motor's sensor, some noises are produced depending on drive control system. It is necessary to assure resolver signal itself(without superimposed noises) and consider how to maintain R/D conversion normally. Though this R/D conversion IC has good interactivity with consideration for noise immunity, it cannot keep up with all noise environments and is needed to consider appropriate surround for usage environment.

Specific measures against noise from **Measure I** to **Measure VIII** are shown for reference.

(1) Measure against Magnetical Disturbance Noise

In case that motor leakage flux passes through resolver, resolver signal looks like angle change and IC has a malfunctions as a result.

Measure I Minimize magnetic loop to resolver penetration assemble of motor flux leakage with structurally/materially engineered (with magnetic shielding effect) in assembling resolver to motor.

Measure II Raise resolver exciting voltage (power current) in order to improve S/N ratio for true signals unless resolver penetration of motor flux leakage completely.

(2) Measure against electrical disturbance Noise

Electrical disturbance(spike, noise, etc.) from motor's PWM drive is very strong and has an impact on electrical system like resolver excitation/signal line and electrical line etc. through various channels.

Measure III Filter out spike noise component with common mode/normal mode filter inserted. Less noise is produced in exciting line of low impedance generally and measure isn't necessary.

Measure IV Filter out spike noise component with common mode/normal mode filter inserted in resolver signal line(S1-S3, S2-S4).In that case, constant selection which is valid for only noise is necessary and has no impact on original resolver signal waveform such as distortion. Also, electric noise waveform of each S1-S4 terminals viewed from AGND is considered to be in phase. Moreover, if error occurs because of electric disturbance noise even after this measure, it is valid to keep resolver signal level lower.

Measure V Power-supply(VCC, VDD, VRR) line inserts bypass capacitors, etc. by condition.

(3) Other Common Measures

Measure VI Use shielded twisted pair for resolver wiring and connect shielded terminal in a lump on circuit side(earth to AGND).And separate wires from motor cables.

Measure VII Power up GND system with low impedance and result in noise reduction and shielding effectiveness with common impedance. Also, it is another measure that potential of motor driver radiator and motor case set to the one of control GND system.

Measure VIII Put motor driver and sensor circuit away physically and cover each with shielding case, etc.

Preliminary

5.4 Fail-safe System Architecture

Especially applied to safe system, fail-safe support is needed in emergency situations and it necessary to review systematically.

The basic concept of R/D conversion IC is premised that IC is used alone not plural and fails(in operation and malfunction, etc.) of angle detection system including sensor(resolver) is recognized surely. Functions of R/D conversion IC for fail-safe system architecture in angle detection system with resolver are as follows.

Moreover, the basic model of fail-safe system architecture refers to Figure.23.It necessary to architect each optimal system in condition with redundant component and concept and functions as follows for specific applications.

I. Redundancy for Fail Cognition in Sensors(Resolver)

- Fail Judgment: Operate BIST(Angle Conversion BIST) by design and check normal operation of IC itself.
- Fail Monitor: Monitor failure detection result embedded in IC as follows;
  A) Resolver signal abnormality
  B) Resolver signal disconnection(DC bias application method)
- Redundant Signal Output: Install resolver signal monitor output(SINMNT/COSMNT) output from IC to A/D input on CPU and monitor resolver signal abnormality in sums of squares method and so on using software. Or, monitor resolver signal abnormality in phase shifter method with attached component(resistor, capacitor).The method to compare R/D output and result directly calculated by CPU from resolver signal is not valid for resolver itself abnormality monitoring.

II. Redundancy for Fail Cognition in R/D Conversion

- Fail Judgment: Operate BIST(Angle Conversion BIST) by design and check normal operation of IC itself.
- Fail Monitor: Monitor failure detection result embedded in IC as follows;
  A) R/D Conversion Abnormality
  B) Internal IC Anomalous Warmth
- Redundant Signal Output: Install resolver signal monitor output(SINMNT/COSMNT) output from IC to A/D input on CPU and calculate angle using software.

. Redundancy for Fail Cognition in Output

- Redundant Signal Output: Digital angle output I/F is triple redundancy (parallel, pulse and serial).Parallel and serial output is with parity bit.

. Redundancy for Fail Cognition in Angle Detect Whole System

- Output behavior Monitor: Monitor IC's digital angle output IC with CPU and check unexpected behaviors(example: sharp angle change, etc.) on operation.
- Comparison with alternate method: Compare angle information(example: sensorless control, etc.) of unique alternate method by host system and monitor angle abnormality.

Preliminary

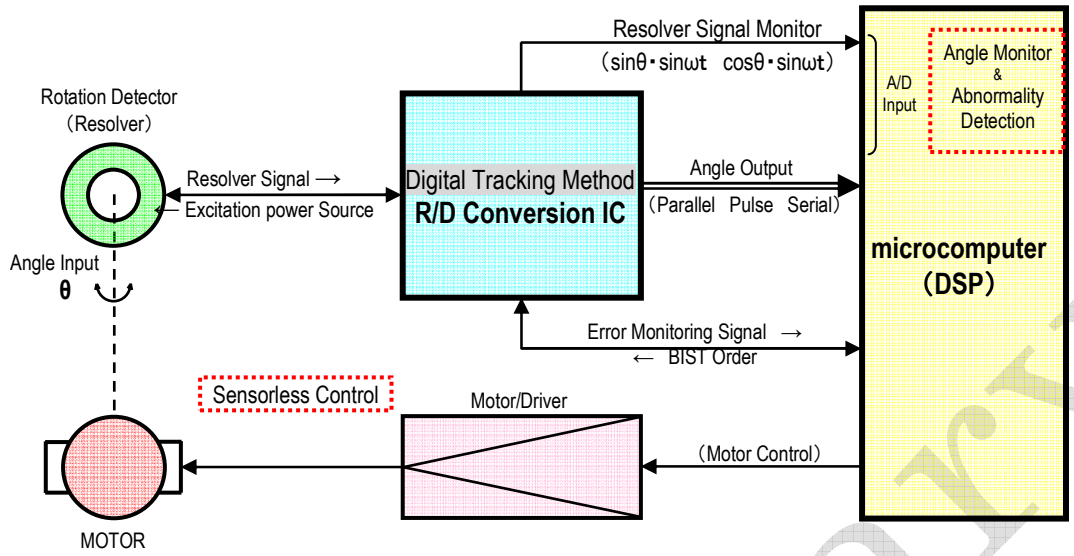
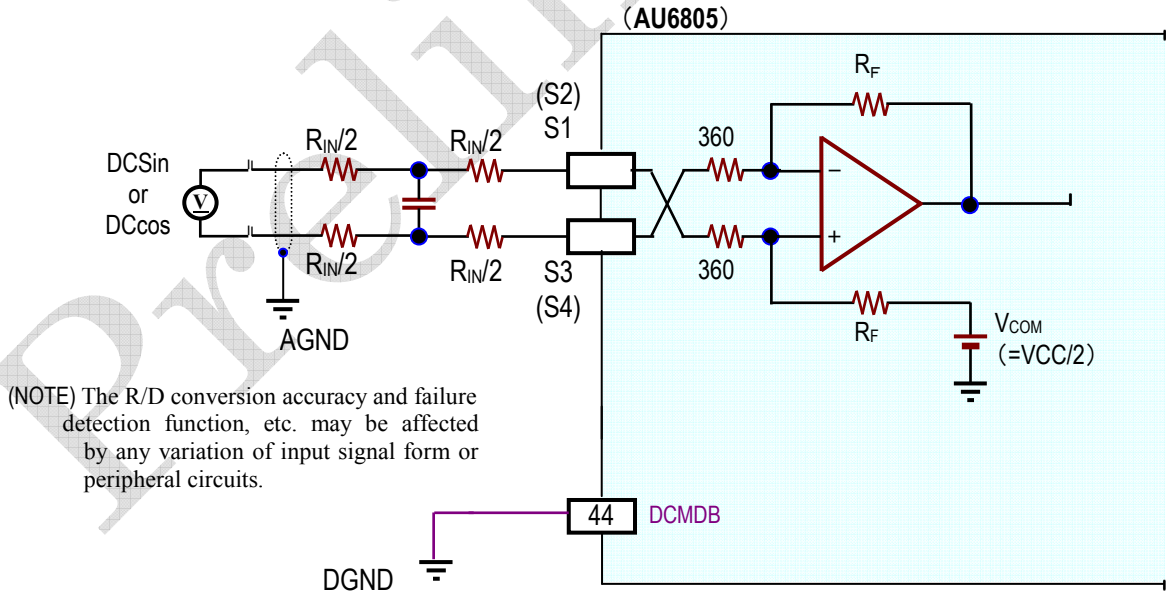


Figure 23. Fail-safe system architecture basic model

5.5 Encoder Application

Though originally resolver signal(K·sinθ•sinωt, K•cosθ•sinωt) contains exciting components(sinωt), this IC is able to function effectively to input even DC resolver signal(E•sinθ, E•cosθ) without exciting components.

It is able to input DC resolver signal to resolver signal input circuit to set DCMDB terminal to L level.



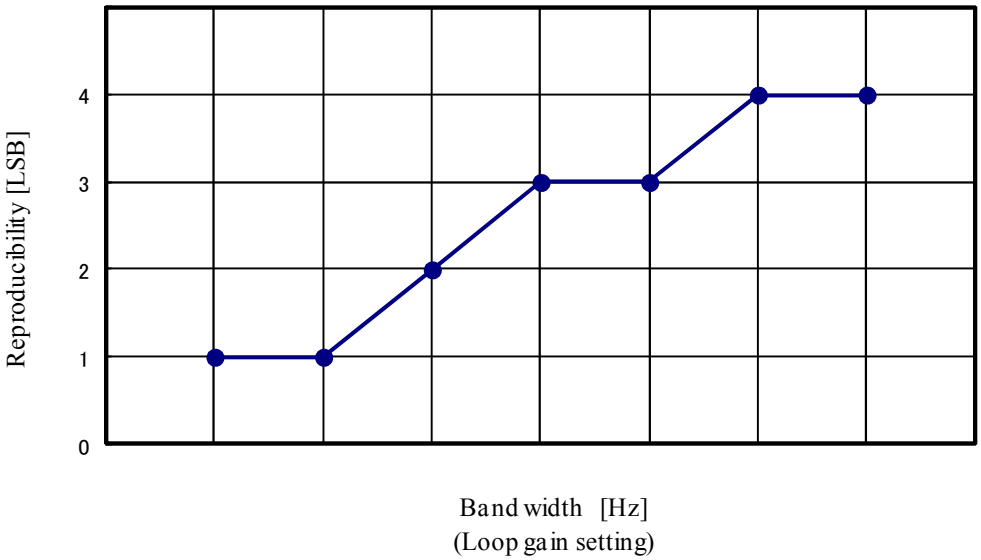
(NOTE) The R/D conversion accuracy and failure detection function, etc. may be affected by any variation of input signal form or peripheral circuits.

Figure 24. Encoder Application

Preliminary

Appended Figure.1　Reproducibility by bandwidth (Roop gain Setting)

(Input Resisntance RIN 4kΩ, 50 degreeC/5V/Process Type)



Prelim

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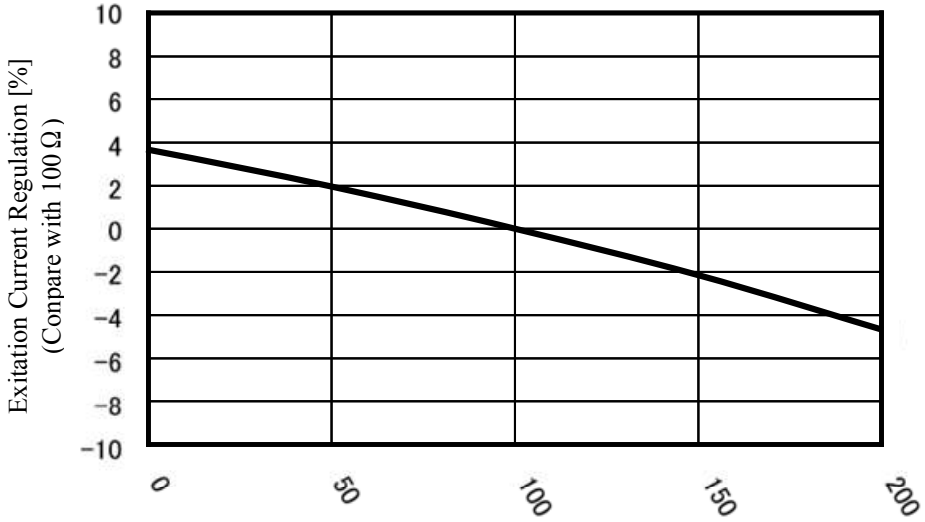
Exitation Loaded Resistance VS Exitation Current Regulation
(10mArms mode, 50degreeC / 5V/ Process Typ)



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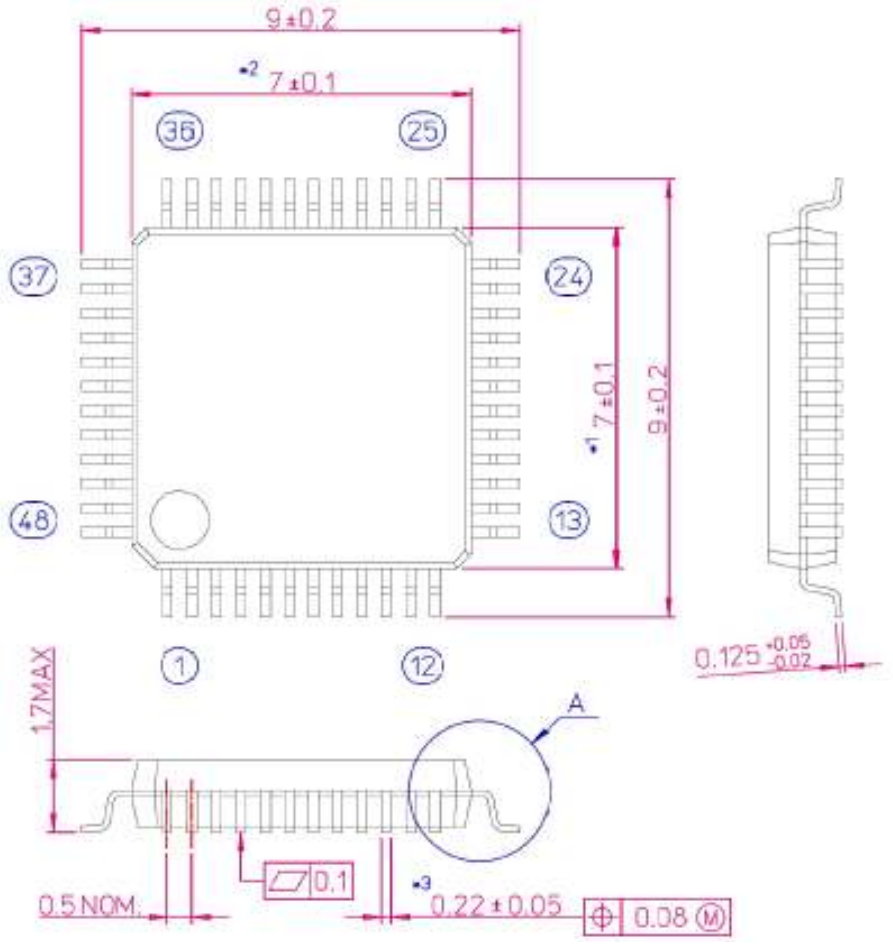
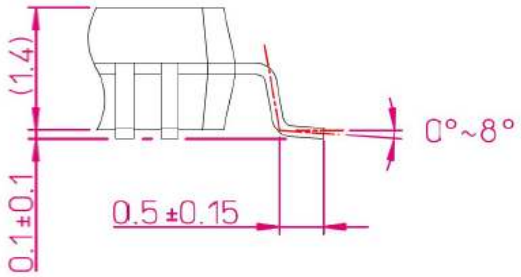
Exitation Loaded Resistance VS Exitation Current Regulation
(20mArms mode, 50degreeC / 5V/ Process Typ)

Appended Figure.2 Excitation current output vs load resistance characteristics

48PIN LQFP (PLASTIC)





Detail A (NTS)

NOTE)
1. Dimensions "*1" and "*2" Do not include mold flash.
2. Dimensions "*3" does not include trim offset.

Attended Figure.2 AU6805 Package Outline Figure

Edition No.

Confidential	DWG NO.	3	4	5	6	7	8	9	10	11	12	SHEET
	S P	C	0	0	0	6	3	0	W	0	0	38