NOTES - UNLESS OTHERWISE NOTED:

1. RESISTANCE VALUES ARE IN OHMS
2. CAPACITANCE VALUES ARE IN MICROFARADS (uF)
3. ALL 0.1uF and 0.01uF CAPACITORS ARE FOR DECOUPLING PURPOSES AND SHOULD BE PLACED CLOSE TO THE IC THEY ARE SHOWN NEAR ON THE SCHEMATIC.

REVISION HISTORY			
REV	DESCRIPTION	DATE	ENG
1	INITIAL RELEASE	05/21/15	WAS
2	BUGS 1137, 1138, 1139, 1154, 1167, 1182, 1195, 1197, 1198, 1203, 1212, 1218, 1219, 1238, 1286, 1287, 1288, 1301, 1315, 1337, 1338, 1339, 1361.	10/20/15	WAS
-	INITIAL PRODUCTION RELEASE. CHANGES INCORPORATED PER BUGS 1818 - 1822	05/19/16	WAS

PAGE 01: TITLE
PAGE 02: BLOCK DIAGRAM
PAGE 03: BIDIRECTIONAL POWER
PAGE 04: INPUT FEEDBACK
PAGE 05: BIDIRECTIONAL FEEDBACK
PAGE 06: DC BUS FEEDBACK
PAGE 07: 24V0 & 12V0 POWER
PAGE 08: 5V0 & 3V3 POWER
PAGE 09: DRV0 - GATE DRIVE
PAGE 10: DRV0 - FETS
PAGE 11: DRV0 - FB/SENSE
PAGE 12: DRV0 - CURRENT SD
PAGE 13: DRV0 - POS FB INTFC
PAGE 13: DRV0 - POS FB MUX
PAGE 15: DRV0 - RESOLVER PG 1
PAGE 16: DRV0 - RESOLVER PG 2
PAGE 17: DRV1 - GATE DRIVE
PAGE 18: DRV1 - FETS
PAGE 19: DRV1 - FB/SENSE
PAGE 20: DRV1 - CURRENT SD
PAGE 21: DRV1 - POS FB INTFC
PAGE 22: DRV1 - POS FB MUX
PAGE 23: DRV1 - RESOLVER PG 1
PAGE 24: DRV1 - RESOLVER PG 2
PAGE 25: BUFFERS
PAGE 26: HSMC CONNECTOR
PAGE 27: MAX10 ANALOG CONNECTOR
PAGE 28: 2V5 SUPPLY

BARE BOARD

PCB-072004001

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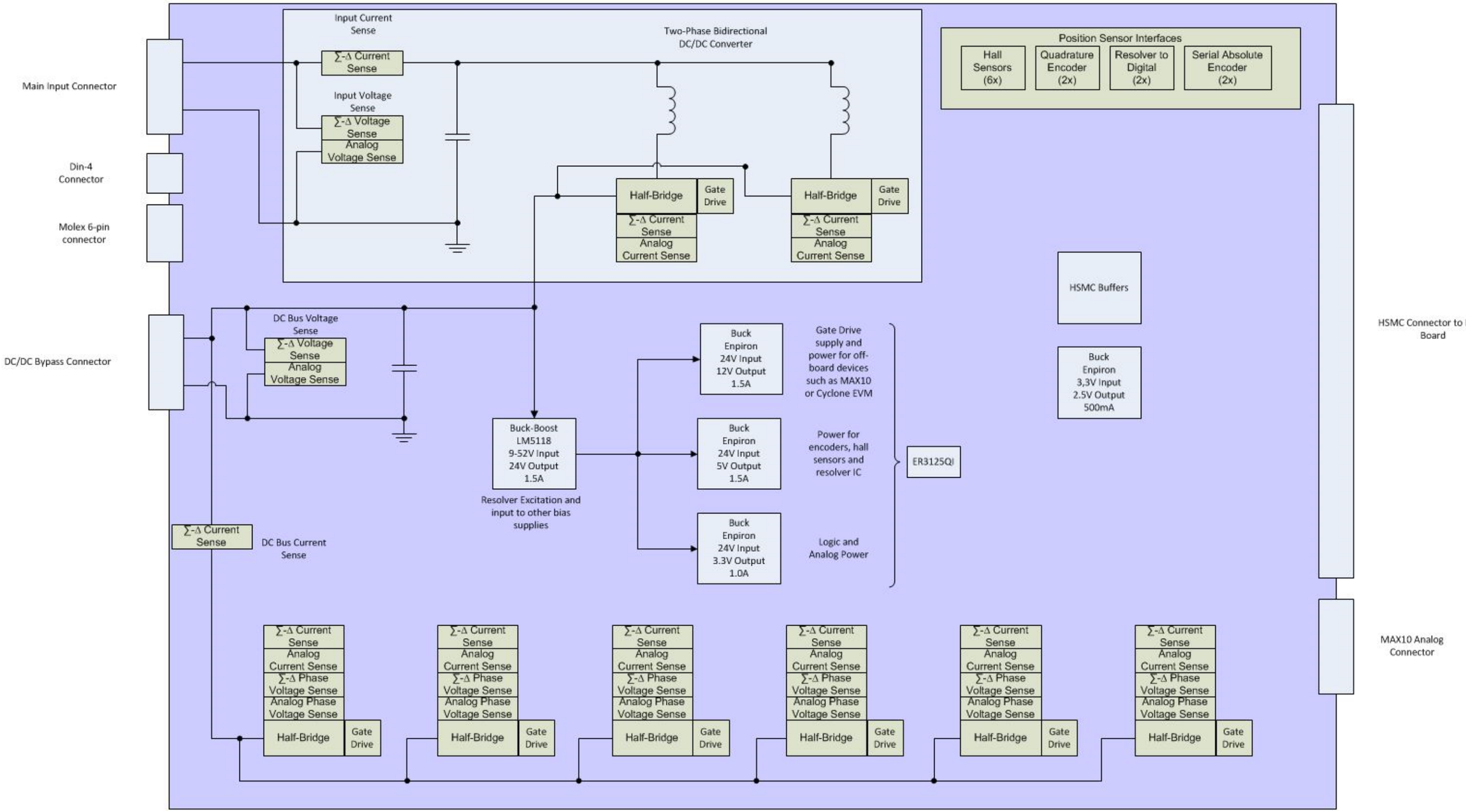
Low Voltage DC to DC and Dual Axis Motor Control Board

Title Page

SIZE	CAGE CODE	DWG NO	REV
B	3V6D5	SCH-072004001	-

SCALE	DWN BY:	APRVD BY:	SHEET
1:1	WAS	JPW	1 OF 28

Thursday, May 19, 2016



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Block Diagram

SIZE	CAGE CODE	DWG NO	REV
B	3V6D5	SCH-072004001	-

SCALE	DWN BY:	APRVD BY:	SHEET
1:1	WAS	JPW	2 OF 28

[4] INPUT_SNS_IN
INPUT_SNS_OUT [4]
[5] BOOST_DRV0_SNS_IN
BOOST_DRV0_SNS_OUT [5]
TP1 TEST-POINT RND
TP2 TEST-POINT RND
TP112 TEST-POINT RND
TP111 TEST-POINT RND
[4] INPUT_VOLTAGE
SILK LABEL: INPUT
TP4 TP-LOOP-RED
INPUT VOLTAGE: 9-16V
R2 0.005 1% 5W
R1 0.007 1% 3W
26A
22uH L1
BOOST_DRV0_GH
BOOST_DRV0_SH
BOOST_DRV0_GL
Q2 SiR826DP 80V 60A
Q1 SiR826DP 80V 60A
DGND
SILK LABEL: BOOST OUTPUT
TP3 TP-LOOP-RED
OUTPUT VOLTAGE: 48V
VDD_BOOST
J1
SILK LABEL: BATTERY
REGEN_EN [26]
VDD_IO
TERM BLOCK HEADER 6x1
C220 0.1uF 25V 20%
C228 270uF 25V 20%
C1 270uF 25V 20%
C2 270uF 25V 20%
C3 82uF 100V 20%
C4 82uF 100V 20%
C5 82uF 100V 20%
C6 82uF 100V 20%
C7 82uF 100V 20%
C8 82uF 100V 20%
NOTE: CERAMIC CAP FOR HF ELEMENTS
R3 0.007 1% 3W
26A
22uH L2
BOOST_DRV1_GH
BOOST_DRV1_SH
BOOST_DRV1_GL
Q4 SiR826DP 60A 80V
Q3 SiR826DP 80V 60A
TP113 TEST-POINT RND
TP114 TEST-POINT RND
[5] BOOST_DRV1_SNS_IN
BOOST_DRV1_SNS_OUT [5]
J2
DIN
KPJX-4S S
J46
39-30-1060
C219 0.1uF 100V 10%
C271 0.1uF 100V 10%
C272 1.0uF 100V 10%
C273 1.0uF 100V 10%
NOTE: CERAMIC CAP FOR HF ELEMENTS
TP162 TEST-POINT RND
TP161 TEST-POINT RND
VDD_12V0
U1
[26] BOOST_DRV0_PWM_H
[26] BOOST_DRV0_PWM_L
VDD HB HI HO LI HS VSS LO PPAD
UCC27201A
C9 0.1uF 25V 20%
R5 NP
R6 10.0 1%
R7 10.0 1%
R8 NP
D2
D3
TP165 TEST-POINT RND
TP166 TEST-POINT RND
TP167 TEST-POINT RND
R372 1.0K_1%
R373 1.0K_1%
C10 0.1uF 25V 20%
C11 4.7uF 25V 10%
MH1 MH2 MH3 MH4 MH5 MH6 MH7
TP5 TP-LOOP-BLACK
TP7 TP-LOOP-BLACK
TP9 TP-LOOP-BLACK
TP6 TP-LOOP-BLACK
TP8 TP-LOOP-BLACK
TP10 TP-LOOP-BLACK
TP163 TEST-POINT RND
TP164 TEST-POINT RND
U2
[26] BOOST_DRV1_PWM_H
[26] BOOST_DRV1_PWM_L
C14 0.1uF 25V 20%
R9 NP
R10 10.0 1%
R11 10.0 1%
R12 NP
D4
D5
TP168 TEST-POINT RND
TP169 TEST-POINT RND
TP170 TEST-POINT RND
R374 1.0K_1%
R375 1.0K_1%
C12 0.1uF 25V 20%
C13 4.7uF 25V 10%

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Bidirectional Power Supply

SIZE	CAGE CODE	DWG NO	REV
B	3V6D5	SCH-072004001	-

SCALE	DWN BY:	APRVD BY:	SHEET
1:1	WAS	JPW	3 OF 28

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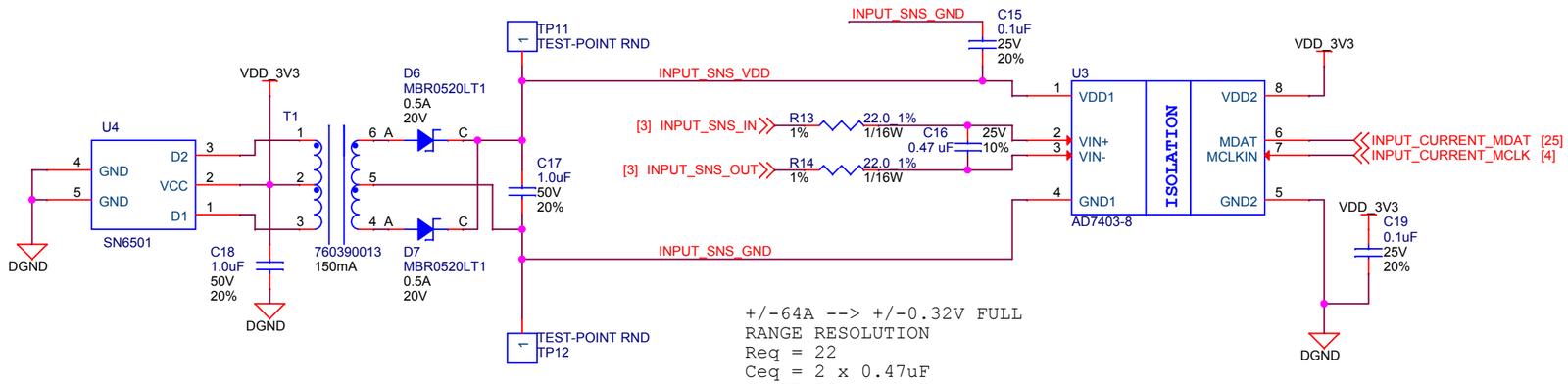

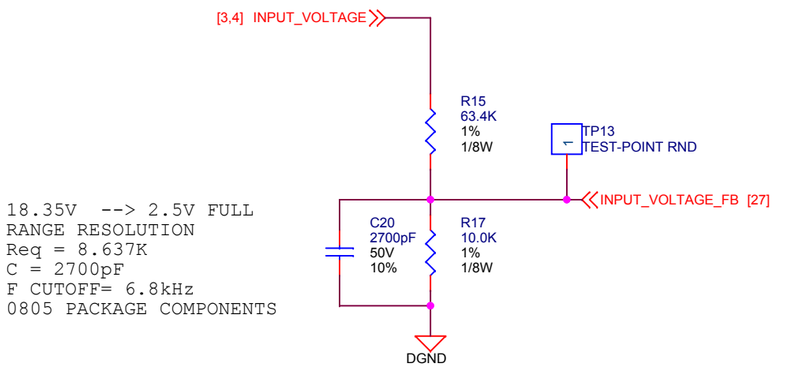

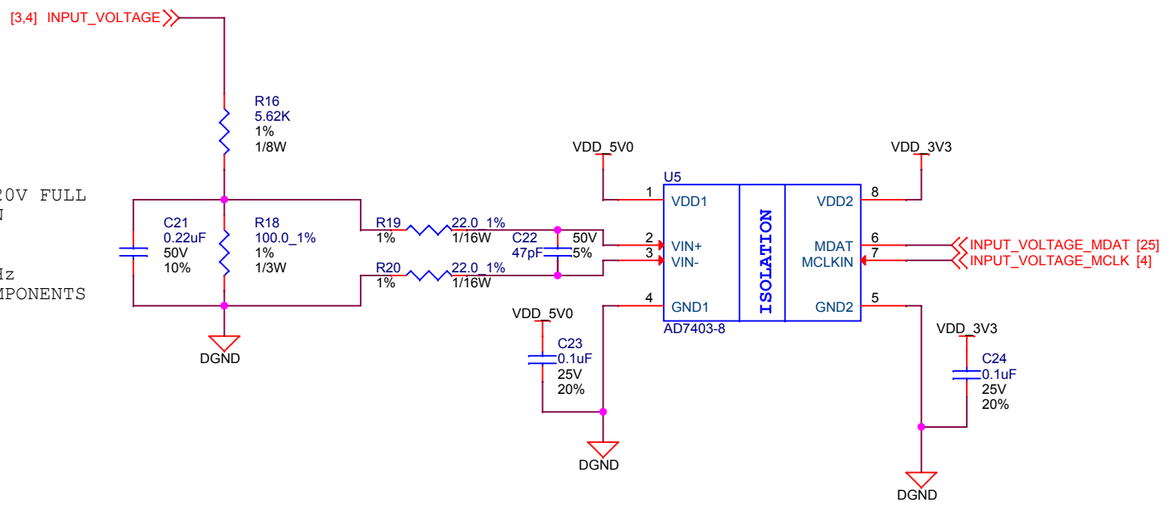

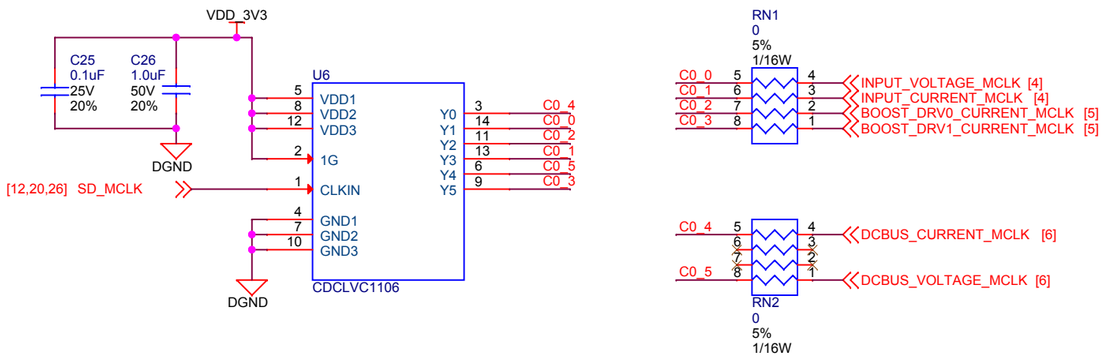

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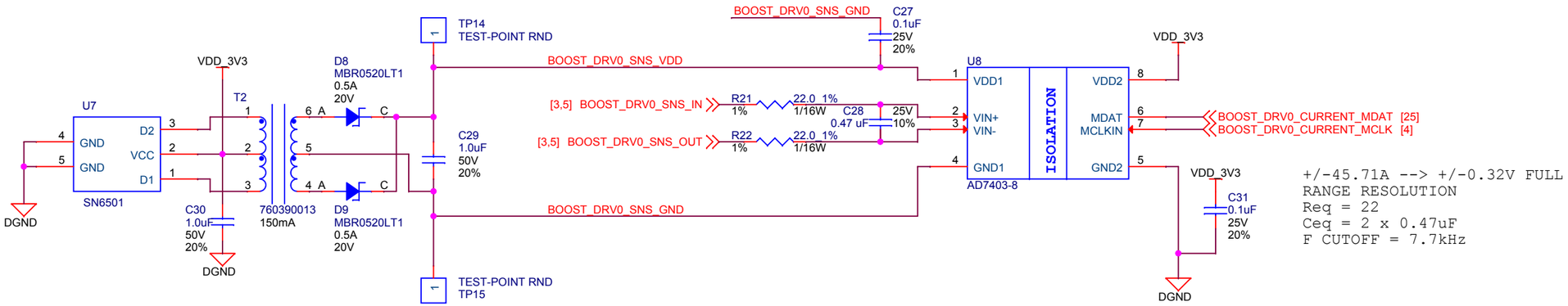
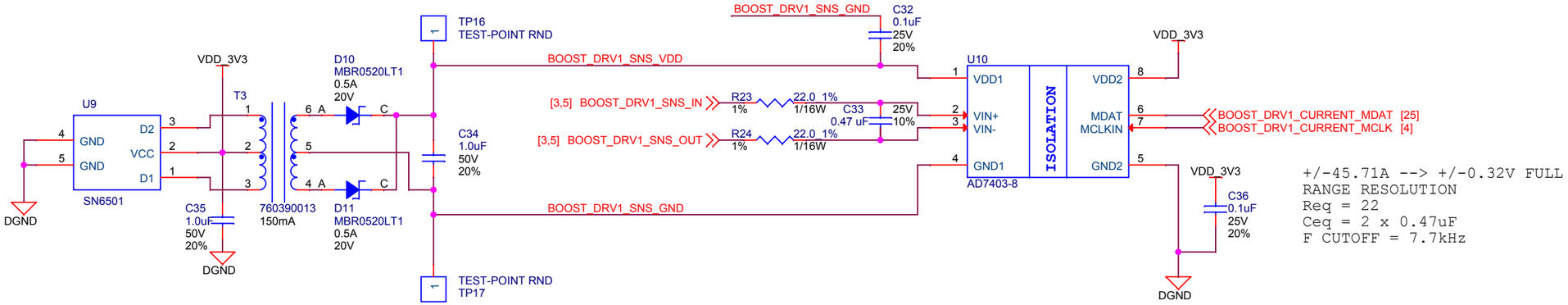
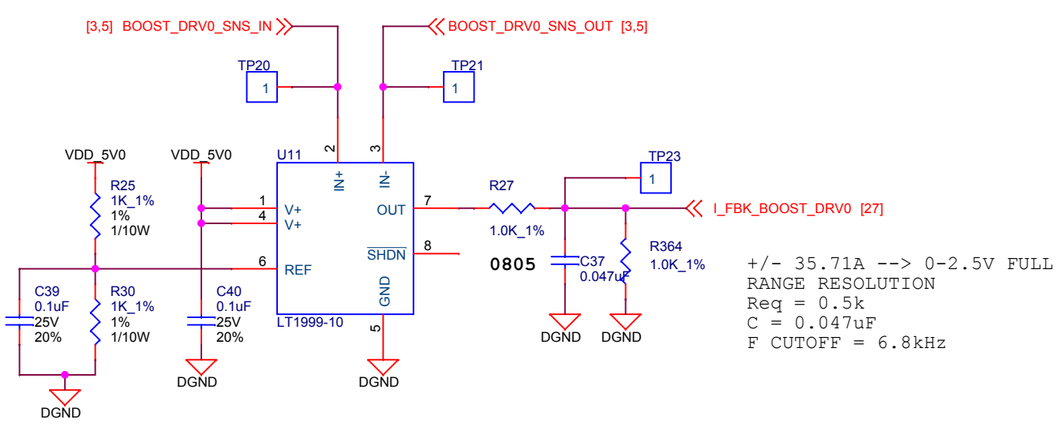
System Power Input Feedback and Sense

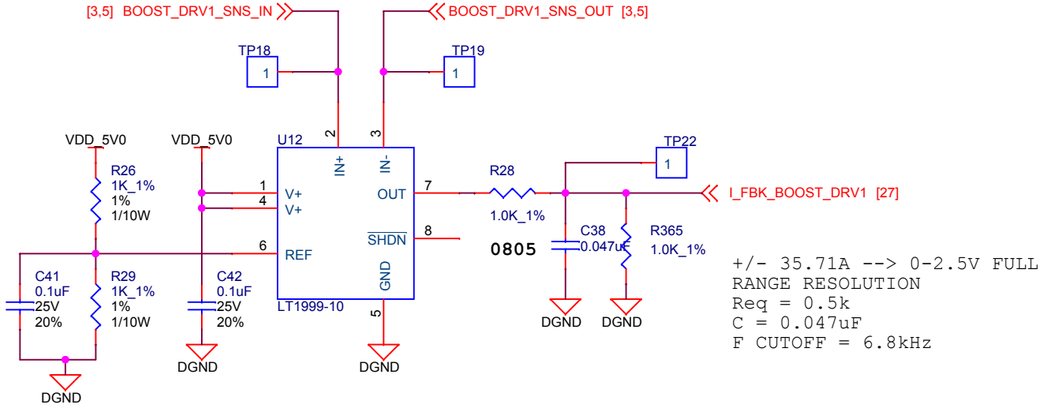
SIZE	CAGE CODE	DWG NO	REV
B	3V6D5	SCH-072004001	-

SCALE	DWN BY:	APRVD BY:	SHEET
1:1	WAS	JPW	4 OF 28









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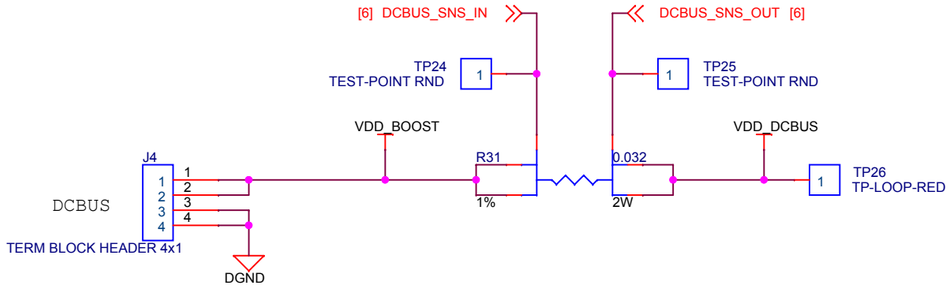
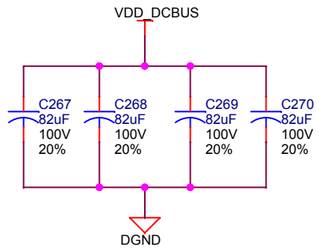
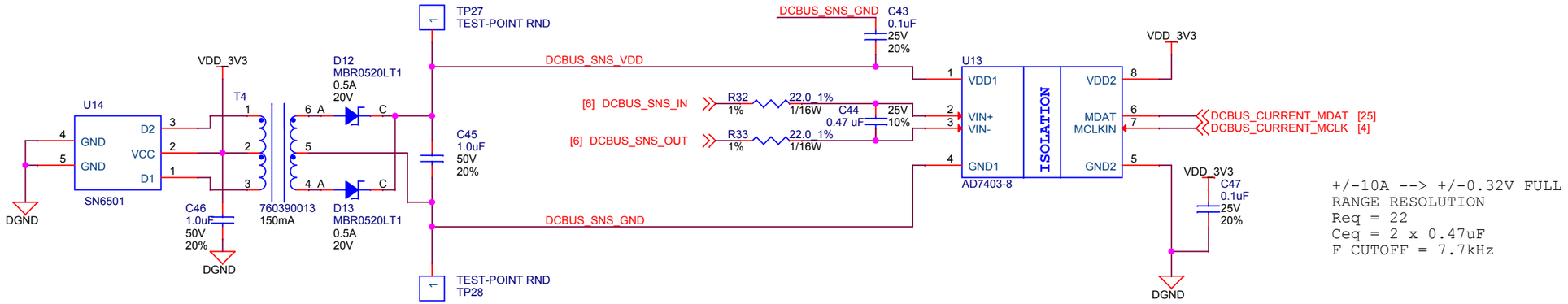
Bidirectional Power Supply Feedback

SIZE	CAGE CODE	DWG NO	REV
B	3V6D5	SCH-072004001	-

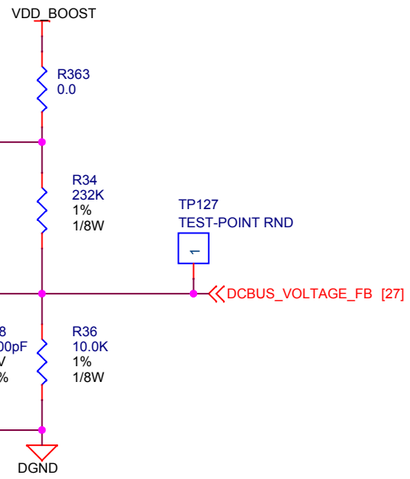
SCALE	DWN BY:	APRVD BY:	SHEET
1:1	WAS	JPW	5 OF 28





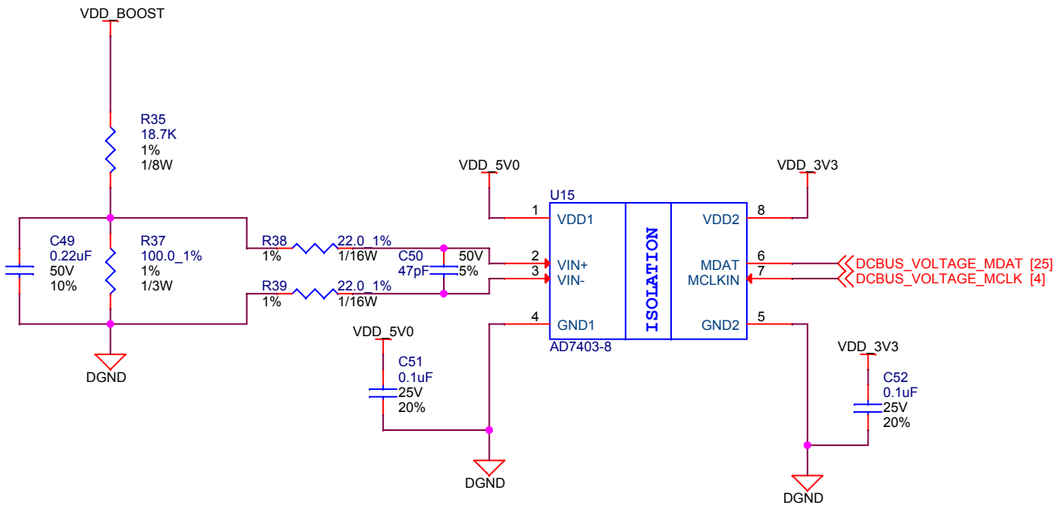


+/-10A --> +/-0.32V FULL
RANGE RESOLUTION
Req = 22
Ceq = 2 x 0.47uF
F CUTOFF = 7.7kHz



60.5V --> 2.5V FULL
RANGE RESOLUTION
Req = 9.59k
C = 2700pF
F CUTOFF = 6.15kHz

60.16V --> 0.320V FULL
RANGE RESOLUTION
Req = 99.47
C = 0.22uF
F CUTOFF = 7.3kHz



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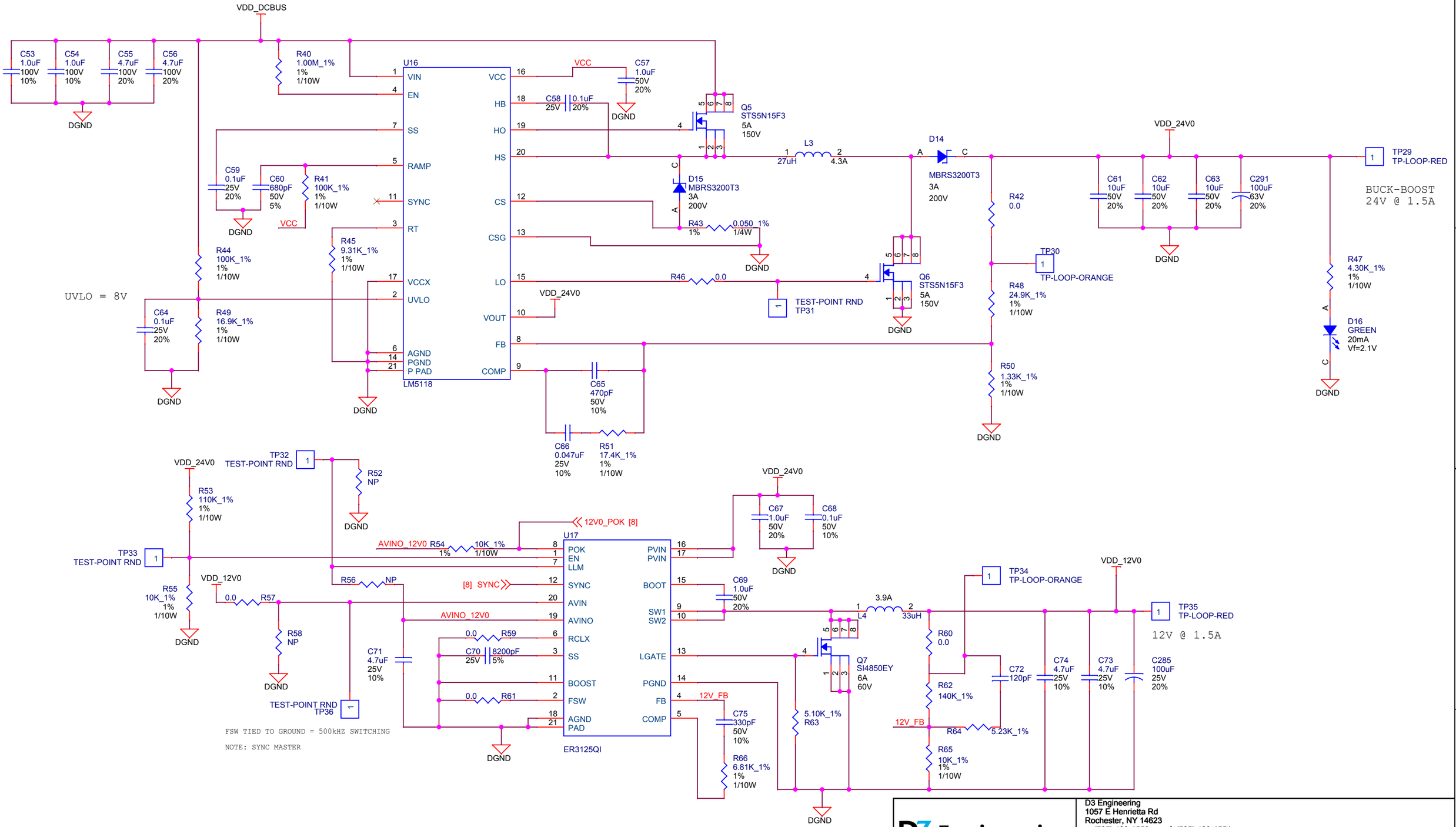
DC Bus Feedback

SIZE	CAGE CODE	DWG NO	REV
B	3V6D5	SCH-072004001	-

SCALE	DWN BY:	APRVD BY:	SHEET
1:1	WAS	JPW	6 OF 28



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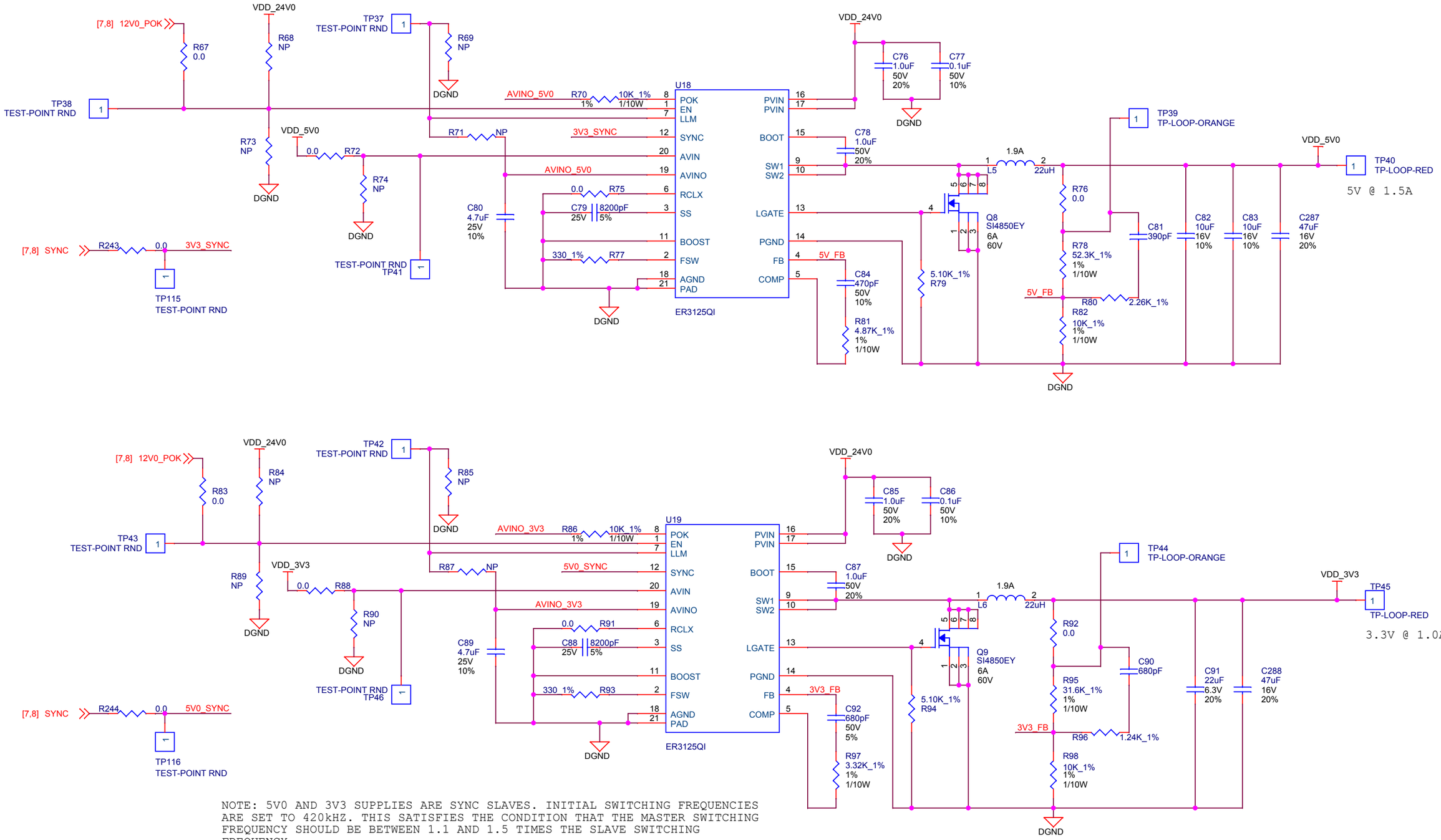
Low Voltage DC to DC and Dual Axis Motor Control Board

24V and 12V Power Domains

SIZE	CAGE CODE	DWG NO	REV
B	3V6D5	SCH-072004001	-

SCALE	DWN BY:	APRVD BY:	SHEET
1:1	WAS	JPW	7 OF 28



NOTE: 5V0 AND 3V3 SUPPLIES ARE SYNC SLAVES. INITIAL SWITCHING FREQUENCIES ARE SET TO 420kHZ. THIS SATISFIES THE CONDITION THAT THE MASTER SWITCHING FREQUENCY SHOULD BE BETWEEN 1.1 AND 1.5 TIMES THE SLAVE SWITCHING FREQUENCY.

THE 5V0 AND 3V3 SWITCHERS ARE GETTING THEIR ENABLES FROM THE 12V POWER OKAY. THIS RESULTS IN A 24V0->12V0->(5V0 & 3V3) POWER SEQUENCE.

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5V and 3.3V Power Domains

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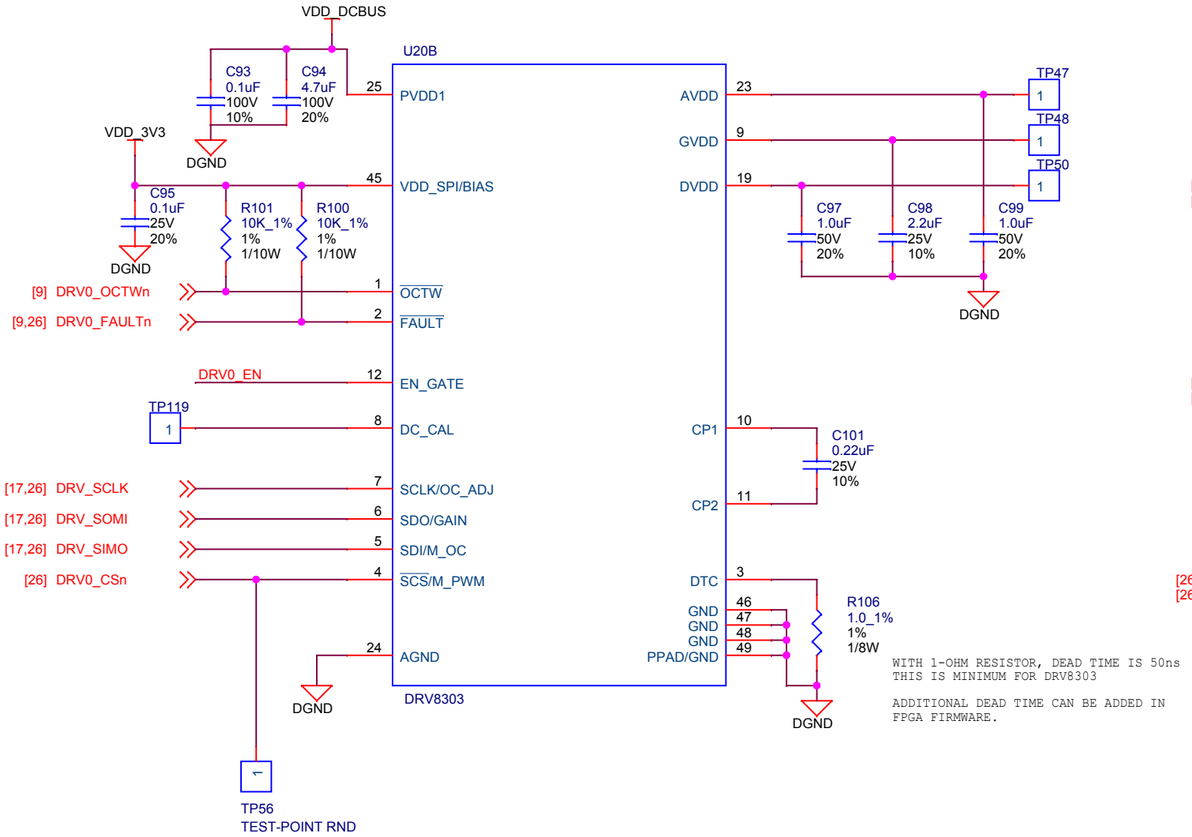
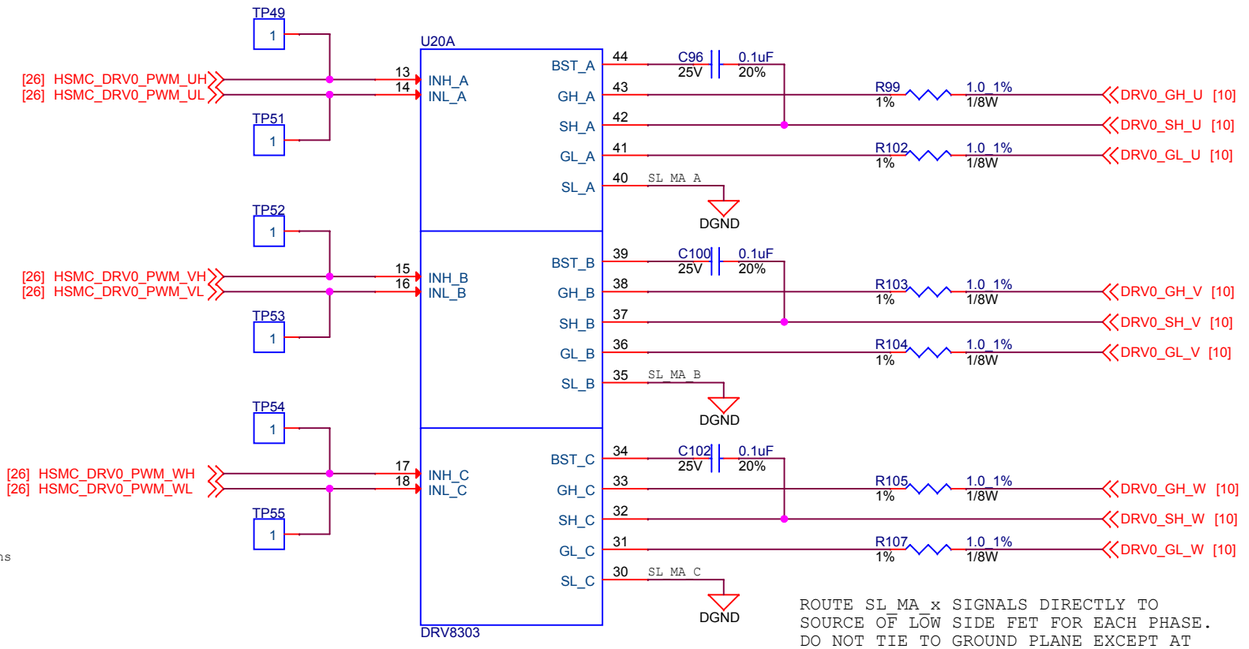
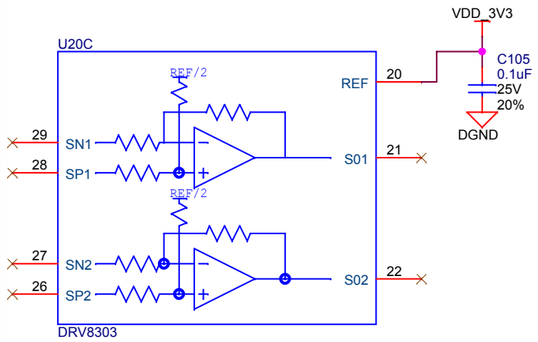
SIZE	CAGE CODE	DWG NO	REV
B	3V6D5	SCH-072004001	-

Monday, May 16, 2016

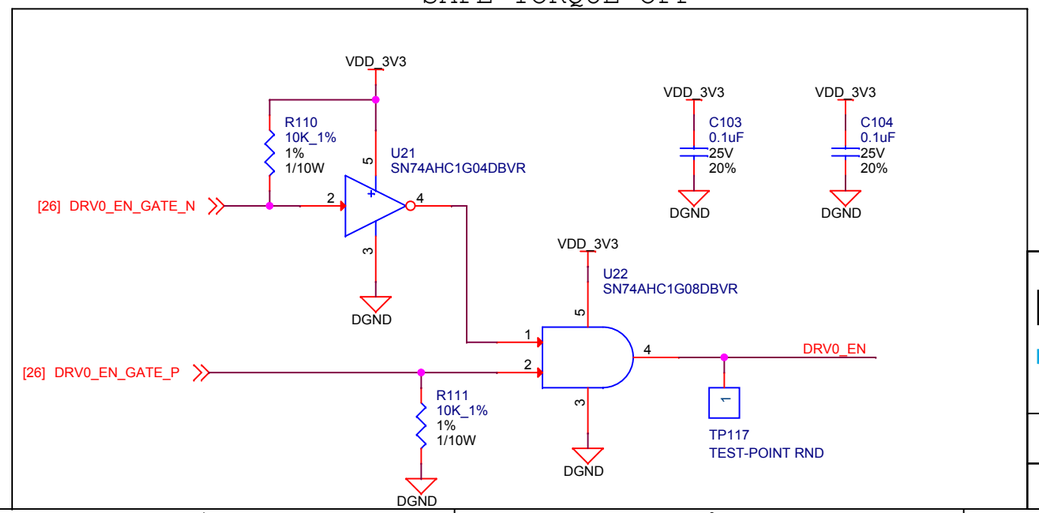
SCALE	DWN BY:	APRVD BY:	SHEET
1:1	WAS	JPW	8 OF 28

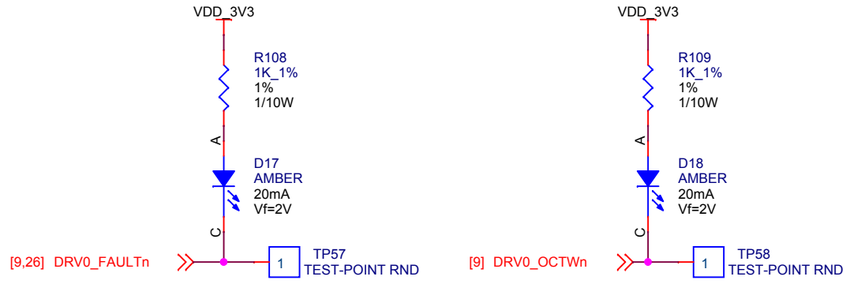






SAFE TORQUE OFF





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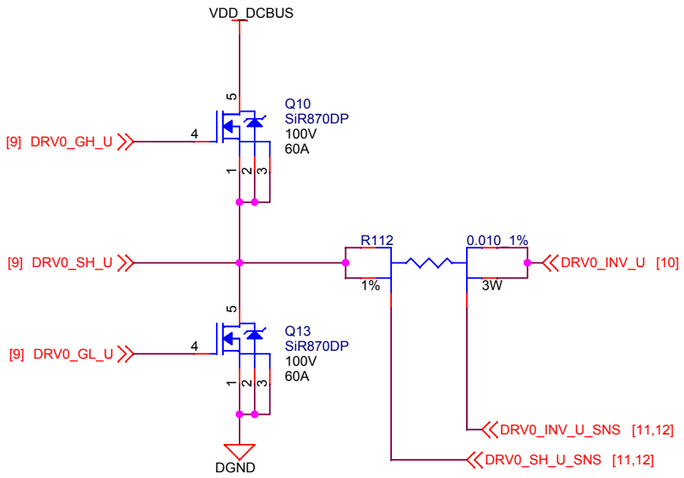
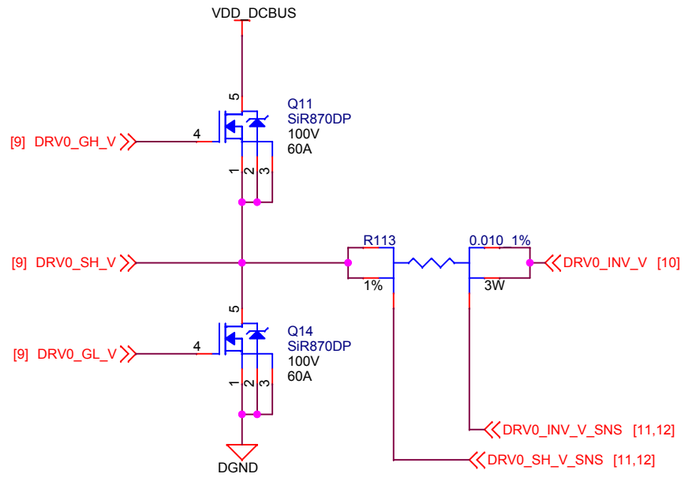
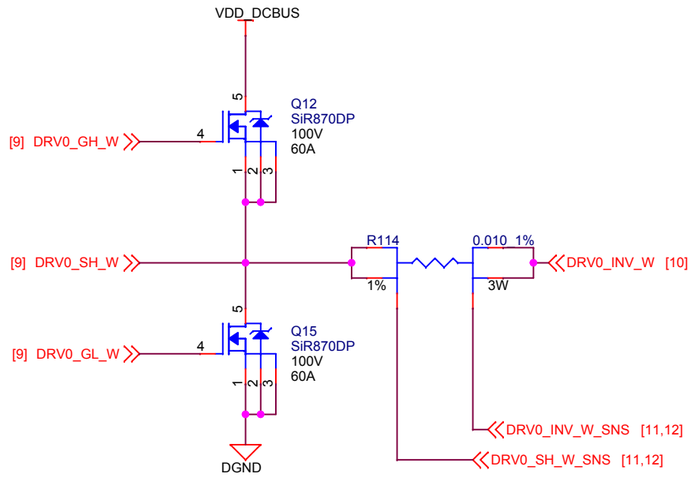
Phase 0: Inverter Gate Drivers

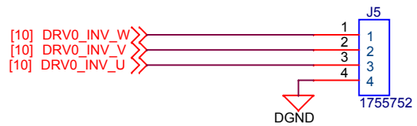
SIZE	CAGE CODE	DWG NO	REV
B	3V6D5	SCH-072004001	-

SCALE	DWN BY:	APRVD BY:	SHEET
1:1	WAS	JPW	9 OF 28









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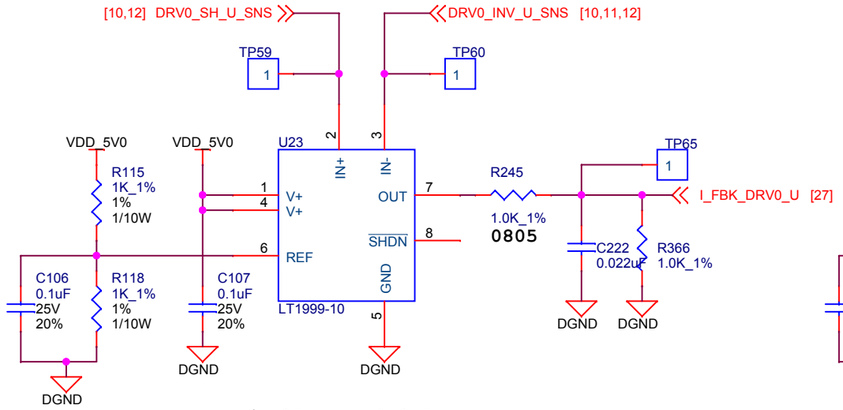
Low Voltage DC to DC and Dual Axis Motor Control Board

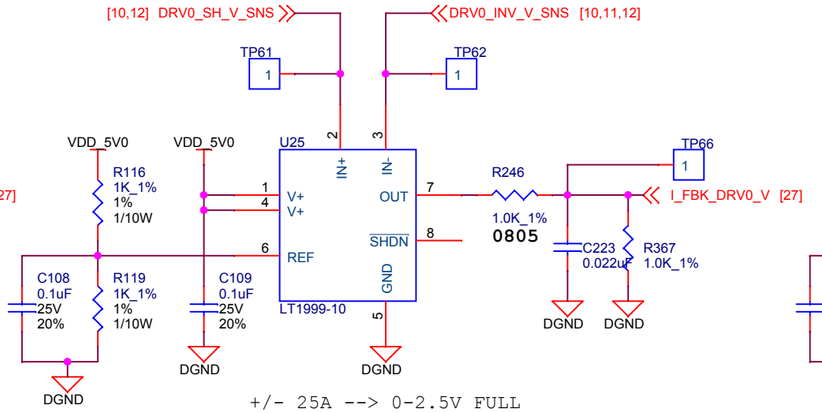
DRV0 & DRV1: Inverter FETs

SIZE	CAGE CODE	DWG NO	REV
B	3V6D5	SCH-072004001	-

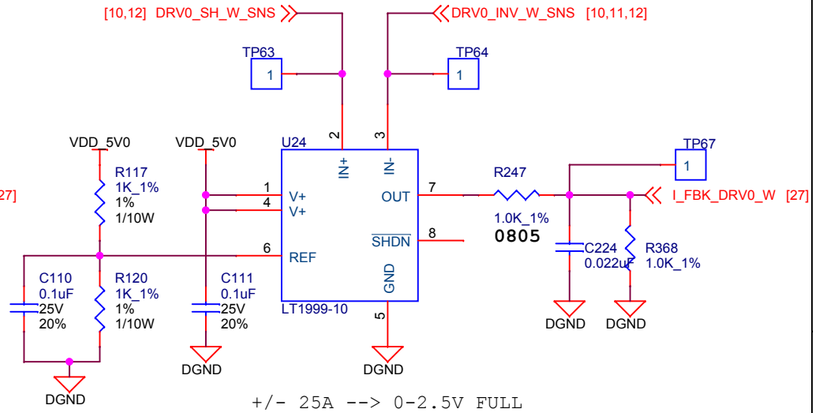
SCALE	DWN BY:	APRVD BY:	SHEET
1:1	WAS	JPW	10 OF 28



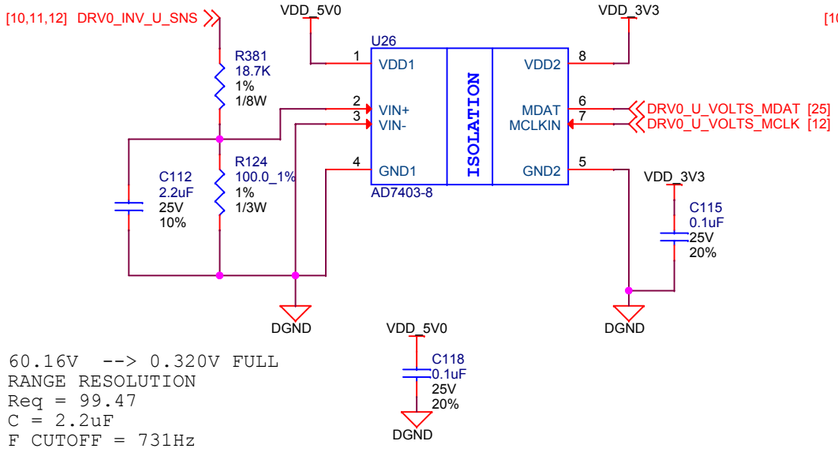
+/- 25A --> 0-2.5V FULL
RANGE RESOLUTION
Req = 0.5k
C = 22,000pF
F CUTOFF = 14 kHz



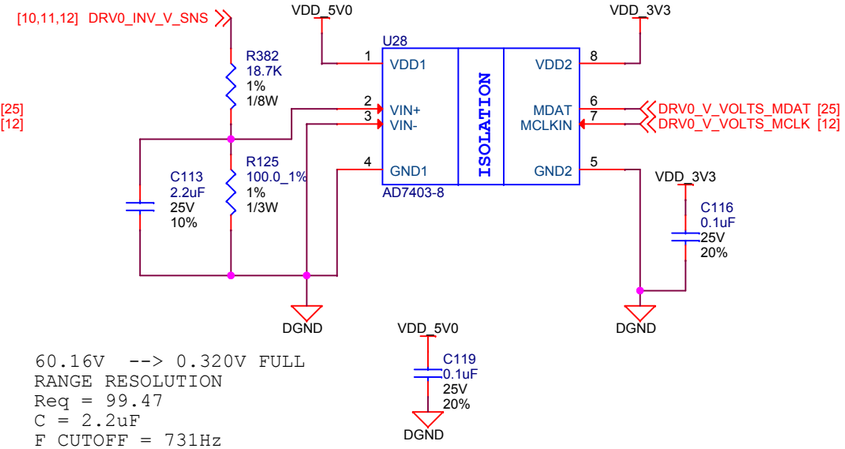
+/- 25A --> 0-2.5V FULL
RANGE RESOLUTION
Req = 0.5k
C = 22,000pF
F CUTOFF = 14 kHz



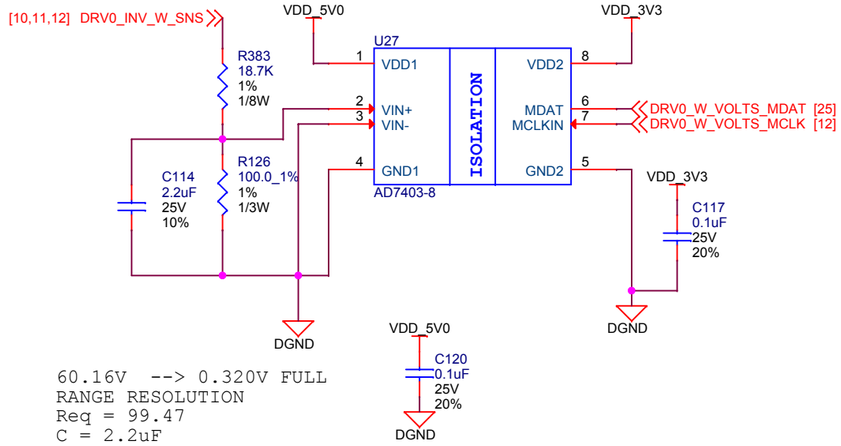
+/- 25A --> 0-2.5V FULL
RANGE RESOLUTION
Req = 0.5k
C = 22,000pF
F CUTOFF = 14 kHz



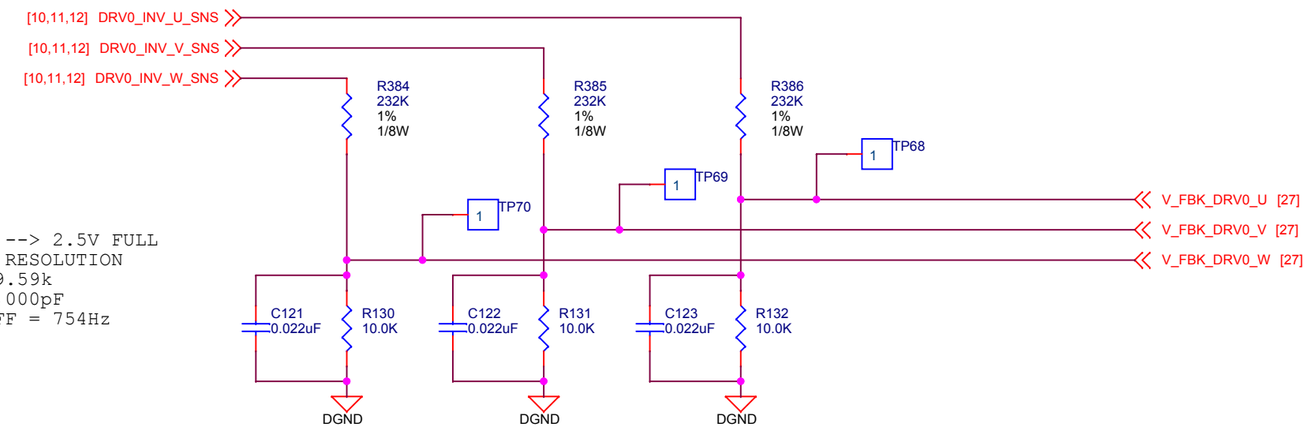
60.16V --> 0.320V FULL
RANGE RESOLUTION
Req = 99.47
C = 2.2uF
F CUTOFF = 731Hz



60.16V --> 0.320V FULL
RANGE RESOLUTION
Req = 99.47
C = 2.2uF
F CUTOFF = 731Hz



60.16V --> 0.320V FULL
RANGE RESOLUTION
Req = 99.47
C = 2.2uF
F CUTOFF = 731Hz



60.5V --> 2.5V FULL
RANGE RESOLUTION
Req = 9.59k
C = 22,000pF
F CUTOFF = 754Hz

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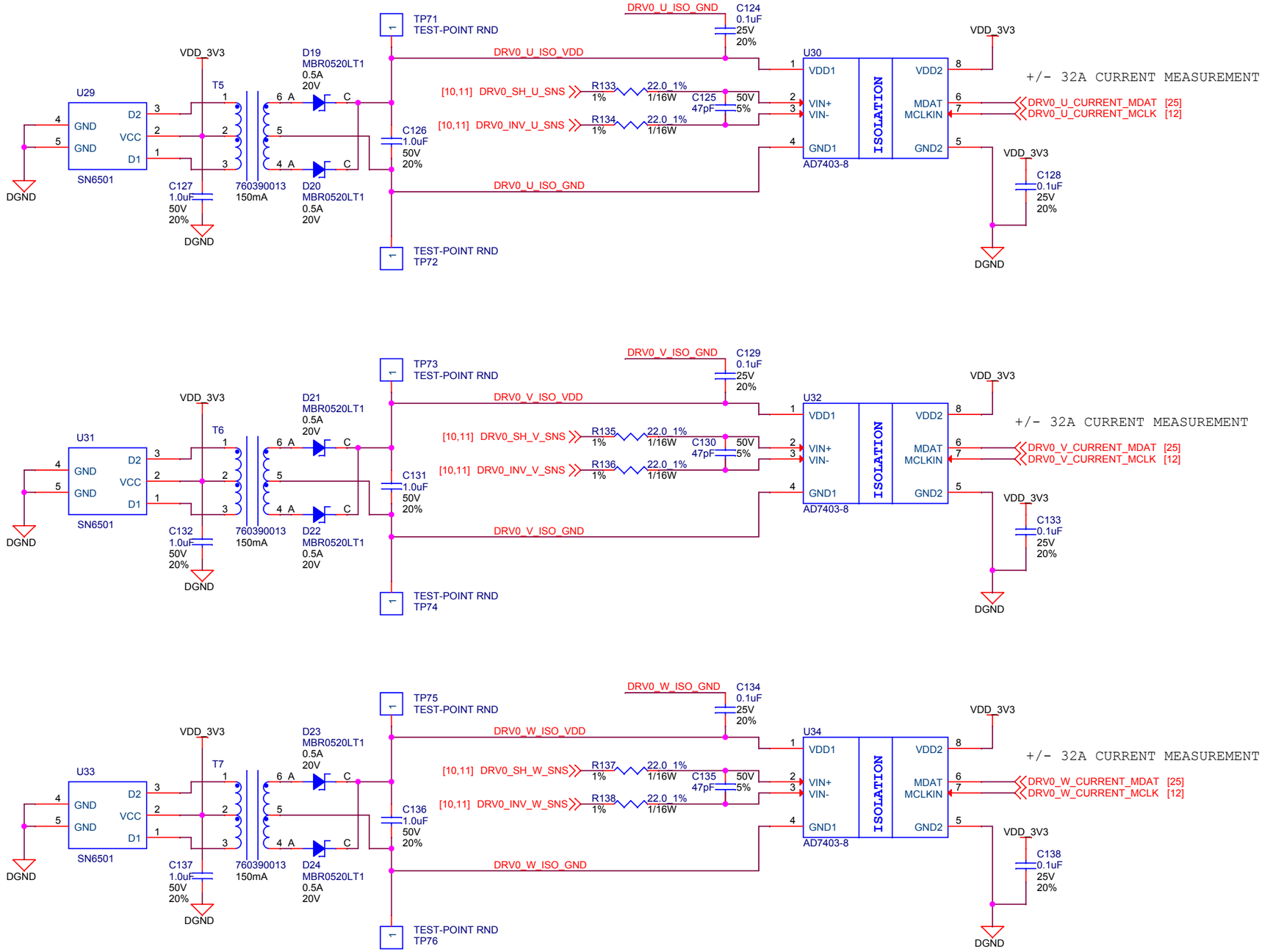
Low Voltage DC to DC and Dual Axis Motor Control Board

DRV0: Voltage and Current Feedback

SIZE	CAGE CODE	DWG NO	REV
B	3V6D5	SCH-072004001	-

SCALE	DWN BY:	APRVD BY:	SHEET
1:1	WAS	JPW	11 OF 28



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Low Voltage DC to DC and Dual Axis Motor Control Board

DRV0: In-Phase Current Sigma Deltas

SIZE	CAGE CODE	DWG NO	REV
B	3V6D5	SCH-072004001	-

SCALE	DWN BY:	APRVD BY:	SHEET
1:1	WAS	JPW	12 OF 28

SHIFTS SIGNALS COMING FROM THE MOTOR FROM 5.0V TO 2.5V

SHIFTS SIGNALS COMING FROM THE FPGA FROM 2.5V TO 5.0V

DEFAULT TO 5V

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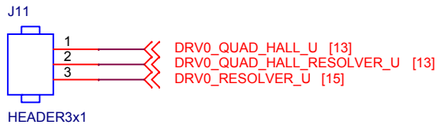
	Low Voltage DC to DC and Dual Axis Motor Control Board		
	DRV0: Position Feedback Interface, Transceivers, & Buffers		
www.D3Engineering.com	SIZE: B	CAGE CODE: 3V6D5	DWG NO: SCH-072004001 / REV: -
Monday, May 16, 2016	SCALE: 1:1	DWN BY: WAS	APRVD BY: JPW / SHEET: 13 OF 28

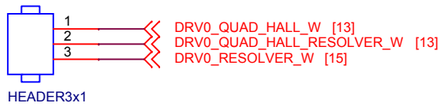
MOTOR DRIVE 0 FEEDBACK BANK A.

CHOOSE BETWEEN QUADRATURE A/B/Z AND RESOLVER A/B/Z. ALL SIGNALS REFERENCED TO 5V.

MOTOR DRIVE 0 FEEDBACK BANK B.

CHOOSE BETWEEN QUADRATURE OR HALL U/V/W AND RESOLVER U/V/W. ALL SIGNALS REFERENCED TO 5V.





MOTOR DRIVE 0 FEEDBACK BANK C.

CHOOSE BETWEEN MOTOR SERIAL ENCORDER AND RESOLVER SERIAL FEEDBACK. SIGNALS ARE REFERENCED TO 5V.

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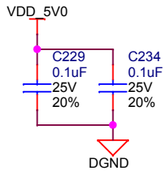
DRV0: Position Feedback Muxes

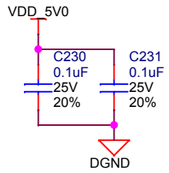
SIZE	CAGE CODE	DWG NO	REV
B	3V6D5	SCH-072004001	-

SCALE	DWN BY:	APRVD BY:	SHEET
1:1	WAS	JPW	14 OF 28

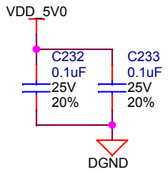
Place these caps near VRR and RGND pins.



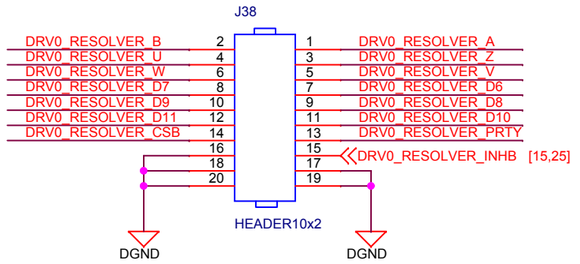
Place these caps near VCC and AGND pins.



Place these caps near VDD and DGND pins.



Test points for entire bus interface



EXMDB DCMDB, INHB and RLV have internal pull-up.

EXMDB - High - R1/R2 are excitation outputs
Low - R1/R2 are excitation inputs

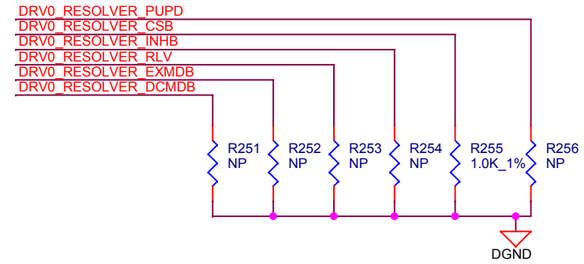
DCMDB - High - Resolver signals are AC (contain carrier)
Low - Resolver signals are DC (no carrier)

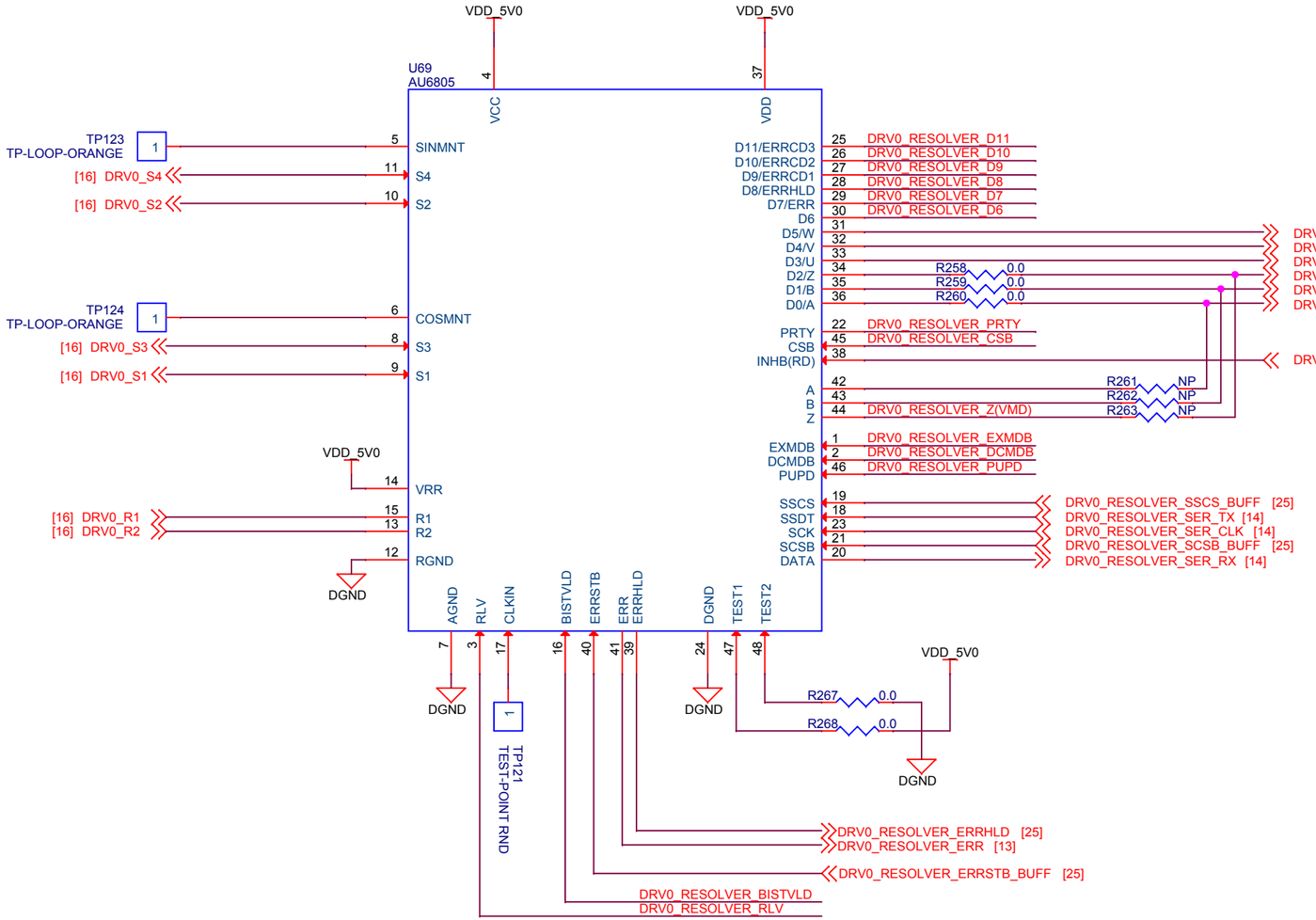
RLV - High - 10mArms excitation current
Low - 20mArms excitation current

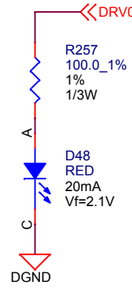
INHB - High - Allow output data to change
Low - Hold output data

CSB - High - D0~D11, PRTY High-Z
Low - D0~D11, PRTY output enable

PUPD - High - Parallel output update freq. 25MHz
Low - Parallel output update freq. 12.5MHz





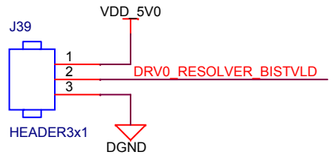


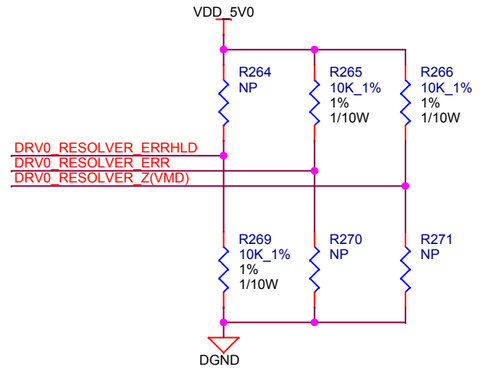
ERRHLD - High - Absolute parallel angle data
Low - Pulses equivalent to encoder

ERR - High - Internal oscillator
Low - External clk input

Z - High - Current excitation mode (VMD=0)
Low - Voltage excitation mode (VMD=1)

BISTVLD - High - Do not allow BIST to execute
Low - Allow BIST to execute





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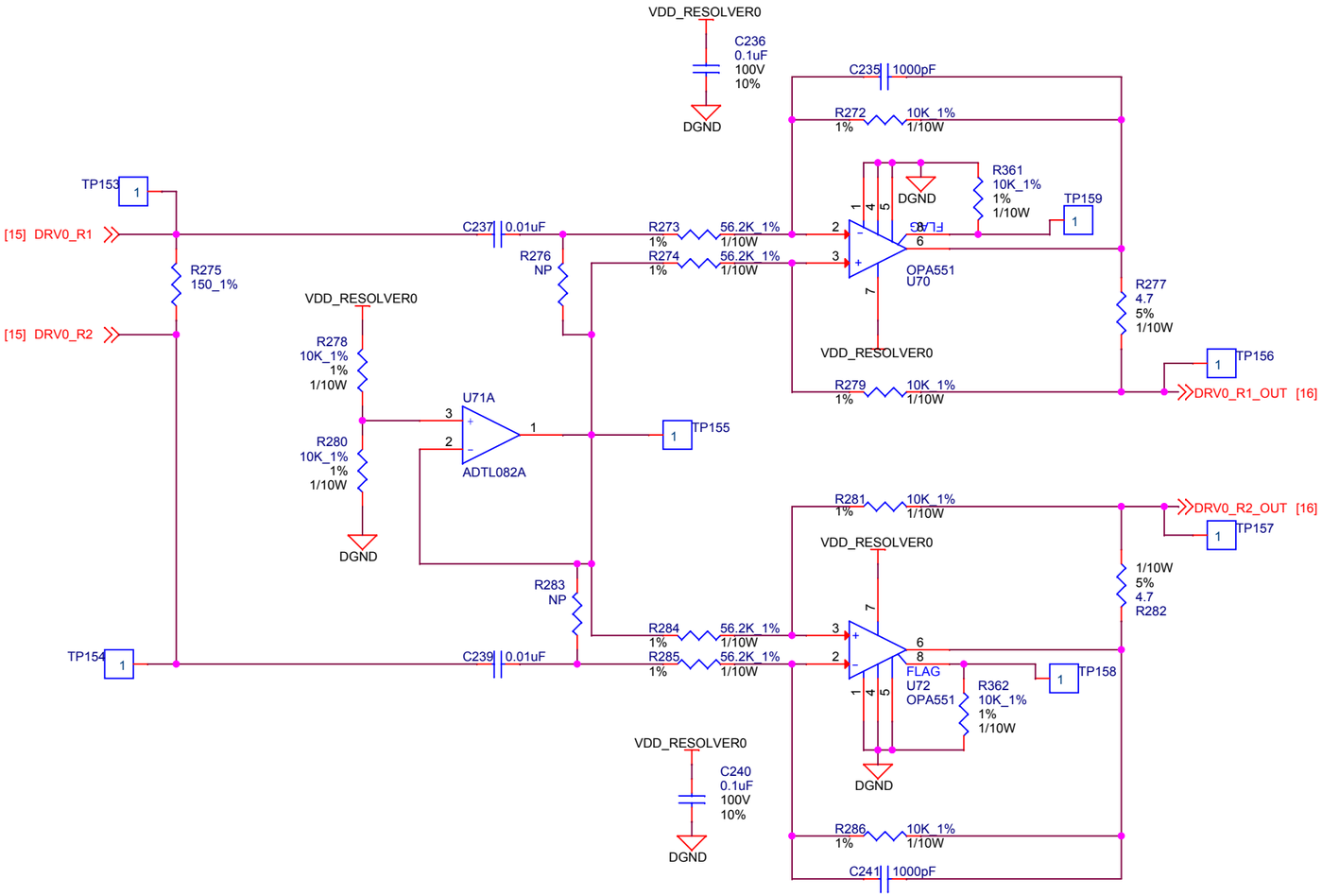
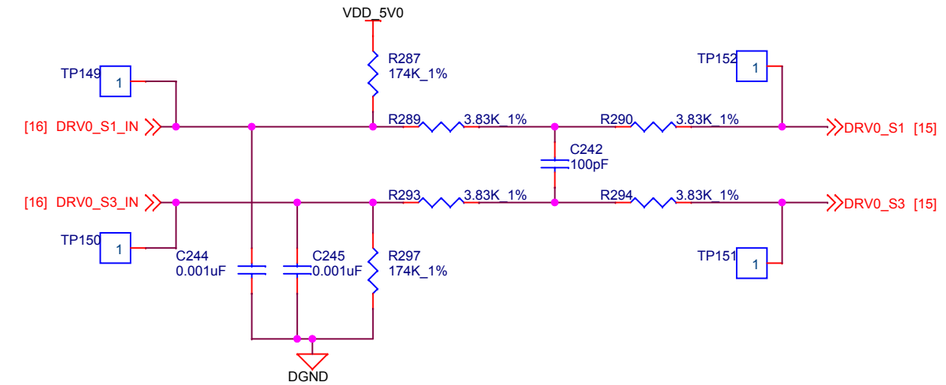
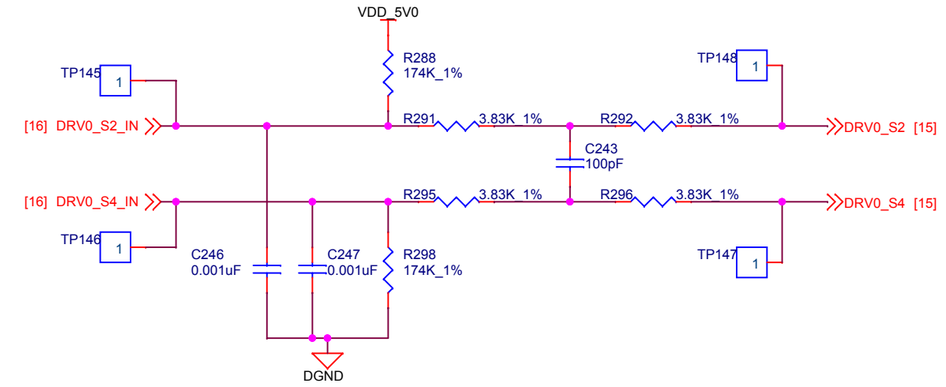
DRV0: Resolver, Page 1

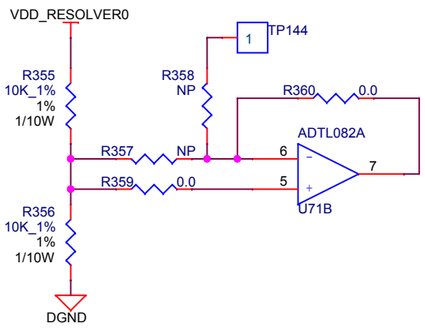
SIZE	CAGE CODE	DWG NO	REV
B	3V6D5	SCH-072004001	-

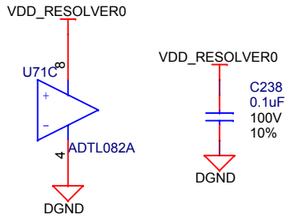
SCALE	DWN BY:	APRVD BY:	SHEET
1:1	WAS	JPW	15 OF 28

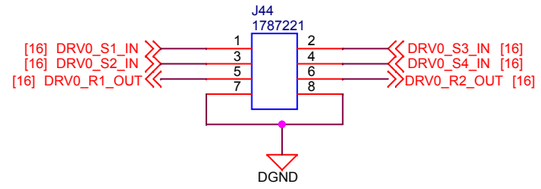


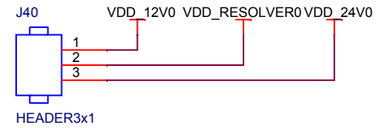












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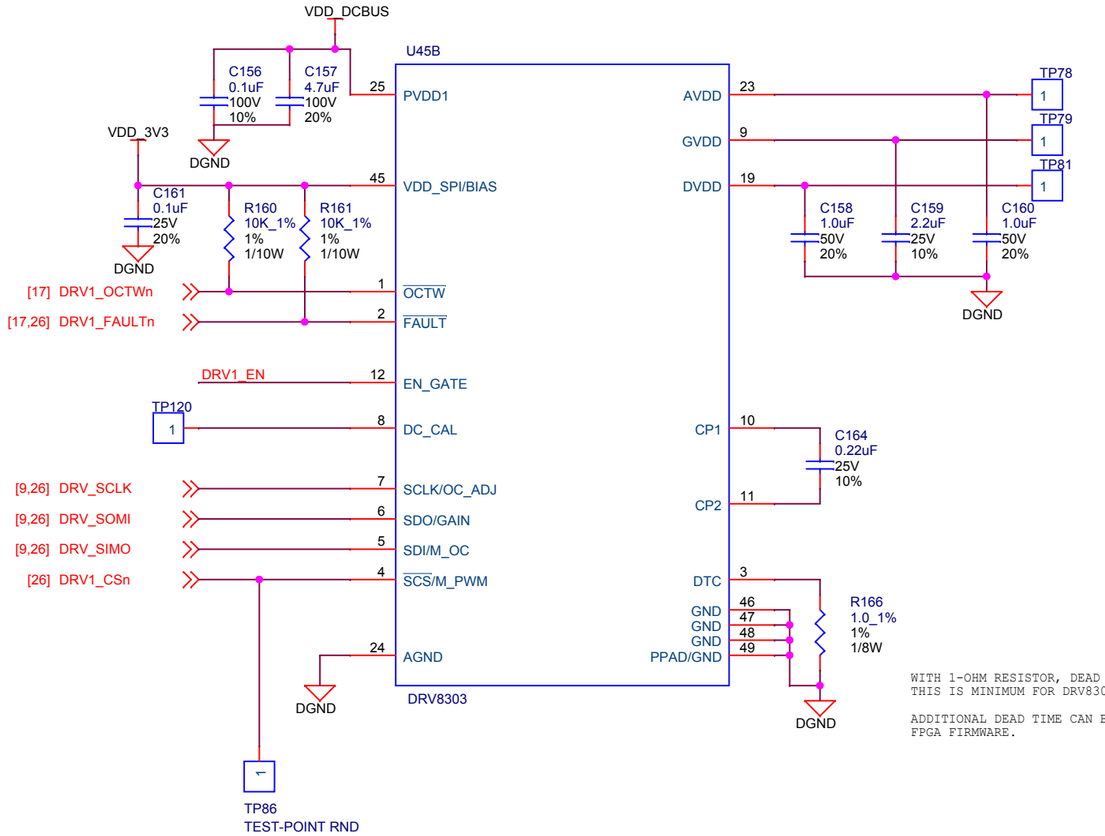
Low Voltage DC to DC and Dual Axis Motor Control Board

DRV0: Resolver, Page 2

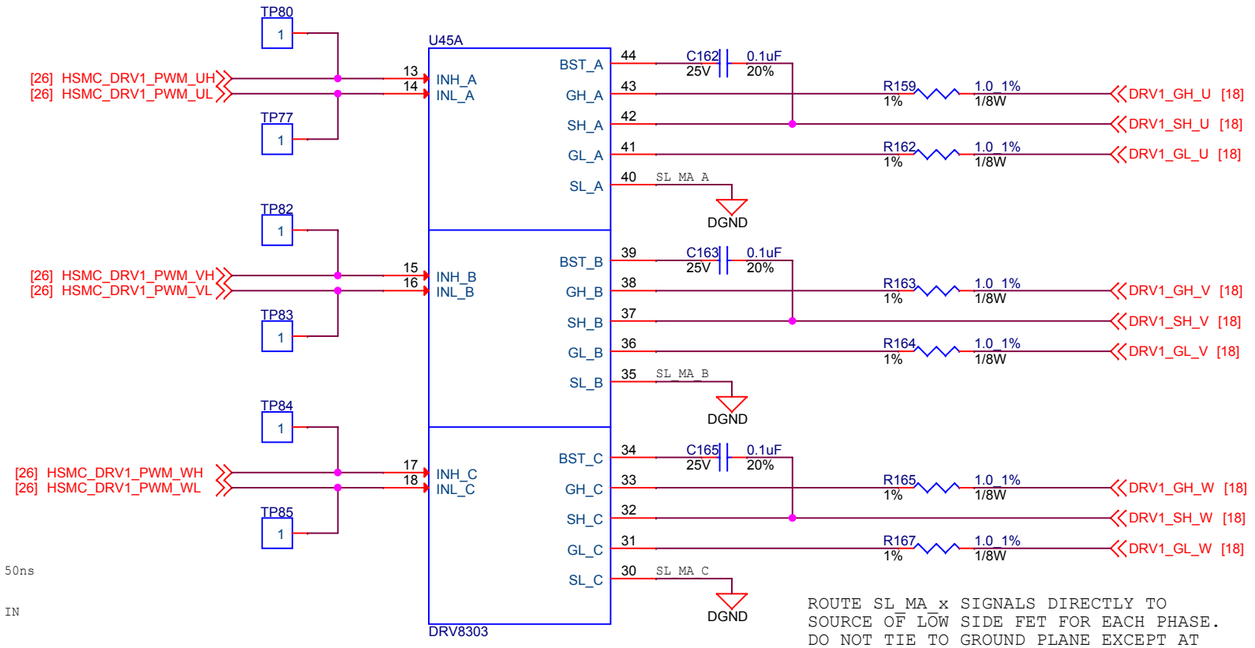
SIZE	CAGE CODE	DWG NO	REV
B	3V6D5	SCH-072004001	-

SCALE	DWN BY:	APRVD BY:	SHEET
1:1	WAS	JPW	16 OF 28

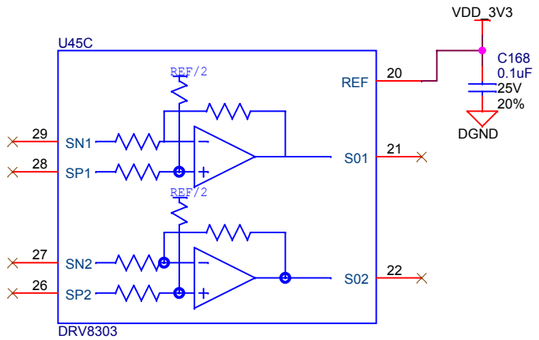


WITH 1-OHM RESISTOR, DEAD TIME IS 50ns
THIS IS MINIMUM FOR DRV8303

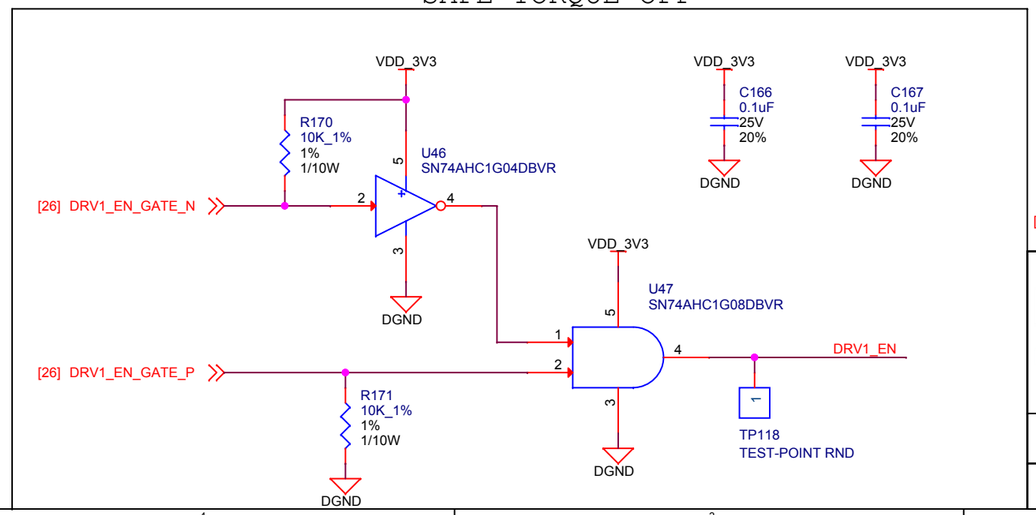
ADDITIONAL DEAD TIME CAN BE ADDED IN FPGA FIRMWARE.

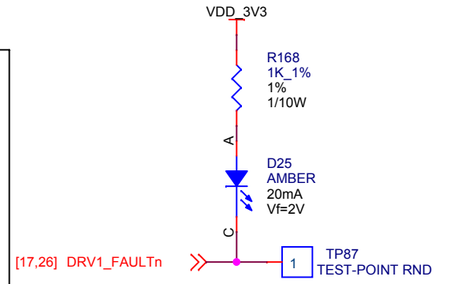


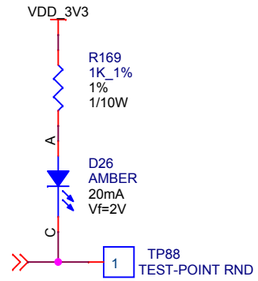
ROUTE SL_MA_x SIGNALS DIRECTLY TO SOURCE OF LOW SIDE FET FOR EACH PHASE. DO NOT TIE TO GROUND PLANE EXCEPT AT FET.



SAFE TORQUE OFF







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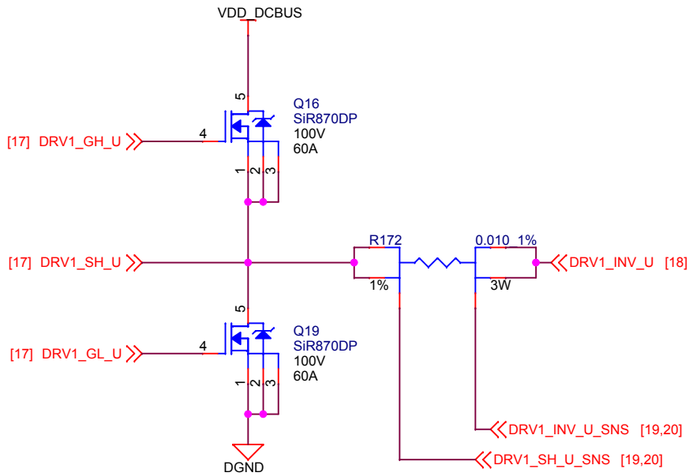
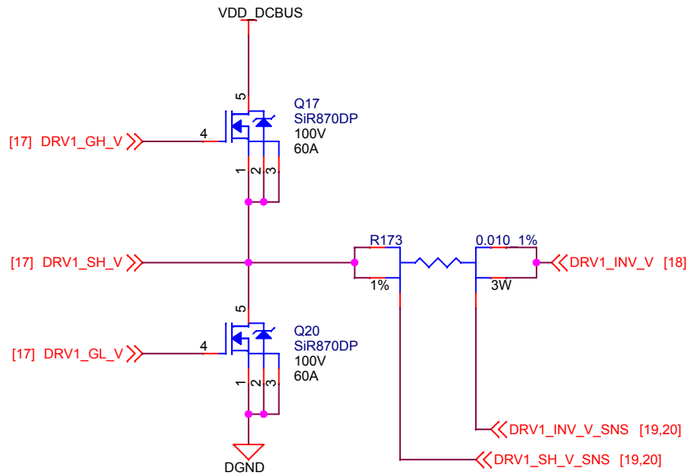
Low Voltage DC to DC and Dual Axis Motor Control Board

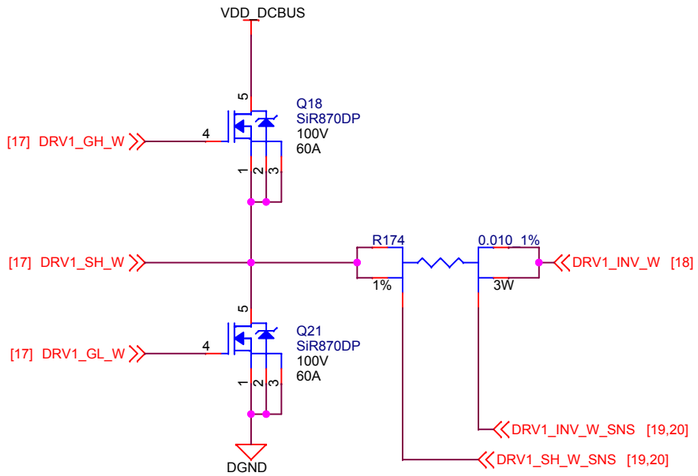
Phase 1: Inverter Gate Drivers

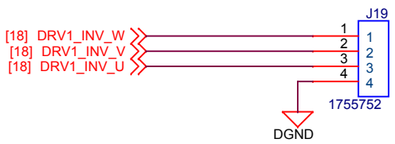
SIZE	CAGE CODE	DWG NO	REV
B	3V6D5	SCH-072004001	-

SCALE	DWN BY:	APRVD BY:	SHEET
1:1	WAS	JPW	17 OF 28









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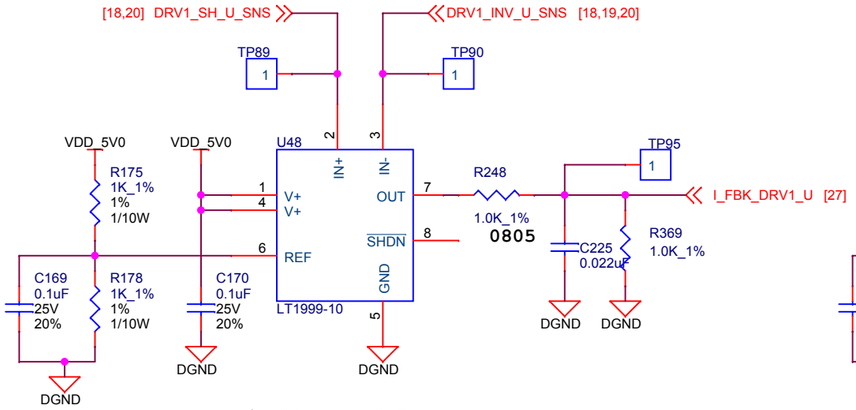
Low Voltage DC to DC and Dual Axis Motor Control Board

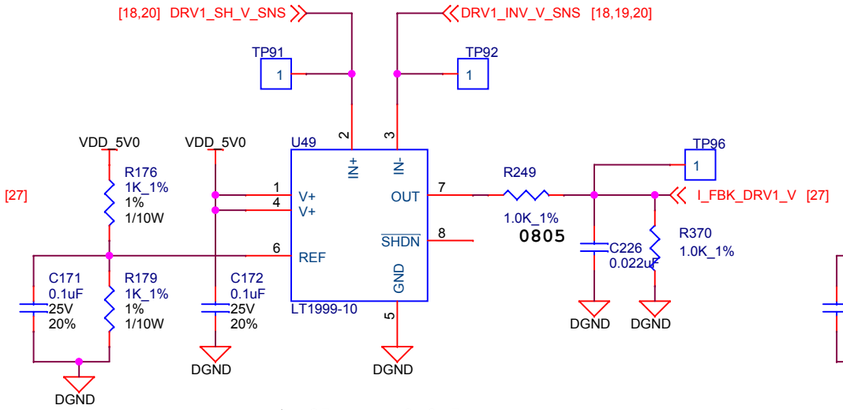
DRV0 & DRV1: Inverter FETs

SIZE	CAGE CODE	DWG NO	REV
B	3V6D5	SCH-072004001	-

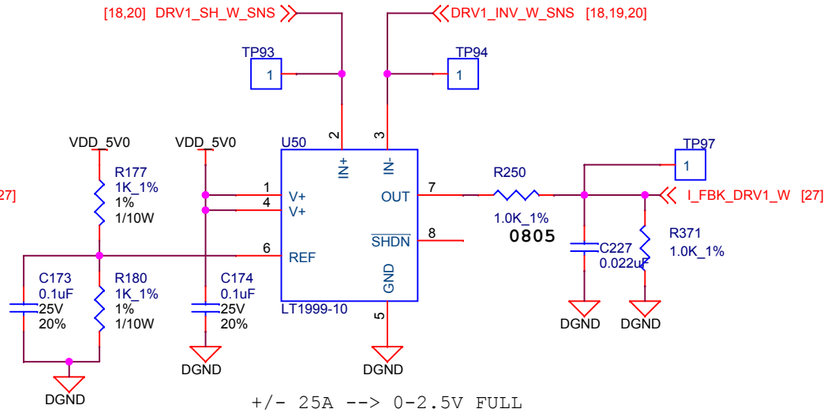
SCALE	DWN BY:	APRVD BY:	SHEET
1:1	WAS	JPW	18 OF 28



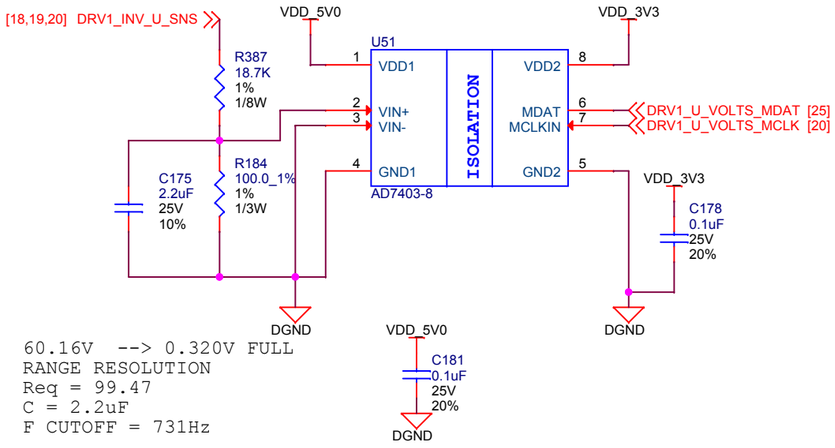
+/- 25A --> 0-2.5V FULL
RANGE RESOLUTION
Req = 0.5k
C = 22,000pF
F CUTOFF = 14 kHz



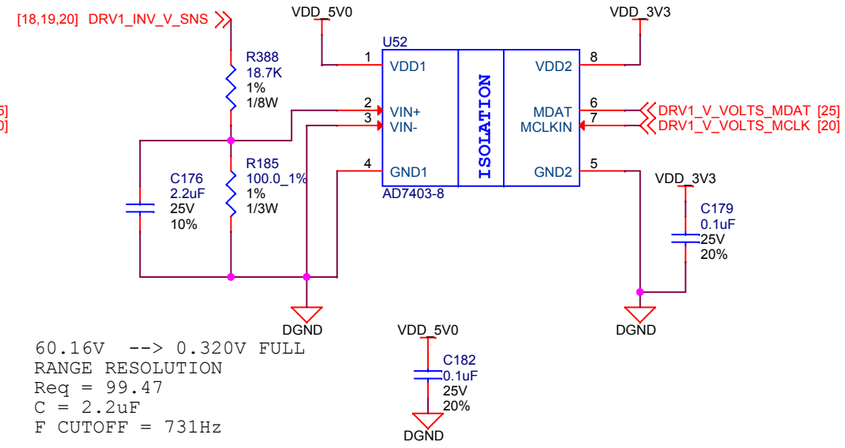
+/- 25A --> 0-2.5V FULL
RANGE RESOLUTION
Req = 0.5k
C = 22,000pF
F CUTOFF = 14 kHz



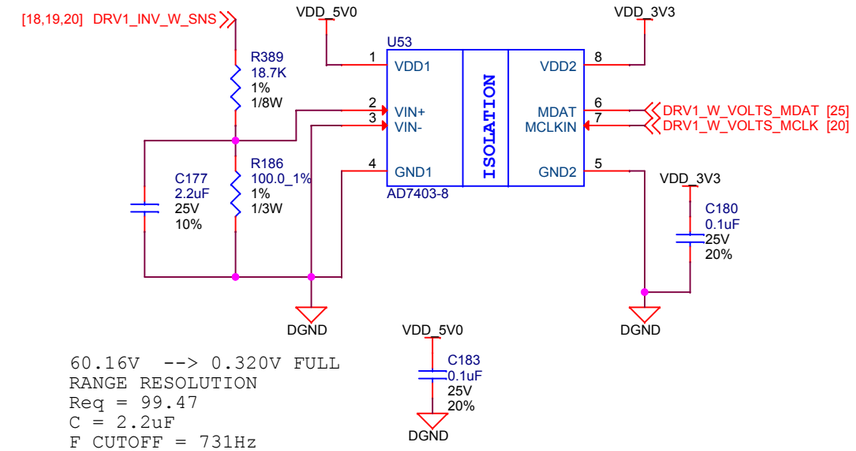
+/- 25A --> 0-2.5V FULL
RANGE RESOLUTION
Req = 0.5k
C = 22,000pF
F CUTOFF = 14 kHz



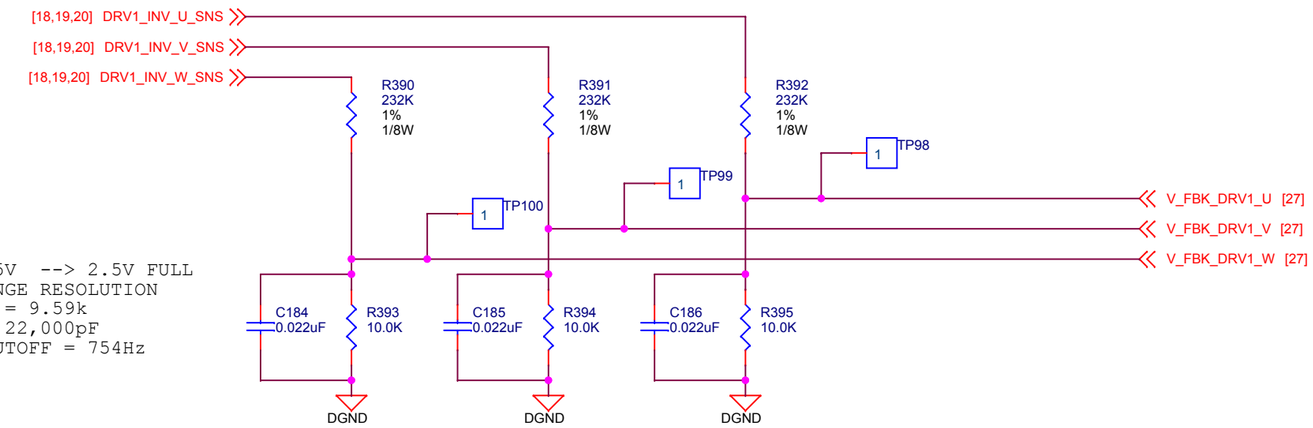
60.16V --> 0.320V FULL
RANGE RESOLUTION
Req = 99.47
C = 2.2uF
F CUTOFF = 731Hz



60.16V --> 0.320V FULL
RANGE RESOLUTION
Req = 99.47
C = 2.2uF
F CUTOFF = 731Hz



60.16V --> 0.320V FULL
RANGE RESOLUTION
Req = 99.47
C = 2.2uF
F CUTOFF = 731Hz



60.5V --> 2.5V FULL
RANGE RESOLUTION
Req = 9.59k
C = 22,000pF
F CUTOFF = 754Hz

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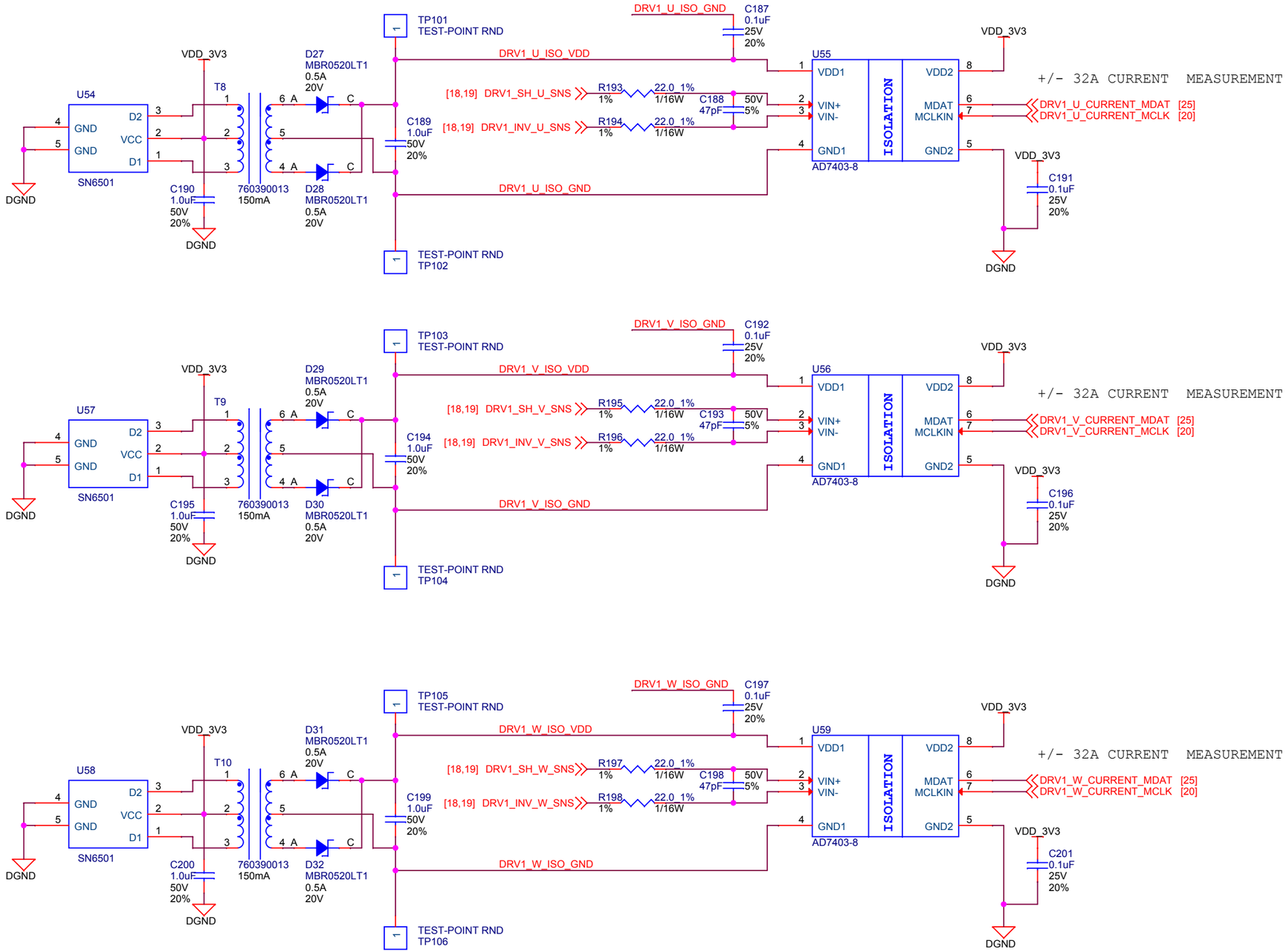
DRV1: Voltage and Current Feedback

SIZE	CAGE CODE	DWG NO	REV
B	3V6D5	SCH-072004001	-

SCALE	DWN BY:	APRVD BY:	SHEET
1:1	WAS	JPW	19 OF 28



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Low Voltage DC to DC and Dual Axis Motor Control Board

DRV1: In-Phase Current Sigma Deltas

SIZE	CAGE CODE	DWG NO	REV
B	3V6D5	SCH-072004001	-

SCALE	DWN BY:	APRVD BY:	SHEET
1:1	WAS	JPW	20 OF 28

SHIFTS SIGNALS COMING
FROM THE MOTOR FROM 5.0V
TO 2.5V

U86
VDD_IO
VCC 14
[26] DRV1_SER_RX 3 1Y
[26] DRV1_QR_A 6 2Y
[26] DRV1_QR_B 8 3Y
[26] DRV1_QR_Z 11 4Y
1A 2 DRV1_SER_DATA_RX [22]
2A 5 DRV1_QUAD_RESOLVER_A [22]
3A 9 DRV1_QUAD_RESOLVER_B [22]
4A 12 DRV1_QUAD_RESOLVER_Z [22]
1 1OE
4 2OE
10 3OE
13 4OE
GND 7
74LV4T125
DGND

VDD_IO
C281
0.1uF
50V
10%
DGND

U87
VDD_IO
VCC 14
[26] DRV1_QHR_U 3 1Y
[26] DRV1_QHR_V 6 2Y
[26] DRV1_QHR_W 8 3Y
[23] DRV1_RESOLVER_ERR_BUFF 11 4Y
1A 2 DRV1_QUAD_HALL_RESOLVER_U [22]
2A 5 DRV1_QUAD_HALL_RESOLVER_V [22]
3A 9 DRV1_QUAD_HALL_RESOLVER_W [22]
4A 12 DRV1_RESOLVER_ERR [23]
1 1OE
4 2OE
10 3OE
13 4OE
GND 7
74LV4T125
DGND

VDD_IO
C282
0.1uF
50V
10%
DGND

VDD_5V0
C207
0.1uF
50V
10%
DGND
R203
4.70K_1%
1%
1/10W

U64
VDD 14
A 12
B 11
Z 10
Y 9
NC3 1
NC1 8
NC2 13
[25] DRV1_SER_TX_EN_BUFF 3 RE
[22] DRV1_MTR_SER_DATA_RX 2 R
4 DE
[22] DRV1_MTR_SER_DATA_TX 5 D
6 GND
7 GND
LTC1687
DGND

DRV1_SER_DATA_RX_P
R205
56.0_1%
1%
1/10W
C210
2.2uF
25V
10%
DGND
R206
56.0_1%
1%
1/10W
DRV1_SER_DATA_RX_N
J20
HEADER2x1
J21
HEADER2x1
DRV1_SER_DATA_TX_N
DRV1_SER_DATA_TX_P

VDD_5V0
U62
[22] DRV1_QUAD_HALL_U 1 VCC
2 RO
3 DI
4 GND
A 8
B 7
Z 6
Y 5
ST490ABDR
R204
10K_1%
1%
1/10W
DGND
VDD_5V0
C208
0.1uF
50V
10%
DGND
DRV1_QUAD_HALL_U_P
R199
60.4_1%
1%
1/8W
C205
2.2uF
25V
10%
DGND
R201
60.4_1%
1%
1/8W
DRV1_QUAD_HALL_U_N

VDD_5V0
U65
[22] DRV1_QUAD_HALL_V 1 VCC
2 RO
3 DI
4 GND
A 8
B 7
Z 6
Y 5
ST490ABDR
R211
10K_1%
1%
1/10W
DGND
VDD_5V0
C213
0.1uF
50V
10%
DGND
DRV1_QUAD_HALL_V_P
R207
60.4_1%
1%
1/8W
C211
2.2uF
25V
10%
DGND
R209
60.4_1%
1%
1/8W
DRV1_QUAD_HALL_V_N

VDD_5V0
U67
[22] DRV1_QUAD_HALL_W 1 VCC
2 RO
3 DI
4 GND
A 8
B 7
Z 6
Y 5
ST490ABDR
R217
10K_1%
1%
1/10W
DGND
VDD_5V0
C217
0.1uF
50V
10%
DGND
DRV1_QUAD_HALL_W_P
R213
60.4_1%
1%
1/8W
C215
2.2uF
25V
10%
DGND
R215
60.4_1%
1%
1/8W
DRV1_QUAD_HALL_W_N

VDD_5V0
U63
[22] DRV1_QUAD_A 1 VCC
[22] DRV1_MTR_SER_DATA_CLK 2 RO
3 DI
4 GND
A 8
B 7
Z 6
Y 5
ST490ABDR
DGND
VDD_5V0
C209
0.1uF
50V
10%
DGND
DRV1_QUAD_A_P
R200
60.4_1%
1%
1/8W
C206
2.2uF
25V
10%
DGND
R202
60.4_1%
1%
1/8W
DRV1_QUAD_A_N
DRV1_SER_DATA_CLK_N
DRV1_SER_DATA_CLK_P

VDD_5V0
U66
[22] DRV1_QUAD_B 1 VCC
2 RO
3 DI
4 GND
A 8
B 7
Z 6
Y 5
ST490ABDR
R212
10K_1%
1%
1/10W
DGND
VDD_5V0
C214
0.1uF
50V
10%
DGND
DRV1_QUAD_B_P
R208
60.4_1%
1%
1/8W
C212
2.2uF
25V
10%
DGND
R210
60.4_1%
1%
1/8W
DRV1_QUAD_B_N

VDD_5V0
U68
[22] DRV1_QUAD_Z 1 VCC
2 RO
3 DI
4 GND
A 8
B 7
Z 6
Y 5
ST490ABDR
R218
10K_1%
1%
1/10W
DGND
VDD_5V0
C218
0.1uF
50V
10%
DGND
DRV1_QUAD_Z_P
R214
60.4_1%
1%
1/8W
C216
2.2uF
25V
10%
DGND
R216
60.4_1%
1%
1/8W
DRV1_QUAD_Z_N

VDD_24V0 VDD_5V0
VDD_12V0 VDD_3V3
J22
HEADER4x2
7 8
5 6
3 4
1 2
DEFAULT TO 5V

J23
1787289
DRV1_QUAD_HALL_U_N 3
DRV1_QUAD_HALL_V_N 5
DRV1_QUAD_HALL_W_N 7
DRV1_QUAD_A_N 9
DRV1_QUAD_B_N 11
DRV1_QUAD_Z_N 13
DRV1_SER_DATA_CLK_N 15
DRV1_SER_DATA_TX_N 17
DRV1_SER_DATA_RX_N 19
1 2 DRV1_QUAD_HALL_U_P
4 DRV1_QUAD_HALL_V_P
6 DRV1_QUAD_HALL_W_P
8 DRV1_QUAD_A_P
10 DRV1_QUAD_B_P
12 DRV1_QUAD_Z_P
14 DRV1_SER_DATA_CLK_P
16 DRV1_SER_DATA_TX_P
18 DRV1_SER_DATA_RX_P
20
DGND

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Low Voltage DC to DC and Dual Axis Motor Control Board

DRV1: Position Feedback Interface, Transceivers, & Buffers

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SIZE	CAGE CODE	DWG NO	REV
B	3V6D5	SCH-072004001	-

Monday, May 16, 2016

SCALE	DWN BY:	APRVD BY:	SHEET
1:1	WAS	JPW	21 OF 28

MOTOR DRIVE 1 FEEDBACK BANK A.

CHOOSE BETWEEN QUADRATURE A/B/Z AND RESOLVER A/B/Z. ALL SIGNALS REFERENCED TO 5V.

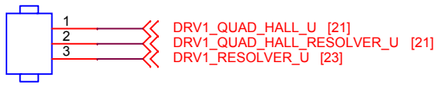
J24

HEADER3x1

MOTOR DRIVE 1 FEEDBACK BANK B.

CHOOSE BETWEEN QUADRATURE OR HALL U/V/W AND RESOLVER U/V/W. ALL SIGNALS REFERENCED TO 5V.

J25



HEADER3x1

MOTOR DRIVE 1 FEEDBACK BANK C.

CHOOSE BETWEEN MOTOR SERIAL ENCORDER AND RESOLVER SERIAL FEEDBACK. SIGNALS ARE REFERENCED TO 5V.

J26

HEADER3x1

J27

HEADER3x1

J28

HEADER3x1

J29

HEADER3x1

J30

HEADER3x1

J31

HEADER3x1

J32

HEADER3x1

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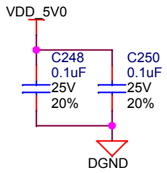
Low Voltage DC to DC and Dual Axis Motor Control Board

DRV1: Position Feedback Muxes

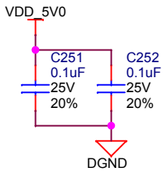
SIZE	CAGE CODE	DWG NO	REV
B	3V6D5	SCH-072004001	-

SCALE	DWN BY:	APRVD BY:	SHEET
1:1	WAS	JPW	22 OF 28

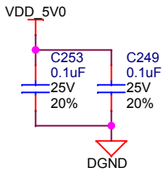
Place these caps
near VRR and RGND
pins.



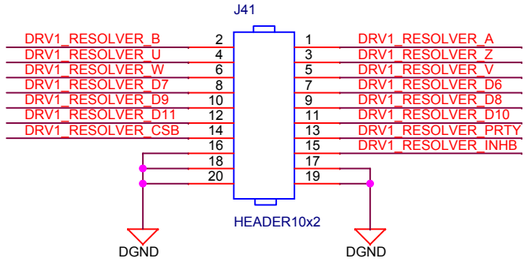
Place these caps
near VCC and AGND
pins.



Place these caps
near VDD and DGND
pins.



Test points for entire bus interface



EXMDB DCMDB, INHB and RLV have internal pull-up.

EXMDB - High - R1/R2 are excitation outputs
Low - R1/R2 are excitation inputs

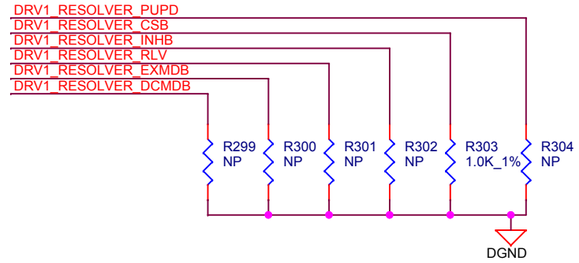
DCMDB - High - Resolver signals are AC (contain carrier)
Low - Resolver signals are DC (no carrier)

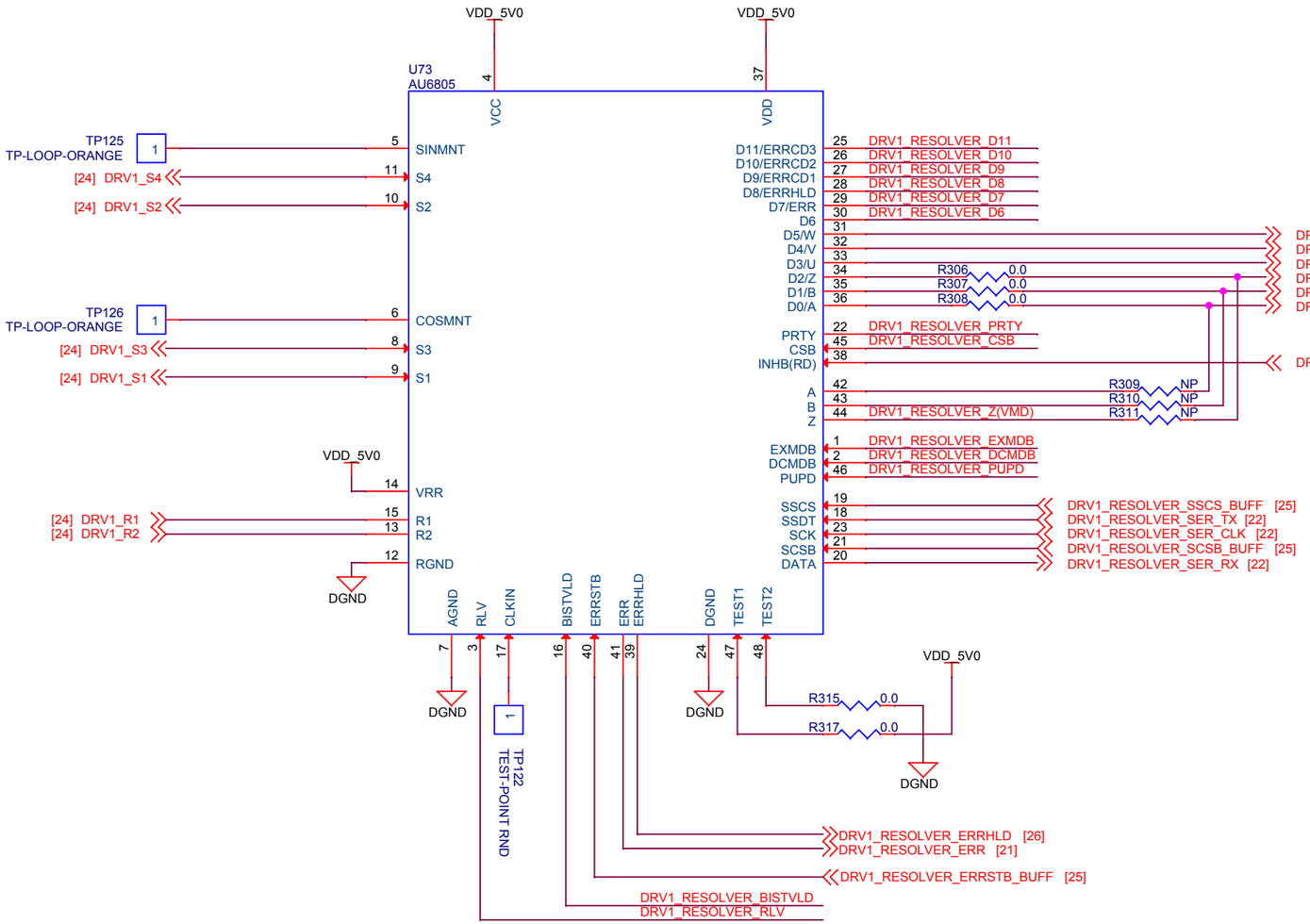
RLV - High - 10mArms excitation current
Low - 20mArms excitation current

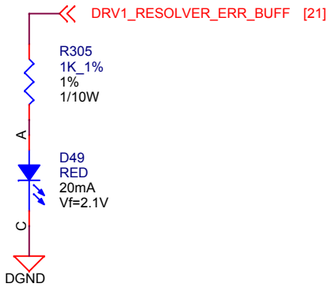
INHB - High - Allow output data to change
Low - Hold output data

CSB - High - D0~D11, PRTY High-Z
Low - D0~D11, PRTY output enable

PUPD - High - Parallel output update freq. 25MHz
Low - Parallel output update freq. 12.5MHz





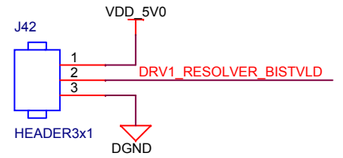


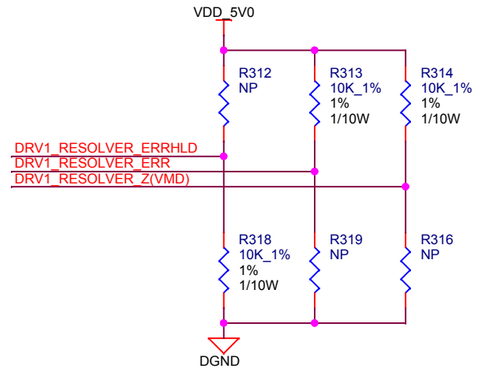
ERRHLD - High - Absolute parallel angle data
Low - Pulses equivalent to encoder

ERR - High - Internal oscillator
Low - External clk input

Z - High - Current excitation mode (VMD=0)
Low - Voltage excitation mode (VMD=1)

BISTVLD - High - Do not allow BIST to execute
Low - Allow BIST to execute





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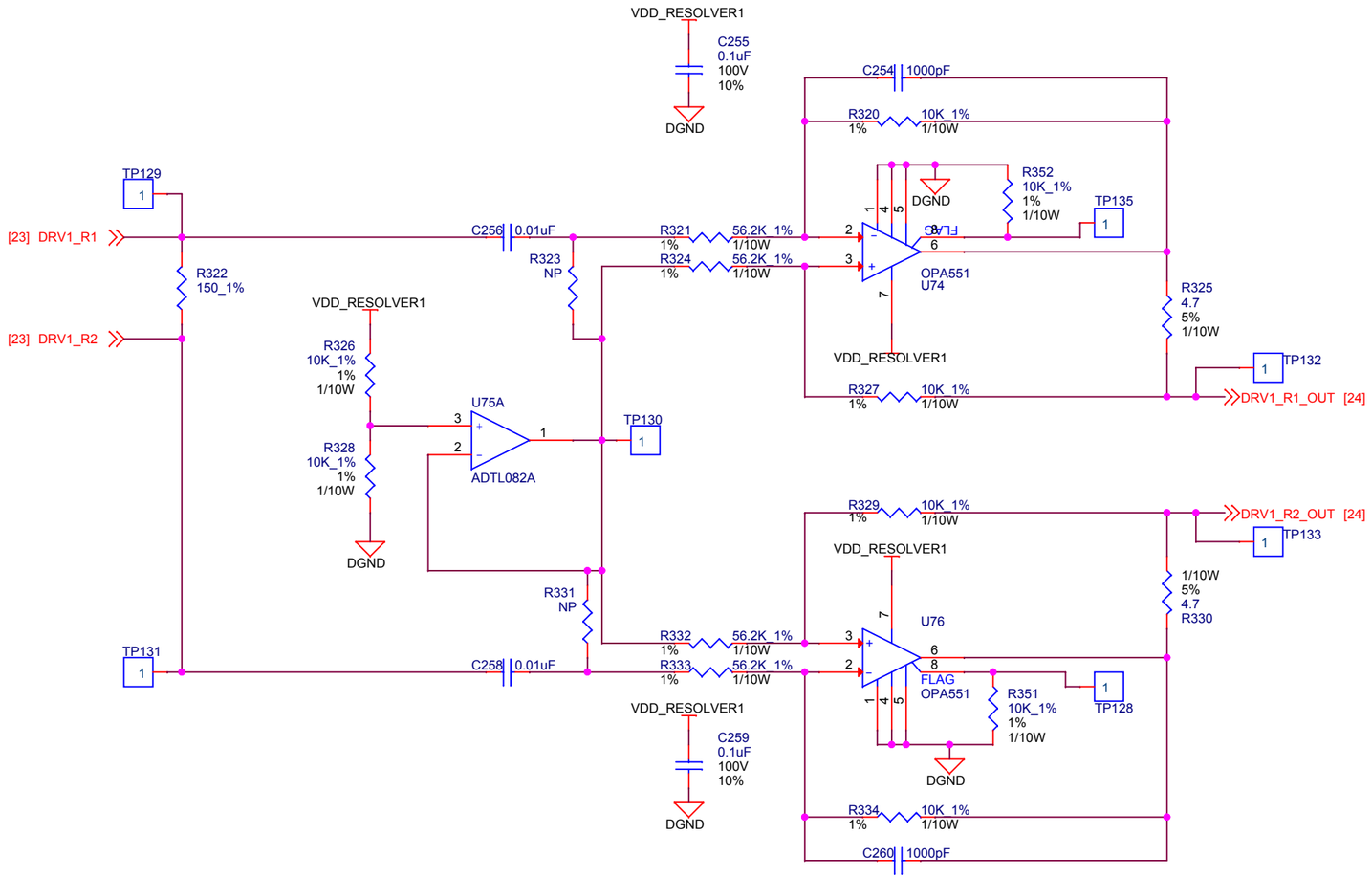
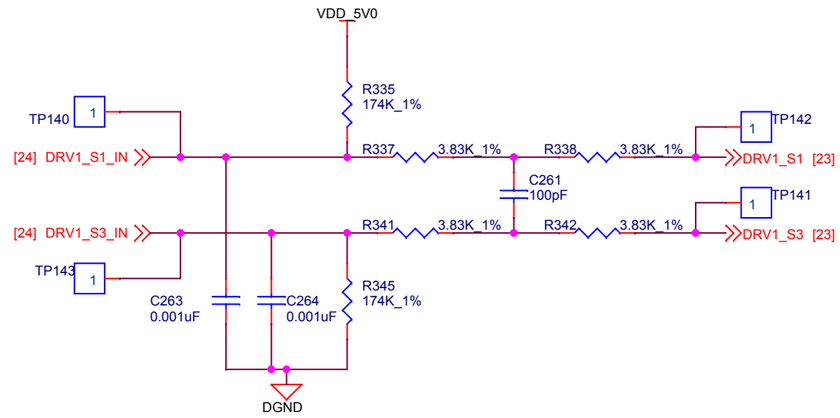
Low Voltage DC to DC and Dual Axis Motor Control Board

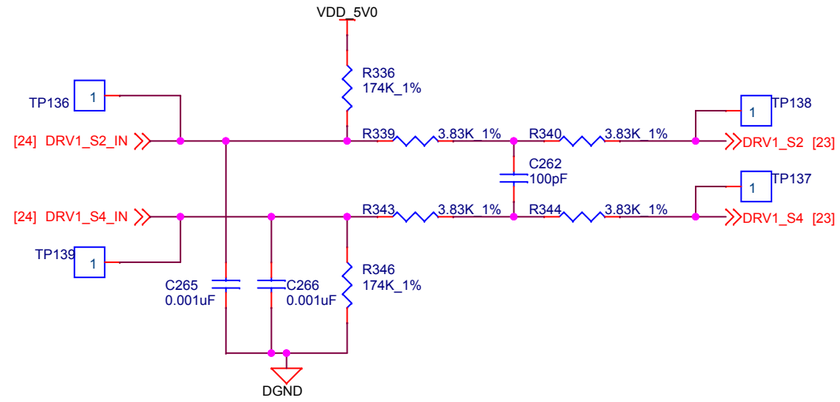
DRV1: Resolver, Page 1

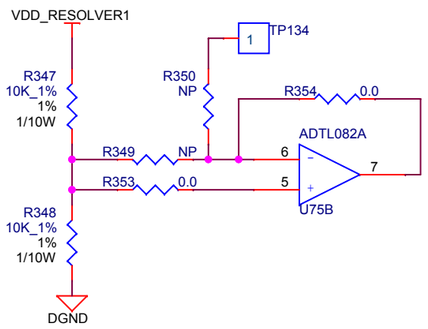
SIZE	CAGE CODE	DWG NO	REV
B	3V6D5	SCH-072004001	-

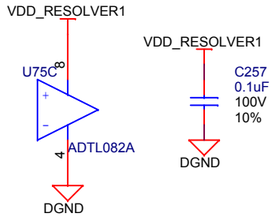
SCALE	DWN BY:	APRVD BY:	SHEET
1:1	WAS	JPW	23 OF 28

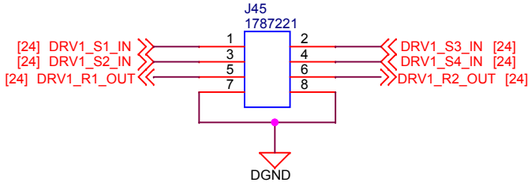


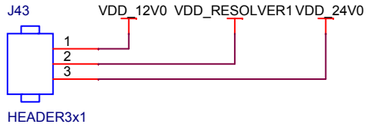












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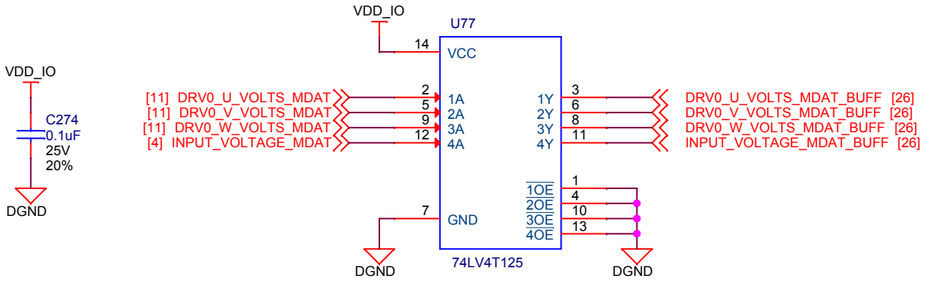
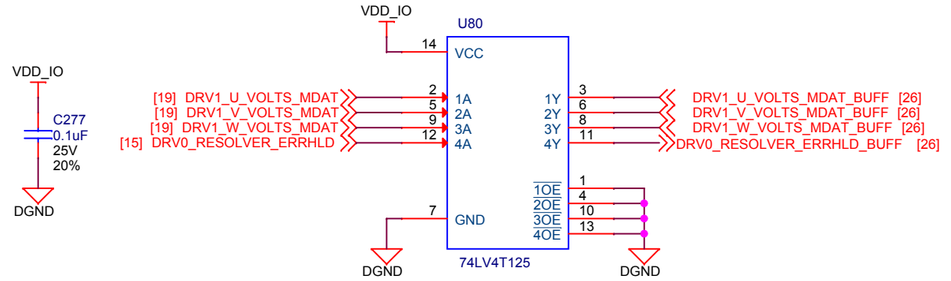
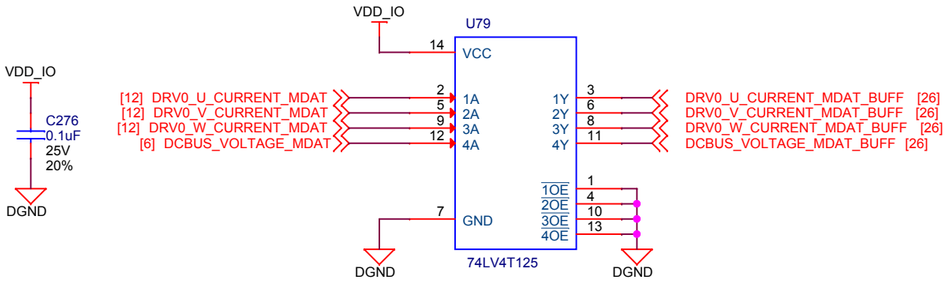
DRV1: Resolver, Page 2

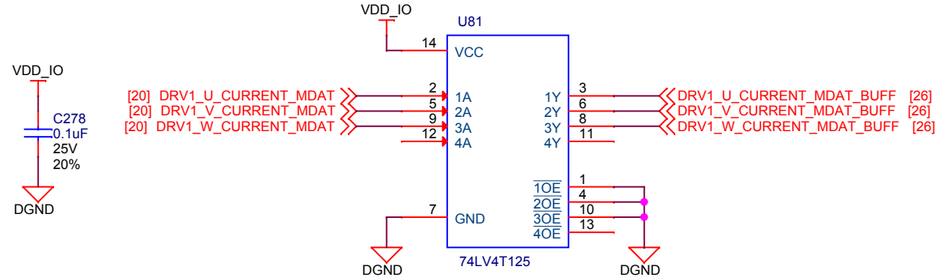
SIZE	CAGE CODE	DWG NO	REV
B	3V6D5	SCH-072004001	-

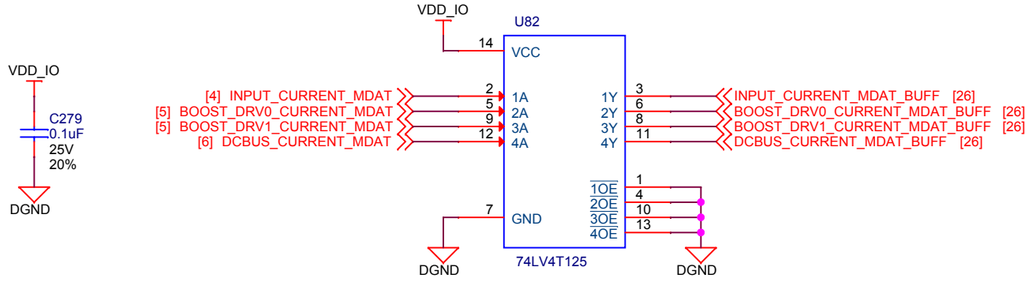
SCALE	DWN BY:	APRVD BY:	SHEET
1:1	WAS	JPW	24 OF 28

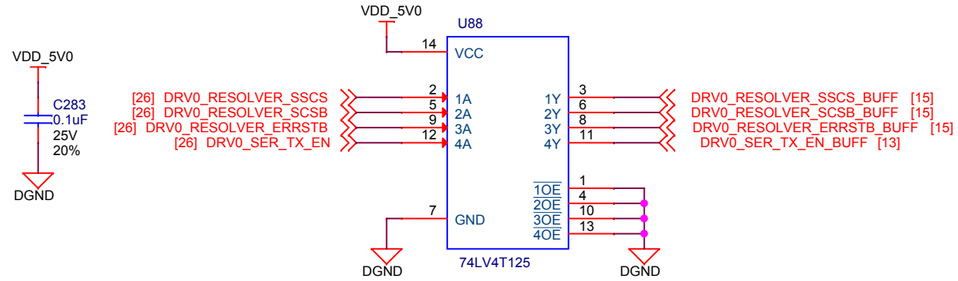


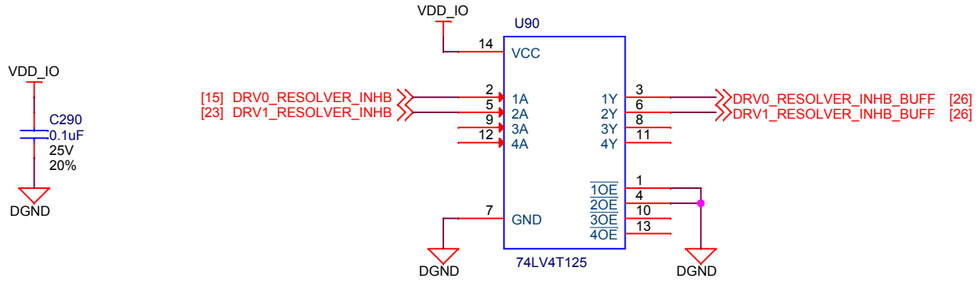


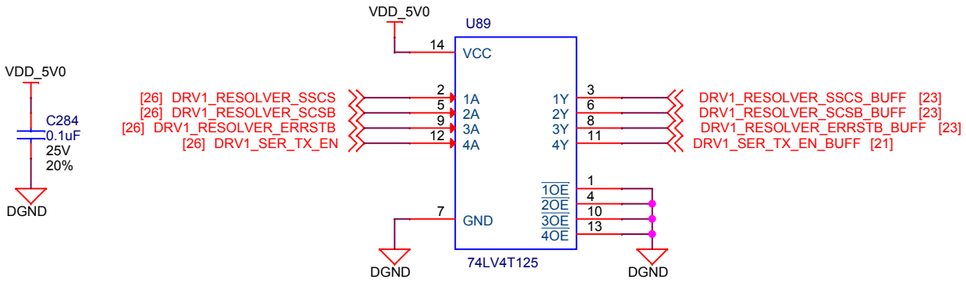












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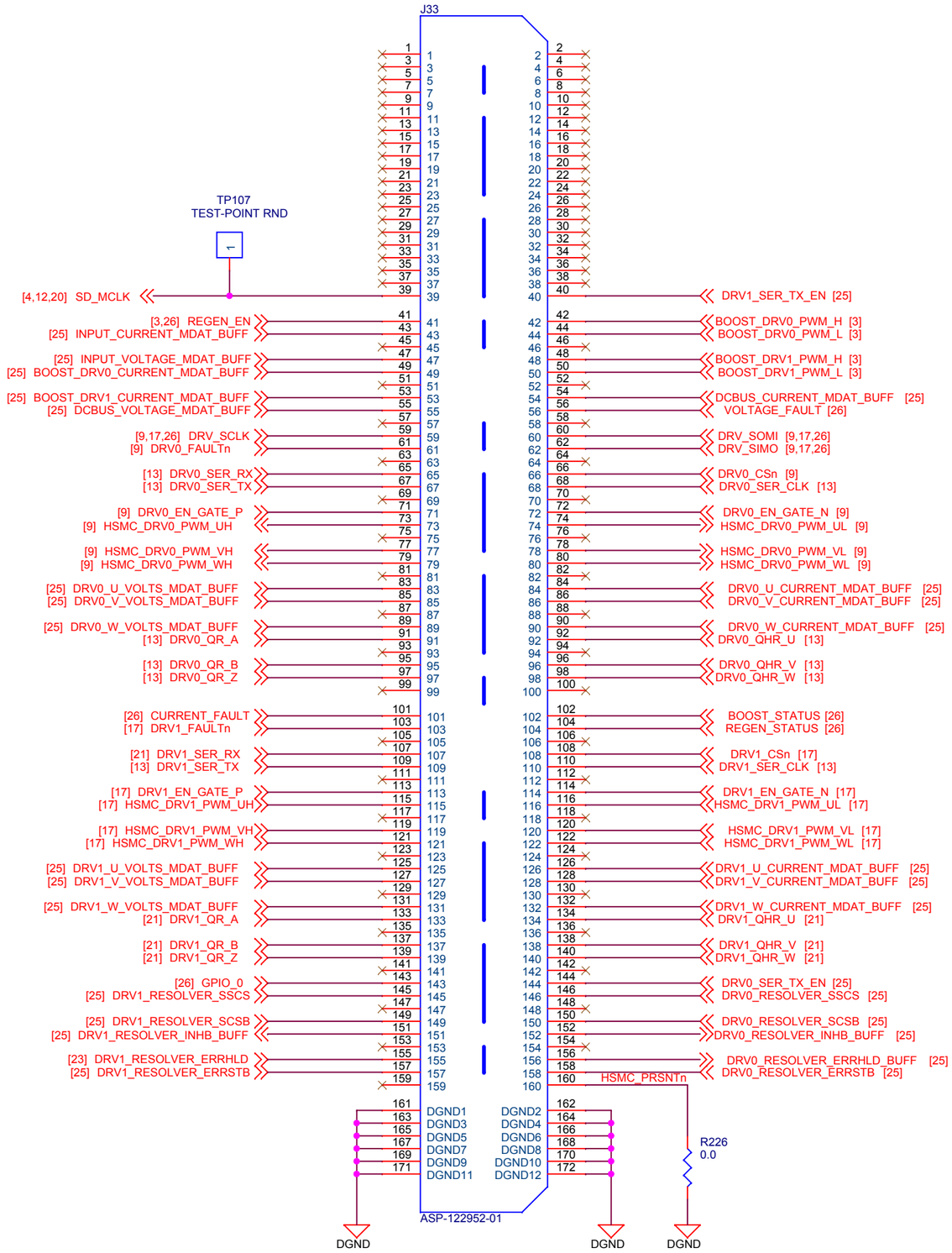
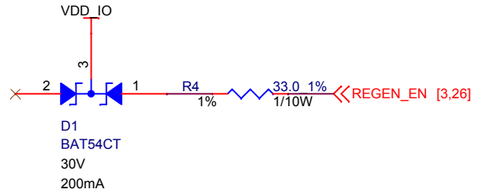
Low Voltage DC to DC and Dual Axis Motor Control Board

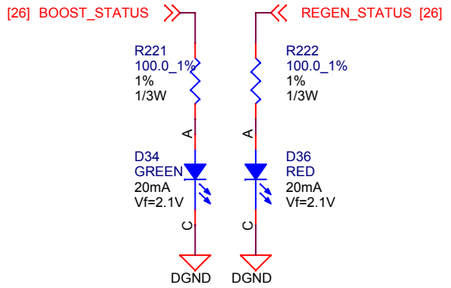
Buffers

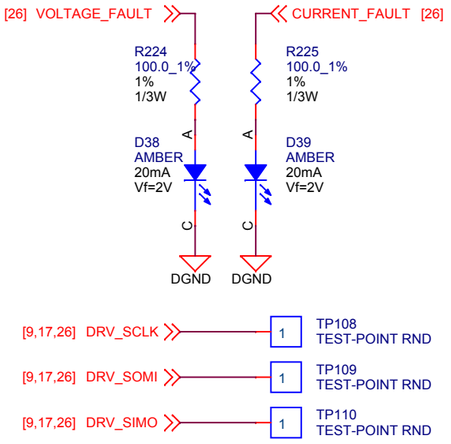
SIZE	CAGE CODE	DWG NO	REV
B	3V6D5	SCH-072004001	-

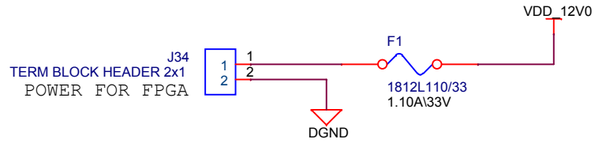
SCALE	DWN BY:	APRVD BY:	SHEET
1:1	WAS	JPW	25 OF 28

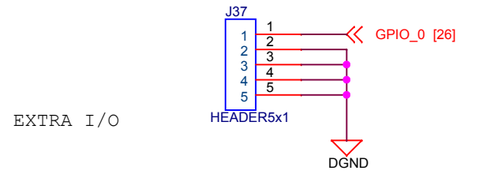












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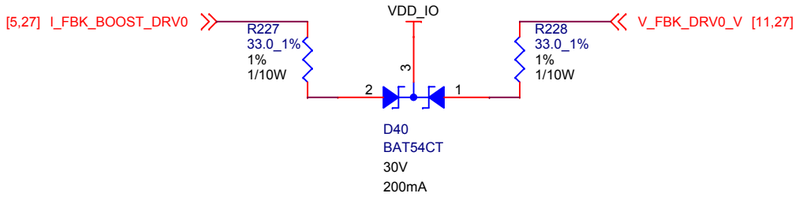
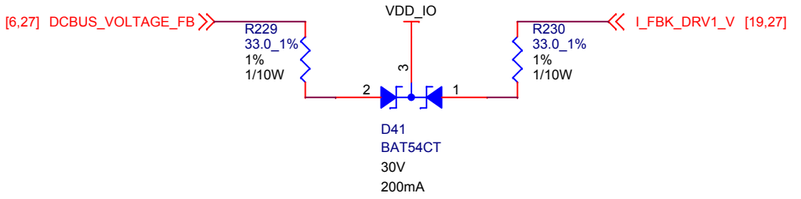
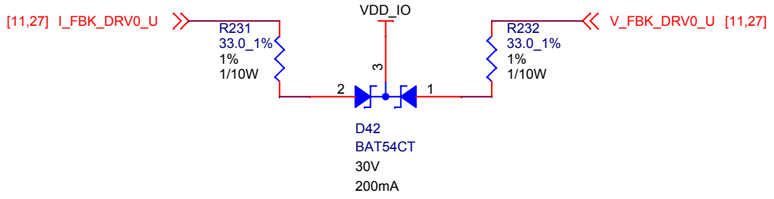
HSMC Interface

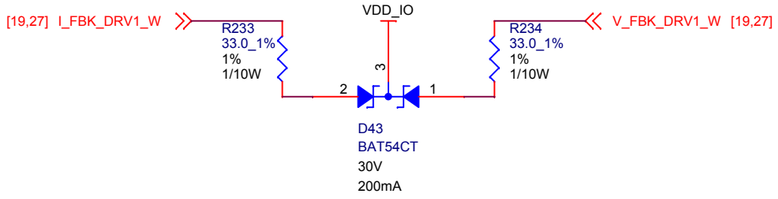
SIZE	CAGE CODE	DWG NO	REV
B	3V6D5	SCH-072004001	-

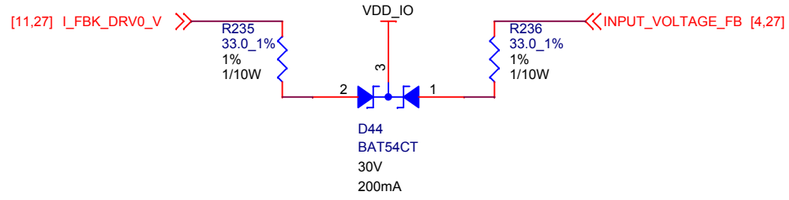
SCALE	DWN BY:	APRVD BY:	SHEET
1:1	WAS	JPW	26 OF 28

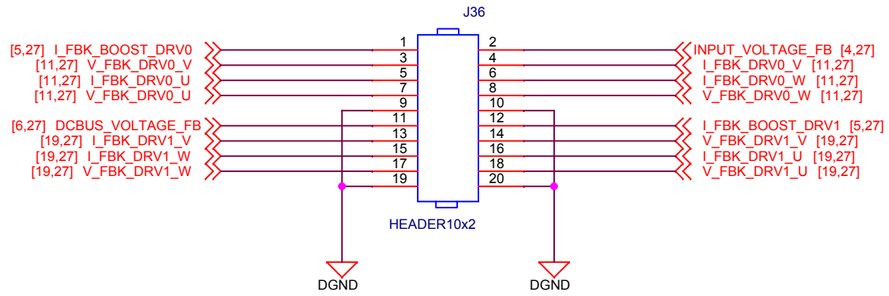


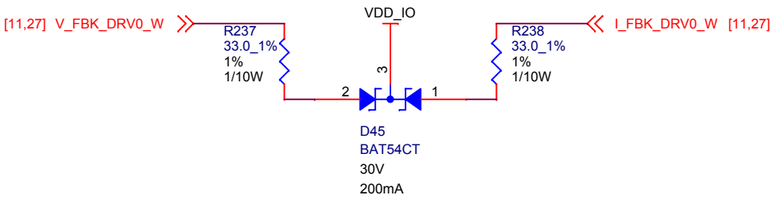


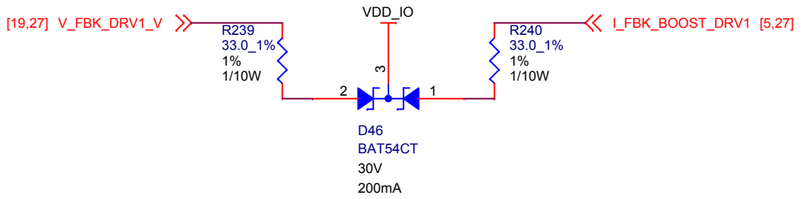


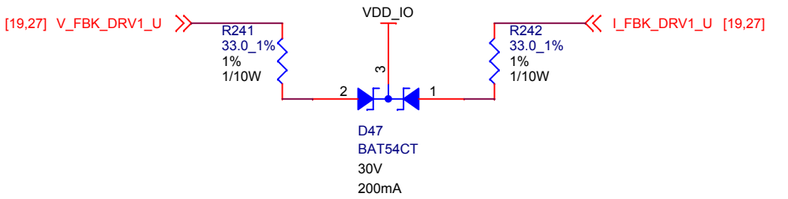












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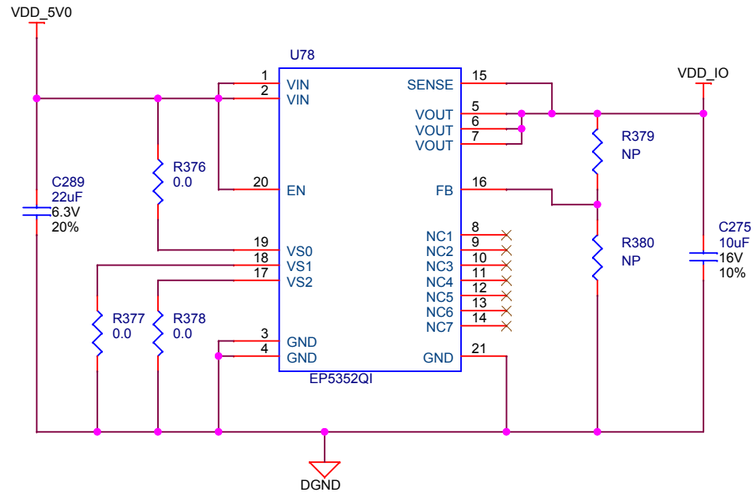
Low Voltage DC to DC and Dual Axis Motor Control Board

MAX10 Analog Connections

SIZE	CAGE CODE	DWG NO	REV
B	3V6D5	SCH-072004001	-

SCALE	DWN BY:	APRVD BY:	SHEET
1:1	WAS	JPW	27 OF 28

VS2	VS1	VS0	VOUT
0	0	0	3.3
0	0	1	2.5
0	1	0	2.8
0	1	1	1.2
1	0	0	3.0
1	0	1	1.8
1	1	0	2.7
1	1	1	EXT



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2V5 Supply

SIZE	CAGE CODE	DWG NO	REV
B	3V6D5	SCH-072004001	-

SCALE	DWN BY:	APRVD BY:	SHEET
1:1	WAS	JPW	28 OF 28