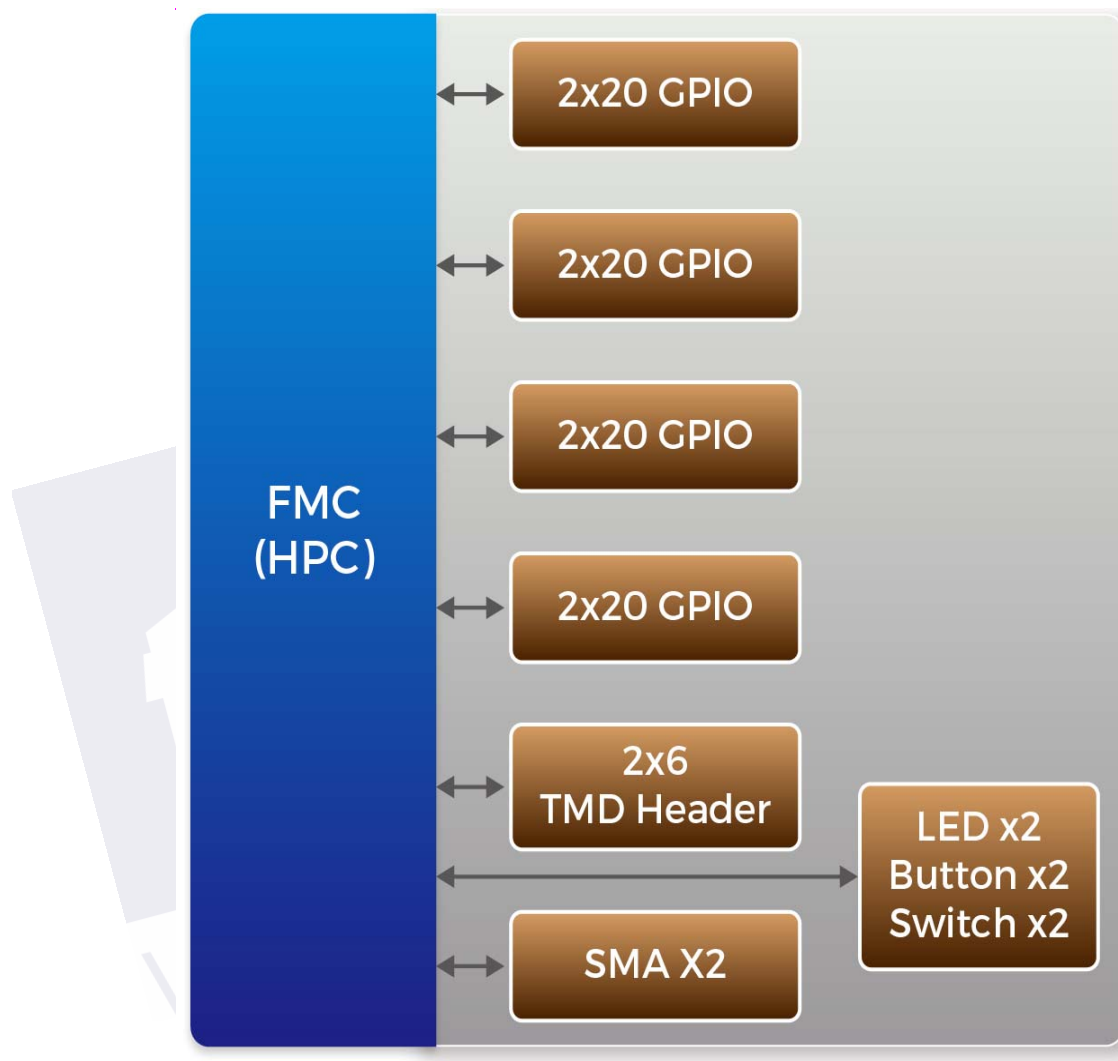
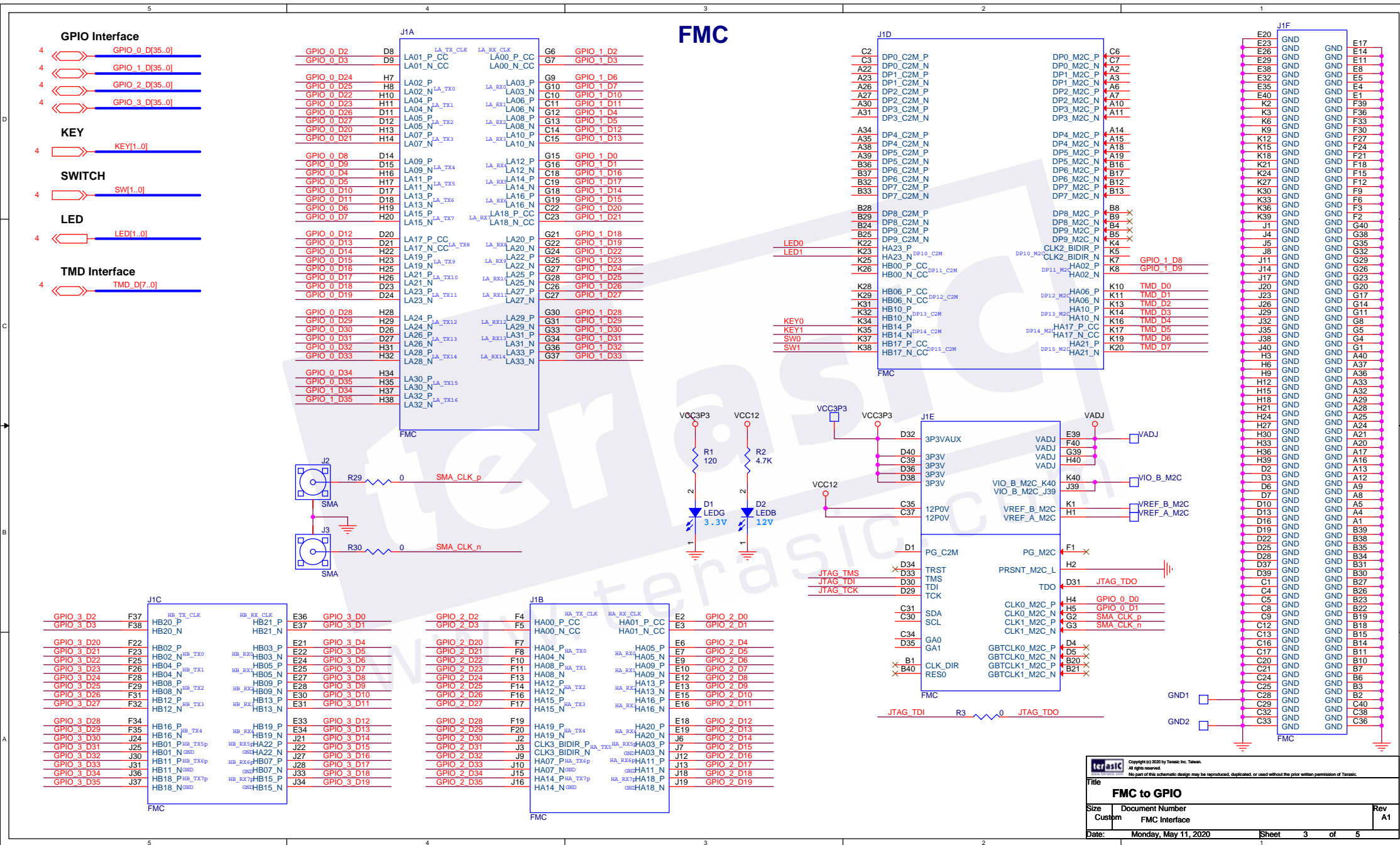


## FMC (HPC) to Terasic GPIO

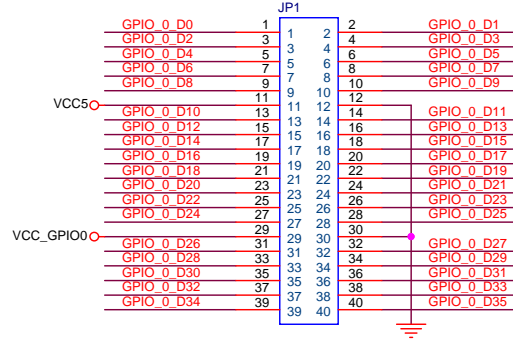
SCHEMATIC	CONTENT	PAGE
01 - Cover Page	Cover Page	01
02 - Block Diagram	Block Diagram	02
03 - FMC	FMC (FPGA Mezzanine Card) Interface	03
04 - GPIO	GPIO Interface	04
05 - Power	5V power	05

# Block Diagram

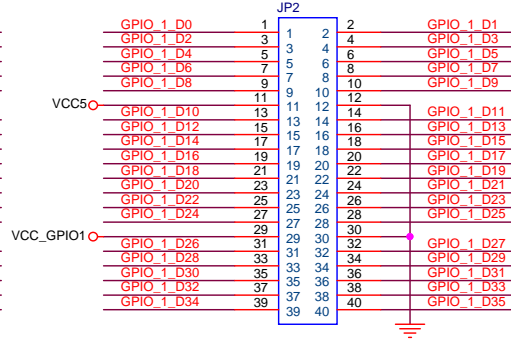




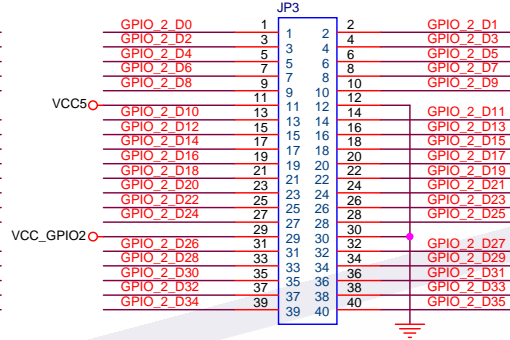
### GPIO 0 Header



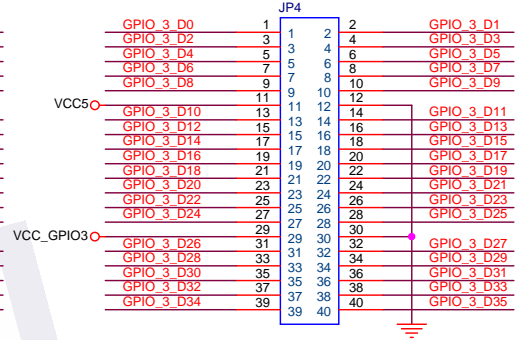
### GPIO 1 Header



### GPIO 2 Header



### GPIO 3 Header



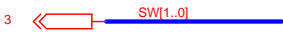
### GPIO Interface



### KEY



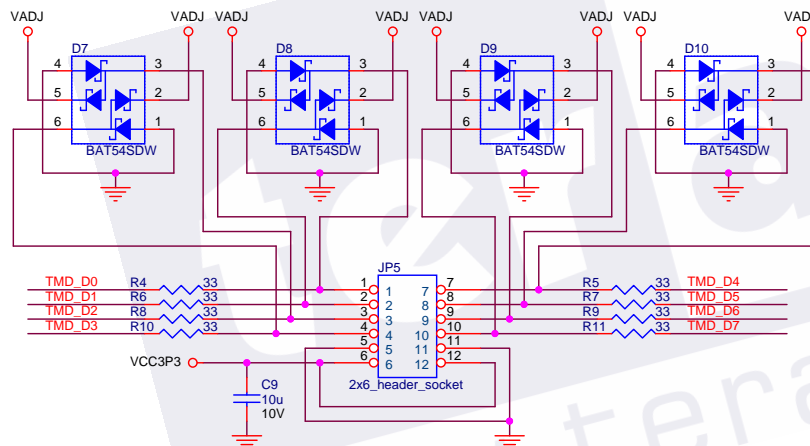
### SWITCH



### LED

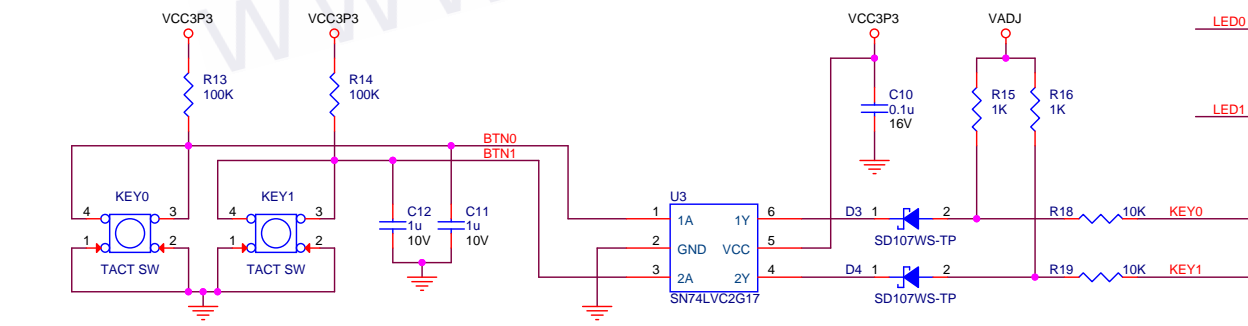
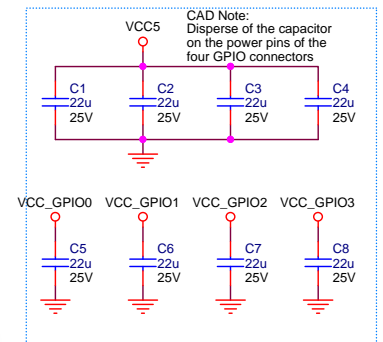
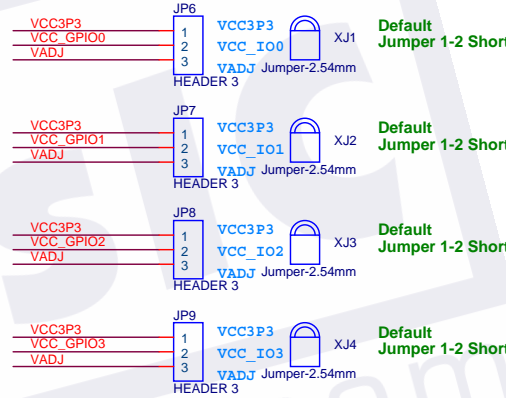


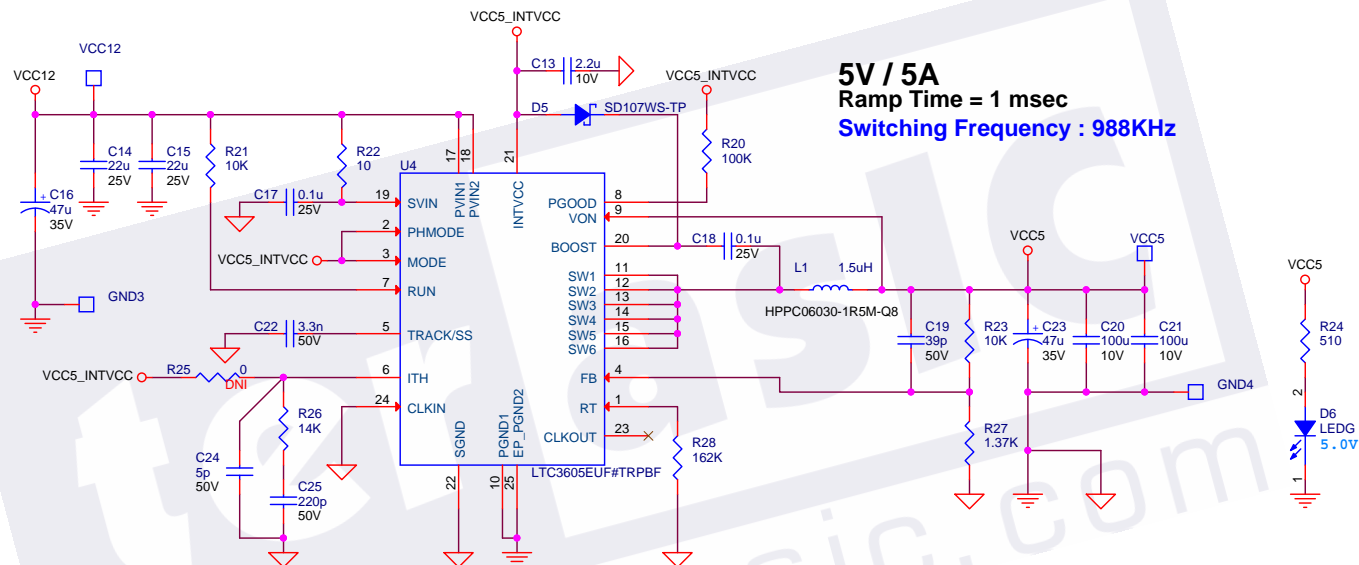
### TMD Interface



### JP6 / JP7 / JP8 / JP9 VCC\_GPIO Power Path Select

Jumper Setting	Power Path Select
Open	No Select, No Power
1-2 short	VCC_GPIO = 3.3V
2-3 short	VCC_GPIO = VADJ





PCB1  
 PCB

MH1 MH2 MH3 MH4 FID1 FID2 FID3 FID4 FID5 FID6 FID7

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