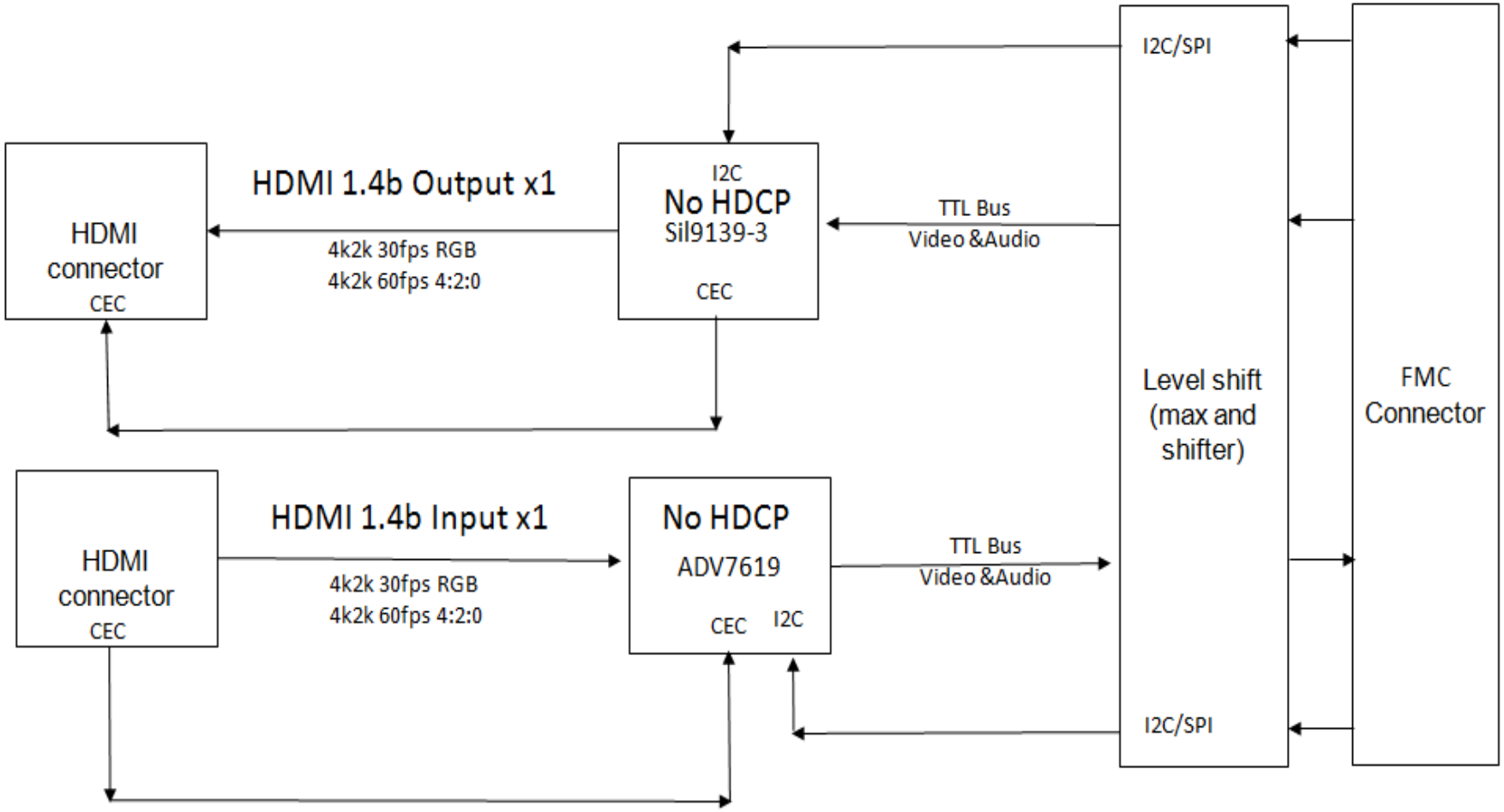
HDMI-FMC

SCHEMATIC	*CONTENT*	*PAGE*
TOP	Cover Page, Block Diagram	01 ~ 02
FMC	FMC Interface	03
HDMI TX	SiI9136-3	04
HDMI RX	ADV7619	05
Level Shift	MAX10 System	06 ~ 09
Power	Power System	10

Title: HDMI-FMC		
Size: B	Document Number: COVER	Rev: C1
Date: Wednesday, October 05, 2022	Sheet 1 of 10	

Block Diagram



Title: HDMI-FMC		
Size: B	Document Number: Block Diagram	Rev: C1
Date: Wednesday, October 05, 2022	Sheet 2 of 10	

To MAX10 Input

SII9136_INT 4
SII9136_RST_N 4
TX_DSR3R 4
TX_DSR3L 4

iTX_DE 6 — TX_DE
iTX_HS 6 — TX_HS
iTX_VS 6 — TX_VS
iTX_PCLK 8 — TX_PCLK
iTX_BD[11..0] 6 — TX_BD[11..0]
iTX_GD[11..0] 6 — TX_GD[11..0]
iTX_RD[11..0] 6 — TX_RD[11..0]
iTX_I2S[3..0] 6 — TX_I2S[3..0]
iTX_MCLK 6 — TX_MCLK
iTX_WS 6 — TX_WS
iTX_SPDIF 6 — TX_SPDIF
iTX_SCK 6 — TX_SCK

VCC3P3 VCCADJ
R46 200K, R39 4.7K, R40 4.7K, C57 0.1u, C58 0.1u, R42 4.7K, R41 4.7K
U8 PCA9306 (EN, Vref_B, Vref_A, B1, B2, A1, A2, GND)
SII9136_CSCL_4 SII9136_CSDA_4 SII9136_CSCL_FMC SII9136_CSDA_FMC

ADV7619_INT 5
ADV7619_RESET_N 5
ADV7619_CS_N 5
ADV7619_CSCL 5
ADV7619_CSDA 5

From MAX10 Output

oRX_BD[15..0] 6 — RX_BD[15..0]
oRX_GD[15..0] 6 — RX_GD[15..0]
oRX_RD[15..0] 6 — RX_RD[15..0]
oRX_DE 6 — RX_DE
oRX_HS 6 — RX_HS
oRX_VS 6 — RX_VS
oRX_PCLK 8 — RX_PCLK

RX_API5..0] 5
RX_SCLK 5
RX_MCLK 5
RX0_DDC_SCL 5
RX0_DDC_SDA 5
RX1_DDC_SCL 5
RX1_DDC_SDA 5

VCC3P3 R99 120 POWER1 LEDG

J1A — FMC_Vita57_1_HPC

TX_PCLK D8 — SII9136_RST_N D9
TX_SCK H7
TX_WS H8
TX_I2S1 H10
TX_GD2 H11
TX_BD10 D11
TX_BD4 D12
TX_GD0 H13
TX_BD11 H14
TX_BD7 D14
TX_MCLK D15
TX_BD1 H16
TX_VS H17
TX_BD0 D17
SII9136_INT D18
TX_DE H19
TX_RD7 H20
TX_RD6 D20
TX_RD4 D21
TX_RD0 H22
TX_GD10 H23
TX_DSR3L H25
TX_DSR3R H26
TX_RD1 D23
TX_GD9 D24
TX_GD5 H28
TX_GD6 D27
TX_SPDIF H31
TX_I2S3 H32
TX_I2S2 H34
TX_RD11 H35
TX_RD10 H37
TX_RD9 H38

G6 RX_PCLK — G7 for different clock input OCT only
G9 ADV7619_CS_N
G10 TX_GD3
C10 TX_I2S0
C11 TX_BD5
G12 TX_GD1
G13 ADV7619_RESET_N
C14 TX_BD8
C15 TX_BD9
G15 TX_BD3
G16 TX_BD2
C18 TX_BD6
C19 TX_HS
G18 RX_BD6
G19 RX_BD4
C22 TX_RD3
C23 TX_RD2
G21 TX_RD5
G22 TX_GD11
G24 ADV7619_INT
G25 TX_GD8
G27 TX_GD4
G28 RX_RD9
C26 TX_RD8
C27 TX_GD7
G30 RX_GD11
G31 RX_GD12
G33 RX1_DDC_SCL
G34 RX1_DDC_SDA
G36 RX_RD3
G37 RX_RD6

JTAG Interface

FMC_JTAG_TCK 8
FMC_JTAG_TMS 8
FMC_JTAG_TDI 8
FMC_JTAG_TDO 8

VCC12: C176 10u 25V, C174 0.1u, C175 0.1u
VCC3P3: C177 10u, C178 0.1u, C179 0.1u
VCCADJ: C171 10u, C173 0.1u, C172 0.1u

J1E — FMC_Vita57_1_HPC

VCC3P3 — D32 3P3VAUX; D40 3P3V; C39 3P3V; D36 3P3V; D38 3P3V; 3P3V
VCC12 — C35 12P0V; C37 12P0V
VCCADJ — E39 VADJ; F40 VADJ; G39 VADJ; H40 VADJ
K40 VIO_B_M2C; J39 VIO_B_M2C
K1 VREF_B_M2C; H1 VREF_A_M2C
D1 PG_C2M — F1 PG_M2C
H2 PRSNT_M2C_L — R147 0 — D31 FMC_JTAG_TDO
D34 TRST; D33 TMS; D30 TDI; D29 TCK — TDO
C31 SDA; C30 SCL — CLK0_M2C_P H5; CLK0_M2C_N G2; CLK1_M2C_P G3; CLK1_M2C_N
C34 GA0; D35 GA1 — D4; D5; B20 GBTCLK0_M2C_N; B21 GBTCLK1_M2C_P
B1 CLK_DIR; B40 RES0 — GBTCLK0_M2C_P; GBTCLK1_M2C_N

VCC3P3 R108 10K — FMC_JTAG_TRST, FMC_JTAG_TMS, FMC_JTAG_TDI, FMC_JTAG_TCK
FMC_JTAG_TDI R101 0 FMC_JTAG_TDO

J1F — FMC_Vita57_1_HPC

VCCADJ C187 0.1u U15 R148 4.7K R138 4.7K
VCC3P3 R139 200K R149 4.7K R150 4.7K C188 0.1u
PCA9306 (GND, EN, Vref_A, Vref_B, A1, A2, B1, B2)
ADV7619_CSCL_FMC ADV7619_CSDA_FMC — FPGA side
ADV7619_CSCL ADV7619_CSDA

J1D — FMC_Vita57_1_HPC

C2 DP0_C2M_P; C3 DP0_C2M_N; A22 DP1_C2M_P; A23 DP1_C2M_N; A26 DP2_C2M_P; A27 DP2_C2M_N; A30 DP3_C2M_P; A31 DP3_C2M_N
A34 DP4_C2M_P; A35 DP4_C2M_N; A38 DP5_C2M_P; A39 DP5_C2M_N; B36 DP6_C2M_P; B37 DP6_C2M_N; B32 DP7_C2M_P; B33 DP7_C2M_N
B28 DP8_C2M_P; B29 DP8_C2M_N; B24 DP9_C2M_P; B25 DP9_C2M_N
K23 HA23_P; K25 HA23_N; K26 HB00_P_CC; K28 HB06_P_CC; K29 HB06_N_CC; K31 HB10_P; K32 HB10_N; K34 HB14_P; K35 HB14_N; K37 HB17_P_CC; K38 HB17_N_CC

DP0_M2C_P C6; DP0_M2C_N C7; DP1_M2C_P A2; DP1_M2C_N A3; DP2_M2C_P A6; DP2_M2C_N A7; DP3_M2C_P A10; DP3_M2C_N A11
DP4_M2C_P A14; DP4_M2C_N A15; DP5_M2C_P A18; DP5_M2C_N A19; DP6_M2C_P B16; DP6_M2C_N B17; DP7_M2C_P B12; DP7_M2C_N B13
DP8_M2C_P B8; DP8_M2C_N B9; DP9_M2C_P B4; DP9_M2C_N B5
CLK2_BIDIR_P K4; CLK2_BIDIR_N K5; HA02_P K7; HA02_N K8
HA06_P K10; HA06_N K11; HA10_P K13; HA10_N K14; HA17_P_CC K16; HA17_N_CC K17; HA21_P K19; HA21_N K20

J1B — FMC_Vita57_1_HPC

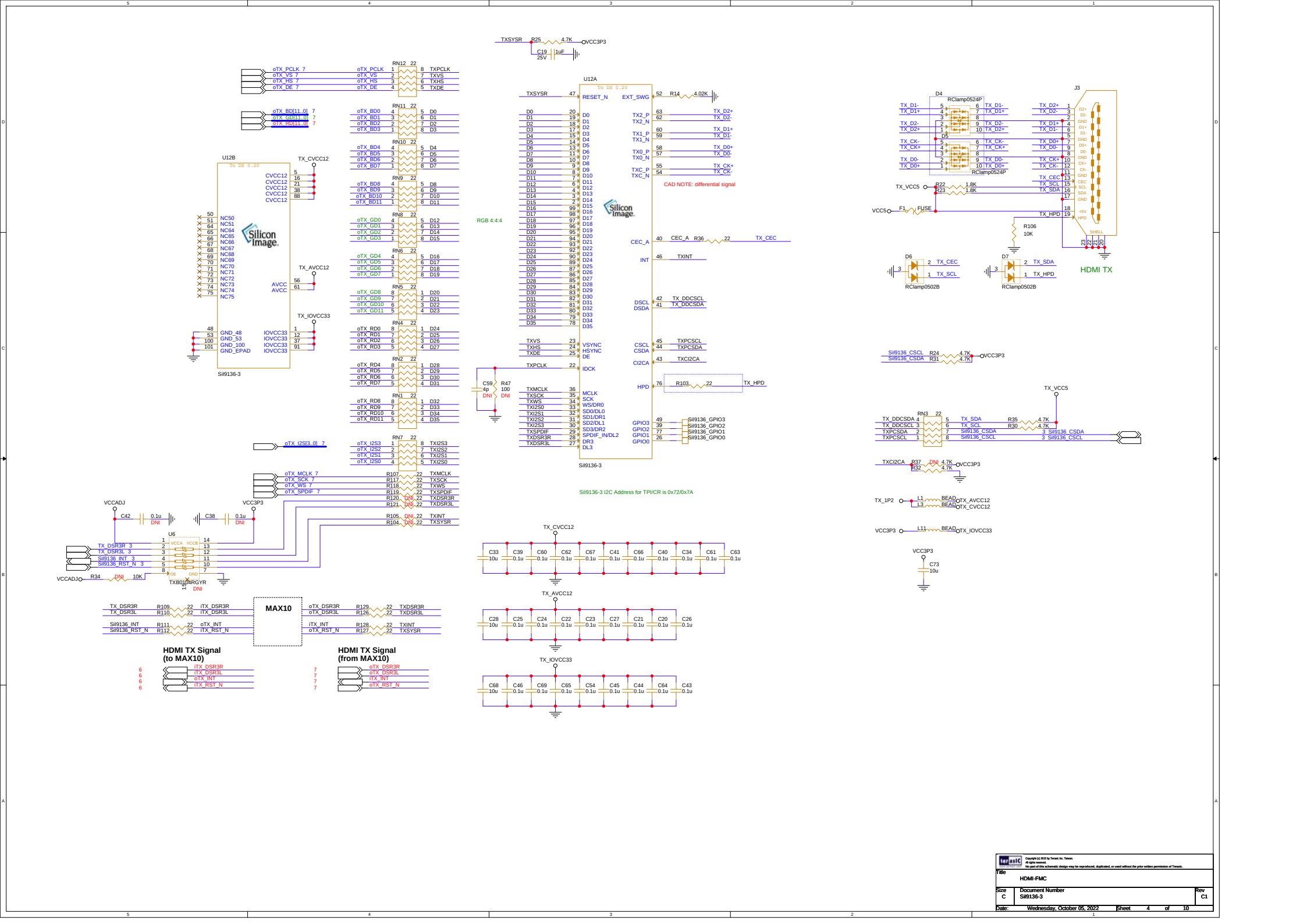
ADV7619_CSCL_FMC F4 — RX_MCLK F5
RX_GD6 F7; RX_BD0 F8; RX_DE F10; RX_BD8 F11; RX_VS F13; RX_HS F14; RX_BD11 F16; RX_BD7 F17
RX_BD3 F19; RX_GD7 F20; RX_RD15 J2; RX_RD14 J3; RX_GD4 J9; RX_BD10 J10
HA19_P J15; HA19_N J16; CLK3_BIDIR_P; CLK3_BIDIR_N; HA07_P J20; HA07_N J21; HA14_P J22; HA14_N J23
HA00_P_CC F4; HA00_N_CC F5
HA04_P F8; HA04_N F9; HA08_P F11; HA08_N F12; HA12_P F14; HA12_N F15; HA15_P F17; HA15_N F18
HA20_P E18; HA20_N E19; HA03_P J6; HA03_N J7; HA11_P J12; HA11_N J13; HA18_P J18; HA18_N J19
ADV7619_CSDA_FMC E2
HA01_P_CC E3 — for different clock input OCT only
HA05_P E6; HA05_N E7; HA09_P E9; HA09_N E10; HA13_P E12; HA13_N E13; HA16_P E15; HA16_N E16
HA21_P E18; HA21_N E19; HA02_P J6; HA02_N J7; HA10_P J12; HA10_N J13; HA17_P_CC J18; HA17_N_CC J19
RX_GD3 E6; RX_GD1 E7; RX_GD2 E9; RX_GD0 E10; RX_BD14 E12; RX_BD12 E13; RX_BD13 E15; RX_BD9 E16
RX_BD5 E18; RX_BD1 E19; RX_GD5 J6; RX_BD15 J7; RX_AP1 J12

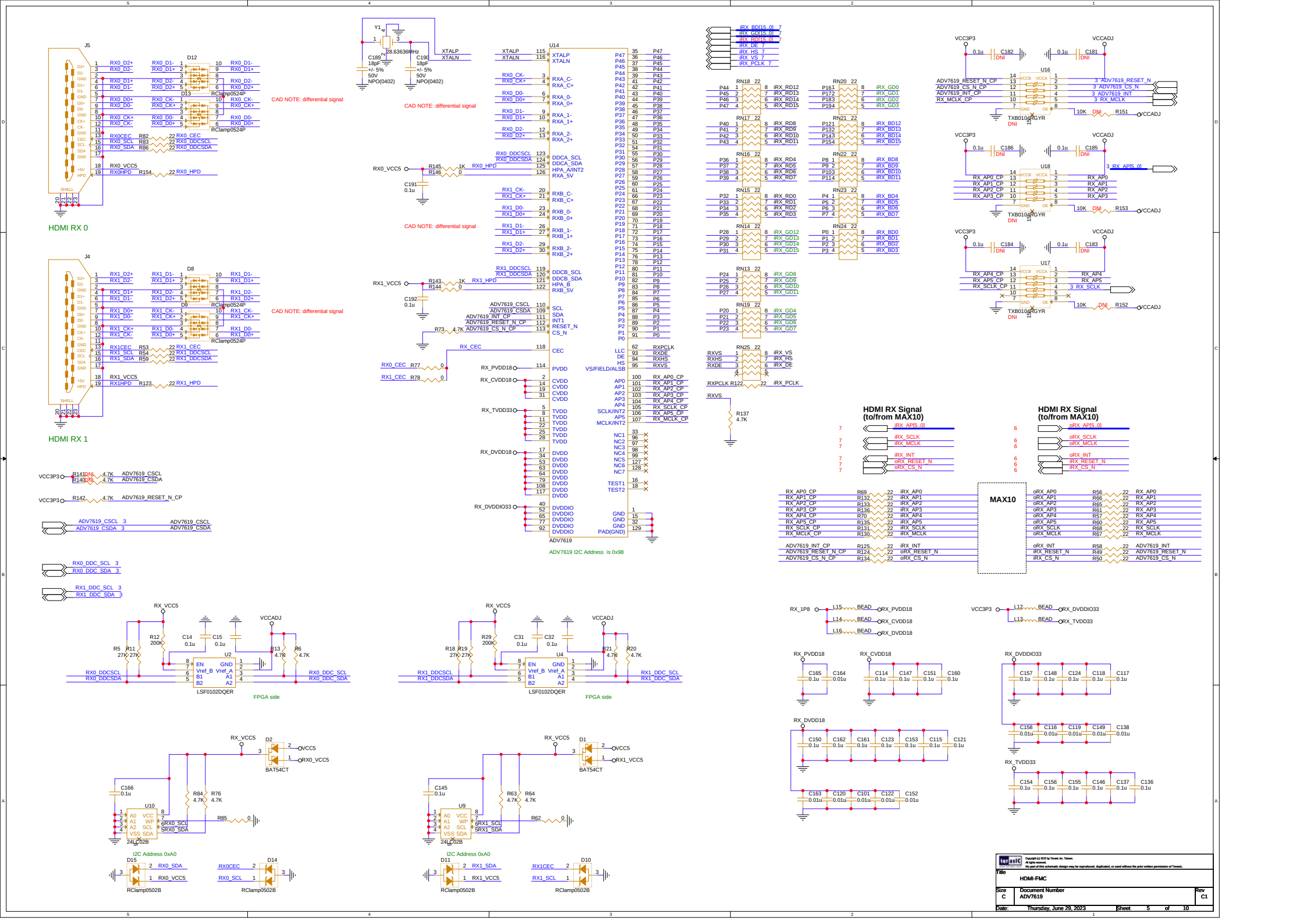
J1C — FMC_Vita57_1_HPC

RX_RD4 F37; RX_RD7 F38; RX_AP2 F22; RX_AP3 F23; RX_AP5 F25; RX_RD12 F26; RX_RD8 F28; RX_GD9 F29; RX_GD13 F31; RX_GD14 F32; RX_RD1 F34; RX_RD0 F35; RX_RD13 J24; RX_GD10 J30; RX_RD5 J36
HB20_P F22; HB20_N F23; HB02_P F25; HB02_N F26; HB04_P F28; HB04_N F29; HB08_P F31; HB08_N F32; HB12_P F34; HB12_N F35; HB16_P J24; HB16_N J25; HB01_P J30; HB01_N J31; HB11_P J36; HB11_N J37; HB18_P; HB18_N
HB21_P E36; HB21_N E37 — for different clock input OCT only
HB03_P E21; HB03_N E22; HB05_P E24; HB05_N E25; HB09_P E27; HB09_N E28; HB13_P E30; HB13_N E31; HB19_P E33; HB19_N E34; HB22_P J21; HB22_N J22; HB07_P J27; HB07_N J28; HB15_P J33; HB15_N J34
RX_GD15 E36; RX_BD2 E21; RX_AP0 E22; RX_AP4 E24; RX_SCLK E25; RX_RD11 E27; RX_RD10 E28; RX_GD8 E30; RX_GD12 E31; RX0_DDC_SCL E33; RX0_DDC_SDA E34; LED0 J21; RX_RD2 J27; LED1 J33

VCC3P3 R92 1K DNI, R90 1K DNI, R88 1K DNI
FMC_GA0 FMC_GA1
U11 24LC02B (A0, A1, A2, VSS, SDA, SCL, WP, VCC)
R91 1K, R89 1K, R87 1K
U3: Address 0~7
Default Address 0
VCC3P3 C170 0.1u R94 2K R93 2K
FMC_I2C_SCL FMC_I2C_SDA

Title: HDMI-FMC
Size: C
Document Number: FMC & Power
Rev: C1
Date: Wednesday, October 05, 2022
Sheet 3 of 10


U12B
To DS 0.20
Sil9136-3
U12A
To DS 0.20
Sil9136-3
RGB 4:4:4
CAD NOTE: differential signal
Sil9136-3 I2C Address for TPI/CR is 0x72/0x7A
HDMI TX
RCLamp0524P
RCLamp0502B
MAX10
HDMI TX Signal (to MAX10)
HDMI TX Signal (from MAX10)
TX_CVCC12
TX_AVCC12
TX_IOVCC33
VCCADJ
VCC3P3
VCC5
TX_VCC5
TX_HPD
TX_CEC
TX_SCL
TX_SDA
TX_DDCSCL
TX_DDCSDA
TXCI2CA
TX_1P2
Sil9136_CSCL
Sil9136_CSDA
Sil9136_GPIO3
Sil9136_GPIO2
Sil9136_GPIO1
Sil9136_GPIO0
TXSYSR
TXINT
TXSYSR
TXPCSCL
TXPCSDA
TXCI2CA
TXPCLK
TXMCLK
TXSCK
TXWS
TXSPDIF
TXDSR3R
TXDSR3L
TXINT
TXSYSR
TXVS
TXHS
TXDE
TXI2S3
TXI2S2
TXI2S1
TXI2S0
SHELL
HDMI-FMC
Sil9136-3
Wednesday, October 05, 2022
Sheet 4 of 10


HDMI RX 0
HDMI RX 1
CAD NOTE: differential signal
ADV7619 I2C Address is 0x98
HDMI RX Signal (to/from MAX10)
MAX10
FPGA side
I2C Address 0xA0
Title
HDMI-FMC
Document Number
ADV7619
Rev
C1
Size
C
Date:
Thursday, June 29, 2023
Sheet
5
of
10

MAX10 Bank 1 ~ 4

HDMI TX Video Signal (from FMC)

3 iTX_DE
3 iTX_HS
3 iTX_VS

3 iTX_BD[11..0]
3 iTX_GD[11..0]
3 iTX_RD[11..0]

HDMI TX Audio Signal (from FMC)

3 iTX_I2S[3..0]
3 iTX_MCLK
3 iTX_WS
3 iTX_SPDIF
3 iTX_SCK

HDMI TX Signal (to/from FMC)

4 iTX_DSR3R
4 iTX_DSR3L
4 oTX_INT
4 iTX_RST_N

HDMI RX Video Signal (to FMC)

3 oRX_BD[15..0]
3 oRX_GD[15..0]
3 oRX_RD[15..0]
3 oRX_DE
3 oRX_HS
3 oRX_VS

HDMI RX Signal (to/from FMC)

5 oRX_AP[5..0]
5 oRX_SCLK
5 oRX_MCLK
5 oRX_INT
5 iRX_RESET_N
5 iRX_CS_N

MAX10 Bank 1 & 2

U13A

MAX 10 LEFT BANKS

	BANK-1A VCCIO = 3.3V	BANK-2 VCCIO = Vadj		
F5	DIFFIO_RX_L1N/ADC1IN1	DIFFIO_RX_L29N	P4	iTX_I2S3
F4	DIFFIO_RX_L1P/ADC1IN2	DIFFIO_RX_L29P	P5	iTX_GD6
E4	DIFFIO_RX_L2N/ADC2IN1	DIFFIO_RX_L37N	N3	iTX_RD9
E3	DIFFIO_RX_L2P/ADC2IN8	DIFFIO_RX_L37P	N2	iTX_RD11
J8	DIFFIO_RX_L3N/ADC1IN3	DIFFIO_RX_L39N	R4	iTX_SPDIF
J9	DIFFIO_RX_L3P/ADC1IN4	DIFFIO_RX_L39P	R5	iTX_I2S1
G4	DIFFIO_RX_L4N/ADC2IN3	DIFFIO_RX_L40N	T1	iTX_GD7
F3	DIFFIO_RX_L4P/ADC2IN4	DIFFIO_RX_L40P	T2	iTX_BD5
H3	DIFFIO_RX_L5P/ADC1IN6	DIFFIO_RX_L41N	N8	iTX_WS
J4	DIFFIO_RX_L5N/ADC1IN5	DIFFIO_RX_L41P	N9	iTX_SCK
H4	DIFFIO_RX_L6N/ADC2IN5	DIFFIO_RX_L42N	P1	iTX_I2S2
G3	DIFFIO_RX_L6P/ADC2IN6	DIFFIO_RX_L42P	N1	iTX_RD10
K5	DIFFIO_RX_L7N/ADC1IN7	DIFFIO_RX_L43N	T3	iTX_RD8
K6	DIFFIO_RX_L7P/ADC1IN8	DIFFIO_RX_L43P	U2	iTX_GD4
J3	DIFFIO_RX_L8P/ADC2IN2	DIFFIO_RX_L44N	U1	iTX_GD5
K4	DIFFIO_RX_L8N/ADC2IN7	DIFFIO_RX_L44P	V1	iTX_GD9
		DIFFIO_RX_L45N	U4	iTX_RD5
		DIFFIO_RX_L45P	U5	iTX_GD2
		DIFFIO_RX_L46N	U3	iTX_RD1
		DIFFIO_RX_L46P	V3	iTX_RD0
		DIFFIO_RX_L47N	P8	iTX_I2S0
		DIFFIO_RX_L47P	R7	iTX_GD3
		DIFFIO_RX_L48N	W1	iTX_RD2
		DIFFIO_RX_L48P	W2	iTX_GD8
		DIFFIO_RX_L60N	R1	iTX_DSR3R
		DIFFIO_RX_L60P	R2	iTX_DSR3L
		VREFB2N0	M2	oTX_INT
		IO_BANK2	M1	iTX_RST_N

BANK-1B VCCIO = 3.3V

K8	DIFFIO_RX_L15N
D3	DIFFIO_RX_L16N
D2	DIFFIO_RX_L16P
K2	DIFFIO_RX_L19N
L2	DIFFIO_RX_L19P
L8	DIFFIO_RX_L20N
L9	DIFFIO_RX_L20P
E1	DIFFIO_RX_L21N
F2	DIFFIO_RX_L21P
H1	DIFFIO_RX_L22N
J1	DIFFIO_RX_L22P
G1	DIFFIO_RX_L23N
F1	DIFFIO_RX_L23P
M4	DIFFIO_RX_L24N
M3	DIFFIO_RX_L24P
K1	DIFFIO_RX_L25N
L1	DIFFIO_RX_L25P
C1	VREFB1N0
D1	IO_BANK1

10M50DAF484

MAX10 Bank 3 & 4

U13B

MAX 10 BOTTOM BANKS

		BANK-3 VCCIO = Vadj		BANK-4 VCCIO = Vadj		
iTX_BD1	Y7	DIFFIO_RX_B10N		DIFFIO_RX_B25N	W11	oRX_RD9
iTX_GD1	Y8	DIFFIO_RX_B10P		DIFFIO_RX_B25P	Y11	oRX_RD12
iTX_GD11	AB2	DIFFIO_RX_B12N		DIFFIO_RX_B27N	AB10	oRX_RD2
	AB3	DIFFIO_RX_B12P		DIFFIO_RX_B27P	AB11	
iTX_HS	Y3	DIFFIO_RX_B14N		DIFFIO_RX_B29N	AB12	oRX_BD3
iTX_BD9	Y4	DIFFIO_RX_B14P		DIFFIO_RX_B29P	AB13	oRX_BD6
iTX_DE	AA5	DIFFIO_RX_B17N		DIFFIO_RX_B35N	W12	oRX_BD1
iTX_RD7	AB5	DIFFIO_RX_B17P		DIFFIO_RX_B35P	W13	oRX_BD5
iTX_MCLK	AB6	DIFFIO_RX_B19N		DIFFIO_RX_B38N	AA14	oRX_BD11
iTX_BD2	AB7	DIFFIO_RX_B19P		DIFFIO_RX_B38P	AB15	oRX_BD10
iTX_BD11	AA8	DIFFIO_RX_B21N		DIFFIO_RX_B40N	AA15	oRX_BD13
iTX_BD3	AB8	DIFFIO_RX_B21P		DIFFIO_RX_B40P	Y16	oRX_DE
iTX_BD6	AA9	DIFFIO_RX_B23N		DIFFIO_RX_B42N	AB16	oRX_HS
iTX_GD0	AB9	DIFFIO_RX_B23P		DIFFIO_RX_B42P	AA16	oRX_BD14
iTX_BD8	V4	DIFFIO_RX_B2N		DIFFIO_RX_B44N	AB19	oRX_GD0
iTX_BD7	V5	DIFFIO_RX_B2P		DIFFIO_RX_B44P	AB20	oRX_GD4
iTX_RD3	Y1	DIFFIO_RX_B4N		DIFFIO_RX_B46N	AA19	oRX_GD2
iTX_RD4	Y2	DIFFIO_RX_B4P		DIFFIO_RX_B46P	Y18	oRX_GD6
iTX_GD10	AA1	DIFFIO_RX_B6N		DIFFIO_RX_B50N	AB21	oRX_BD0
iTX_RD6	AA2	DIFFIO_RX_B6P		DIFFIO_RX_B50P	AA20	oRX_GD1
iTX_BD0	Y5	DIFFIO_RX_B8N		DIFFIO_RX_B58N	AB17	oRX_VS
iTX_VS	Y6	DIFFIO_RX_B8P		DIFFIO_RX_B58P	AB18	oRX_BD15
iTX_BD4	W9	DIFFIO_TX_RX_B11N		DIFFIO_TX_RX_B24N	V11	oRX_GD9
iTX_BD10	W10	DIFFIO_TX_RX_B11P		DIFFIO_TX_RX_B24P	V12	oRX_BD2
oRX_GD12	W7	DIFFIO_TX_RX_B13N		DIFFIO_TX_RX_B26N	R12	oRX_RD13
oRX_GD11	W8	DIFFIO_TX_RX_B13P		DIFFIO_TX_RX_B26P	P12	oRX_RD14
oRX_GD8	R10	DIFFIO_TX_RX_B15N		DIFFIO_TX_RX_B28N	AA11	oRX_RD11
oRX_GD10	P10	DIFFIO_TX_RX_B15P		DIFFIO_TX_RX_B28P	AA12	oRX_BD4
oRX_GD14	AA6	DIFFIO_TX_RX_B16N		DIFFIO_TX_RX_B34N	V13	oRX_GD7
oRX_GD13	AA7	DIFFIO_TX_RX_B16P		DIFFIO_TX_RX_B34P	W14	oRX_BD8
oRX_RD3	W5	DIFFIO_TX_RX_B1N		DIFFIO_TX_RX_B36N	R13	oRX_BD9
oRX_RD0	W6	DIFFIO_TX_RX_B1P		DIFFIO_TX_RX_B36P	P13	oRX_RD15
oRX_RD8	Y10	DIFFIO_TX_RX_B22N		DIFFIO_TX_RX_B37N	Y13	oRX_BD7
oRX_RD10	AA10	DIFFIO_TX_RX_B22P		DIFFIO_TX_RX_B37P	Y14	oRX_BD12
oRX_RD7	U6	DIFFIO_TX_RX_B3N		DIFFIO_TX_RX_B39N	V14	oRX_GD5
oRX_RD6	U7	DIFFIO_TX_RX_B3P		DIFFIO_TX_RX_B39P	W15	oRX_GD3
oRX_RD5	W4	DIFFIO_TX_RX_B5N		DIFFIO_TX_RX_B41N	U15	oRX_AP0
oRX_RD4	W3	DIFFIO_TX_RX_B5P		DIFFIO_TX_RX_B41P	V16	oRX_AP1
oRX_GD15	V7	DIFFIO_TX_RX_B7N		DIFFIO_TX_RX_B43N	AA17	oRX_AP2
oRX_RD1	V8	DIFFIO_TX_RX_B7P		DIFFIO_TX_RX_B43P	Y17	oRX_AP3
	R9	DIFFIO_TX_RX_B9N		DIFFIO_TX_RX_B45N	V15	oRX_AP4
	P9	DIFFIO_TX_RX_B9P		DIFFIO_TX_RX_B45P	W16	oRX_AP5
iRX_RESET_N	AA3	VREFB3N0		DIFFIO_TX_RX_B49N	Y19	oRX_SCLK
iRX_CS_N	AB4	IO_BANK3		DIFFIO_TX_RX_B49P	W18	oRX_MCLK
				VREFB4N0	AA13	
				IO_BANK4	AB14	oRX_INT

10M50DAF484

Title	HDMI-FMC	
Size B	Document Number MAX 10 Bank 1 ~ 4	Rev C1
Date: Wednesday, October 05, 2022	Sheet 6 of 10	

MAX10 Bank 5 ~ 8

HDMI TX Video Signal (to Chip)

4 oTX_PCLK
4 oTX_VS
4 oTX_HS
4 oTX_DE
4 oTX_BD[11..0]
4 oTX_GD[11..0]
4 oTX_RD[11..0]

HDMI TX Audio Signal (to Chip)

4 oTX_I2S[3..0]
4 oTX_MCLK
4 oTX_SCK
4 oTX_WS
4 oTX_SPDIF

HDMI TX Signal (to/from Chip)

4 oTX_DSR3R
4 oTX_DSR3L
4 iTX_INT
4 oTX_RST_N

HDMI RX Video Signal (from Chip)

5 iRX_BD[15..0]
5 iRX_GD[15..0]
5 iRX_RD[15..0]
5 iRX_DE
5 iRX_HS
5 iRX_VS
5 iRX_PCLK

HDMI RX Signal (to/from Chip)

5 iRX_AP[5..0]
5 iRX_SCLK
5 iRX_MCLK
5 iRX_INT
5 oRX_RESET_N
5 oRX_CS_N

VCC3P3

LED0 — 1 — LEDG — LED0 — 2 — R155 — 120

LED1 — 1 — LEDG — LED1 — 2 — R156 — 120

U13C MAX10 Bank 5 & 6

MAX 10 RIGHT BANKS

		BANK-5 VCCIO = 3.3V		BANK-6 VCCIO = 3.3V		
iRX_GD6	U19	DIFFIO_RX_R19N	H21	DIFFIO_RX_R39N	H21	iRX_BD10
iRX_GD4	V18	DIFFIO_RX_R19P	H22	DIFFIO_RX_R39P	H22	iRX_BD9
iRX_GD5	U18	DIFFIO_RX_R1P/RUP	J21	DIFFIO_RX_R41N	J21	iRX_BD0
iRX_GD7	U17	DIFFIO_RX_R1N/RDN	J22	DIFFIO_RX_R41P	J22	iRX_DE
	W22	DIFFIO_RX_R20N	G19	DIFFIO_RX_R42N	G19	
iRX_GD1	Y22	DIFFIO_RX_R20P	G20	DIFFIO_RX_R42P	G20	
iRX_GD2	W20	DIFFIO_RX_R21N	F22	DIFFIO_RX_R43N	F22	
iRX_GD3	W19	DIFFIO_RX_R21P	G22	DIFFIO_RX_R43P	G22	
iRX_GD0	Y21	DIFFIO_RX_R22N	M14	DIFFIO_RX_R44N/DQ2R	M14	iRX_RD4
	Y20	DIFFIO_RX_R22P	M15	DIFFIO_RX_R44P/DQ2R	M15	iRX_RD2
oTX_DSR3R	U20	DIFFIO_RX_R23N	E21	DIFFIO_RX_R45N	E21	iRX_BD13
oTX_DSR3L	V20	DIFFIO_RX_R23P	E22	DIFFIO_RX_R45P	E22	iRX_BD12
iTX_INT	V22	DIFFIO_RX_R24N	N19	DIFFIO_RX_R46N/DM2R	N19	
oTX_RST_N	V21	DIFFIO_RX_R24P	N18	DIFFIO_RX_R46P/DQ2R	N18	
	R14	DIFFIO_RX_R25N/DQ1R	M20	DIFFIO_RX_R47P/DQ2R	M20	iRX_HS
iRX_AP0	R15	DIFFIO_RX_R25P/DQ1R	N20	DIFFIO_RX_R47N/DQ2R	N20	iRX_VS
iRX_AP1	T22	DIFFIO_RX_R26N	F20	DIFFIO_RX_R48N	F20	iRX_RD15
iRX_AP2	T21	DIFFIO_RX_R26P	F21	DIFFIO_RX_R48P	F21	iRX_BD11
iRX_AP3	T18	DIFFIO_RX_R27N/DM1R	C22	DIFFIO_RX_R49N	C22	iRX_BD15
iRX_AP4	T19	DIFFIO_RX_R27P/DQ1R	D22	DIFFIO_RX_R49P	D22	
iRX_AP5	R20	DIFFIO_RX_R28N/DQ1R	L18	DIFFIO_RX_R51N/DQ2R	L18	iRX_GD15
iRX_SCLK	T20	DIFFIO_RX_R28P/DQ1R	M18	DIFFIO_RX_R51P/DQ2R	M18	iRX_GD14
iRX_MCLK	U22	DIFFIO_RX_R29N	L20	DIFFIO_RX_R52N/DQ2R	L20	iRX_BD1
	U21	DIFFIO_RX_R29P	L19	DIFFIO_RX_R52P/DQ2R	L19	iRX_BD3
iRX_INT	AA22	DIFFIO_RX_R2N	F18	DIFFIO_RX_R53N	F18	iRX_PCLK
oRX_RESET_N	AA21	DIFFIO_RX_R2P	E19	DIFFIO_RX_R53P	E19	iRX_RD12
oRX_CS_N	P14	DIFFIO_RX_R30N/DQ1R	E20	DIFFIO_RX_R54N	E20	iRX_RD13
	P15	DIFFIO_RX_R30P/DQ1R	F19	DIFFIO_RX_R54P	F19	iRX_RD14
	N22	DIFFIO_RX_R31N	K15	DIFFIO_RX_R55N/DQSN3R	K15	iRX_RD3
	P21	DIFFIO_RX_R31P	K14	DIFFIO_RX_R55P/DQS3R	K14	oTX_GD0
	P18	DIFFIO_RX_R32N/DQSN1R	D19	DIFFIO_RX_R56N	D19	iRX_RD10
	R18	DIFFIO_RX_R32P/DQS1R	C20	DIFFIO_RX_R56P	C20	iRX_RD8
	P20	DIFFIO_RX_R33N/DQ1R	J18	DIFFIO_RX_R57N/DQ3R	J18	iRX_GD13
	P19	DIFFIO_RX_R33P/DQ1R	K18	DIFFIO_RX_R57P/DQ3R	K18	iRX_GD12
LED0	L22	DIFFIO_RX_R34N	K20	DIFFIO_RX_R58N/DQ3R	K20	iRX_BD2
	M21	DIFFIO_RX_R34P	K19	DIFFIO_RX_R58P/DQ3R	K19	iRX_BD4
LED1	M22	DIFFIO_RX_R35N	E17	DIFFIO_RX_R59N	E17	iRX_GD9
	N21	DIFFIO_RX_R35P	F17	DIFFIO_RX_R59P	F17	iRX_GD8
	P22	VREFB5N0	B21	DIFFIO_RX_R60N	B21	oTX_DE
	R22	IO_BANK5	B22	DIFFIO_RX_R60P	B22	iRX_RD11
			J15	DIFFIO_RX_R61N/DM3R	J15	iRX_RD1
			J14	DIFFIO_RX_R61P/DQ3R	J14	iRX_RD0
			A21	DIFFIO_RX_R62N	A21	oTX_HS
			B20	DIFFIO_RX_R62P	B20	oTX_VS
			H18	DIFFIO_RX_R63N/DQ3R	H18	iRX_GD10
			H19	DIFFIO_RX_R63P/DQ3R	H19	iRX_BD7
			H20	DIFFIO_RX_R64N/DQ3R	H20	iRX_BD6
			J20	DIFFIO_RX_R64P/DQ3R	J20	iRX_BD5
			E18	DIFFIO_RX_R70N/CK#_6	E18	iRX_RD6
			D18	DIFFIO_RX_R70P/CK_6	D18	iRX_RD5
			D21	VREFB6N0	D21	iRX_BD14
			C21	IO_BANK6	C21	

10M50DAF484

U13D MAX10 Bank 7 & 8

MAX 10 TOP BANKS

		BANK-7 VCCIO = 3.3V		BANK-8 VCCIO = 3.3V	
oTX_BD6	A17	DIFFIO_RX_T10N	C7	DIFFIO_RX_T39N	C7
oTX_BD3	A18	DIFFIO_RX_T10P	C8	DIFFIO_RX_T39P	C8
oTX_RD10	C15	DIFFIO_RX_T15N	A6	DIFFIO_RX_T41N	A6
oTX_BD9	C16	DIFFIO_RX_T15P	B7	DIFFIO_RX_T41P	B7
oTX_BD5	A16	DIFFIO_RX_T16N	D8	DIFFIO_RX_T42P	D8
oTX_BD8	B16	DIFFIO_RX_T16P	A4	DIFFIO_RX_T43N	A4
oTX_RD3	J13	DIFFIO_RX_T17N	A5	DIFFIO_RX_T43P	A5
oTX_RD5	H14	DIFFIO_RX_T17P	E9	DIFFIO_RX_T44N	E9
oTX_I2S2	C13	DIFFIO_RX_T18N	A2	DIFFIO_RX_T45P	A2
oTX_SPDIF	C14	DIFFIO_RX_T18P	A3	DIFFIO_RX_T45N	A3
oTX_BD10	B14	DIFFIO_RX_T19N	B3	DIFFIO_RX_T46P	B3
oTX_BD11	A14	DIFFIO_RX_T19P	B4	DIFFIO_RX_T46N	B4
iRX_BD8	E15	DIFFIO_RX_T1N	B5	DIFFIO_RX_T47P	B5
oTX_RD11	E16	DIFFIO_RX_T1P	C4	DIFFIO_RX_T47N	C4
oTX_RD6	E13	DIFFIO_RX_T20N	E8	DIFFIO_RX_T48P	E8
oTX_RD8	D14	DIFFIO_RX_T20P	D5	DIFFIO_RX_T49N	D5
oTX_WS	E12	DIFFIO_RX_T21P	C5	DIFFIO_RX_T49P	C5
oTX_I2S3	D13	DIFFIO_RX_T21N	B1	DIFFIO_RX_T51N	B1
oTX_RD2	J12	DIFFIO_RX_T22N	B2	DIFFIO_RX_T51P	B2
oTX_RD4	H13	DIFFIO_RX_T22P	C2	DIFFIO_RX_T53N	C2
oTX_GD2	A12	DIFFIO_RX_T23N	C3	DIFFIO_RX_T53P	C3
oTX_BD7	A13	DIFFIO_RX_T23P	D7	VREFB8N0	D7
oTX_I2S1	D12	DIFFIO_RX_T24N	C6	IO_BANK8	C6
oTX_I2S0	C12	DIFFIO_RX_T24P			
oTX_GD6	A10	DIFFIO_RX_T25N			
oTX_GD4	A11	DIFFIO_RX_T25P			
oTX_SCK	C10	DIFFIO_RX_T26N			
oTX_GD3	C11	DIFFIO_RX_T26P			
oTX_GD5	B11	DIFFIO_RX_T27N			
oTX_GD1	B12	DIFFIO_RX_T27P			
oTX_RD0	J11	DIFFIO_RX_T28N			
oTX_RD1	H12	DIFFIO_RX_T28P			
oTX_GD10	B8	DIFFIO_RX_T31N			
oTX_GD8	A9	DIFFIO_RX_T31P			
iRX_GD11	C17	DIFFIO_RX_T2N			
oTX_PCLK	D17	DIFFIO_RX_T2P			
oTX_MCLK	C9	DIFFIO_RX_T30N			
oTX_GD7	B10	DIFFIO_RX_T30P			
oTX_GD11	A7	DIFFIO_RX_T29P			
oTX_GD9	A8	DIFFIO_RX_T29N			
oTX_RD7	F15	DIFFIO_RX_T5N			
oTX_RD9	F16	DIFFIO_RX_T5P			
oTX_BD0	B19	DIFFIO_RX_T6N			
iRX_RD7	C19	DIFFIO_RX_T6P			
oTX_BD4	B17	DIFFIO_RX_T7N			
oTX_BD2	C18	DIFFIO_RX_T7P			
oTX_BD1	A19	DIFFIO_RX_T8N			
iRX_RD9	A20	DIFFIO_RX_T8P			
	E14	DIFFIO_RX_T9N			
	D15	DIFFIO_RX_T9P			
	B15	VREFB7N0			
	A15	IO_BANK7			

10M50DAF484

Title: **HDMI-FMC**

Size	Document Number	Rev
B	MAX 10 Bank 5 ~ 8	C1

Date: Wednesday, October 05, 2022 Sheet 7 of 10

MAX10 Clock

HDMI TX Video Signal (from FMC)

3 iTX_PCLK

HDMI RX Video Signal (to FMC)

3 oRX_PCLK

U13E

MAX 10 CLOCK

BANK-2 VCCIO = Vadj

N4	DIFFIO_RX_L28N/CLK0N	DIFFIO_RX_L38N/DPCLK0	P3
N5	DIFFIO_RX_L28P/CLK0P	DIFFIO_RX_L38P/DPCLK1	R3
M8	DIFFIO_RX_L36N/CLK1N	DIFFIO_RX_L59N/PLL_L_CLKOUTN	T5
M9	DIFFIO_RX_L36P/CLK1P	DIFFIO_RX_L59P/PLL_L_CLKOUTP	T6

BANK-3 VCCIO = Vadj

iTX_PCLK

V9	DIFFIO_TX_RX_B18N/CLK6N
V10	DIFFIO_TX_RX_B18P/CLK6P
R11	DIFFIO_TX_RX_B20N/CLK7N
P11	DIFFIO_TX_RX_B20P/CLK7P

BANK-4 VCCIO = Vadj

DIFFIO_TX_RX_B57N/PLL_B_CLKOUTN	W17	
DIFFIO_TX_RX_B57P/PLL_B_CLKOUTP	V17	oRX_PCLK

BANK-6 VCCIO = 3.3V

MAX10_CLK1_50

N15	DIFFIO_RX_R38N/CLK2N	DIFFIO_RX_R50N/DPCLK2/DQSn2R	L15
N14	DIFFIO_RX_R38P/CLK2P	DIFFIO_RX_R50P/DPCLK3/DQS2R	L14
K21	DIFFIO_RX_R40N/CLK3N	DIFFIO_RX_R69N/PLL_R_CLKOUTN	G17
K22	DIFFIO_RX_R40P/CLK3P	DIFFIO_RX_R69P/PLL_R_CLKOUTP	H17

BANK-8 VCCIO = 3.3V

E10	DIFFIO_RX_T38N/CLK4N		
E11	DIFFIO_RX_T38P/CLK4P		
J10	DIFFIO_RX_T40P/CLK5P	DIFFIO_RX_T52N/PLL_T_CLKOUTN	E6
H11	DIFFIO_RX_T40N/CLK5N	DIFFIO_RX_T52P/PLL_T_CLKOUTP	D6

10M50DAF484

CAD Note:
Place near power pin

VCC3P3 — C159 0.1u 10V

X1: EN, VCC, GND, OUT — 50MHz

VCC3P3 — R72 18.2 — MAX10_CLK1_50

MAX10 Configuration

JTAG Interface

3 FMC_JTAG_TCK
3 FMC_JTAG_TMS
3 FMC_JTAG_TDI
3 FMC_JTAG_TDO

VCC3P3 — R55 10K, R114 10K, R113 10K

R116 0 DNI, R115 1K, C180 12p DNI

Design Note:
Optional termination resistor for JTAG TCK

CAD Note:
Place near JTAG TCK pin

U13F

MAX 10 Configuration

BANK-1B VCCIO = 3.3V

MAX_JTAG_EN	K9
MAX_JTAG_TCK	G2
MAX_JTAG_TMS	H2
MAX_JTAG_TDI	L4
MAX_JTAG_TDO	M5
DIFFIO_RX_L15P/JTAGEN	
DIFFIO_RX_L17P/TCK	
DIFFIO_RX_L17N/TMS	
DIFFIO_RX_L18N/TDI	
DIFFIO_RX_L18P/TDO	

BANK-8 VCCIO = 3.3V

NCONFIG	H9	NCONFIG
CONFIG_SEL	H10	CONFIG_SEL
DIFFIO_RX_T42N/DEV_CLRN	D9	
DIFFIO_RX_T44P/DEV_OE	D10	
DIFFIO_RX_T48N/CRC_ERROR	F7	
DIFFIO_RX_T50P/NSTATUS	G9	NSTATUS
DIFFIO_RX_T50N/CONF_DONE	F8	CONF_DONE

10M50DAF484

VCC3P3 — R48 10K, R52 10K, R51 10K

VCC3P3 — R75 10K DNI, R71 10K

VCC3P3 — R74 1K

Boot Select

JP1 — DNI — 1X2 Header

BOOT Select

Default Disable (Jumper Open)

OPEN = configuration image 0 (Low)
SHORT = configuration image 1 (High)

FMC Side / MAX10 Side

FMC Side	MAX10 Side
TRST	TRST
TMS	TMS
TDO	TDO
TDI	TDI
TCK	TCK

FMC_JTAG_TMS	R95	DNI 0	MAX_JTAG_TMS	
FMC_JTAG_TDO	R97	DNI 0	MAX_JTAG_TDO	
FMC_JTAG_TDI	R98	DNI 0	MAX_JTAG_TDI	
FMC_JTAG_TCK	R96	DNI 0	MAX_JTAG_TCK	

MAX_JTAG_TCK
MAX_JTAG_TDO
MAX_JTAG_TMS
MAX_JTAG_TDI

J2 — CPLD ISP — DNI — VCC3P3

Title: HDMI-FMC

Size	Document Number	Rev
B	MAX 10 Clocks and Config	C1

Date: Wednesday, October 05, 2022 Sheet 8 of 10

MAX10 Power

VCC1P2_VCC — L10 30ohm, 3A — VCC1P2_VCCD
C78 4.7u

VCC1P2_VCC — L9 30ohm, 3A — VCC1P2_VDDADC
C72 10u
C81 10u
CAD Notes: Place the 10uF cap close to ferrite bead. Place the 0.1uF cap close to MAX10 pin.

REF_VCC2P5 — R45 1 — ADC_VREF
C70 10u
C74 1u
CAD Notes: Put the caps close to MAX10 pin.

VCC2P5_CORE — L7 30ohm, 3A — VCC2P5_VCCA
CAD Notes: Place the 10uF cap close to ferrite bead. Place the 0.1uF cap close to MAX10 pin.
C51 10u
C50 0.1u

VCC2P5_CORE — L8 220ohm, 2.5A — VCC2P5_VCCADC
CAD Notes: Place the 10uF cap close to ferrite bead. Place the 0.1uF cap close to MAX10 pin.
C56 10u
C71 0.1u

VCC1P2_VCC
CAD Note: Place capacitor near FPGA pins
C52 10u, C53 10u, C97 1u, C108 1u, C110 1u, C95 1u, C92 1u, C107 1u, C94 1u, C109 1u, C96 22n, C93 22n, C106 10n, C105 10n

VCC2P5_VCCA
CAD Notes: Place a 1uF cap close to each MAX10 VCCA pins.
C127 0.1u, C86 0.1u, C134 0.1u, C80 0.1u

VCC1P2_VCCD
CAD Notes: Place a 0.1uF cap close to each MAX10 VCCD pins.
C79 0.1u, C88 0.1u, C135 0.1u, C126 0.1u

U13G

MAX 10 POWER

VCC1P2_VCC
N12 VCC, N10 VCC, M13 VCC, M12 VCC, M11 VCC, L12 VCC, L11 VCC, L10 VCC, K13 VCC, K11 VCC

VCC1P2_VCCD
T7 VCCD_PLL1, G16 VCCD_PLL2, G7 VCCD_PLL3, U16 VCCD_PLL4

VCC2P5_VCCA
R8 VCCA1, H15 VCCA2, H8 VCCA3, T15 VCCA4

VCC1P2_VDDADC
VCC2P5_VCCADC
J7 VCCINT, H7 VCCA_ADC

ADC_VREF
H6 ADC_VREF

NC
G5 ANAIN1, J5 ANAIN2

VCC3P3
L6 VCCIO1A, K7 VCCIO1A, M6 VCCIO1B, L7 VCCIO1B

VCCADJ
R6 VCCIO2, P7 VCCIO2, N7 VCCIO2, N6 VCCIO2

VCCADJ
U9 VCCIO3, U8 VCCIO3, T9 VCCIO3, T11 VCCIO3, T10 VCCIO3

VCCADJ
U14 VCCIO4, U12 VCCIO4, U11 VCCIO4, T13 VCCIO4, T12 VCCIO4

VCC3P3
T17 VCCIO5, R17 VCCIO5, R16 VCCIO5, P16 VCCIO5, N16 VCCIO5

VCC3P3
N17 VCCIO6, M17 VCCIO6, L16 VCCIO6, K17 VCCIO6, K16 VCCIO6, J17 VCCIO6, H16 VCCIO6

VCC3P3
G14 VCCIO7, G13 VCCIO7, G12 VCCIO7, F14 VCCIO7, F12 VCCIO7

VCC3P3
G11 VCCIO8, G10 VCCIO8, F9 VCCIO8, F11 VCCIO8

10M50DAF484

U13H

MAX 10 GROUND

Y9, Y15, Y12, W21, V6, V2, V19, U13, U10, T8, T4, T16, T14, R21, R19, P6, P2, P17, N13, N11, M7, M19, M16, M10, L5, L21, L17, L13 — GND

REFGND — L3 — REFGND H5

DNU
REFGND

K12, K10, K3, J6, J2, J19, J16, G8, G6, G21, G18, G15, F13, F10, E7, E2, D4, D20, D16, D11, B9, B6, B18, B13, AB22, AB1, AA4, AA18, A22, A1 — GND

E5 NC1
F6 NC2

10M50DAF484

1. Use REFGND as ground reference.
2. Route analog input signal adjacent to AVSSREF as possible.

CAD Notes: Place this FB close to MAX10 ADC_VREF.

L17 30ohm, 3A

VCC3P3
CAD Notes: Place these caps close to MAX10 VCCIO1, VCCIO5, VCCIO6, VCCIO7 and VCCIO8 pins.
C75 4.7u, C82 4.7u, C83 0.1u, C91 0.1u, C104 0.1u, C102 0.1u, C90 0.1u, C103 0.1u, C125 0.1u, C139 0.1u, C140 0.1u, C141 0.1u, C142 0.1u, C143 0.1u 10V, C144 0.1u 10V, C128 0.1u 10V, C129 0.1u 10V, C130 0.1u 10V, C131 0.1u 10V, C132 0.1u 10V, C133 0.1u 10V

VCCADJ
CAD Notes: Place these caps close to MAX10 VCCIO2, VCCIO3, and VCCIO4 pins.
C113 10u, C77 1u, C84 1u, C89 0.1u, C87 0.1u, C100 0.1u, C98 0.1u, C112 10n, C76 10n, C99 0.1u, C85 0.1u, C111 10n

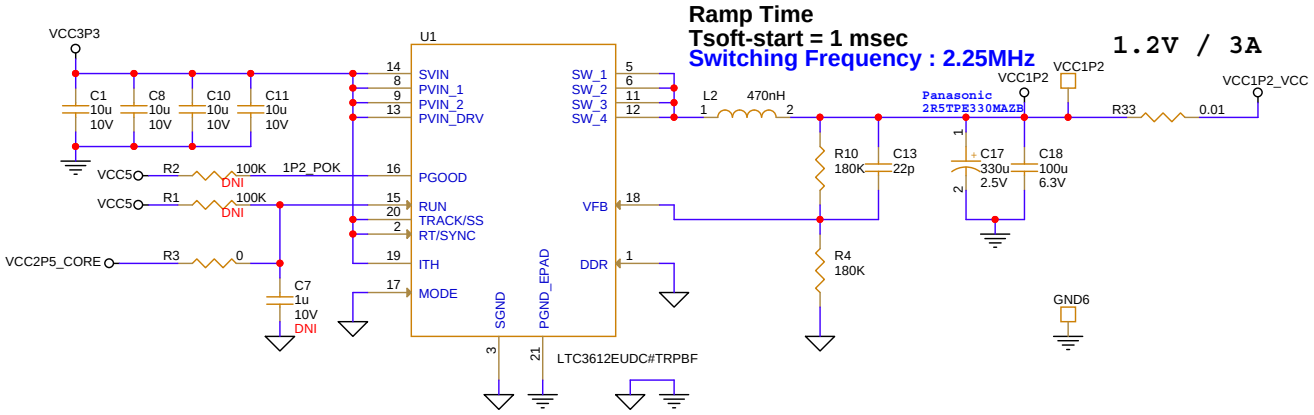
Title: **HDMI-FMC**

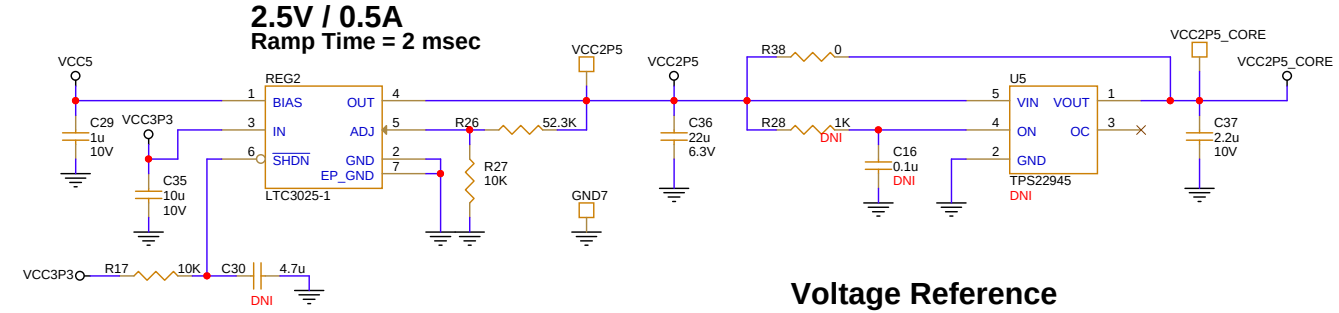
Size	Document Number	Rev
B	MAX10 Power & Decoupling	C1

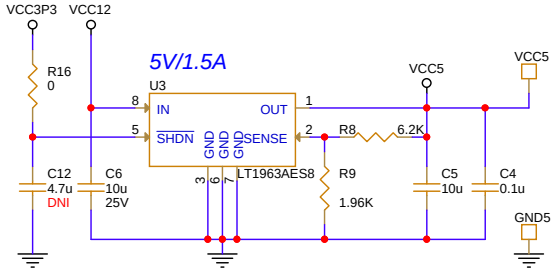
Date: Wednesday, October 05, 2022 Sheet 9 of 10

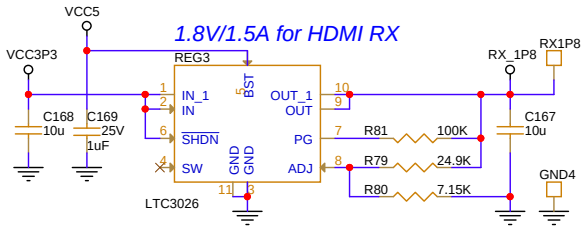
Power

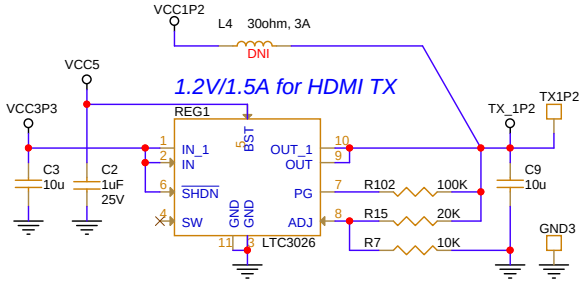
Power up Sequence:
VCC5---> VCC2P5, VCC3P3 ---> VCC1P2_VCC



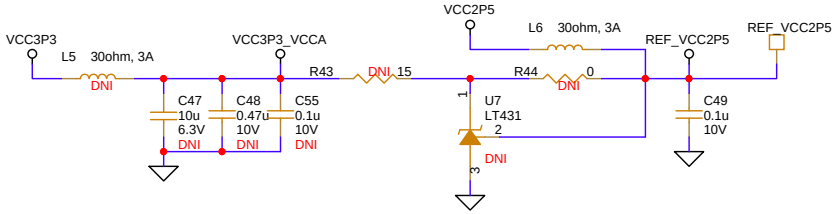


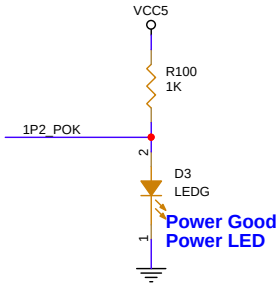






Voltage Reference





Layout:
Place on bottom corners of board

FID2 FID4 FID3 FID1 PCB1
MH1 MH4 MH7 MH8 FID5 FID8 FID7 FID6
10-21508210-C0

Title	HDMI-FMC	
Size B	Document Number Power System	Rev C1
Date: Wednesday, October 05, 2022	Sheet 10 of 10	