IT6613

HDMI 1.4 Transmitter with 3D Support

ITE TECH. INC.

General Description

The IT6613 is a high-performance HDMI transmitter, fully compatible with HDMI 1.3, compatible with HDMI 1.4a 3D and HDCP 1.4 compliance and also backward compatible to DVI 1.0 specifications. The IT6613 supports color depth of up to 36 bits (12 bits/color) and ensures robust transmission of high-quality uncompressed video content, along with state-of-the-art uncompressed and compressed digital audio content such as DTS-HD and Dolby TrueHD in DVD/HD-DVD/Bluray players and settop boxes. The IT6613 also supports diverse 3D formats which are compliant with HDMI 1.4a 3D specification.

Aside from the various video output formats supported, the IT6613 also encodes and transmits up to 8 channels of I^2S digital audio, with sampling rate up to 192kHz and sample size up to 24 bits. In addition, an S/PDIF input port takes in compressed audio of up to 192kHz frame rate, while Super Audio Compact Disc (SACD) is supported through dedicated DSD ports (Direct Stream Digital ports) at up to 88.2kHz one-bit audio.

The High-Bit Rate (HBR) audio is also provided by the IT6613 in two interfaces: with the four I^2S input ports or the S/PDIF input port. With both interfaces the highest possible HBR frame rate is supported at up to 768kHz.

Each IT6613 chip comes preprogrammed with an unique HDCP key, in compliance with the HDCP 1.4 standard so as to provide secure transmission of high-definition content. Users of the IT6613 need not purchase any HDCP keys or ROMs.

The IT6613 is pin compatible with the CAT6613, the previous generation HDMI 1.3 transmitter.

Features

- HDMI 1.4 transmitter
- Pin compatible with CAT6613
- Compliant with HDMI 1.3, HDMI 1.4a 3D, HDCP 1.4 and DVI 1.0 specifications
- Supporting link speeds of up to 2.25Gbps (link clock rate of 225MHz).
- Supporting diverse 3D formats which are compliant with HDMI 1.4a 3D specification.
  - Supporting 3D video up to 1080P@23.98/24/30Hz, 1080i@50/59.94/60/Hz, 720P@50/59.94/60Hz
  - Supporting formats: framing packing, side-by-side (half), top-and-bottom.
- Various video input interface supporting digital video standards such as:
  - 24/30/36-bit RGB/YCbCr 4:4:4

  - 16/20/24-bit YCbCr 4:2:2
  - 8/10/12-bit YCbCr 4:2:2 (CCIR-656)
  - 12/15/18-bit double data rate interface (data bus width halved, clocked with both rising and falling edges) for RGB/YCbCr 4:4:4
- Bi-direction Color Space Conversion (CSC) between RGB and YCbCr color spaces with programmable coefficients.
- Up/down sampling between YCbCr 4:4:4 and YCbCr 4:2:2
- Dithering for conversion from 12-bit/10-bit component to 8-bit
- Support Gammat Metadata packet
- Digital audio input interface supporting
  - up to four I^2S interface supporting 8-channel audio, with sample rates of 32~192 kHz and smaple sizes of 16~24 bits
  - S/PDIF interface supporting PCM, Dolby Digital, DTS digital audio at up to 192kHz frame rate
  - Support for high-bit-rate (HBR) audio such as DTS-HD and Dolby TrueHD through the four I^2S interface or the S/PDIF interface, with frame rates as high as 768kHz
  - Support for 8-channel DSD audio through dedicated inputs
  - Compatible with IEC 60958 and IEC 61937
  - Audio down-sampling of 2X and 4X
- Software programmable, auto-calibrated TMDS source terminations provide for optimal source signal quality
- Software programmable HDMI output current level
- MCLK input is optional for audio operation. Users could opt to implement audio input interface with or without MCLK.
- Integrated pre-programmed HDCP keys
- Purely hardware HDCP engine increasing the robustness and security of HDCP operation
- Monitor detection through Hot Plug Detection and Receiver Termination Detection
- Embedded full-function pattern generator
- Intelligent, programmable power management
- 100-pin LQFP package

Ordering Information

Model	Temperature Range	Package Type	Green/Pb free Option
IT6613E	0~70	100-pin LQFP	Green

Pin Diagram

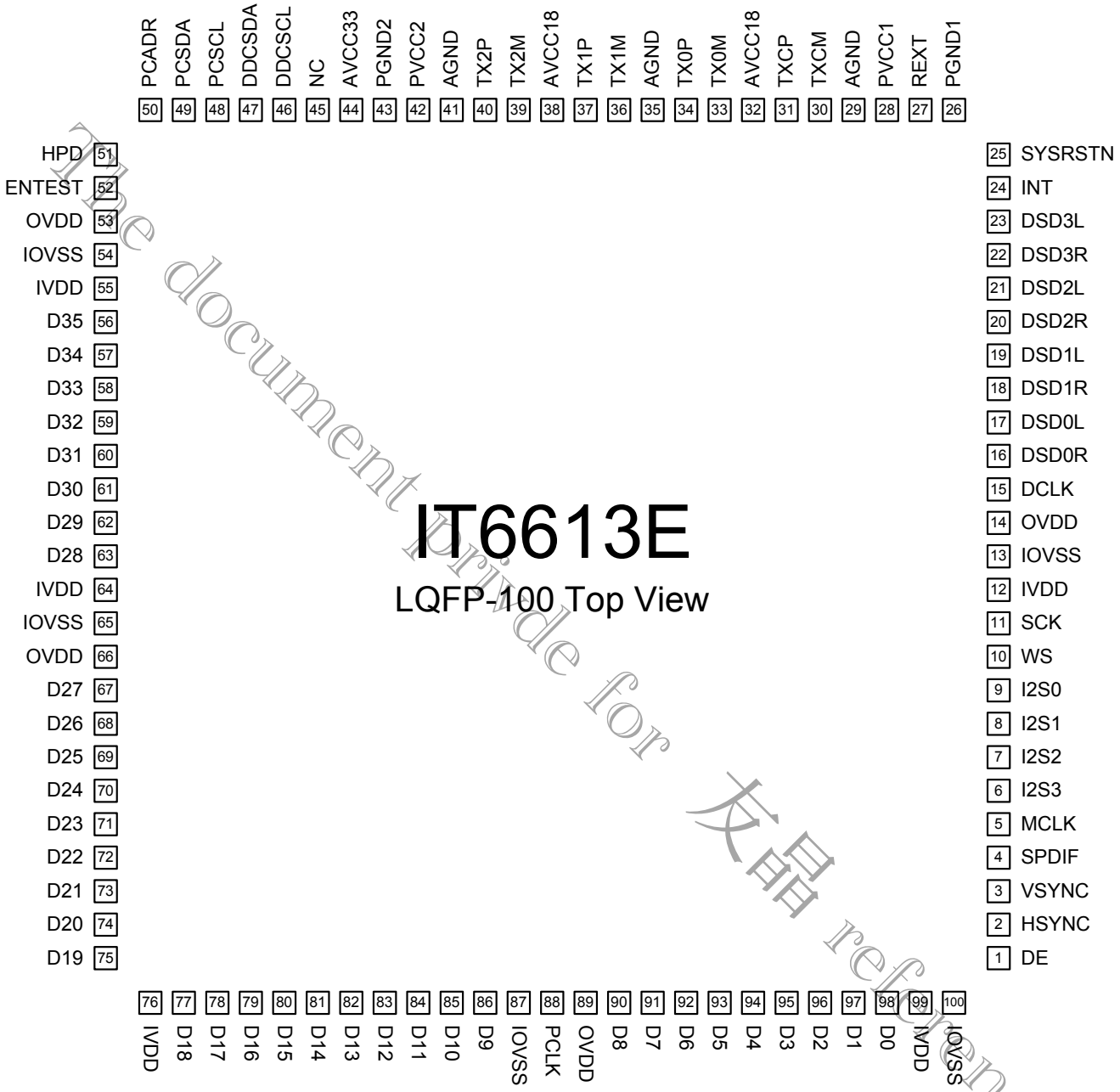


Figure 1. IT6613 pin diagram

Pin Description

Digital Video Input Pins

Pin Name	Direction	Description	Type	Pin No.
D[35:0]	Input	Digital video input pins.	LVTTL	56-63, 67-75, 77-86, 90-98
DE	Input	Data enable	LVTTL	1
HSYNC	Input	Horizontal sync. signal	LVTTL	2
VSYNC	Input	Vertical sync. signal	LVTTL	3
PCLK	Input	Input data clock	LVTTL	88

Digital Audio Input Pins

Pin Name	Direction	Description	Type	Pin No.
MCLK	Input	Audio master clock input	LVTTL	5
SCK	Input	I2S serial clock input	LVTTL	11
WS	Input	I2S word select input	LVTTL	10
I2S0	Input	I2S serial data input	LVTTL	9
I2S1	Input	I2S serial data input	LVTTL	8
I2S2	Input	I2S serial data input	LVTTL	7
I2S3	Input	I2S serial data input	LVTTL	6
SPDIF	Input	S/PDIF audio input	LVTTL	4
DCLK	Input	DSD Serial audio clock input	LVTTL	15
DSD0R	Input	DSD Serial Right CH0 data input	LVTTL	16
DSD0L	Input	DSD Serial Left CH0 data input	LVTTL	17
DSD1R	Input	DSD Serial Right CH1 data input	LVTTL	18
DSD1L	Input	DSD Serial Left CH1 data input	LVTTL	19
DSD2R	Input	DSD Serial Right CH2 data input	LVTTL	20
DSD2L	Input	DSD Serial Left CH2 data input	LVTTL	21
DSD3R	Input	DSD Serial Right CH3 data input	LVTTL	22
DSD3L	Input	DSD Serial Left CH3 data input	LVTTL	23

Programming Pins

Pin Name	Direction	Description	Type	Pin No.
INT#	Output	Interrupt output. Default active-low (5V-tolerant)	LVTTL	24
SYSRSTN	Input	Hardware reset pin. Active LOW (5V-tolerant)	Schmitt	25
DDCSCL	I/O	I^2C Clock for DDC (5V-tolerant)	Schmitt	46
DDCSDA	I/O	I^2C Data for DDC (5V-tolerant)	Schmitt	47

PCSCL	Input	Serial Programming Clock for chip programming (5V-tolerant)	Schmitt	48
PCSDA	I/O	Serial Programming Data for chip programming (5V-tolerant)	Schmitt	49
PCADR	Input	Serial programming device address select	LVTTL	50
HPD	Input	Hot Plug Detection (5V-tolerant)	LVTTL	51
ENTEST	Input	Must be tied low via a resistor.	LVTTL	52
NC		Could be left unconnected		45

HDMI front-end interface pins

Pin Name	Direction	Description	Type	Pin No.
TX2P	Analog	HDMI Channel 2 positive output	TMDS	40
TX2M	Analog	HDMI Channel 2 negative output	TMDS	39
TX1P	Analog	HDMI Channel 1 positive output	TMDS	37
TX1M	Analog	HDMI Channel 1 negative output	TMDS	36
TX0P	Analog	HDMI Channel 0 positive output	TMDS	34
TX0M	Analog	HDMI Channel 0 negative output	TMDS	33
TXCP	Analog	HDMI Clock Channel positive output	TMDS	31
TXCM	Analog	HDMI Clock Channel negative output	TMDS	30
REXT	Analog	External resistor for setting TMDS output level. Default tied to AVCC18 via a 698-Ohm SMD resistor.	Analog	27

Power/Ground Pins

Pin Name	Description	Type	Pin No.
IVDD	Digital logic power (1.8V)	Power	12, 55, 64, 76, 99
OVDD	I/O Pin power (3.3V)	Power	14, 53, 66, 89
IOVSS	Digital logic and I/O pin common ground	Ground	13, 54, 65, 87, 100
AVCC18	HDMI analog frontend power (1.8V)	Power	32, 38
AVCC33	HDMI analog frontend power (3.3V)	Power	44
AGND	HDMI analog frontend ground	Ground	29, 35, 41
PVCC1	HDMI core PLL power (1.8V)	Power	28
PGND1	HDMI core PLL ground	Ground	26
PVCC2	Filter PLL power (1.8V)	Power	42
PGND2	Filter PLL ground	Ground	43

Functional Description

The IT6613 is the 3nd generation HDMI transmitter and provides complete solutions for HDMI v1.4 Source systems, supporting processing and transmission of Deep Color video and state-of-the-art digital audio such as DTS-HD and Dolby TrueHD. The IT6613 supports color depths of 10 bits and 12 bits up to 1080p. Advanced processing algorithms are employed to optimize the performance of video processing such as color space conversion and up/down sampling. The functional block digram of the IT6613 is shown in Figure 1, which describes clearly the data flow.

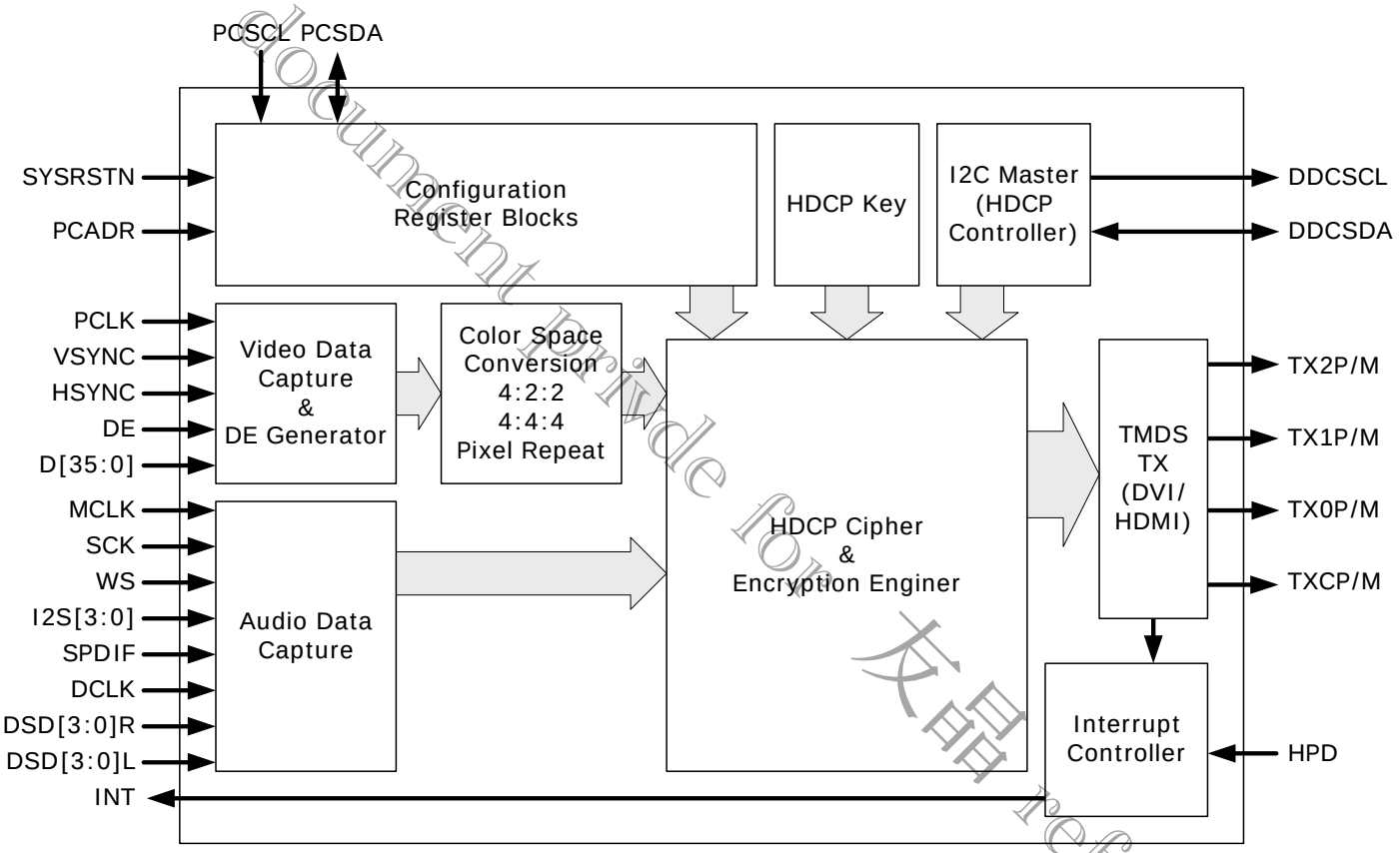


Figure 2. Functional block diagram of IT6613

Video Data Processing Flow

Figure 3 depicts the video data processing flow. For the purpose of retaining maximum flexibility, most of the block enablings and path bypassings are controlled through register programming. Please refer to IT6613 Programming Guide for detailed and precise descriptions.

As can be seen from Figure 3, the first step of video data processing is to prepare the video data (Data), data enable signal (DE), video clock (Clock), horizontal sync and vertical sync signals (H/VSYNC). While the video data and video clock are always readily available from input pins, the preparation of the data enable and sync signals require special extraction process (Embedded Ctrl.

Signals Extraction & DE Generator) depending on the format of input video data.

All the data then undergo a series of video processing including YCbCr up/down-sampling, color-space conversion and dithering. Depending on the selected input and output video formats, different processing blocks are either enabled or bypassed via register control. For the sake of flexibility, this is all done in software register programming. Therefore, extra care should be taken in keeping the selected input-output format combination and the corresponding video processing block selection. Please refer to the IT6613 Programming Guide for suggested register setting.

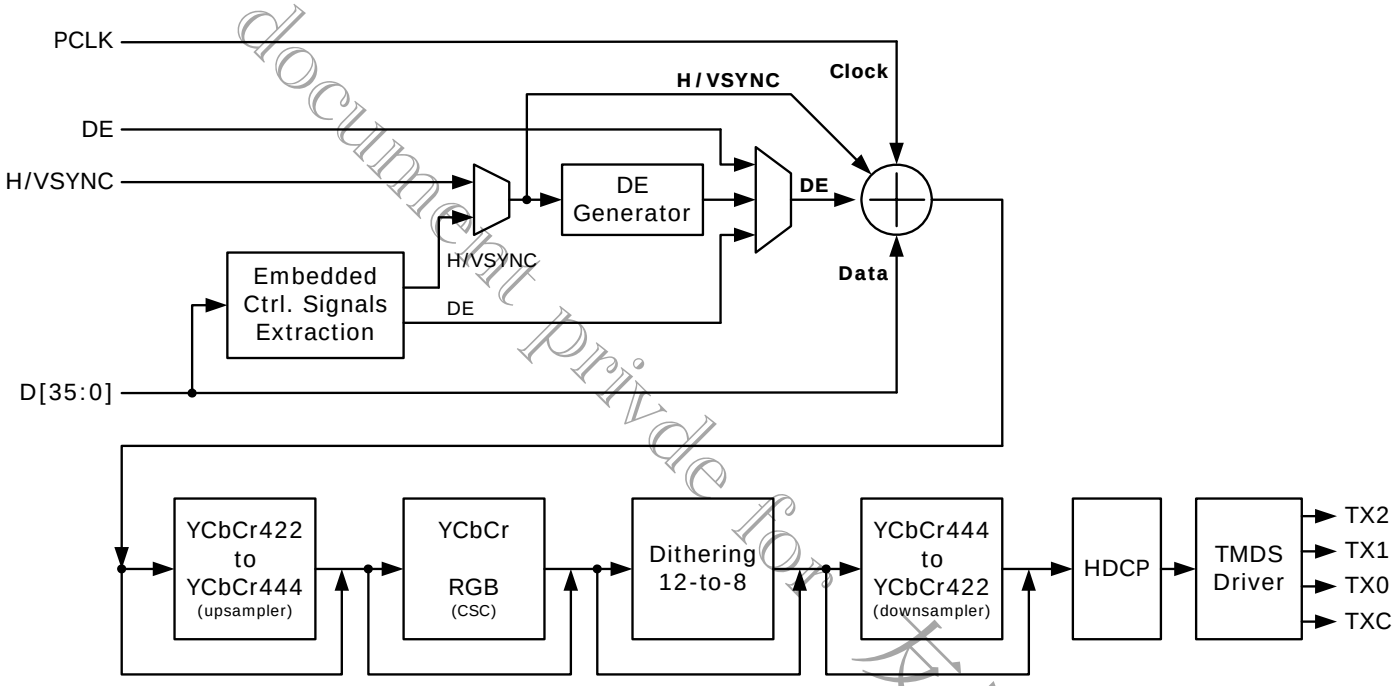


Figure 3. Video data processing flow of the IT6613

Designated as D[35:0], the input video data could take on bus width of 8 bits to 36 bits. This input interface could be configured to support various data formats as listed in Table 1.

All the major video processings in the IT6613 are done in 14 bits per channel in order to minimize rounding errors and other computational residuals that occur during processing. General description of block functions is as follows:

Extraction of embedded control signals (Embedded Ctrl. Signals Extraction)

Input video formats with only embedded sync signals rely on this block to derive the proper Hsync, Vsync and DE signals. Specifically, CCIR-656 video streams includes Start of Active Video (SAV) and End of Active Video (EAV) that this block uses to extract the required control signals.

Generation of data enable signal (DE Generator)

DE signal defines the region of active video data. In cases where the video decoders supply no such

DE signals to the IT6613, this block is used to generate appropriate DE signal from Hsync, Vsync and Clock.

Upsampling (YCbCr422 to YCbCr444)

In cases where input signals are in YCbCr 4:2:2 format and output is selected as 4:4:4, this block is enabled to do the upsampling. Well-designed signal filtering is employed to avoid visible artifacts generated during upsampling.

Bi-directional Color Space Conversion (YCbCr ↔ RGB)

Many video decoders only offer YCbCr outputs, while DVI 1.0 supports only RGB color space. In order to offer full compatibility between various Source and Sink combination, this block offers bi-directional RGB ↔ YCbCr color space conversion (CSC). To provide maximum flexibility, the maxtrix coefficients of the CSC engine in the IT6613 are fully programmable. Users could elect to employ their preferred conversion formula.

Dithering (Dithering 12-to-8)

For outputing to the 8-bits-per-channel formats, decimation from 12 bits to 8 bits is required. This block performs the necessary dithering for decimation to prevent visible artifacts from appearing.

Downsampling (YCbCr444 to YCbCr422)

In cases where input signals are in YCbCr 4:4:4 format and output is selected as YCbCr 4:2:2, this block is enabled to do the downsampling. Well-designed signal filtering is employed to avoid visible artifacts generated during downsampling.

HDCP engine (HDCP)

The HDCP engine in the IT6613 handles all the processing requried by HDCP mechanism in hardware. Software intervention is not necessary except checking for revocation. Preprogrammed HDCP keys are also embedded in the IT6613. Users need not worry about the purchasing and management of the HDCP keys.

TMDS driver (TMDS Driver)

The final step of the data processing flow is TMDS serializer. The TMDS driver serializes the input parallel data and drive out the proper electrical signals to the HDMI cable. The output current level is controlled through connecting a precision resistor of proper value to Pin 27 (REXT).

Supported Input Video Formats

The IT6613 supports deep-color video of 30-bit (10-bit per color) and 36-bit (12-bit per color). At the maximum resolution and bit depth, namely 36-bit/1080p, the TMDS data rate at the link is as high as 2.25Gbps. Table 1 lists the input video formats supported by the IT6613.

				Input Pixel Clock Frequency (MHz)							
Color Space	Video Format	Bus Width	Hsync/ Vsync	480i	480p	XGA	720p	1080i	SXGA	1080p	UXGA
RGB	4:4:4	24	Separate	13.5	27	65	74.25	74.25	108	148.5	162
		30/36		13.5	27	65	74.25	74.25	108	148.5	
		12/15/18	Separate	13.5	27	65	74.25	74.25			
YCbCr	4:4:4	24	Separate	13.5	27	65	74.25	74.25	108	148.5	162
		30/36		13.5	27	65	74.25	74.25	108	148.5	
		12/15/18	Separate	13.5	27	65	74.25	74.25			
	4:2:2	16/20/24	Separate	13.5	27		74.25	74.25		148.5	
			Embedded	13.5	27		74.25	74.25		148.5	
		8/10/12	Separate	27	54		148.5	148.5			
			Embedded	27	54		148.5	148.5			

Table 1. Input video formats supported by the IT6613

Notes:
1. Table cells that are left blanks are those format combinations that are not supported by the IT6613.
2. Input channel number is defined by the way the three color components (either R, G & B or Y, Cb & Cr) are arranged. Refer to Video Data Bus Mappings for better understanding.
3. Embedded sync signals are defined by CCIR-656 standard, using SAV/EAV sequences of FF, 00, 00, XY.

Supported 3D Formats

The IT6604 supports all the HDMI 1.4a 3D mandatory formats and most optional 3D formats including

- 1920x1080P@23.98/24/30Hz -- Framing Packing
- 1920x1080P@23.98/24/30Hz -- Top-and-Bottom
- 1920x1080i @50/59.94/60Hz -- Side-by-Side (Half)
- 1280x 720P@50/59.94/60Hz -- Framing Packing
- 1280x 720P@50/59.94/60Hz -- Top-and-Bottom

Audio Data Capture and Processing

The IT6613 supports all audio formats and interfaces specified by the HDMI Specification v1.3 through I^2S, S/PDIF and optional one-bit audio inputs.

I^2S

Four I^2S inputs are provided to support 8-channel uncompressed audio data at up to 192kHz sample rate. If the input audio data come with a multiple (master) clock, pin 5 (MCLK) takes in the clock to faciliate audio processing. Note that this is optional. By default IT6613 generates the MCLK internally to process the audio. Neither I^2S nor S/PDIF inputs requires MCLK input, coherent or not. However, if the user prefers inputing MCLK from external audio source, such configuration could be enabled through register setting. Refer to IT6613 Programming Guide for such setting. The supported

multiplied factor and sample frequency as well as the resultant MCLK frequencies are summarized in Table 2.

S/PDIF

The S/PDIF input supports 2-channel uncompressed PCM data (IEC 60958) or compressed multi-channel data (IEC 61937) at up to 192kHz. By default the clock of S/PDIF is carried within the datastream itself via coding. The IT6613 could also process the S/PDIF audio with coherent MCLK input as indicated in Table 2.

Multiple of audio sample frequency	Audio sample frequency						
	32kHz	44.1kHz	48kHz	88.2kHz	96kHz	176.4kHz	192kHz
128	4.096	5.645	6.144	11.290	12.288	22.579	24.576
256	8.192	11.290	12.288	22.579	24.576	45.158	49.152
512	16.384	22.579	24.576	45.158	49.152	90.317	98.304
1024	32.768	45.158	49.152	90.316	98.304	(180.634)	(196.608)

Table 2. Output MCLK frequencies (MHz) supported by the IT6613

Notes:

1. The MCLK frequencies in parenthesis are MCLK frequencies over 100MHz. These frequencies are implemented in the IT6613 and could be output through register setting as well. However, the I/O circuit of the MCLK pin does not guarantee to be operating at such a high frequency under normal operation conditions. In addition, few audio frontend ICs outputs such high MCLK frequencies. Therefore, using the MCLKs in parenthesis is strongly discouraged.

One-Bit Audio (DSD/SACD)

Direct stream digital (DSD) audio is an one-bit audio format which is prescribed by Super Audio CD (SACD) to provide superiore audio hearing experiences. The IT6613 provides dedicated input pins for DSD audio. A total of 8 data inputs are provided for right channels and left channels.

High-Bit-Rate Audio (HBR)

High-Bit-Rate Audio is also new to the HDMI standard. It is called upon by high-end audio system such as DTS-HD and Dolby TrueHD. No specific interface is defined by the HBR standard. The IT6613 supports HBR audio in two ways. One is to employ the four I^2S inputs simultaneously, where the original streaming DSD audio is broken into four parallel data streams before entering the IT6613. The other is to use the S/PDIF input port. Since the data rate here is as high as 98.304Mbps, a coherent MCLK is required in this application.

Audio Downsampling

Audio data can be down sampled in cases where the sinks only support audio with lower sampling rates. The IT6613 offers audio down-sampling of both a factor of two and a factor of four. Refer to Table 3 for supported down-samplings.

Down-sampling factor of 2	192kHz → 96kHz	176.4kHz → 88.2kHz
	96kHz → 48kHz	88.2kHz → 44.1kHz
Down-sampling factor of 4	192kHz → 48kHz	176.4kHz → 44.1kHz

Table 3. Audio down-samplings supported by the IT6613

Interrupt Generation

The system micro-controller should monitor the interrupt output by the IT6613 at PIN 24 (INT). The IT6613 generates an interrupt signal with events involving the following signals or situations:

1. A status change at Pin 51 (HPD), implicating hot-plug/unplug events
2. Receiver detection circuit in the IT6613 reports the presence or absence of an active termination at the TMDS Clock Channel (Register 0Eh[5], RxSENDetect)
3. DDC bus is hanged for whatever reasons
4. Audio FIFO overflows
5. HDCP authentication fails
6. Video data is stable or not

In an HDMI link the transmitter is responsible for initialize the link, which should be based on interrupt signal and appropriate register probing. Recommended flow is detailed in IT6613 Programming Guide. Simply put, the microcontroller should monitor the HPD status first. Upon valid HPD event, move on to check RxSENDetect register to see if the receiver chip is ready for further handshaking. When RxSENDetect is asserted, start reading EDID data through DDC channels and carry on the rest of the handshaking subsequently.

If the micro-controller makes no use of the interrupt signal as well as the above-mentioned status registers, the link establishment might fail. Please do follow the suggested initialization flow recommended in IT6613 Programming Guide.

Configuration and Function Control

The IT6613 includes two serial programming ports by default (i.e. with embedded HDCP keys): one for interfacing with micro-controller, the other for accessing the DDC channels of HDMI link. The serial programming interface for interfacing the micro-controller is a slave interface, comprising PCSCL (Pin 48) and PCSDA (Pin 49). The micro-controller uses this interface to monitor all the statuses and control all the functions. Two device addresses are available, depending on the input logic level of PCADR (Pin 50). If PCADR is pulled high by the user, the device address is **0x9A**. If pulled low, **0x98**.

The I^2C interface for accessing the DDC channels of the HDMI link is a master interface, comprising DDCSCL (Pin 46) and DDCSDA (Pin 47). the IT6613 uses this interface to read the EDID data and perform HDCP authentication protocol with the sink device over the HDMI cable.

For temporarily storing the acquired EDID data, the IT6613 embedded a dedicated FIFO of 32 bytes. The micro-controller may command the IT6613 to acquire 32 bytes of EDID information at a time, read them back and then continue to read the next 32 bytes until all neccessary EDID informations are retrieved.

The HDCP protocol of the IT6613 is completely implemented in hardware. No software intervention is needed except for revocation list checking. Various HDCP-related statuses are stored in HDCP registers for the reference of micro-controller. Refer to IT6613 Programming Guide for detailed register descriptions. The HDCP Standard also specifies a special message read protocol other than the standard I^2C protocol. See Figure 4 for checking HDCP port link integrity.

S=Start; R=Read; A=Ack; NA=No Ack; P=Stop

Figure 4. HDCP port link integrity message read

All serial programming interfaces conform to standard I^2C transactions and operate at up to 100kHz.

Electrical Specifications

Absolute Maximum Ratings

Symbol	Parameter	Min.	Typ	Max	Unit
IVDD	Core logic supply voltage	-0.3		2.5	V
OVDD	I/O pins supply voltage	-0.3		4.0	V
AVCC18	HDMI analog frontend supply voltage	-0.3		2.5	V
AVCC33	HDMI analog frontend supply voltage	-0.3		4.0	V
PVCC1	HDMI core PLL supply voltage	-0.3		2.5	V
PVCC2	Filter PLL supply voltage	-0.3		2.5	V
V_I	Input voltage	-0.3		OVDD+0.3	V
V_O	Output voltage	-0.3		OVDD+0.3	V
T_J	Junction Temperature			125	°C
T_{STG}	Storage Temperature	-65		150	°C
ESD_HB	Human body mode ESD sensitivity	2000			V
ESD_MM	Machine mode ESD sensitivity	200			V

Notes:
1. Stresses above those listed under Absolute Maximum Ratings might result in permanent damage to the device.
2. Refer to Functional Operation Conditions for normal operation.

Functional Operation Conditions

Symbol	Parameter	Min.	Typ	Max	Unit
IVDD	Core logic supply voltage	1.62	1.8	1.98	V
OVDD	I/O pins supply voltage	2.97	3.3	3.63	V
AVCC18	HDMI analog frontend supply voltage	1.71	1.8	1.89	V
AVCC33	HDMI analog frontend supply voltage	2.97	3.3	3.63	V
PVCC1	HDMI core PLL supply voltage	1.62	1.8	1.98	V
PVCC2	Filter PLL supply voltage	1.62	1.8	1.98	V
$V_{CCNOISE}$	Supply noise			100	mV_{pp}
T_A	Ambient temperature	0	25	70	°C
Θ_{ja}	Junction to ambient thermal resistance				°C/W

Notes:
1. AVCC18, AVCC33, PVCC1 and PVCC2 should be regulated.
2. See System Design Consideration for supply decoupling and regulation.

Operation Supply Current Specification

Symbol	Parameter	TMDSCLK	Typ	Max	Unit
I_{IVDD_OP}	IVDD current under normal operation	27MHz	29	32	mA
		74.25MHz	69	76	mA
		148.5MHz	113	127	mA
		222.75MHz	138	154	mA
I_{OVDD_OP}	OVDD current under normal operation	27MHz	1	1	mA
		74.25MHz	1	1	mA
		148.5MHz	1	1	mA
		222.75MHz	1	1	mA
I_{AVCC18_OP}	AVCC18 current under normal operation	27MHz	35	38	mA
		74.25MHz	36	40	mA
		148.5MHz	38	43	mA
		222.75MHz	41	45	mA
I_{AVCC33_OP}	AVCC33 current under normal operation	27MHz	1	1	mA
		74.25MHz	1	1	mA
		148.5MHz	1	1	mA
		222.75MHz	1	1	mA
I_{PVCC1_OP}	PVCC1 current under normal operation	27MHz	2	2	mA
		74.25MHz	3	3	mA
		148.5MHz	5	6	mA
		222.75MHz	9	10	mA
I_{PVCC2_OP}	PVCC2 current under normal operation	27MHz	2	2	mA
		74.25MHz	3	3	mA
		148.5MHz	6	6	mA
		222.75MHz	8	8	mA
PW_{TOTAL_OP}	Total power consumption under normal operation[3]	27MHz	129	154	mW
		74.25MHz	206	249	mW
		148.5MHz	298	368	mW
		222.75MHz	359	437	mW

Notes:
1. Typ: OVDD=AVCC33=3.3V, IVDD=AVCC18=PVCC1=PVCC2=1.8V
   Max: OVDD=AVCC33=3.6V, IVDD=AVCC18=PVCC1=PVCC2=1.98V
2. TMDSCLK refer to the differential clock
3. TMDSCLK=27MHz: 480p with 48kHz/8-channel audio,
   TMDSCLK=74.25MHz: 1080i with 192kHz/8-channel audio,
   TMDSCLK=148.5MHz: 1080p with 192kHz/8-channel audio,
   TMDSCLK=222.75MHz: 1080p**@36-bit Deep Color** with 192kHz/8-channel audio
4. PW_{TOTAL_OP} are calculated by multiplying the supply currents with their corresponding supply voltage and summing up all the items.

DC Electrical Specification

Under functional operation conditions

Symbol	Parameter	Pin Type	Conditions	Min.	Typ	Max	Unit
V_{IH}	Input high voltage[1]	LVTTL		2.0			V
V_{IL}	Input low voltage[1]	LVTTL				0.8	V
V_T	Switching threshold[1]	LVTTL			1.5		V
V_{T-}	Schmitt trigger negative going threshold voltage[1]	Schmitt		0.8	1.1		V
V_{T+}	Schmitt trigger positive going threshold voltage[1]	Schmitt			1.6	2.0	V
V_{OL}	Output low voltage[1]	LVTTL	I_{OL}=2~16mA			0.4	
V_{OH}	Output high voltage[1]	LVTTL	I_{OH}=-2~-16mA	2.4			
I_{IN}	Input leakage current[1]	all	V_{IN}=5.5V or 0		±5		μA
I_{OZ}	Tri-state output leakage current[1]	all	V_{IN}=5.5V or 0		±10		μA
I_{OL}	Serial programming output sink current[2]	Schmitt	V_{OUT}=0.2V	4		16	mA
V_{swing}	TMDS output single-ended swing[3]	TMDS	R_{LOAD}=50Ω V_{LOAD}=3.3V R_{EXT}=698Ω	400		600	mV
I_{OFF}	Single-ended standby output current[3]	TMDS	V_{OUT}=0			10	μA

Notes:

1. Guaranteed by I/O design.
2. The serial programming output ports are not real open-drain drivers. Sink current is guaranteed by I/O design under the condition of driving the output pin with 0.2V. In a real serial programming environment, multiple devices and pull-up resistors could be present on the same bus, rendering the effective pull-up resistance much lower than that specified by the I^2C Standard. When set at maximum current, the serial programming output ports of the IT6613 are capable of pulling down an effective pull-up resistance as low as 500Ω connected to 5V termination voltage to the standard I^2C V_{IL}. When experiencing insufficient low level problem, try setting the current level to higher than default. Refer to IT6613 Programming Guide for proper register setting.
3. Internal source turned off. Limits defined by HDMI Specifications v1.3a

Audio AC Timing Specification

Under functional operation conditions

Symbol	Parameter	Conditions	Min.	Typ	Max	Unit
F_{S_I2S}	I^2S sample rate	Up to 8 channels	32		192	kHz
F_{S_SPDIF}	S/PDIF sample rate	2 channels	32		192	kHz

Video AC Timing Specification

Under functional operation conditions

Symbol	Parameter	Conditions	Min.	Typ	Max	Unit
T_{pixel}	PCLK pixel clock period[1]	Single-edged clocking	6		40	ns
F_{pixel}	PCLK pixel clock frequency[1]		25		162	MHz
T_{CDE}	PCLK dual-edged clock period[2]	Dual-edged clocking	8.88		40	ns
F_{CDE}	PCLK dual-edged clock frequency[2]		25		82	MHz
T_{PDUTY}	PCLK clock duty cycle		40%		60%	
T_{PJ}	PCLK worst-case jitter				1.0	ns
T_S	Video data setup time[3]	Single-edged clocking	1.0		-	ns
T_H	Video data hold time[3]		0.5		-	ns
T_{SDE}	Video data setup time[3]	Dual-edged clocking	1.0		-	ns
T_{HDE}	Video data hold time[3]		0.5		-	ns

Notes:

1. Fpixel is the inverse of Tpixel. Operating frequency range is given here while the actual video clock frequency should comply with all video timing standards. Refer to Table 1 for supported video timings and corresponding pixel frequencies.
2. 12-bit dual-edged clocking is supported up to 74.5MHz of PCLK frequency, which covers 720p/1080i.
3. All setup time and hold time specifications are with respect to the latching edge of PCLK selected by the user through register programming.

Video Data Bus Mappings

The IT6613 supports various output data mappings and formats, including those with embedded control signals only. Corresponding register setting is to be taken care of for any chosen input data mappings. Refer to IT6613 Programming Guide for detailed instruction.

Color Space	Video Format	Bus Width	H/Vsync	Clocking	Table
RGB	4:4:4	24/30/36	Seperate	1X	5
		12/15/18	Seperate	Dual-edged	10
		24/30/36	Seperate	0.5X, Dual-edged	5
YCbCr	4:4:4	24/30/36	Seperate	1X	5
		12/15/18	Seperate	Dual-edged	10
		24/30/36	Seperate	0.5X, Dual-edged	5
	4:2:2	16/20/24	Seperate	1X	6
			Embedded	1X	7
		8/10/12	Seperate	2X	9
			Embedded	2X	8

Table 4. Output video format supported by the IT6613

RGB 4:4:4 and YCbCr 4:4:4 with Separate Syncs

	RGB			YCbCr		
Pin Name	36-bit	30-bit	24-bit	36-bit	30-bit	24-bit
D0	B0	grounded	grounded	Cb0	grounded	grounded
D1	B1	grounded	grounded	Cb1	grounded	grounded
D2	B2	B0	grounded	Cb2	Cb0	grounded
D3	B3	B1	grounded	Cb3	Cb1	grounded
D4	B4	B2	B0	Cb4	Cb2	Cb0
D5	B5	B3	B1	Cb5	Cb3	Cb1
D6	B6	B4	B2	Cb6	Cb4	Cb2
D7	B7	B5	B3	Cb7	Cb5	Cb3
D8	B8	B6	B4	Cb8	Cb6	Cb4
D9	B9	B7	B5	Cb9	Cb7	Cb5
D10	B10	B8	B6	Cb10	Cb8	Cb6
D11	B11	B9	B7	Cb11	Cb9	Cb7
D12	G0	grounded	grounded	Y0	grounded	grounded
D13	G1	grounded	grounded	Y1	grounded	grounded
D14	G2	G0	grounded	Y2	Y0	grounded
D15	G3	G1	grounded	Y3	Y1	grounded
D16	G4	G2	G0	Y4	Y2	Y0
D17	G5	G3	G1	Y5	Y3	Y1
D18	G6	G4	G2	Y6	Y4	Y2
D19	G7	G5	G3	Y7	Y5	Y3
D20	G8	G6	G4	Y8	Y6	Y4
D21	G9	G7	G5	Y9	Y7	Y5
D22	G10	G8	G6	Y10	Y8	Y6
D23	G11	G9	G7	Y11	Y9	Y7
D24	R0	grounded	grounded	Cr0	grounded	grounded
D25	R1	grounded	grounded	Cr1	grounded	grounded
D26	R2	R0	grounded	Cr2	Cr0	grounded
D27	R3	R1	grounded	Cr3	Cr1	grounded
D28	R4	R2	R0	Cr4	Cr2	Cr0
D29	R5	R3	R1	Cr5	Cr3	Cr1
D30	R6	R4	R2	Cr6	Cr4	Cr2
D31	R7	R5	R3	Cr7	Cr5	Cr3
D32	R8	R6	R4	Cr8	Cr6	Cr4
D33	R9	R7	R5	Cr9	Cr7	Cr5
D34	R10	R8	R6	Cr10	Cr8	Cr6
D35	R11	R9	R7	Cr11	Cr9	Cr7
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE

Table 5. RGB & YCbCr 4:4:4 Mappings

These are the simplest formats, with a complete definition of every pixel in each clock period. Figure 5

and Figure 6 give two examples

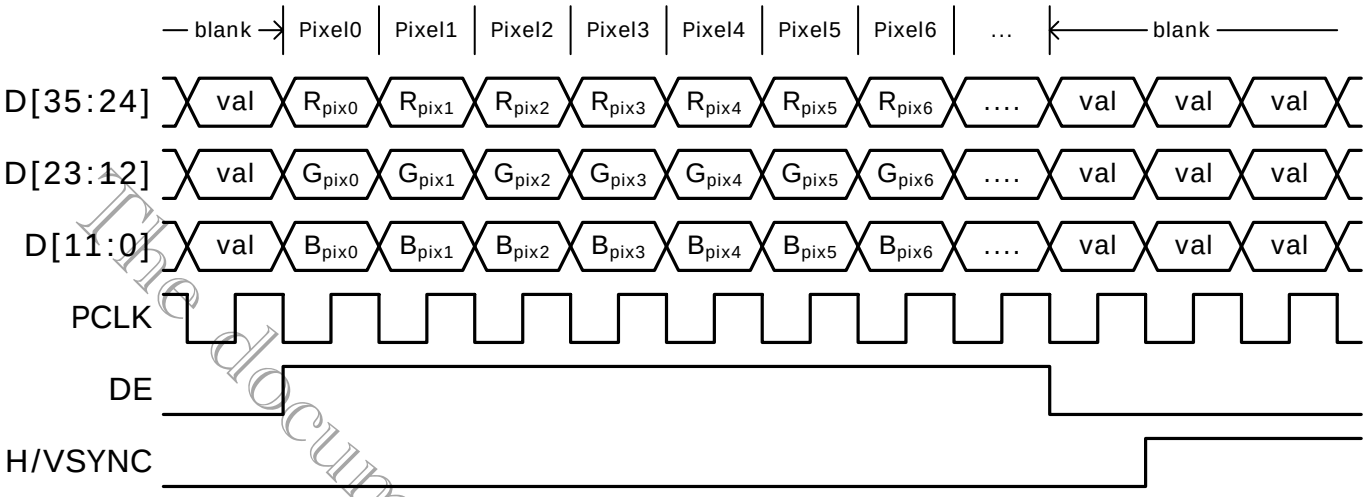


Figure 5. 36-bit RGB 4:4:4 Timing Diagram

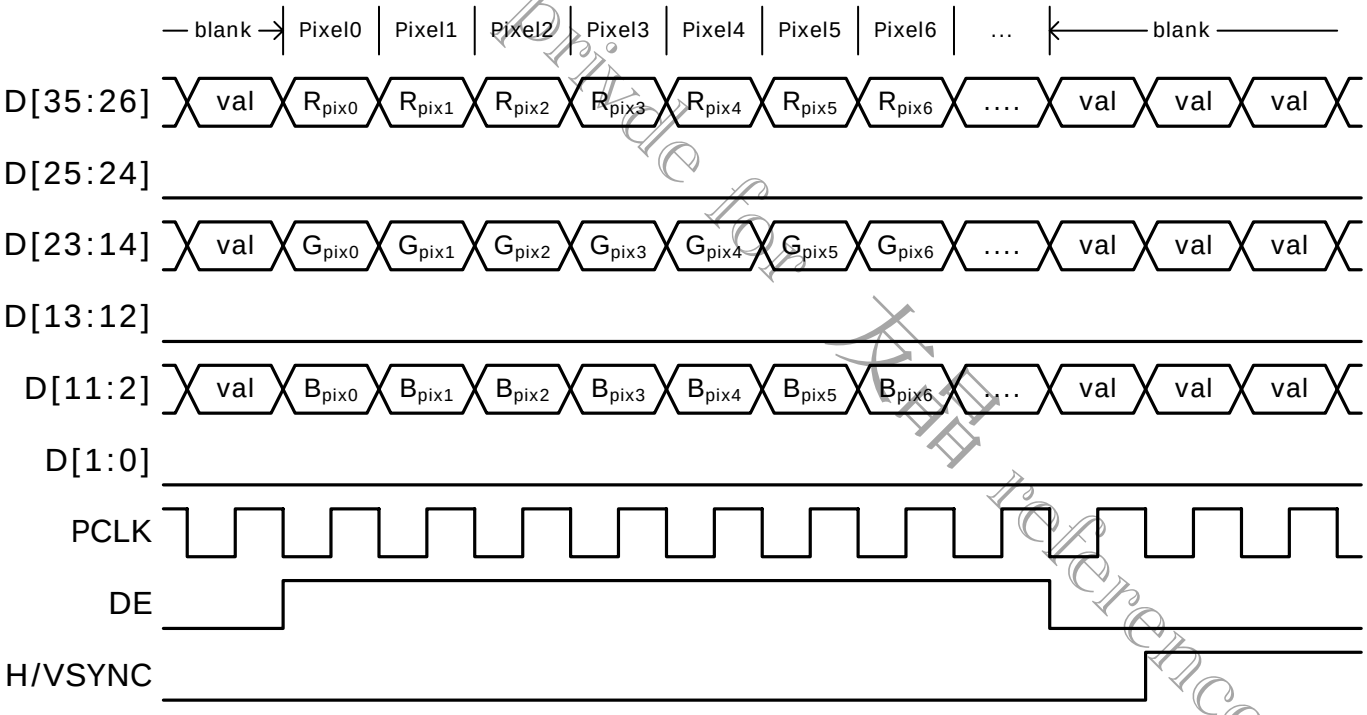


Figure 6. 30-bit RGB 4:4:4 Timing Diagram

YCbCr 4:2:2 with Separate Syncs

	24-bit		20-bit		16-bit	
Pin Name	Pixel#2N	Pixel#2N+1	Pixel#2N	Pixel#2N+1	Pixel#2N	Pixel#2N+1
D0	grounded	grounded	grounded	grounded	grounded	grounded
D1	grounded	grounded	grounded	grounded	grounded	grounded
D2	grounded	grounded	grounded	grounded	grounded	grounded
D3	grounded	grounded	grounded	grounded	grounded	grounded
D4	Y0	Y0	grounded	grounded	grounded	grounded
D5	Y1	Y1	grounded	grounded	grounded	grounded
D6	Y2	Y2	Y0	Y0	grounded	grounded
D7	Y3	Y3	Y1	Y1	grounded	grounded
D8	Cb0	Cr0	grounded	grounded	grounded	grounded
D9	Cb1	Cr1	grounded	grounded	grounded	grounded
D10	Cb2	Cr2	Cb0	Cr0	grounded	grounded
D11	Cb3	Cr3	Cb1	Cr1	grounded	grounded
D12	grounded	grounded	grounded	grounded	grounded	grounded
D13	grounded	grounded	grounded	grounded	grounded	grounded
D14	grounded	grounded	grounded	grounded	grounded	grounded
D15	grounded	grounded	grounded	grounded	grounded	grounded
D16	Y4	Y4	Y2	Y2	Y0	Y0
D17	Y5	Y5	Y3	Y3	Y1	Y1
D18	Y6	Y6	Y4	Y4	Y2	Y2
D19	Y7	Y7	Y5	Y5	Y3	Y3
D20	Y8	Y8	Y6	Y6	Y4	Y4
D21	Y9	Y9	Y7	Y7	Y5	Y5
D22	Y10	Y10	Y8	Y8	Y6	Y6
D23	Y11	Y11	Y9	Y9	Y7	Y7
D24	grounded	grounded	grounded	grounded	grounded	grounded
D25	grounded	grounded	grounded	grounded	grounded	grounded
D26	grounded	grounded	grounded	grounded	grounded	grounded
D27	grounded	grounded	grounded	grounded	grounded	grounded
D28	Cb4	Cr4	Cb2	Cr2	Cb0	Cr0
D29	Cb5	Cr5	Cb3	Cr3	Cb1	Cr1
D30	Cb6	Cr6	Cb4	Cr4	Cb2	Cr2
D31	Cb7	Cr7	Cb5	Cr5	Cb3	Cr3
D32	Cb8	Cr8	Cb6	Cr6	Cb4	Cr4
D33	Cb9	Cr9	Cb7	Cr7	Cb5	Cr5
D34	Cb10	Cr10	Cb8	Cr8	Cb6	Cr6
D35	Cb11	Cr11	Cb9	Cr9	Cb7	Cr7
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE

Table 6. Mappings of YCbCr 4:2:2 with separate syncs

YCbCr 4:2:2 format does not have one complete pixel for every clock period. Luminace channel (Y) is

given for every pixel, while the two chroma channels are given alternatively on every other clock period. The average bit amount of Y is twice that of Cb or Cr. Depending on the bus width, each component could take on different lengths. The DE period should contain an even number of clock periods. Figure 7 and Figure 8 give two timing examples.

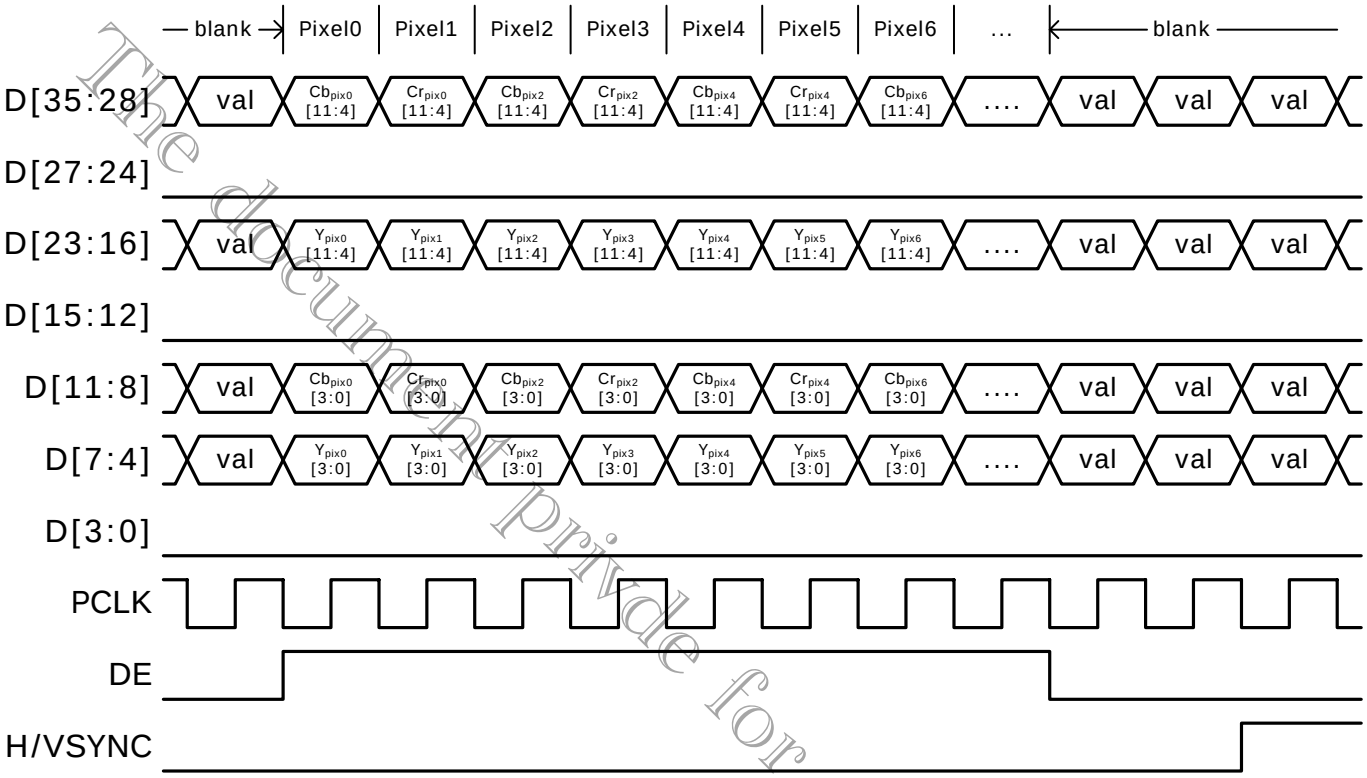


Figure 7. 24-bit YCbCr 4:2:2 with separate syncs

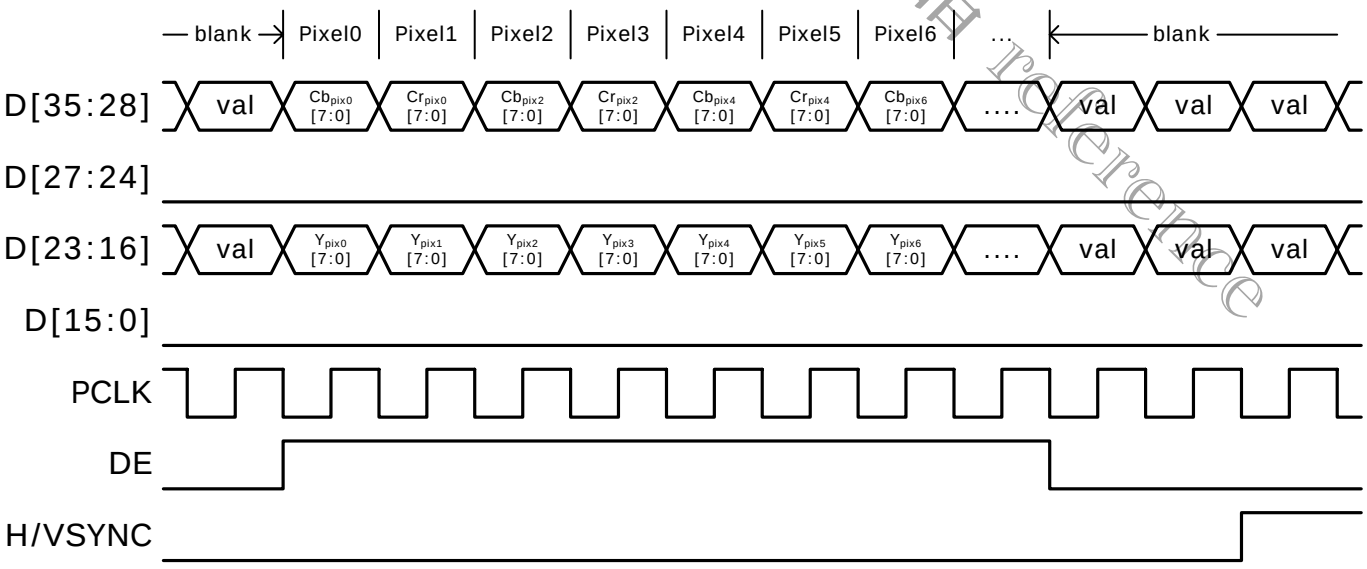


Figure 8. 16-bit YCbCr 4:2:2 with separate syncs

YCbCr 4:2:2 with Embedded Syncs

	24-bit		20-bit		16-bit	
Pin Name	Pixel#2N	Pixel#2N+1	Pixel#2N	Pixel#2N+1	Pixel#2N	Pixel#2N+1
D0	grounded	grounded	grounded	grounded	grounded	grounded
D1	grounded	grounded	grounded	grounded	grounded	grounded
D2	grounded	grounded	grounded	grounded	grounded	grounded
D3	grounded	grounded	grounded	grounded	grounded	grounded
D4	Y0	Y0	grounded	grounded	grounded	grounded
D5	Y1	Y1	grounded	grounded	grounded	grounded
D6	Y2	Y2	Y0	Y0	grounded	grounded
D7	Y3	Y3	Y1	Y1	grounded	grounded
D8	Cb0	Cr0	grounded	grounded	grounded	grounded
D9	Cb1	Cr1	grounded	grounded	grounded	grounded
D10	Cb2	Cr2	Cb0	Cr0	grounded	grounded
D11	Cb3	Cr3	Cb1	Cr1	grounded	grounded
D12	grounded	grounded	grounded	grounded	grounded	grounded
D13	grounded	grounded	grounded	grounded	grounded	grounded
D14	grounded	grounded	grounded	grounded	grounded	grounded
D15	grounded	grounded	grounded	grounded	grounded	grounded
D16	Y4	Y4	Y2	Y2	Y0	Y0
D17	Y5	Y5	Y3	Y3	Y1	Y1
D18	Y6	Y6	Y4	Y4	Y2	Y2
D19	Y7	Y7	Y5	Y5	Y3	Y3
D20	Y8	Y8	Y6	Y6	Y4	Y4
D21	Y9	Y9	Y7	Y7	Y5	Y5
D22	Y10	Y10	Y8	Y8	Y6	Y6
D23	Y11	Y11	Y9	Y9	Y7	Y7
D24	grounded	grounded	grounded	grounded	grounded	grounded
D25	grounded	grounded	grounded	grounded	grounded	grounded
D26	grounded	grounded	grounded	grounded	grounded	grounded
D27	grounded	grounded	grounded	grounded	grounded	grounded
D28	Cb4	Cr4	Cb2	Cr2	Cb0	Cr0
D29	Cb5	Cr5	Cb3	Cr3	Cb1	Cr1
D30	Cb6	Cr6	Cb4	Cr4	Cb2	Cr2
D31	Cb7	Cr7	Cb5	Cr5	Cb3	Cr3
D32	Cb8	Cr8	Cb6	Cr6	Cb4	Cr4
D33	Cb9	Cr9	Cb7	Cr7	Cb5	Cr5
D34	Cb10	Cr10	Cb8	Cr8	Cb6	Cr6
D35	Cb11	Cr11	Cb9	Cr9	Cb7	Cr7
HSYNC	embedded	embedded	embedded	embedded	embedded	embedded
VSYNC	embedded	embedded	embedded	embedded	embedded	embedded
DE	embedded	embedded	embedded	embedded	embedded	embedded

Table 7. Mappings of YCbCr 4:2:2 with embedded syncs

Similar to YCbCr 4:2:2 with Separate Sync. The only difference is that the syncs are now non-explicit,

i.e. embedded. Bus width could be 16-bit, 20-bit or 24-bit. Figure 9 and Figure 10 give two timing examples

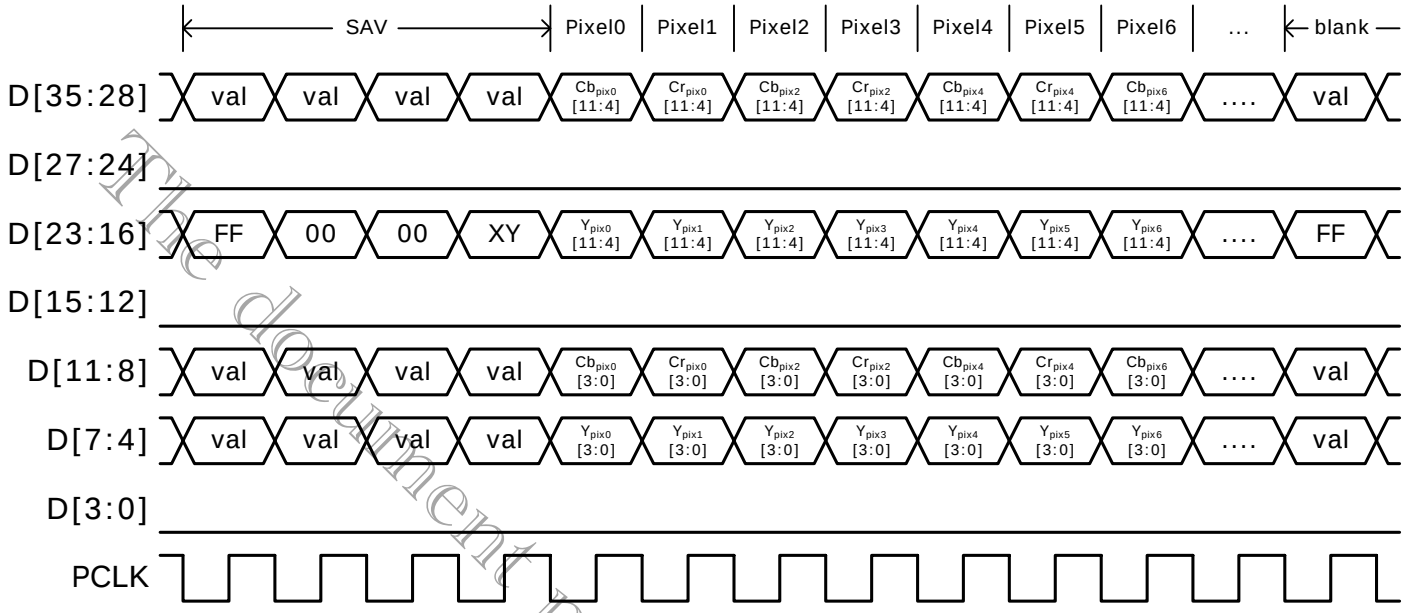


Figure 9. 24-bit YCbCr 4:2:2 with embedded syncs

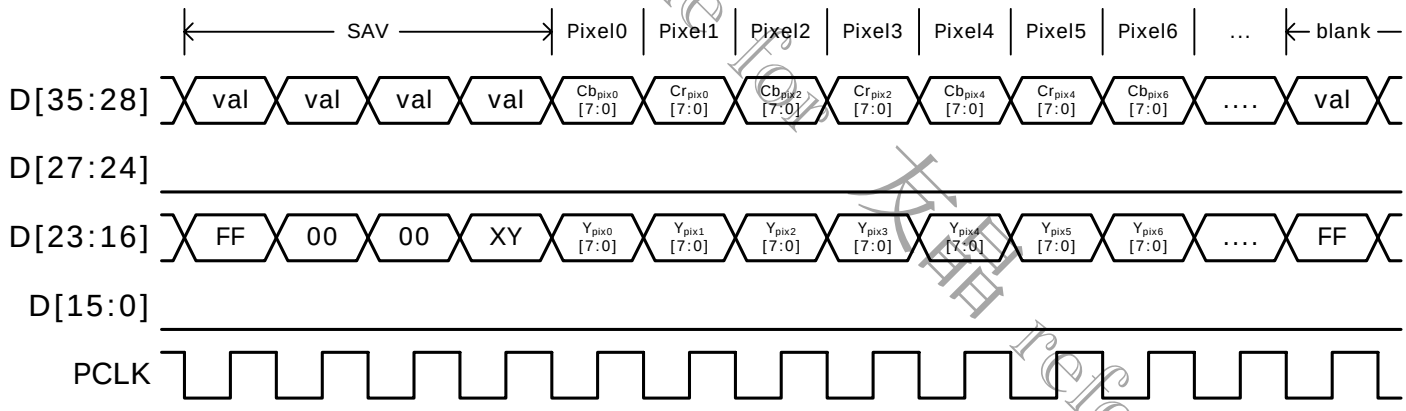


Figure 10. 16-bit YCbCr 4:2:2 with embedded syncs

CCIR-656 Format

	12-bit		10-bit		8-bit	
Pin Name	PCLK#2N	PCLK#2N+1	PCLK#2N	PCLK#2N+1	PCLK#2N	PCLK#2N+1
D0	grounded	grounded	grounded	grounded	grounded	grounded
D1	grounded	grounded	grounded	grounded	grounded	grounded
D2	grounded	grounded	grounded	grounded	grounded	grounded
D3	grounded	grounded	grounded	grounded	grounded	grounded
D4	C0	Y0	grounded	grounded	grounded	grounded
D5	C1	Y1	grounded	grounded	grounded	grounded
D6	C2	Y2	C0	Y0	grounded	grounded
D7	C3	Y3	C1	Y1	grounded	grounded
D8	grounded	grounded	grounded	grounded	grounded	grounded
D9	grounded	grounded	grounded	grounded	grounded	grounded
D10	grounded	grounded	grounded	grounded	grounded	grounded
D11	grounded	grounded	grounded	grounded	grounded	grounded
D12	grounded	grounded	grounded	grounded	grounded	grounded
D13	grounded	grounded	grounded	grounded	grounded	grounded
D14	grounded	grounded	grounded	grounded	grounded	grounded
D15	grounded	grounded	grounded	grounded	grounded	grounded
D16	C4	Y4	C2	Y2	C0	Y0
D17	C5	Y5	C3	Y3	C1	Y1
D18	C6	Y6	C4	Y4	C2	Y2
D19	C7	Y7	C5	Y5	C3	Y3
D20	C8	Y8	C6	Y6	C4	Y4
D21	C9	Y9	C7	Y7	C5	Y5
D22	C10	Y10	C8	Y8	C6	Y6
D23	C11	Y11	C9	Y9	C7	Y7
D24	grounded	grounded	grounded	grounded	grounded	grounded
D25	grounded	grounded	grounded	grounded	grounded	grounded
D26	grounded	grounded	grounded	grounded	grounded	grounded
D27	grounded	grounded	grounded	grounded	grounded	grounded
D28	grounded	grounded	grounded	grounded	grounded	grounded
D29	grounded	grounded	grounded	grounded	grounded	grounded
D30	grounded	grounded	grounded	grounded	grounded	grounded
D31	grounded	grounded	grounded	grounded	grounded	grounded
D32	grounded	grounded	grounded	grounded	grounded	grounded
D33	grounded	grounded	grounded	grounded	grounded	grounded
D34	grounded	grounded	grounded	grounded	grounded	grounded
D35	grounded	grounded	grounded	grounded	grounded	grounded
HSYNC	grounded	grounded	grounded	grounded	grounded	grounded
VSYNC	grounded	grounded	grounded	grounded	grounded	grounded
DE	grounded	grounded	grounded	grounded	grounded	grounded

Table 8. Mappings of CCIR-656

The CCIR-656 format is yet another variation of the YCbCr formats. The bus width is further reduced

by half compared from the previous YCbCr 4:2:2 formats, to either 8-bit, 10-bit or 12-bit. To compensate for the halving of data bus, PCLK frequency is doubled. With the double-rate output clock, luminance channel (Y) and chroma channels (Cb or Cr) are alternated. Normally this mode is used only for 480i, 480p, 576i and 576p. The IT6613 supports CCIR-656 format of up to 720p or 1080i, with the doubled-rate clock running at 148.5MHz. CCIR-656 format supports embedded syncs only. Figure 11 and Figure 12 give two examples.

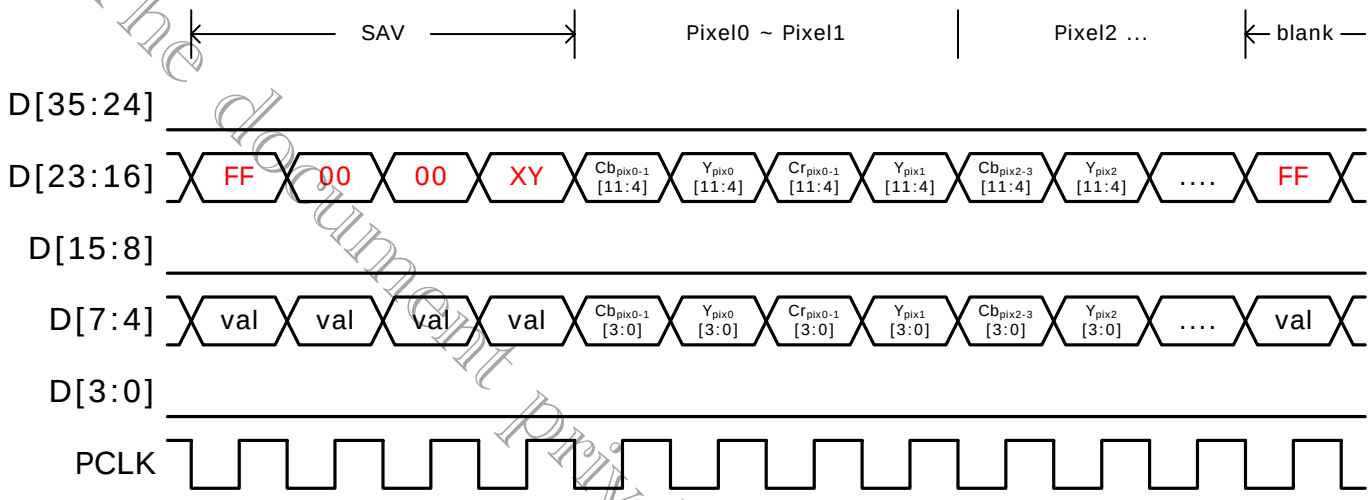


Figure 11. 12-bit CCIR-656

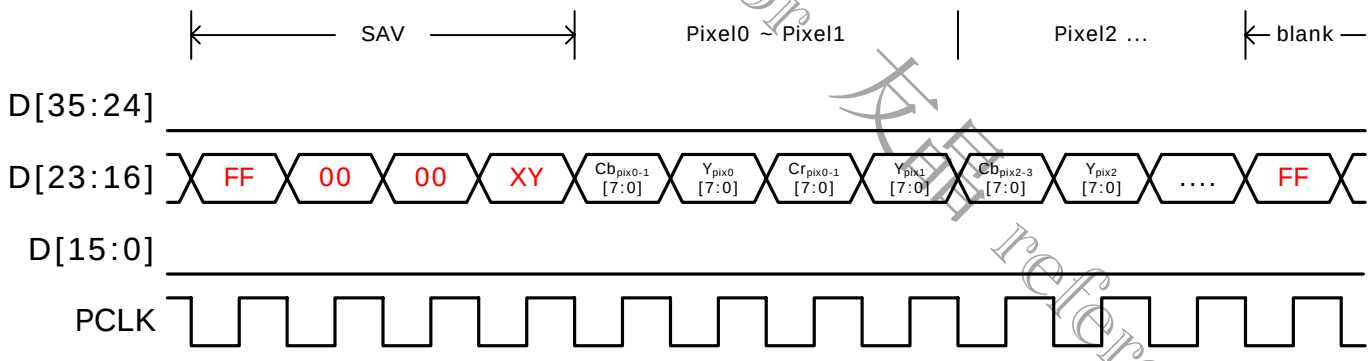


Figure 12. 8-bit CCIR-656

CCIR-656 + separate syncs

	12-bit		10-bit		8-bit	
Pin Name	PCLK#2N	PCLK#2N+1	PCLK#2N	PCLK#2N+1	PCLK#2N	PCLK#2N+1
D0	grounded	grounded	grounded	grounded	grounded	grounded
D1	grounded	grounded	grounded	grounded	grounded	grounded
D2	grounded	grounded	grounded	grounded	grounded	grounded
D3	grounded	grounded	grounded	grounded	grounded	grounded
D4	C0	Y0	grounded	grounded	grounded	grounded
D5	C1	Y1	grounded	grounded	grounded	grounded
D6	C2	Y2	C0	Y0	grounded	grounded
D7	C3	Y3	C1	Y1	grounded	grounded
D8	grounded	grounded	grounded	grounded	grounded	grounded
D9	grounded	grounded	grounded	grounded	grounded	grounded
D10	grounded	grounded	grounded	grounded	grounded	grounded
D11	grounded	grounded	grounded	grounded	grounded	grounded
D12	grounded	grounded	grounded	grounded	grounded	grounded
D13	grounded	grounded	grounded	grounded	grounded	grounded
D14	grounded	grounded	grounded	grounded	grounded	grounded
D15	grounded	grounded	grounded	grounded	grounded	grounded
D16	C4	Y4	C2	Y2	C0	Y0
D17	C5	Y5	C3	Y3	C1	Y1
D18	C6	Y6	C4	Y4	C2	Y2
D19	C7	Y7	C5	Y5	C3	Y3
D20	C8	Y8	C6	Y6	C4	Y4
D21	C9	Y9	C7	Y7	C5	Y5
D22	C10	Y10	C8	Y8	C6	Y6
D23	C11	Y11	C9	Y9	C7	Y7
D24	grounded	grounded	grounded	grounded	grounded	grounded
D25	grounded	grounded	grounded	grounded	grounded	grounded
D26	grounded	grounded	grounded	grounded	grounded	grounded
D27	grounded	grounded	grounded	grounded	grounded	grounded
D28	grounded	grounded	grounded	grounded	grounded	grounded
D29	grounded	grounded	grounded	grounded	grounded	grounded
D30	grounded	grounded	grounded	grounded	grounded	grounded
D31	grounded	grounded	grounded	grounded	grounded	grounded
D32	grounded	grounded	grounded	grounded	grounded	grounded
D33	grounded	grounded	grounded	grounded	grounded	grounded
D34	grounded	grounded	grounded	grounded	grounded	grounded
D35	grounded	grounded	grounded	grounded	grounded	grounded
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE

Table 9. Mappings of CCIR-656 + separate syncs

This format is not specified by CCIR-656. It's simply the previously mentioned CCIR-656 format plus

separate syncs. Figure 13 and Figure 14 give two examples

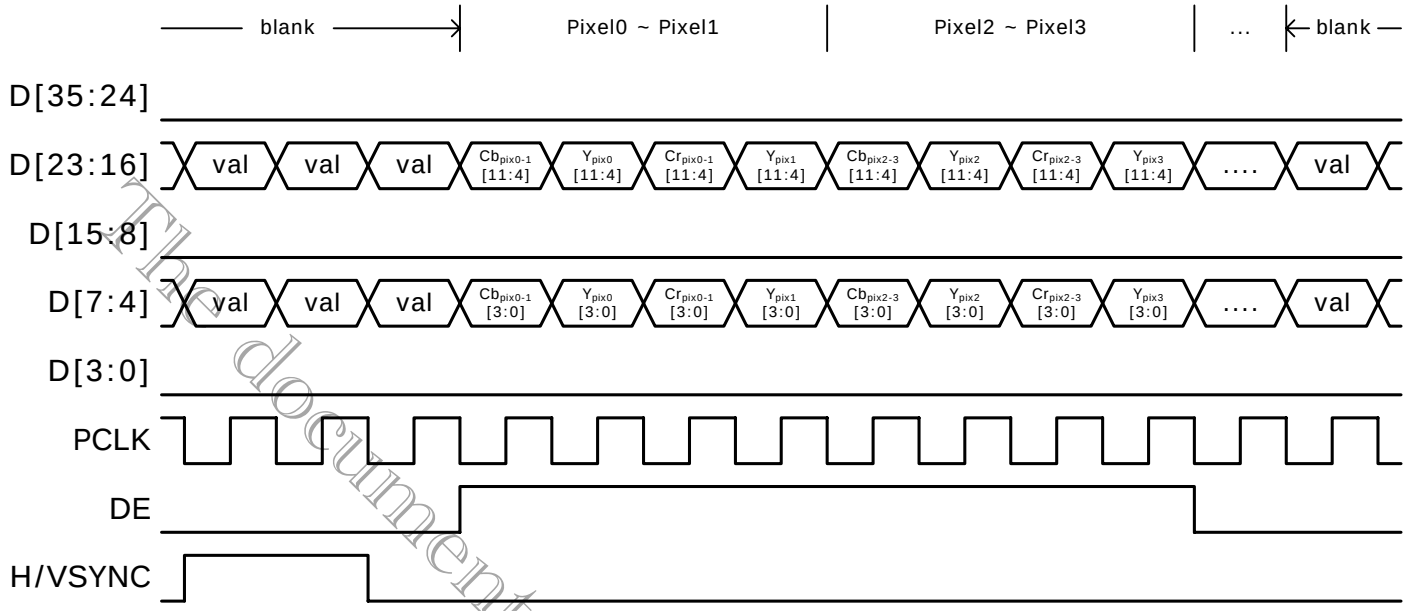


Figure 13. 12-bit CCIR-656 + separate syncs

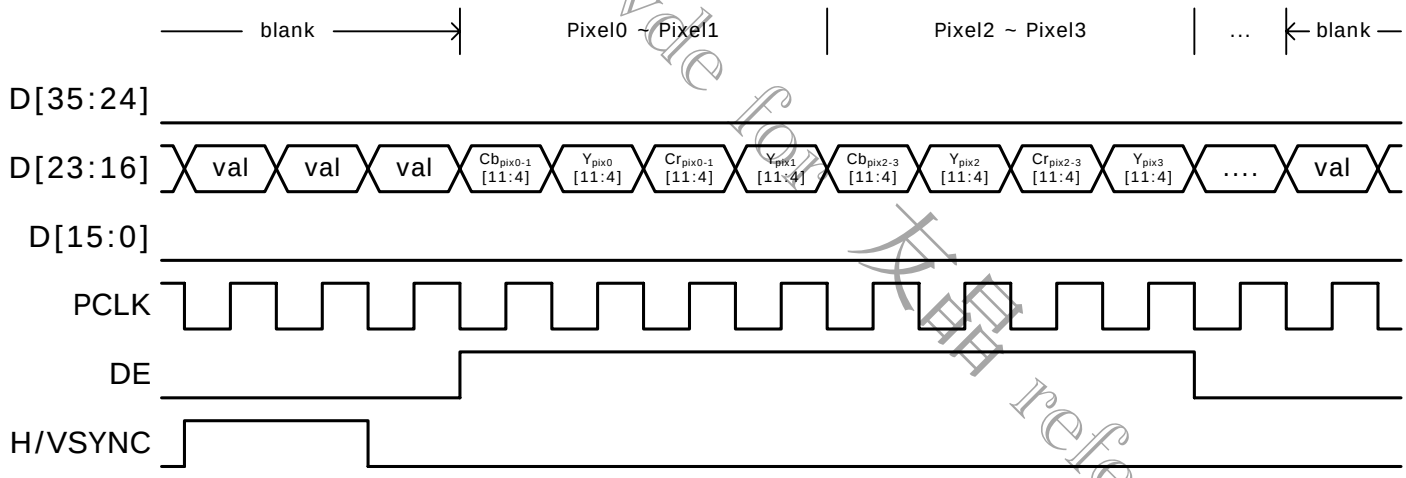


Figure 14. 8-bit CCIR-656 + separate syncs

24/15/18-bit RGB 4:4:4 and YCbCr 4:4:4 Using Dual-Edge Triggering

	RGB						YCbCr					
	18-bit		15-bit		12-bit		18-bit		15-bit		12-bit	
Pin Name	1st edge	2nd edge	1st edge	2nd edge	1st edge	2nd edge	1st edge	2nd edge	1st edge	2nd edge	1st edge	2nd edge
D0	B0	G6	gnded	gnded	gnded	gnded	Cb0	Y6	gnded	gnded	gnded	gnded
D1	B1	G7	gnded	gnded	gnded	gnded	Cb1	Y7	gnded	gnded	gnded	gnded
D2	B2	G8	B0	G5	gnded	gnded	Cb2	Y8	Cb0	Y5	gnded	gnded
D3	B3	G9	B1	G6	gnded	gnded	Cb3	Y9	Cb1	Y6	gnded	gnded
D4	B4	G10	B2	G7	B0	G4	Cb4	Y10	Cb2	Y7	Cb0	Y4
D5	B5	G11	B3	G8	B1	G5	Cb5	Y11	Cb3	Y8	Cb1	Y5
D6	B6	R0	B4	G9	B2	G6	Cb6	Cr0	Cb4	Y9	Cb2	Y6
D7	B7	R1	B5	R0	B3	G7	Cb7	Cr1	Cb5	Cr0	Cb3	Y7
D8	B8	R2	B6	R1	B4	R0	Cb8	Cr2	Cb6	Cr1	Cb4	Cr0
D9	B9	R3	B7	R2	B5	R1	Cb9	Cr3	Cb7	Cr2	Cb5	Cr1
D10	B10	R4	B8	R3	B6	R2	Cb10	Cr4	Cb8	Cr3	Cb6	Cr2
D11	B11	R5	B9	R4	B7	R3	Cb11	Cr5	Cb9	Cr4	Cb7	Cr3
D12	G0	R6	gnded	gnded	gnded	gnded	Y0	Cr6	gnded	gnded	gnded	gnded
D13	G1	R7	gnded	gnded	gnded	gnded	Y1	Cr7	gnded	gnded	gnded	gnded
D14	G2	R8	G0	R5	gnded	gnded	Y2	Cr8	Y0	Cr5	gnded	gnded
D15	G3	R9	G1	R6	gnded	gnded	Y3	Cr9	Y1	Cr6	gnded	gnded
D16	G4	R10	G2	R7	G0	R4	Y4	Cr10	Y2	Cr7	Y0	Cr4
D17	G5	R11	G3	R8	G1	R5	Y5	Cr11	Y3	Cr8	Y1	Cr5
D18	gnded	gnded	G4	R9	G2	R6	gnded	gnded	Y4	Cr9	Y2	Cr6
D19	gnded	gnded	gnded	gnded	G3	R7	gnded	gnded	gnded	gnded	Y3	Cr7
D20	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded
D21	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded
D22	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded
D23	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded
D24	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded
D25	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded
D26	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded
D27	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded
D28	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded
D29	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded
D30	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded
D31	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded
D32	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded
D33	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded
D34	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded
D35	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded	gnded
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE

Table 10. Mappings of 12/15/18-bit 4:4:4 dual-edge triggered

In this double-edge triggering mode, PCLK frequency remains at the nominal pixel clock rate. The halved data pins, however, run at a data rate double that of the nominal pixel clock rate. Each set of data are clocked out by the rising edge and the falling edge alternatively. Overall one complete pixel is output within one PCLK period. Figure 15 and Figure 16 give two examples.

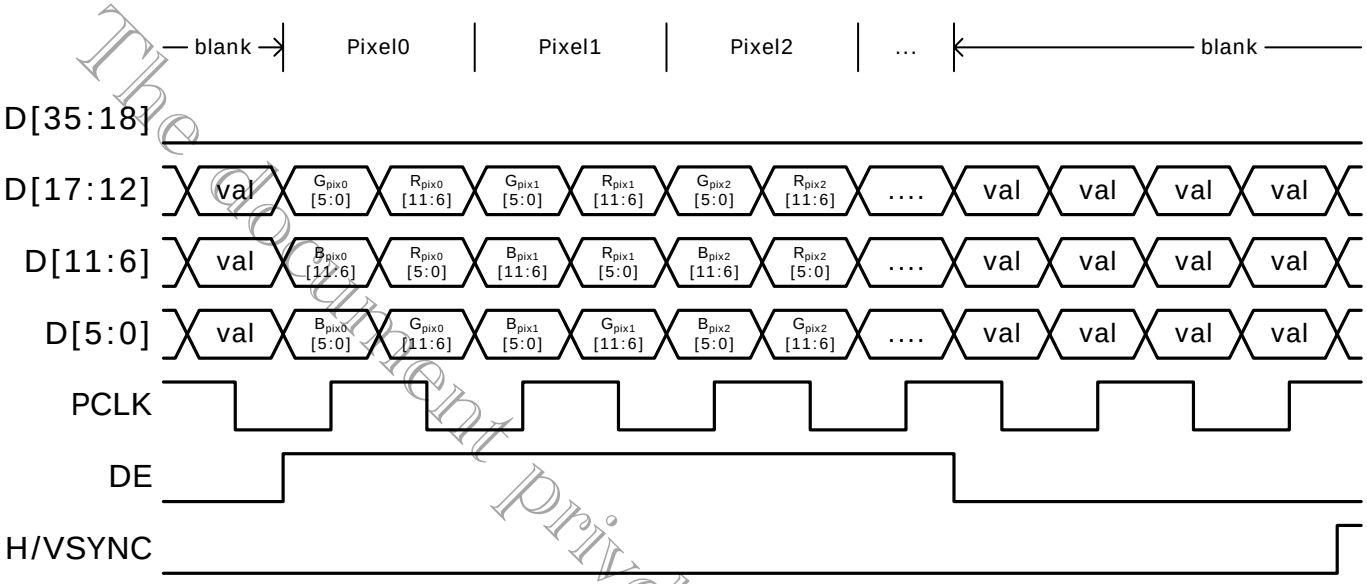


Figure 15. 18-bit RGB 4:4:4 dual-edge triggered

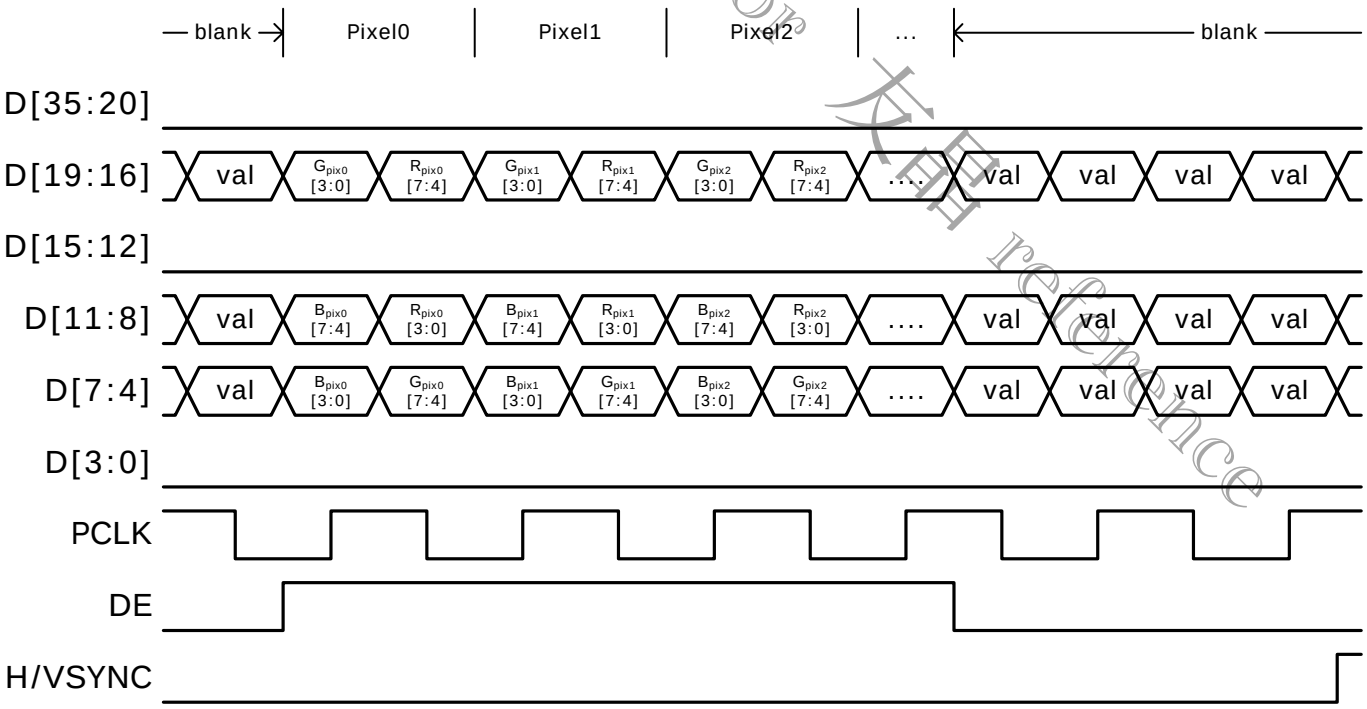


Figure 16. 12-bit RGB 4:4:4 dual-edge triggered

RGB 4:4:4 and YCbCr 4:4:4 Triggered with 0.5X PCLK at Dual Edges

The bus mapping in this format is the same as that of RGB 4:4:4 and YCbCr 4:4:4 with Separate Syncs. The only difference is that the input video clock (PCLK) is now halved in frequency. The data are in turn to be latched in with both the rising and falling edges of the 0.5X PCLK. Figure 17 and Figure 18 give two examples of such timing format.

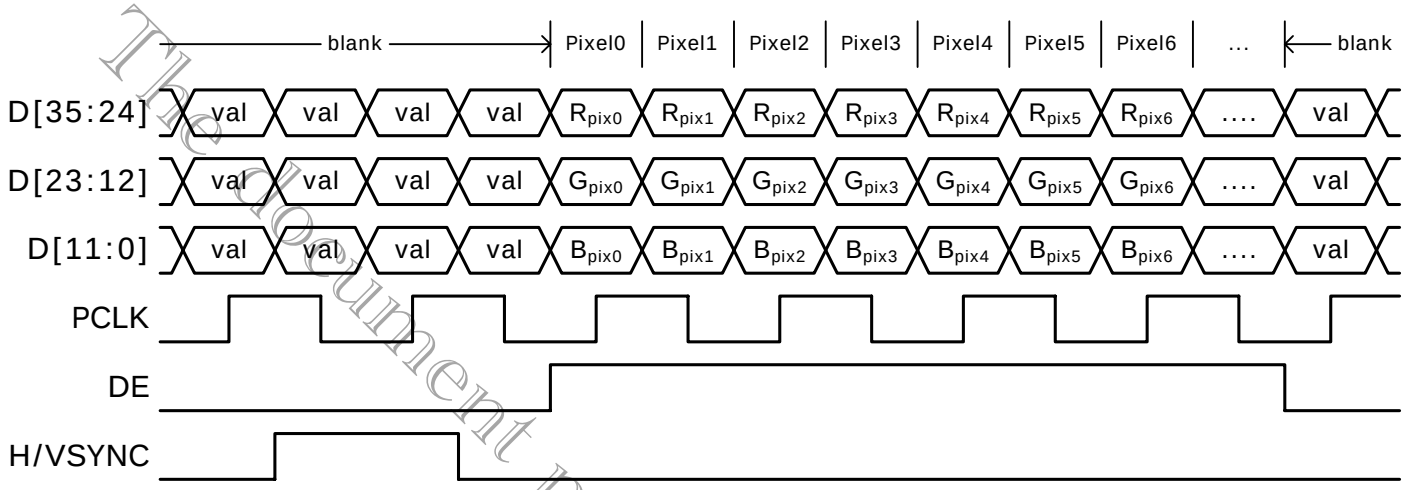


Figure 17. 36-bit RGB 4:4:4 dual-edges triggered with 0.5X PCLK

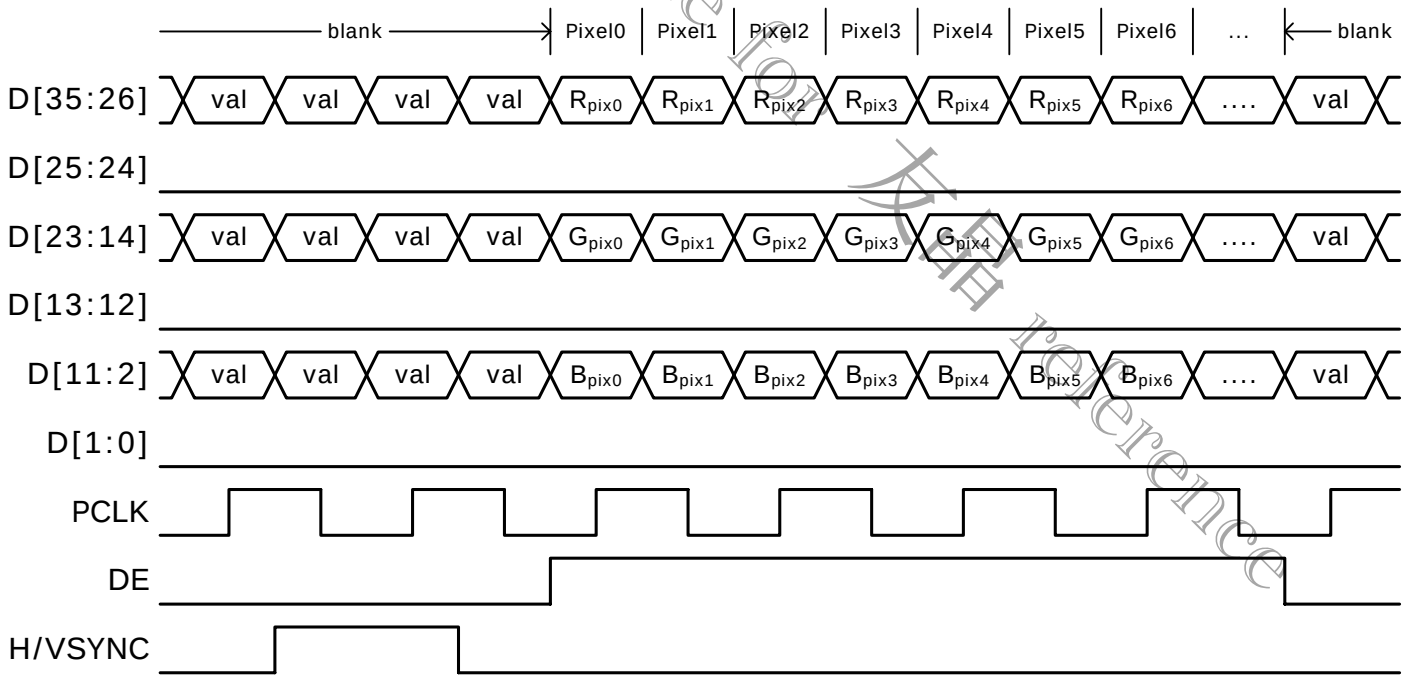


Figure 18. 30-bit RGB 4:4:4 dual-edges triggered with 0.5X PCLK

System Design Consideration

The IT6613 is a very high-speed interface chip. It takes in TTL signals at up to 148.5MHz with 36-bit data bus and transmits TMDS differential signals at as high as 2.25Gbps and s. At such speeds any PCB design imperfection could lead to compromised signal integrity and hence degraded performance. To get the optimum performance the system designers sould follow the guideline below when designing the application circuits and PCB layout.

1. Pin 28 (PVCC1) should be supplied with clean power: ferrite-decoupled and capacitively- bypassed, since this is the power for the transmitter PLL, which is crucial in determining the TMDS output signal quality . Excess power noise might degrade the system performance.

2. It is highly recommended that all power pins are decoupled to ground pins via capacitors of 0.01uF and 0.1uF. Low-ESL capacitors are prefered. Generally these capacitors should be placed on the same side of the PCB with the IT6613 and as close to the pins as possible, preferably within 0.5cm from the pins. It is also recommended that the power and ground traces run relatively short distances and are connected directly to respecitve power and ground planes through via holes.

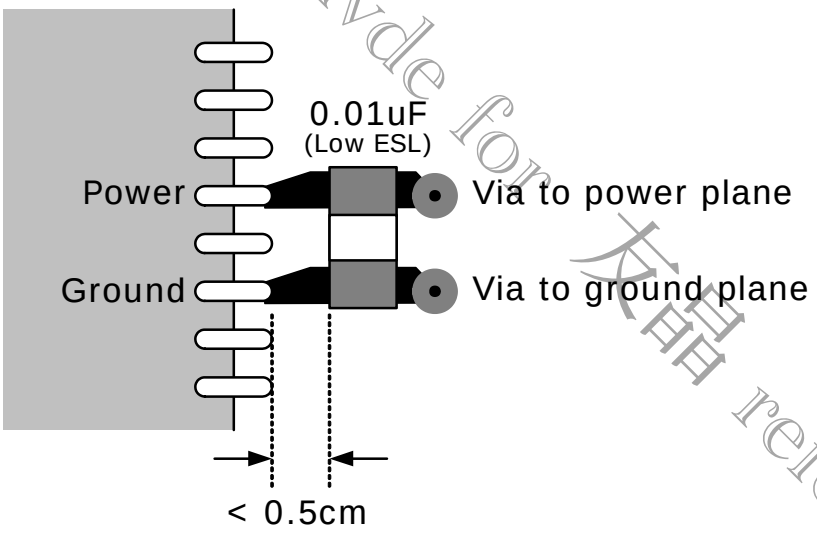


Figure 19. Layout example for decoupling capacitors.

3. The IT6613 supports 36-bit input bus running at as high as 148.5MHz. To maintain signal integrity and lower EMI, the following guidelines should be followed:

A. Employ **4-layer PCB** design, where a ground or power plane is directly placed under the signal buses at middle layes. The ground and power planes underneath these buses should be continuous in order to provide a solid return path for EM-wave introduced currents.

B. Whenever possible, keep all TTL signal traces on the same layer with the IT6613 and the

frontend decoder.

C. TTL input traces from the decoder should be kept as short as possible

D. Depending on the TTL output specifications of the frontend decoder, 33Ω resistors might be placed in series to its output pins. This slow down the signal rising edges, reduces current spikes and lower the reflections.

E. The PCLK signal should be kept away from other signal traces to avoid crosstalk interference. A general guideline is 2X the dielectric thickness. For example, if the dielectric layer between the signal layer and the immediate power/ground layer is 7 mil, then the PCLK trace should be kept at least 14 mil away from all other signal traces.

4. The characteristic impedance of all differential PCB traces should be kept at 100Ω all the way from the HDMI connector to the IT6613. This is crucial to the system performance at high speeds. When layouting these differential transmission lines, the following guidelines should be followed:

A. The signals traces should be on the outside layers (TOP layer or BOTTOM layer) while beneath it there should be a continuous ground plane in order to maintain the so-called micro-strip transmission line structure, giving stable and well-defined characteristic impedances.

B. Carefully choose the width and spacing of the differential transmission lines as their characteristic impedance depends on various parameters of the PCB: trace width, trace spacing, copper thickness, dielectric constant, dielectric thickness, etc. Careful 3D EM simulation is the best way to derive a correct dimension that enables a nominal 100Ω differential impedance.

C. Cornering, through holes, crossing and any irregular signal routing should be minimized so as to prevent from disrupting the EM field and creating discontinuity in characteristic impedance.

D. The IT6613 should be placed as close to the HDMI connector as possible. As a rule of thumb, the lengths of the TMDS differential traces (from the TMDS output pins of the IT6613 to the HDMI connector) **should be smaller than 1 cm (refer to Figure 20)**, especially for applications that support TMDS data rates at more than 1.62 Gbps. This is because at such high transmission rates, the source-side reflections would seriously impact the output data eyes. Since PCB traces, even when carefully designed, suffer from large impedance variations, it's a must that the reflection route be kept as short as possible.

5. Special care should be taken when adding discrete ESD devices to all differential PCB traces (TX2P/M, TX1P/M, TX0P/M, TXCP/M). The IT6613 is designed to provide ESD protection for up to 2kV at these pins, which is good enough to prevent damages during assembly. To meet the system EMC specification, external discrete ESD diodes might be added. But note that adding discrete ESD diodes inevitably add capacitive loads, therefore degrade the electrical performance at high speeds. If not chosen carefully, these diodes coupled with less-than-optimal layout would degrade the output

data eyes, which might fail to pass the SOURCE Data Eye Diagram test in the HDMI Compliance Test (Test ID 7-10). One should only use low-capacitance ESD diode to protect these high-speed pins. Commercially available devices such as Semtech's RClamp0524p that take into consideration of all aspects of designing and protecting high-speed transmission lines are recommended. *(http://www.semtech.com/products/product-detail.jsp?navId=H0,C2,C222,P3028)*.

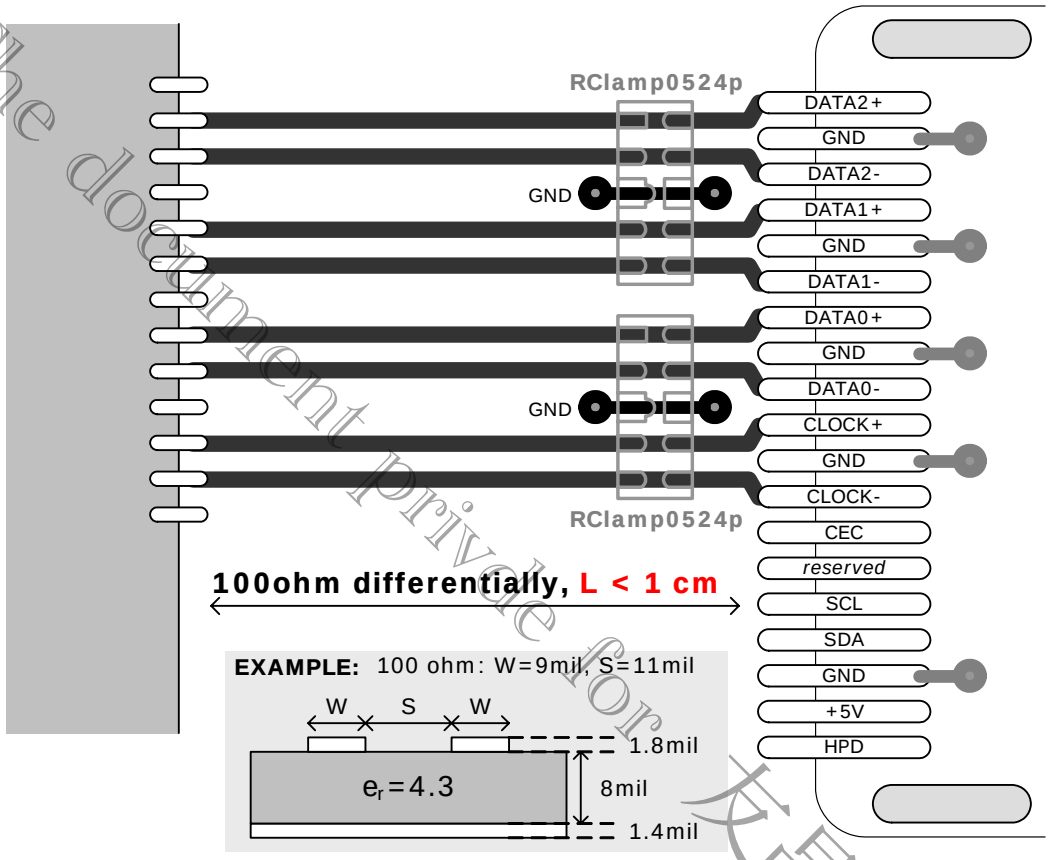
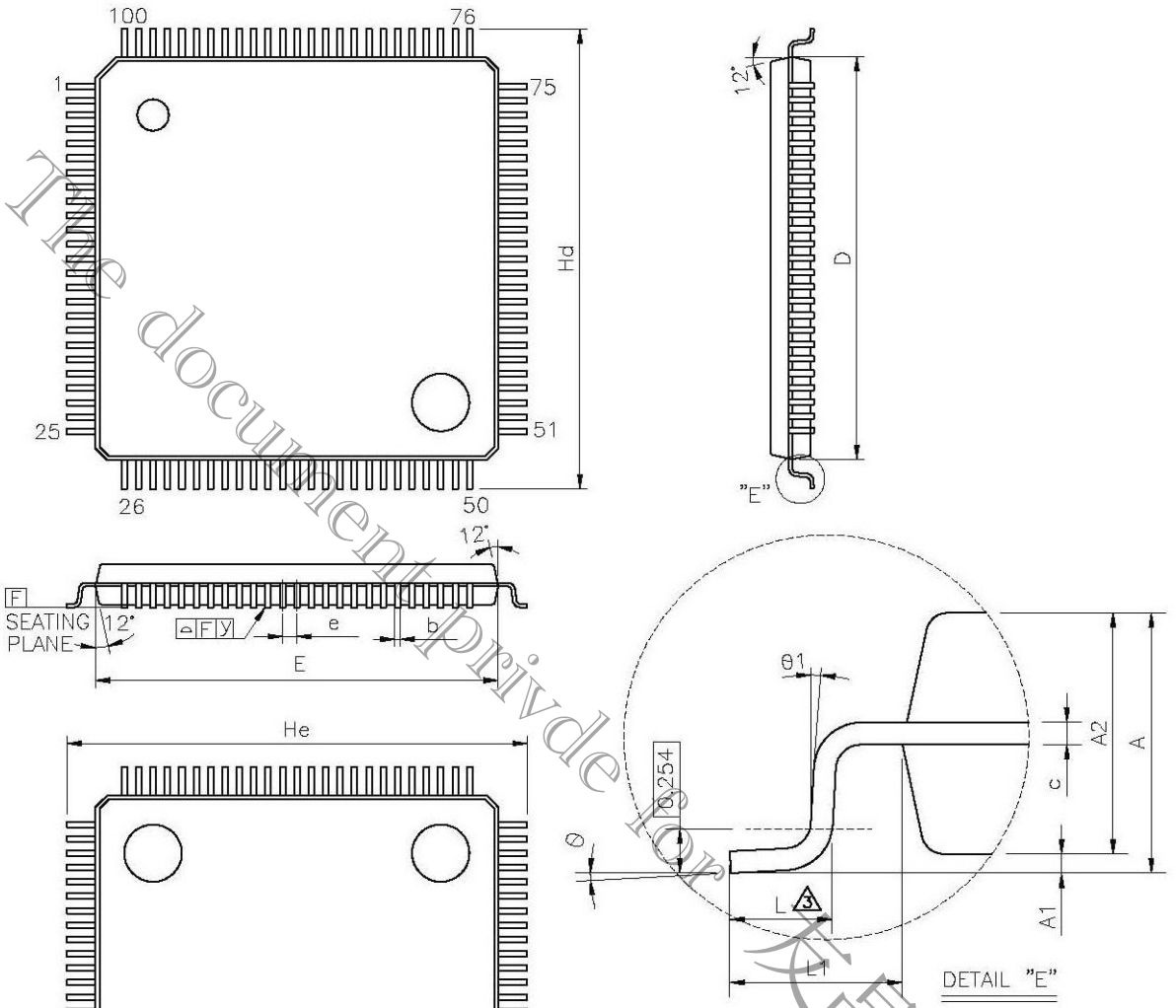


Figure 20. Layout example for high-speed TMDS differential signals

4. Pin 27 (REXT) should be connected to AVCC18 via a 698Ω/1% precision SMD resistor. This resistor is used to calibrate the TMDS output current level and should be placed as close as possible to the IT6613.

5. The IT6613 comes embedded with optionally programmable source terminations. It is recommended by HDMI Specifications v1.3a that source terminations be turned on when the operating link rate is over 1.65Gbps. User of the IT6613 may refer to IT6613 Programming Guide for proper control of source terminations through register setting.

Package Dimensions



Symbol \ Unit	mm	inch
A	1.600 MAX.	0.0629 MAX.
A1	0.10±0.10	0.004±0.004
A2	1.40±0.15	0.055±0.006
b	0.20±0.10	0.008±0.004
c	0.15±0.05	0.006±0.002
D	14.00±0.10	0.551±0.004
E	14.00±0.10	0.551±0.004
e	0.50NOM	0.020NOM
Hd	16.00±0.25	0.630±0.010
He	16.00±0.25	0.630±0.010
L	0.60±0.150	0.020±0.006
L1	1.00NOM	0.039NOM
y	0.08MAX	0.003MAX
θ	0° ~10°	0° ~10°
θ1	0° MIN	0° MIN

Figure 21. 100-pin LQFP Package Dimensions

Classification Reflow Profiles

Reflow Profile	Pb-Free Assembly
Average Ramp-Up Rate (Ts_{max} to Tp)	3℃/second max.
Preheat -Temperature Min(Ts_{min}) -Temperature Max(Ts_{max}) -Time(ts_{min} to ts ts_{max})	 150℃ 200℃ 60-180 seconds
Time maintained above: -Temperature(T_L) -Time(t_L)	 217℃ 60-150 seconds
Peak Temperature(Tp)	260 +0 /-5℃
Time within 5 ℃ of actual Peak Temperature(tp)	20-40 seconds
Ramp-Down Rate	6℃/second max.
Time 25℃ to Peak Temperature	8 minutes max.

Note: All Temperature refer to topside of the package, measured on the package body surface.