IT6605

Dual-Port HDMI 1.4 Receiver with 3D Support

ITE TECH. INC.

General Description

The IT6605 is a dual-port HDMI receiver, fully compatible with HDMI 1.3, compatible with HDMI 1.4a 3D and HDCP 1.4 and also backward compatible to DVI 1.0 specifications. The IT6605 with its Deep Color capability (up to 36-bit) ensures robust reception of high-quality uncompressed video content, along with state-of-the-art uncompressed and compressed digital audio content such as DTS-HD and Dolby TrueHD in digital televisions and projectors. The IT6605 also supports diverse 3D formats which are compliant with HDMI 1.4a 3D specification.

Aside from the various video output formats supported, the IT6605 also receives and provides up to 8 channels of I^2S digital audio outputs, with sampling rate up to 192kHz and sample size up to 24 bits, facilitating direct connection to industry-standard low-cost audio DACs. Also, an S/PDIF output is provided to support up to compressed audio of 192kHz frame rate. Super Audio Compact Disc (SACD) is supported at up to 8 channels and 88.2kHz through DSD (Direct Stream Digital ports) ports.

The High-Bit Rate (HBR) audio is also provided by the IT6605 in two interfaces: with the four I^2S input ports or the S/PDIF input port. With both interfaces the highest possible HBR frame rate is supported at up to 768kHz.

Each IT6605 comes preprogrammed with an unique HDCP key, in compliance with the HDCP 1.4 standard so as to provide secure transmission of high-definition content. Users of the IT6605 need not purchase any HDCP keys or ROMs.

The IT6605 is pin compatible with the CAT6023, the previous HDMI 1.3 receiver.

Features

- Dual-port HDMI 1.4 receiver
- Pin compatible with CAT6023
- Compliant with HDMI 1.3, HDMI 1.4a 3D, HDCP 1.4 and DVI 1.0 specifications
- Supporting link speeds of up to 2.25Gbps (link clock rate of 225MHz).
- Supporting diverse 3D formats which are compliant with HDMI 1.4a 3D specification.
  - Supporting 3D video up to 1080P@23.98/24/30Hz, 1080i@50/59.94/60/Hz, 720P@50/59.94/60Hz
  - Supporting formats: framing packing, side-by-side (half), top-and-bottom.
- Video output interface supporting digital video standards such as:
  - 24/30/36-bit RGB/YCbCr 4:4:4
  - 16/20/24-bit YCbCr 4:2:2

  - 8/10/12-bit YCbCr 4:2:2 (ITU BT-656)
  - 12/15/18-bit double data rate interface (data bus width halved, clocked with both rising and falling edges) for RGB/YCbCr 4:4:4
  - 24/30/36-bit double data rate interface (full bus width, pixel clock rate halved, clocked with both rising and falling edges)
  - Input channel swap
  - MSB/LSB swap
- Bi-direction Color Space Conversion (CSC) between RGB and YCbCr color spaces with programmable coefficients.
- Up/down sampling between YCbCr 4:4:4 and YCbCr 4:2:2
- Dithering for conversion from 12-bit component to 10-bit/8-bit
- Digital audio output interface supporting
  - up to four I^2S interface supporting 8-channel audio, with sample rates of 32~192 kHz and smaple sizes of 16~24 bits
  - S/PDIF interface supporting PCM, Dolby Digital, DTS digital audio at up to 192kHz frame rate
  - Optional support for 8-channel DSD audio up to 8 channels at 88.2kHz sample rate
  - Support for high-bit-rate (HBR) audio such as DTS-HD and Dolby TrueHD through the four I^2S interface or the S/PDIF interface, with frame rates as high as 768kHz
  - automatic audio error detection for programmable soft mute, preventing annoying harsh output sound due to audio error or hot-unplug
- Auto-calibrated input termination impedance provides process-, voltage- and temperature-invariant matching to the input transmission lines.
- Integrated pre-programmed HDCP keys
- Intelligent, programmable power management
- 144-pin LQFP (20mm x 20mm) package
- RoHS Compliant (100% Green available)

Ordering Information

Model	Temperature Range	Package Type	Green/Pb free Option
IT6605E	0~70	144-pin LQFP	Green

Pin Diagram

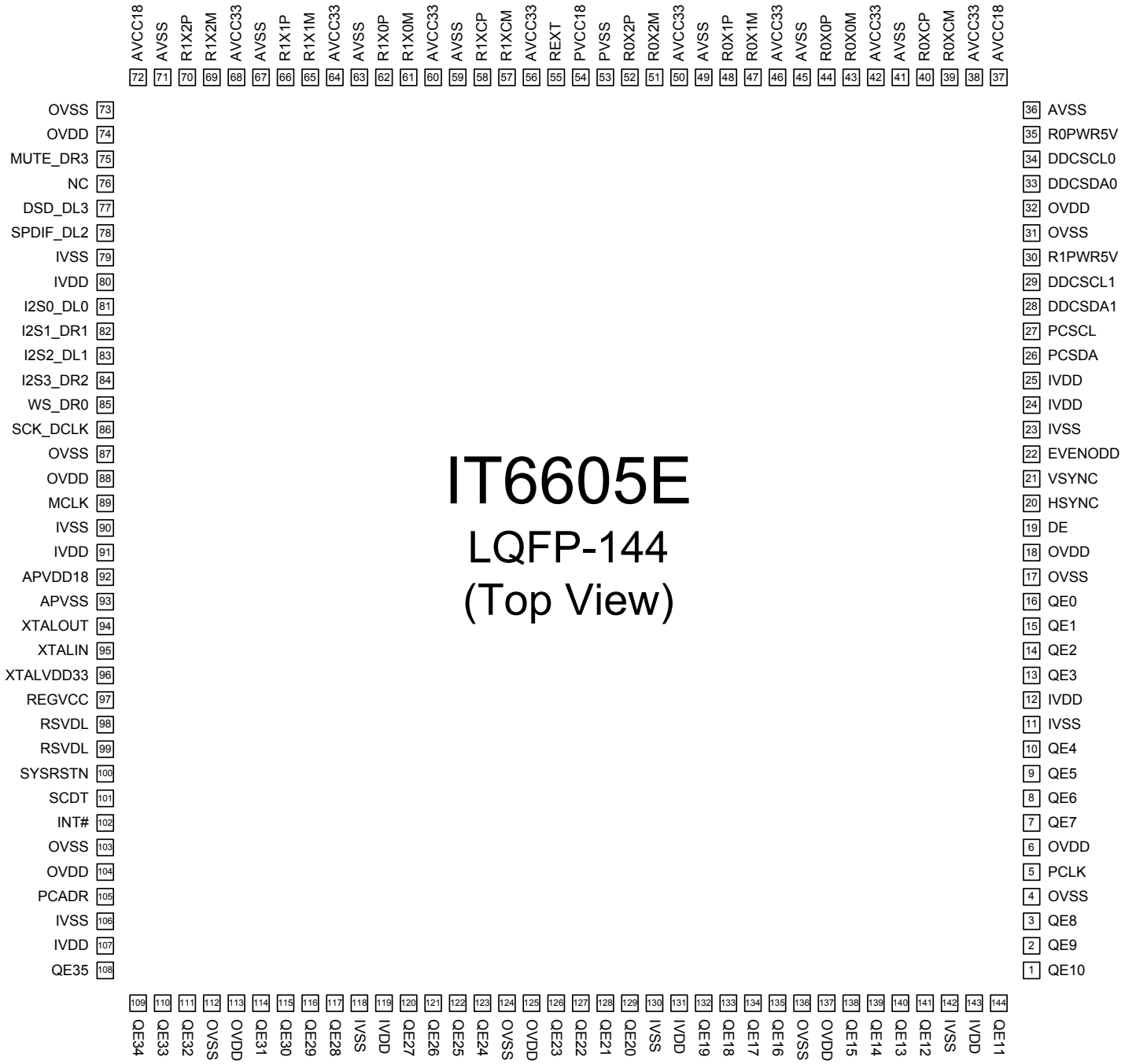


Figure 1. IT6605 pin diagram

Note:

1. *Pin55 must be connected with an external 500Ω SMD resistor to ground. This resistor serves to calibrate the on-chip termination impedances of all four pairs of high-speed serial links.*
2. *Pins marked with NC should be left unconnected.*

Pin Description

Digital Video Onput Pins

Pin Name	Direction	Description	Type	Pin No.
QE[35:0]	Output	Digital Video Output Pins. Channel swap and MSB-LSB reversal are supported through register setting.	LVTTL	1-3, 7-10, 13-16, 108-111, 114-117, 120-123, 126-129, 132-135, 138-141, 144
PCLK	Output	Output data clock. The backend controller should use the rising edge of PCLK to strobe QE[35:0]	LVTTL	5
DE	Output	Data enable	LVTTL	19
HSYNC	Output	Horizontal sync. signal	LVTTL	20
VSYNC	Output	Vertical sync. signal	LVTTL	21
EVENODD	Output	Indicates whether the current field is Even or Odd for interlaced format	LVTTL	22

Digital Audio Onput Pins

Pin Name	Direction	Description	Type	Pin No.
XTALIN	Input	Crystal clock input (for Audio PLL)	LVTTL	95
XTALOUT	Output	Crystal clock output (for Audio PLL)	LVTTL	94
MCLK	Output	Audio master clock	LVTTL	89
SCK_DCLK	Output	I2S serial clock output, doubles as DSD clock	LVTTL	86
WS_DR0	Output	I2S word select output, doubles as DSD Serial Right CH0 data output	LVTTL	85
I2S0_DL0	Output	I2S serial data output, doubles as DSD Serial Left CH0 data output	LVTTL	81
I2S1_DR1	Output	I2S serial data output, doubles as DSD Serial Right CH1 data output	LVTTL	82
I2S2_DL1	Output	I2S serial data output, doubles as DSD Serial Left CH2 data output	LVTTL	83
I2S3_DR2	Output	I2S serial data output, doubles as DSD Serial Right CH2 data output	LVTTL	84
SPDIF_DL2	Output	S/PDIF audio output, doubles as DSD Serial Left CH2 data output	LVTTL	78
MUTE_DR3	Output	Mute output, doubles as DSD Serial Right CH3 data output	LVTTL	75
DSD_DL3	Output	DSD Serial Left CH3 data output	LVTTL	77

Programming Pins

Pin Name	Direction	Description	Type	Pin No.
INT#	Output	Interrupt output. Default active-low (5V-tolerant)	LVTTL	102
SYSRSTN	Input	Hardware reset pin. Active LOW (5V-tolerant)	Schmitt	100
DDCSCL0	I/O	DDC I2C Clock for HDMI Port 0 (5V-tolerant)	Schmitt	34
DDCSDA0	I/O	DDC I2C Data for HDMI Port 0 (5V-tolerant)	Schmitt	33
R0PWR5V	Input	TMDS transmitter detection for Port 0(5V-tolerant)	LVTTL	35
DDCSCL1	I/O	DDC I2C Clock for HDMI Port 1 (5V-tolerant)	Schmitt	29
DDCSDA1	I/O	DDC I2C Data for HDMI Port 1 (5V-tolerant)	Schmitt	28
R1PWR5V	Input	TMDS transmitter detection for Port 1(5V-tolerant)	LVTTL	30
PCSCL	Input	Serial Programming Clock for chip programming (5V-tolerant)	Schmitt	27
PCSDA	I/O	Serial Programming Data for chip programming (5V-tolerant)	Schmitt	26
PCADR	Input	Serial Programming device address select. Device address is 0x90 when PCADR is pulled low, 0x92 otherwise	LVTTL	105
SCDT	Output	Indication for active HDMI signal at input port	LVTTL	101
RSVDL	Input	Must be tied low via a resistor.	LVTTL	98, 99
NC		Must be left unconnected		76,

HDMI analog front-end interface pins

Pin Name	Direction	Description	Type	Pin No.
R0X2P	Analog	HDMI Channel 2 positive input for HDMI Port 0	TMDS	52
R0X2M	Analog	HDMI Channel 2 negative input for HDMI Port 0	TMDS	51
R0X1P	Analog	HDMI Channel 1 positive input for HDMI Port 0	TMDS	48
R0X1M	Analog	HDMI Channel 1 negative input for HDMI Port 0	TMDS	47
R0X0P	Analog	HDMI Channel 0 positive input for HDMI Port 0	TMDS	44
R0X0M	Analog	HDMI Channel 0 negative input for HDMI Port 0	TMDS	43
R0XCP	Analog	HDMI Clock Channel positive input for HDMI Port 0	TMDS	40
R0XCM	Analog	HDMI Clock Channel negative input for HDMI Port 0	TMDS	39
REXT	Analog	External resistor for setting termination impedance value. Should be tied to GND via a 500Ω SMD resistor.	Analog	55
R1X2P	Analog	HDMI Channel 2 positive input for HDMI Port 1	TMDS	70
R1X2M	Analog	HDMI Channel 2 negative input for HDMI Port 1	TMDS	69
R1X1P	Analog	HDMI Channel 1 positive input for HDMI Port 1	TMDS	66
R1X1M	Analog	HDMI Channel 1 negative input for HDMI Port 1	TMDS	65
R1X0P	Analog	HDMI Channel 0 positive input for HDMI Port 1	TMDS	62
R1X0M	Analog	HDMI Channel 0 negative input for HDMI Port 1	TMDS	61

R1XCP	Analog	HDMI Clock Channel positive input for HDMI Port 1	TMDS	58
R1XCM	Analog	HDMI Clock Channel negative input for HDMI Port 1	TMDS	57

Power/Ground Pins

Pin Name	Description	Type	Pin No.
IVDD	Digital logic power (1.8V)	Power	12, 24, 25, 80, 91, 107, 119, 131, 143
IVSS	Digital logic ground	Ground	11, 23, 79, 90, 106, 118, 130, 142
OVDD	I/O Pin power (3.3V)	Power	6, 18, 32, 74, 88, 104, 113, 125, 137
OVSS	I/O Pin ground	Ground	4, 17, 31, 73, 87, 103, 112, 124, 136
AVCC33	HDMI analog frontend power (3.3V)	Power	38, 42, 46, 50, 56, 60, 64, 68
AVCC18	HDMI analog frontend power (1.8V)	Power	37, 72
AVSS	HDMI analog frontend ground	Ground	36, 41, 45, 49, 59, 63, 67, 71
PVCC18	HDMI receiver PLL power (1.8V)	Power	54
PVSS	HDMI receiver PLL ground	Ground	53
APVDD18	HDMI audio PLL power (1.8V)	Power	92
APVSS	HDMI audio PLL ground	Ground	93
XTALVDD33	Power for crystal oscillator (3.3V)	Power	96
REGVCC	Regulator power (3.3V) for audio PLL	Power	97

Functional Description

The IT6605 is the 3nd generation HDMI receiver and provides complete solutions for HDMI v1.4 Sink systems, supporting reception and processing of Deep Color video and state-of-the-art digital audio such as DTS-HD and Dolby TrueHD. The IT6605 with its two HDMI input ports supports color depths of 10 bits and 12 bits up to 1080p. Advanced processing algorithms are employed to optimize the performance of video processing such as color space conversion and up/down sampling. The following picture is the functional block digram of the IT6605, which describes clearly the data flow. Note that only one the two inputs can be activated at a time.

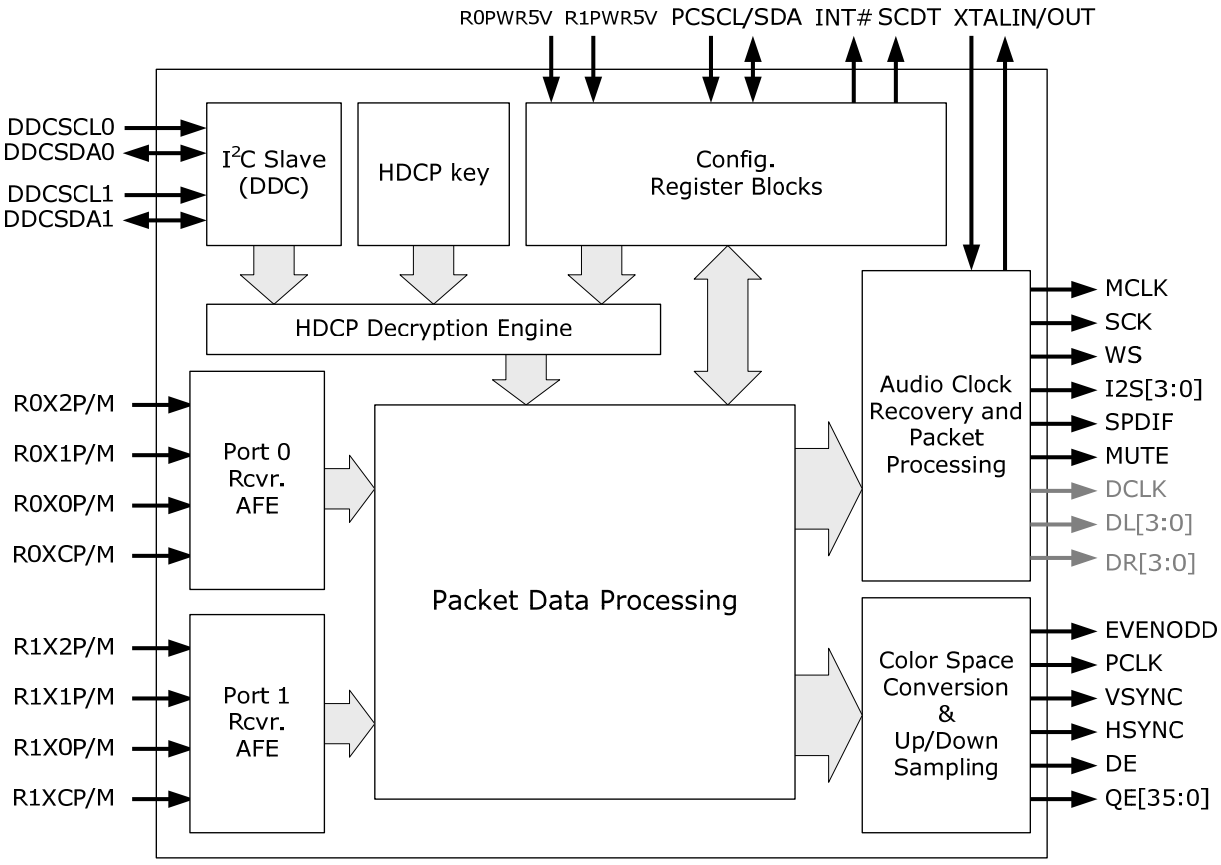


Figure 2. Functional block diagram of the IT6605

Receiver Analog Frontend (Rcvr. AFE)

The two integrated TMDS receiver analog frontend macros are capable of receiving and decoding HDMI data at up to 2.25Gbps (with a TMDS clock of 225MHz). Adaptive equalization is employed to support long cables. Only one port can be actived at a time and the system firmware has total control over this through register settings.

While not indicated in Figure 2, the two HDMI PWR5V signals of the two respective inputs are also monitored by the IT6605. The system controller could poll registers to confirm the existence of actually

connected port.

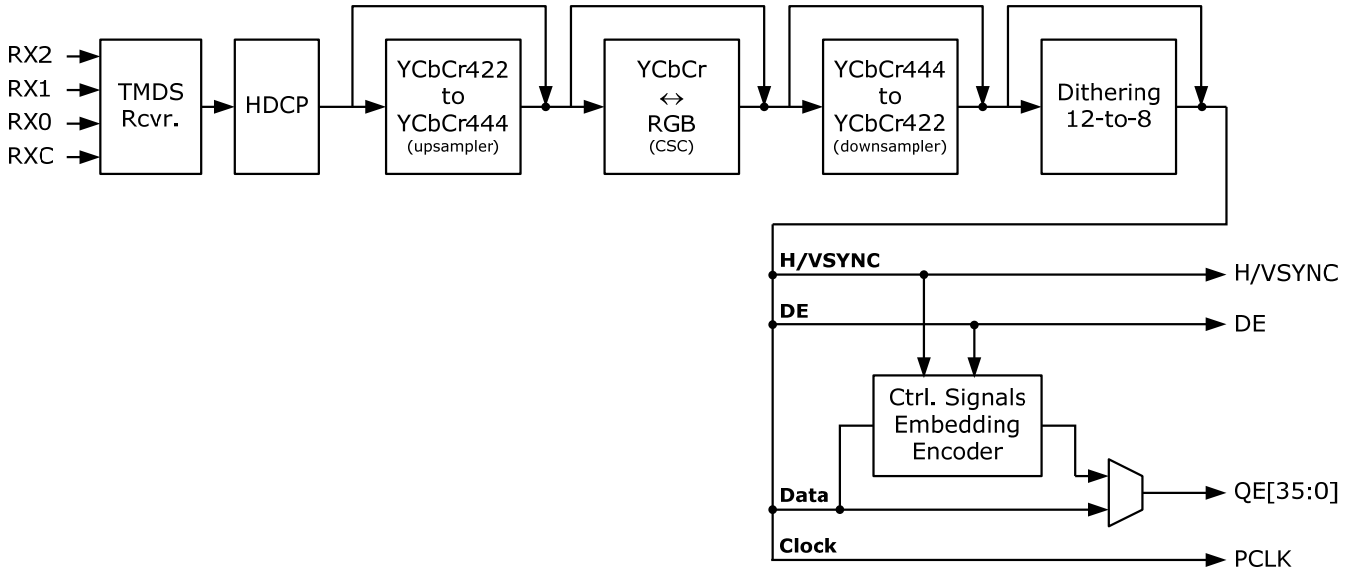


Figure 3. Video data processing flow of the IT6605

Video Data Processing Flow

Figure 3 depicts the video data processing flow. For the purpose of retaining maximum flexibility, most of the block enablings and path bypassings are controlled through register programming. Please refer to IT6605 Programming Guide for detailed and precise descriptions.

As can be seen from Figure 3, the received and recovered HDMI raw data is first HDCP-decrypted. The extracted video data then go through various processing blocks, as described in the following paragraphs, before outputting the proper video format to the backend video controller.

The video processing including YCbCr up/down-sampling, color-space conversion and dithering. Depending on the selected input and output video formats, different processing blocks are either enabled or bypassed via register control. For the sake of flexibility, this is all done in software register programming. Therefore, extra care should be taken in keeping the selected output format and the corresponding video processing block selection. Please refer to the IT6605 Programming Guide for suggested register setting.

Designated as QE[35:0], the output video data could take on bus width of 8 bits to 36 bits, depending on the formats and color depths. The output interface could be configured through register setting to provide various data formats as listed in Table 1 in order to cater to different preferences of different backend controllers.

Major video processings in the IT6605 are carried out in 14 bits per channel in order to minimize rounding errors and other computational residuals that occur during processing. General description of video processing blocks is as follows:

HDCP engine (HDCP)

The HDCP engine decrypts in incoming data. Preprogrammed HDCP keys are embedded in the IT6605. Users need not worry about the purchasing and management of the HDCP keys as Chip Advanced Technology will take care of them.

Upsampling (YCbCr422 to YCbCr444)

In cases where input HDMI video data are in YCbCr 4:2:2 format and output is selected as 4:4:4, this block is enabled to do the upsampling. Well-designed signal filtering is employed to avoid visible artifacts generated during upsampling.

Bi-directional Color Space Conversion (YCbCr ↔ RGB)

Many video decoders only offer YCbCr outputs, while DVI 1.0 supports only RGB color space. In order to offer full compatibility between various Source and Sink combination, this block offers bi-directional RGB ↔ YCbCr color space conversion (CSC). To provide maximum flexibility, the matrix coefficients of the CSC engine in the IT6605 are fully programmable. Users could elect to employ their preferred conversion formula.

Downsampling (YCbCr444 to YCbCr422)

In cases where input HDMI video data are in YCbCr 4:4:4 format and output is selected as YCbCr 4:2:2, this block is enabled to do the downsampling. Well-designed signal filtering is employed to avoid visible artifacts generated during downsampling.

Dithering (Dithering 12-to-10 or 12-to-8)

For outputing to the 10-bits / 8-bits-per-channel formats, decimation might be required depending on the exact input formats. This block performs the necessary dithering for decimation to prevent visible artifacts from appearing.

Supported output Video Formats

Table 1 lists the output video formats supported by the IT6605. The listed Output Pixel Clock Frequency in MHz is the actual clock frequency at the output pin PCLK, regardless of the color depth. According to the HDMI Specification v1.3, the input TMDS clock frequency could be 1.25 times or 1.5 times that of the output PCLK frequency, depending on the color depth:

For 24-bit inputs, TMDS Clock frequency = 1 x PCLK frequency
For 30-bit inputs, TMDS Clock frequency = 1.25 x PCLK frequency
For 36-bit inputs, TMDS Clock frequency = 1.5 x PCLK frequency

The IT6605 also provides automatic video mode detection. The system controller can elect to check out respective status registers to get the informations.

				Output Pixel Clock Frequency (MHz)							
Color Space	Video Format	Bus Width	Hsync/ Vsync	480i	480p	XGA	720p	1080i	SXGA	1080p	UXGA
RGB	4:4:4	24	Separate	13.5	27	65	74.25	74.25	108	148.5	162
		30/36		13.5	27	65	74.25	74.25	108	148.5	
		12/15/18	Separate	13.5	27	65	74.25	74.25			
YCbCr	4:4:4	24	Separate	13.5	27	65	74.25	74.25	108	148.5	162
		30/36		13.5	27	65	74.25	74.25	108	148.5	
		12/15/18	Separate	13.5	27	65	74.25	74.25			
	4:2:2	16/20/24	Separate	13.5	27		74.25	74.25		148.5	
			Embedded	13.5	27		74.25	74.25		148.5	
		8/10/12	Separate	27	54		148.5	148.5			
			Embedded	27	54		148.5	148.5			

Table 1. Output video formats supported by the IT6605

Notes:
1. Table cells that are left blanks are those format combinations that are not supported by the IT6605.
2. Output channel number is defined by the way the three color components (either R, G & B or Y, Cb & Cr) are arranged. Refer to Video Data Bus Mappings for better understanding.
3. Embedded sync signals are defined by CCIR-656 standard, using SAV/EAV sequences of FF, 00, 00, XY.
4. The lowest TMDS clock frequency specified by the HDMI standard is 25MHz for 640X480@60Hz.

Supported 3D Formats

The IT6604 supports all the HDMI 1.4a 3D mandatory formats and most optional 3D formats including

- 1920x1080P@23.98/24/30Hz -- Framing Packing
- 1920x1080P@23.98/24/30Hz -- Top-and-Bottom
- 1920x1080i @50/59.94/60Hz -- Side-by-Side (Half)
- 1280x 720P@50/59.94/60Hz -- Framing Packing
- 1280x 720P@50/59.94/60Hz -- Top-and-Bottom

Audio Clock Recovery and Data Processing

The audio processing block in the HDMI Sink is crucial to the system performance since human hearing is susceptive to audio imperfection. The IT6605 prides itself in outstanding audio recovery performances. In addition, the audio clock recovery PLL uses an external crystal reference so as to provide stable and reliable audio clocks for all audio output formats.

The IT6605 supports all audio formats and interfaces specified by the HDMI Specification v1.3 through I^2S, S/PDIF and optional one-bit audio outputs. The one-bit audio outputs take on the pins used by I^2S outputs, so only one between the two could be activated at a time.

I²S

Four I²S outputs are provided to support 8-channel uncompressed audio data at up to 192kHz sample rate. A coherent multiple (master) clock MCLK is generated at pin 89 to facilitate proper functions of mainstream backend audio DAC ICs. The supported multiplied factor and sample frequency as well as the resultant MCLK frequencies are summarized in Table 2.

Multiple of audio sample frequency	Audio sample frequency						
	32kHz	44.1kHz	48kHz	88.2kHz	96kHz	176.4kHz	192kHz
128	4.096	5.645	6.144	11.290	12.288	22.579	24.576
256	8.192	11.290	12.288	22.579	24.576	45.158	49.152
384	12.288	16.934	18.432	33.869	36.864	67.738	73.728
512	16.384	22.579	24.576	45.158	49.152	90.317	98.304
640	20.480	28.224	30.720	56.448	61.440	(112.896)	(122.880)
768	24.576	33.868	36.864	67.738	73.728	(135.475)	(147.456)
896	28.672	39.514	43.008	79.027	86.016	(158.054)	(172.032)
1024	32.768	45.158	49.152	90.316	98.304	(180.634)	(196.608)

Table 2. Output MCLK frequencies (MHz) supported by the IT6605

Notes:
1. The MCLK frequencies in parenthesis are MCLK frequencies over 100MHz. These frequencies are implemented in the IT6605 and could be output through register setting as well. However, the I/O circuit of the MCLK pin does not guarantee to be operating at such a high frequency under normal operation conditions. In addition, few audio backend ICs such as DACs support such high MCLK frequencies. Therefore, using the MCLKs in parenthesis is strongly discouraged.

S/PDIF

The S/PDIF output provides 2-channel uncompressed PCM data (IEC 60958) or compressed multi-channel data (IEC 61937) at up to 192kHz. By default the clock of S/PDIF is carried within the datastream itself via coding. The IT6605 also supplies coherent MCLK in cases of S/PDIF output to help ease the implementation with certain audio processing ICs.

One-Bit Audio (DSD/SACD)

Direct stream digital (DSD) audio is an one-bit audio format which is prescribed by Super Audio CD (SACD) to provide superiore audio hearing experiences. Based on the register setting of the system controller, the IT6605 outputs DSD audio optionally through existing I²S output pins. A total of 8 data outputs are provided for right channels and left channels. Refer to Pin Description on page 5 for detailed port-to-pin mapping.

High-Bit-Rate Audio (HBR)

High-Bit-Rate Audio is also new to the HDMI standard. It is called upon by high-end audio system such as DTS-HD and Dolby TrueHD. No specific interface is defined by the HBR standard. The IT6605 supports HBR audio in two ways. One is to employ the four I^2S outputs simultaneously, where the original streaming DSD audio is broken into four parallel data streams. The other is to use the S/PDIF output port. The data rate in the later case is as high as 98.304Mbps. A coherent MCLK is generated by the IT6605 for the backend audio processors.

Smart Audio Error Detection

Some previous HDMI Sink products were reported to generate unbearably harsh sounds during hot-plug/unplug as well as unspecified audio error. Like its predecessor CAT6011, the IT6605 prides itself for detecting all kinds of audio error and soft-mutes the audio accordingly, therefore preventing unpleasant noise from outputting.

Interrupt Generation

To provide automatic format setting, hot plug/unplug handling and error handling, the system micro-controller should monitor the interrupt signal output at Pin 102 (INT#). The IT6605 generates an interrupt signal whenever events involving the following signals or situations occur:

1. A status change of incoming 5V power signals at pin 30 or pin 35 (corresponding to plug/unplug)
2. Stable video is acquired (SCDT at pin 101 is asserted)
3. Events of audio errors and/or audio mute
4. Events of ECC errors
5. Video mode change

Without software intervention the hardware of the IT6605 should be able to output some sort of displayable video data. However, this video could be in the wrong format or color space. Also, hardware alone is not sufficient in handling the exception events listed above. The micro-controller must monitor the INT# signal carefully and poll the corresponding registers for optimum operation.

Configuration and Function Control

The IT6605 comes with three serial programming ports: one for interfacing with micro-controller, the other two allowing access by HDMI Sources through the two DDC channels of the HDMI links.

The serial programming interface for interfacing the micro-controller is a slave interface, comprising PCSCL (Pin 27) and PCSDA (Pin 26). The micro-controller uses this interface to monitor all the statuses and control all the functions. Two device addresses are available, depending on the input logic level of PCADR (Pin 105). If PCADR is pulled high by the user, the device address is **0x92**. If

pulled low, **0x90**.

Since the IT6605 provides two HDMI input ports, two DDC I^2C interface are present at DDCSCL0 (Pin 34) & DDCSDA0 (Pin 33) and DDCSCL1 (Pin 29) & DDCSDA1 (Pin 28). With the interfaces, the IT6605 responds to the access of HDMI Sources via the DDC channels. HDMI Sources use the interfaces to perform HDCP authentication with the IT6605.

All serial programming interfaces conform to standard I^2C transactions and operate at up to 100kHz.

Electrical Specifications

Absolute Maximum Ratings

Symbol	Parameter	Min.	Typ	Max	Unit
IVDD	Core logic supply voltage	-0.3		2.5	V
OVDD	I/O pins supply voltage	-0.3		4.0	V
AVCC33	HDMI analog frontend power	-0.3		4.0	V
AVCC18	HDMI analog frontend power	-0.3		2.5	V
PVCC18	HDMI receiver PLL power	-0.3		2.5	V
APVDD18	HDMI audio PLL power	-0.3		2.5	V
XTALVDD33	Power for crystal oscillator	-0.3		4.0	V
REGVCC	Power for regulator	-0.3		4.0	V
V_I	Input voltage	-0.3		OVDD+0.3	V
V_O	Output voltage	-0.3		OVDD+0.3	V
T_J	Junction Temperature			125	°C
T_{STG}	Storage Temperature	-65		150	°C
ESD_HB	Human body mode ESD sensitivity	2000			V
ESD_MM	Machine mode ESD sensitivity	200			V

Notes:
1. Stresses above those listed under Absolute Maximum Ratings might result in permanent damage to the device.

Functional Operation Conditions

Symbol	Parameter	Min.	Typ	Max	Unit
IVDD	Core logic supply voltage	1.6	1.8	2.0	V
OVDD	I/O pins supply voltage	2.97	3.3	3.63	V
AVCC33	HDMI analog frontend power[2]	3.135	3.3	3.465	V
AVCC18	HDMI analog frontend power	1.6	1.8	2.0	V
PVCC18	HDMI receiver PLL power	1.6	1.8	2.0	V
APVDD18	HDMI audio PLL power	1.6	1.8	2.0	V
XTALVDD33	Power for crystal oscillator	3.0	3.3	3.6	V

REGVCC	Power for regulator	3.0	3.3	3.6	V
$V_{CCNOISE}$	Supply noise			100	mV_{pp}
T_A	Ambient temperature	0	25	70	°C
Θ_{ja}	Junction to ambient thermal resistance				°C/W

Notes:
1. AVCC33, AVCC18, PVCC18 and APVDD18 should be regulated.
2. AVCC33 supplies the termination voltage. Therefore the range is specified by the HDMI Standard.

Operation Supply Current Specification

Symbol	Parameter	PCLK	Typ	Unit
I_{IVDD_OP}	IVDD current under normal operation	27MHz	64	mA
		74.25MHz	146	mA
		148.5MHz	250	mA
		222.75MHz	325	mA
I_{OVDD_OP}	OVDD current under normal operation (with 20pF capacitive output loading)	27MHz	14	mA
		74.25MHz	41	mA
		148.5MHz	60	mA
		222.75MHz	72	mA
I_{AVCC18_OP}	AVCC18 current under normal operation (with input Vdiff= 750 mV)	27MHz	50	mA
		74.25MHz	65	mA
		148.5MHz	82	mA
		222.75MHz	106	mA
I_{AVCC33_OP}	AVCC33 current under normal operation (with input Vdiff= 750 mV)	27MHz	57	mA
		74.25MHz	57	mA
		148.5MHz	57	mA
		222.75MHz	58	mA
I_{PVCC18_OP}	PVCC18 current under normal operation	27MHz	5	mA
		74.25MHz	13	mA
		148.5MHz	23	mA
		222.75MHz	35	mA
$I_{APVDD18\_OP}$	APVDD18 current under normal operation	27MHz	6	mA
		74.25MHz	6	mA
		148.5MHz	6	mA
		222.75MHz	6	mA
$I_{XTALVDD33}$	XTALVDD33 current under normal operation	(all speeds)	1	mA
I_{REGVCC}	REGVCC current under normal operation	(all speeds)	0	mA
PW_{TOTAL_OP}	Total power consumption under normal operation[3]	27MHz	463	mW
		74.25MHz	741	mW
		148.5MHz	1039	mW
		222.75MHz	1282	mW

Notes:
1. Typ: OVDD=AVCC33=XTALVDD33=REGVCC=3.3V, IVDD=AVCC18=PVCC18=APVDD18=1.8V
   PCLK=27MHz: 480p with 48kHz/8-channel audio,
   PCLK=74.25MHz: 1080i with 192kHz/8-channel audio,
   PCLK=148.5MHz: 1080p with 192kHz/8-channel audio,
   PCLK=222.75MHz: 1080p**@36-bit Deep Color** with 192kHz/8-channel audio
2. PW_{TOTAL_OP} are calculated by multiplying the supply currents with their corresponding supply voltage and summing up all the items.

DC Electrical Specification

Under functional operation conditions

Symbol	Parameter	Pin Type	Conditions	Min.	Typ	Max	Unit
V_{IH}	Input high voltage[1]	LVTTL		2.0			V
V_{IL}	Input low voltage[1]	LVTTL				0.8	V
V_T	Switching threshold[1]	LVTTL			1.5		V
V_{T-}	Schmitt trigger negative going threshold voltage[1]	Schmitt		0.8	1.1		V
V_{T+}	Schmitt trigger positive going threshold voltage[1]	Schmitt			1.6	2.0	V
V_{OL}	Output low voltage[1]	LVTTL	I_{OL}=2~16mA			0.4	
V_{OH}	Output high voltage[1]	LVTTL	I_{OH}=-2~-16mA	2.4			
I_{IN}	Input leakage current[1]	all	V_{IN}=5.5V or 0		±5		μA
I_{OZ}	Tri-state output leakage current[1]	all	V_{IN}=5.5V or 0		±10		μA
I_{OL}	Serial programming output sink current[2]	Schmitt	V_{OUT}=0.2V	4		16	mA
V_{diff}	TMDS input differential swing[3]	TMDS	R_{EXT}=500Ω	150		1200	mV

Notes:

1. Guaranteed by I/O design.
2. The serial programming output ports are not real open-drain drivers. Sink current is guaranteed by I/O design under the condition of driving the output pin with 0.2V. In a real I^2C environment, multiple devices and pull-up resistors could be present on the same bus, rendering the effective pull-up resistance much lower than that specified by the I^2C Standard. When set at maximum current, the serial programming output ports of the IT6605 are capable of pulling down an effective pull-up resistance as low as 500Ω connected to 5V termination voltage to the standard I^2C V_{IL}. When experiencing insufficient low level problem, try setting the current level to higher than default. Refer to IT6605 Programming Guide for proper register setting.
3. Limits defined by HDMI 1.3a standard

Audio AC Timing Specification

Under functional operation conditions

Symbol	Parameter	Conditions	Min.	Typ	Max	Unit
F_{S_I2S}	I^2S sample rate	Up to 8 channels	32		192	kHz
F_{S_SPDIF}	S/PDIF sample rate	2 channels	32		192	kHz
F_{S_DSD}	DSD sample rate	Up to 8 channels			96	kHz
F_{XTAL}	External audio crystal frequency[1]	±300ppm accuracy	24	27	28.5	MHz

Notes:

1. The IT6605 is designed to work in default with a 27MHz crystal for audio functions. Crystals of other frequencies within the designated functional range mandate certain register programming for proper functioning.

Video AC Timing Specification

Under functional operation conditions

Symbol	Parameter	Conditions	Min.	Typ	Max	Unit
T_{pixel}	PCLK pixel clock period[1]	Single-edged clocking	4.44		40	ns
F_{pixel}	PCLK pixel clock frequency[1]		25		225	MHz
T_{CDE}	PCLK dual-edged clock period[2]	Dual-edged clocking	8.88		40	ns
F_{CDE}	PCLK dual-edged clock frequency[2]		25		112.5	MHz
T_{PDUTY}	PCLK clock duty cycle		40%		60%	

Notes:

1. Fpixel is the inverse of Tpixel. Operating frequency range is given here while the actual video clock frequency should comply with all video timing standards. Refer to Table 1 for supported video timings and corresponding pixel frequencies.
2. 12-bit dual-edged clocking is supported up to 74.5MHz of PCLK frequency, which covers 720p/1080i.
3. All setup time and hold time specifications are with respect to the latching edge of PCLK selected by the user through register programming.

Video Data Bus Mappings

The IT6605 supports various output data mappings and formats, including those with embedded control signals only. Corresponding register setting is to be taken care of for any chosen input data mappings. Refer to IT6605 Programming Guide for detailed instruction.

Color Space	Video Format	Bus Width	H/Vsync	Clocking	Table
RGB	4:4:4	24/30/36	Seperate	1X	4
		12/15/18	Seperate	Dual-edged	9
		24/30/36	Seperate	0.5X, Dual-edged	4
YCbCr	4:4:4	24/30/36	Seperate	1X	4
		12/15/18	Seperate	Dual-edged	9
		24/30/36	Seperate	0.5X, Dual-edged	4
	4:2:2	16/20/24	Seperate	1X	5
			Embedded	1X	6
		8/10/12	Seperate	2X	8
			Embedded	2X	7

Table 3. Output video format supported by the IT6605

RGB 4:4:4 and YCbCr 4:4:4 with Separate Syncs

	RGB			YCbCr		
Pin Name	36-bit	30-bit	24-bit	36-bit	30-bit	24-bit
QE0	B0	NC	NC	Cb0	NC	NC
QE1	B1	NC	NC	Cb1	NC	NC
QE2	B2	B0	NC	Cb2	Cb0	NC
QE3	B3	B1	NC	Cb3	Cb1	NC
QE4	B4	B2	B0	Cb4	Cb2	Cb0
QE5	B5	B3	B1	Cb5	Cb3	Cb1
QE6	B6	B4	B2	Cb6	Cb4	Cb2
QE7	B7	B5	B3	Cb7	Cb5	Cb3
QE8	B8	B6	B4	Cb8	Cb6	Cb4
QE9	B9	B7	B5	Cb9	Cb7	Cb5
QE10	B10	B8	B6	Cb10	Cb8	Cb6
QE11	B11	B9	B7	Cb11	Cb9	Cb7
QE12	G0	NC	NC	Y0	NC	NC
QE13	G1	NC	NC	Y1	NC	NC
QE14	G2	G0	NC	Y2	Y0	NC
QE15	G3	G1	NC	Y3	Y1	NC
QE16	G4	G2	G0	Y4	Y2	Y0
QE17	G5	G3	G1	Y5	Y3	Y1
QE18	G6	G4	G2	Y6	Y4	Y2
QE19	G7	G5	G3	Y7	Y5	Y3
QE20	G8	G6	G4	Y8	Y6	Y4
QE21	G9	G7	G5	Y9	Y7	Y5
QE22	G10	G8	G6	Y10	Y8	Y6
QE23	G11	G9	G7	Y11	Y9	Y7
QE24	R0	NC	NC	Cr0	NC	NC
QE25	R1	NC	NC	Cr1	NC	NC
QE26	R2	R0	NC	Cr2	Cr0	NC
QE27	R3	R1	NC	Cr3	Cr1	NC
QE28	R4	R2	R0	Cr4	Cr2	Cr0
QE29	R5	R3	R1	Cr5	Cr3	Cr1
QE30	R6	R4	R2	Cr6	Cr4	Cr2
QE31	R7	R5	R3	Cr7	Cr5	Cr3
QE32	R8	R6	R4	Cr8	Cr6	Cr4
QE33	R9	R7	R5	Cr9	Cr7	Cr5
QE34	R10	R8	R6	Cr10	Cr8	Cr6
QE35	R11	R9	R7	Cr11	Cr9	Cr7
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE

Table 4. RGB & YCbCr 4:4:4 Mappings

These are the simpliest formats, with a complete definition of every pixel in each clock period. Timing

examples of 36-bit and 30-bit RGB 4:4:4 is depicted in Figure 4 and Figure 5 respectively.

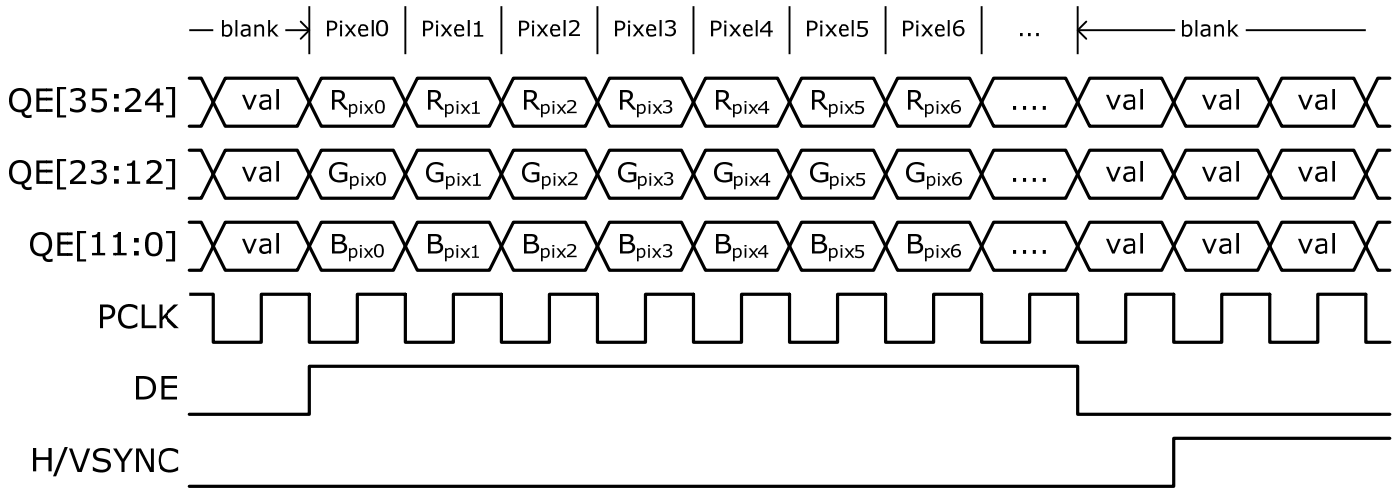


Figure 4. 36-bit RGB 4:4:4 Timing Diagram

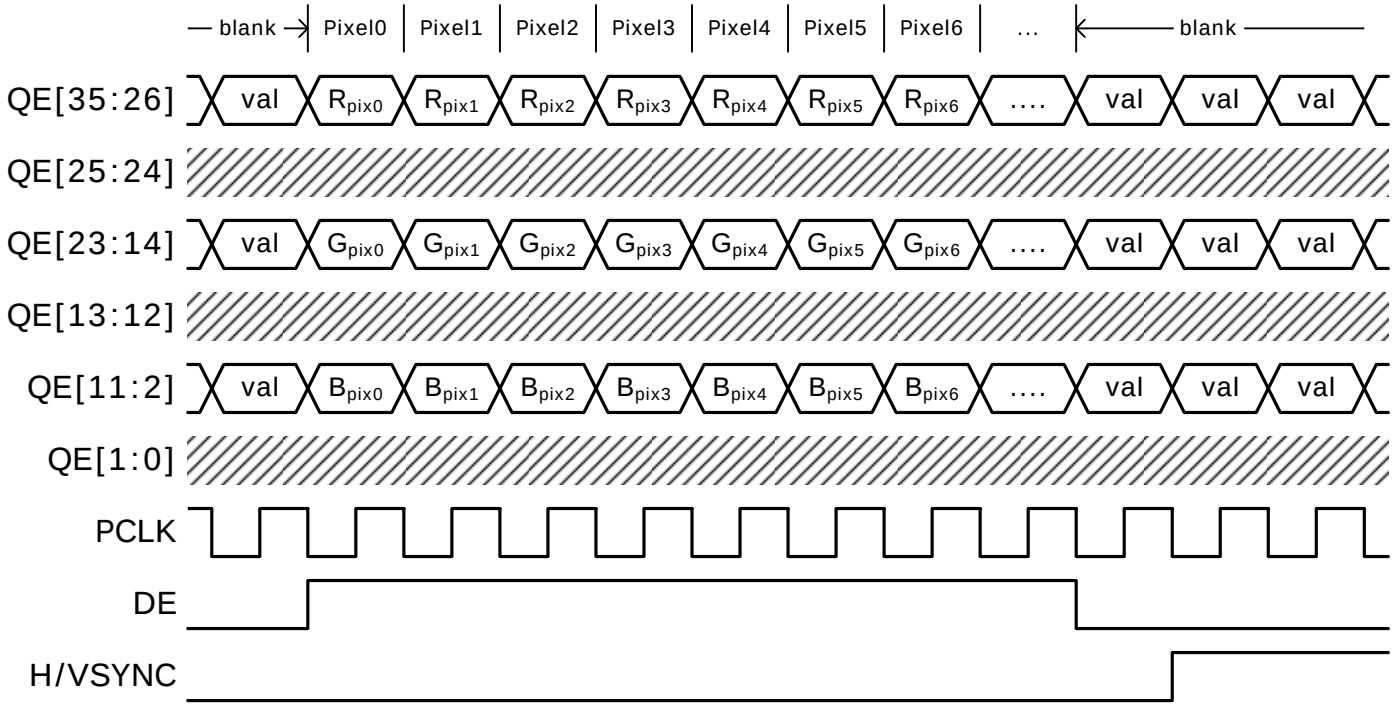


Figure 5, 30-bit RGB 4:4:4 Timing Diagram

YCbCr 4:2:2 with Separate Syncs

	24-bit		20-bit		16-bit	
Pin Name	Pixel#2N	Pixel#2N+1	Pixel#2N	Pixel#2N+1	Pixel#2N	Pixel#2N+1
QE0	NC	NC	NC	NC	NC	NC
QE1	NC	NC	NC	NC	NC	NC
QE2	NC	NC	NC	NC	NC	NC
QE3	NC	NC	NC	NC	NC	NC
QE4	NC	NC	NC	NC	NC	NC
QE5	NC	NC	NC	NC	NC	NC
QE6	NC	NC	NC	NC	NC	NC
QE7	NC	NC	NC	NC	NC	NC
QE8	NC	NC	NC	NC	NC	NC
QE9	NC	NC	NC	NC	NC	NC
QE10	NC	NC	NC	NC	NC	NC
QE11	NC	NC	NC	NC	NC	NC
QE12	Y0	Y0	NC	NC	NC	NC
QE13	Y1	Y1	NC	NC	NC	NC
QE14	Y2	Y2	Y0	Y0	NC	NC
QE15	Y3	Y3	Y1	Y1	NC	NC
QE16	Y4	Y4	Y2	Y2	Y0	Y0
QE17	Y5	Y5	Y3	Y3	Y1	Y1
QE18	Y6	Y6	Y4	Y4	Y2	Y2
QE19	Y7	Y7	Y5	Y5	Y3	Y3
QE20	Y8	Y8	Y6	Y6	Y4	Y4
QE21	Y9	Y9	Y7	Y7	Y5	Y5
QE22	Y10	Y10	Y8	Y8	Y6	Y6
QE23	Y11	Y11	Y9	Y9	Y7	Y7
QE24	Cb0	Cr0	NC	NC	NC	NC
QE25	Cb1	Cr1	NC	NC	NC	NC
QE26	Cb2	Cr2	Cb0	Cr0	NC	NC
QE27	Cb3	Cr3	Cb1	Cr1	NC	NC
QE28	Cb4	Cr4	Cb2	Cr2	Cb0	Cr0
QE29	Cb5	Cr5	Cb3	Cr3	Cb1	Cr1
QE30	Cb6	Cr6	Cb4	Cr4	Cb2	Cr2
QE31	Cb7	Cr7	Cb5	Cr5	Cb3	Cr3
QE32	Cb8	Cr8	Cb6	Cr6	Cb4	Cr4
QE33	Cb9	Cr9	Cb7	Cr7	Cb5	Cr5
QE34	Cb10	Cr10	Cb8	Cr8	Cb6	Cr6
QE35	Cb11	Cr11	Cb9	Cr9	Cb7	Cr7
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE

Table 5. Mappings of YCbCr 4:2:2 with separate syncs

YCbCr 4:2:2 format does not have one complete pixel for every clock period. Luminace channel (Y) is

given for every pixel, while the two chroma channels are given alternatively on every other clock period. The average bit amount of Y is twice that of Cb or Cr. Depending on the bus width, each component could take on different lengths. The DE period should contain an even number of clock periods. Figure 6 gives a timing example of 24-bit YCbCr 4:2:2.

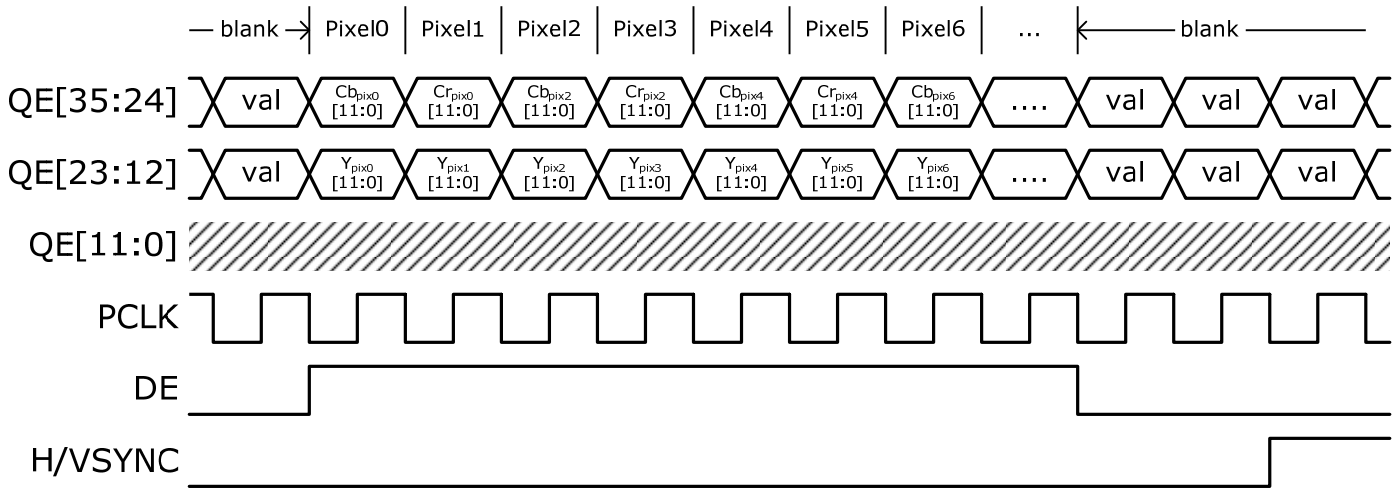


Figure 6. 24-bit YCbCr 4:2:2 with separate syncs

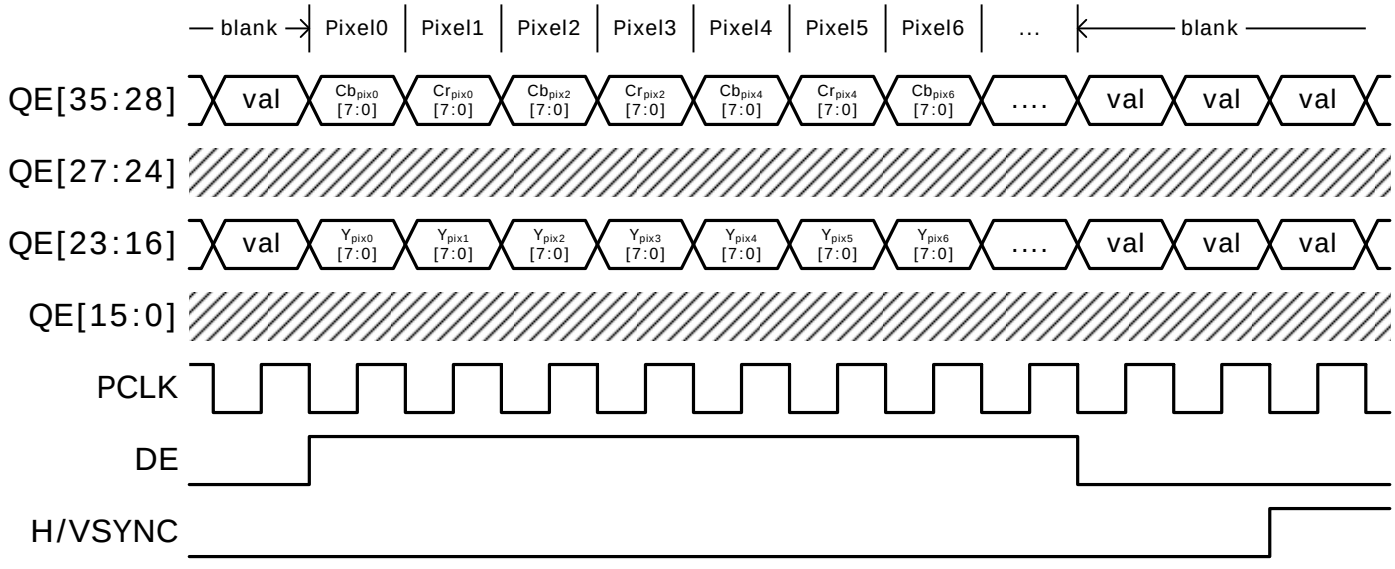


Figure 7. 16-bit YCbCr 4:2:2 with separate syncs

YCbCr 4:2:2 with Embedded Syncs

	24-bit		20-bit		16-bit	
Pin Name	Pixel#2N	Pixel#2N+1	Pixel#2N	Pixel#2N+1	Pixel#2N	Pixel#2N+1
QE0	NC	NC	NC	NC	NC	NC
QE1	NC	NC	NC	NC	NC	NC
QE2	NC	NC	NC	NC	NC	NC
QE3	NC	NC	NC	NC	NC	NC
QE4	NC	NC	NC	NC	NC	NC
QE5	NC	NC	NC	NC	NC	NC
QE6	NC	NC	NC	NC	NC	NC
QE7	NC	NC	NC	NC	NC	NC
QE8	NC	NC	NC	NC	NC	NC
QE9	NC	NC	NC	NC	NC	NC
QE10	NC	NC	NC	NC	NC	NC
QE11	NC	NC	NC	NC	NC	NC
QE12	Y0	Y0	NC	NC	NC	NC
QE13	Y1	Y1	NC	NC	NC	NC
QE14	Y2	Y2	Y0	Y0	NC	NC
QE15	Y3	Y3	Y1	Y1	NC	NC
QE16	Y4	Y4	Y2	Y2	Y0	Y0
QE17	Y5	Y5	Y3	Y3	Y1	Y1
QE18	Y6	Y6	Y4	Y4	Y2	Y2
QE19	Y7	Y7	Y5	Y5	Y3	Y3
QE20	Y8	Y8	Y6	Y6	Y4	Y4
QE21	Y9	Y9	Y7	Y7	Y5	Y5
QE22	Y10	Y10	Y8	Y8	Y6	Y6
QE23	Y11	Y11	Y9	Y9	Y7	Y7
QE24	Cb0	Cr0	NC	NC	NC	NC
QE25	Cb1	Cr1	NC	NC	NC	NC
QE26	Cb2	Cr2	Cb0	Cr0	NC	NC
QE27	Cb3	Cr3	Cb1	Cr1	NC	NC
QE28	Cb4	Cr4	Cb2	Cr2	Cb0	Cr0
QE29	Cb5	Cr5	Cb3	Cr3	Cb1	Cr1
QE30	Cb6	Cr6	Cb4	Cr4	Cb2	Cr2
QE31	Cb7	Cr7	Cb5	Cr5	Cb3	Cr3
QE32	Cb8	Cr8	Cb6	Cr6	Cb4	Cr4
QE33	Cb9	Cr9	Cb7	Cr7	Cb5	Cr5
QE34	Cb10	Cr10	Cb8	Cr8	Cb6	Cr6
QE35	Cb11	Cr11	Cb9	Cr9	Cb7	Cr7
HSYNC	embedded	embedded	embedded	embedded	embedded	embedded
VSYNC	embedded	embedded	embedded	embedded	embedded	embedded
DE	embedded	embedded	embedded	embedded	embedded	embedded

Table 6. Mappings of YCbCr 4:2:2 with embedded syncs

Similar to YCbCr 4:2:2 with Separate Sync. The only difference is that the syncs are now non-explicit,

i.e. embedded. Bus width could be 16-bit, 20-bit or 24-bit. Figure 8 gives a timing example of 24-bit YCbCr 4:2:2 and Figure 9 that of 16-bit. Note that while "embedded syncs" implies that neither DE nor H/VSYNC are required, the IT6605 optionally output these signals via proper register setting to ease the design for some backend processors.

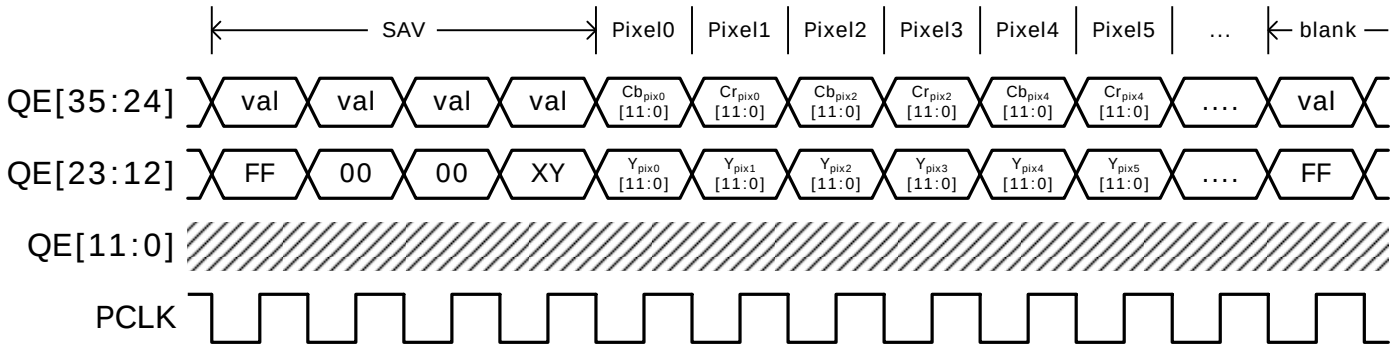


Figure 8. 24-bit YCbCr 4:2:2 with embedded syncs

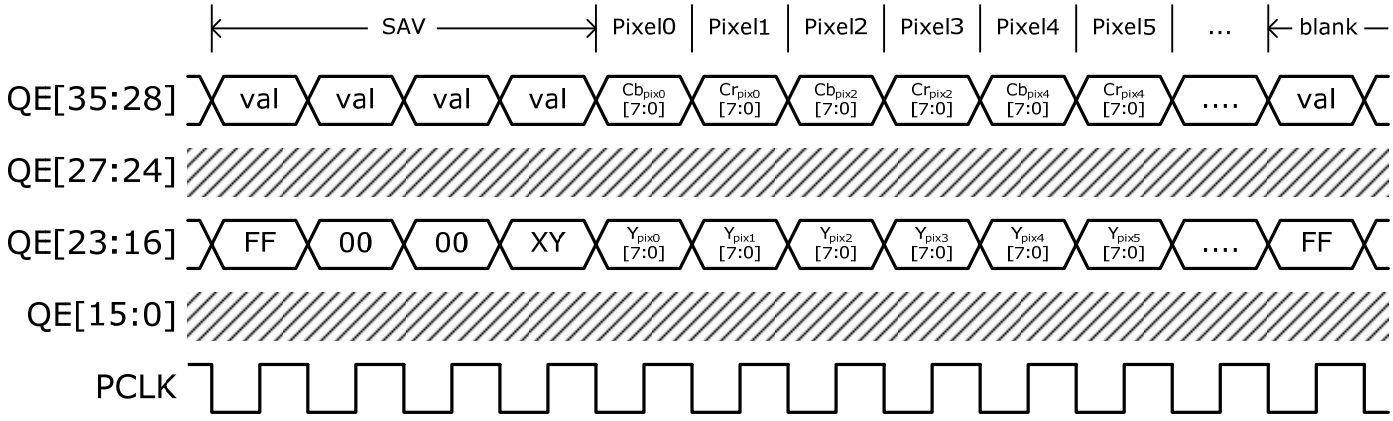


Figure 9. 16-bit YCbCr 4:2:2 with embedded syncs

CCIR-656 Format

	12-bit		10-bit		8-bit	
Pin Name	PCLK#2N	PCLK#2N+1	PCLK#2N	PCLK#2N+1	PCLK#2N	PCLK#2N+1
QE0	NC	NC	NC	NC	NC	NC
QE1	NC	NC	NC	NC	NC	NC
QE2	NC	NC	NC	NC	NC	NC
QE3	NC	NC	NC	NC	NC	NC
QE4	NC	NC	NC	NC	NC	NC
QE5	NC	NC	NC	NC	NC	NC
QE6	NC	NC	NC	NC	NC	NC
QE7	NC	NC	NC	NC	NC	NC
QE8	NC	NC	NC	NC	NC	NC
QE9	NC	NC	NC	NC	NC	NC
QE10	NC	NC	NC	NC	NC	NC
QE11	NC	NC	NC	NC	NC	NC
QE12	C0	Y0	NC	NC	NC	NC
QE13	C1	Y1	NC	NC	NC	NC
QE14	C2	Y2	C0	Y0	NC	NC
QE15	C3	Y3	C1	Y1	NC	NC
QE16	C4	Y4	C2	Y2	C0	Y0
QE17	C5	Y5	C3	Y3	C1	Y1
QE18	C6	Y6	C4	Y4	C2	Y2
QE19	C7	Y7	C5	Y5	C3	Y3
QE20	C8	Y8	C6	Y6	C4	Y4
QE21	C9	Y9	C7	Y7	C5	Y5
QE22	C10	Y10	C8	Y8	C6	Y6
QE23	C11	Y11	C9	Y9	C7	Y7
QE24	NC	NC	NC	NC	NC	NC
QE25	NC	NC	NC	NC	NC	NC
QE26	NC	NC	NC	NC	NC	NC
QE27	NC	NC	NC	NC	NC	NC
QE28	NC	NC	NC	NC	NC	NC
QE29	NC	NC	NC	NC	NC	NC
QE30	NC	NC	NC	NC	NC	NC
QE31	NC	NC	NC	NC	NC	NC
QE32	NC	NC	NC	NC	NC	NC
QE33	NC	NC	NC	NC	NC	NC
QE34	NC	NC	NC	NC	NC	NC
QE35	NC	NC	NC	NC	NC	NC
HSYNC	embedded	embedded	embedded	embedded	embedded	embedded
VSYNC	embedded	embedded	embedded	embedded	embedded	embedded
DE	embedded	embedded	embedded	embedded	embedded	embedded

Table 7. Mappings of CCIR-656

The CCIR-656 format is yet another variation of the YCbCr formats. The bus width is further reduced

by half compared from the previous YCbCr 4:2:2 formats, to either 8-bit, 10-bit or 12-bit. To compensate for the halving of data bus, PCLK frequency is doubled. With the double-rate output clock, luminance channel (Y) and chroma channels (Cb or Cr) are alternated. The syncs signals are embedded in the Y-channel. Normally this format is used only for 480i, 480p, 576i and 576p. The IT6605 supports CCIR-656 format of up to 720p or 1080i, with the doubled-rate clock running at 148.5MHz. CCIR-656 format supports embedded syncs only. Figure 10 and Figure 11 give examples of 12-bit and 8-bit CCIR-656 respectively. Note that while "embedded syncs" implies that neither DE nor H/VSYNC are required, the IT6605 optionally output these signals via proper register setting to ease the design for some backend processors.

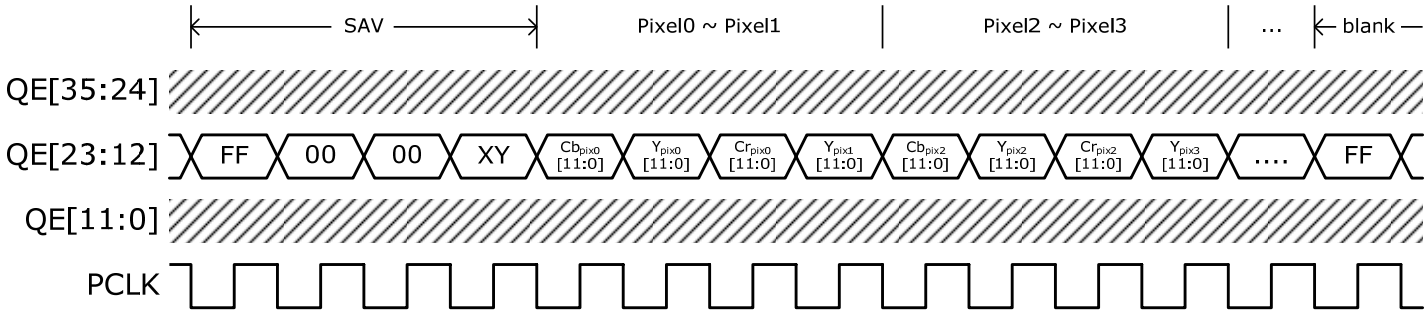


Figure 10. 12-bit CCIR-656

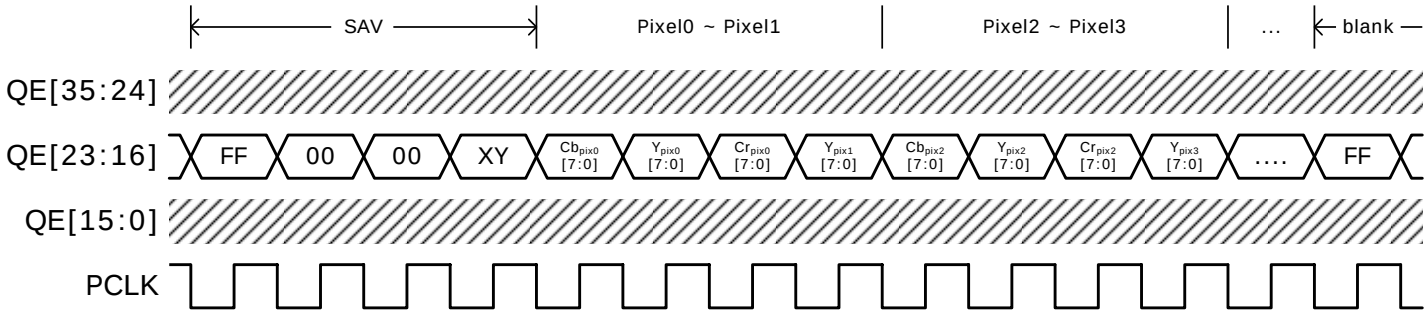


Figure 11. 8-bit CCIR-656

CCIR-656 + separate syncs

	12-bit		10-bit		8-bit	
Pin Name	PCLK#2N	PCLK#2N+1	PCLK#2N	PCLK#2N+1	PCLK#2N	PCLK#2N+1
QE0	NC	NC	NC	NC	NC	NC
QE1	NC	NC	NC	NC	NC	NC
QE2	NC	NC	NC	NC	NC	NC
QE3	NC	NC	NC	NC	NC	NC
QE4	NC	NC	NC	NC	NC	NC
QE5	NC	NC	NC	NC	NC	NC
QE6	NC	NC	NC	NC	NC	NC
QE7	NC	NC	NC	NC	NC	NC
QE8	NC	NC	NC	NC	NC	NC
QE9	NC	NC	NC	NC	NC	NC
QE10	NC	NC	NC	NC	NC	NC
QE11	NC	NC	NC	NC	NC	NC
QE12	C0	Y0	NC	NC	NC	NC
QE13	C1	Y1	NC	NC	NC	NC
QE14	C2	Y2	C0	Y0	NC	NC
QE15	C3	Y3	C1	Y1	NC	NC
QE16	C4	Y4	C2	Y2	C0	Y0
QE17	C5	Y5	C3	Y3	C1	Y1
QE18	C6	Y6	C4	Y4	C2	Y2
QE19	C7	Y7	C5	Y5	C3	Y3
QE20	C8	Y8	C6	Y6	C4	Y4
QE21	C9	Y9	C7	Y7	C5	Y5
QE22	C10	Y10	C8	Y8	C6	Y6
QE23	C11	Y11	C9	Y9	C7	Y7
QE24	NC	NC	NC	NC	NC	NC
QE25	NC	NC	NC	NC	NC	NC
QE26	NC	NC	NC	NC	NC	NC
QE27	NC	NC	NC	NC	NC	NC
QE28	NC	NC	NC	NC	NC	NC
QE29	NC	NC	NC	NC	NC	NC
QE30	NC	NC	NC	NC	NC	NC
QE31	NC	NC	NC	NC	NC	NC
QE32	NC	NC	NC	NC	NC	NC
QE33	NC	NC	NC	NC	NC	NC
QE34	NC	NC	NC	NC	NC	NC
QE35	NC	NC	NC	NC	NC	NC
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE

Table 8. Mappings of CCIR-656 + separate syncs

This format is not specified by CCIR-656. It's simply the previously mentioned CCIR-656 format plus

separate syncs. Examples of this mode are given in Figure 12 and Figure 13.

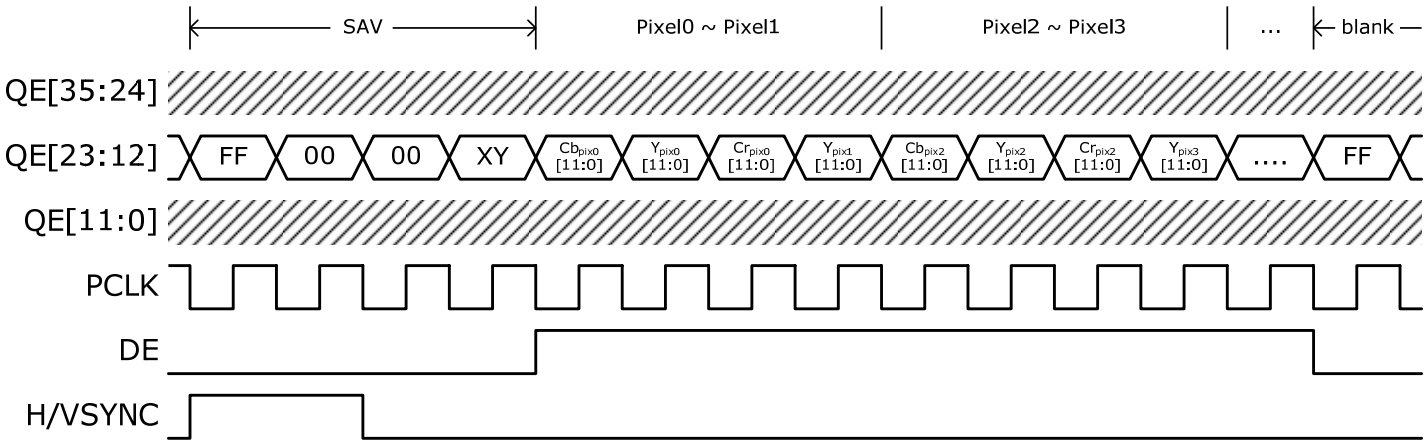


Figure 12. 12-bit CCIR-656 + separate syncs

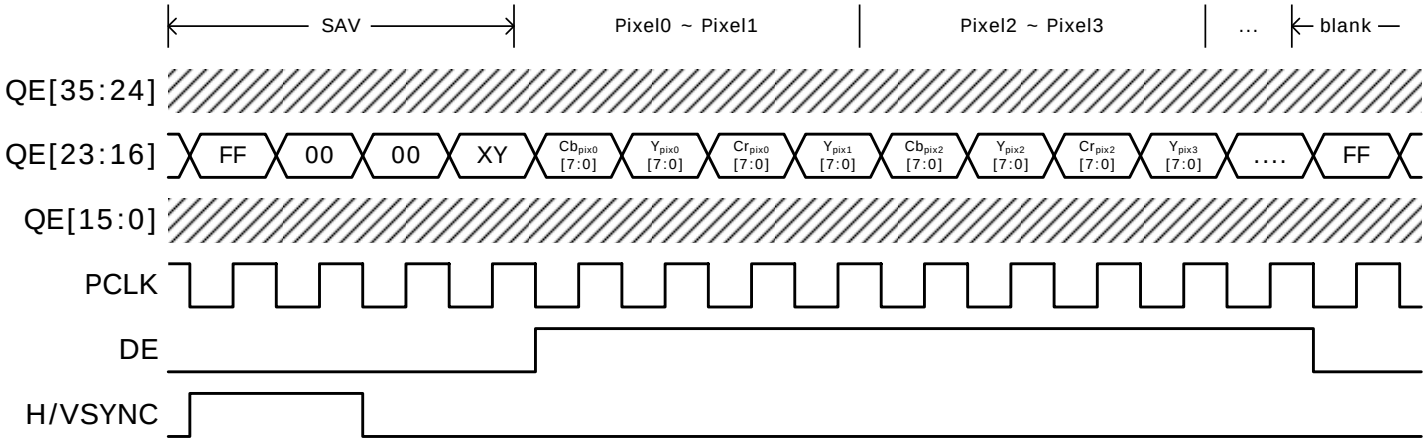


Figure 13. 8-bit CCIR-656 + separate syncs

12/15/18-bit RGB 4:4:4 and YCbCr 4:4:4 Using Dual-Edge Triggering

	RGB						YCbCr					
	18-bit		15-bit		12-bit		18-bit		15-bit		12-bit	
Pin Name	1st edge	2nd edge	1st edge	2nd edge	1st edge	2nd edge	1st edge	2nd edge	1st edge	2nd edge	1st edge	2nd edge
QE0	B0	G6	NC	NC	NC	NC	Cb0	Y6	NC	NC	NC	NC
QE1	B1	G7	NC	NC	NC	NC	Cb1	Y7	NC	NC	NC	NC
QE2	B2	G8	NC	NC	NC	NC	Cb2	Y8	NC	NC	NC	NC
QE3	B3	G9	B0	G5	NC	NC	Cb3	Y9	Cb0	Y5	NC	NC
QE4	B4	G10	B1	G6	NC	NC	Cb4	Y10	Cb1	Y6	NC	NC
QE5	B5	G11	B2	G7	NC	NC	Cb5	Y11	Cb2	Y7	NC	NC
QE6	B6	R0	B3	G8	B0	G4	Cb6	Cr0	Cb3	Y8	Cb0	Y4
QE7	B7	R1	B4	G9	B1	G5	Cb7	Cr1	Cb4	Y9	Cb1	Y5
QE8	B8	R2	B5	R0	B2	G6	Cb8	Cr2	Cb5	Cr0	Cb2	Y6
QE9	B9	R3	B6	R1	B3	G7	Cb9	Cr3	Cb6	Cr1	Cb3	Y7
QE10	B10	R4	B7	R2	B4	R0	Cb10	Cr4	Cb7	Cr2	Cb4	Cr0
QE11	B11	R5	B8	R3	B5	R1	Cb11	Cr5	Cb8	Cr3	Cb5	Cr1
QE12	G0	R6	B9	R4	B6	R2	Y0	Cr6	Cb9	Cr4	Cb6	Cr2
QE13	G1	R7	G0	R5	B7	R3	Y1	Cr7	Y0	Cr5	Cb7	Cr3
QE14	G2	R8	G1	R6	G0	R4	Y2	Cr8	Y1	Cr6	Y0	Cr4
QE15	G3	R9	G2	R7	G1	R5	Y3	Cr9	Y2	Cr7	Y1	Cr5
QE16	G4	R10	G3	R8	G2	R6	Y4	Cr10	Y3	Cr8	Y2	Cr6
QE17	G5	R11	G4	R9	G3	R7	Y5	Cr11	Y4	Cr9	Y3	Cr7
QE18	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
QE19	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
QE20	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
QE21	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
QE22	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
QE23	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
QE24	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
QE25	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
QE26	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
QE27	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
QE28	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
QE29	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
QE30	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
QE31	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
QE32	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
QE33	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
QE34	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
QE35	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE

Table 9. Mappings of 12/15/18-bit 4:4:4 dual-edge triggered

In this double-edge triggering mode, PCLK frequency remains at the nominal pixel clock rate. The halved data pins, however, run at a data rate double that of the nominal pixel clock rate. Each set of data are clocked out by the rising edge and the falling edge alternatively. Overall one complete pixel is output within one PCLK period. Figure 14 and Figure 15 give examples of 18-bit and 12-bit RGB 4:4:4 Dual-Edge Triggered output respectively.

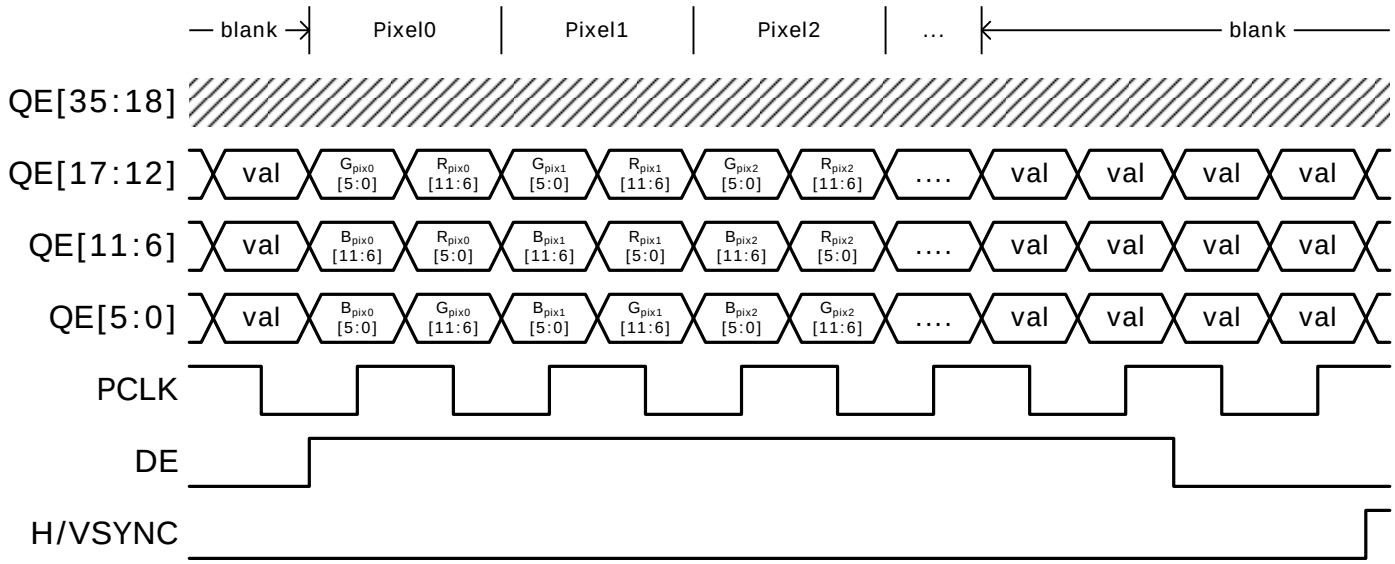


Figure 14. 18-bit RGB 4:4:4 dual-edge triggered

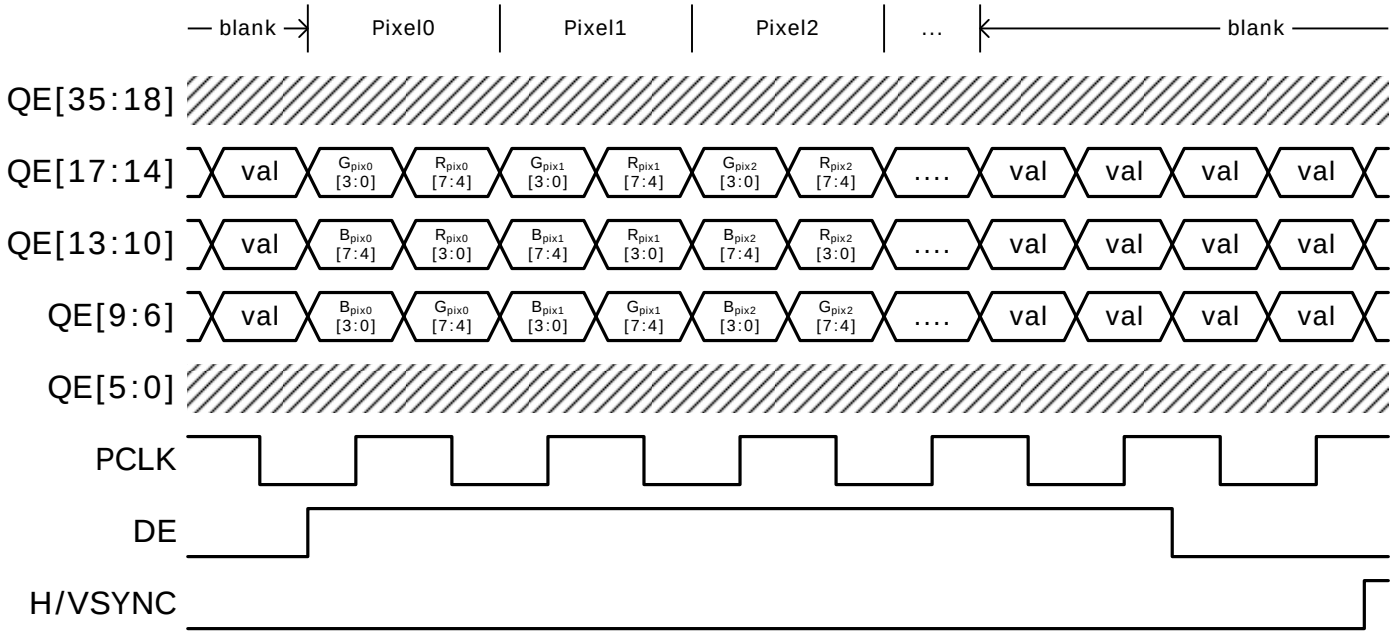


Figure 15. 12-bit RGB 4:4:4 dual-edge triggered

RGB 4:4:4 and YCbCr 4:4:4 Triggered with 0.5X PCLK at Dual Edges

The bus mapping in this format is the same as that of RGB 4:4:4 and YCbCr 4:4:4 with Separate Syncs. The only difference is that the output video clock (PCLK) is now halved in frequency. The data are in turn to be latched in with both the rising and falling edges of the 0.5X PCLK.

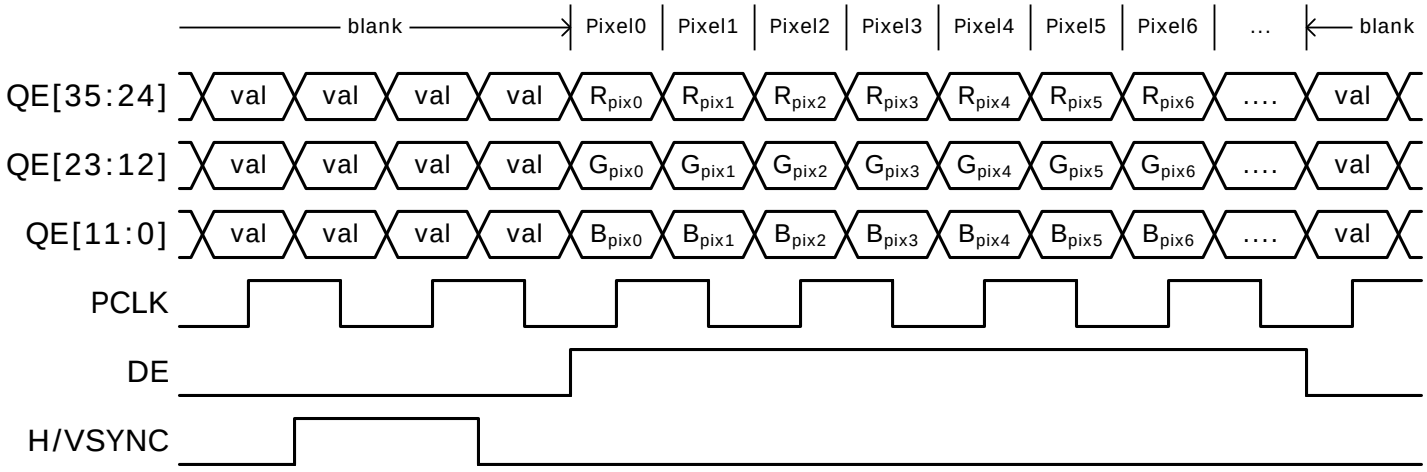


Figure 16. 36-bit RGB 4:4:4 dual-edges triggered with 0.5X PCLK

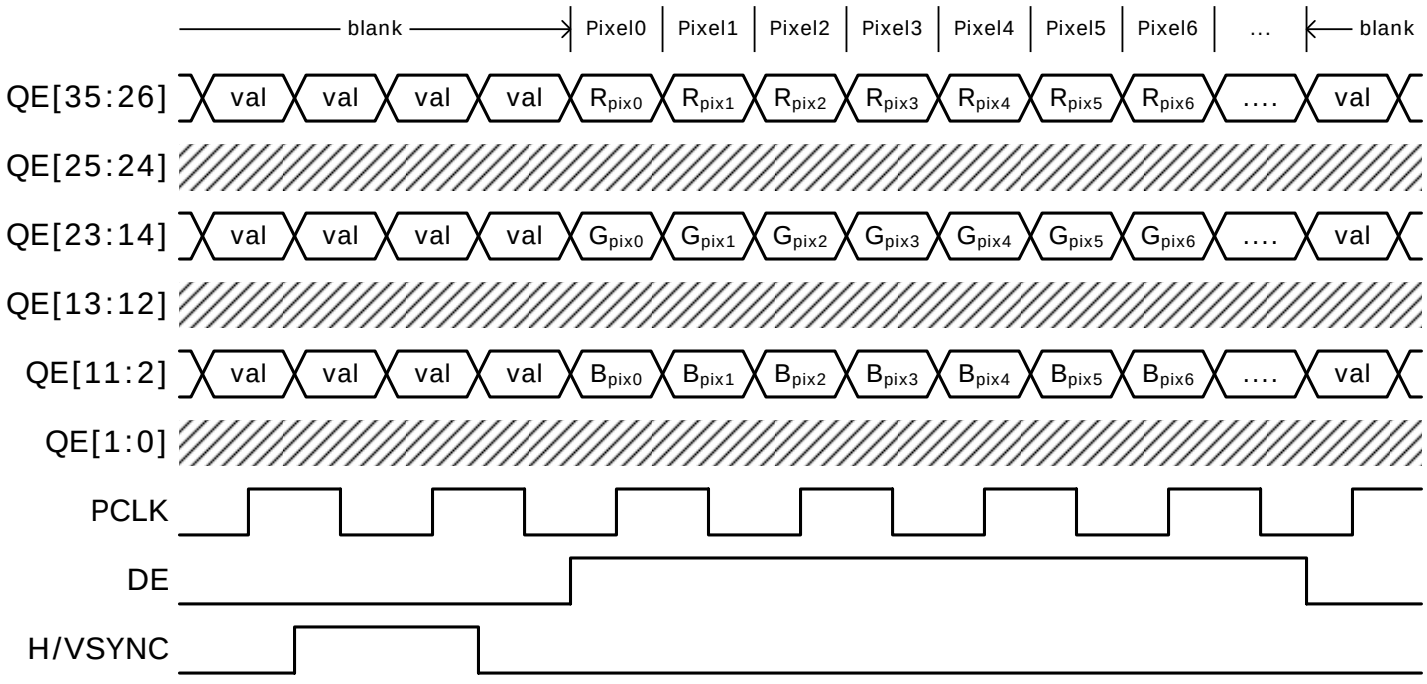


Figure 17. 30-bit RGB 4:4:4 dual-edges triggered with 0.5X PCLK

System Design Consideration

The IT6605 is a very high-speed interface chip. It receives TMDS differential signals at as high as 2.25Gbps and output TTL signals at up to 148.5MHz with 36-bit data bus. At such high speeds any PCB design imperfection could lead to compromised signal integrity and hence degraded performance. To get the optimum performance the system designers sould follow the guideline below when designing the application circuits and PCB layout.

1. Pin 54 (PVCC18) and Pin 53 (PVSS) should be supplied with clean power: ferrite-decoupled and capacitively-bypassed, since they supply the power for the receiver PLL, which is a crucial block in terms of receiving quality. Excess power noise might degrade the system performance.

2. It is highly recommended that all power pins are decoupled to ground pins via capacitors of 0.01uF and 0.1uF. Low-ESL capacitors are prefered. Generally these capacitors should be placed on the same side of the PCB with the IT6605 and as close to the pins as possible, preferably within 0.5cm from the pins. It is also recommended that the power and ground traces run relatively short distances and are connected directly to respecitve power and ground planes through via holes.

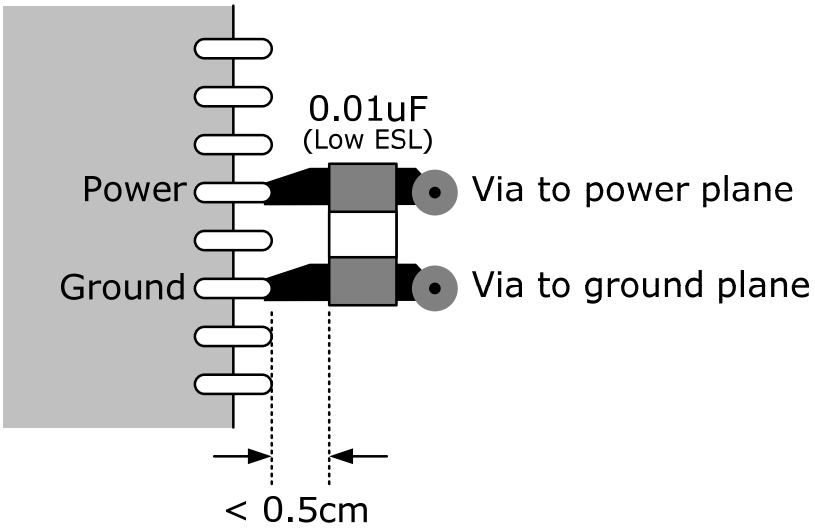


Figure 18. Layout example for decoupling capacitors.

3. The IT6605 supports 36-bit output bus running at as high as 148.5MHz. To maintain signal integrity and lower EMI, the following guidelines should be followed:

A. Employ **4-layer PCB** design, where a ground or power plane is directly placed under the signal buses at middle layes. The ground and power planes underneath these buses should be continuous in order to provide a solid return path for EM-wave introduced currents.

B. Whenever possible, keep all TTL signal traces on the same layer with the IT6605 and the

backend scalers.

C. TTL output traces to the scaler should be kept as short as possible
D. 33Ω resistors could be placed in series to the output pins. This slow down the signal rising edges, reduces current spikes and lower the reflections.
E. The PCLK signal should be kept away from other signal traces to avoid crosstalk interference. A general guideline is 2X the dielectric thickness. For example, if the dielectric layer between the signal layer and the immediate power/ground layer is 7 mil, then the PCLK trace should be kept at least 14 mil away from all other signal traces.

4. The characteristic impedance of all differential PCB traces should be kept at 100Ω all the way from the HDMI connector to the IT6605. This is crucial to the system performance at high speeds. When layouting these differential transmission lines, the following guidelines should be followed:

A. The signals traces should be on the outside layers (TOP layer or BOTTOM layer) while beneath it there should be a continuous ground plane in order to maintain the so-called micro-strip transmission line structure, giving stable and well-defined characteristic impedances.
B. Carefully choose the width and spacing of the differential transmission lines as their characteristic impedance depends on various parameters of the PCB: trace width, trace spacing, copper thickness, dielectric constant, dielectric thickness, etc. Careful 3D EM simulation is the best way to derive a correct dimension that enables a nominal 100Ω differential impedance.
C. Cornering, through holes, crossing and any irregular signal routing should be minimized so as to prevent from disrupting the EM field and creating discontinuity in characteristic impedance.
D. The IT6605 should be placed as close to the HDMI connector as possible. If the distance between the chip and the connector is under 2 cm, the reflections could be kept small even if the PCB traces do not have an 100Ω characteristic impedance. The extra signal attenuation contributed by the PCB traces could be minimized, too.

5. Special care should be taken when adding discrete ESD devices to all differential PCB traces (RX2P/M, RX1P/M, RX0P/M, RXCP/M). The IT6605 is designed to provide ESD protection for up to 2kV at these pins, which is good enough to prevent damages during assembly. To meet the system EMC specification, external discrete ESD diodes might be added. But note that adding discrete ESD diodes inevitably add capacitive loads, therefore degrade the electrical performance at high speeds. If not chosen carefully, these diodes coupled with less-than-optimal layout would prevent the system from passing the SINK TMDS-Differential Impedance test in the HDMI Compliance Test (Test ID 8-8). One should only use low-capacitance ESD diode to protect these high-speed pins. Commercially available devices such as Semtech's RClamp0524p that take into consideration of all aspects of designing and protecting high-speed transmission lines are recommended. *(http://www.semtech.com/*

products/product-detail.jsp?navId=H0,C2,C222,P3028).

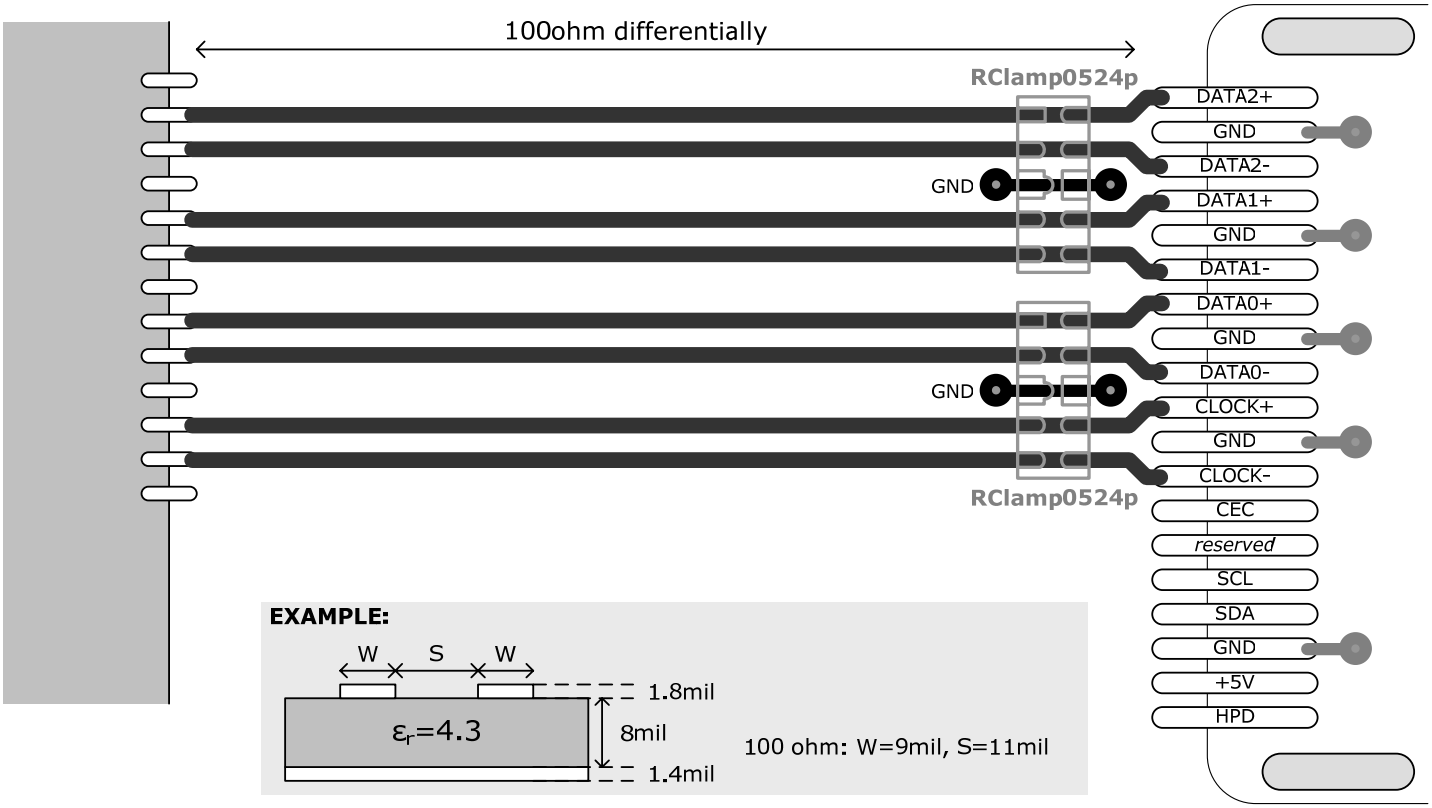
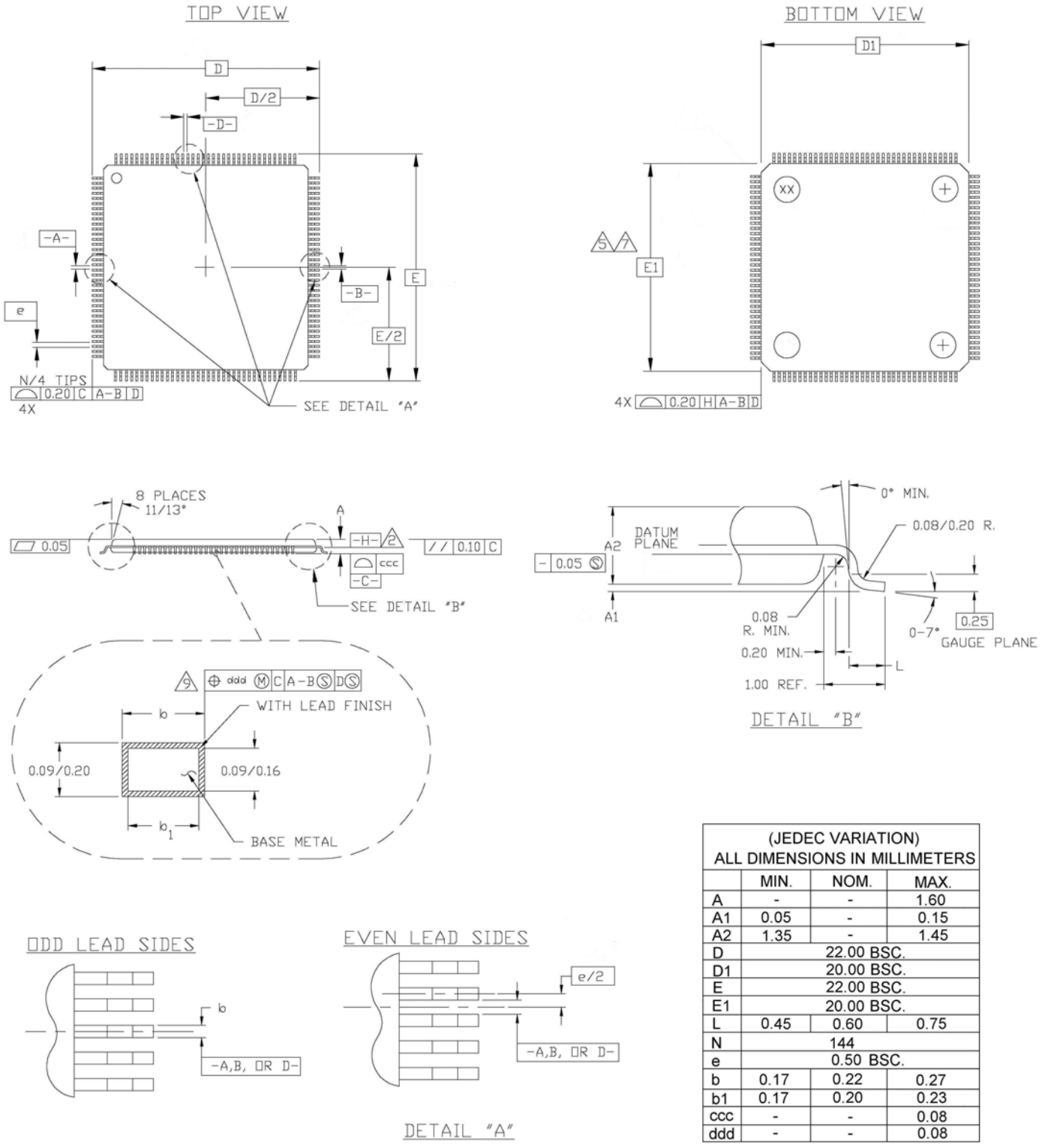


Figure 19. Layout example for high-speed TMDS differential signals

6. By default Pin 55 (REXT) should be connected to ground via a 500Ω/1% precision SMD resistor to provide for receiver termination calibration. If this pin is to be left open, be sure to set the **bit 6** of register **0x6A** to **'1'** in order to disable the termination calibration. Disabling the termination calibration would leave the value of termination impedance subject to process, supply voltage and temperature variation, sometimes rendering it out of specification and degrading the performance. Therefore it is highly recommended that this calibration function is left turned-on and a 500Ω/1% resistor is connected between Pin 55 and ground. The resistor should be placed as close to the IT6605 as possible.

Package Dimensions



(JEDEC VARIATION) ALL DIMENSIONS IN MILLIMETERS			
	MIN.	NOM.	MAX.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	-	1.45
D		22.00 BSC.	
D1		20.00 BSC.	
E		22.00 BSC.	
E1		20.00 BSC.	
L	0.45	0.60	0.75
N		144	
e		0.50 BSC.	
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
ccc	-	-	0.08
ddd	-	-	0.08

Figure 20. 144-pin LQFP Package Dimensions

Classification Reflow Profiles

Reflow Profile	Pb-Free Assembly
Average Ramp-Up Rate (Ts_{max} to Tp)	3℃/second max.
Preheat -Temperature Min(Ts_{min}) -Temperature Max(Ts_{max}) -Time(ts_{min} to ts ts_{max})	 150℃ 200℃ 60-180 seconds
Time maintained above: -Temperature(T_L) -Time(t_L)	 217℃ 60-150 seconds
Peak Temperature(Tp)	260 +0 /-5℃
Time within 5 ℃ of actual Peak Temperature(tp)	20-40 seconds
Ramp-Down Rate	6℃/second max.
Time 25℃ to Peak Temperature	8 minutes max.

Note: All Temperature refer to topside of the package, measured on the package body surface.