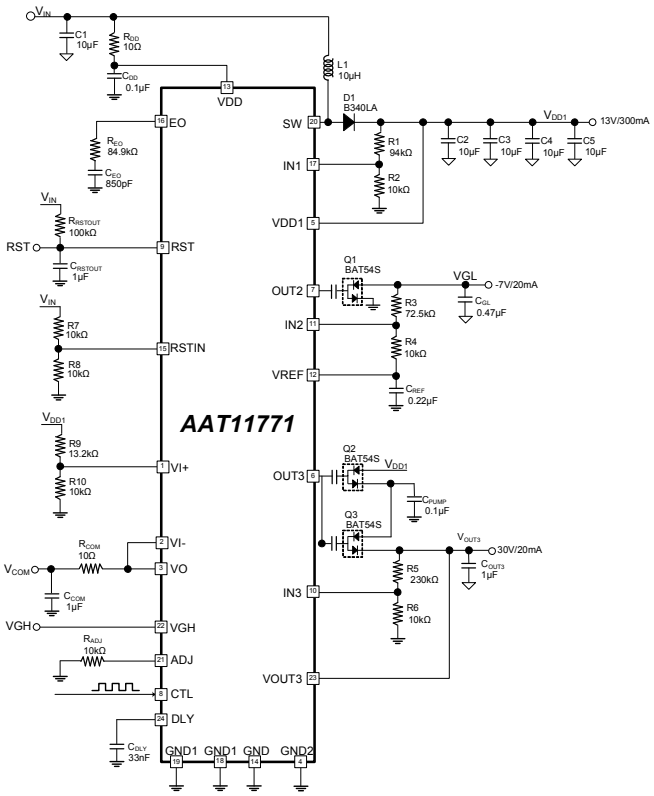
INTEGRATED TFT-LCD POWER SOLUTION

FEATURES

- **Built-in 3A, 0.2Ω Switching NMOS**
- **VGH and VGL Charge Pumps**
- **V_{COM} Operational Amplifier**
- **Adjustable VGH Delay**
- **Open-Drain Reset Output for TCON**
- **1.2MHz Fixed Switching Frequency**
- **Thermal Protection**
- **Low Dissipation Current :**
  Typical 2.3mA in Operation
- **VQFN24 4*4 Package Available**

TYPICAL APPLICATION



GENERAL DESCRIPTION

The AAT11771 provides a step-up PWM controller, dual charge pumps, V_{COM} operational amplifier, and one open drain reset output for TFT LCD displays.

The PWM controller consists of an on-chip voltage reference, oscillator, error amplifier, current sense circuit, comparator, under-voltage lockout protection and soft-start control circuit. The thermal fault protection prevents excessive current from damaging internal circuit.

Integrated charge pump controllers regulate VGH and VGL. The power on sequence of AAT11771 is:

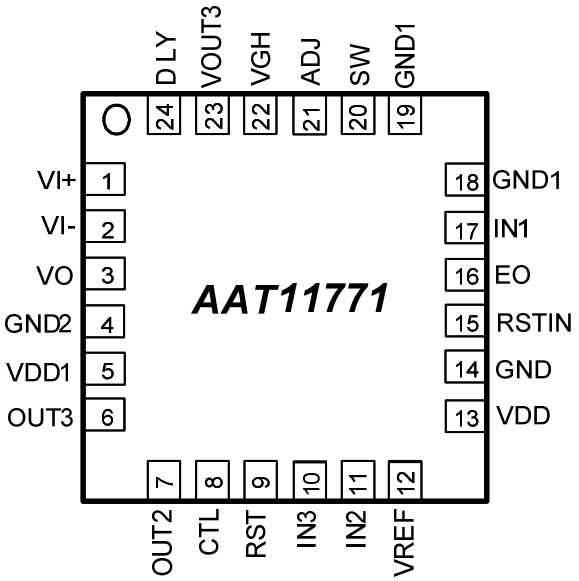
VGL → AVDD → VGH

(Please refer to the "Timing Chart" for more details.)

RST signal will keep high for 163ms and will pull low when the RSTIN falls below 1.25V after 163ms.

With the minimal external components, the AAT11771 offers a simple and economical solution for TFT LCD power management.

PIN CONFIGURATION



ORDERING INFORMATION

DEVICE TYPE	PART NUMBER	PACKAGE	PACKING	TEMP. RANGE	MARKING	MARKING DESCRIPTION
AAT11771	AAT11771-Q7-T	Q7:VQFN 24-4*4	T: Tape and Reel	–40 °C to +85 °C	AAT11771 XXXXX XXXX	Device Type Lot no. (6~9 Digits) Date Code (4 Digits)

Note: All AAT products are lead free and halogen free.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
VDD, RST to GND	V_{DD}	7	V
VDD1, AVIN, AVDD, SW to GND	V_{H1}	20	V
VOUT3 to GND	V_{H3}	36	V
Input Voltage 1 (IN1, IN2, IN3, DLY, RSTIN)	V_{I1}	V_{DD} +0.3	V
Input Voltage 2 (VI+, VI–)	V_{I2}	V_{H1} +0.3	V
Output Voltage 1 (EO, VREF)	V_{O1}	V_{DD} +0.3	V
Output Voltage 2 (VO, OUT2, OUT3)	V_{O2}	V_{H1} +0.3	V
Operating Ambient Temperature Range	T_C	–40 to +85	°C
Operating Junction Temperature Range	T_J	–40 to +150	°C
Storage Temperature Range	$T_{STORAGE}$	–65 to +150	°C
Package Thermal Range	Θ_{JA}	36	°C
Power Dissipation @ T_C = +25°C, T_J = +125°C	P_d	2.78	W

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the devices. Exposure to ABSOLUTE MAXIMUM RATINGS conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.5V to 5.5V, T_C = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature, V_{DD} = 3.3V, V_{DD1} = 10V.)

Operating Power

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
VDD Input Voltage Range	V_{DD}		2.5	-	5.5	V
VDD1 Input Voltage Range	V_{DD1}		6	-	18	V
VDD Under Voltage Lockout	V_{UVLO}	Falling	2.05	2.15	2.25	V
		Rising	2.15	2.25	2.35	
VDD Operating Current	I_{DD}	V_{IN1} = 1.5V, Not Switching	-	0.4	0.8	mA
		V_{IN1} = 1.2V, Switching	-	2.3	5.0	mA
VDD1 Operating Current	V_{DD1}	V_{VI+} = 5V	-	1.2	3.0	mA
VDD Operating Current	I_{DD}	V_{IN1} = 1.5V, Not Switching	-	0.4	0.8	mA

Reference Voltage

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Reference Voltage	V_{REF}	I_{VREF} = 100µA	1.238	1.250	1.262	V
Line Regulation		I_{VREF} = 100µA V_{DD} = 2.5V~5.5V	-	2	5	%/V
Load Regulation		I_{VREF} = 0~100µA	-	1	5	%/mA

Oscillator

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Oscillation Frequency	f_{OSC}		1.0	1.2	1.4	MHz
Maximum Duty Cycle	D_{MAX}		86	90	94	%

ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.5V to 5.5V, T_C = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature, V_{DD} = 3.3V, V_{DD1} = 10V.)

Soft Start & Fault Detect & DLY

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
PWM Soft Start Time	t_{SS1}		-	10	-	ms
VGL Soft Start Time	t_{SS2}		-	3.4	-	ms
VGH Soft Start Time	t_{SS3}		-	3.4	-	ms
During Fault Protect Trigger Time	t_{FP}		-	55	-	ms
IN1 Fault Protection Voltage	V_{f1}		0.95	1.00	1.05	V
IN2 Fault Protection Voltage	V_{f2}		0.40	0.45	0.50	V
IN3 Fault Protection Voltage	V_{f3}		0.95	1.00	1.05	V
IN1 Under Voltage Protect	V_{f4}		-	0.1	-	V

Error Amplifier (Channel 1)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Feedback Voltage	V_{IN1}		1.238	1.250	1.262	V
Input Bias Current	I_{B1}	V_{IN1} = 1V to 1.5V	–40	0	+40	nA
Feedback-Voltage Line Regulation		Level to Produce V_{EO} = 1.25V 2.3V < V_{DD} < 5.5V	-	0.05	0.15	%/V
Transconductance	G_m	ΔI = 5μA	-	85	-	μS
Voltage Gain	A_V		-	1,500	-	V/V

Switching NMOS (Channel 1)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Current Limit	I_{LIM}		2.5	3.0	-	A
On-Resistance	R_{ON1}	I_{SW} = 1.0A	-	0.2	-	Ω
Leakage Current	I_{SWOFF}	V_{SW} = 15V	-	0.01	20.00	μA

ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.5V to 5.5V, T_C = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature, V_{DD} = 3.3V, V_{DD1} = 10V.)

Charge Pump (Channel 2 and Channel 3)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VDD1 Input Supply Range	V_H		6	-	18	V
VDD1 Over Voltage Protect	V_{OVP}		-	18	20	V
Charge Pump Frequency	f_{OSCP}		500	600	700	kH_Z
IN2 Threshold Voltage	V_{H2}		235	250	265	mV
IN3 Threshold Voltage	V_{H3}		1.23	1.25	1.27	V
IN2 Input Bias Current	I_{B2}	V_{IN2} = –0.25V to 0.25V	–40	0	+40	nA
IN3 Input Bias Current	I_{B3}	V_{IN3} = 1V to 1.5V	–40	0	+40	nA
OUT2 Switch RON	R_{ONP2}		-	3	20	Ω
	R_{ONP2}		-	3	20	Ω
OUT3 Switch RON	R_{ONP3}		-	3	20	Ω
	R_{ONP2}		-	3	20	Ω

Reset Output

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
RST Output Voltage	V_{RST}	I_{RST} = 1.2mA	-	-	0.2	V
RSTIN Threshold Voltage	V_{INR}	H_{YS} = 50mV	-	1.25	-	V
RSTIN Input Current	I_{B4}		–40	0	+40	nA
RST Blanking Time	t_{BLK}		146	163	180	ms

ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.5V to 5.5V, T_C = –40°C to +85°C , unless otherwise specified. Typical values are tested at +25°C ambient temperature, V_{DD} = 3.3V, V_{DD1} = 10V.)

V_{COM} Buffer

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Input Offset Voltage	V_{OS}	V_{VI+} = 5V	-	2	15	mV
Input Bias Current	I_{B5}	$V_{VI+/}$ = 5V	–40	0	+40	nA
Output Swing	V_{OH}	I_{VO} = –50mA, V_{VI+} = 5V	-	5.03	5.06	V
		I_{VO} = 5mA, V_{VI+} = 10V	9.85	9.92	-	
	V_{OL}	I_{VO} = 50mA, V_{VI+} = 5V	4.94	4.97	-	
		I_{VO} = –5mA, V_{VI+} = 0V	-	0.08	0.15	
Short Circuit Current	I_{SHORT}	Measure I_{VO}	-	±200	-	mA
Slew Rate	SR	V_{VI+} = 2V to 8V, V_{VI+} = 8V to 2V, 20% to 80%	-	40	-	V/µs
Settling Time	t_S	V_{VI+} = 4.5V to 5.5V, 90%	-	5	-	µs

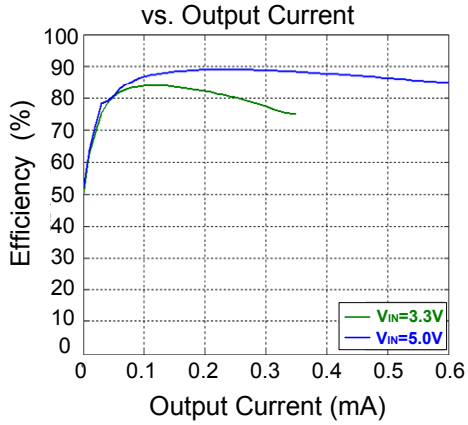
High Voltage Switch Controller

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DLY Source Current	I_{DLY}		4	5	6	µA
DLY Threshold Voltage	V_{DLY}		1.22	1.25	1.28	V
DLY Discharge RON	R_{DLY}		-	8	-	Ω
CTL Input Low Voltage	V_{IL}		-	-	0.5	V
CTL Input High Voltage	V_{IH}		2	-	-	V
CTL Input Bias Current	I_{B4}	V_{CTL} = 0 to V_{DD}	–40	0	+40	nA
Propagation Delay CTL to VGH	t_{PP}	OUT3 = 25V	-	100	-	ns
VOUT3 to VGH Switch RON	R_{ONSC}	V_{DLY} = 1.5V, V_{CTL} = V_{DD}	-	15	30	Ω
ADJ to VGH Switch RON	R_{ONDC}	V_{DLY} = 1.5V, V_{CTL} = GND	-	30	60	Ω
VGH to GND1 Switch RON	R_{ONCG}	V_{DLY} = 1V	1.5	2.5	3.5	kΩ

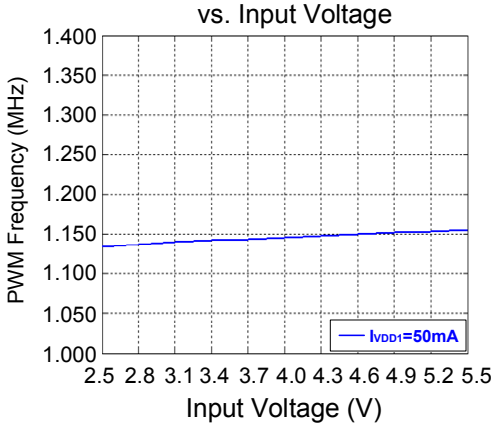
TYPICAL OPERATING CHARACTERISTICS

(V_{IN} = 5.0 V, V_{DD1} = 13 V, V_{GL} = –7 V, V_{OUT3} = 30 V, T_C = +25°C unless otherwise noted.)

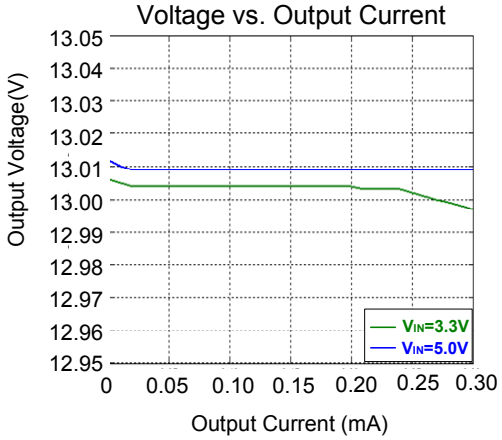
Boost Converter Efficiency vs. Output Current



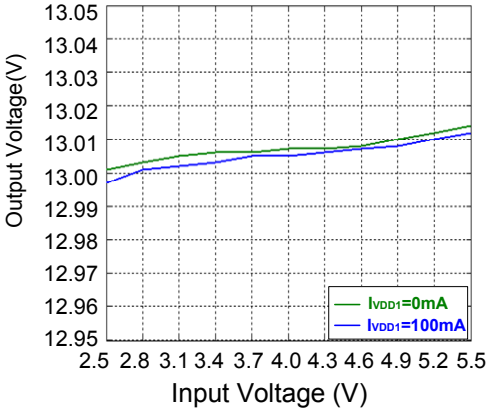
Boost Converter PWM Frequency vs. Input Voltage



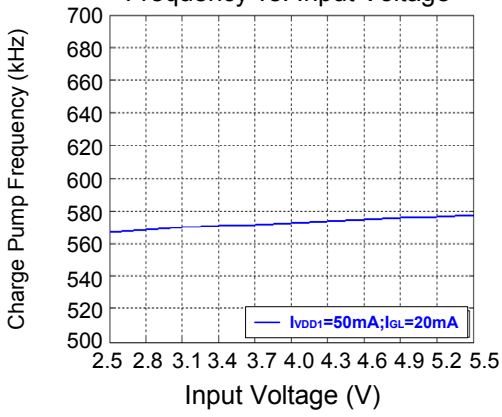
Boost Converter Output Voltage vs. Output Current



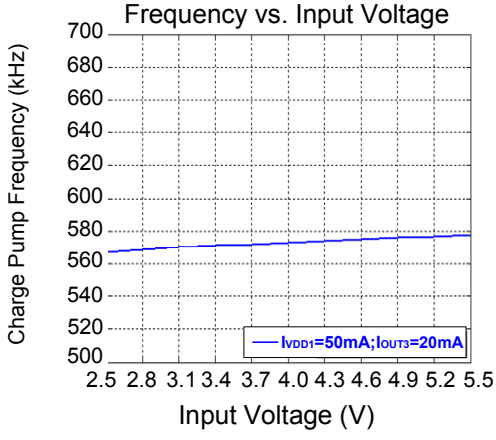
Boost Converter Output Voltage vs. Input Voltage



VGL Charge Pump Frequency vs. Input Voltage

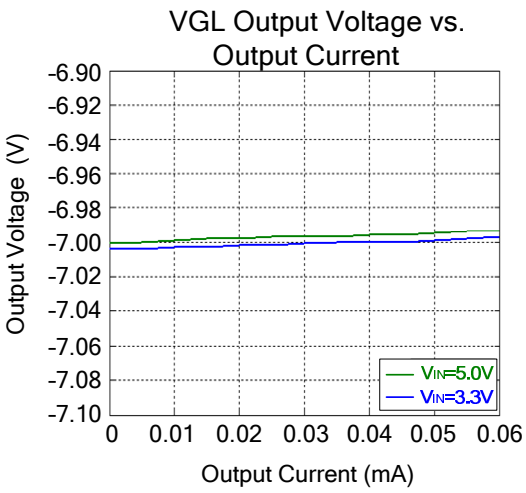


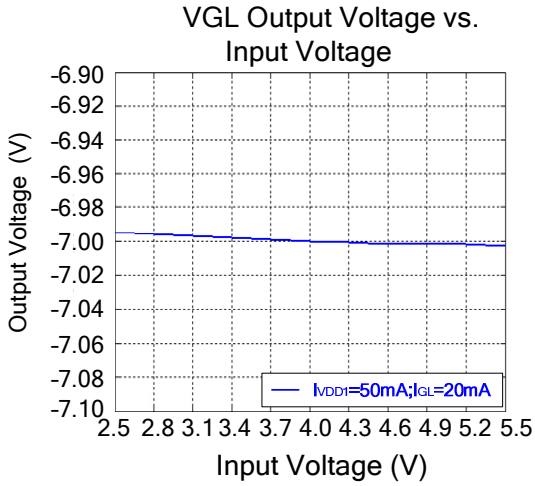
VOUT3 Charge Pump Frequency vs. Input Voltage

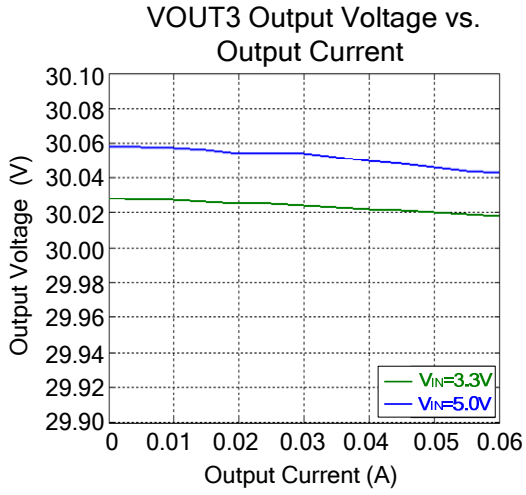


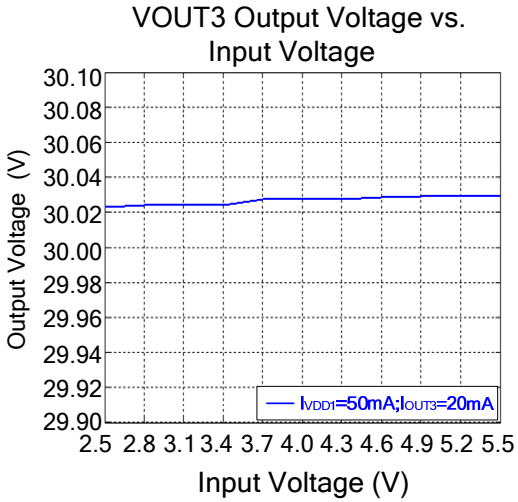
TYPICAL OPERATING CHARACTERISTICS

(V_{IN} = 5.0 V, V_{DD1} = 13 V, V_{GL} = –7 V, V_{OUT3} = 30 V, T_C = +25°C unless otherwise noted.)





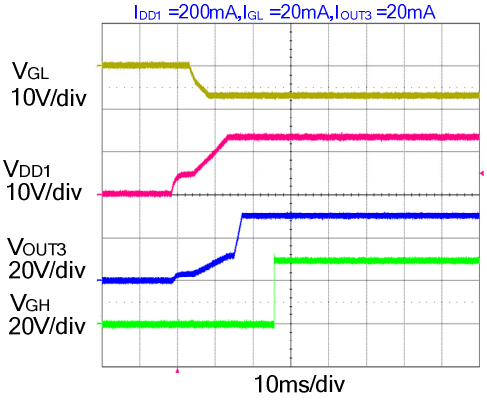




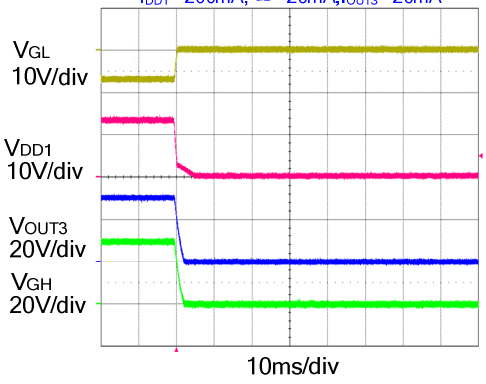
TYPICAL OPERATING CHARACTERISTICS

(V_{IN} = 5.0 V, V_{DD1} = 13 V, V_{GL} = –7V, V_{OUT3} = 30 V, T_C = +25°C unless otherwise noted.)

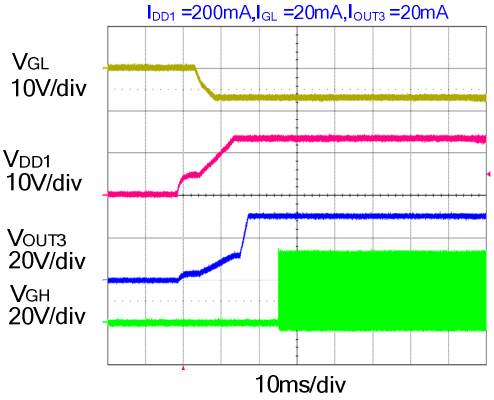
Power On Sequence
CTL=VIN, ADJ=N.C
I_{DD1} =200mA,I_{GL} =20mA,I_{OUT3} =20mA



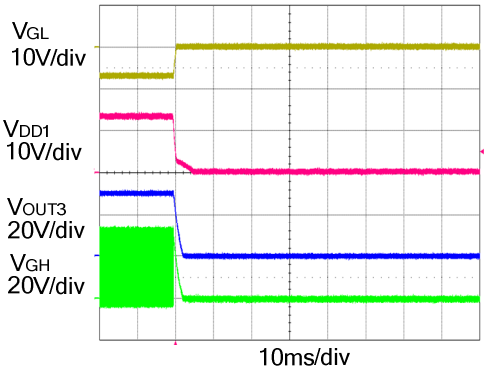
Power Off Sequence
CTL=VIN, ADJ=N.C
I_{DD1} =200mA,I_{GL} =20mA,I_{OUT3} =20mA



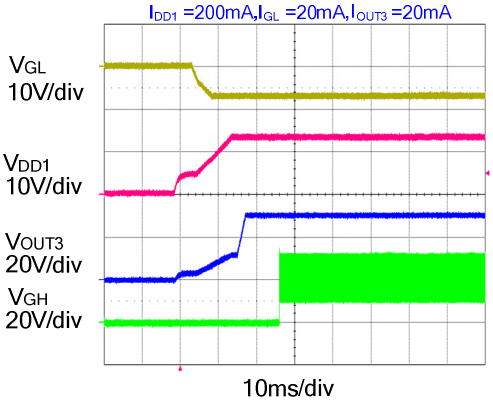
Power On Sequence
CTL=Signal, ADJ=GND
I_{DD1} =200mA,I_{GL} =20mA,I_{OUT3} =20mA



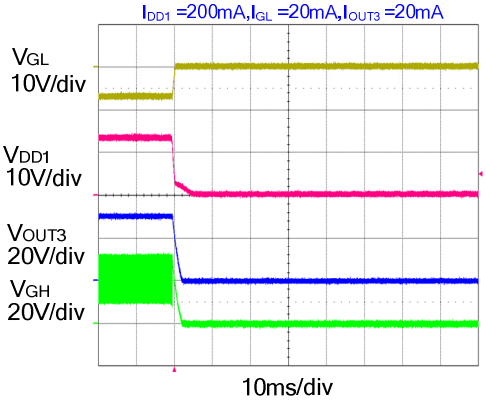
Power Off Sequence
CTL=Signal, ADJ=GND
I_{DD1} =200mA,I_{GL} =20mA,I_{OUT3} =20mA



Power On Sequence
CTL=Signal, ADJ=VDD1
I_{DD1} =200mA,I_{GL} =20mA,I_{OUT3} =20mA



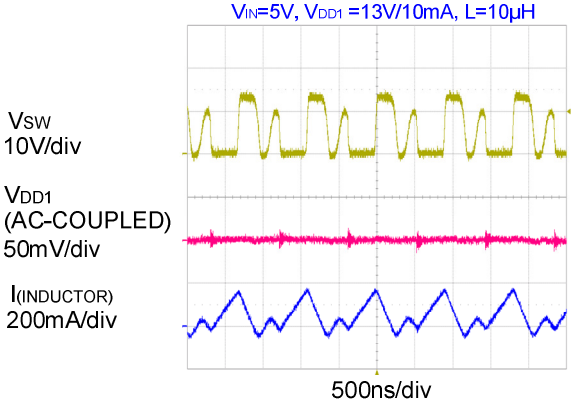
Power On Sequence
CTL=Signal, ADJ=VDD1
I_{DD1} =200mA,I_{GL} =20mA,I_{OUT3} =20mA



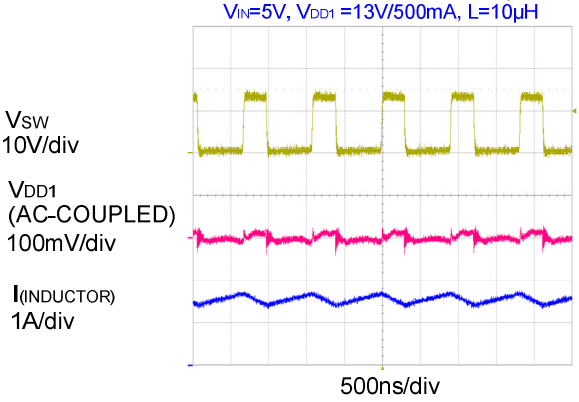
TYPICAL OPERATING CHARACTERISTICS

(V_{IN} = 5.0 V, V_{DD1} = 13 V, V_{GL} = –7 V, V_{OUT3} = 30 V, T_C = +25°C unless otherwise noted.)

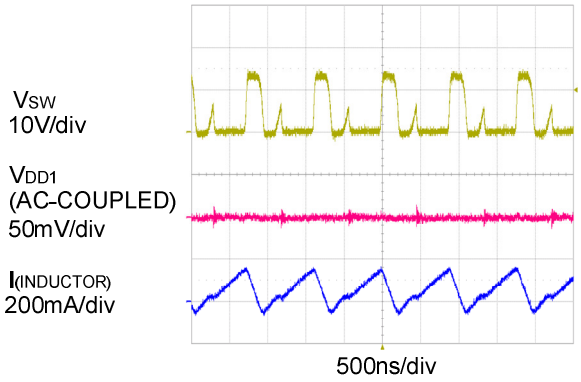
Boost Converter PWM
Discontinuous Mode: Light Load
V_{IN}=5V, V_{DD1} =13V/10mA, L=10µH



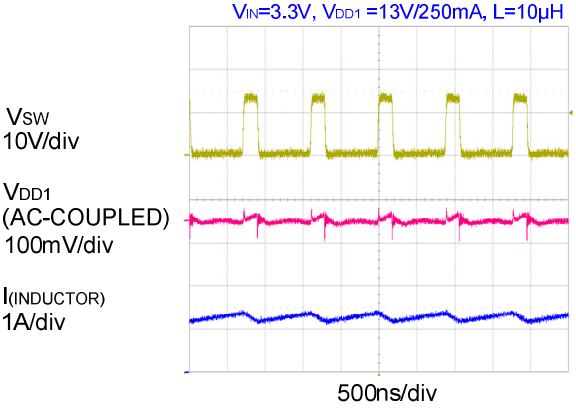
Boost Converter PWM
Discontinuous Mode: Heavy Load
V_{IN}=5V, V_{DD1} =13V/500mA, L=10µH



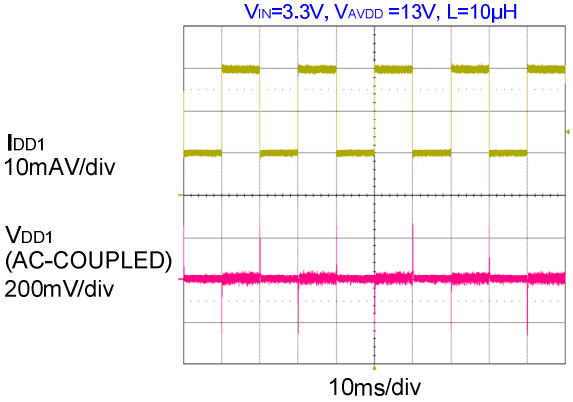
Boost Converter PWM
Discontinuous Mode: Light Load
V_{IN}=3.3V, V_{DD1} =13V/5mA, L=10µH



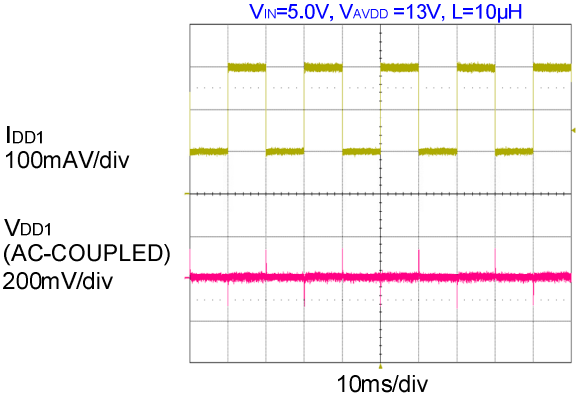
Boost Converter PWM
Discontinuous Mode: Heavy Load
V_{IN}=3.3V, V_{DD1} =13V/250mA, L=10µH



Boost Converter Load Transient
Response
V_{IN}=3.3V, V_{AVDD} =13V, L=10µH



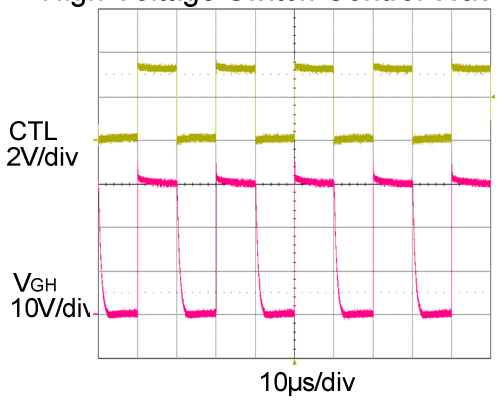
Boost Converter Load Transient
Response
V_{IN}=5.0V, V_{AVDD} =13V, L=10µH



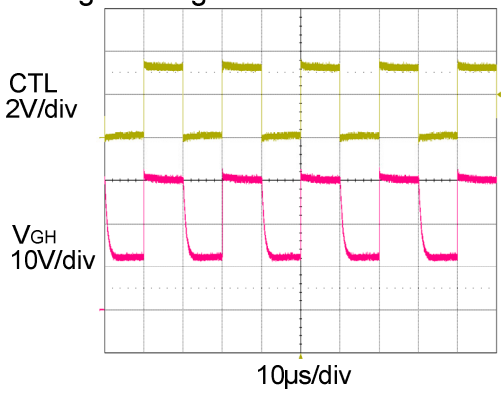
TYPICAL OPERATING CHARACTERISTICS

(V_{IN} = 5.0 V, V_{DD1} = 13 V, V_{GL} = –7 V, V_{OUT3} = 30 V, T_C = +25°C unless otherwise noted.)

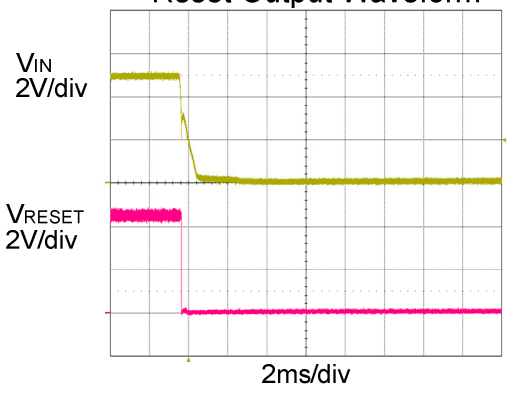
High Voltage Switch Control Waveform



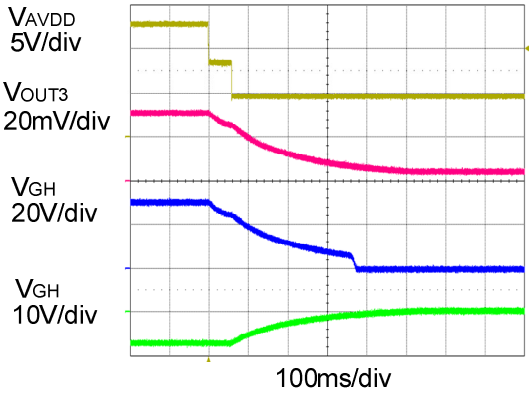
High Voltage Switch Control Waveform



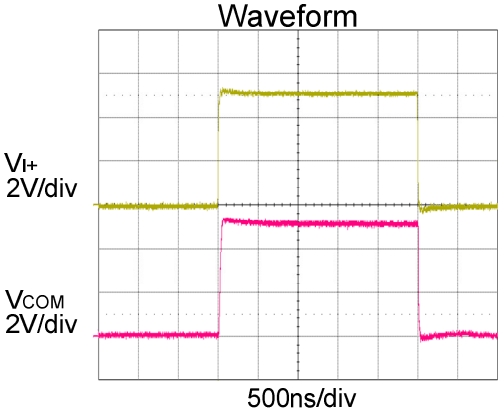
Reset Output Waveform



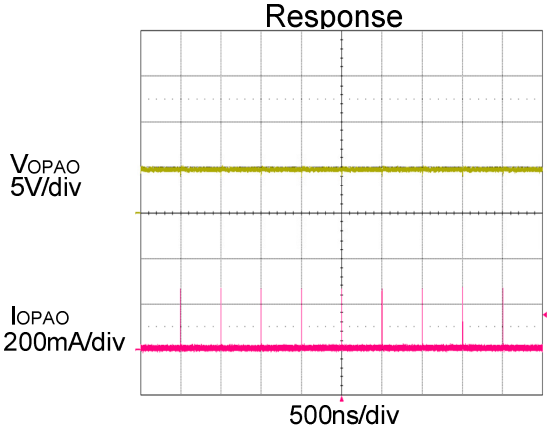
Fault Protection Waveform



VCOM Buffer Large Signal Waveform



VCOM Buffer Load Transient Response

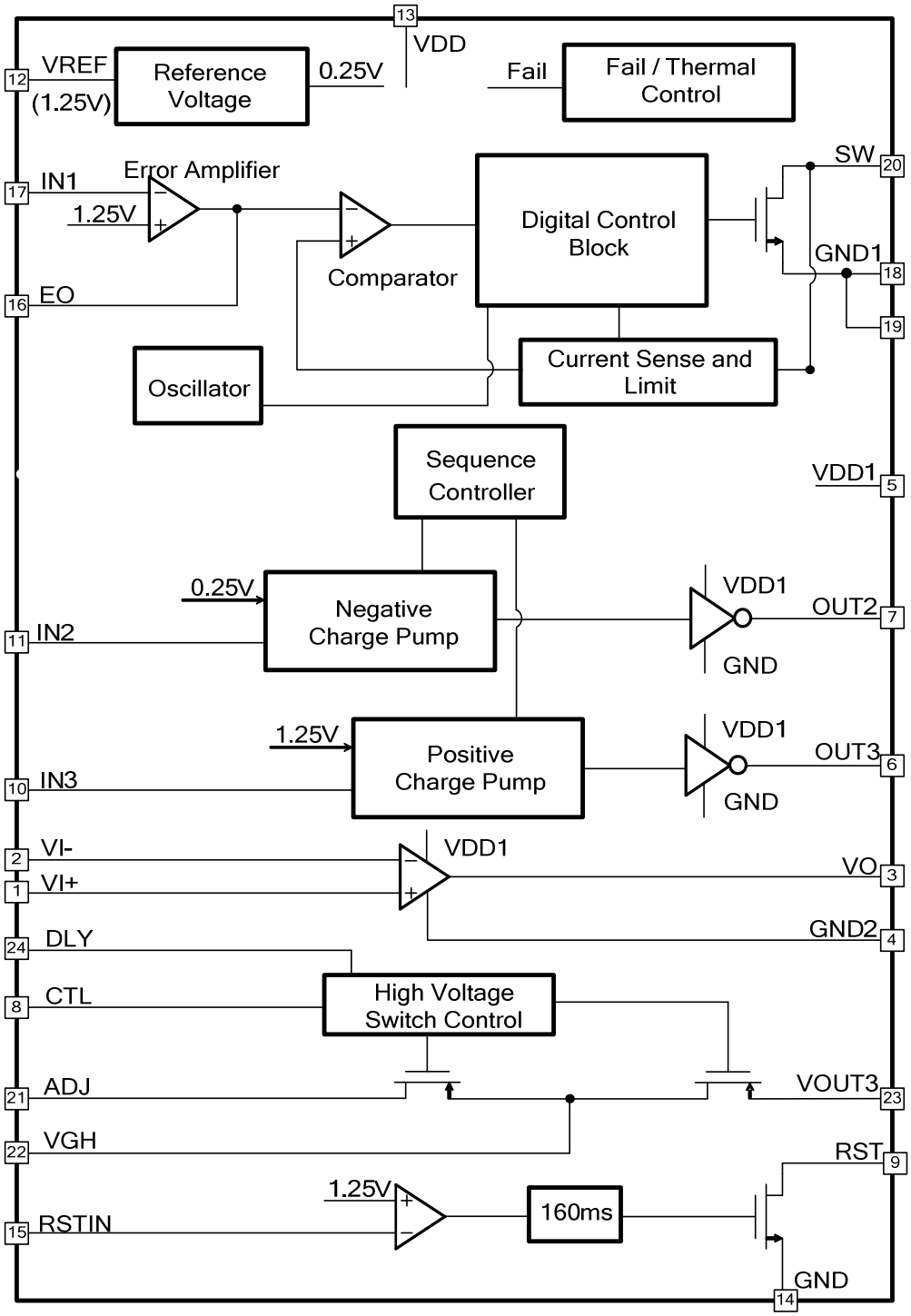


PIN DESCRIPTION

PIN NO.	NAME	I/O	DESCRIPTION
1	VI+	I	V_{COM} Buffer Positive Input
2	VI–	I	V_{COM} Buffer Negative Input
3	VO	O	V_{COM} Buffer Output
4	GND2	-	V_{COM} Buffer Ground
5	VDD1	I	V_{COM} Buffer and Charge Pump Power Supply
6	OUT3	O	Positive Charge Pump Output Pin
7	OUT2	O	Negative Charge Pump Output Pin
8	CTL	I	High Voltage Switch Control Pin
9	RST	O	Reset Signal Open Drain Output
10	IN3	I	Positive Charge Pump Feedback Pin
11	IN2	I	Negative Charge Pump Feedback Pin
12	VREF	O	Internal Reference Voltage Output
13	VDD	I	Main PWM Power Supply
14	GND	-	Analog Ground
15	RSTIN	I	Reset Comparator Input
16	EO	O	Main PWM Error Amplifier Output
17	IN1	I	Main PWM Feedback Pin
18	GND1	-	SW MOS Ground
19	GND1	-	SW MOS Ground
20	SW	-	Main PWM Switching Pin
21	ADJ	O	Gate High Voltage Fall Time Setting Pin
22	VGH	O	Switching Gate High Voltage for TFT
23	VOUT3	-	Gate High Voltage Input
24	DLY	I	VGH Delay Adjust Pin

FUNCTION BLOCK DIAGRAM

AAT11771



TYPICAL APPLICATION CIRCUIT

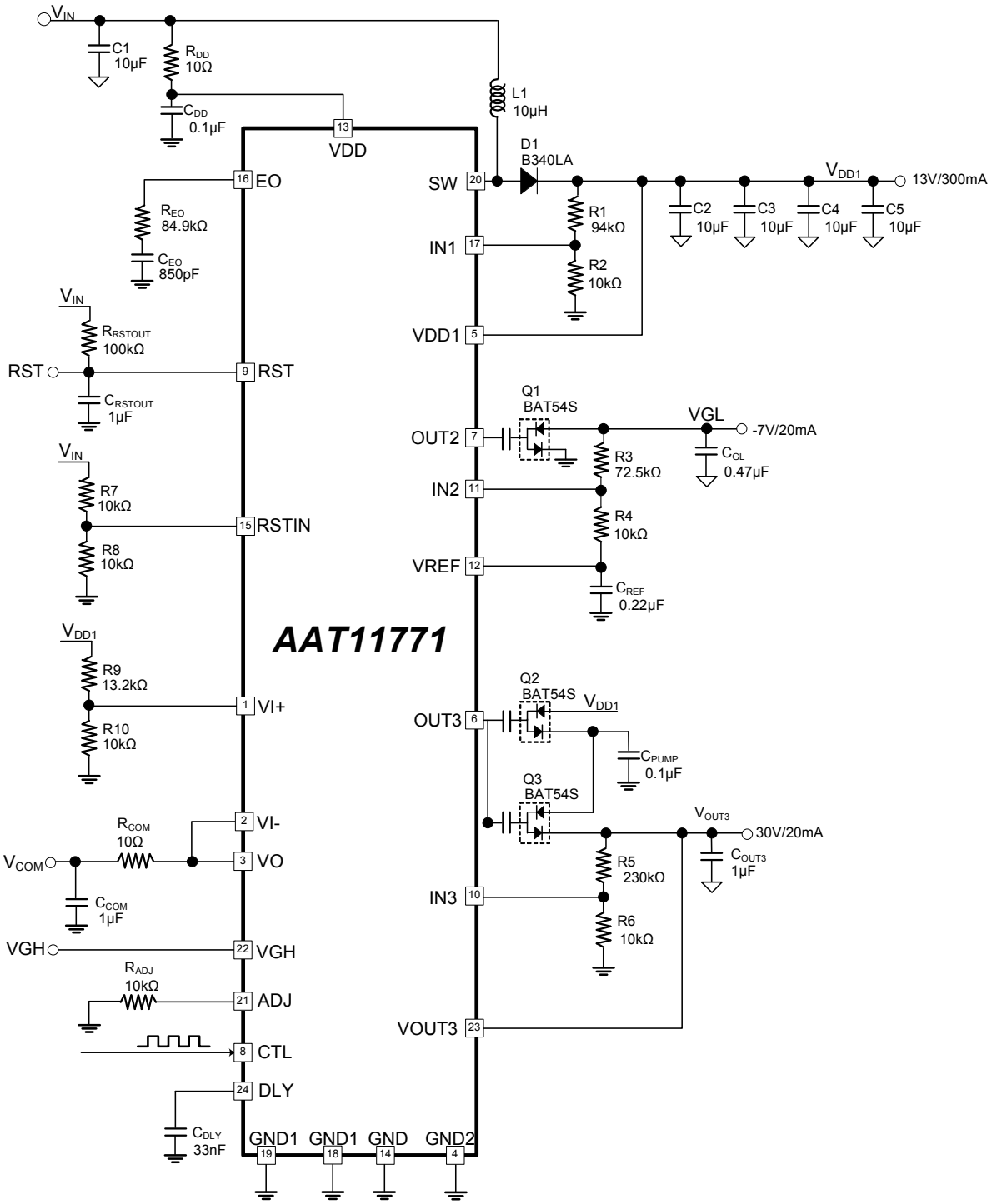


TABLE COMPONENT LIST

DESIGNATION	DESCRIPTION
C1, C2, C3, C4, C5	10µF ±20%, 16V X5R Ceramic capacitors (0805) TAIYO YUDEN (EMK212BJ106MG-T)
D1	3A, 40V Schottky barrier rectifier (SMA) DIODES (B340LA)
L1	10µH, 1.7A DC Inductor TAIYO YUDEN (NR6020)

DESIGN PROCEDURE

Boost Regulator

The Boost regulator includes current mode pulse width modulation control with a fixed frequency and cycle-by-cycle current limit. Capacitance connected to EO pin can compensate internal error amplifier, and will help system-designers to get tailor-made compensation for different applications. An external Schottky rectifier is always required.

Reference Voltage (V_{REF})

The reference output is 1.250V (typ.) and can source at least 100µA. Bypass V_{REF} with a 0.22µF ceramic capacitor connected between V_{REF} and GND.

Under Voltage Lockout (UVLO)

To avoid misoperation at low input voltage, the AAT11771 shuts down all functions when input voltage is lower than UVLO falling threshold (2.15V, typ.). The AAT11771 begins to startup when input voltage exceeds the UVLO rising threshold (2.25V, typ.).

Power on Sequence and Soft Start

The soft start of each regulator is controlled by an internal 7-bit digital controller output to minimize the inrush current. The controller output has 128 steps from zero to feedback voltage threshold for step-up regulator and VGH charge pump; and from reference voltage to feedback voltage threshold for VGL charge pump.

During start-up, a frequency-fixed clock will be inputted to the digital controller to control the soft start time, the PWM soft start time is 10ms (typ.); VGL and VGH soft start time is 3.4ms (typ.).

The startup delay of high voltage switch control block is controlled by a capacitor connected between DLY and GND. When the input voltage exceeds the UVLO rising threshold and the soft start for each regulator and charge pump is implemented and no fault feedback threshold is detected, a 5µA constant current starts to charge the capacitor. The high voltage switch control block is activated after the capacitor voltage exceeds 1.25V (typ.).

The power on sequence of AAT11771 is:

$V_{GL} \rightarrow V_{DD1} \rightarrow V_{GH}$

(Please refer to Figure 1.)

Input Capacitor

The input capacitor has two important functions. It is the power source of the soft start process and can also filter the noise from converter or other circuit. A RC low pass filter is often added to decrease interference from noise.

Output Capacitor

Changes in output capacitor current will induce output voltage ripple. When ripple current is small, ripple voltage will also be small. The actual simplified circuit model of the capacitor is serial connection consisted of ESL, capacitor, and ESR. Many circuits require the usage of aluminum electron capacitor or a tantalum capacitor with low ESR. But due to the drastic increase of the electron capacitor under low temperature,

electron capacitor is not recommended when temperature is lower than –25°C. Tantalum capacitor is often used in a low temp because it has a better ESR performance. However, ceramic capacitors are often used for their environment friendly nature. Capacitor with small ESR or multiple capacitors in parallel connection can improve voltage ripple.

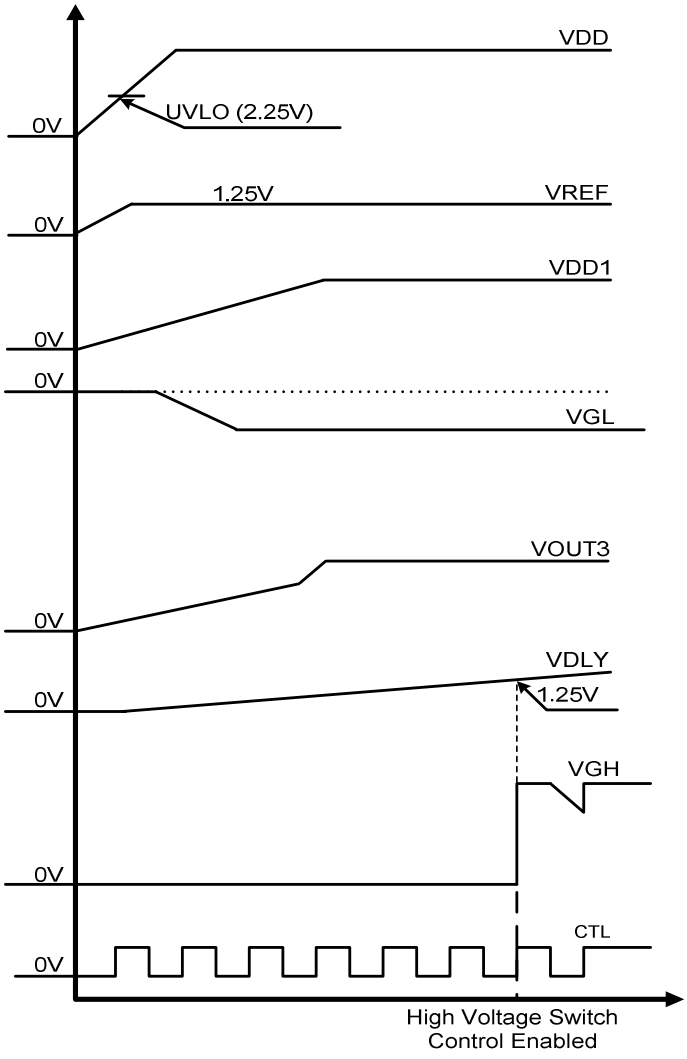


Figure 1. Power on Sequence and Soft Start

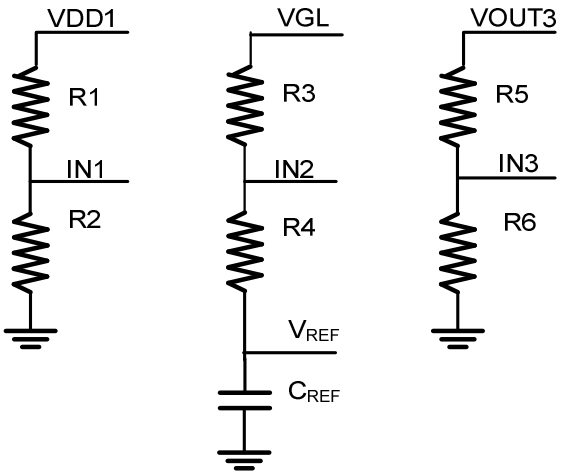


Figure 2. Using Resistive Divider to Set Output Voltage

Output Voltage Selection

The output voltage is set using the feedback pin, IN1, IN2, and IN3. Connect resistive divider from the output to feedback pin to analog ground or reference voltage (V_{REF}) as shown in Figure 2.

$$V_{DD1} = IN1 \times \left(1 + \frac{R1}{R2}\right)$$

IN1 range is 1.250V±12mV

Negative Charge Pump

The negative charge pump is typically used to generate the negative supply rail for the TFT LCD gate driver ICs. The output voltage is set with external resistor ladder from its output to V_{REF} pin with the center tap connected to IN2 pin. The negative charge pump provides a regulated output voltage set by the external resistor divider see in Figure 2.

$$V_{GL} = \{[IN2 \times (R3 + R4)] - (VREF \times R3)\} \div R4$$

IN2 range is 0.250V±15mV

V_{REF} range is 1.250V±12mV

Positive Charge Pump

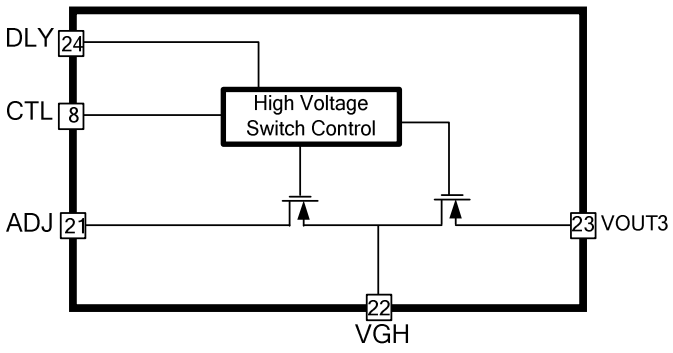
The positive charge pump is typically used to generate the positive supply rail for the TFT LCD gate driver ICs. The output voltage is set with external resistor ladder from its output to GND with the center tap connected to IN3 pin. The positive charge pump provides a regulated output voltage set by the external resistor divider. (See in Figure 2.)

$$V_{OUT3} = IN3 \times \left(1 + \frac{R5}{R6}\right)$$

IN3 range is 1.250V±20mV

CTL and DLY Function

When power on, the high voltage switch controlled by CTL will latch until V_{DLY} reaches 1.25V.
If CTL = "Low", V_{GH} = ADJ
If CTL = "High", $V_{GH} = V_{OUT3}$
DLY pin connects a capacitor, C_{DLY}, to analog ground to set delay time.
Delay time = $(V_{DLY} \times C_{DLY}) / I_{DLY}$



Diode Selection

The diode voltage rating must be greater than output voltage and the current rating must exceed the inductor peak current
$I_{L(PEAK)}$. The lower forward voltage, V_F, will increase to efficiency.

Example:
V_{IN} = 5.0V, V_{OUT} = 13V, I_{OUT} = 300mA, f_{OSC} = 1.2MHz,
V_{FB} = 1.24V, Gm = 85μS, R_S = 0.2V/A, r_{DS} = 0.2Ω,
R_F = 0.333Ω.

Inductor Selection

Where $D = 1 - \frac{V_{IN}}{V_{OUT}}$ D is duty cycle

$$L_{min} > \frac{V_{OUT}}{2I_{OUT} \times f_{OSC}} \times D \times (1-D)^2$$

$$I_{IN} = \frac{I_{OUT}}{1-D}$$

$$I_{L(peak)} = I_{IN} + \frac{V_{IN} \times D}{2 \times L \times f_{OSC}}$$

The inductor current rating must be greater than $I_{L(peak)}$
∴We select L = 10μH, $I_{L(peak)}$ = 0.907A, r_L = 125mΩ.
r_L is the inductor equivalent series resistance.

Output Capacitor Selection

$V_O = 1\% \times V_{OUT} = 1\% \times 13V = 130mV$
V_O is ripple voltage of V_{OUT}, and C is output filter capacitor.

$$\text{Where } C_{min}(\mu F) > \frac{I_{OUT} \times D}{V_O \times f_{OSC}}$$

∴We select C = 10μF, that r_C = 10mΩ.
r_C is the capacitor equivalent series resistance.

Crossover Frequency Selection

$f_{CI} = [\frac{1}{10} \sim \frac{1}{60}] \times f_{OSC}$ ∴We select f_{CI} = 20kHz

$$R_{EO} = \frac{V_{OUT}}{V_{FB}} \times \frac{2\pi \times f_{CI} \times Rs}{gm} \times \frac{[(R_L) + (2 \times r_C)]}{[(1-D) \times R_L - \frac{r}{1-D}]}$$

$r = r_L + (D x r_{DS}) + (1–D) x R_F$

∴We select R_{EO} = 84.91kΩ

R_L is the converter load resistance

Compensator Capacitor Selection

The output filter capacitor is then chosen

So C R_L pole cancels R_{EO} C_{EO} zero

$$R_{EO} \times C_{EO} = \frac{C}{\varepsilon} \times \left[\frac{R_L}{2} + r_C\right], \text{ and}$$

$$C_{EO} = \frac{C}{\varepsilon \times R_{EO}} \times \left[\frac{R_L}{2} + r_C\right]$$

ε = (1~3)

∴We select C_{EO} = 850pF

Reset Output (RST)

The AAT11771 has an internal reset circuit to monitor the RSTIN voltage. When RSTIN voltage is lower than the threshold voltage 1.25V (typ.), RST voltage will be pulled low to GND. RST is an open-drain output that needs a pull-up resistor connected between V_{IN} and RST.

Operational Amplifier

The AAT11771 has one operational amplifier to drive the LCD backplane (V_{COM}) or the gamma-correction divider string. The operational amplifier features rail-to-rail input and output, ±200mA output short-circuit current, and 40V/μs slew rate.

Fault Protection

The AAT11771 activates an internal fault timer when any of the regulator or charge pump output voltage is detected under the fault feedback threshold. After counting 55ms (typ.), the AAT11771 will shutdown all the output except reference voltage.

LAYOUT CONSIDERATION

The system's performances including switching noise, transient response, and PWM feedback loop stability are greatly affected by the PC board layout and grounding. There are some general guidelines for layout:

Inductor

Always try to use a low EMI inductor with a ferrite core.

Filter Capacitors

Place low ESR ceramics filter capacitors (between 0.1µF and 0.22µF) close to VDD and VREF pins. This will eliminate as much trace inductance effects as possible and give the internal IC rail a cleaner voltage supply. The ground connection of the VDD and VREF bypass capacitor should be connected to the analog ground pin (GND) with a wide trace.

Output Capacitors

Place output capacitors as close as possible to the IC. Minimize the length and maximize the width of traces to get the best transient response and reduce the ripple noise. We choose 10µF ceramics capacitor to reduce the ripple voltage, and use 0.1µF ceramics capacitor to reduce the ripple noise.

Feedback

If external compensation components are needed for stability, they should also be placed close to the IC. Take care to avoid the feedback voltage-divider resistors trace near the SW. Minimize feedback track lengths to avoid the digital signal noise of TFT control board.

Ground Plane

The grounds of the IC, input capacitors, and output capacitors should be connected close to a ground plane. It would be a good design rule to have a ground plane on the PCB. This will reduce noise and ground loop errors as well as absorb more of the EMI radiated by the inductor. For boards with more than two layers, a ground plane can be used to separate the power plane and the signal plane for improved performance.

PC Board Layout

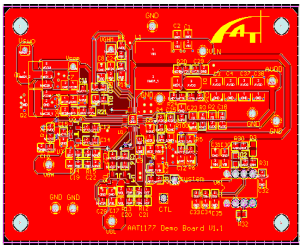


Figure 3. TOP Layer

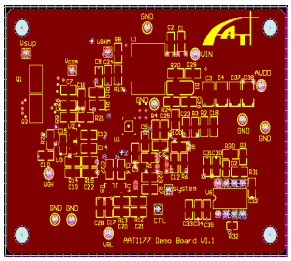


Figure 4. Midlayer1 (Ground Plane)

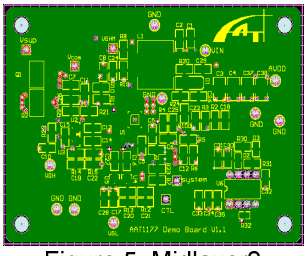


Figure 5. Midlayer2 (Power Plane)

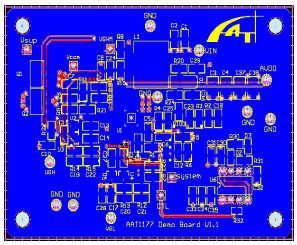
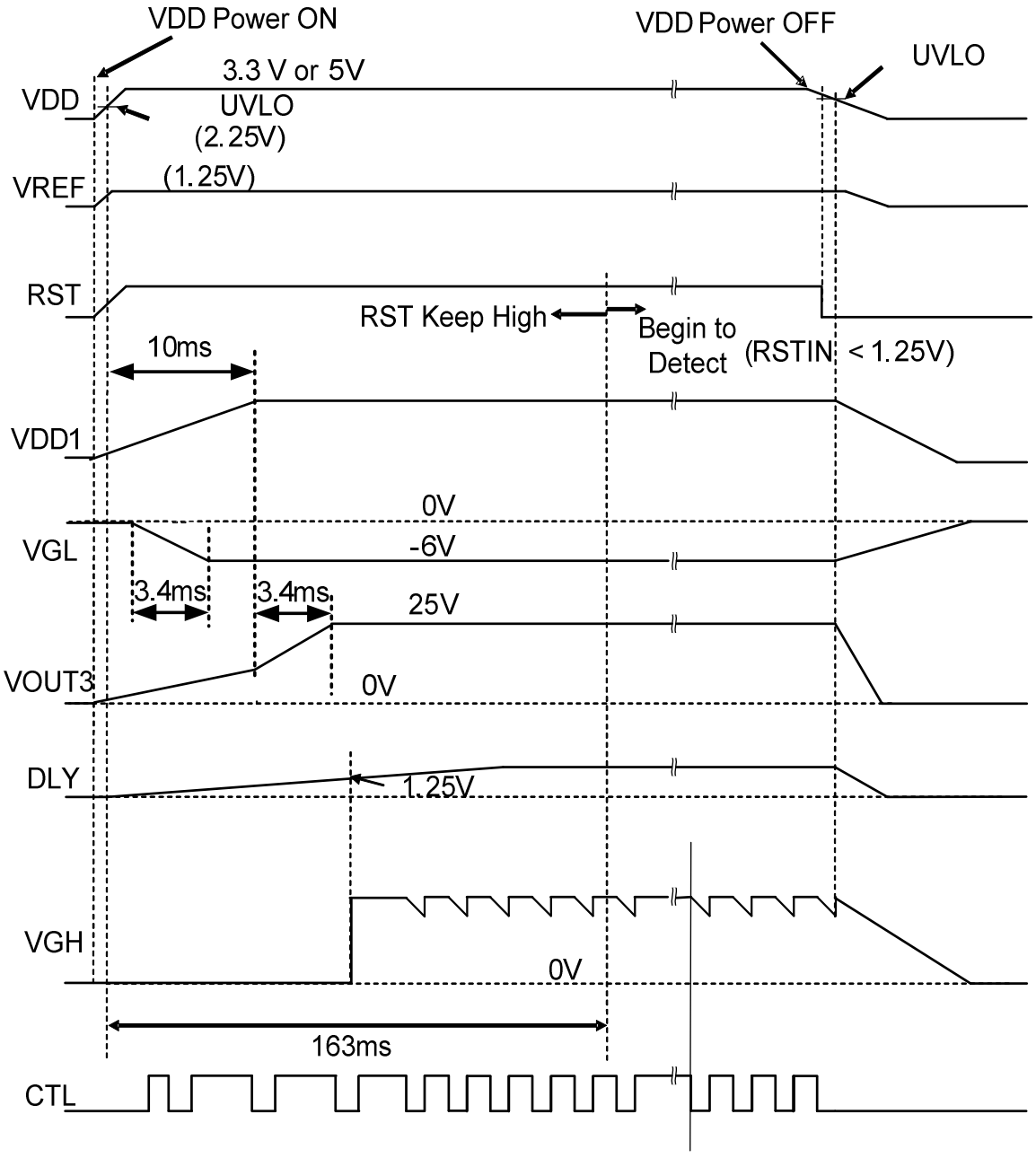


Figure 6. Bottom Layer

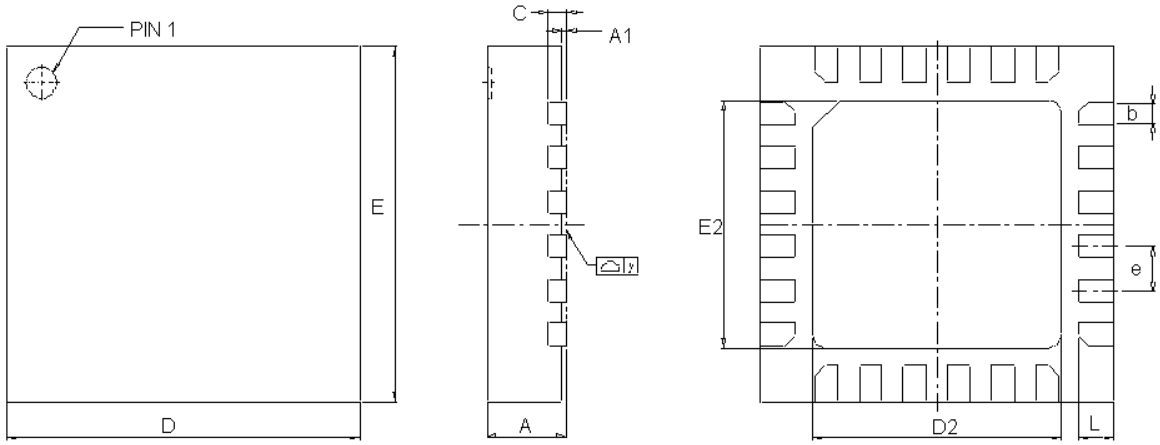
POWER ON AND POWER OFF TIMING CHART

AAT11771



PACKAGE DIMENSION

VQFN24-4*4



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.18	0.23	0.30
C	0.19	0.20	0.25
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
E	3.90	4.00	4.10
E2	2.70	2.80	2.90
e	------	0.50	------
L	0.30	0.40	0.50
y	0.00	-----	0.076