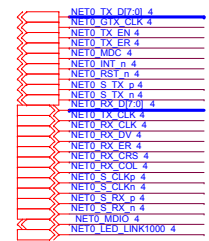


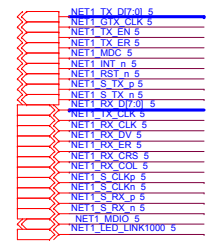
NET-FMC

SCHEMATIC	CONTENT	PAGE
01 TOP	Cover Page	01
02 FMC	FMC Connector	02
03 Power	POWER	03
04 Ethernet 0	10/100/1000 Ethernet PHY 0	04
05 Ethernet 1	10/100/1000 Ethernet PHY 1	05
06 Ethernet 2	10/100/1000 Ethernet PHY 2	06
07 Ethernet 3	10/100/1000 Ethernet PHY 3	07

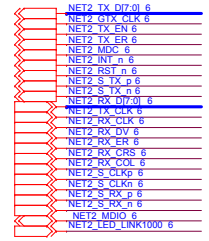
Ethernet 0



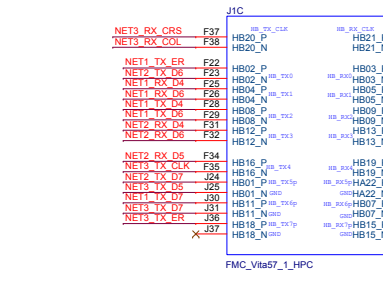
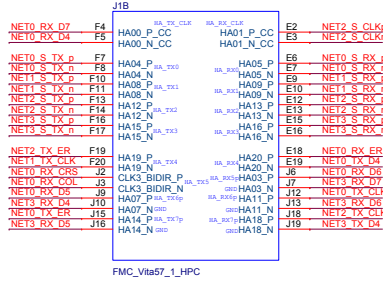
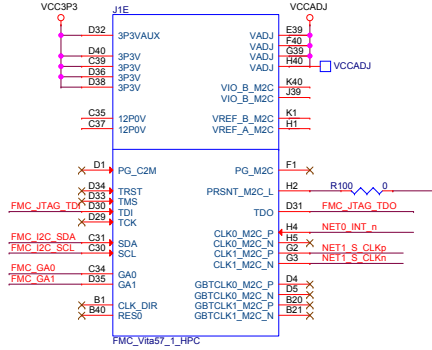
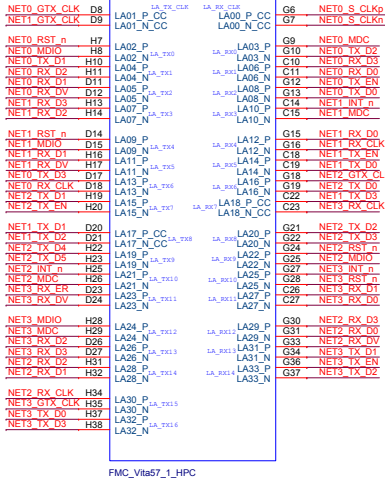
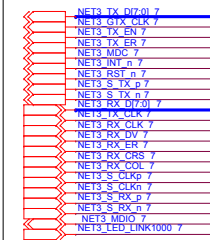
Ethernet 1



Ethernet 2

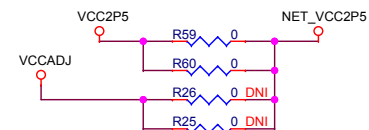
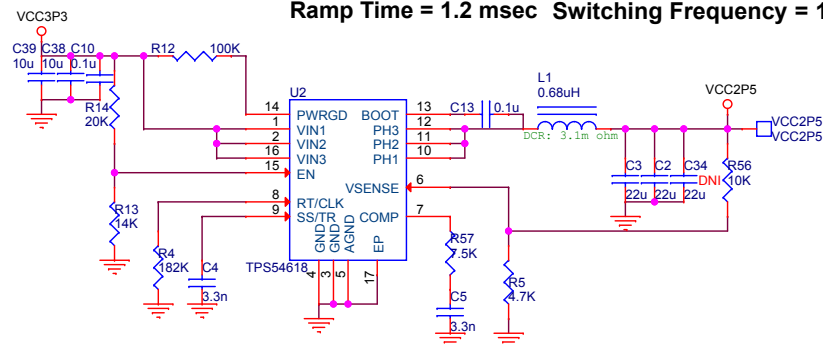
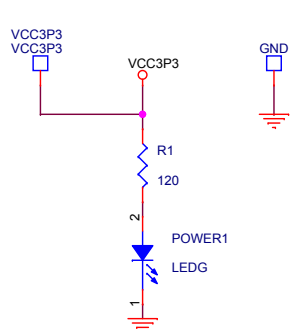


Ethernet 3



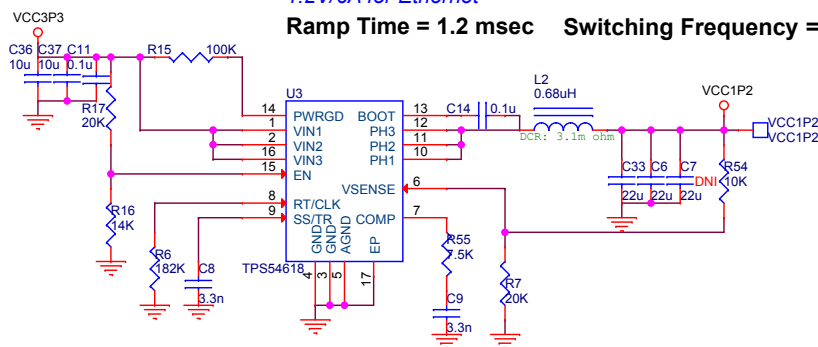
2.5V/6A for Ethernet

Ramp Time = 1.2 msec Switching Frequency = 1MHz

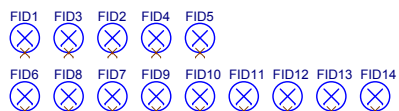


1.2V/6A for Ethernet

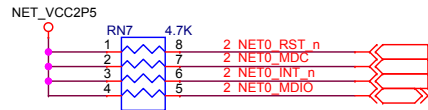
Ramp Time = 1.2 msec Switching Frequency = 1MHz



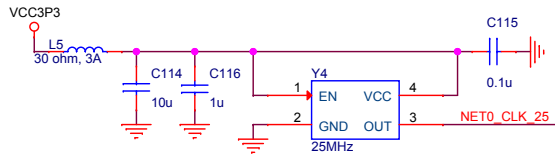
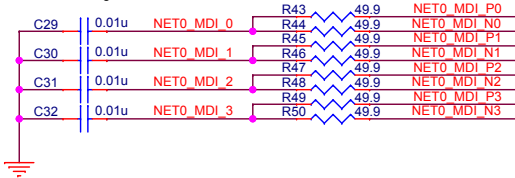
PCB1
10-21605250-B0



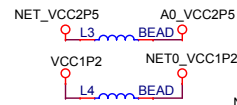
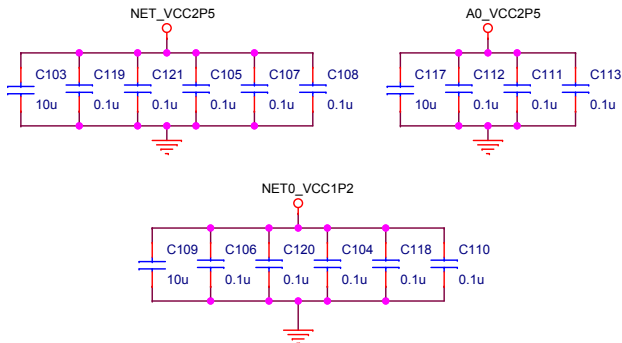
10/100/1000 Ethernet 0



Design Note:
MDI signals termination

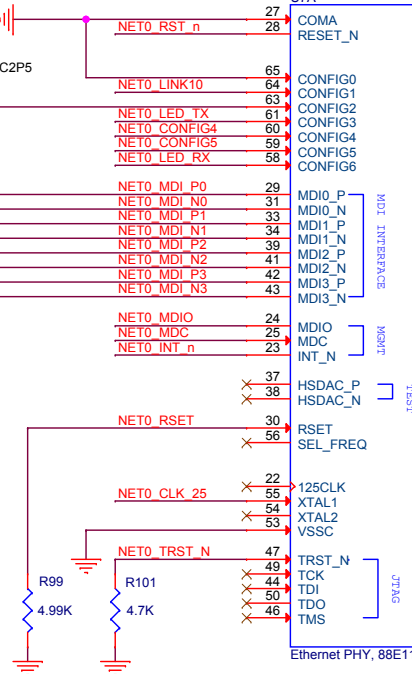
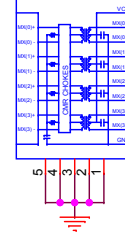


Frequency Stability: ± 8 ppm

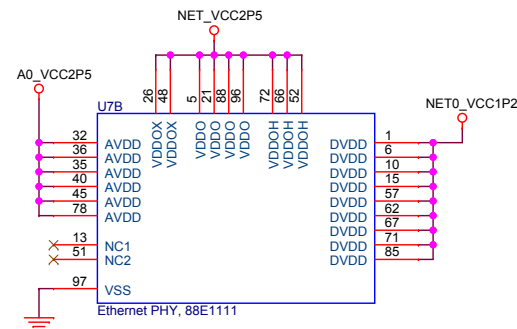


PHYADR[4:0]=10000b

Ethernet PHY A

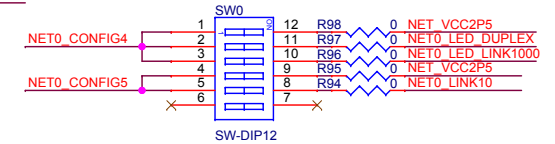
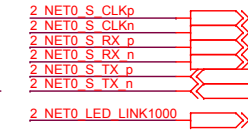
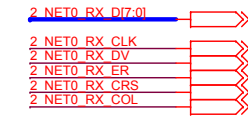
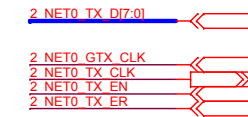


Ethernet PHY, 88E1111

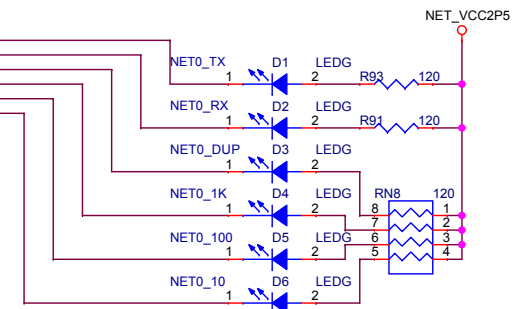


Ethernet PHY, 88E1111

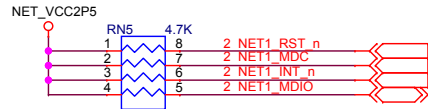
FPGA Interface



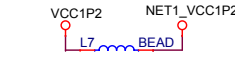
CONFIG4	CONFIG5	MODE
1---12	4---9	GMII/MII
2---11	4---9	RGMII
3---10	5---8	SGMII



10/100/1000 Ethernet 1



NET_VCC2P5 A1_VCC2P5



PHYADR[4:0]=10001b

Ethernet PHY B

FPGA Interface

2 NET1_TX_D[7:0]

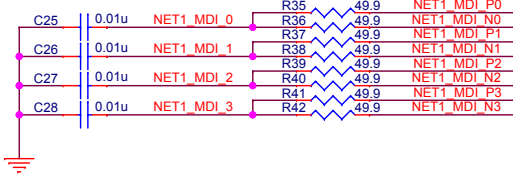
2 NET1 GTX_CLK
2 NET1 TX_CLK
2 NET1 TX_EN
2 NET1 TX_ER

2 NET1 RX_D[7:0]

2 NET1 RX_CLK
2 NET1 RX_DV
2 NET1 RX_ER
2 NET1 RX CRS
2 NET1 RX COL

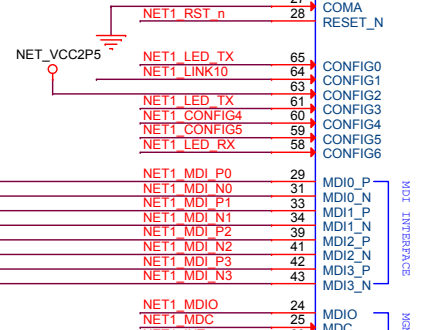
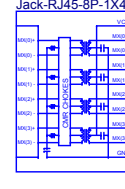
2 NET1 S_CLKp
2 NET1 S_CLKn
2 NET1 S_RX_p
2 NET1 S_RX_n
2 NET1 S_TX_p
2 NET1 S_TX_n
2 NET1 LED LINK1000

Design Note:
MDI signals termination

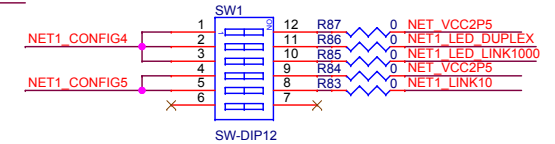
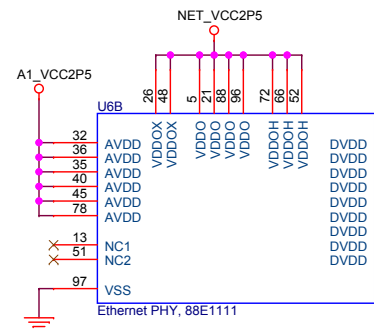


RJ45-B

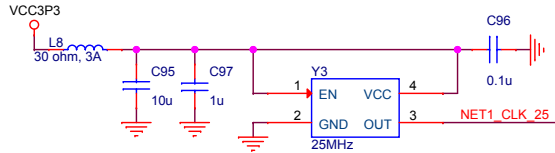
J2B Jack-RJ45-8P-1X4



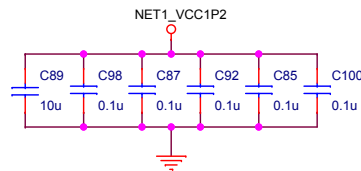
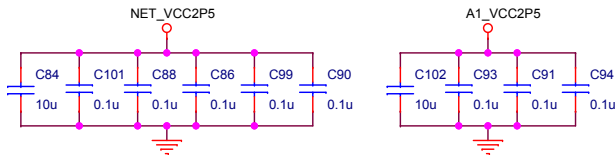
Ethernet PHY, 88E1111



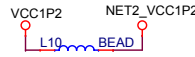
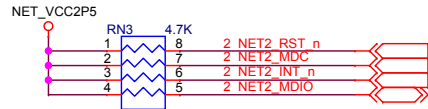
CONFIG4	CONFIG5	MODE
1--12	4--9	GMII/MII
2--11	4--9	RGMII
3--10	5--8	SGMII



Frequency Stability: +- 8 ppm



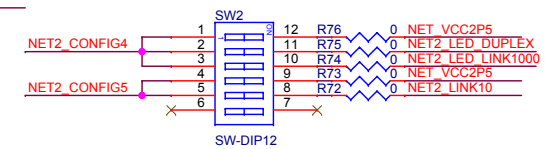
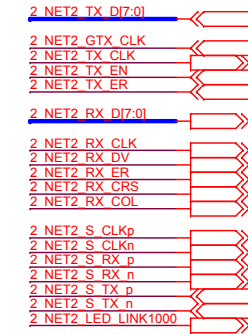
10/100/1000 Ethernet 2



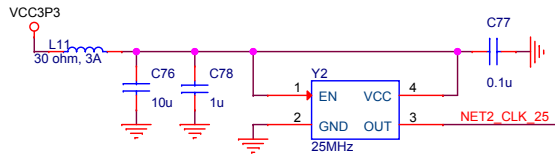
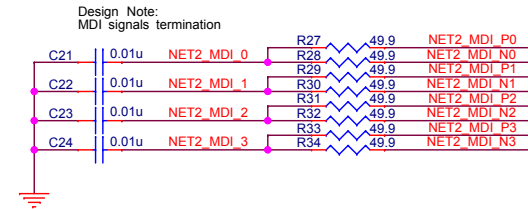
PHYADR[4:0]=10010b

Ethernet PHY C

FPGA Interface

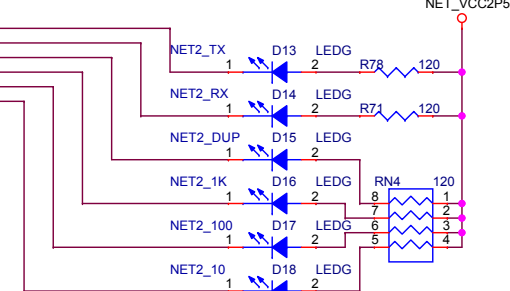
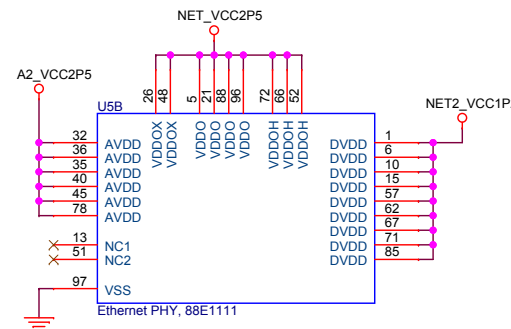
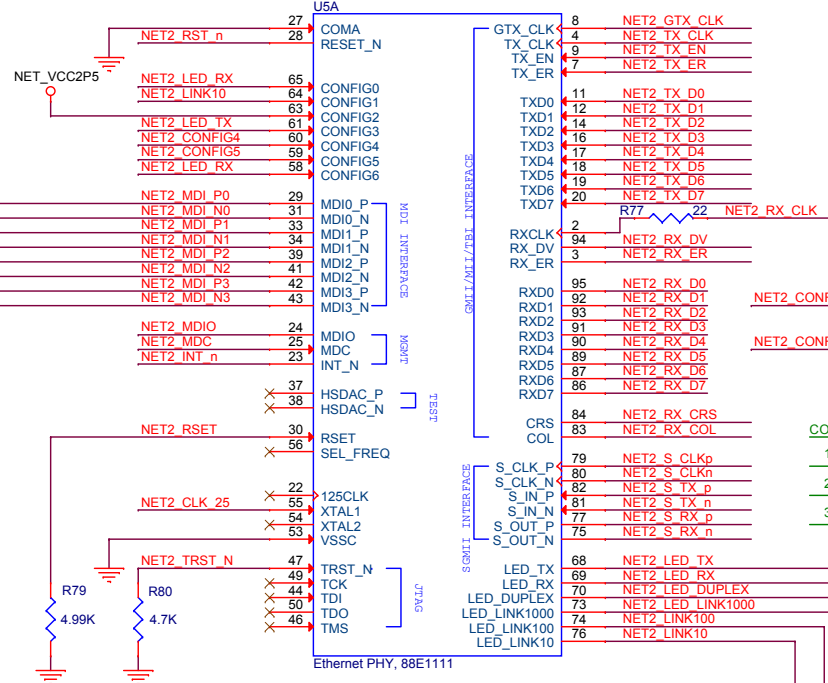
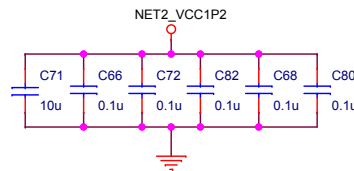
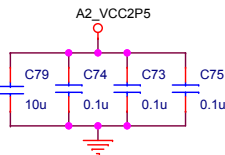
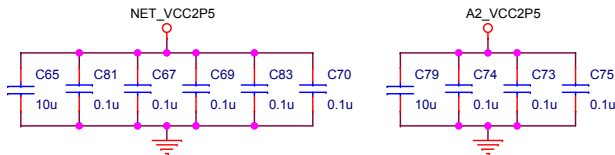
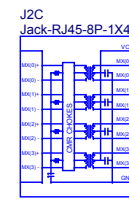


CONFIG4	CONFIG5	MODE
1--12	4--9	GMII/MII
2--11	4--9	RGMII
3--10	5--8	SGMII

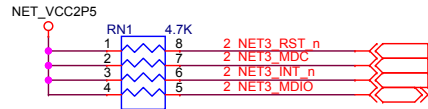


Frequency Stability: +- 8 ppm

RJ45-C



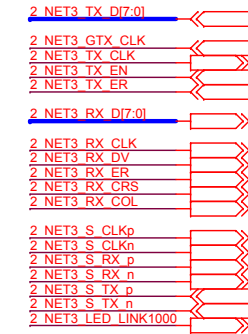
10/100/1000 Ethernet 3



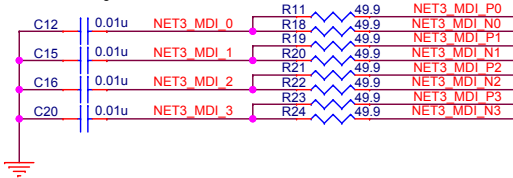
PHYADR[4:0]=10011b

Ethernet PHY D

FPGA Interface

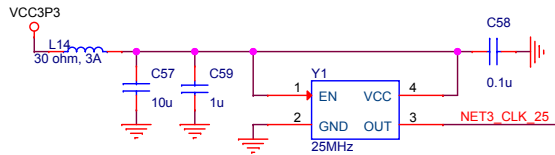
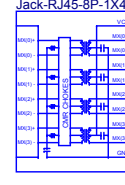


Design Note:
MDI signals termination

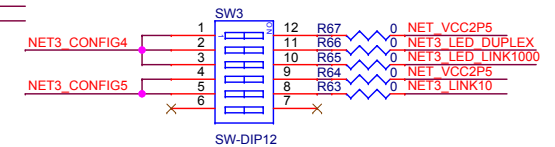
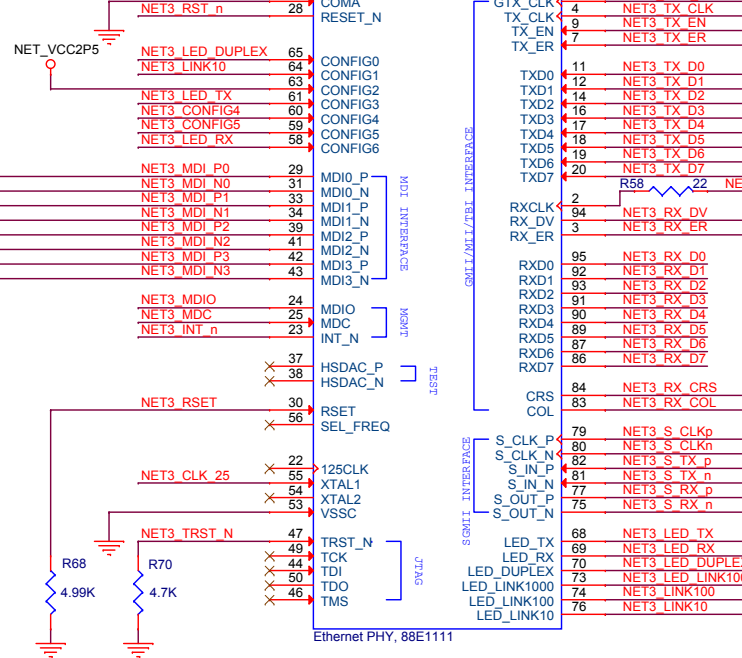
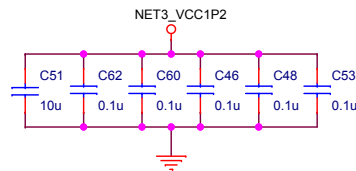
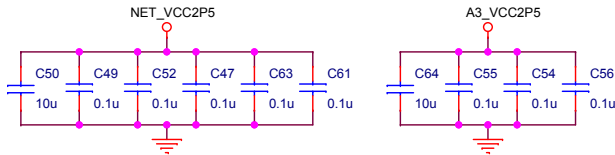


RJ45-D

J2D Jack-RJ45-8P-1X4



Frequency Stability: +- 8 ppm



CONFIG4	CONFIG5	MODE
1--12	4--9	GMII/MII
2--11	4--9	RGII
3--10	5--8	SGMII

