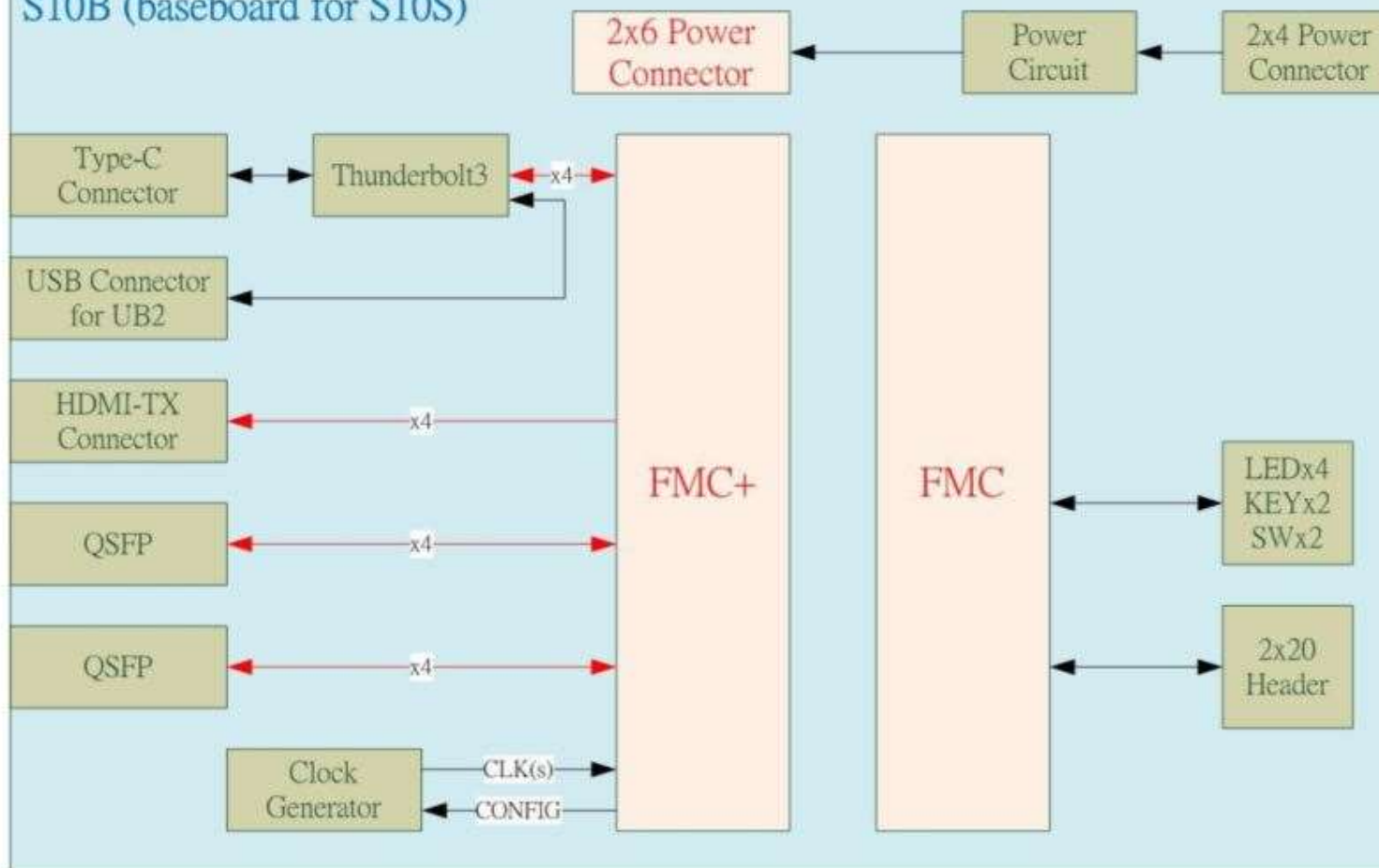
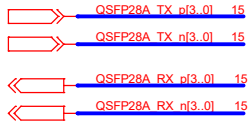


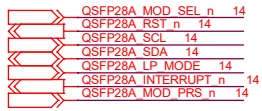
S10B (baseboard for S10S)



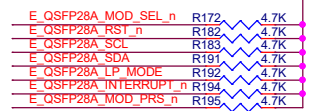
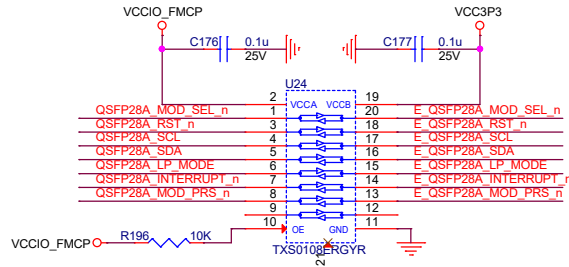
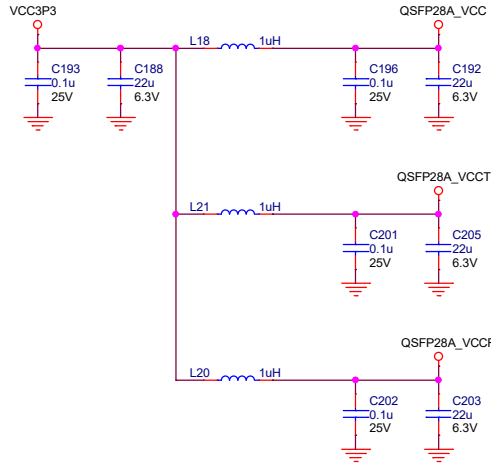
QSFP28 Port A Transceivers



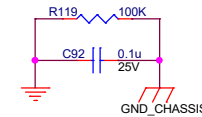
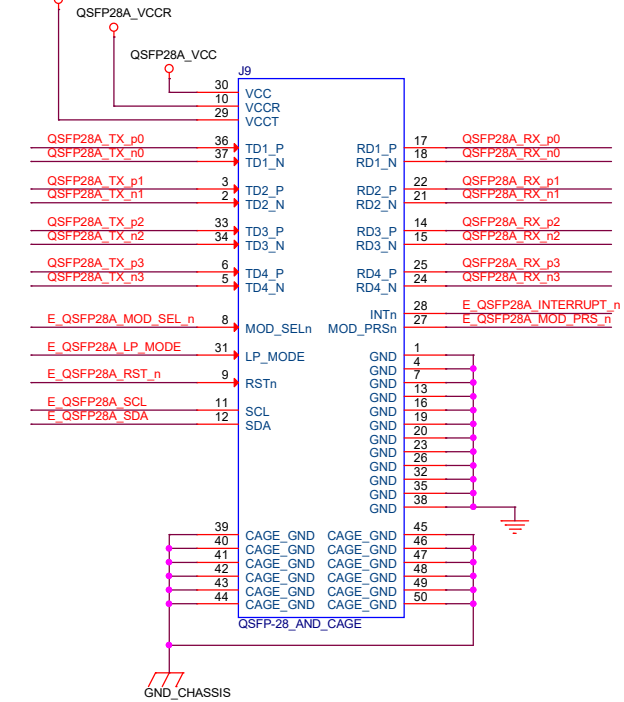
QSFP28A Control Interface



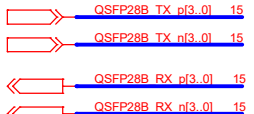
NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.
 NOTE 2: Assuming that the SFP RD 100-ohm termination on the Host Board FPGA device will be implemented via the on-chip termination circuit.
 NOTE 3: DC blocking capacitors are in the module for RX and TX.
 NOTE 4: 1uH inductors should have a DC Resistance of less than 0.1-ohm.



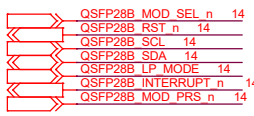
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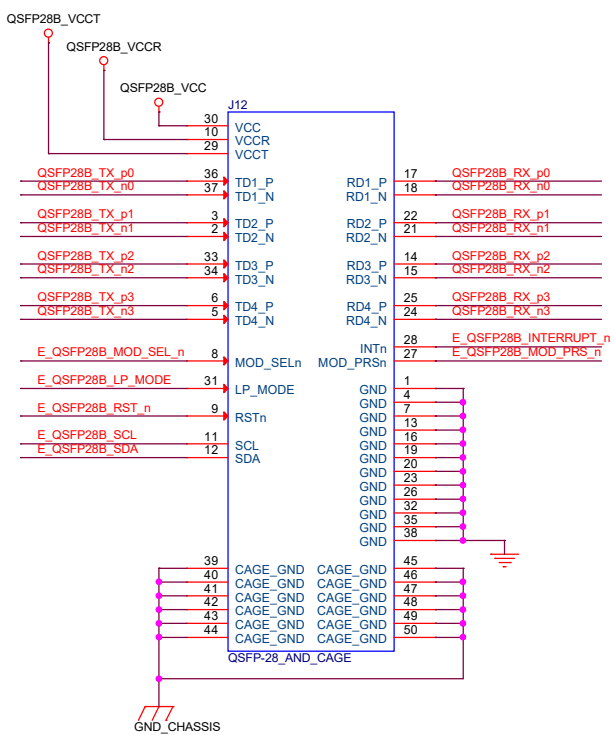
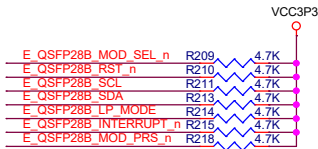
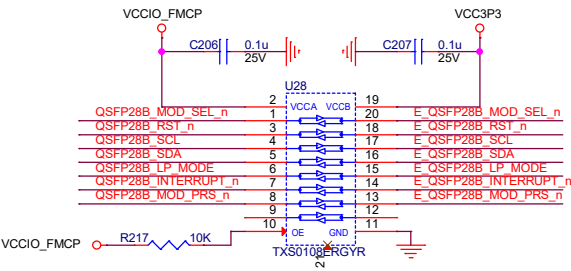
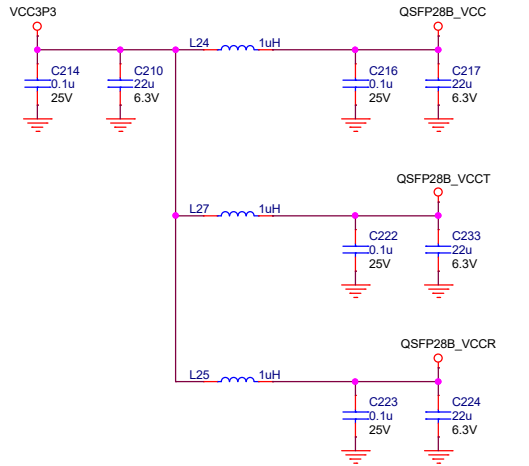
QSFP28 Port B Transceivers



QSFP28B Control Interface



NOTE 1: Bypass Capacitors should be placed as close to the associated 20-pin connector as possible.
NOTE 2: Assuming that the SFP RD 100-ohm termination on the Host Board FPGA device will be implemented via the on-chip termination circuit.
NOTE 3: DC blocking capacitors are in the module for RX and TX.
NOTE 4: 1uH inductors should have a DC Resistance of less than 0.1-ohm.



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Title

Apollo Carrier

Size

B

Document Number

QSFP28 Connector Port B

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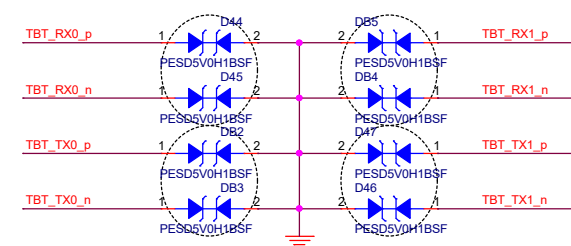
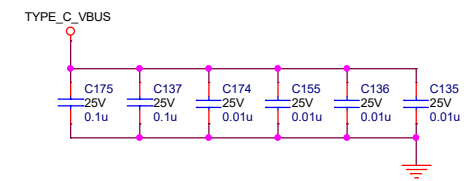
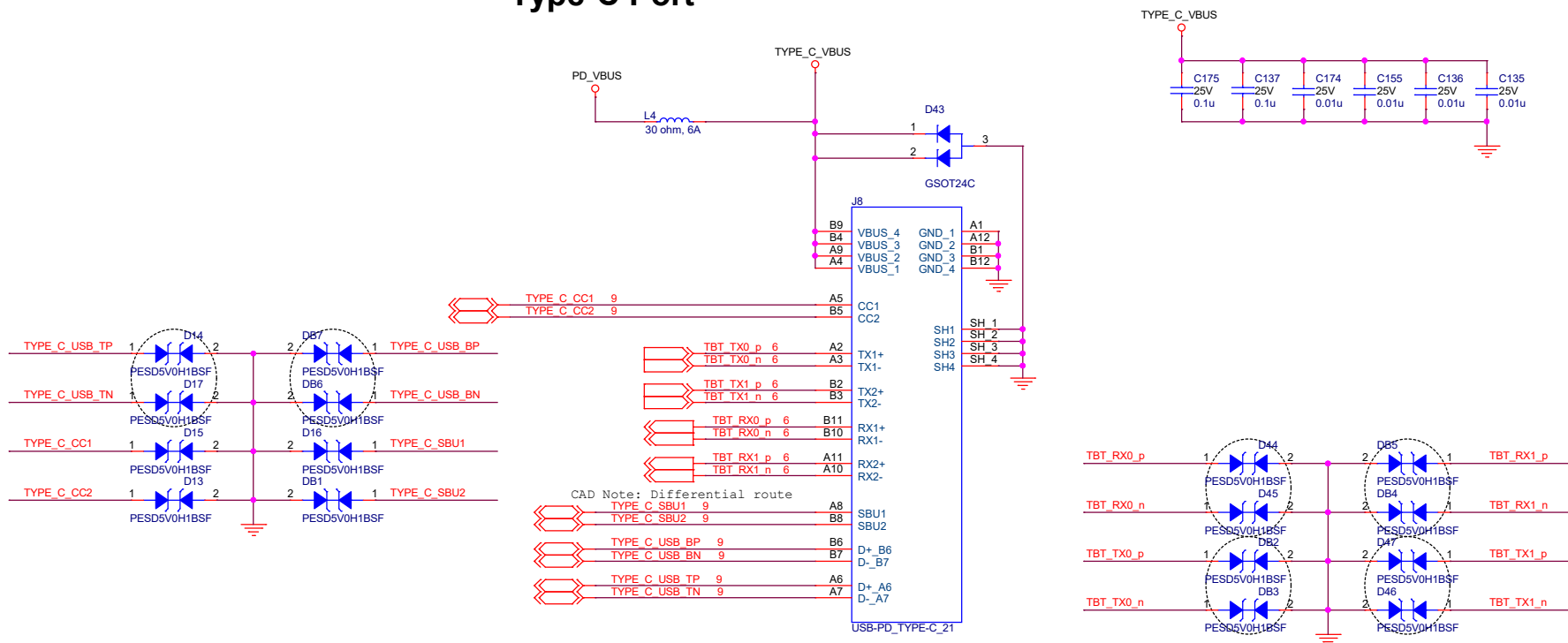
of

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Rev

B0

Type-C Port



CAD Note: Differential route

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Title Apollo Carrier	
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Alpine Ridge 4C - TBT, USB2

The schematic diagram illustrates the electrical connections for the Alpine Ridge 4C module, specifically for TBT (Thunderbolt) and USB2 interfaces. The central component is the **Alpine_Ridge_Device** (U18E), which is connected to a **USB A-Type** connector (J6) and various external components.

USB A-Type Connector (J6):

- VBUS:** Connected to **U_VCC5** through a resistor **R64** (0Ω).
- D-** and **D+** pins are connected to **USB UBII_DM** and **USB UBII_DP** signals.
- GND:** Connected to ground through a resistor **R62** (0Ω).

Alpine_Ridge_Device (U18E):

- TBT Ports:**
 - TBT RX0:** PA_RX0_P (B21) and PA_RX0_N (A21).
 - TBT TX0:** PA_TX0_P (B19) and PA_TX0_N (A19).
 - TBT RX1:** PA_RX1_P (A15) and PA_RX1_N (B15).
 - TBT TX1:** PA_TX1_P (A17) and PA_TX1_N (B17).
 - TBT DPSRC AUX:** PA_DPSRC_AUX_P (Y15) and PA_DPSRC_AUX_N (W15).
 - TBT USB DP:** PA_USB2_D_P (E20) and PA_USB2_D_N (D20).
 - TBT USB DM:** PA_USB2_D_P (E20) and PA_USB2_D_N (D20).
 - TBT ACE LSTX:** PA_LSTX (A5).
 - TBT ACE LSRX:** PA_LSRX (A4).
 - DG PA DPSRC HPD:** PA_DPSRC_HPD (M4).
- DP (DisplayPort) Ports:**
 - DPSNK0:** PA_RX0_P (B21), PA_TX0_P (B19), PA_RX1_P (A15), PA_TX1_P (A17), PA_DPSRC_AUX_P (Y15), PA_USB2_D_P (E20), PA_LSTX (A5), PA_LSRX (A4), PA_DPSRC_HPD (M4).
 - DPSNK1:** PB_RX0_P (B13), PB_TX0_P (B11), PB_RX1_P (A7), PB_TX1_P (A9), PB_DPSRC_AUX_P (Y16), PB_USB2_D_P (E19), PB_LSTX (B4), PB_LSRX (B5), PB_DPSRC_HPD (F19).
 - DPSRC:** PA_RX0_P (B21), PA_TX0_P (B19), PA_RX1_P (A15), PA_TX1_P (A17), PA_DPSRC_AUX_P (Y15), PA_USB2_D_P (E20), PA_LSTX (A5), PA_LSRX (A4), PA_DPSRC_HPD (M4).

External Components:

- Resistors:** R64 (0Ω), R62 (0Ω), R158 (0Ω), R157 (0Ω), R159 (0Ω), R160 (0Ω), R85 (1M), R87 (1M), R185 (100K), R162 (499), R88 (1M), R86 (1M), R106 (100K), R163 (499), R105 (100K), R178 (15K).
- Capacitors:** C74 (0.22u), C75 (0.22u), C154 (0.22u), C153 (0.22u), C142 (0.1u), C141 (0.1u), C49 (10u), C46 (10u), C48 (0.1u), C52 (0.1u).
- Inductors:** L2, BEAD.
- Diodes:** D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19, D20, D21, D22, D23, D24, D25, D26, D27, D28, D29, D30, D31, D32, D33, D34, D35, D36, D37, D38, D39, D40, D41, D42, D43, D44, D45, D46, D47, D48, D49, D50, D51, D52, D53, D54, D55, D56, D57, D58, D59, D60, D61, D62, D63, D64, D65, D66, D67, D68, D69, D70, D71, D72, D73, D74, D75, D76, D77, D78, D79, D80, D81, D82, D83, D84, D85, D86, D87, D88, D89, D90, D91, D92, D93, D94, D95, D96, D97, D98, D99, D100.

Legend:

- Port A:** TBT RX0, TBT TX0, TBT RX1, TBT TX1, TBT DPSRC AUX, TBT USB DP, TBT USB DM, TBT ACE LSTX, TBT ACE LSRX, DG PA DPSRC HPD.
- Port B:** TBT RX0, TBT TX0, TBT RX1, TBT TX1, TBT DPSRC AUX, TBT USB DP, TBT USB DM, TBT ACE LSTX, TBT ACE LSRX, DG PA DPSRC HPD.
- Source Port:** DPSNK0, DPSNK1, DPSRC.
- Sink Port 0:** DPSNK0, DPSNK1, DPSRC.
- Sink Port 1:** DPSNK0, DPSNK1, DPSRC.

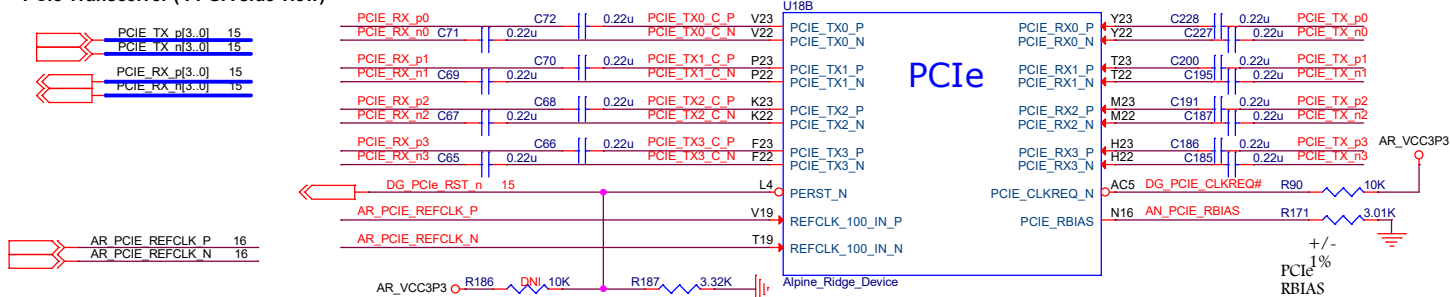
Notes:

- U_VCC5 is connected to VCC5 through a resistor **R64** (0Ω).
- U_VCC5 is connected to GND through a resistor **R62** (0Ω).
- U_VCC5 is connected to GND through a resistor **R158** (0Ω).
- U_VCC5 is connected to GND through a resistor **R157** (0Ω).
- U_VCC5 is connected to GND through a resistor **R159** (0Ω).
- U_VCC5 is connected to GND through a resistor **R160** (0Ω).
- U_VCC5 is connected to GND through a resistor **R85** (1M).
- U_VCC5 is connected to GND through a resistor **R87** (1M).
- U_VCC5 is connected to GND through a resistor **R185** (100K).
- U_VCC5 is connected to GND through a resistor **R162** (499).
- U_VCC5 is connected to GND through a resistor **R88** (1M).
- U_VCC5 is connected to GND through a resistor **R86** (1M).
- U_VCC5 is connected to GND through a resistor **R106** (100K).
- U_VCC5 is connected to GND through a resistor **R163** (499).
- U_VCC5 is connected to GND through a resistor **R105** (100K).
- U_VCC5 is connected to GND through a resistor **R178** (15K).

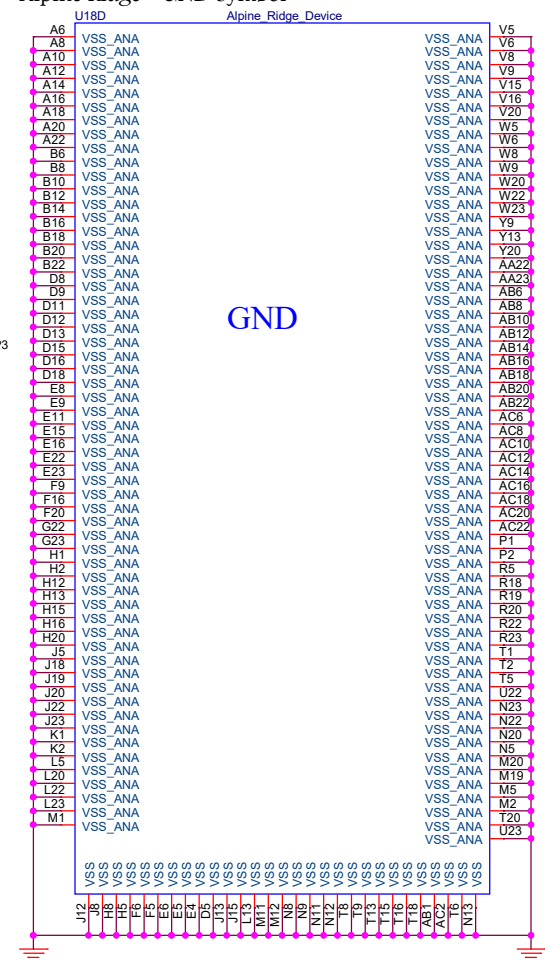
TPD2E001DRLR (U15) is connected to **U_VCC5** through a resistor **R64** (0Ω).

Alpine Ridge 4C - PCIe & GND

PCIe Transceiver (FPGA side view)



Alpine Ridge - GND Symbol

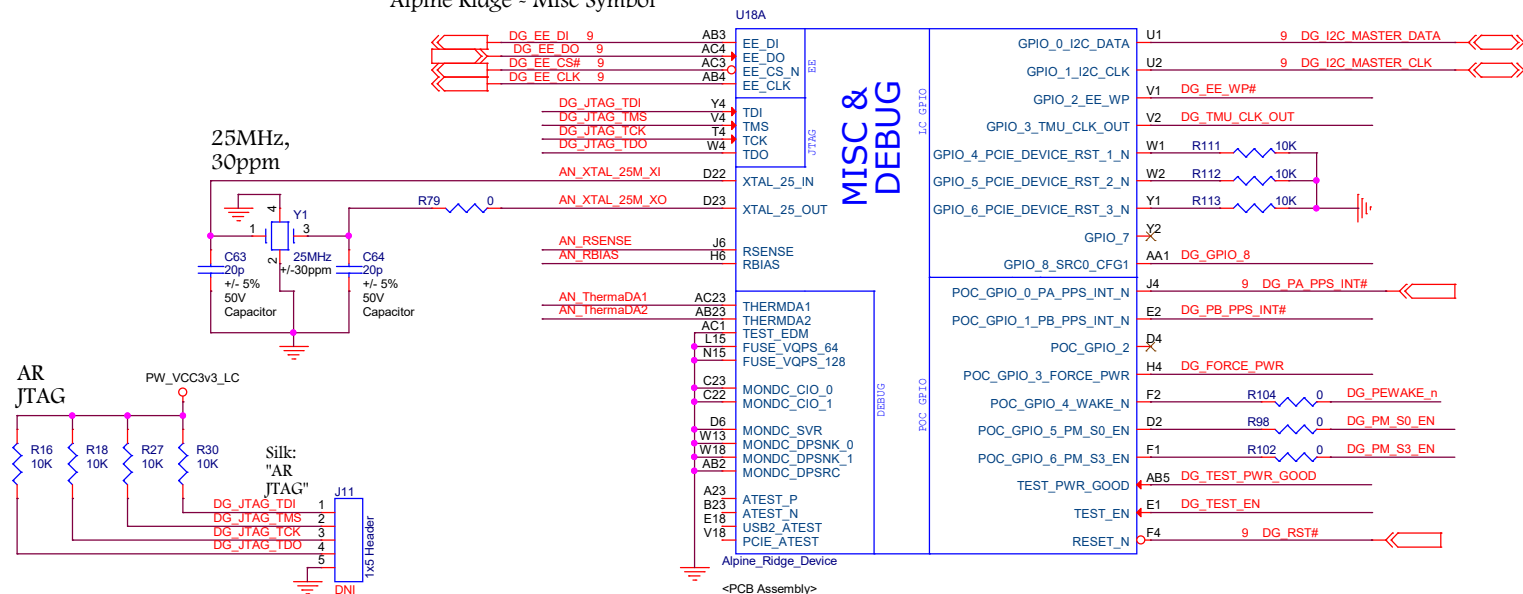


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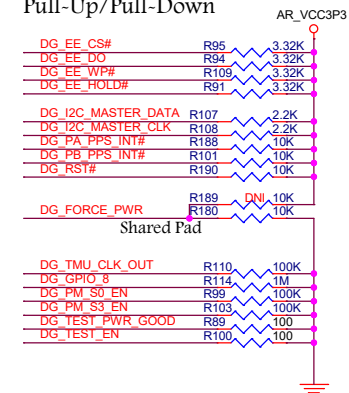
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Apollo Carrier		
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AR - MISC

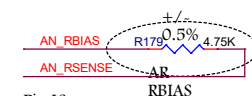
Alpine Ridge - Misc Symbol



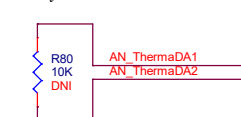
HW Pull-Up/Pull-Down



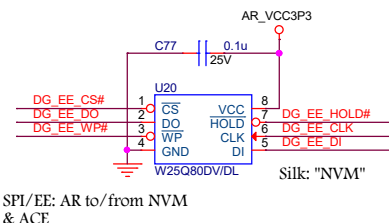
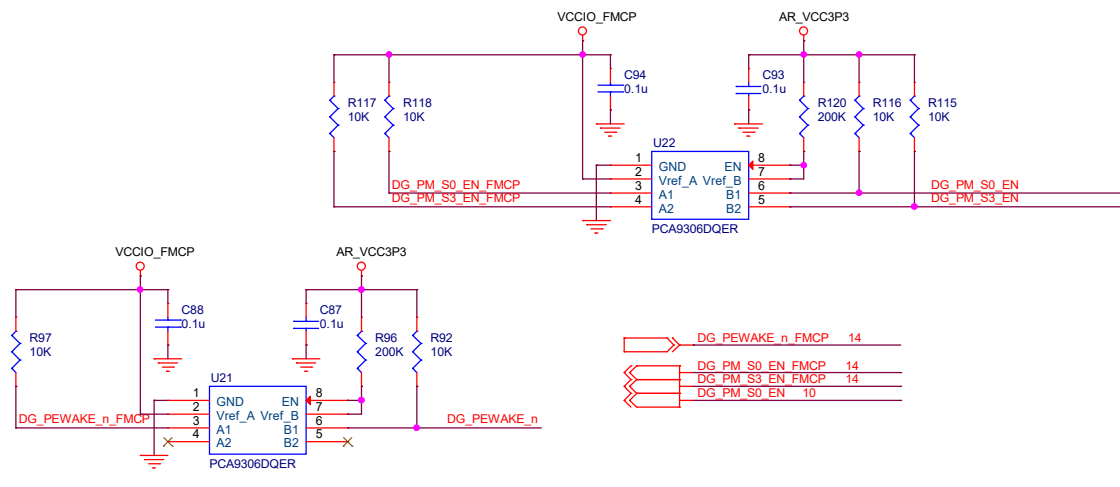
Pin H6



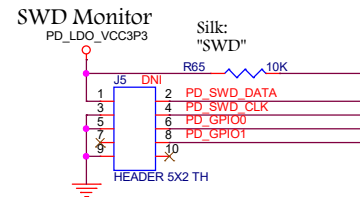
Pin J6



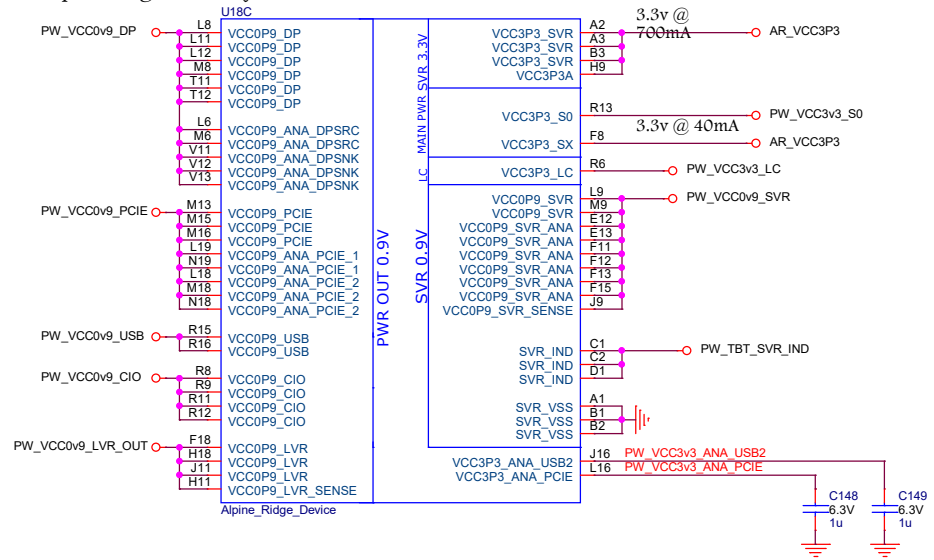
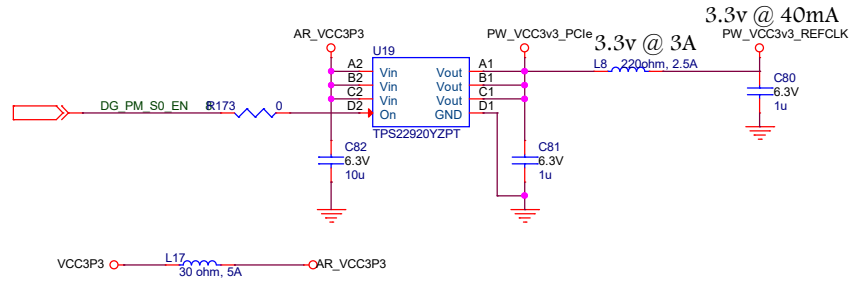
8Mbit Flash (Mutual for AR and ACE)



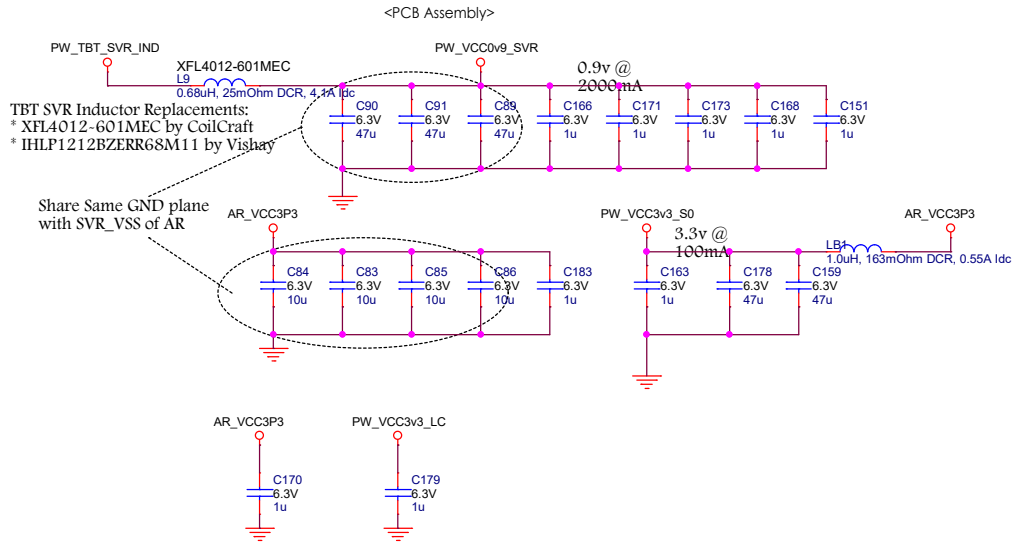
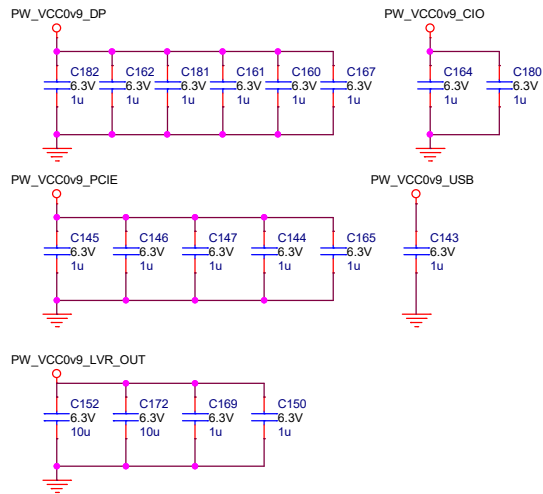
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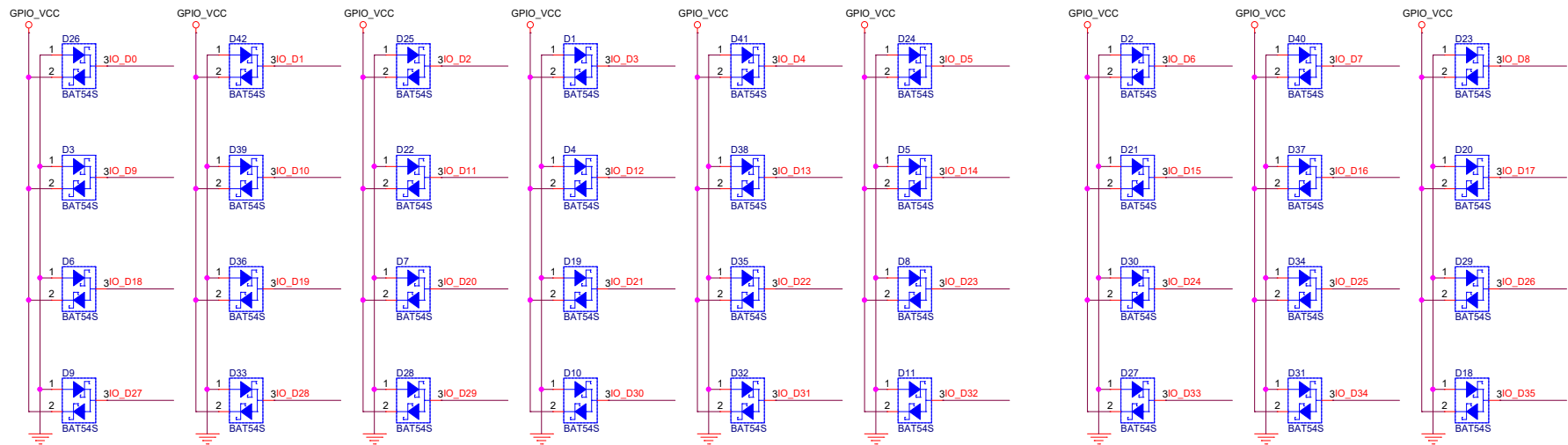


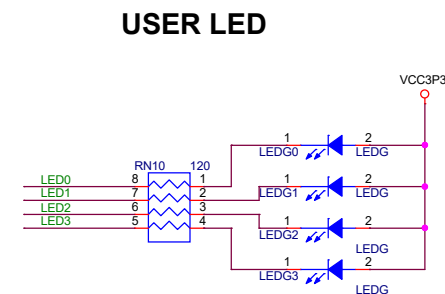
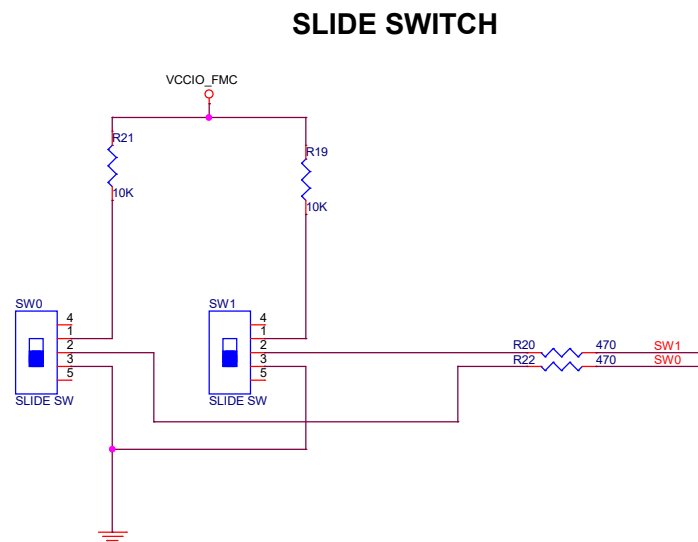
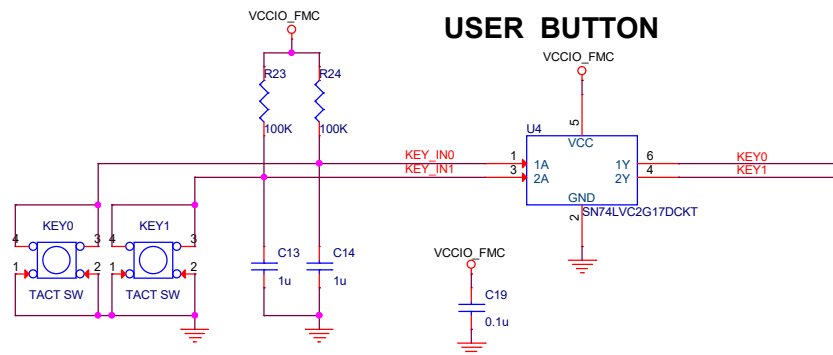
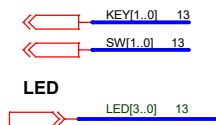
Alpine Ridge - VCC Symbol



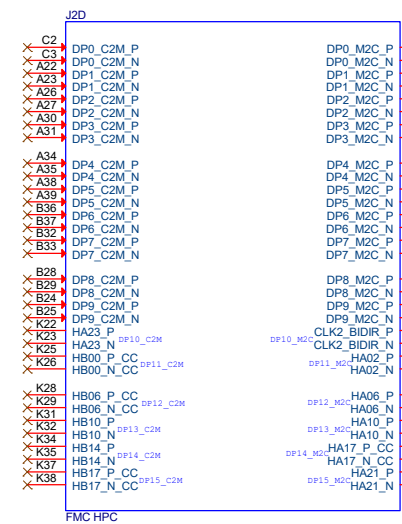
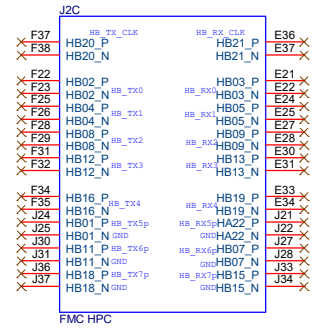
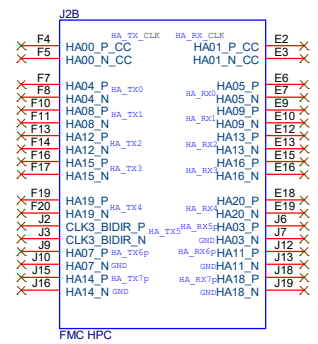
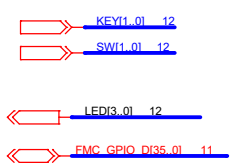
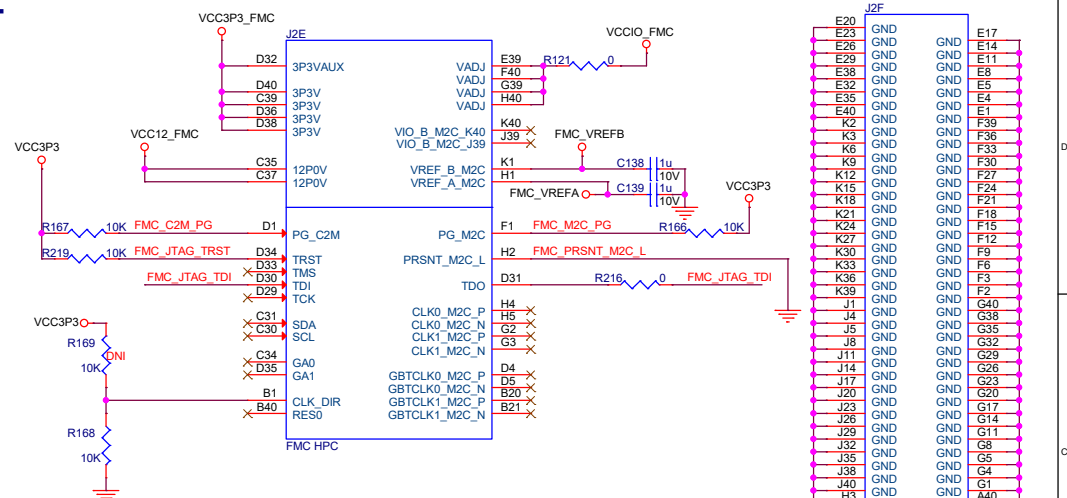
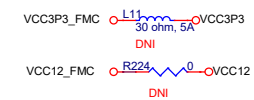
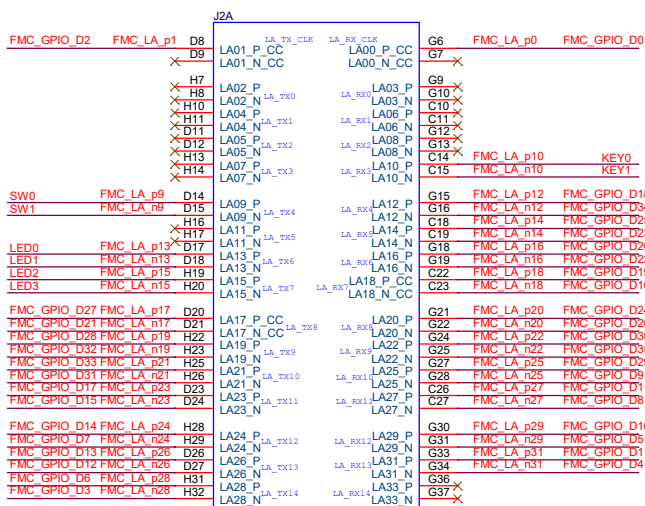
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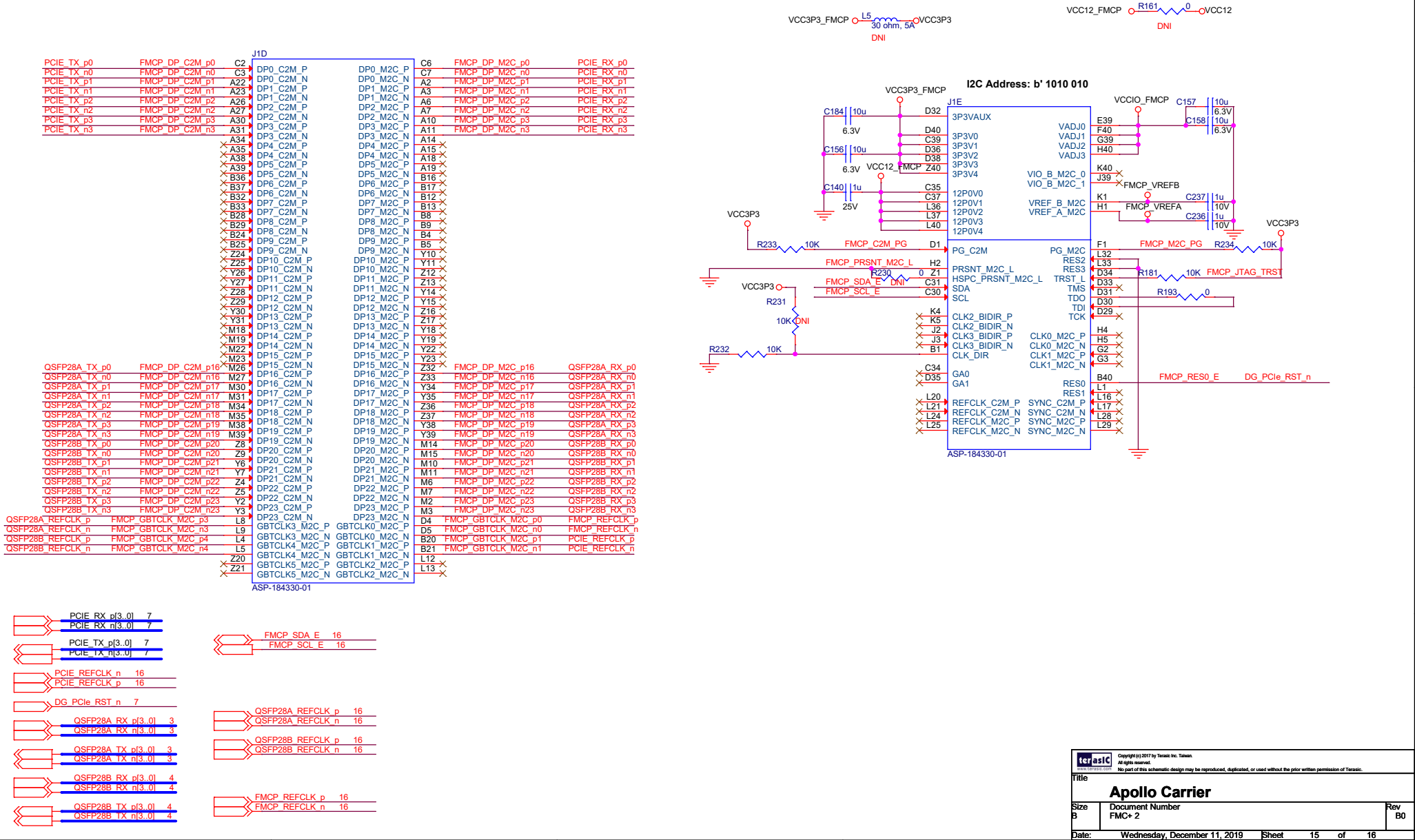
FMC PORT



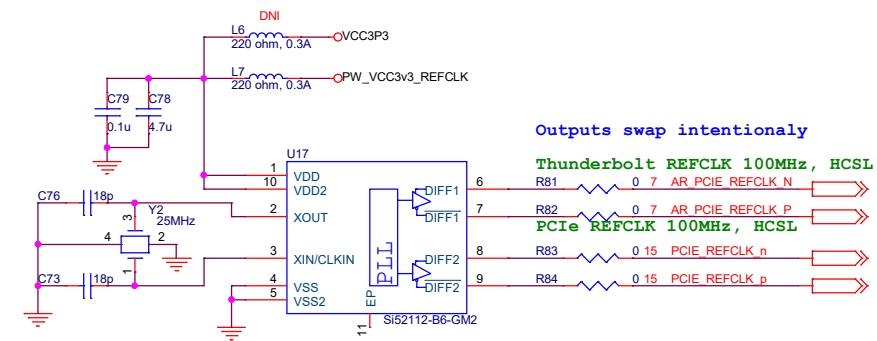
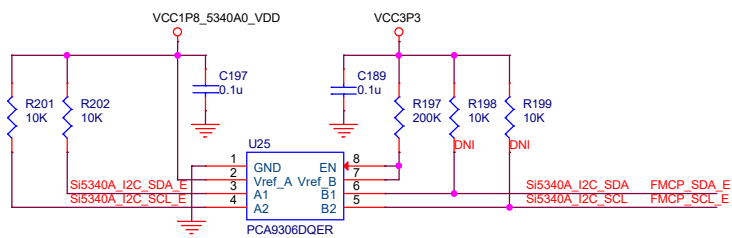
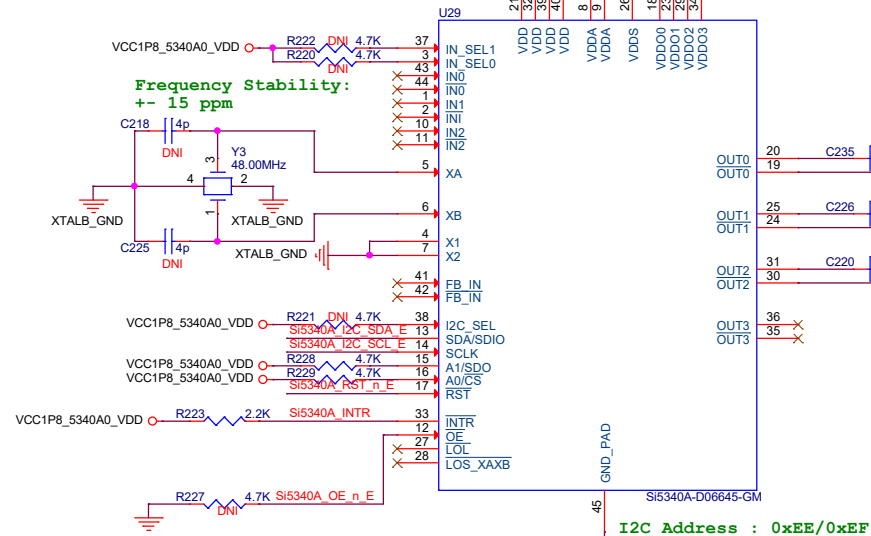
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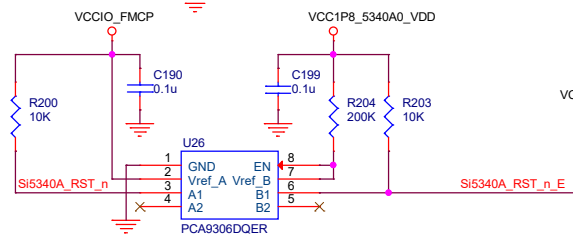
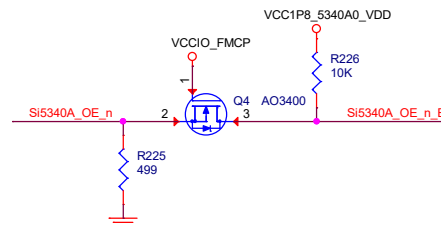
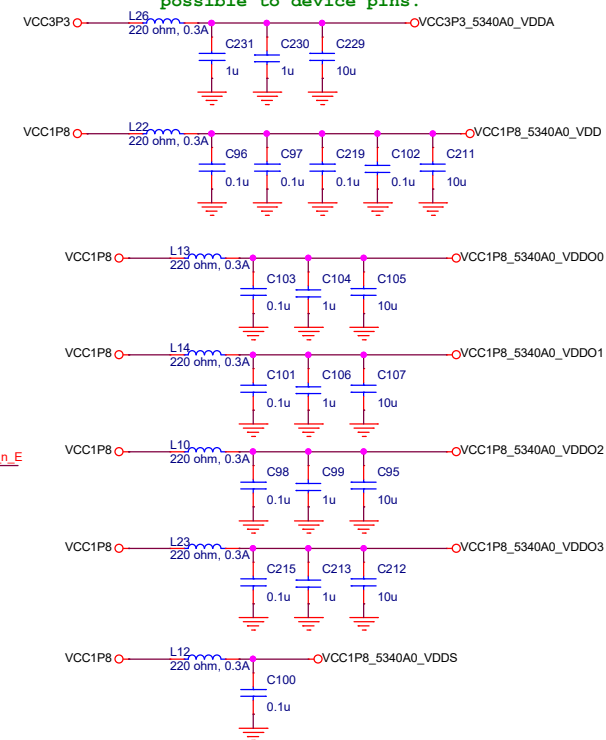
FMC+ 2



FMCP_SDA_E 15
FMCP_SCL_E 15
SI5340A_RST_n 14
SI5340A_OE_n 14



Place 0.1uF and 1uF caps as close as possible to device pins.



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