友晶科技
TERASIC TECHNOLOGIES
新竹縣竹北市福興東路一段 356 號
TEL ：03-550-8800
FAX ：03-550-2860

料 件 承 認 書

文件編號 ：MIC-3203-01	發行日期	
文 件 名 稱 ： IC －TI, 8 包 裝 雙 向 電 位 轉 換 器 (TXB0108RGYR) 承認書	發行版次	**1.0**
	總 頁 數	

廠內料號 ： **MIC-3203-TIX**

供應商名稱 ： **TI**

供應商料號 ： **TXB0108RGYR**

名稱／規格 ： **8 包裝雙向電位轉換器(TXB0108RGYR)**

是否需要預先燒錄 ：□是 ■否
附件連結 ：(連結位址)
料號申請連結 ：(Mantis link)

NO	發行日期	製/修訂內容	修訂頁次	版本
01		初版發行	-	1.0

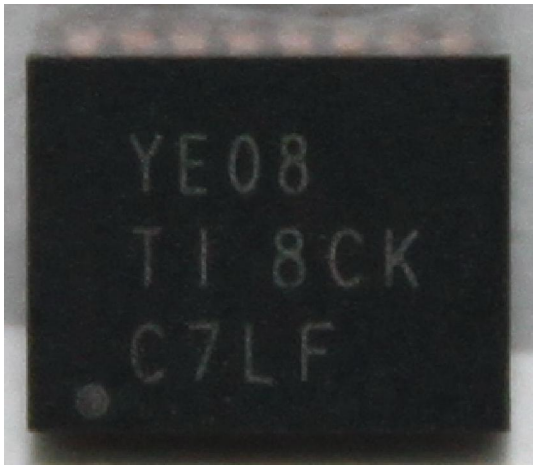
DCC	審核	主管	製作
			Allen Wang

友晶科技
TERASIC TECHNOLOGIES
新竹縣竹北市福興東路一段 356 號
TEL ：03-550-8800
FAX ：03-550-2860

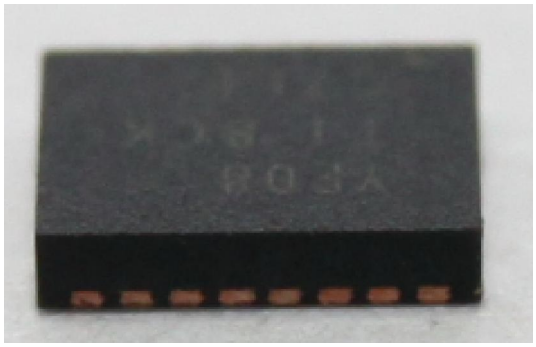
料件外觀 ：

料件外觀 ：

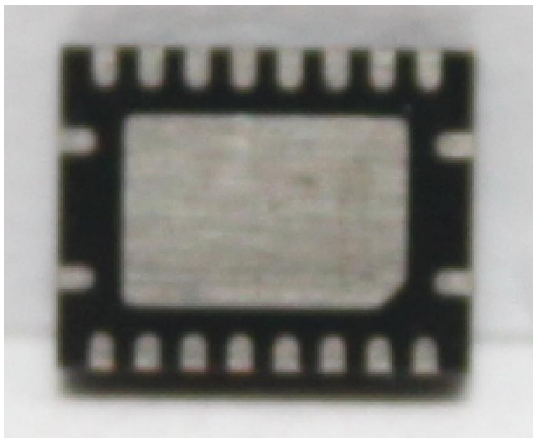
正面



側面



背面



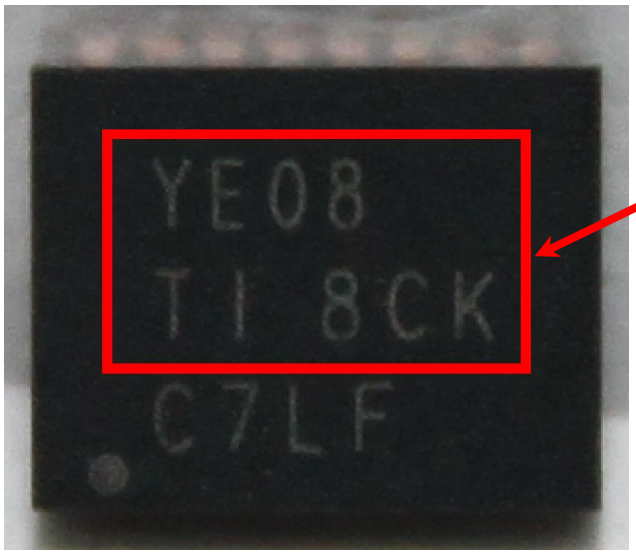
新竹縣竹北市福興東路一段 356 號
TEL ：03-550-8800
FAX ：03-550-2860

檢驗規範 / 重點

1. 請核對原廠料號。
2. 請確認零件的引脚是否有脱落。
3. 請確認零件包裝是否正確。
4. 請確認零件正面的 Mark 是否有 “YE08 TI 8CK” 字樣。

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Reel of 1000	TXB0108RGYR	YE08
	TSSOP – PW	Reel of 2000	TXB0108PWR	YE08
	VFBGA – GXY	Reel of 2500	TXB0108GXYR	YE08
	VFBGA – ZXY (Pb-free)	Reel of 2500	TXB0108ZXYR	YE08



請確認零件上面的文字印刷
是 “YE08 TI 8CK” 字樣

DESCRIPTION/ORDERING INFORMATION

This 8-bit noninverting translator uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.65 V to 5.5 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes. V_{CCA} should not exceed V_{CCB}.

When the output-enable (OE) input is low, all outputs are placed in the high-impedance state.

The TXB0101 is designed so that the OE input circuit is supplied by V_{CCA}.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Table 1. ORDERING INFORMATION(1)

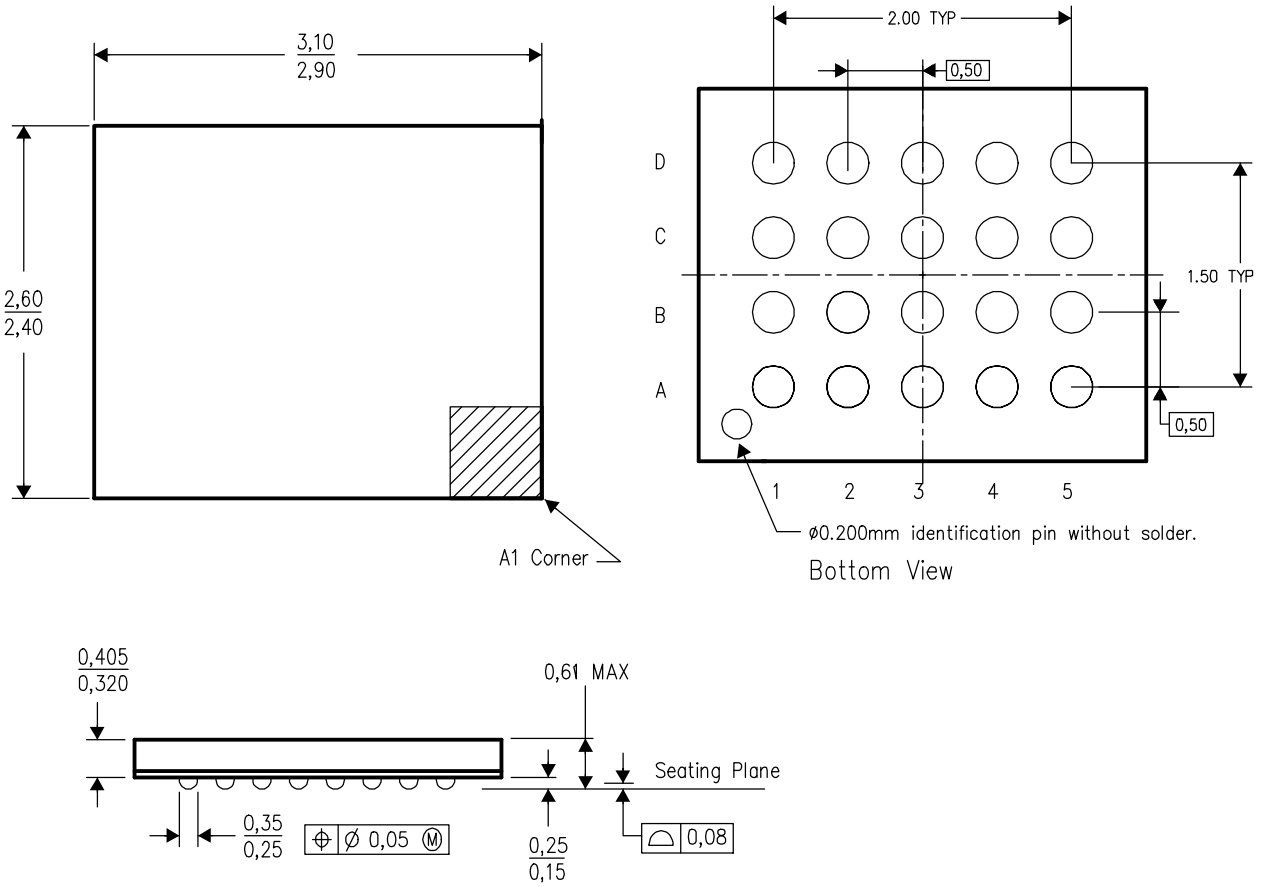
T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Reel of 1000	TXB0108RGYR	YE08
	SON – DQS	Reel of 2000	TXB0108DQSR	5MR
	TSSOP – PW	Reel of 2000	TXB0108PWR	YE08
	VFBGA – GXY	Reel of 2500	TXB0108GXYR	YE08
	VFBGA – ZXY (Pb-free)	Reel of 2500	TXB0108ZXYR	YE08

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

PIN DESCRIPTION

NO. (DQS, PW, RGY)	NAME	FUNCTION
1	A1	Input/output 1. Referenced to V_{CCA}.
2	V_{CCA}	A-port supply voltage. 1.1 V ≤ V_{CCA} ≤ 3.6 V, V_{CCA} ≤ V_{CCB}.
3	A2	Input/output 2. Referenced to V_{CCA}.
4	A3	Input/output 3. Referenced to V_{CCA}.
5	A4	Input/output 4. Referenced to V_{CCA}.
6	A5	Input/output 5. Referenced to V_{CCA}.
7	A6	Input/output 6. Referenced to V_{CCA}.
8	A7	Input/output 7. Referenced to V_{CCA}.
9	A8	Input/output 8. Referenced to V_{CCA}.
10	OE	Output enable. Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}.
11	GND	Ground
12	B8	Input/output 8. Referenced to V_{CCB}.
13	B7	Input/output 7. Referenced to V_{CCB}.
14	B6	Input/output 6. Referenced to V_{CCB}.
15	B5	Input/output 5. Referenced to V_{CCB}.
16	B4	Input/output 4. Referenced to V_{CCB}.
17	B3	Input/output 3. Referenced to V_{CCB}.
18	B2	Input/output 2. Referenced to V_{CCB}.
19	V_{CCB}	B-port supply voltage. 1.65 V ≤ V_{CCB} ≤ 5.5 V.
20	B1	Input/output 1. Referenced to V_{CCB}.

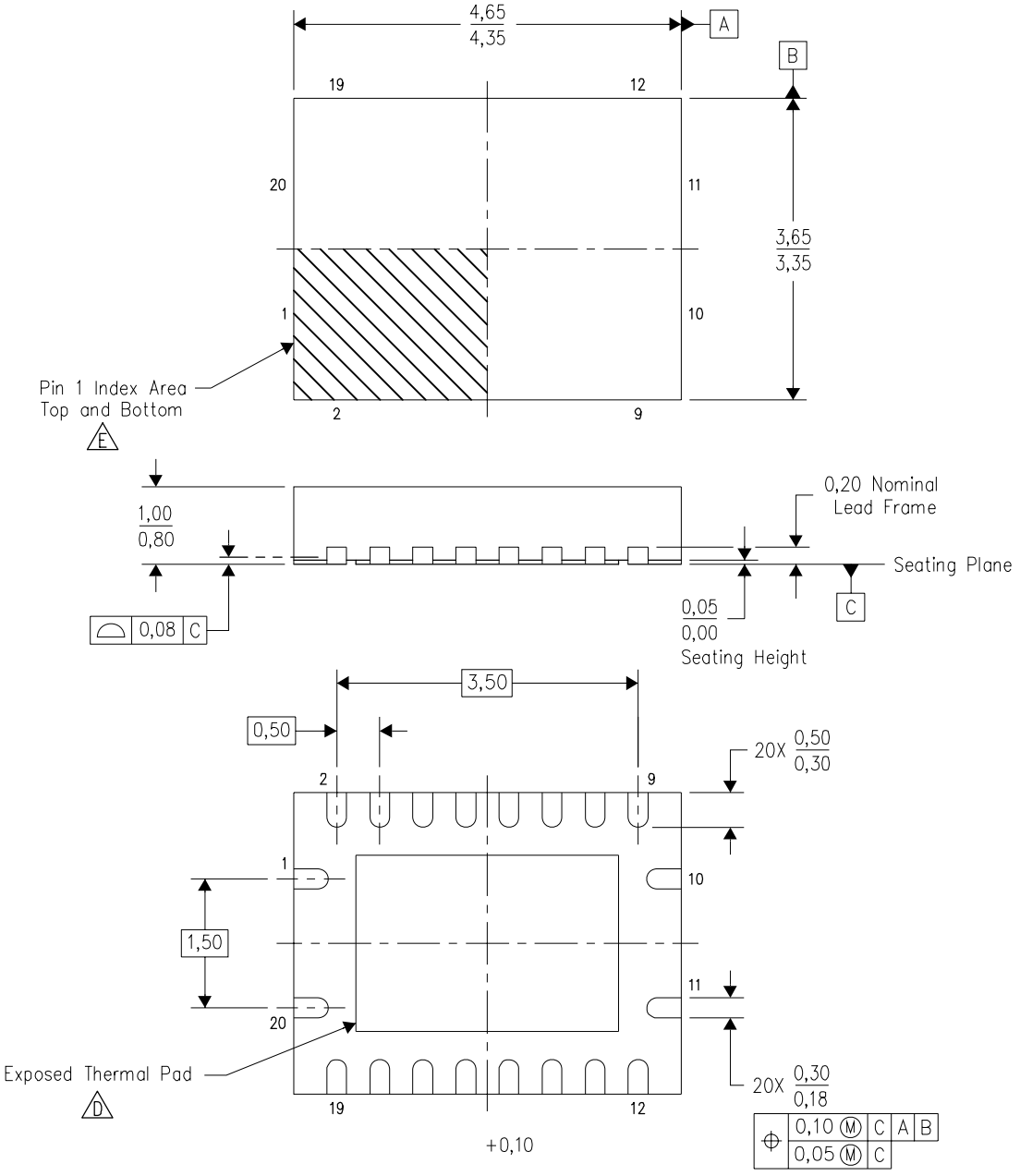
ZXY (S–PBGA–N20) PLASTIC BALL GRID ARRAY



4207061/A 06/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is a lead–free solder ball design.

RGY (R–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



4203539–4/H 06/2009

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
F. Package complies to JEDEC MO–241 variation BC.

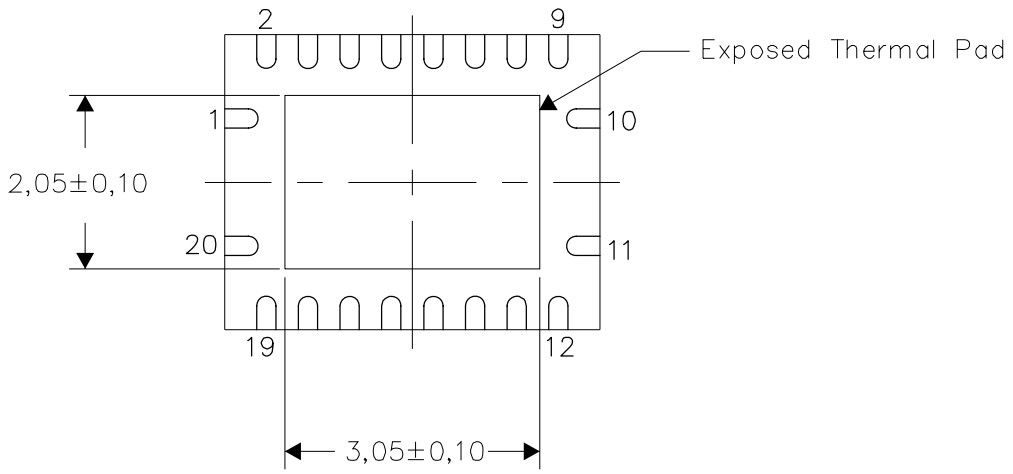
RGY (R–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

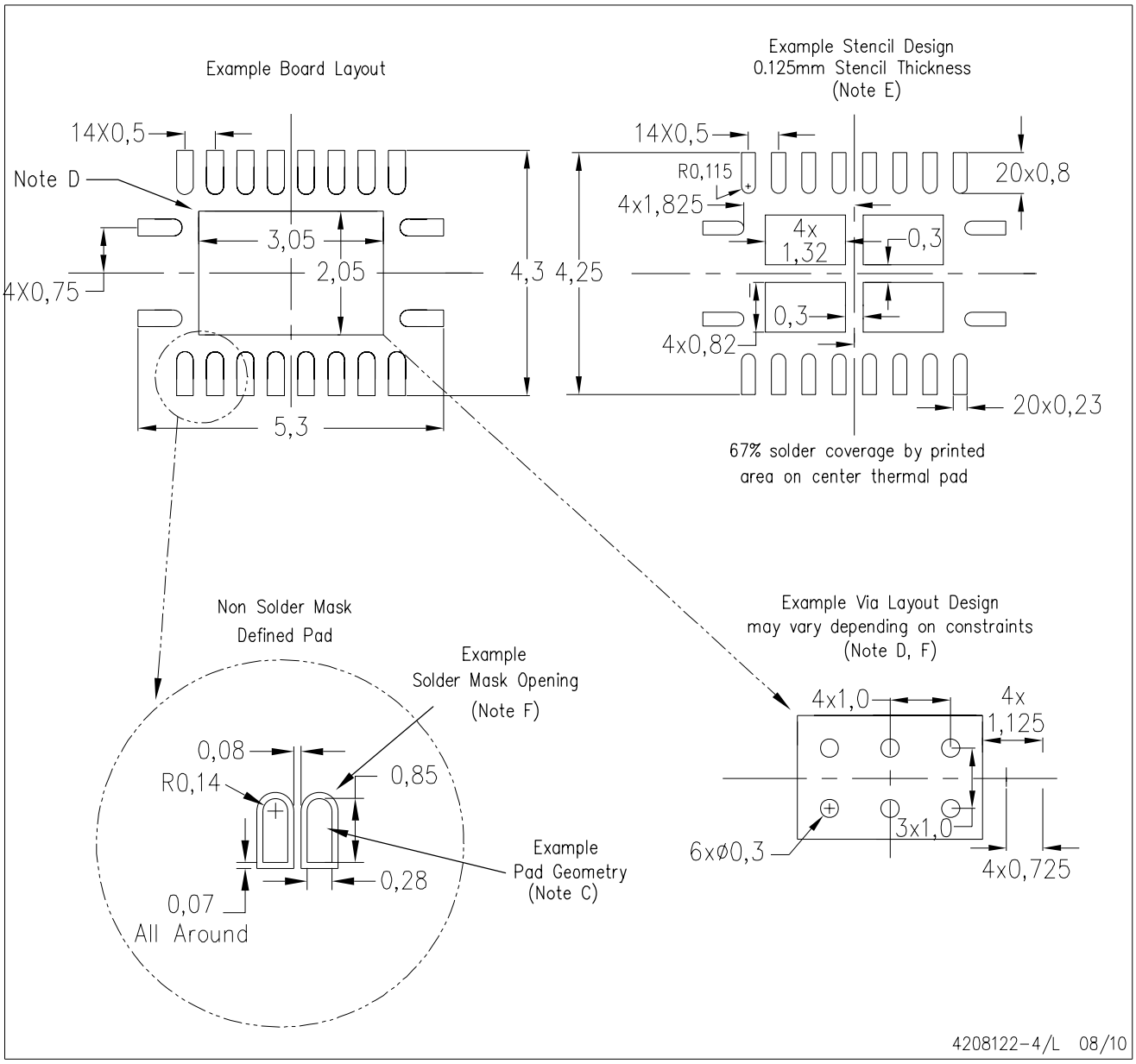


Bottom View

NOTE: All linear dimensions are in millimeters

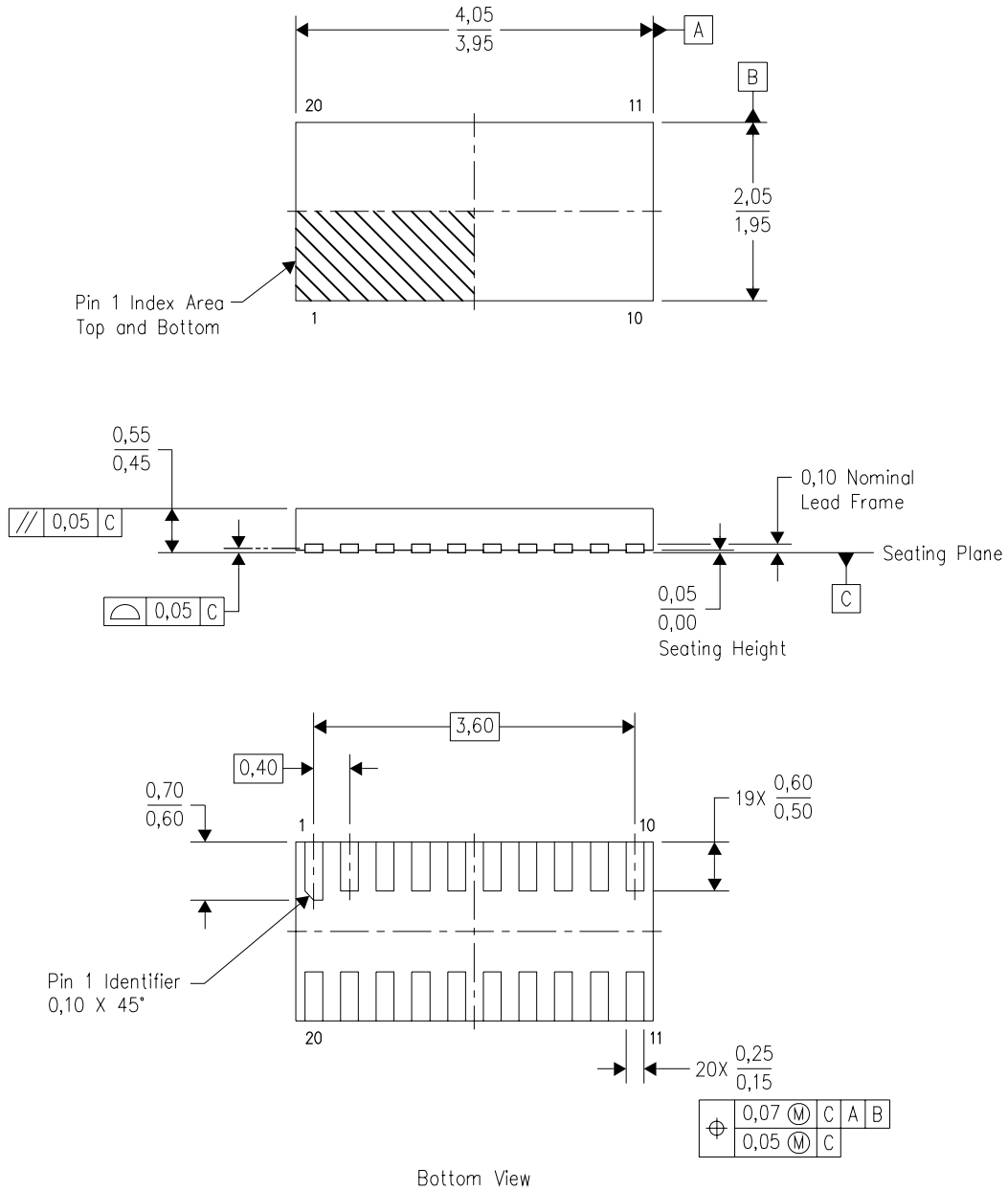
Exposed Thermal Pad Dimensions

RGY (R–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

DQS (R–PSON–N20) PLASTIC SMALL OUTLINE NO–LEAD



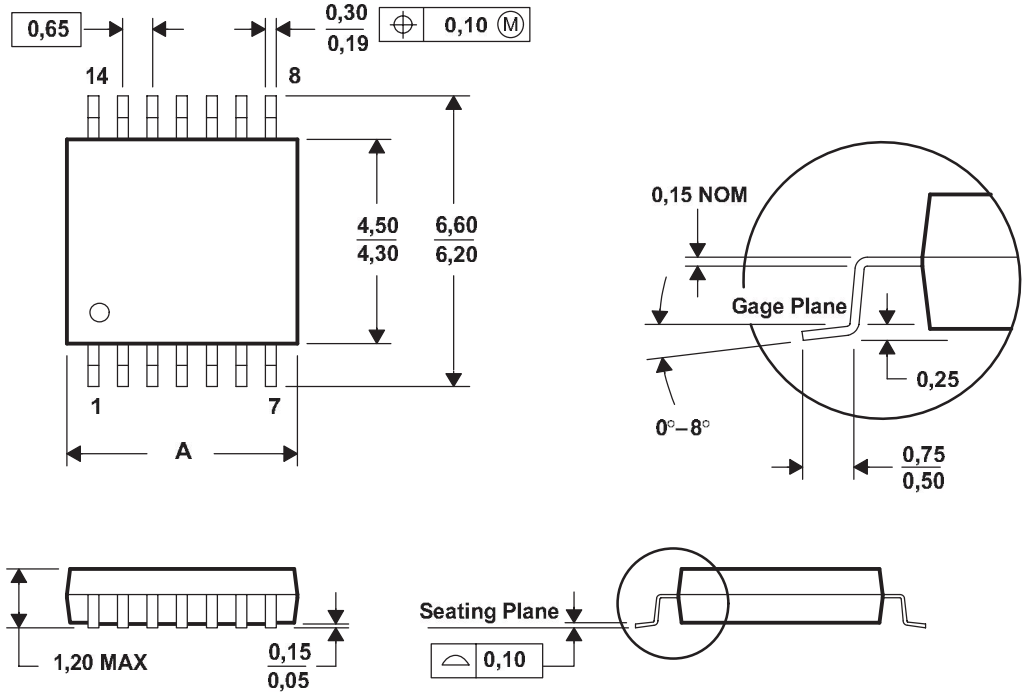
4210558/A 09/2009

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.

MTSS001C – JANUARY 1995 – REVISED FEBRUARY 1999

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153