產 品 承 認 書
(APPROVAL SHEET)

公司名稱 (Customer)：友晶科技股份有限公司

商越料號 (Customer P/N)：D3SH28081XH18AB

產品名稱 (Part Description)：DDR3-1066 1GB 204PIN 記憶體模組(無鉛)

製造原廠 (Manufacture)：商越科技股份有限公司

晶片廠牌 (Chip brand)：HYNIX (128MX8)

晶片編號 (Dram P/N:)：H5TQ1G83(X)FR-H9C

日 期 (Date)：

核准 (Approval by)	客戶料號 (Customer P/N:)	承認日期 (Date of Issuance)

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D3SH28081XH18AB

Specifications

Density:	1GB	**Data Rate:**	1066 Mbps
Pin Count:	204-pin	**CAS Latency:**	7
Version:	Unbuffered	**Voltage:**	1.5V
Type:	SO-DIMM	**PCB Layers:**	6
Speed:	PC3-8500	**ECC :**	Non-ECC
Component Config:	128Meg x 8	**Module Ranks :**	Single Rank

Features

- Data rate:1066Mbps
- Power supply: VDD= 1.5V ± 0.075V
- Interface: SSTL_15
- /CAS Latency(CL):5,6,7,8,9
- /CAS write latency(CWL):5,6,7
- Fully differential clock inputs (CK, /CK) operation
- Differential Data Strobe (DQS, /DQS)
- DM masks write data-in at the both rising and falling edges of the data strobe
- BL switch on the fly
- 8banks
- 8K refresh cycles /64ms
- Dynamic On Die Termination supported
- Asynchronous RESET pin supported
- ZQ calibration supported
- TDQS (Termination Data Strobe) supported (x8 only)
- Write Levelization supported
- Refresh: Auto-Refresh, Self-Refresh
- On Die Thermal Sensor supported(JEDEC optional)
- 8 bit pre-fetch
- Lead-Free Products are RoHS compliant
- Average Refresh Period 7.8us at 0℃ ≦TC≦85℃
  3.9us at 85℃ ＜TC≦95℃

D3SH28081XH18AB

Description

The D3SH28081XH18AB is 128M words X 64 bits, 1 ranks . Unbuffered Small Outline Dual In-Line Memory Module (SO-DIMM) .DDR3 SDRAMs in Fine Ball Grid Array(FBGA) packages on a 204pin glass-epoxy substrate. Provide a high performance 8 byte interface in 67.60mm width form factor of industry standard. It is suitable for easy interchange and addition.

Speed Grade & Key Parameters

Speed	DDR3-800	DDR3-1066	DDR3-1333	Unit
CL-tRCD-tRP	6-6-6	7-7-7	9-9-9	
tCK(min)	2.5	1.875	1.5	ns
CAS Latency	6	7	9	tCK
tRCD(min)	15	13.13	13.5	ns
tRP(min)	15	13.13	13.5	ns
tRAS(min)	37.5	37.5	36	ns
tRC(min)	52.5	50.625	49.5	ns
tRCF(min)	110	110	110	ns
tRRD(min)	10	7.5	6.0	ns
tFAW(min)	40	37.5	30	ns

Address Configuration

	512MB	1GB	1GB	2GB	2GB
Organization	64M X 64	128M X 64	128M X 72	256M X 64	256M X 72
Refresh Method	8K/64ms	8K/64ms	8K/64ms	8K/64ms	8K/64ms
Row Address	A0-A12	A0-A13	A0-A13	A0-A13	A0-A13
Column address	A0-A9	A0-A9	A0-A9	A0-A9	A0-A9
Bank Address	BA0-BA2	BA0-BA2	BA0-BA2	BA0-BA2	BA0-BA2
Auto Precharge	A10	A10	A10	A10	A10
# of Rank	1	1	1	2	2
# of DRAMs	4	8	9	16	18

D3SH28081XH18AB

Absolute Maximum ratings

Parameter	Symbol	Rating	Units	Notes
Voltage on VDD pin relative to Vss	VDD	-0.4V ~ +1.975V	V	
Voltage on VDDQ pin relative to Vss	VDDQ	-0.4V ~ +1.975V	V	
Input voltage	Vin	-0.4V ~ +1.975V	V	
Output voltage	VOUT	-0.4V ~ +1.975V	V	
Storage Temperature	TSTG	-55 to +100	℃	1
Operating case temperature	Toper	0 to 95	℃	2,3
Storage Humidity	HSTG	5 to 95	%	
Power dissipation	PD	9	W	
Short circuit output current	IOUT	50	mA	

Note:

1. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0-85℃ under all operating conditions.
3. Some applications require operation of the Extended Temperature Range between 85℃ and 95℃ case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
   a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9us. It is also possible to specify a component with 1X refresh(tREFI to 7.8us) in the Extended Temperature Range.
   b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability(MR2A6=0b and MR2A7=1b) or enable the optional Auto Self-Refresh mode(MR2A6=1b and MR2A7=0b)

D3SH28081XH18AB

Recommended DC Operating Conditions(SSTL-15)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max		
VDD	Supply Voltage	1.425	1.5	1.575	V	1,2
VDDQ	Supply Voltage for Output	1.425	1.5	1.575	V	1,2
VSS	Supply Voltage	0	0	0	V	1
VDDSPD	Supply Voltage	3.0	3.3	3.6	V	
VREFCA(DC)	Input reference voltage	0.49xVDDQ	0.50xVDDQ	0.51xVDDQ	V	1
VREFDQ(DC)	Input reference voltage for DQ	0.49xVDDQ	0.50xVDDQ	0.51xVDDQ	V	1

Note:

1. DDR3 SDRAM component specification.
2. Under all conditions VDDQ must be less than or equal to VDD.

Pin Description

Pin Name	Description	Pin Name	Description
A0~A9,A11 A13-A15	Address intput	VREFCA VREFDQ	Input/Output voltage reference
A10(AP)	Auto precharge	/CK0,/CK1	SDRAM differential clock input
A12(/BC)	Bust chop	CK0,CK1	SDRAM clocks input
/RAS	SDRAM Row address strobe	SCL	Clock input for serial PD
/CAS	SDRAM Column address strobe	SDA	Data intput/output for serial PD
/WE	SDRAM write enable	SA0-SA1	Serial address select intput
/CS0-/CS1	Chip select	VDD*	SDRAM core power supply
CKE0,CKE1	SDRAM clock enable	VDDQ*	SDRAM I/O Driver power supply
ODT0,ODT1	On-die termination control	VREF	SDRAM I/O reference supply
DQ0-DQ63	Data input/output	VSS	Ground
BA0-BA2	SDRAM bank addresses	VDDSPD	Serial EEPROM positive power supply
DQS0-DQS7	Input and output data strobe	NC	No connection
DM0-DM7	SDRAM data mask /high data strobe	/RESET	Set DRAM to known state
/DQS0-/DQS7	Input and output data strobe	TEST	Used by memory bus analysis tools(unused on memory DIMMs)
VTT	SDRAM I/O termination supply	/EVENT	Temperature event pin

D3SH28081XH18AB

Pin Configuration

Pin	Front	Pin	Front	Pin	Front	Pin	Front	Pin	Front	Pin	Front
1	VREFD	2	Vss	71	Vss	72	Vss	139	Vss	140	DQ38
3	Vss	4	DQ4	K E Y				141	DQ34	142	DQ39
5	DQ0	6	DQ5	73	CKE0	74	CKE1	143	DQ35	144	Vss
7	DQ1	8	Vss	75	VDD	76	VDD	145	Vss	146	DQ44
9	Vss	10	/DQS0	77	NC	78	A15	147	DQ40	148	DQ45
11	DM0	12	DQS0	79	BA2	80	A14	149	DQ41	150	Vss
13	Vss	14	Vss	81	VDD	82	VDD	151	Vss	152	/DQS5
15	DQ2	16	DQ6	83	A12/BC	84	A11	153	DM5	154	DQS5
17	DQ3	18	DQ7	85	A9	86	A7	155	Vss	156	Vss
19	Vss	20	Vss	87	VDD	88	VDD	157	DQ42	158	DQ46
21	DQ8	22	DQ12	89	A8	90	A6	159	DQ43	160	DQ47
23	DQ9	24	DQ13	91	A5	92	A4	161	Vss	162	Vss
25	Vss	26	Vss	93	VDD	94	VDD	163	DQ48	164	DQ52
27	/DQS1	28	DM1	95	A3	96	A2	165	DQ49	166	DQ53
29	DQS1	30	/RESE	97	A1	98	A0	167	Vss	168	Vss
31	Vss	32	Vss	99	VDD	100	VDD	169	/DQS6	170	DM6
33	DQ10	34	DQ14	101	CK0	102	CK1	171	DQS6	172	Vss
35	DQ11	36	DQ15	103	/CK0	104	/CK1	173	Vss	174	DQ54
37	Vss	38	Vss	105	VDD	106	VDD	175	DQ50	176	DQ55
39	DQ16	40	DQ20	107	A10/AP	108	BA1	177	DQ51	178	Vss
41	DQ17	42	DQ21	109	BA0	110	/RAS	179	Vss	180	DQ60
43	Vss	44	Vss	111	VDD	112	VDD	181	DQ56	182	DQ61
45	/DQS2	46	DM2	113	/WE	114	/S 0	183	DQ57	184	Vss
47	DQS2	48	Vss	115	/CAS	116	ODT0	185	Vss	186	/DQS7
49	Vss	50	DQ22	117	VDD	118	VDD	187	DM7	188	DQS7
51	DQ18	52	DQ23	119	A13	120	ODT1	189	Vss	190	Vss
53	DQ19	54	Vss	121	/S 1	122	NC	191	DQ58	192	DQ62
55	Vss	56	DQ28	123	VDD	124	VDD	193	DQ59	194	DQ63
57	DQ24	58	DQ29	125	TEST	126	VREFCA	195	Vss	196	Vss
59	DQ25	60	Vss	127	Vss	128	Vss	197	SA0	198	NC
61	Vss	62	/DQS3	129	DQ32	130	DQ36	199	VDDSPD	200	SDA
63	DM3	64	DQS3	131	DQ33	132	DQ37	201	SA1	202	SCL
65	Vss	66	Vss	133	Vss	134	Vss	203	VTT	204	VTT
67	DQ26	68	DQ30	135	/DQS4	136	DM4				
69	DQ27	70	DQ31	137	DQS4	138	Vss				

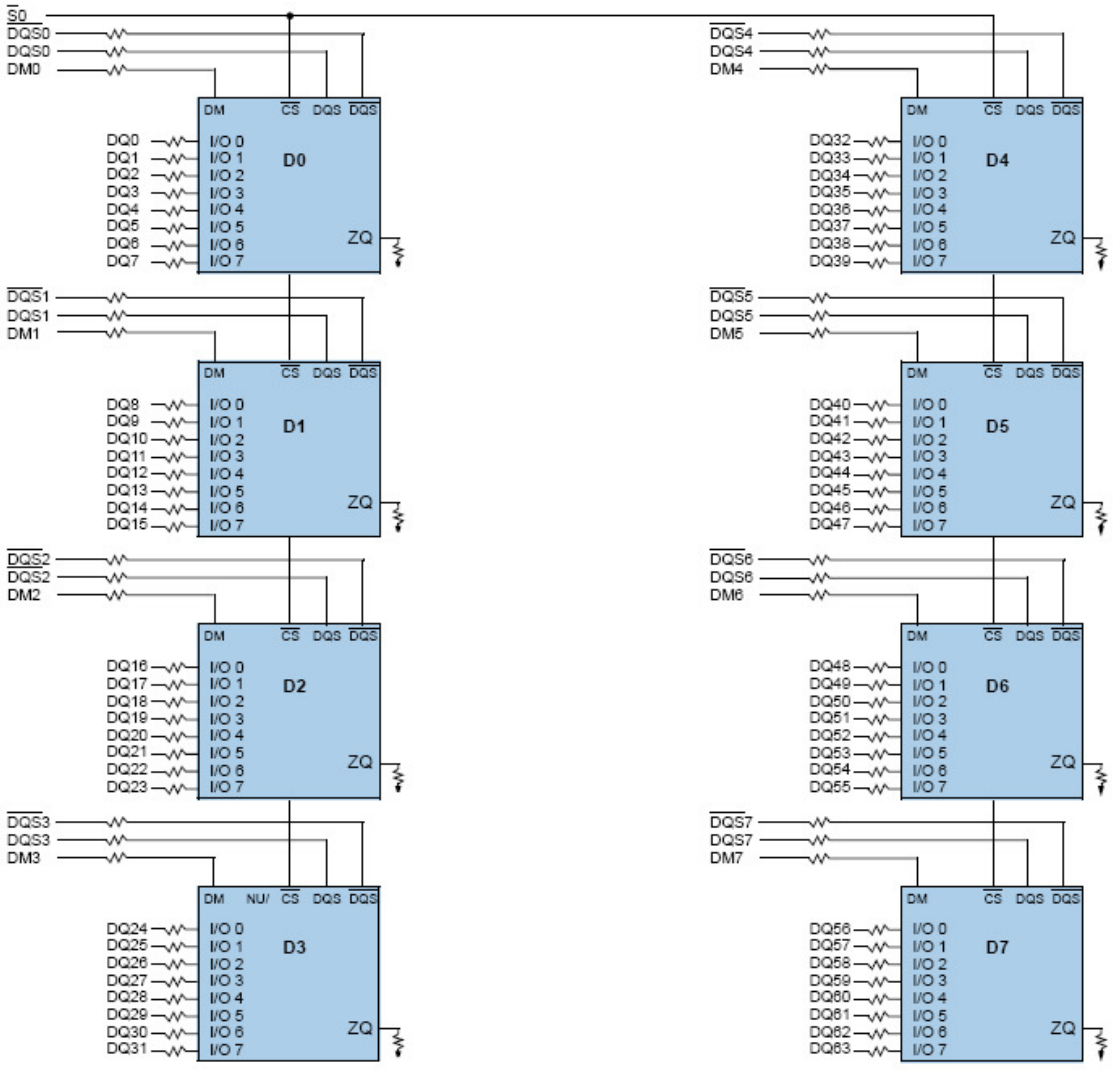
D3SH28081XH18AB

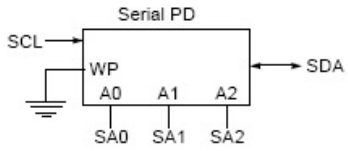
Input/Output Functional Description

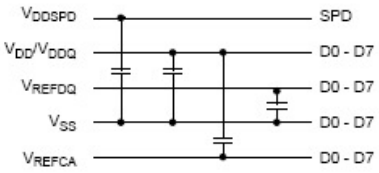
Symbol	Type	Function
CK0-CK1 /CK0-/CK1	Intput	The system clock inputs. All adrress and command lines are sampled on the cross point of the rising edge of CK and falling edge of CK. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operartion is synchronized to the input clock.
CKE0,CKE1	Intput	Activates the SDRAM CK signal when high and deactivates the CK Signal When low. By deactivating the clock, CKE low initiates the Power Down mode, or the Self-Refresh mode.
/S0,/S1	Intput	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new command are ignored but previous operations continue. Rank0 is selected by /S0;Rank1 is selected by /S1
/RAS,/CAS,/WE	Intput	$\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$(ALONG WITH /S) define the command being entered.
ODT0-ODT1	Intput	When high, termination resistance is enabled for all DQ, DQ and DM pins, assuming the function is enabled in the Extended Mode Register Set (EMRS).
VREFDQ	Supply	Reference voltage for SSTL 15 I/O Inputs.
VREFCA	Supply	Reference voltage for SSTL 15 command/address inputs.
VDDQ	Supply	Power supply for the DDR3 SDRAM output buffers to provide improved noise immunity. For all current DDR3 unbuffered DIMM designs, VDDQ shares the same power plane as VDD pins.
BA0-BA2	Intput	Selects which SDRAM bank of eight is activated.
A0-A9 A10(AP) A11 A12(/BC) A13-A15	Intput	During a Bank Activate command cycle, Address input defines the row address(RA0-RA13) During a Read or Write command cycle. Address input defines the column address. In addition to the column address. AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1,BA2 defines the bank to be precharged. If AP is low, autoprecharge is disbled. During a precharge command cycle, AP is used in conjunction with BA0,BA1,BA2 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0,BA1,BA2. If AP is low, BA0, BA1 are used to define which bank to precharge.
DQ0-DQ63	I/O	Data input/Output pins.
DM0-DM8	Intput	DM is and input mask signal for write data. Input data is masked when DM is sampled High coincident with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
VDD, Vss	Supply	Power and ground for DDR3 SDRAM input buffers, and core logic. VDD and VDDQ pins are tied to VDD/VDDQ planes on these modules.
DQS0-DQS8 /DQS0-/DQS8	I/O	Data strobe for input and output data.
SA0-SA2	Input	These signals and tied at the system planar to either VSS or VDD to configure the serial SPD EERPOM address range.
SDA	I/O-	This bi-directional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to VDD to act as a pullup on the system board.
SCL	Input	This signal is used to clock data into and out of the SPD EEPROM. An external resistor may be connected from the SCL bus time to VDDSPD to act as a pullup on the system board.
/EVENT		This signal indicates that a thermal event has been detected in the thermal sensing device. The system Should guarantee the electrical level requirement is met for /EVENT pin on TS/SPD part
VDD SPD	Supply	Power supply for SPD EEPROM. This supply is separate from the VDD/VDDQ power plane. EEPROM supply is operable from 3.0V to 3.6V.

D3SH28081XH18AB

FUNCTIONAL BLOCK DIAGRAM







BA0 - BA2	BA0-BA2 : SDRAMs D0 - D7
A0 - A13	A0-A13 : SDRAMs D0 - D7
$\overline{RAS}$	$\overline{RAS}$: SDRAMs D0 - D7
$\overline{CAS}$	$\overline{CAS}$: SDRAMs D0 - D7
CKE0	CKE : SDRAMs D0 - D7
$\overline{WE}$	$\overline{WE}$: SDRAMs D0 - D7
ODT0	ODT : SDRAMs D0 - D7
CK0	CK : SDRAMs D0 - D7

Note :

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/$\overline{DQS}$/ODT/DM/CKE/$\overline{S}$ relationships must be maintained as shown.
3. DQ, DM, DQS/$\overline{DQS}$ resistors: Refer to associated topology diagram.
4. Refer to the appropriate clock wiring topology under the DIMM wiring details section of this document.
5. Refer to section 7.1 of this document for details on address mirroring.
6. For each DRAM, a unique ZQ resistor is connected to ground. The ZQ resistor is 240 Ohm +/- 1%
7. One SPD exists per module.

D3SH28081XH18AB

Byte No.	Function Described	Function Supported	Hex Value
0	Number of serial PD bytes written/SPD device size/CRC coverage	176/256/0-116	92
1	SPD revision	Revision 1.0	10
2	Key bytes/DRAM device type	DDR3 SDRAM	0B
3	Key byte/module type	SO-DIMM	03
4	SDRAM density and banks	1G bite 8banks	02
5	SDRAM addressing	14row, 10 columns	11
6	Module nominal voltage, VDD	1.5V	00
7	Module organization	1 rank/x8 bites	01
8	Module memory bus width	64 bites / non-ECC	03
9	Fine timebase (FTB)dividend/divisor	5/2	52
10	Medium timebass (MTB) dividend	1	01
11	Medium timebass (MTB)divisor	8	08
12	SDRAM minimum cycle time	1.875ns	0F
13	Reserved		00
14	SDRAM /CAS latencies supported,LSB	CL=5,6,7,8	1E
15	SDRAM /CAS latencies supported, LSB		00
16	SDRAM minimum /CAS latencies time	13.125ns	69
17	SDRAM write recovery time	15ns	78
18	SDRAM minimum /RAS to CAS delay	13.125ns	69
19	SDRAM minimum row active to row active delay	7.5ns	3C
20	SDRAM minimum row precharge time	13.125ns	69
21	SDRAM upper nibbles for t RAS and t RC		11
22	SDRAM minimum active to precharge time	37.5ns	2C
23	SDRAM minimum active to active /autorefresh time	50.625 ns	95
24	SDRAM minimum refresh recovery time delay ,LSB	110 ns	70
25	SDRAM minimum refresh recovery time delay ,MSB	110 ns	03
26	SDRAM minimum internal write to read command delay	7.5 ns	3C
27	SDRAM minimum internal read to prechange command delay	7.5 ns	3C
28	Upper nibble for t FAW	37.5ns	01
29	Minimum for activate window delay time	37.5 ns	2C
30	SDRAM output drivers supported	DLL-off / RZQ/6,7	83

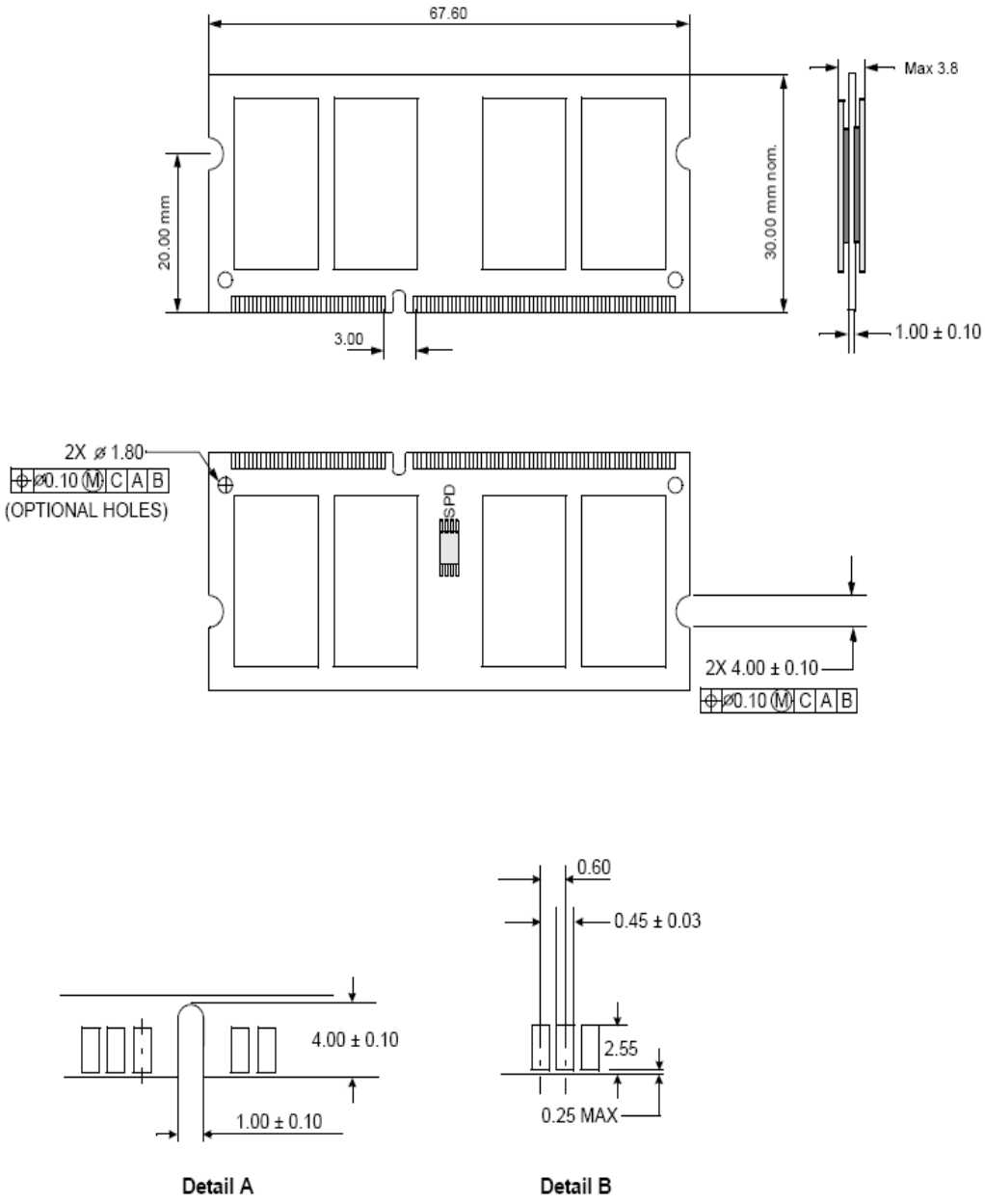
D3SH28081XH18AB

Byte No.	Function Described	Function Supported	Hex Value
31	SDRAM refresh options	PASR/2X refresh rate at +85°C to +95°C	05
32	Module thermal sensor	Not Incorparated	00
33	SDAM device type	Standard	00
34to59	Reserved	--	00
60	Module Nominal height	29<height≦30mm	0F
61	Module maximum thickness	--	11
62	Reference raw card used	Raw Card B1	01
63	Address mapping from edge connecter to DRAM	Standard	00
64to125			00
126	Cyclical redundancy code (CRC)	--	62
127	Cyclical redundancy code (CRC)	--	08
128	Module part number	D	44
129	Module part number	3	33
130	Module part number	S	53
131	Module part number	E	48
132	Module part number	2	32
133	Module part number	8	38
134	Module part number	0	30
135	Module part number	8	38
136	Module part number	1	31
137	Module part number	X	58
138	Module part number	H	48
139	Module part number	1	31
140	Module part number	8	38
141	Module part number	A	41
142	Module part number	B	42

D3SH28081XH18AB

PACKAGE DIMENSIONS

Unit :mm



Tolerances : ± 0.15mm unless otherwise specified

The used device is 128Mx8 HYNIX, DDR3,FBGA
DDR3 SDRAM Part No.: **H5TQ1G83(X)FR-H9C** *8EA

Declaration of Compliance with the RoHS Directive

DATA SPECIALTIES CO.,LTD Hereby declares that the products compliant with the European Union Directive 2002/95/EC for Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment(RoHS Directive).

Below list of DSL(DATA SPECIALTIES CO.,LTD.) products are Compliance.

No.	Substance	Max. Conc.
1	Cd (Cadmium)	<100ppm
2	Hg (Mercury)	<1000ppm
3	Pb (Lead)	<1000ppm
4	Cr+6 (Hexavalent Chromium)	<1000ppm
5	PBB (Polybrominated Biphenyl ethers)	<1000ppm
6	PBDE (Polybrominated Diphenyl)	<1000ppm

DATA SPECIALTIES CO., LTD.

Approved: Quality Engineering Team

Issued Date: 2007-06-20

Doc No: DS-0706-20

Declaration of Compliance with the PFOS Directive

DATA SPECIALTIES CO.,LTD Hereby declares that the products compliant with DIRECTIVE 2006/122/ECOF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL regarding exception of the use in photoresist or anti reflective coatings for photolithigrahy(usually semiconductor).

Only some kind of DATA SPECIALTIES CO.,LTD. Use PFOS in photoresist process, but do not contain PFOS in the Product.

DATA SPECIALTIES CO., LTD.
Approved: Quality Engineering Team
Issued Date: 2008-07-01
Doc No: DS-0807-01