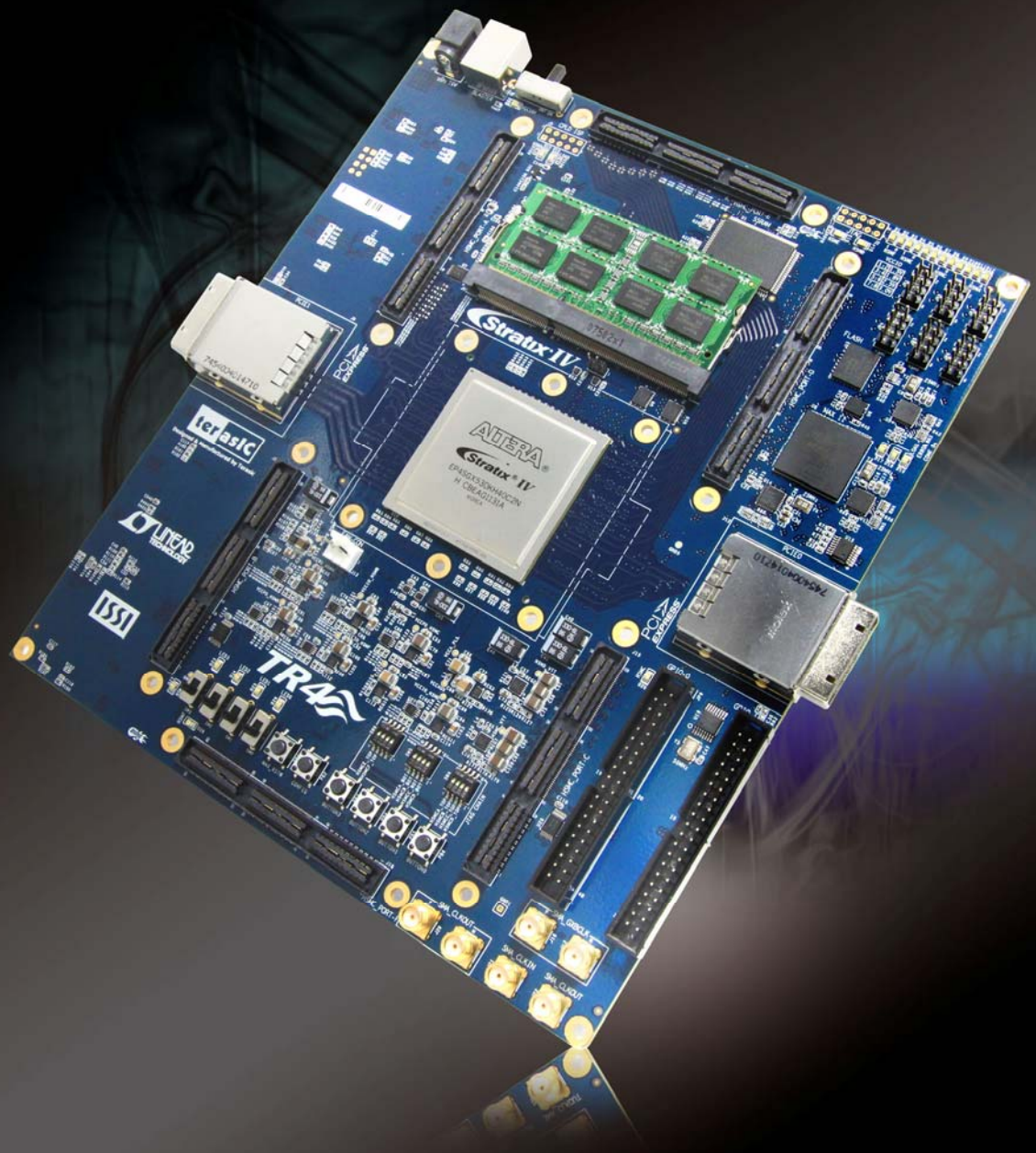
TR4

FPGA Development Kit

Getting Started Guide



Stratix IV GX | hsmc | Memory | PCI EXPRESS | DDR3

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Chapter 1

About this Guide

The TR4 Getting Started Guide contains a quick overview of the hardware and software setup including step-by-step procedures from installing the necessary software tools to using the TR4 board. Please read the user manual for an in-depth explanation of all components.

1.1 Introduction

The TR4 Development Board enables hardware and software developers to create or evaluate designs targeting two Stratix IV GX devices, EP4SGX230 or EP4SGX530. It provides a development environment for system designs that demand high-performance, serial connectivity and advanced memory interfacing.

The TR4 board features many embedded processing requirements that include: DDR3 SODIMM memory, two 4-lane PCI Express interface, and general purpose I/O. The TR4 is supported by multiple targeted reference designs in addition to High Speed Mezzanine Card (HSMC) connectors that allow scaling and customization with HSMC daughter cards.

1.2 TR4 Development Kit Contents

- TR4 FPGA Development Board
- 19V Power Supply (120W)
- Other Accessories
    - Type A-B USB cable
    - Screws, copper stands and jumpers
    - Fan (installed)
    - DDR3-1066 1GB SO-DIMM module
    - HSMC debug card
    - HSMC loopback adapter x 2
    - HTG (HSMC to GPIO daughter card)
    - THCB-HMF (HSMC Height Extension Male to Female card) x 2

- TR4 Development Kit CD-ROM – A CD-ROM that includes all the documentation and design examples.

Available on the Web

- Product home page: www.TR4.terasic.com
- Reference user guide, and design files
- Additional detailed documentation

1.3 Key Features

- Featured Device
  - Altera Stratix® IV GX FPGA (EP4SGX230C2/EP4SGX530C2)

- Configuration and Set-up Elements
  - Built-in USB Blaster circuit for programming
  - Fast passive parallel (FPP) configuration via MAX II CPLD and FLASH

- Components and Interfaces
  - Six HSMC connectors (two with transceiver support)
  - Two 40-pin GPIO expansion headers (shares pins with HSMC port C)
  - Two PCI Express 2.0 (x4 lane) connectors

- Memory
  - DDR3 SO-DIMM socket (4GB Max) •
  - 64MB FLASH
  - 2MB SSRAM

- General User Input/Output:
  - Four LEDs
  - Four push-buttons
  - Four slide switches

- Clock system
  - On-board 50MHz oscillator
  - Three on-board programmable PLL timing chips
  - One pair of SMA differential clock inputs

- One pair of SMA differential clock outputs
- SMA connector for external clock input
- SMA connector for clock output

- Other
  - Temperature sensor
  - FPGA cooling fan

1.4 Before You Begin

At all times, read the *Getting Started Guide* for the application instruction and be wary of precautions when operating the equipment. If any malfunctions occur, stop operation immediately and review the procedures. Please contact Terasic Technologies if there for any questions regarding the correct operating procedure. Never try to revise the development board's I/O direction, including wires and cables, by mounting daughter cards in any method besides original design intention. Doing so may void your warranty.

Chapter 2

Software Installation

2.1 Introduction

This section explains how to install the following software:

- Altera Complete Design Suite
- TR4 Development Board Contents
- USB-Blaster Driver

2.2 Installing the Altera Complete Design Suite

The Altera Complete Design Suite provides the necessary tools used for developing hardware and software solutions for Altera FPGAs. The Quartus II software is the primary FPGA development tool used to create reference designs along with the Nios II soft-core embedded processor integrated development environment, which are both included in the package DVD. Install the following software accompanied from the DVD or download the software from the Altera webpage: https://www.altera.com/download/software/quartus-ii-se/11.1

Obtaining a License File from Altera

The TR4 requires Quartus II Subscription Edition Software v11.1 to support the Stratix IV GX device. The Altera Complete Design Suite DVD from the TR4 kit includes the installation files for the Quartus II Subscription Edition Software v11.1, but the license must be separately requested from Altera's website (http://www.altera.com/support/licensing/lic-index.html). Please not that Quartus II Web Edition does not support Stratix IV GX devices. Only Quartus II Subscription Edition is enabled for Stratix IV GX compilation.

2.3 Installing the TR4 Contents

To install the necessary components for development on the TR4, copy the contents from the folder (TR4_SYSTEM_CD) located in the TR4 system CD to your computer. **Table 2–1** lists the associated directory name and description of contents.

Table 2–1 TR4 System CD Contents

Directory Name	*Description of Contents*
UserManual	**Contains the TR4 documentations**
Demonstrations	**Contains design examples of TR4**
Datasheet	**Contains the datasheets of the components on TR4**
Schematic	**Contains the schematic of TR4**
Tools	**Contains the design and testing tools for TR4**

2.4 Installing the USB-Blaster Driver

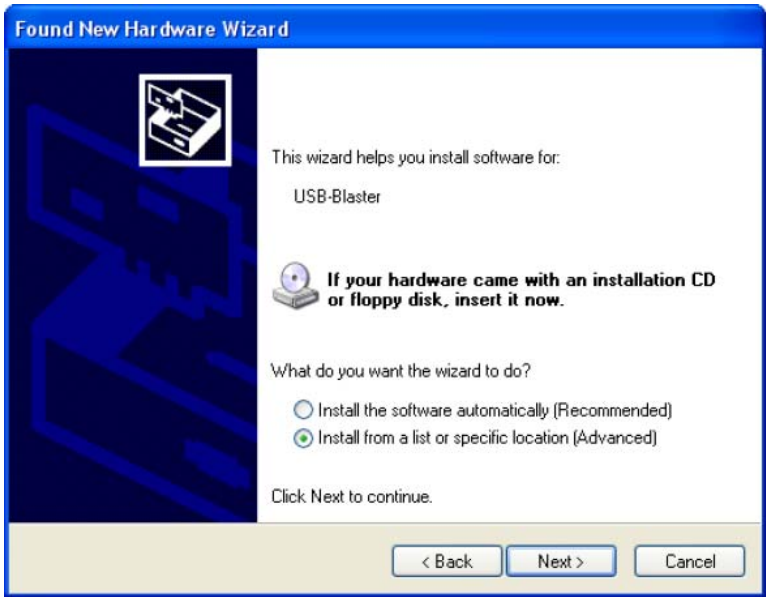
The TR4 development board includes an integrated USB Blaster circuitry for FPGA programming. However, for the host computer and development board to communicate, you must install the USB-Blaster driver on the host computer. Before you begin the installation, verify whether the USB-Blaster driver is located under the directory: \<Quartus II installation directory>\drivers\usb-blaster. If the USB-Blaster driver is not found, confirm the Quartus II software is properly installed.

The steps below outline how to install the USB-Blaster driver.

1. Recognize the new hardware connected:
The computer will recognize the new hardware connected to its USB port, but it will be unable to proceed if it does not have the required driver installed. The TR4 board is programmed by using Altera's USB-Blaster mechanism. Plug in the USB cable from the TR4 board to the PC and the *Found New Hardware Wizard* window will appear if no USB-blaster driver has been installed before.

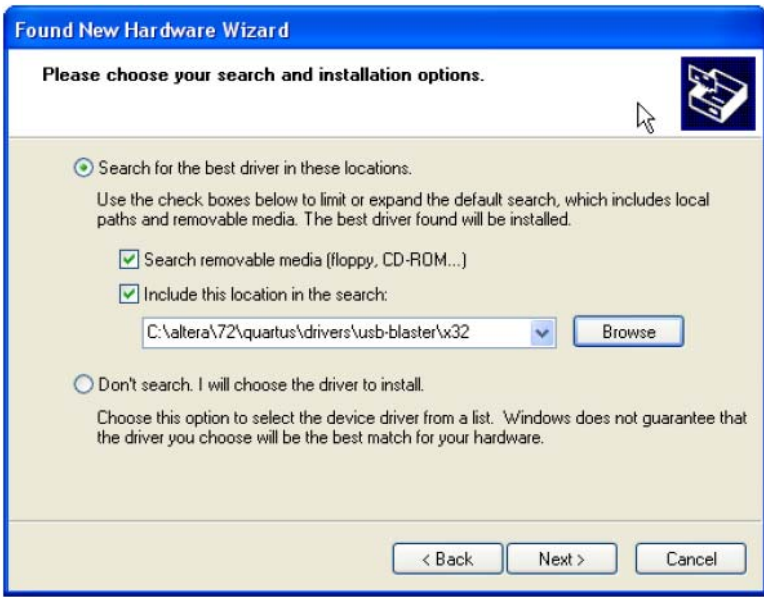
2. Specify the path for USB Blaster driver:

On the *Found New Hardware Wizard* window, click **No, not this time** and then click **Next** leading to the window below. Select Install from a **list of specific location (Advanced)** and click **Next** to continue.



3. Select appropriate driver version for USB-Blaster:

Select Search for **best driver in these locations** and click browse leading to pop-up box.

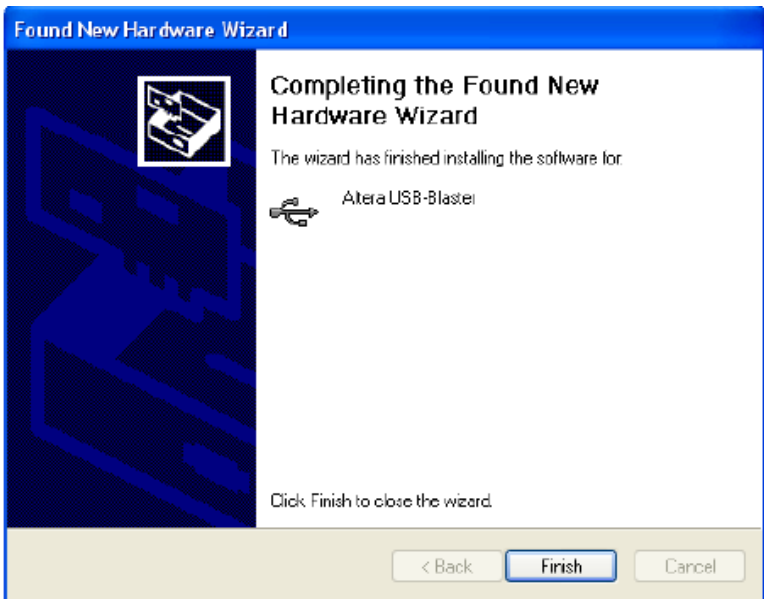


Find the appropriate driver located in \<Quartus II system directory>\drivers\usb-blaster. Click **OK** and from the returning window. Click **Next** to install the driver**.**

At this point the installation will commence, but a dialog box shown below will appear indicating the driver has not pass the Windows Logo testing. Click **Continue Anyway**.

4. The USB Blaster is ready for use:

The driver is now installed as indicated below. Click **Finish** and you can begin using the TR4 board.



Chapter 3

Development Board Setup

3.1 Introduction

The instructions in this section explain how to setup the TR4 development board.

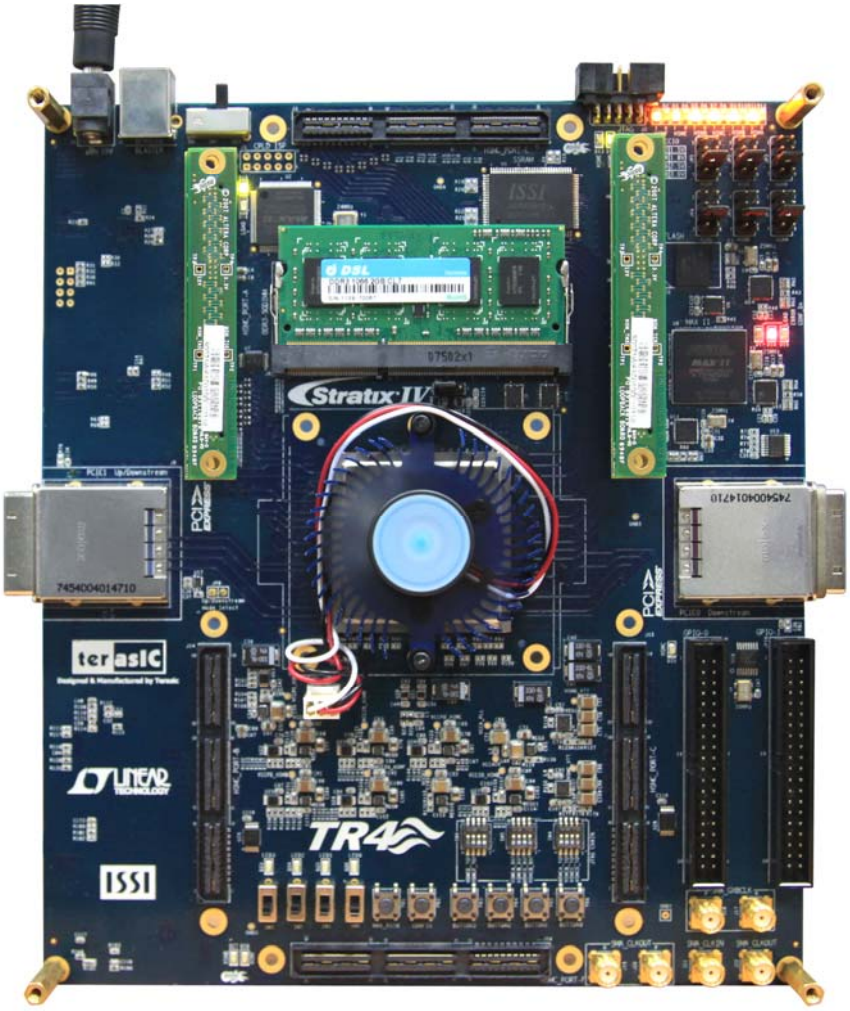
3.2 Powering up the TR4 Board

The MAX II CPLD (EPM2210) device on the TR4 contains a parallel flash loader (PFL) megafunction where a preloaded default configuration bit stream is loaded onto the CFI flash memory. The TR4 powering up sequence begins as the PFL initiates to read the design from the flash memory and configures the FPGA. To power-up the board, perform the following steps below:

1. Connect the provided power cord to the power supply and plug the cord into a power outlet (verify the voltage supplied is the same as the specification on the power supply).

2. Connect the supplied TR4 power cable from the connector of the power supply to the power connector (J1) on the TR4 board.

Connection setup for the TR4 board and power supply



3. Set the POWER_ON switch (SW7) in the ‘ON’ position. As power is supplied to the board, the LED (D33) illuminates to indicate the board has power from the 19V DC inputs.
You should observe the following once the default bit stream is loaded:

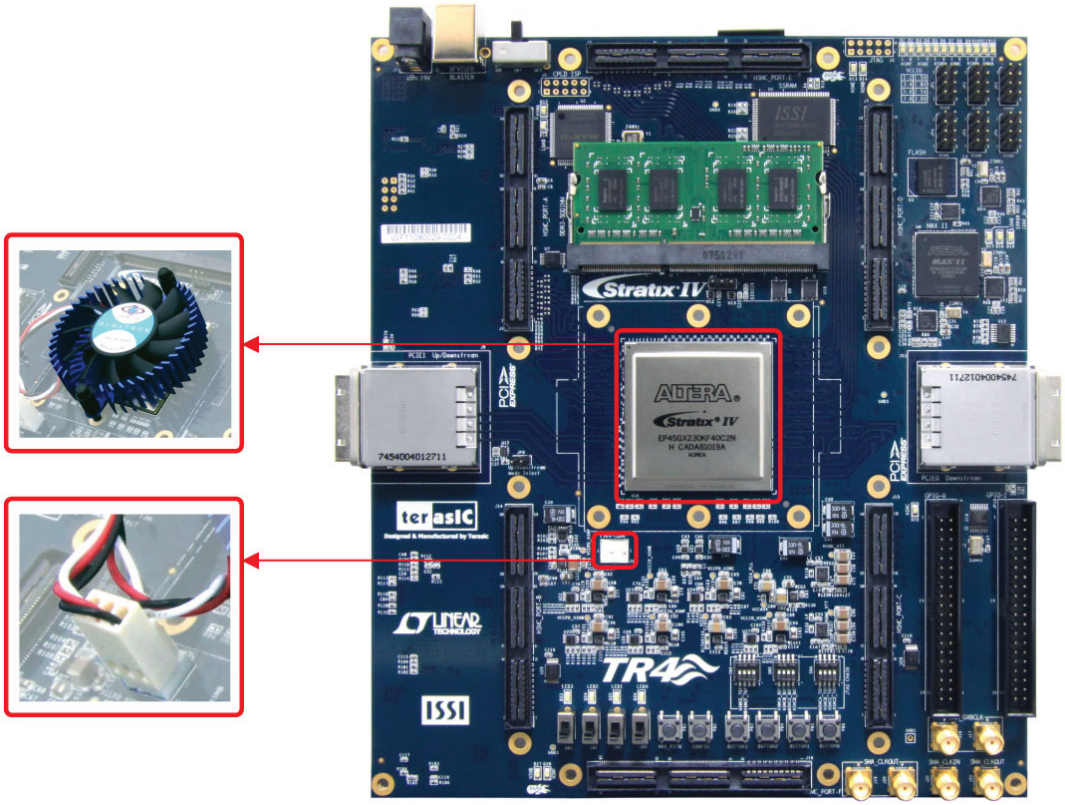
- User LEDs (LED0_LED3) flash in sequential pattern.
- Fan turns on.

CAUTION. It is important the fan is rotating after the TR4 is turned-on to prevent the Stratix IV GX device from overheating. In case the fan stops rotating, turn-off the TR4 board immediately to prevent damage.

3.3 Fan Installation

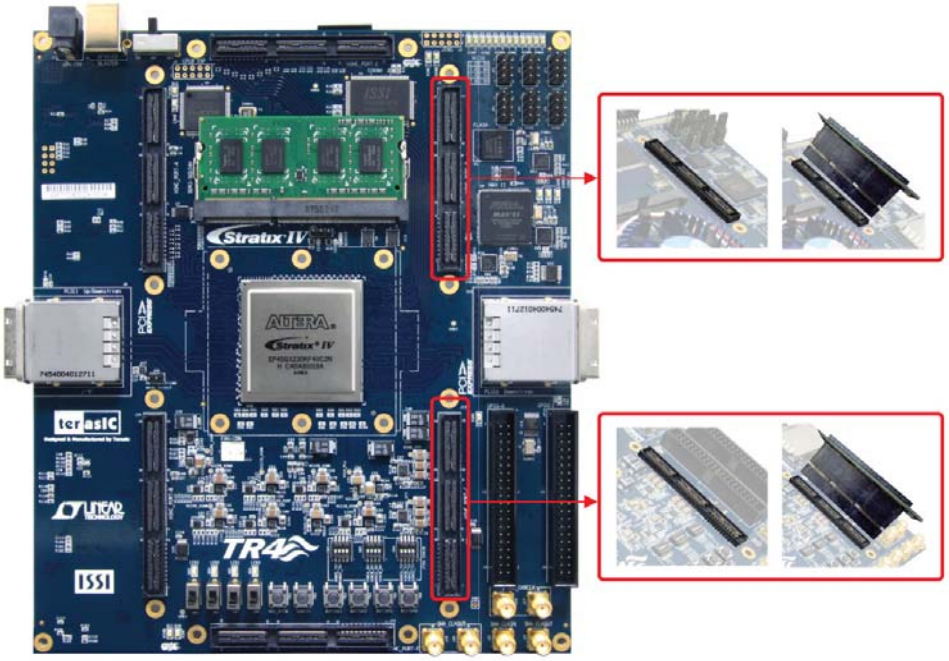
By default, a cooling fan is installed onto the Stratix IV GX device. It is recommended the fan be

placed on top of the Stratix IV GX device at all times to prevent it from overheating. In case the fan is accidentally removed, you can install it back in by pushing the two spring screws of the fan onto the holes followed by connecting the 3-pin connector onto the 3-pin header (J13) shown below.



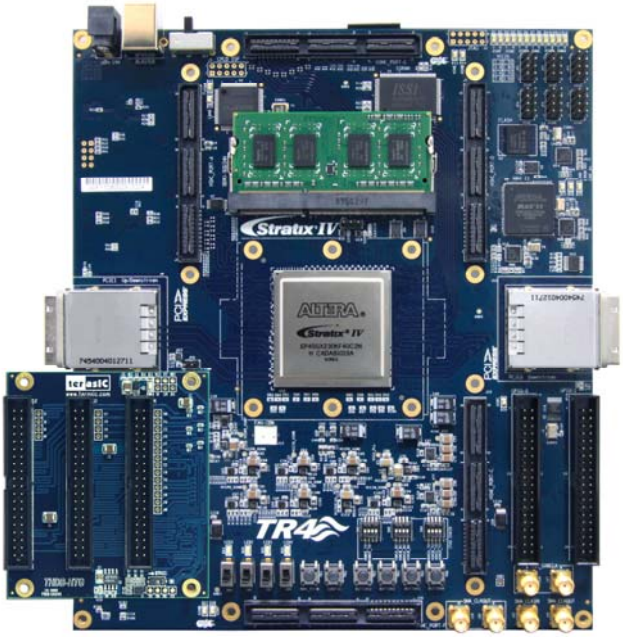
3.4 Using the THCB-HMF2

The purpose of the HSMC Height Extension Male to Female card (THCB-HMF2) is to provide proper spacing by increasing the height of the HSMC connector to avoid any obstruction that might take place when a HSMC daughter cards is connected. The THCB-HMF2 adapter card can be connected to any HSMC port depending on users' preference.



3.5 Using the HTG

The purpose of the HTG card is to provide conversion of the High-Speed Mezzanine Card (HSMC) port I/O to three 40-pin expansion prototype connectors.



Chapter 4

Programming the FPGA

4.1 Introduction

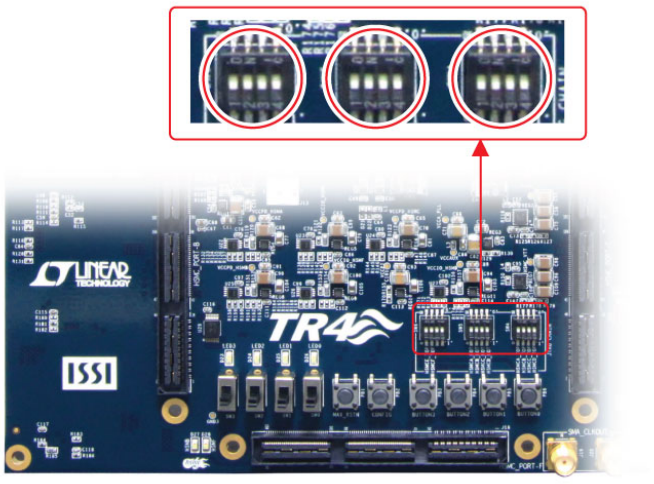
The Quartus II Programmer is used to configure the FPGA with a specific .sof. Before configuring the FPGA, ensure that the Quartus II software and the USB-Blaster driver are installed on the host computer.

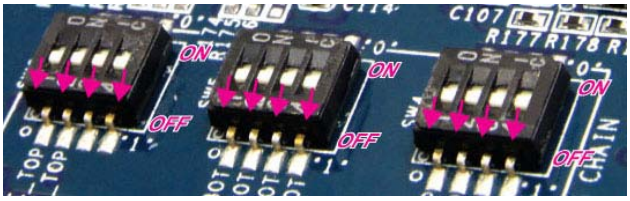
If users would like to program their SRAM Object File (.sof) into the Stratix IV GX FPGA device on the TR4 board, execute the following steps:

1. Connect the TR4 power cable to the power connector (J1) of the TR4 board while connecting the power cord to the power outlet.

2. Connect the USB cable from the USB blaster port (J4) on the TR4 board to your host computer.

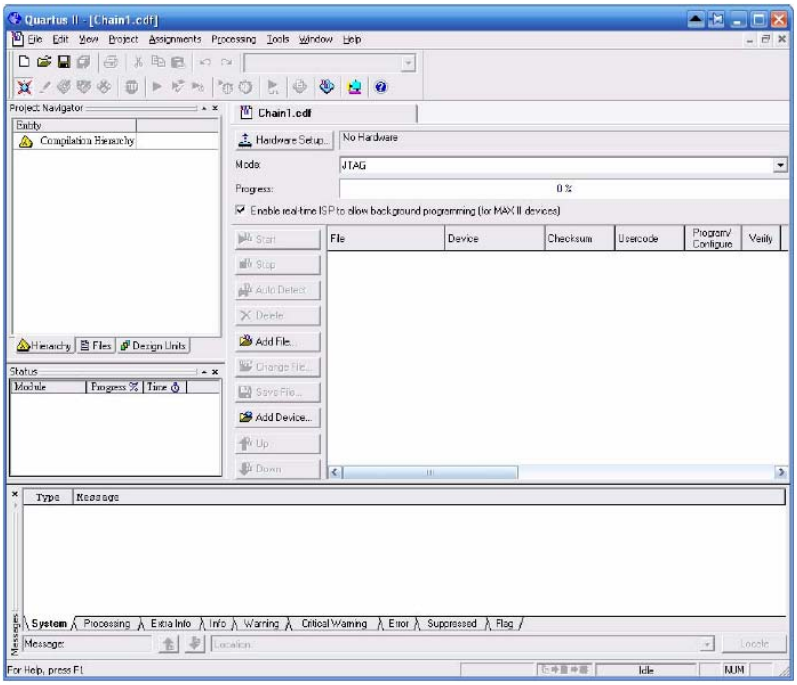
3. Set all the 4-position DIP switches (SW4, SW5, SW6) to the 'OFF' position.





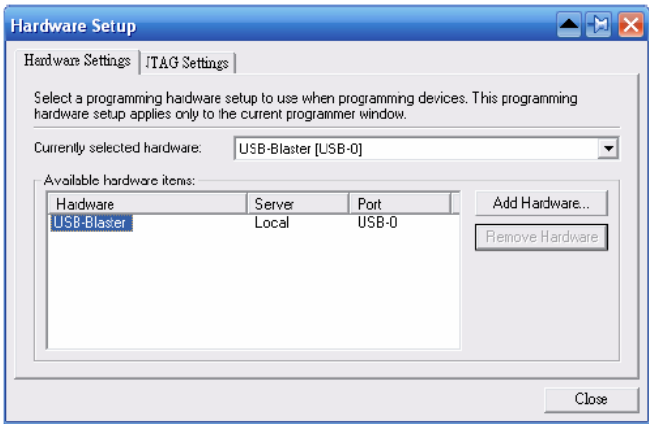
4. Turn on the power by switching the POWER_ON switch (SW7).

5. Open Quartus II software, select **Tools > Programmer**. The Programmer window will appear.



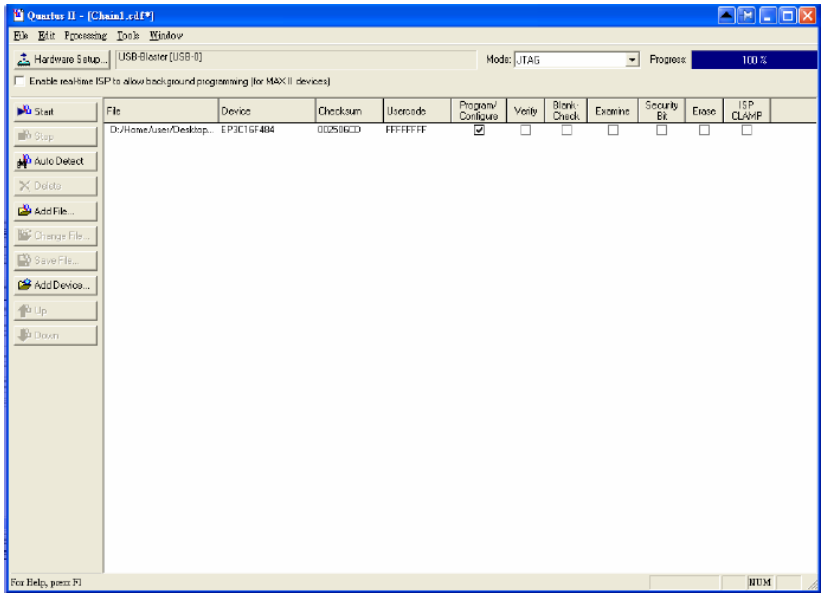
6. Click **Hardware Setup**.

7. If **USB-Blaster [USB-0]** does not appear under **Currently Selected Hardware**, select that option and click **Close** shown below.



8. Click **Add File** to select the .sof file and click **Open.**

9. Turn on the **Program/Configure** option that corresponds to the .sof file and click **Start** which will automatically download the file onto the TR4 board shown below.



Chapter 5

Programming with Flash

5.1 Introduction

The TR4 offers FPGA programming ability from the flash memory utilizing the Default Flash Loader to configure the FPGA. As you develop your own project using Altera tools, the demand for larger configuration storage will probably increase. Thus, the availability of Flash programming allows you to load your own designs onto the large Flash memory. There are several other factory software files written to the CFI flash device to support the Board Update Portal. These software files were created using Nios II EDS, just as the hardware design was created using Quartus II software.

5.2 CFI Flash Memory Map

Table 5–1 lists the default memory contents of the 512Mb (64MB) Intel PC48F4400P0VB00 CFI flash device. For the Board Update Portal to run correctly and to update designs in the user memory, this memory map should not be altered.

Table 5–1 Flash Memory Map

Block Description	*Size*	*Address Range*
User design reset vector	32KB	0x00000000 – 0x00007FFF
Unused	32KB	0x00008000 – 0x0000FFFF
Unused	32KB	0x00010000 – 0x00017FFF
PFL option bits	32KB	0x00018000 – 0x0001FFFF
Factory hardware image (User hardware)	24,576KB	0x00020000 – 0x0181FFFF
Unused	8,192KB	0x01820000 – 0x0201FFFF
Factory software image (User software)	32,640KB	0x02020000 – 0x03FDFFFF
Unused	32KB	0x03FE0000 – 0x03FE7FFF
Unused	32KB	0x03FE8000 – 0x03FEFFFF

Unused	**32KB**	**0x03FF0000 – 0x03FF7FFF**
Unused	**32KB**	**0x03FF8000 – 0x03FFFFFF**

5.3 Preparing Design Files

The Nios II EDS sof2flash command line utility converts your Quartus II-compiled **.sof** into **.flash** format necessary for the flash device. Similarly, the Nios II EDS elf2flash command line utility converts your compiled and linked Executable and Linking Format File (**.elf**) software design to **.flash**. After your design files are in the **.flash** format, use the Default Flash Loader or the Nios II EDS nios2-flash-programmer utility to write the **.flash** files to the user hardware and user software locations of the flash memory.

If your design uses additional files such as image data or files used by the runtime program, you must first convert the files to **.flash** format and concatenate them into one **.flash** file before using the Board Update Portal to upload them. Note a programming flash example with screen-shots is provided in section 5.5.

Creating flash files using the Nios II EDS command shell

If you have an FPGA design developed using the Quartus II software, and software developed using the Nios II EDS, follow these instructions:

1. On the Windows Start menu, click All Programs > Altera > Nios II EDS > Nios II Command Shell.

2. In the Nios II command shell, navigate to the directory where your design files reside and type the following Nios II EDS commands:
   a. For Quartus II .sof files:
   sof2flash --input=<your_design>_hw.sof --output=<your_design>_hw.flash --offset=0x00020000 --pfl --optionbit=0x18000 --programmingmode=FPP

   b. For Nios II .elf files:
   elf2flash --base=0x08000000 --end=0x0BFFFFFF --reset=0x0A020000 --input=<your_design>_sw.elf --output=<your_design>_sw.flash --boot=$SOPC_KIT_NIOS2/components/altera_nios2/boot_loader_cfi.srec

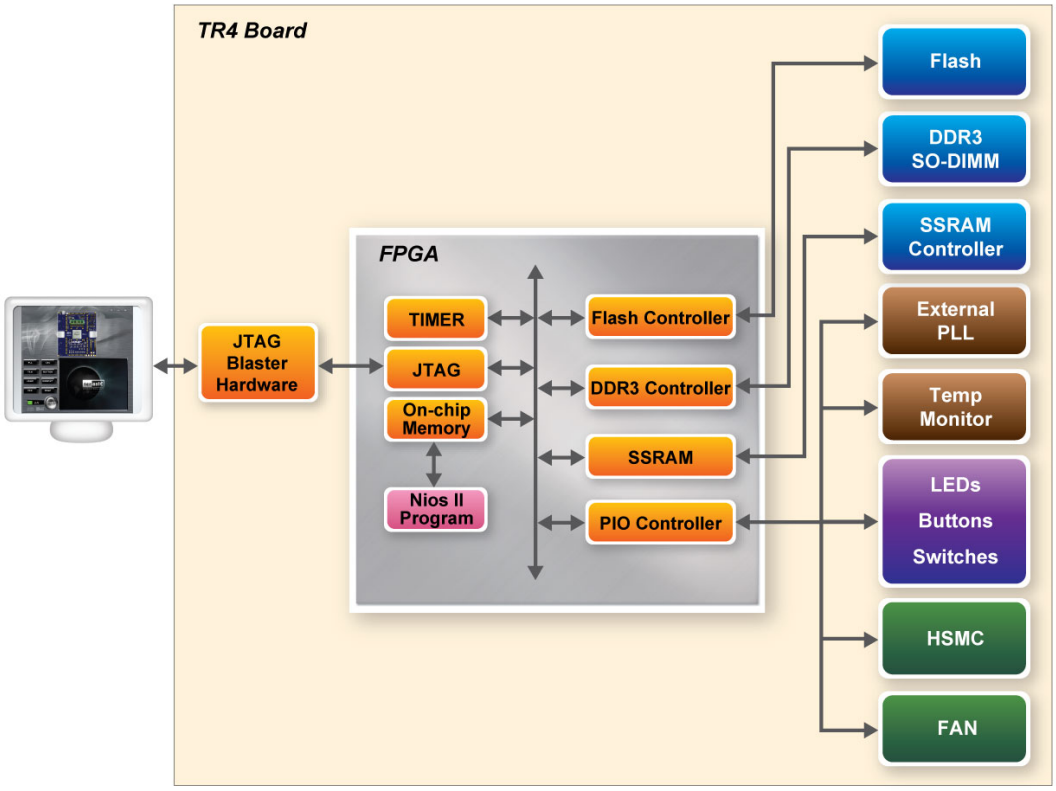
Note: If Nios II software is not incorporated in your design project, step b. of converting the .elf to flash is not required.

5.4 Using the Default Flash Loader

If you have the necessary **.flash** files, you can use the Default Flash Loader to reprogram the flash memory

Default Flash Loader

The purpose of the Default Flash Loader is to establish communication with Nios II through JTAG to program the flash memory. The block diagram of the Default Flash Loader is depicted below:



The Default Flash Loader is located in the TR4 System CD under the directory tr4_ default_flash_loader. Using the Default Flash Loader the .flash file can be programmed onto the flash memory. The flash base address is 0x08000000.

Programming Flash Memory Using the Nios II EDS

The following .flash files are created once the conversion is complete:
<your_file>_hw.flash → hardware image file
<your_file >_hw.map.flash → PFL option bit information file
<your_file >_sw.flash → software image file

The Nios II EDS offers a nios2-flash-programmer utility to program the flash memory directly. To program the **.flash** files or any compatible S-Record File (**.srec**) to the board using nios2-flash-programmer, perform the following steps:

1. Open Quartus II software and launch the Quartus II Programmer (Tools > Programmer) to configure the FPGA with a .sof capable of flash programming
2. Click **Add File** and select <CD-ROM_dir>\demonstrations\<TR4_<Stratix device>\ tr4_default_flash_loader \ tr4_default_flash_loader.sof
3. Turn on the Program/Configure option for the added file.
4. Click **Start** to download the selected configuration file to the FPGA. Configuration is complete when the progress bar reaches 100%.
5. On the Windows Start menu, click **All Programs > Altera > Nios II EDS > Nios II Command Shell.**
6. In the Nios II command shell, navigate to the work directory (or to the directory of the .flash files you created) and type the following Nios II EDS command:
   nios2-flash-programmer --base=0x08000000 <your_file>_hw.flash
7. From the <your_design>_hw.map.flash file, insert "S21501808003FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF6" to the last line and save the file.
8. Type the following Nios II EDS command:
   nios2-flash-programmer --base=0x08000000 <your_file>_hw.map.flash
9. After programming completes, if you have a software file to program, type the following Nios II EDS command:
   nios2-flash-programmer --base=0x0A000000 <your_file>_sw.flash

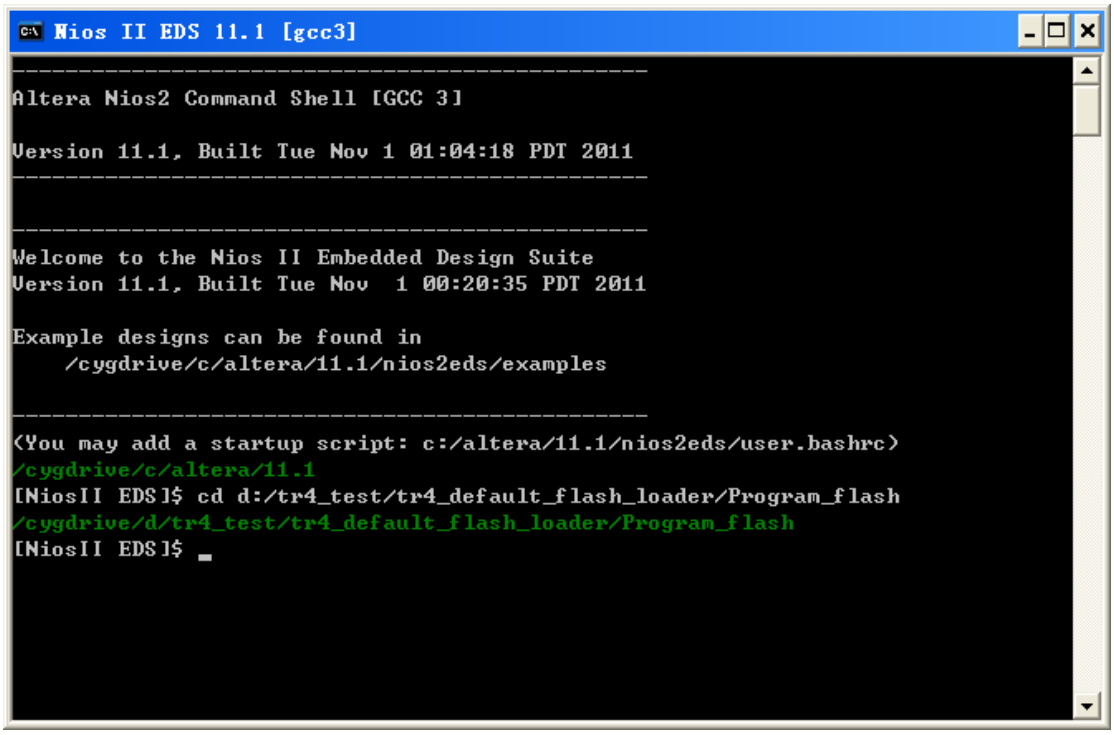
Programming the flash is now complete.

5.5 Programming Flash Device Example

In this example, we've created a project folder 'tr4_test/tr4_default_flash_loader/Program_flash' which contains the following files tr4.sof and tr4.elf.

Note. The names of the .sof and .elf files may be different from the ones you've generated from Quartus II and Nios II software.

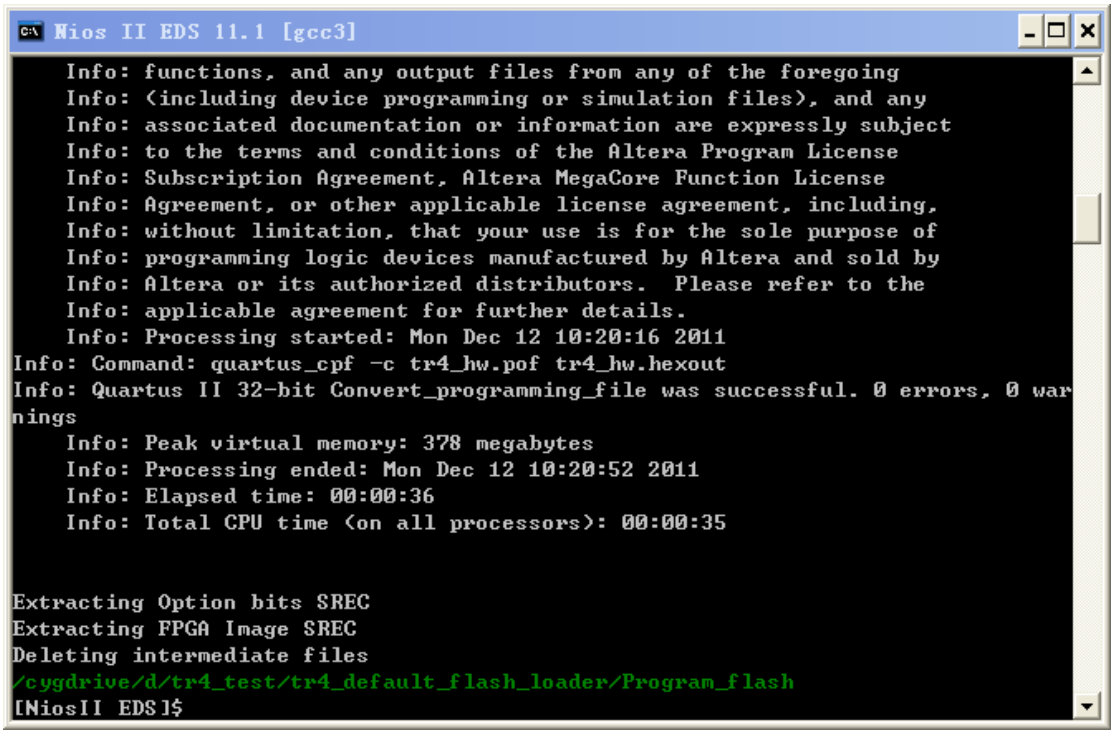
1. Open Nios II EDS Command Shell (On the Windows Start menu, click **All Programs > Altera > Nios II EDS > Nios II Command Shell**), and go to directory of your project.



2. Enter the following below to convert the tr4.sof into .flash:

sof2flash --input= tr4_default_flash_loader.sof --output=tr4_hw.flash --offset=0x00020000 --pfl --optionbit=0x18000 --programmingmode=FPP

Conversion is complete.

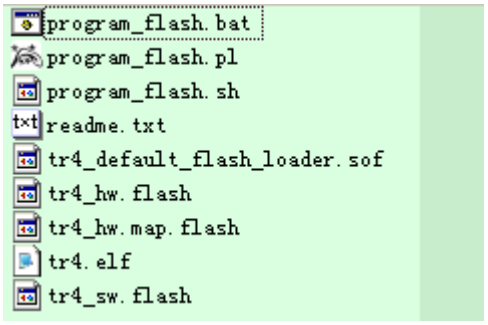


3. Enter following to convert the tr4.elf into .flash:

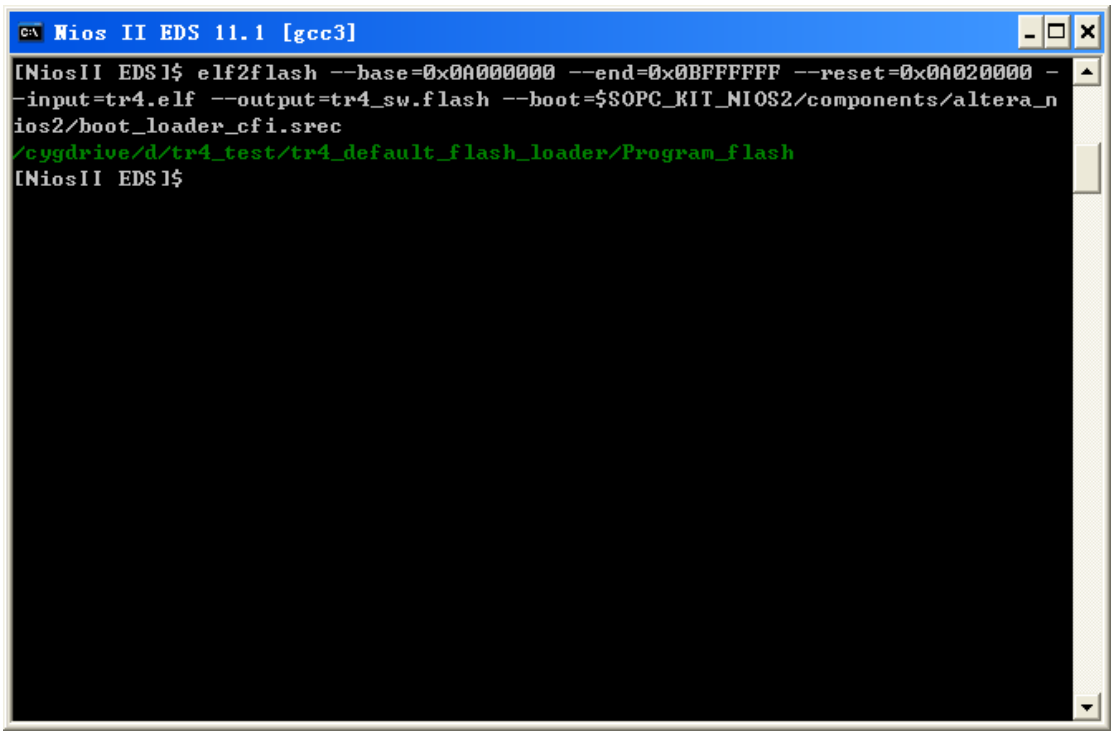
elf2flash --base=0x0A000000 --end=0x0BFFFFFF --reset=0x0A020000 --input=tr4.elf --output=tr4_sw.flash --boot=$SOPC_KIT_NIOS2/components/altera_nios2/boot_loader_cfi.srec

Note. If the Nios II software is not incorporated in your design project, converting the .elf to flash is not required.

After conversion is complete, the following .flash files are created below:



4. Next, we are ready to program the .flash files onto the flash memory.

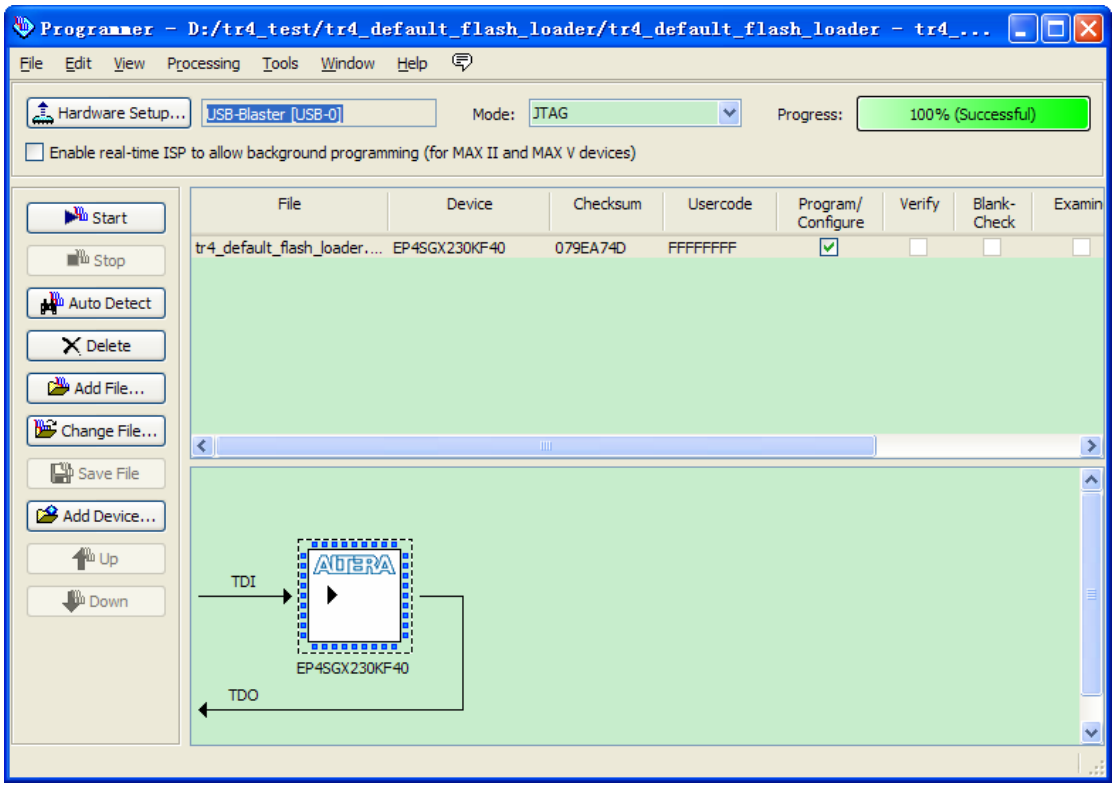


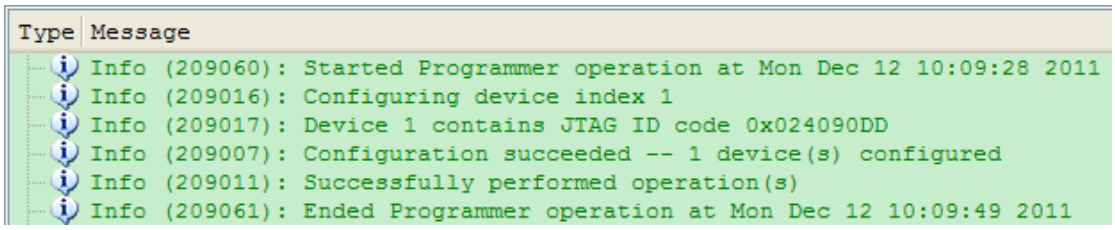
a. Launch the Quartus II Programmer to configure the FPGA with a .sof capable of flash programming.

b. Click **Add File** and select <CD-ROM_dir>\demonstrations\tr4_<Stratix device> tr4_default_flash_loader\ tr4_default_flash_loader.sof

c. Turn on the Program/Configure option for the added file.

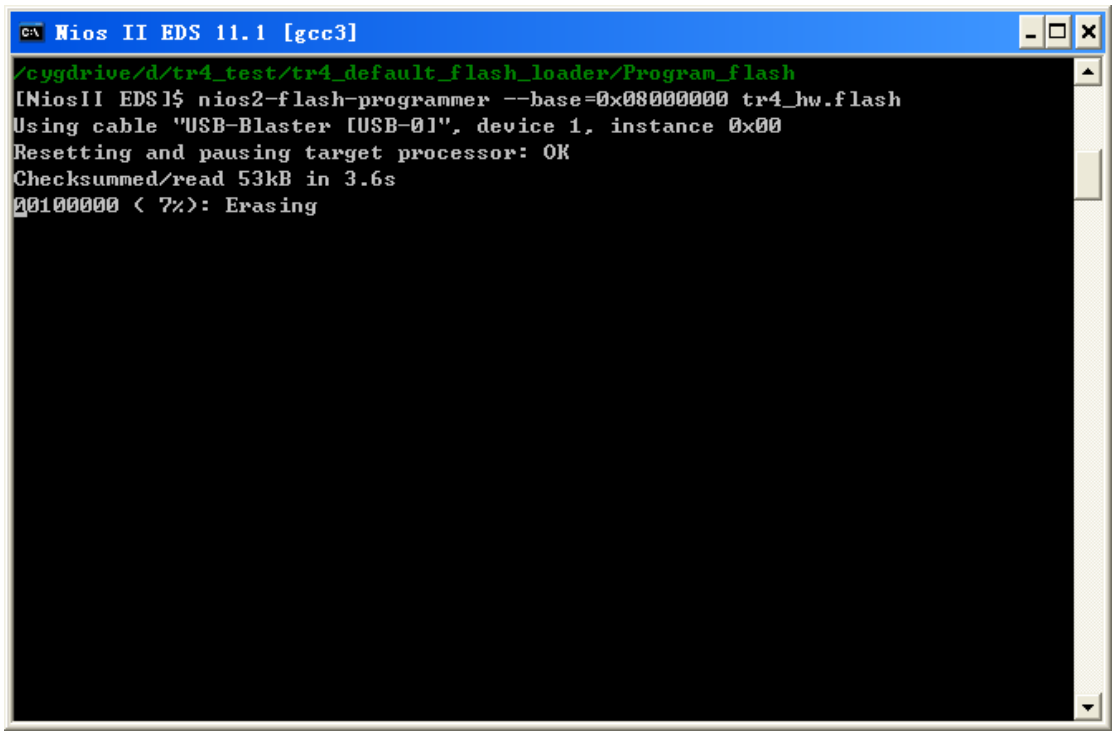
d. Click **Start** to download the selected configuration file to the FPGA. Configuration is complete when the progress bar reaches 100%.

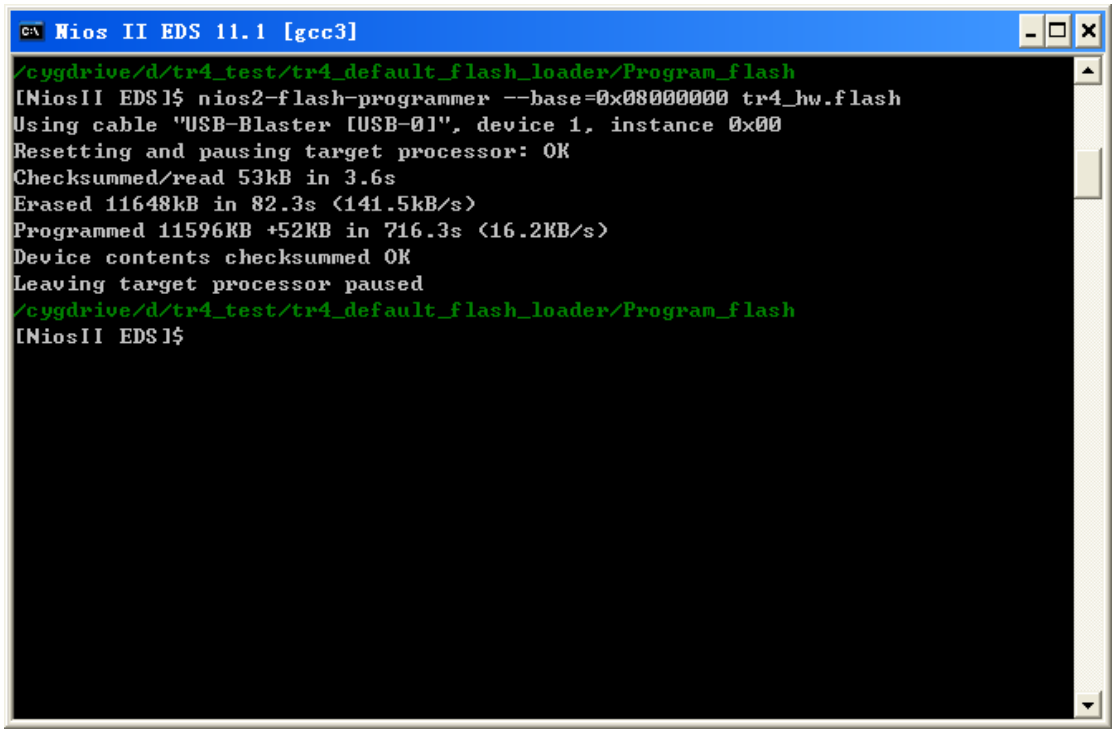




e. On the Windows Start menu, click **All Programs > Altera > Nios II EDS > Nios II Command Shell.**

f. In the Nios II command shell, navigate to the work directory (or to the directory of the .flash files you created) and type the following Nios II EDS command:
nios2-flash-programmer --base=0x08000000 tr4_hw.flash





g. From the tr4_hw.map.flash file, insert the following to the last line S21501808003FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF6, and save.

```
S325000180002000740BFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFD6
S32500018020FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF59
S32500018040FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF39
S32500018060FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF19
S21501808003FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF6
```

h. Type the following Nios II EDS command:

nios2-flash-programmer --base=0x08000000 tr4_hw.map.flash

```
Nios II EDS 11.1 [gcc3]
/cygdrive/d/tr4_test/tr4_default_flash_loader/Program_flash
[NiosII EDS]$ nios2-flash-programmer --base=0x08000000 tr4_hw.map.flash
Using cable "USB-Blaster [USB-0]", device 1, instance 0x00
Resetting and pausing target processor: OK
Checksummed/read 1kB in 0.0s
Erase not required
Programmed 1KB in 0.0s
No change to device contents
Leaving target processor paused
/cygdrive/d/tr4_test/tr4_default_flash_loader/Program_flash
[NiosII EDS]$
```

i. After programming completes, if you have a software file to program, type the following Nios II EDS command:
nios2-flash-programmer --base=0x0A000000 tr4_sw.flash.

```
[NiosII EDS]$ nios2-flash-programmer --base=0x0A000000 tr4_sw.flash
Using cable "USB-Blaster [USB-0]", device 1, instance 0x00
Resetting and pausing target processor: OK
Checksums took 0.0s
Erase not required
Programmed 346KB in 19.3s (17.9KB/s)
Device contents checksummed OK
Leaving target processor paused
```

Programming the flash is now complete.

5.6 Programming Flash Memory using Program_flash.bat

The TR4 provides a program_flash.bat batch file to limit the steps that are taken when users program the flash memory on the TR4.

Software Requirements:
1. Quartus II 11.0 or later
2. Nios II IDE tools 11.0 or later

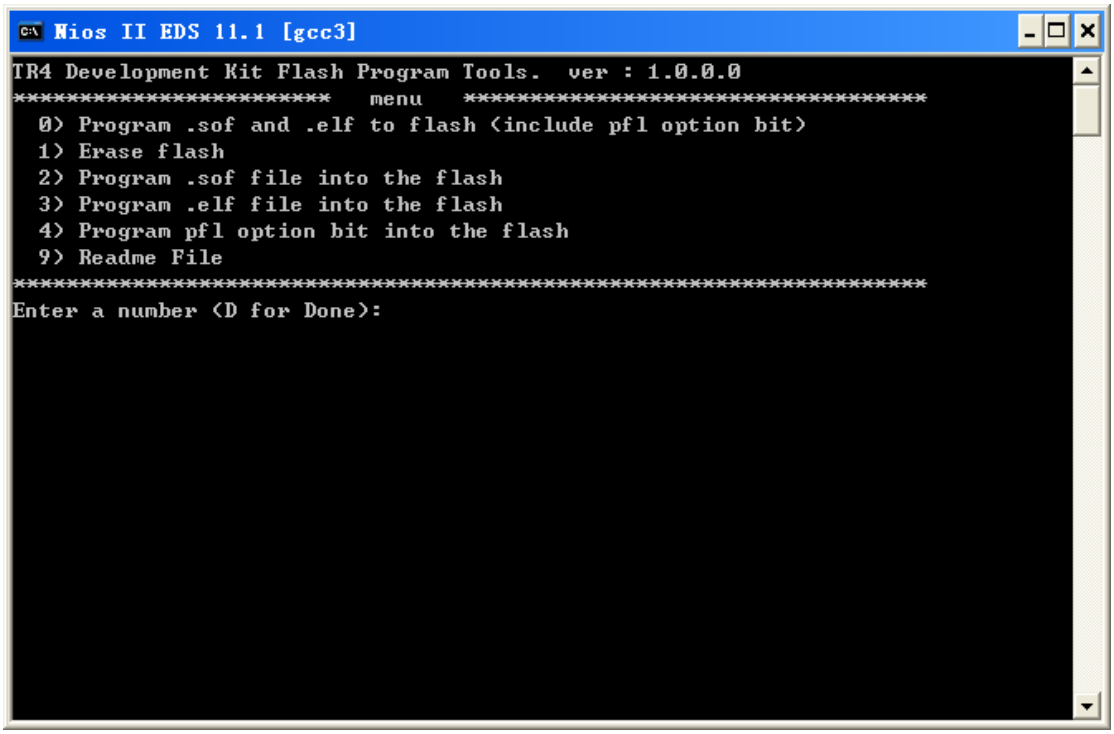
Program_flash folder contents (<CD-ROM_dir>\demonstrations\TR4_<Stratix device>\TR4_Default_Flash_Loader\ Program_flash\):

1. program_flash.bat
2. program_flash.pl
3. program_flash.sh
4. tr4_default_flash_loader.sof

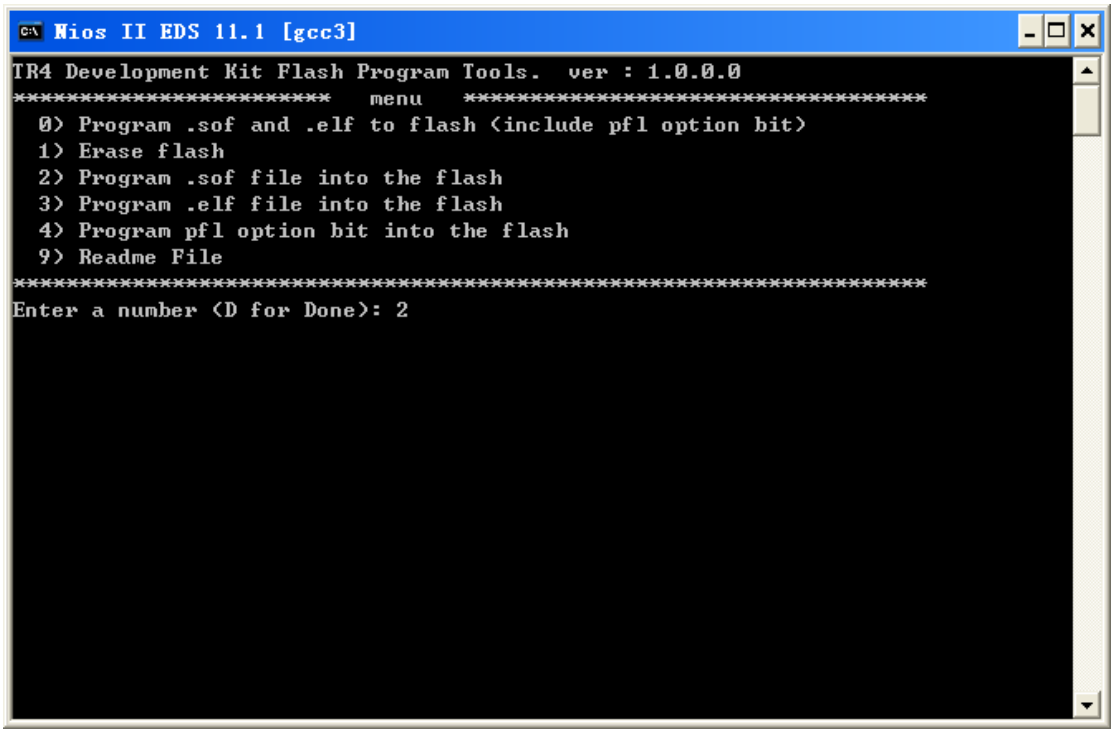
Before you use the program_flash.bat batch file to program the flash memory, make sure the TR4 is turned on and USB cable is connected to the USB blaster port (J4). In addition, place the .sof and .elf file you wish to program/convert in the Program_flash directory.

Programming Flash memory with .sof using Program_flash.bat

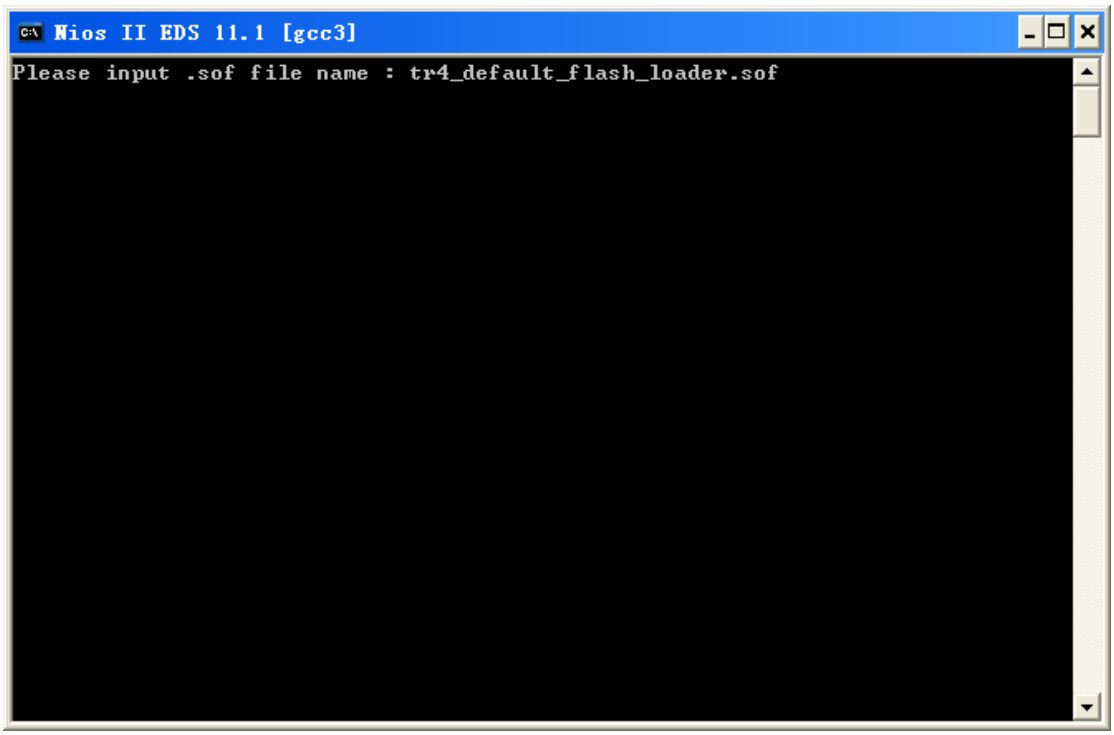
1. Launch the program_flash.bat batch file.
2. The flash program tool shows the menu options.



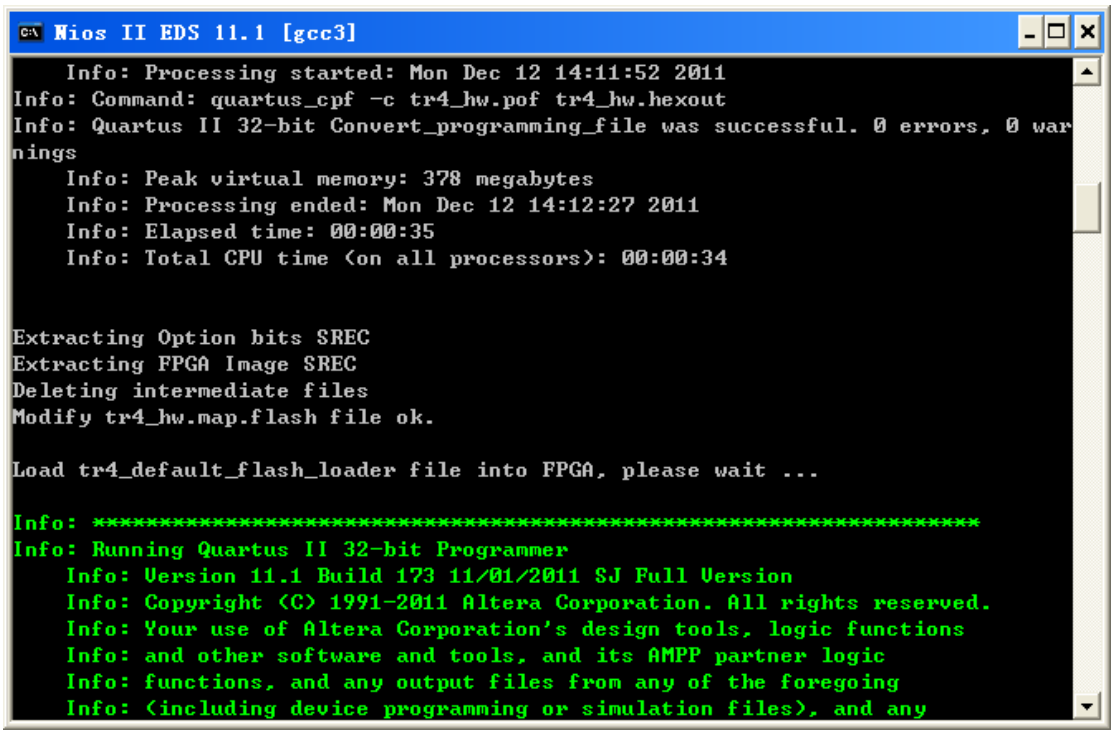
3. Select option 2.



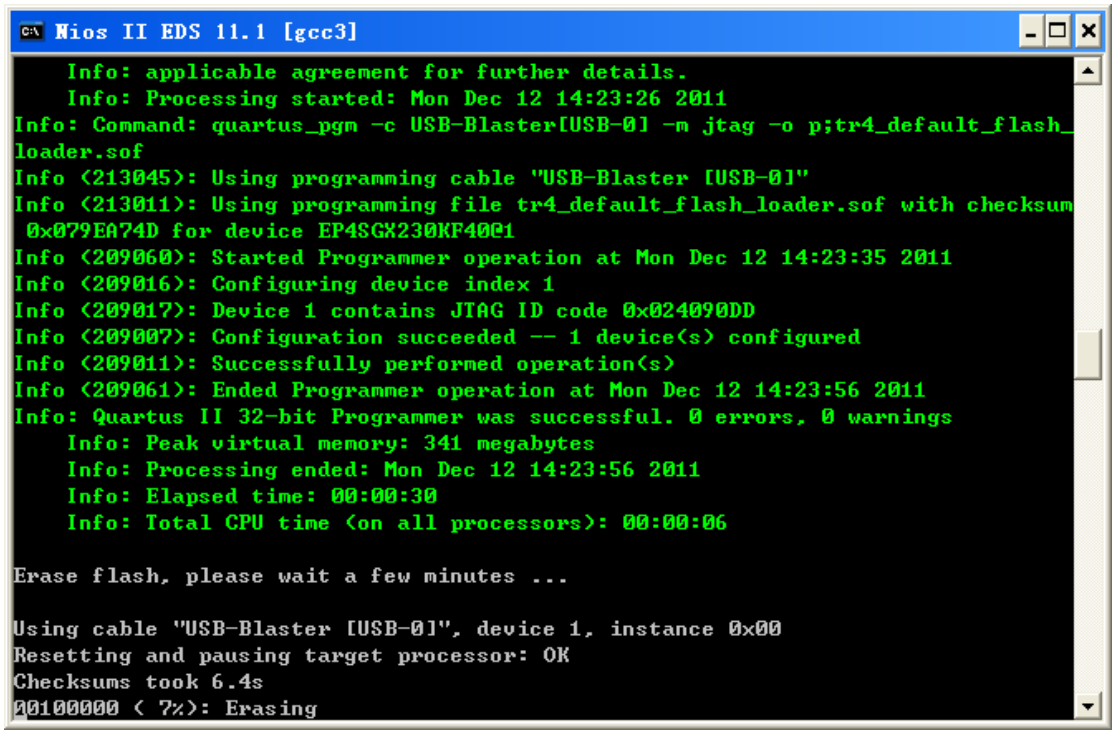
4. Enter the .sof file name to be programmed onto the flash.



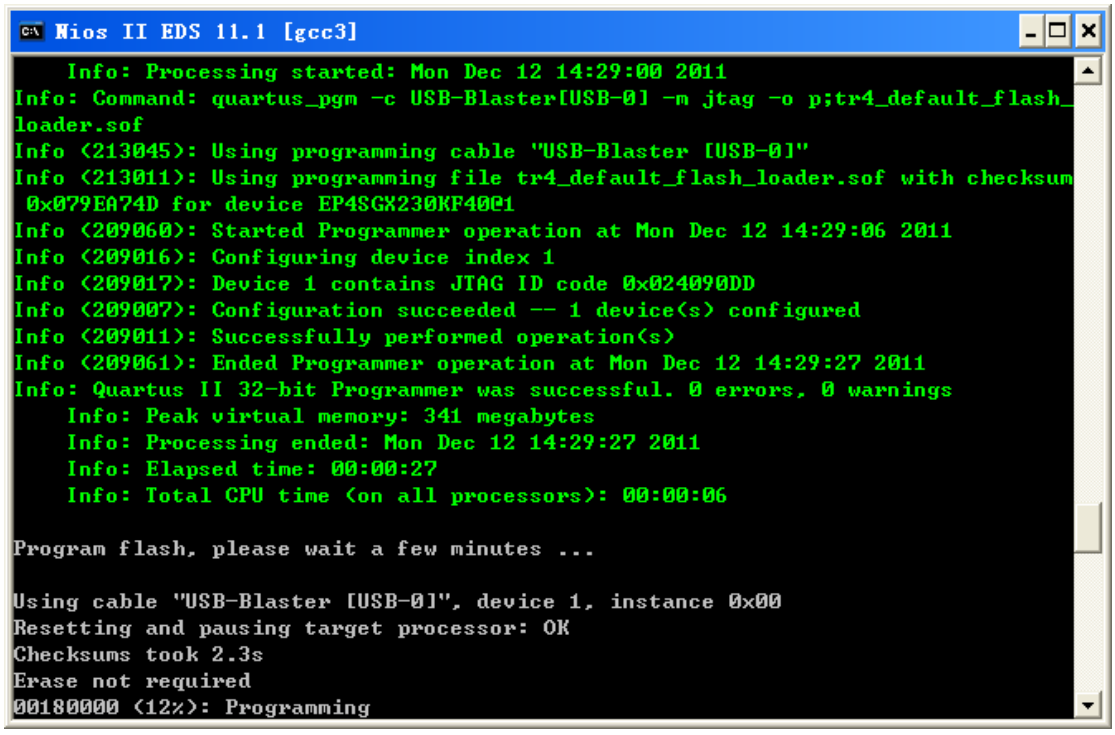
5. The following lines will appear during flash programming: ‘Extracting Option bits SREC’, ‘Extracting FPGA Image SREC’, and ‘Deleting intermediate files’. If these lines don’t appear on the windows command, programming on the Flash memory is not successfully setup. Please make sure Quartus II 11.0 and Nios II 11.0 IDE or later is used.



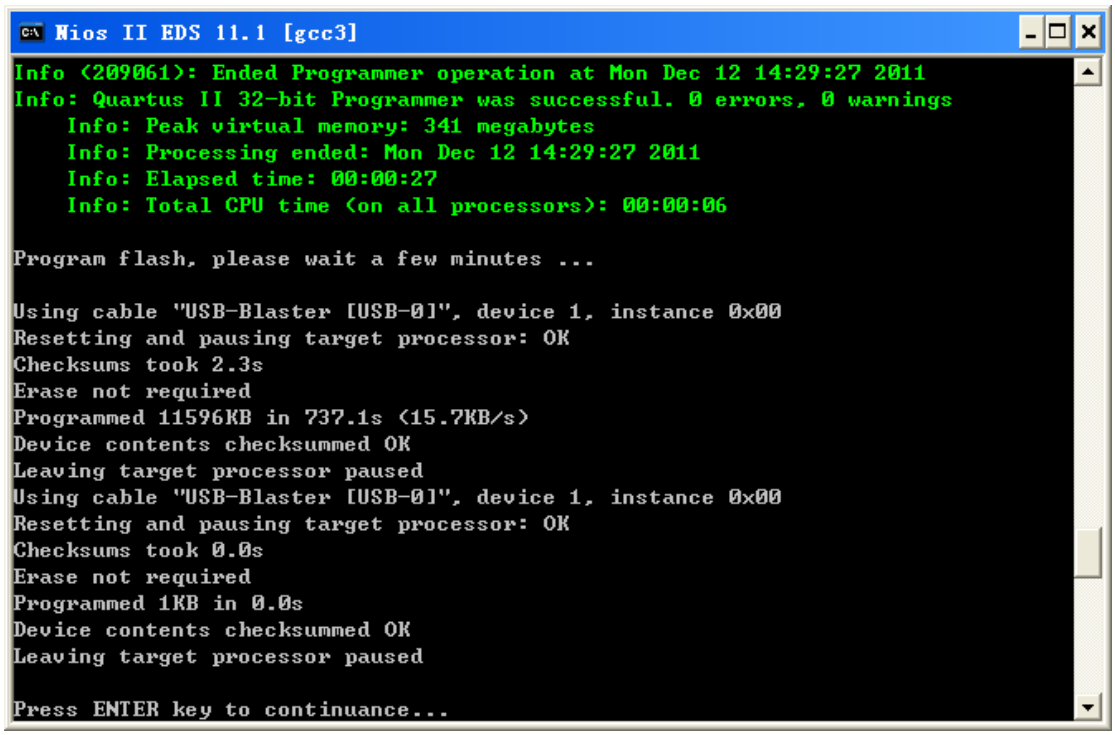
6. Erasing flash.



7. Programming Flash.



8. Programming complete.



Additional Information

Revision History

Version	*Change Log*
V1.0	**Initial Version (Preliminary)**
V1.1	**Remove Quartus DVD description**
V1.2	**Update CH5.6 Program_flash folder contents**