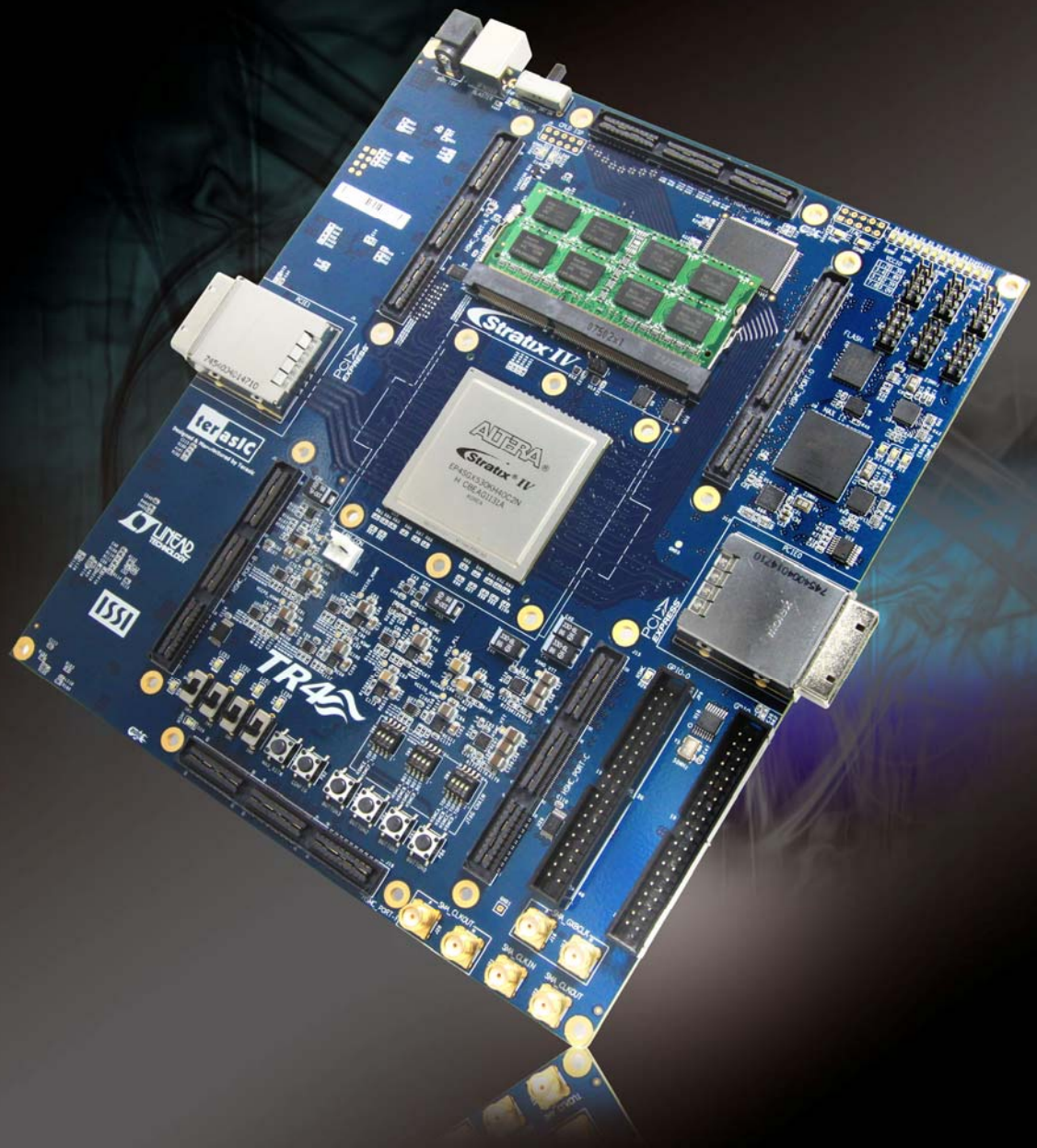
TR4

FPGA Development Kit

Using Multi-TR4 Systems



CONTENTS

Chapter 1

About this Guide

This document describes how to link and operate multiple TR4 development systems.

1.1 Introduction

The TR4 FPGA Development Platform provides 6 High Speed Mezzanine Card (HSMC) ports, made up of 6 female connectors on the top, and four male connectors on the bottom. HSMC ports allow extensibility for designs and functions, and if user requirements for LEs or I/O increase, the HSMC ports also allow the stacking of multiple systems to create a multi-FPGA development platform.

There are three ways to link multiple TR4 systems together.

The first is to connect two TR4s together is through vertical stacking, as shown in Figure 1-1 and Figure 1-2. This form of stacking connects the HSMC ports of the TR4s together via an extension adapter to add height, thus enabling stacking. The benefits of stacking include compact size and JTAG chaining between boards for simultaneous FPGA configuration.

The second method of linking two TR4s together is through an HSMC cable shown in Figure 1-3, which is a viable solution where there are no stringent space requirements.

The third method is to link two TR4s together with a PCIe cable, shown in Figure 1-4, which utilizes the transceivers and Megacore IP to establish communication.

The above three methods for connecting TR4 boards together will be described in detail in the following chapters.

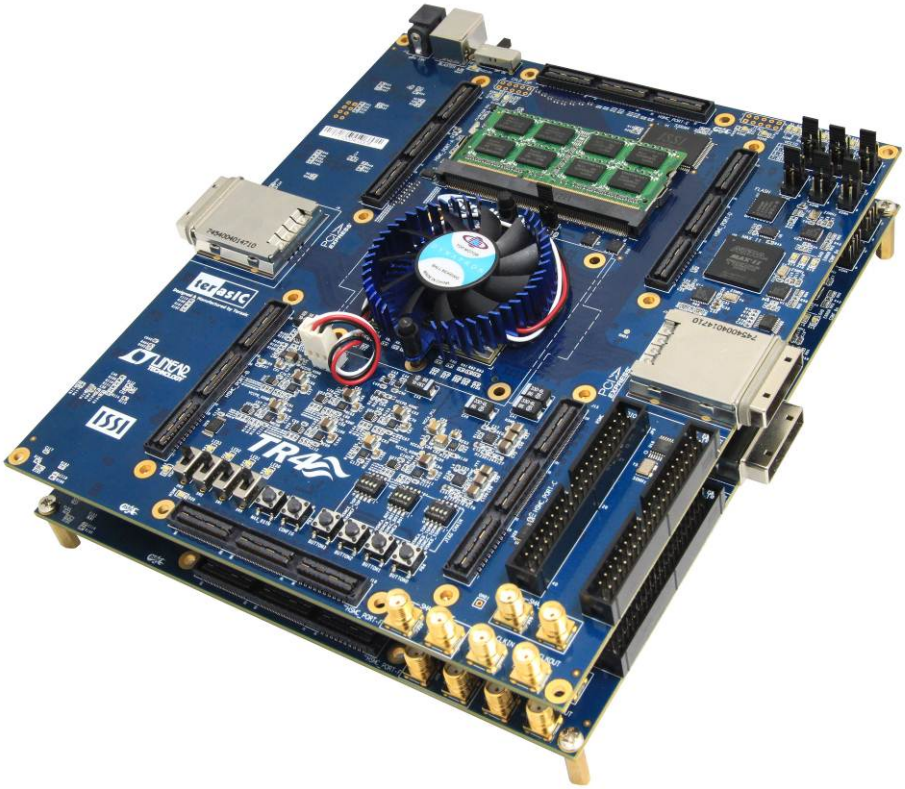


Figure 1-1 TR4 Vertical Stacking

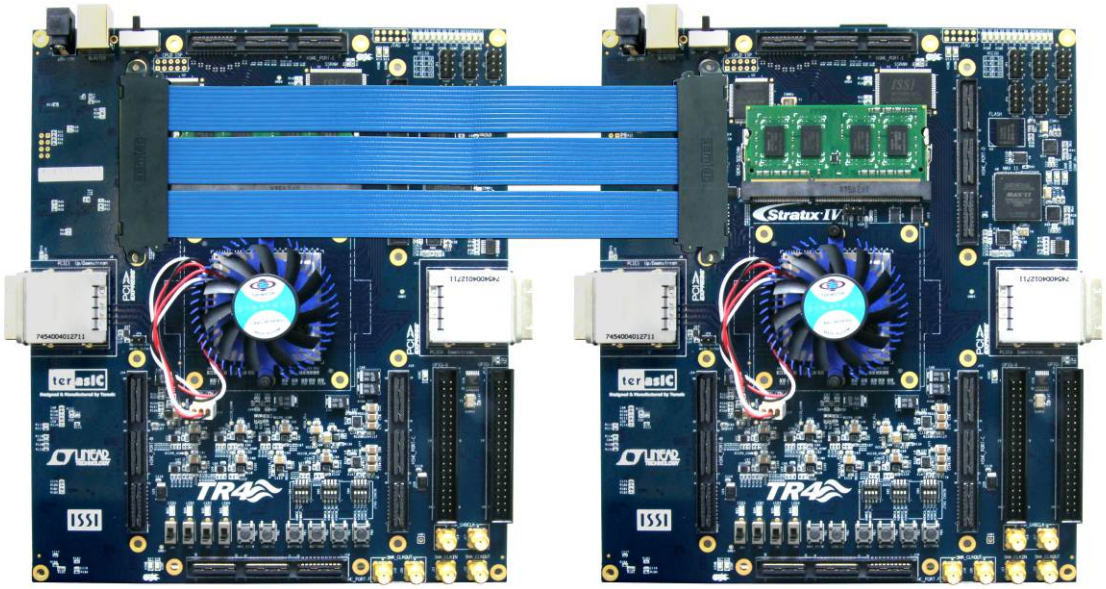


Figure 1-2 TR4 Linking via HSMC

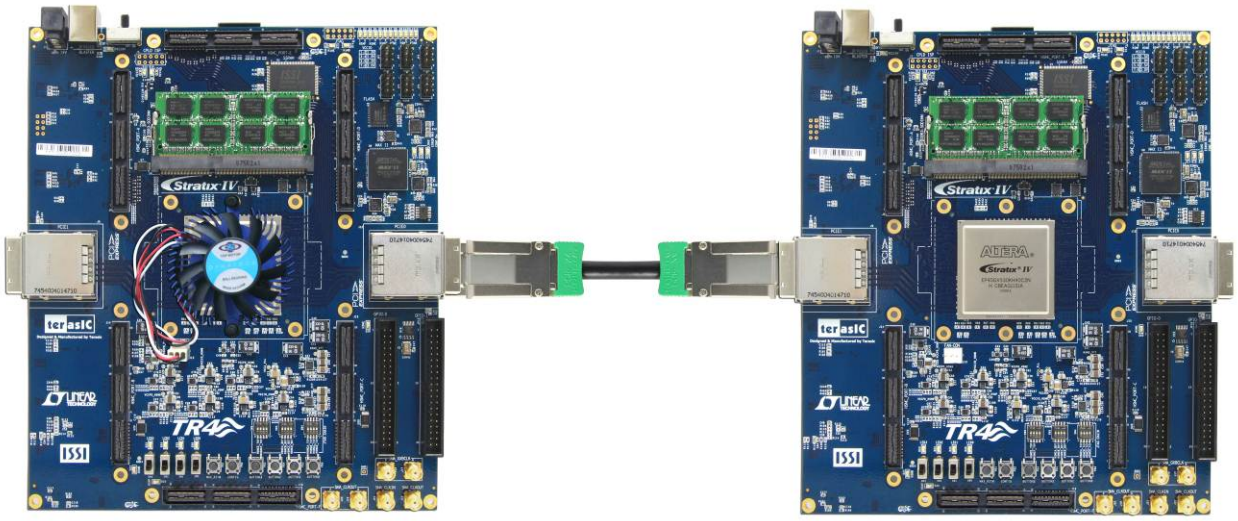


Figure 1-3 TR4 Linking via PCIe Cable

Chapter 2

Vertical Stacking

2.1 Requirements

If two TR4s are to be stacked together, an HSMC adapter card must be used. Presently, the HMF3C and HMF3D HSMC adapters are compatible for stacking. These adapters add the necessary height required to mount one TR4 on top of another.

The HMF3C not only serves the purpose of connecting two TR4 systems together,,as is shown in Figure 2-1,but also enables signaling between the boards by crisscrossing connections of the TX and RX signals as shown in Figure 2-2. This allows two FPGAs to engage in single-ended transmission as well as differential I/O data transfer. For more details on HMF3C I/O, please refer to the TR4 System CD's HMF3C schematic at CD\Schematic\HSMC_Adapter_Card.

Figure 2-1 HMF3C Adapter

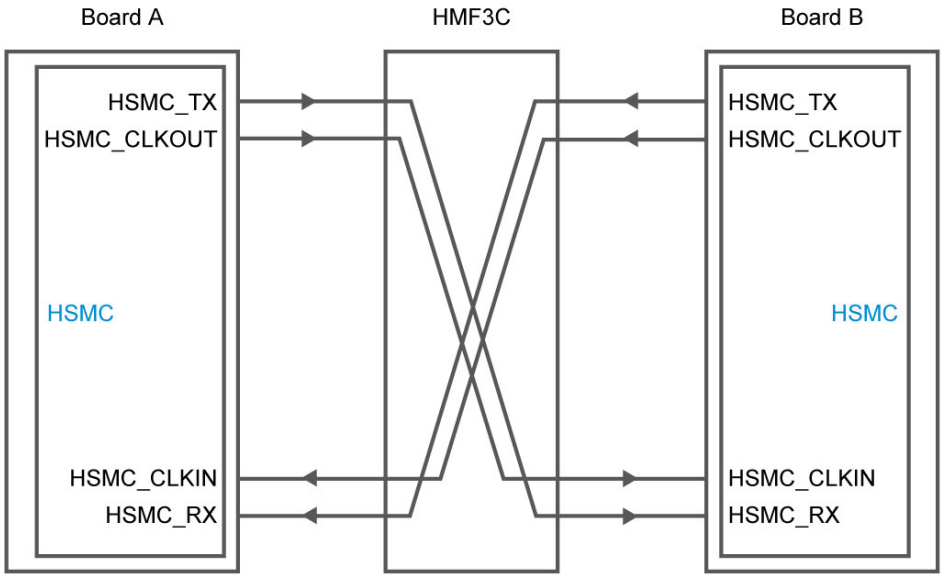


Figure 2-2 HMF3C Architecture Diagram

If signaling between the two boards on an HSMC port is not required, the HMF3D can be used, shown in Figure 2-3. The block diagram can be seen in Figure 2-4, which shows that if this adapter is used, the HSMC TX and RX pins will not cross to connect with their respective input pins.

Figure 2-3 HMF3D Adapter

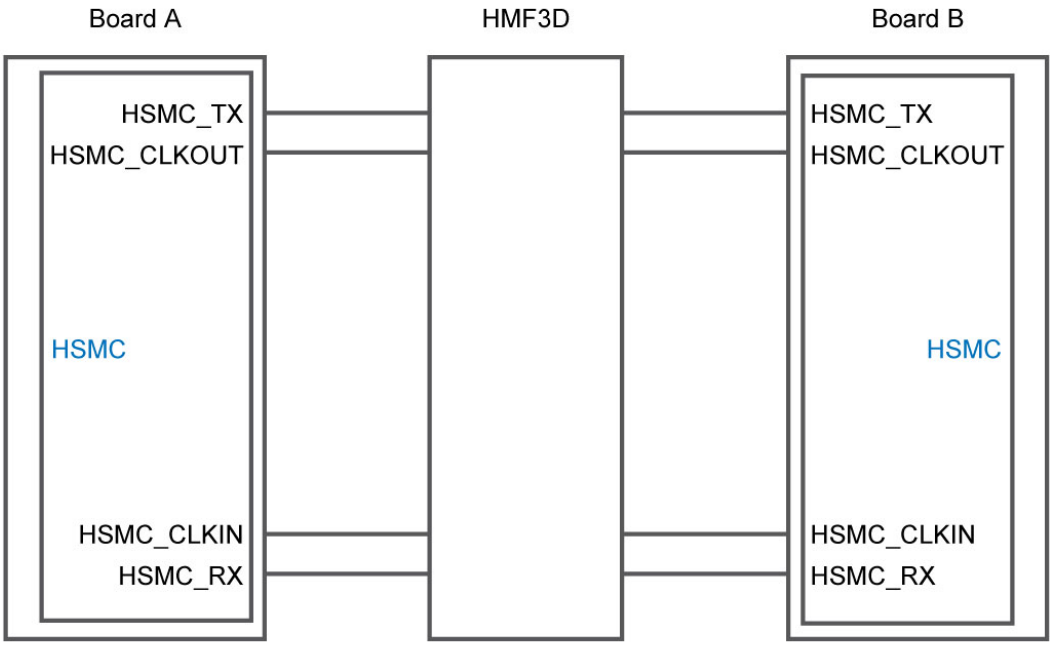


Figure 2-4 HMF3D Block Diagram

2.2 Setup Details

This section describes an example of using 3 HMF3C adapters and 1 HMF3D adapter to connect two TR4 systems together. Setup details and notes are described below.

1. When stacking two boards in this fashion, users can choose to apply power to one board or two via power adapter. When only one TR4 is connected to a power adapter, the second TR4 can be powered via HSMC ports. The TR4 serving as a power source will require the backside 12V and 3V HSMC fuses to be inserted. Please make sure there are at least 3 HMF3C adapters between the two TR4s to ensure enough power is provided to the secondary TR4. If each TR4 will be independently powered with a power adapter, the 12V and 3.3V fuses can be removed. In this example, the boards will be independently powered via power adapter, and the back-side fuses shall be removed.

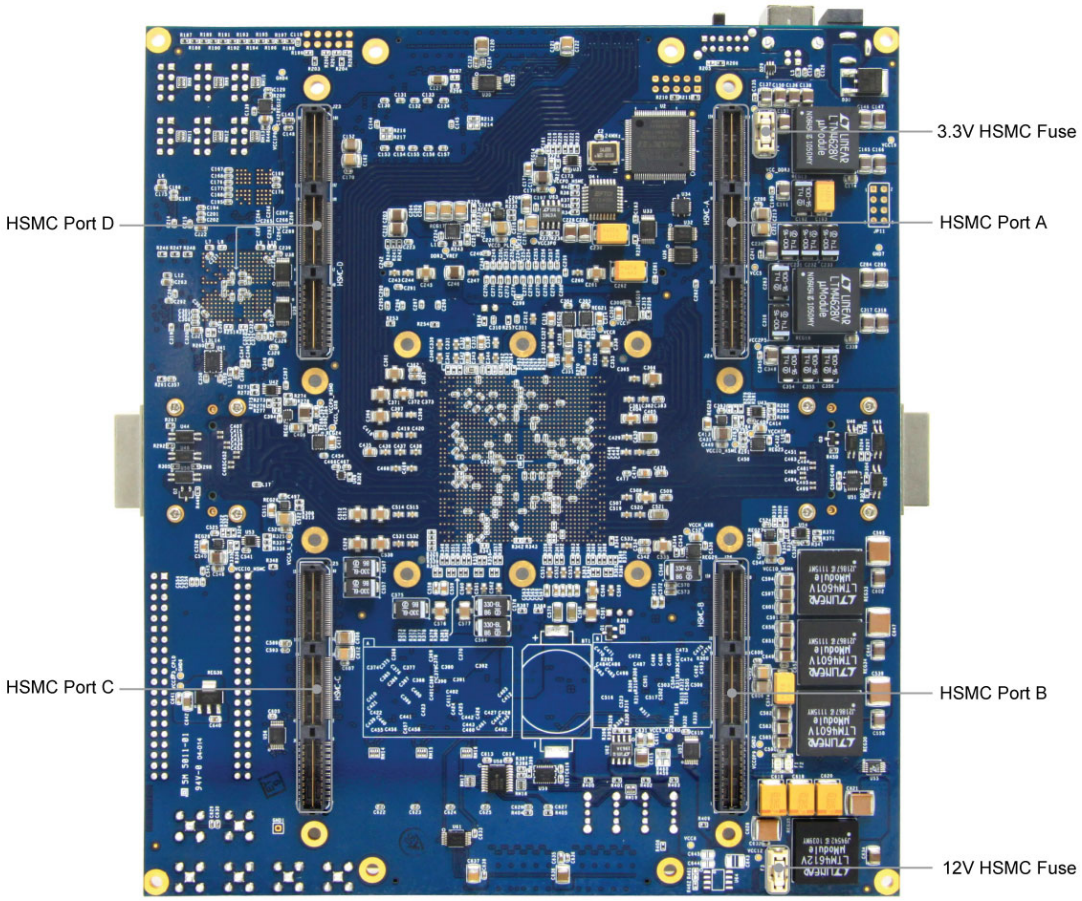


Figure 2-5 HSMC Power Source Fuses

Make sure that every TR4 HSMC VCCIO voltage settings are the same. In Figure 2-6, we have set HSMC Port A ~D (JP1~JP6) to all be 2.5V. Different settings for the I/O standards between TR4 boards might result in abnormal behavior.

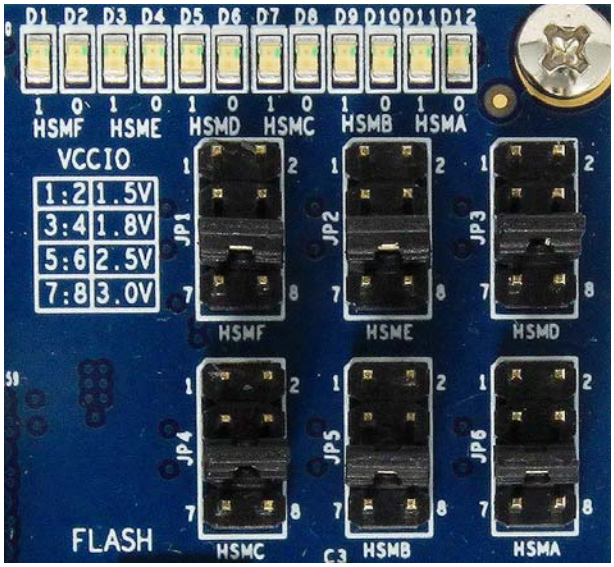


Figure 2-6 JP1-JP6 I/O Standard Settings

2. Making sure no power is currently applied to the board, we connect the two TR4 boards together, with HMF3C on HSMC ports A, B, and C. The HMF3D will be on HSMC Port D.

3. We connect both TR4s to the power adapter and a USB cable to the upper TR4 J4 port, and turn on both boards.

Chapter 3

HSMC Cable Connection

Besides stacking with adapter cards, multiple TR4s can be connected together with HSMC cables. Setup details are provided below.

3.1 Requirements

Two TR4 boards can connected horizontally to conduct data transfer with an HSMC High Speed Cable shown in Figure 3-1. The HSMC cable serves the same function as the HMF3C, which crisscrosses the signals to match the TX and RX of the respective HSMC ports, allowing for not only single-ended transmission, but also differential signaling.

For more information about the HSMC High Speed Cable, please refer to this link:
http://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=77&No=598

Figure 3-1 HSMC High Speed Cable

3.2 Setup Details

1. Determine the HSMC ports you would like to connect, and connect both to the ends of the HSMC cable. In figure 3-2, HSMC ports A of both TR4s have been connected to each other via HSMC cable.

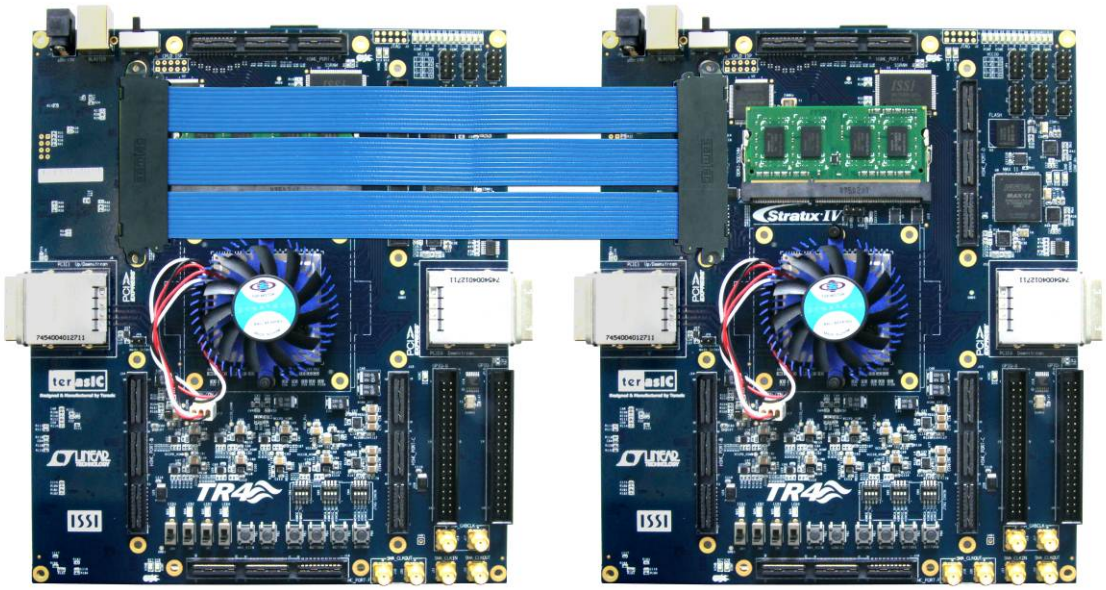


Figure 3-2 HSMC ports A connected via HSMC cable

2. Assure that both HSMC ports have the same VCCIO value. In Figure 3-3, the HSMC ports have both been set to 2.5V.

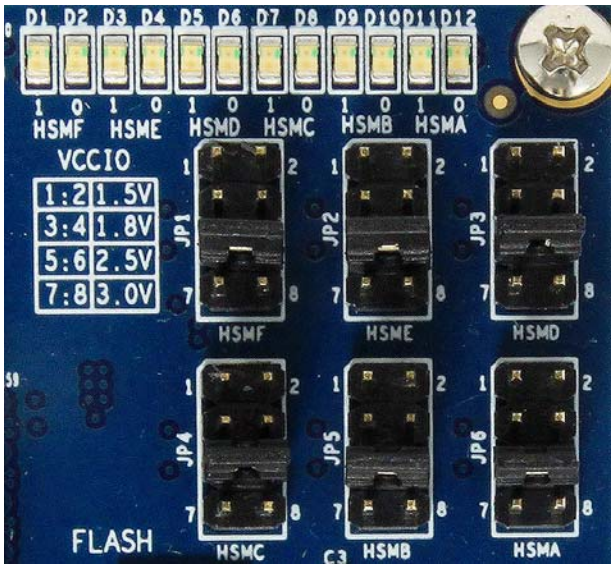


Figure 3-3 Set HSMC ports to 2.5V

3. Since the HSMC cable does not provide transmission of power, connected TR4 boards must be powered via power adapter independently.

4. The HSMC cable does not provide a JTAG signal, so assure that the JP7 jumper is not connected. Please connect the USB cable to each TR4 board to commence programming.

Chapter 4

PCIe Cable Connection

The TR4 FPGA Development System provides two PCIe connectors, which provide the functionality of connecting to a host computer, or interlinking two TR4 boards for high speed transmission. The TR4's PCIe connectors utilize 4 pairs of transceivers each for data transfer, allowing a bandwidth of 42.5 Gbps bandwidth (8.5 Gbps x 4) over a distance of one meter.

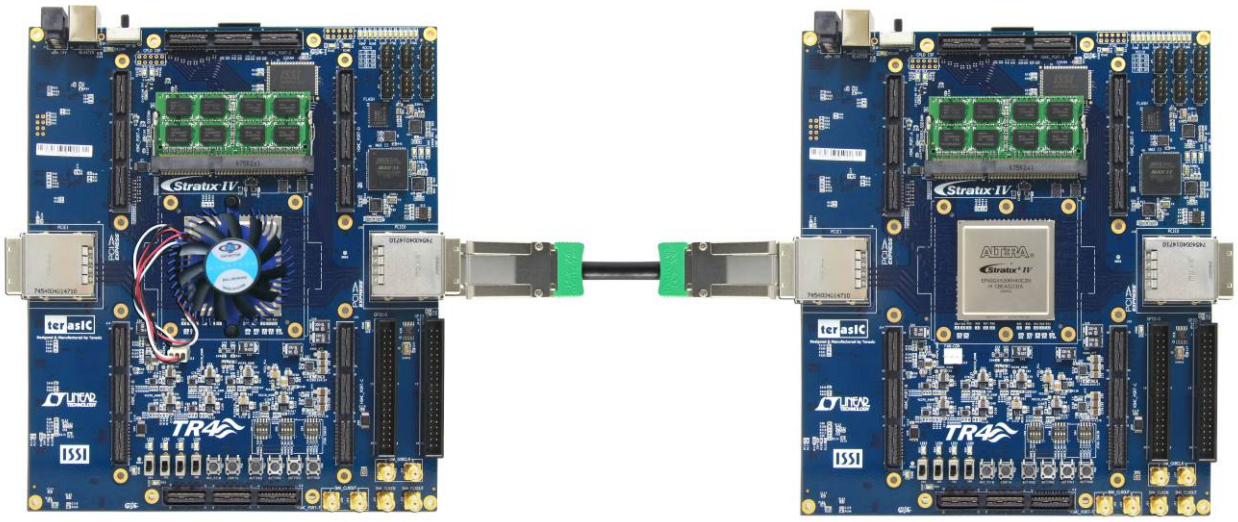


Figure 4-1 Two TR4 Boards Connected via PCIe Cable

4.1 Requirements

For more information on how to acquire a PCIe cable, please contact Terasic sales at sales@terasic.com.

Figure 4-2 PCIe Adapter Cable

4.2 Setup Details

1. Determine the PCIe connectors for linking and connect the PCIe cable to enable transmission between two TR4 boards. Figure 4-1 shows two TR4s connected through PCIe 0 port and PCIe1 port.
2. Since the PCIe cable does not provide power transmission, each TR4 board must be separately powered via power adapter.
3. The PCIe cable does not allow JTAG chaining so ensure that JP7 does not have a jumper connected to it. To commence programming, attach a USB cable to each TR4 board.
4. The IP core used to transfer data between two TR4 boards is “ALTGX”. The user can configure operation mode, base data rate, and other items as show in **Figure 4-3**.

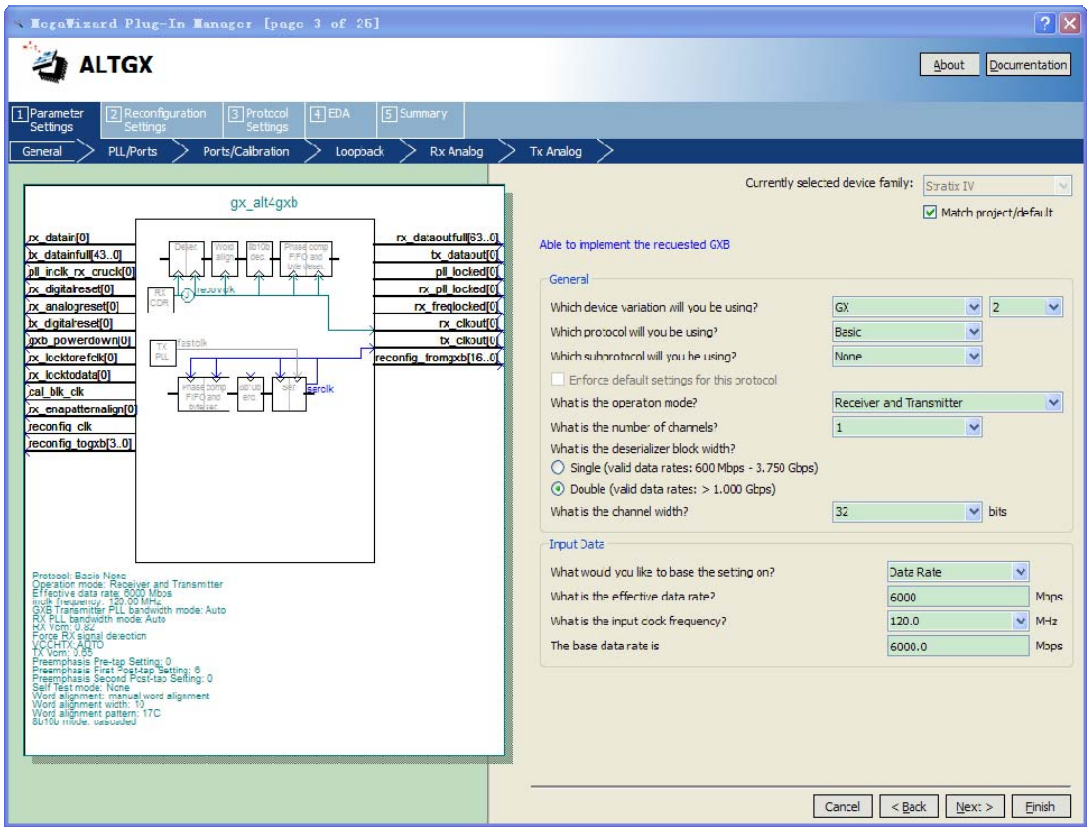


Figure 4-3 ALTGX Megacore

Additional Information

Getting Help

Here is the contact information where you can get help if you encounter problems:

- Terasic Technologies
  No. 356, Sec. 1, Fusing E. Rd.
  Jhubei City, HsinChu County, Taiwan, 302
  Email: support@terasic.com
  Web: www.terasic.com

Revision History

Date	Version	Changes
2011.12.29	First publication	