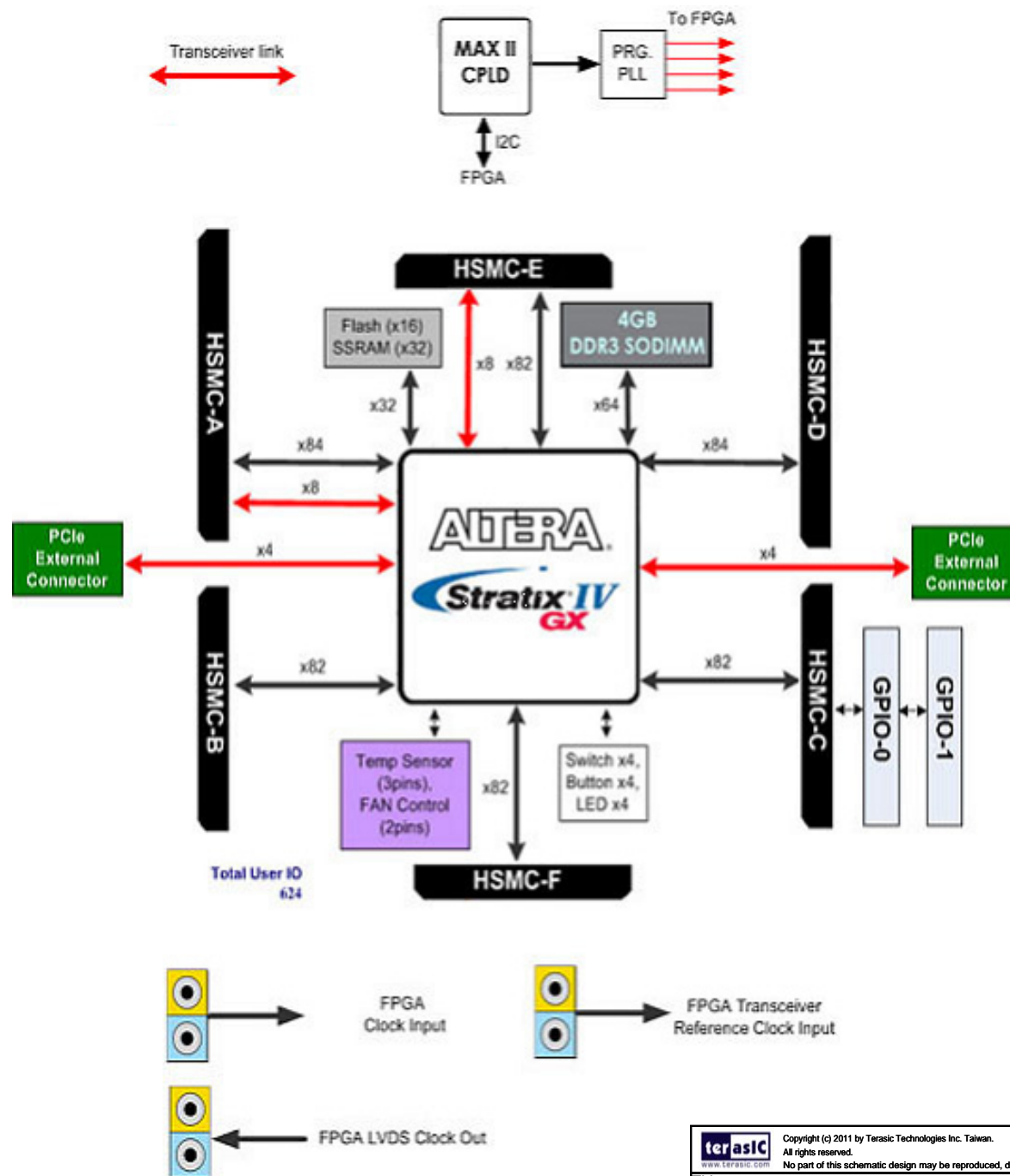

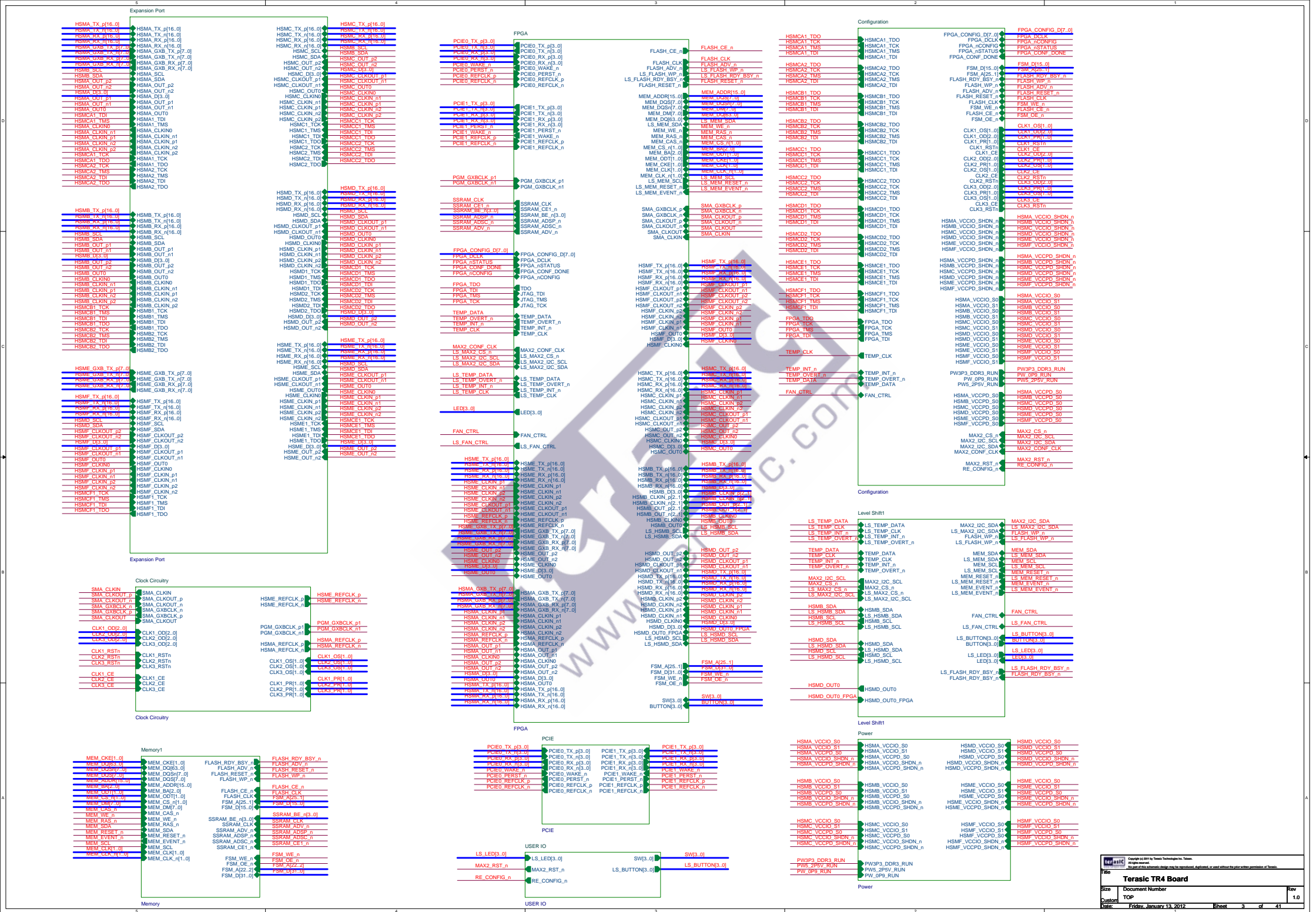


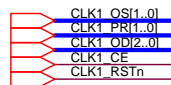
Terasic TREX Board (TR4)

SCHEMATIC	CONTENT	PAGE
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07 Memory	DDR3 SO-DIMM, Flash, SSRAM	28 ~ 30
08 PCIE	PCI Express	31
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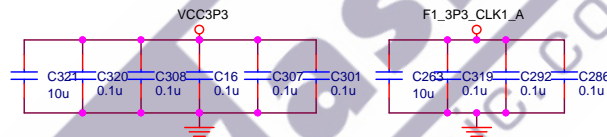
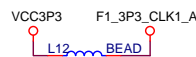
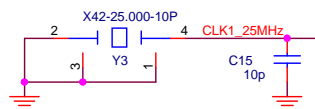
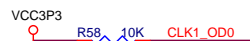
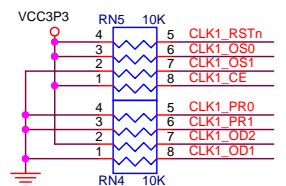


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Title		
Terasic TR4 Board		
Size	Document Number	Rev
A	Block Diagram	1.0
Date:	Friday, January 13, 2012	Sheet 2 of 41

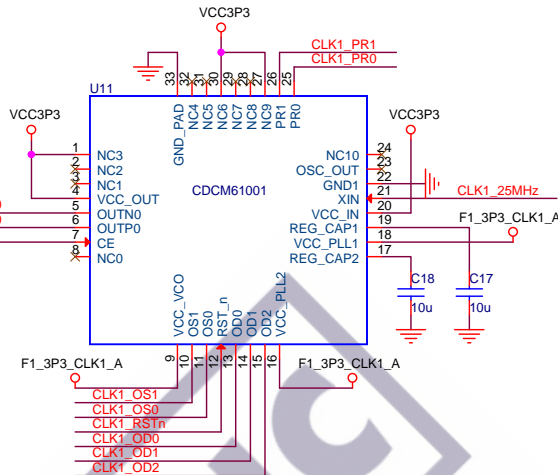




Default 100MHz



place the AC Termination near Clock Generator

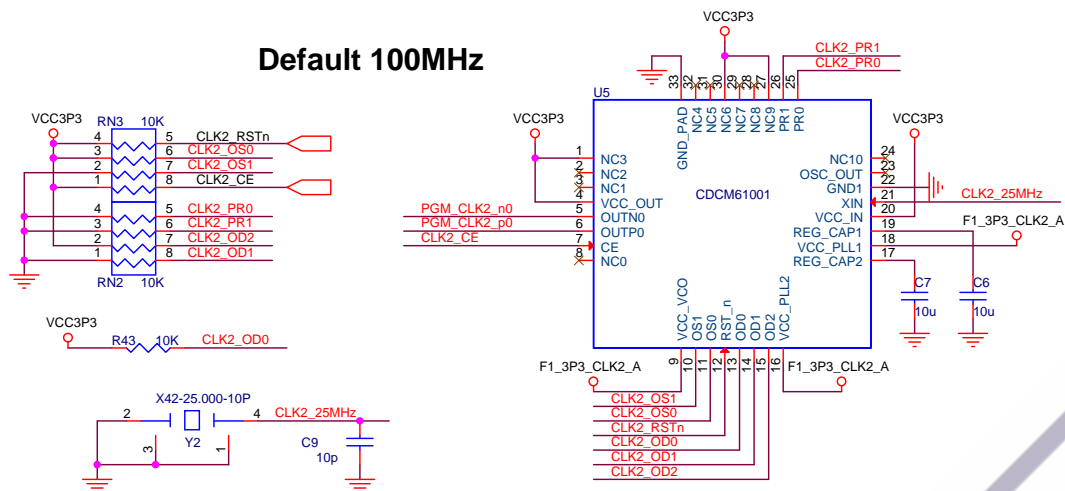


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Title	
Terasic TR4 Board	
Size	Document Number
B	Clock Generator 1
Date:	Friday, January 13, 2012
Sheet	4 of 41
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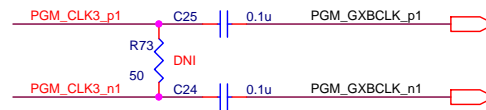
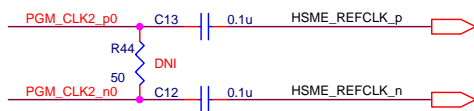
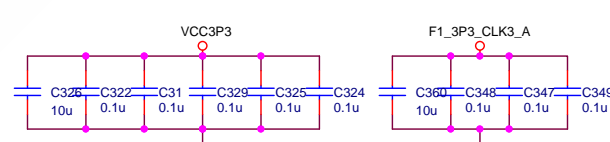
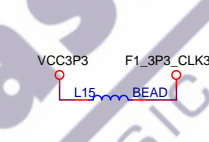
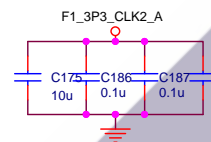
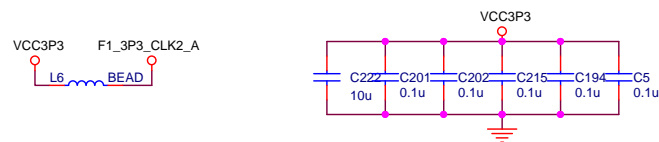
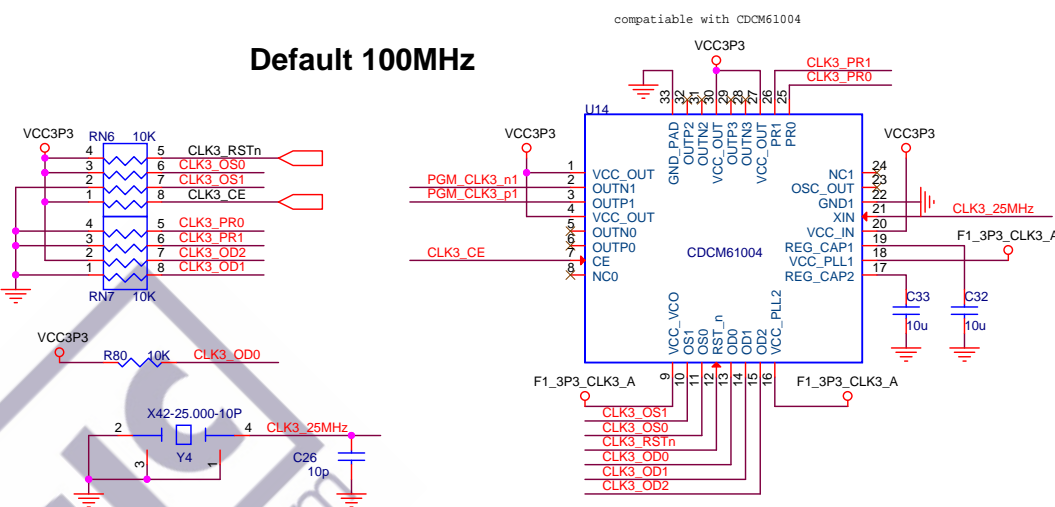
CLK2\_OS[1..0]  
CLK2\_PR[1..0]  
CLK2\_OD[2..0]

CLK3\_OS[1..0]  
CLK3\_PR[1..0]  
CLK3\_OD[2..0]

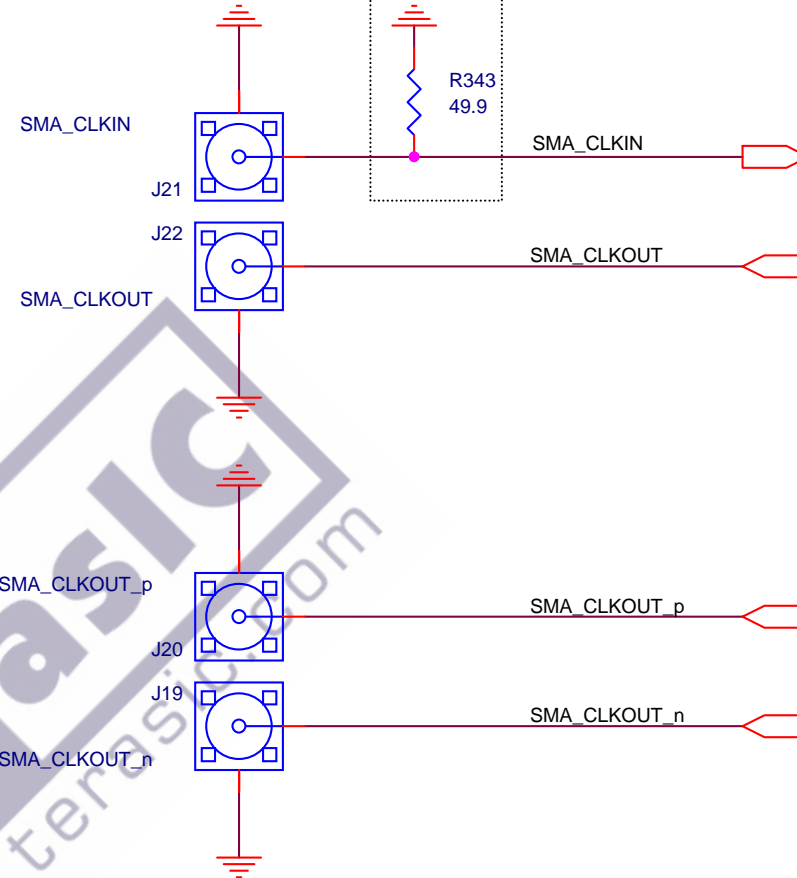
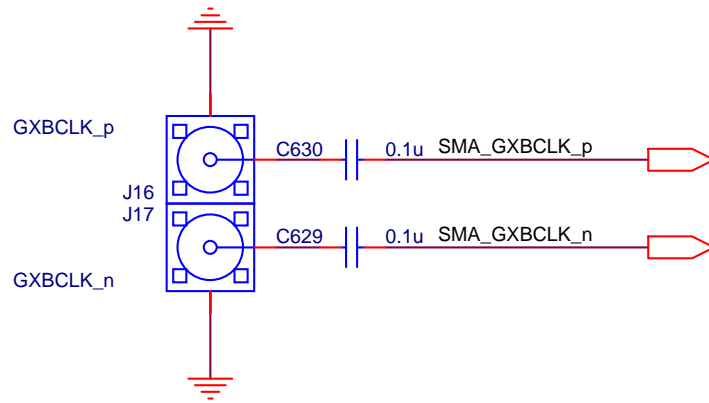
## Default 100MHz




## Default 100MHz



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Title		
Terasic TR4 Board		
Size	Document Number	Rev
B	Clock Generator 2	1.0
Date:	Friday, January 13, 2012	Sheet 5 of 41



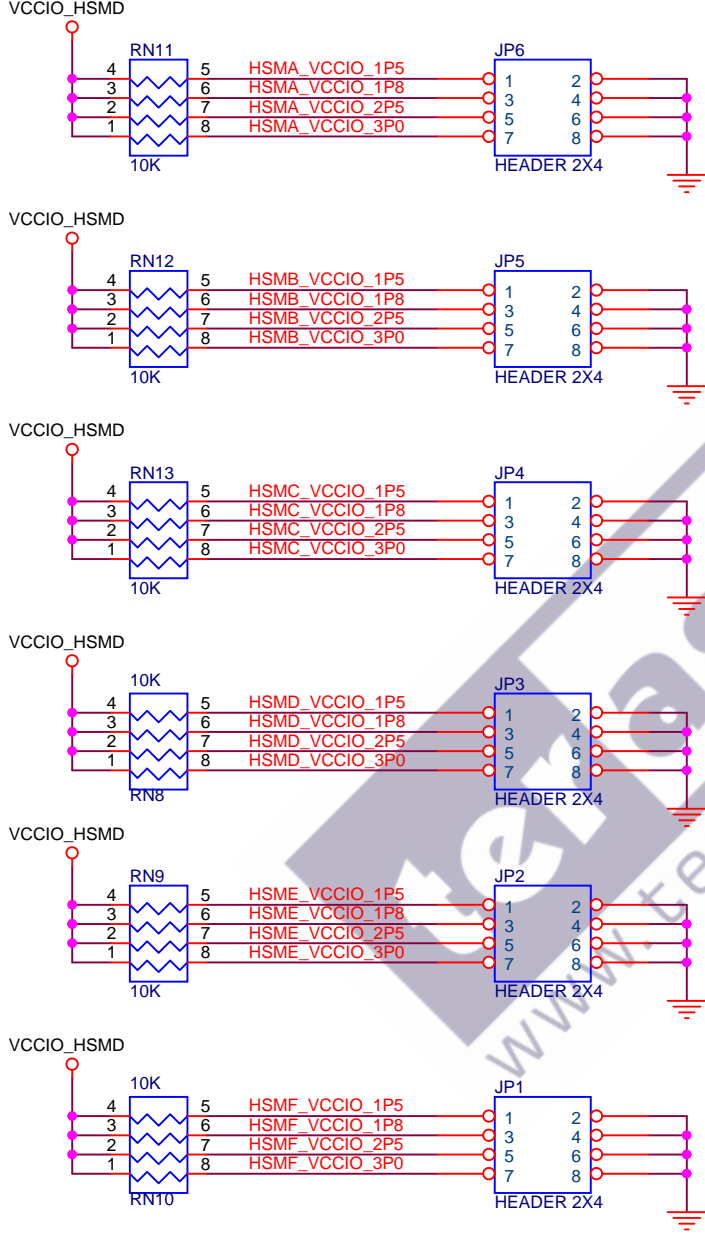
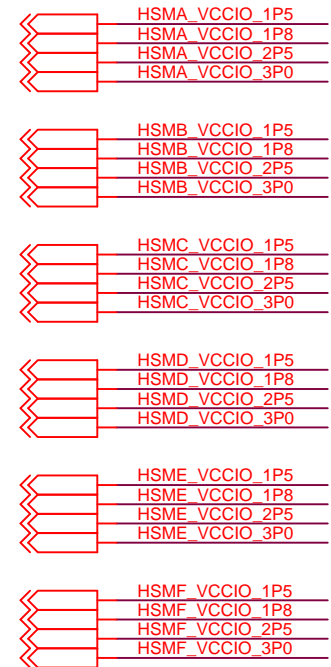
Place Termination  
at S4GX

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Title		
ALTERA DE4 Board		
Size	Document Number	Rev
A	SMA Clock Circuit	1.0
Date:	Friday, January 13, 2012	Sheet 6 of 41

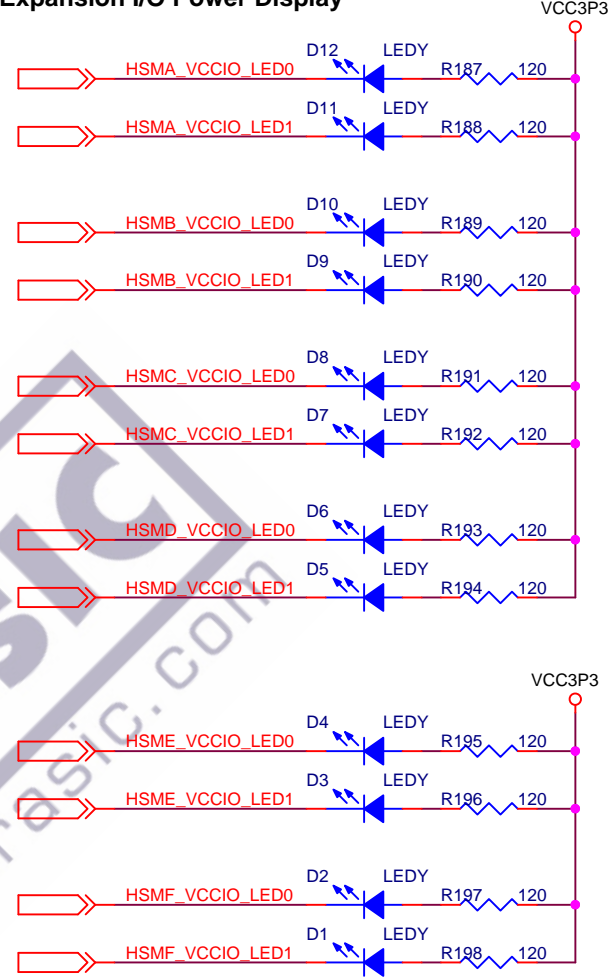




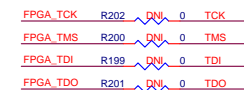
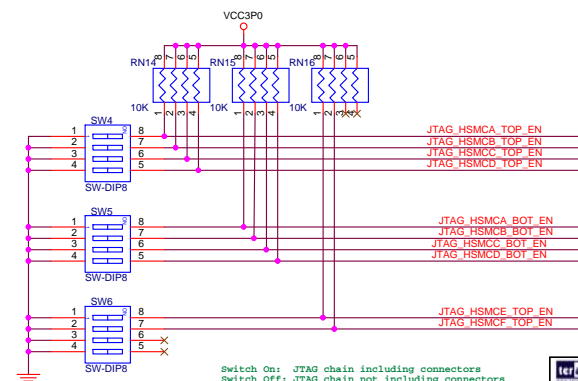
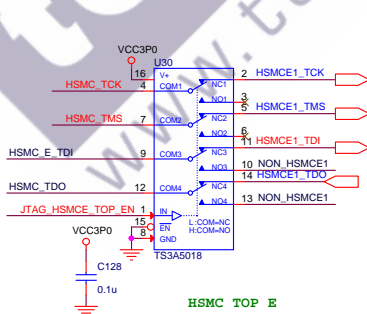
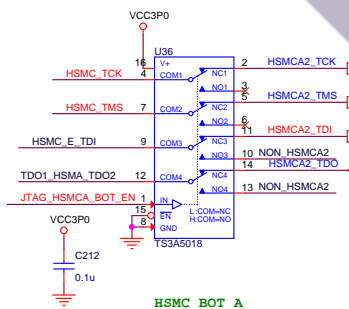
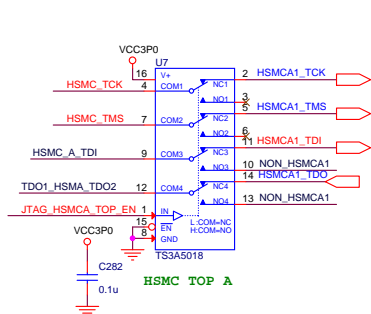
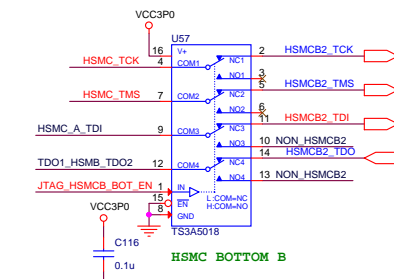
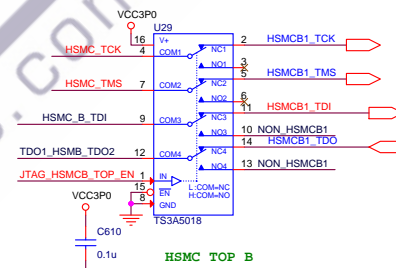
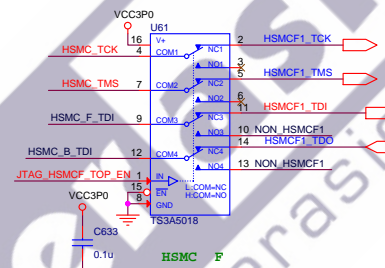
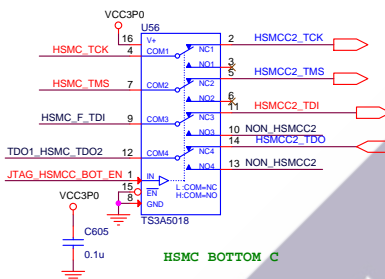
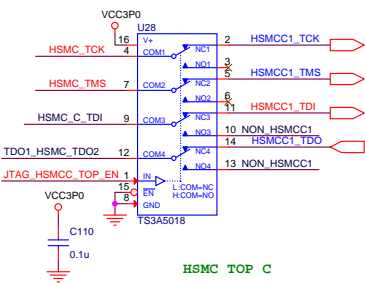
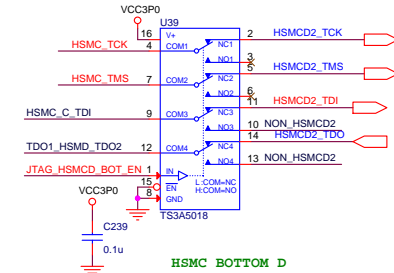
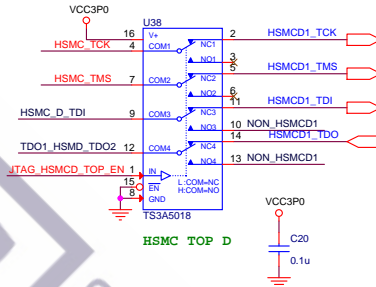
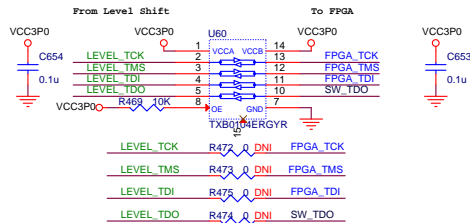
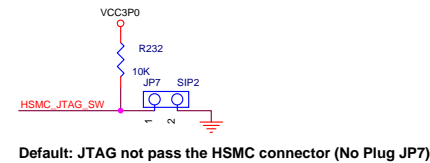
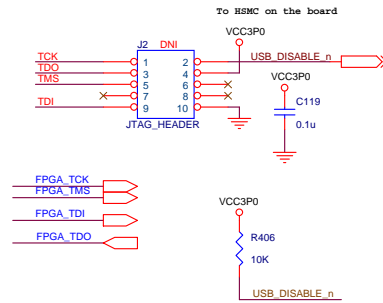
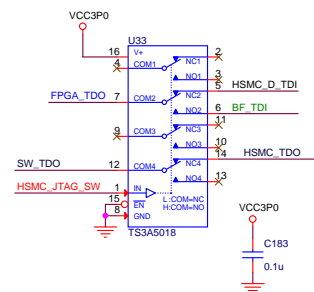
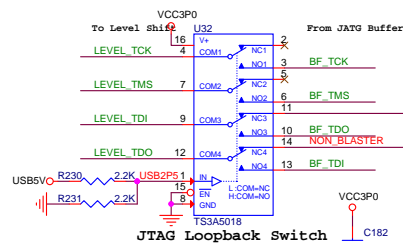
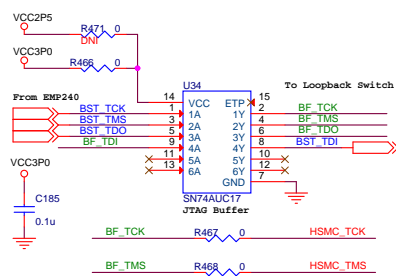
Expansion I/O Power Select



Expansion I/O Power Display

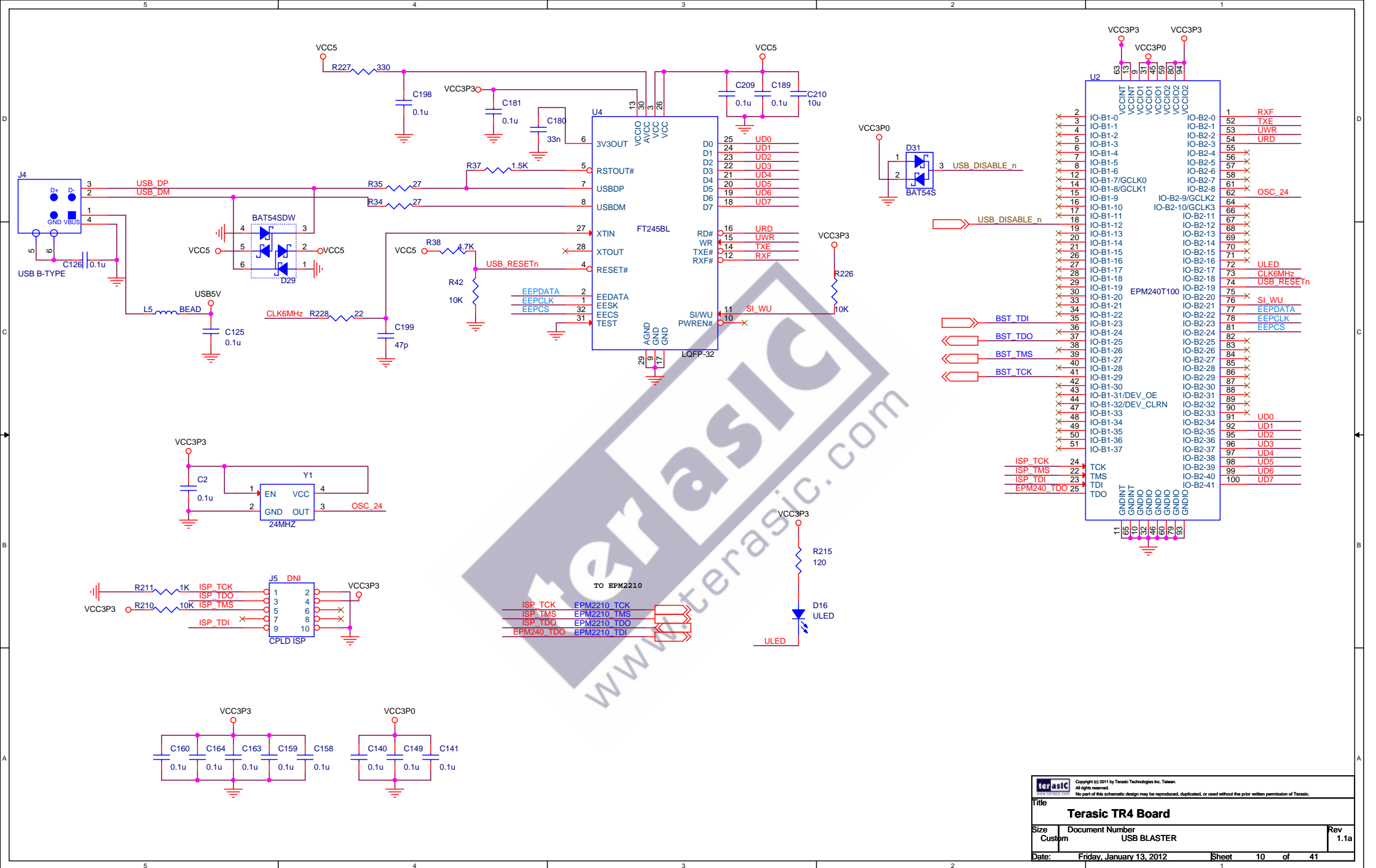


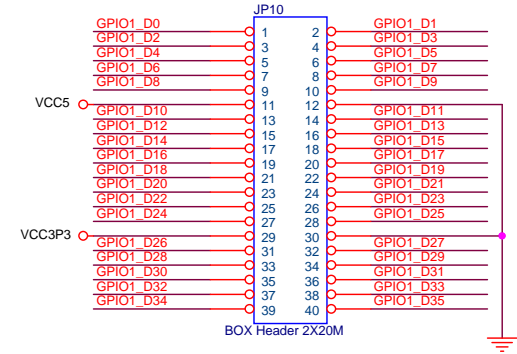
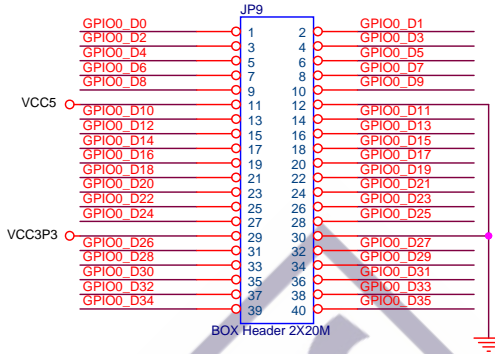
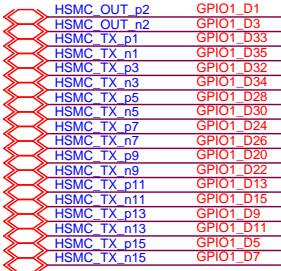
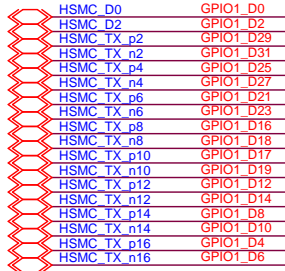
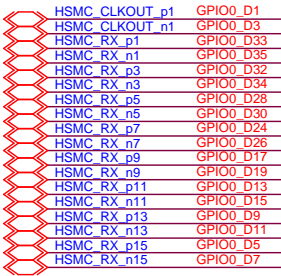
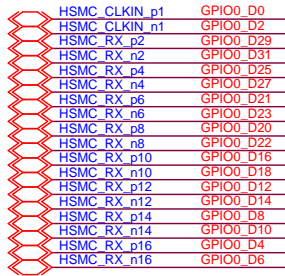


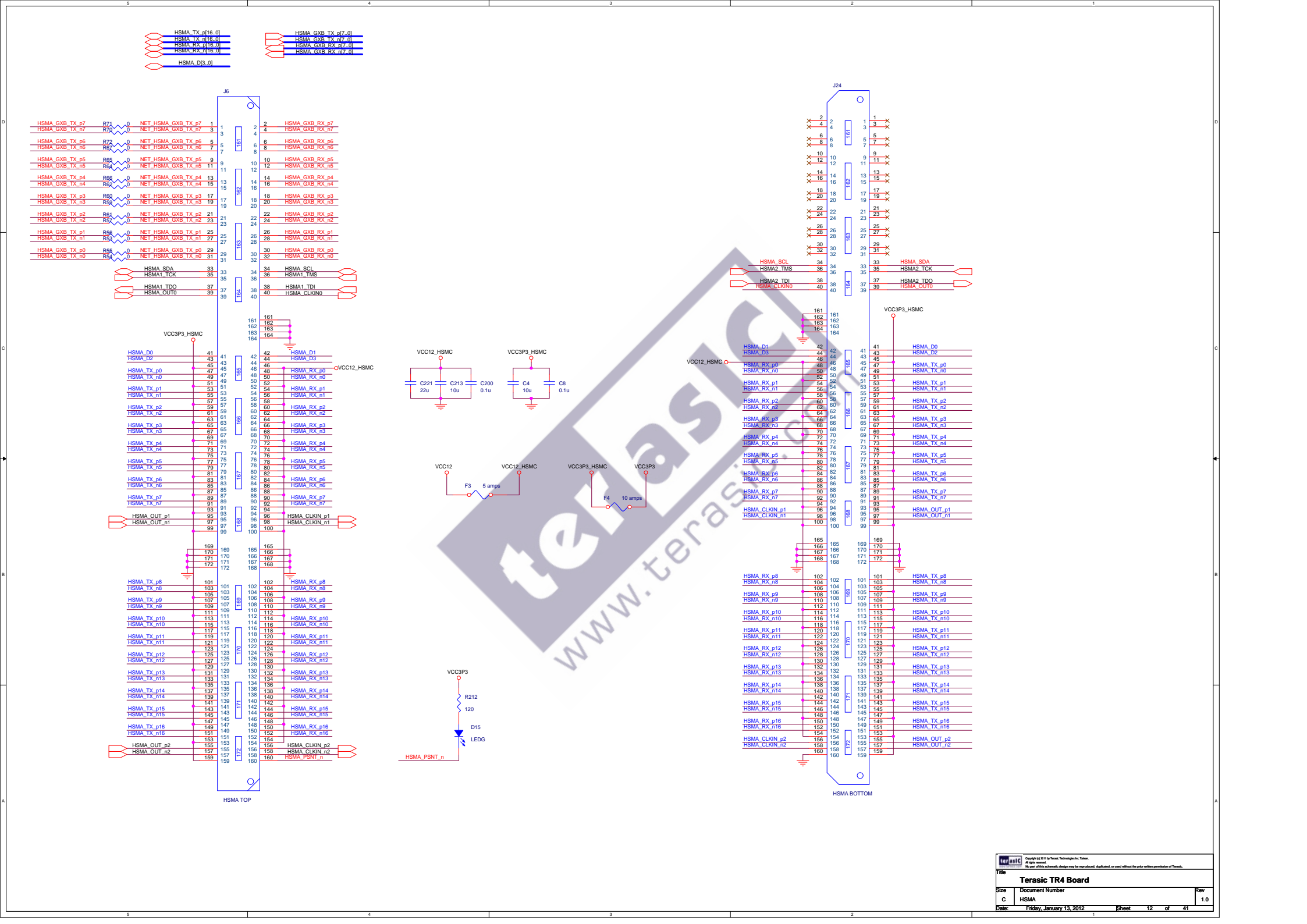


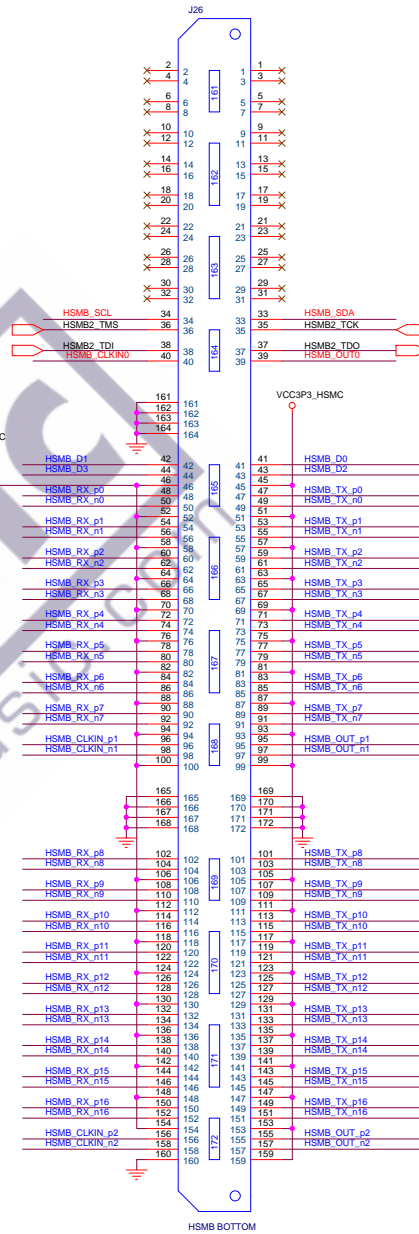
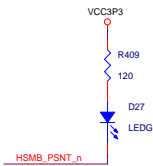
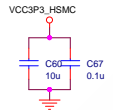
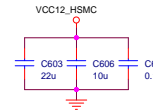
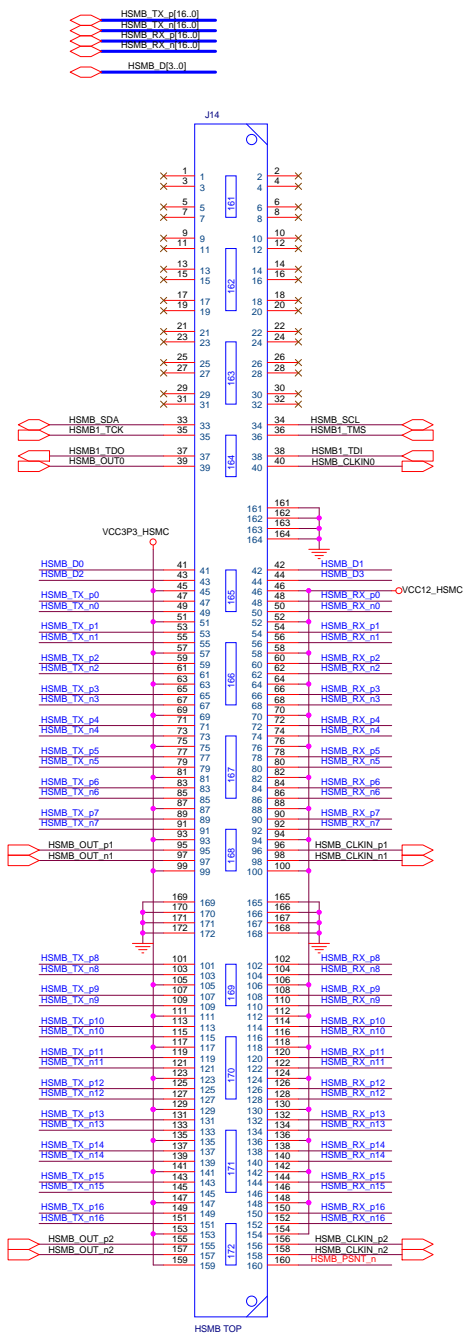
Switch On: JTAG chain including connectors  
Switch Off: JTAG chain not including connectors

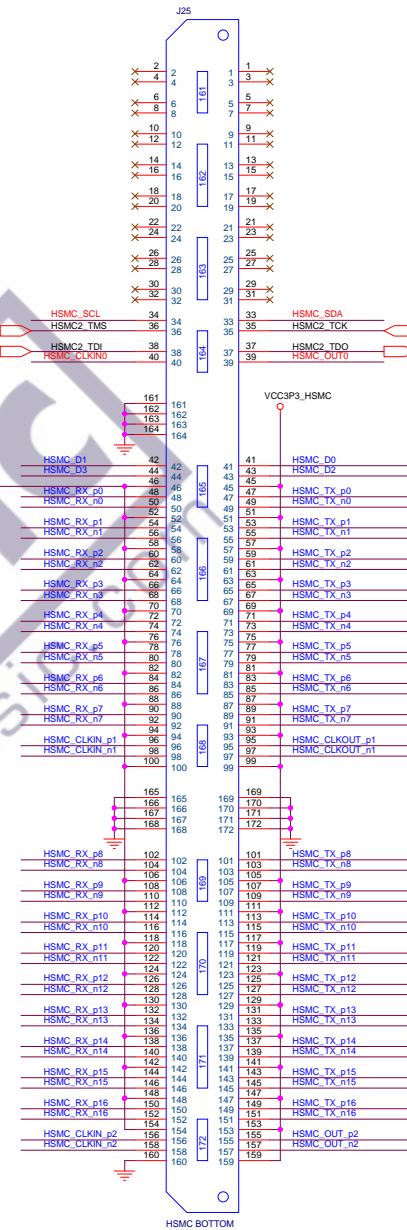
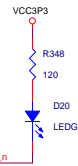
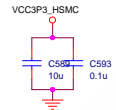
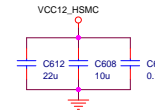
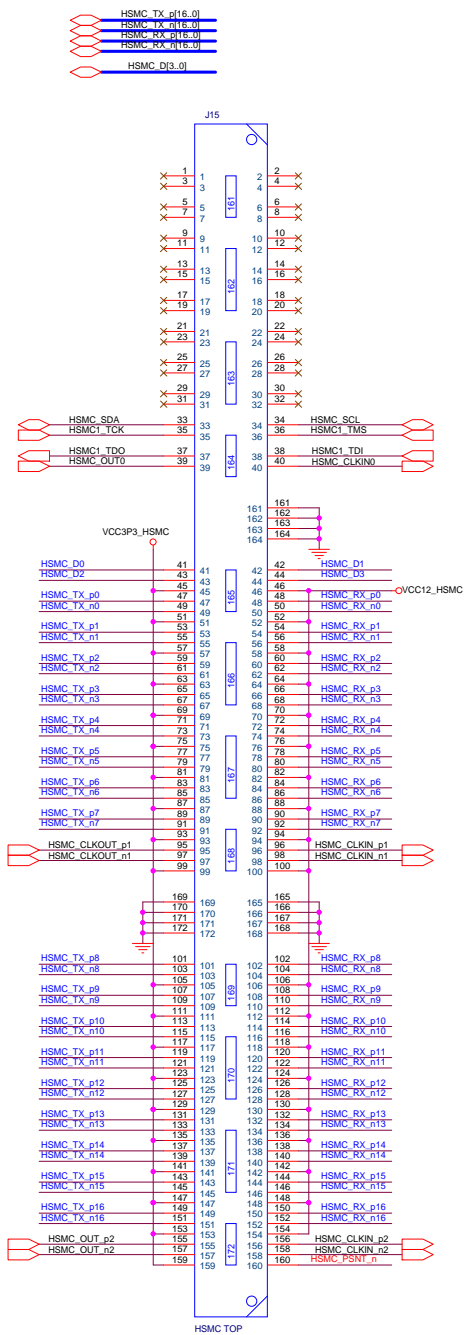
<b>Terasic TR4 Board</b>		
Size	Document Number	Rev
Custom JTAG Chain		1.0
Date	Friday, January 13, 2012	Sheet 9 of 41



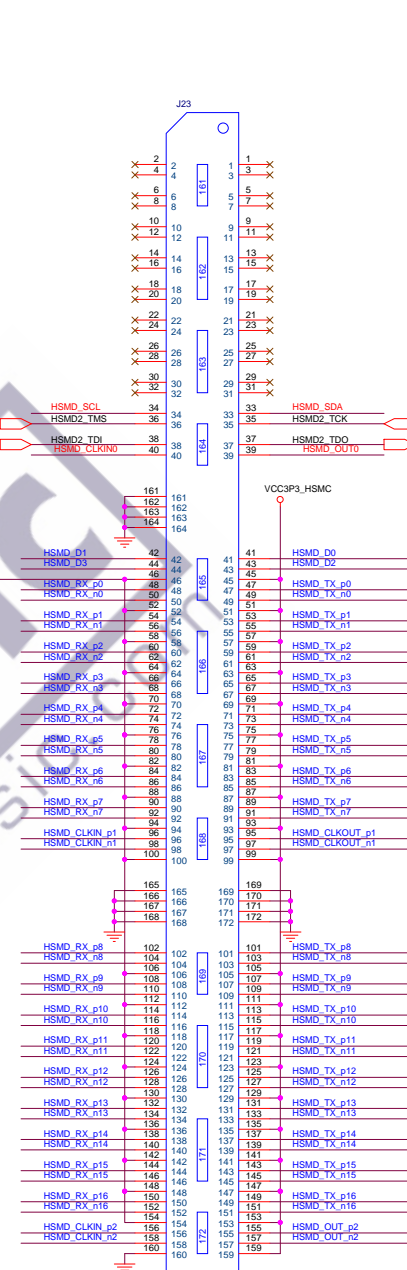
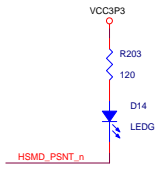
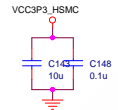
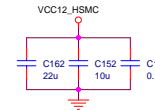
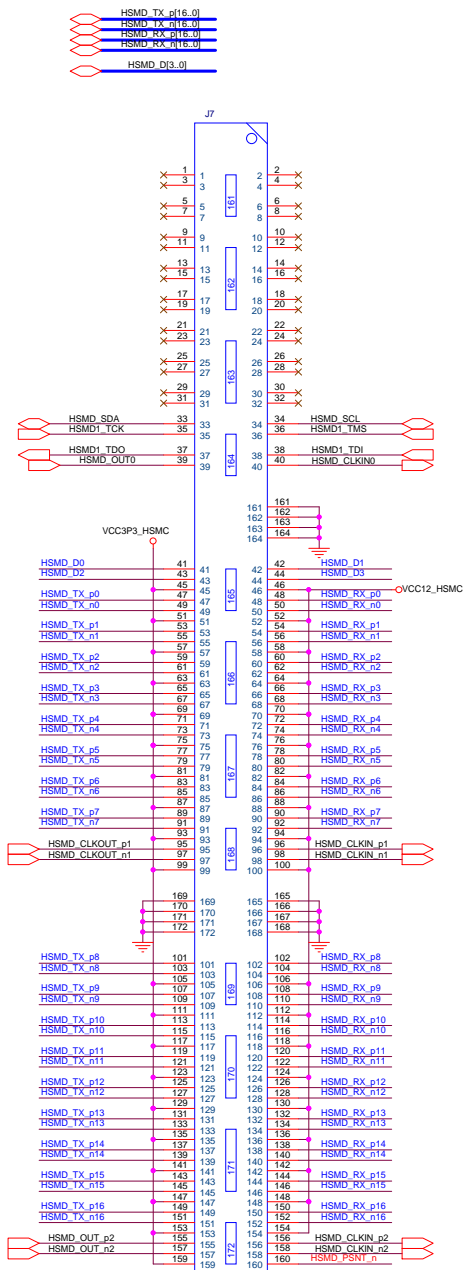






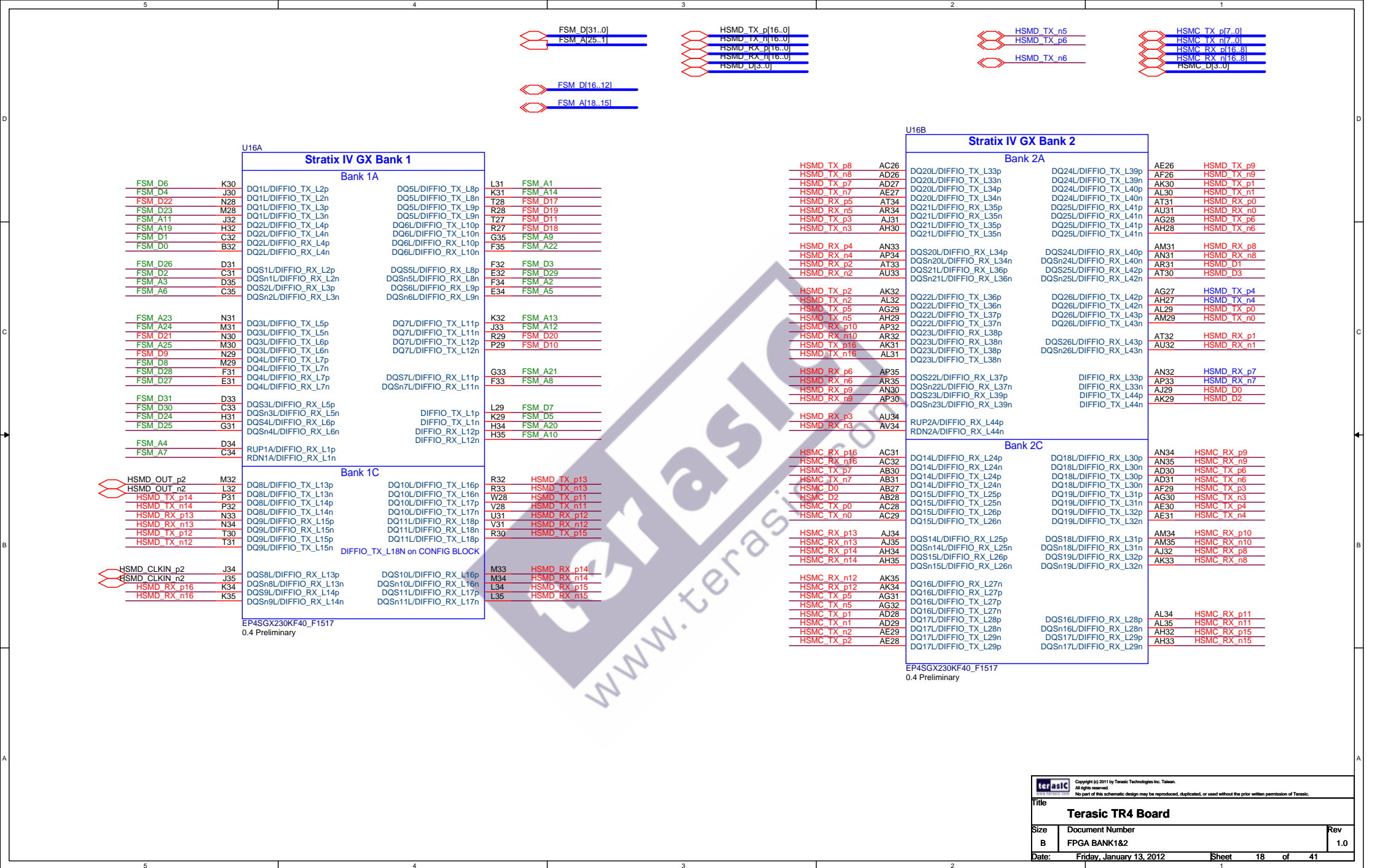






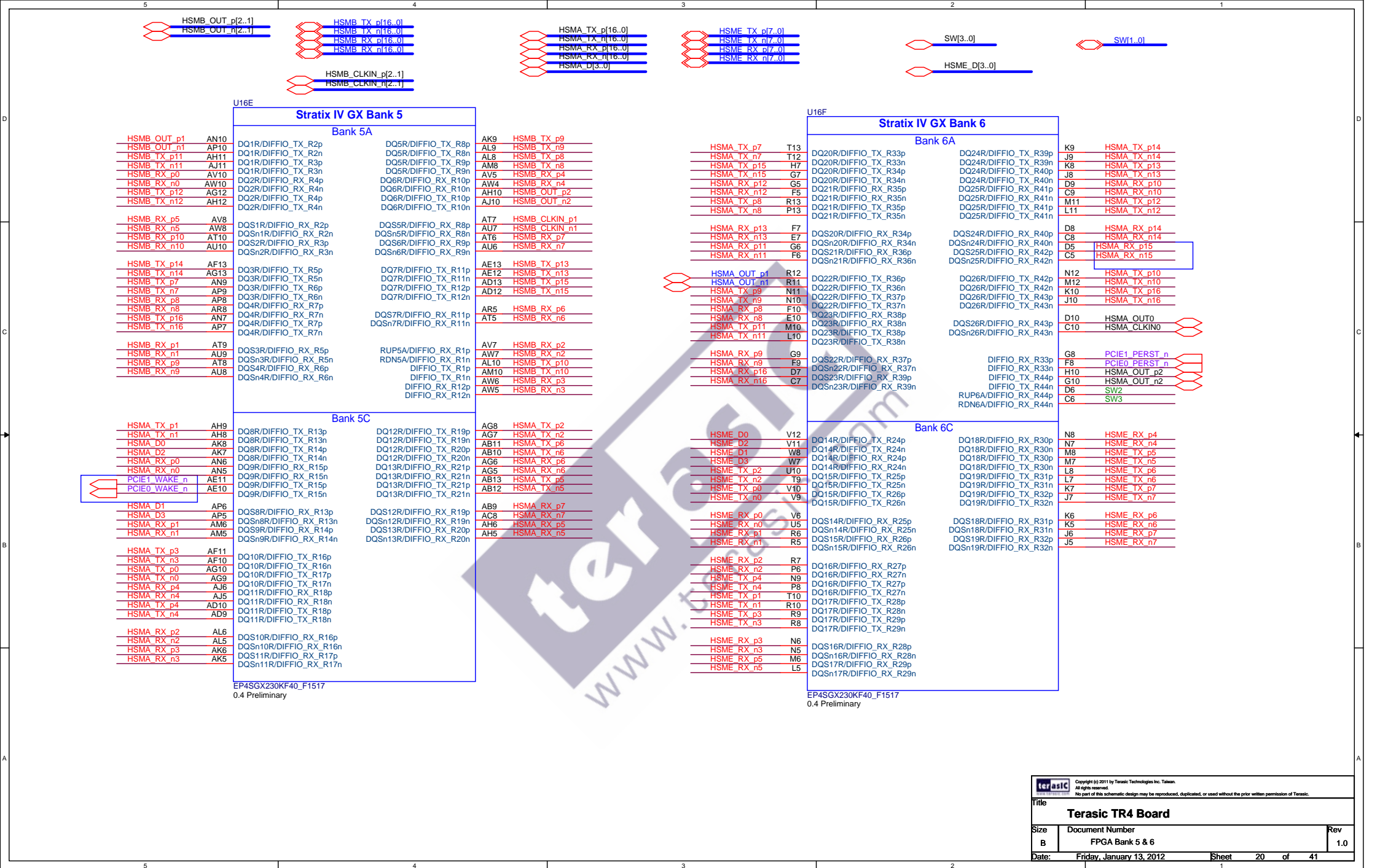




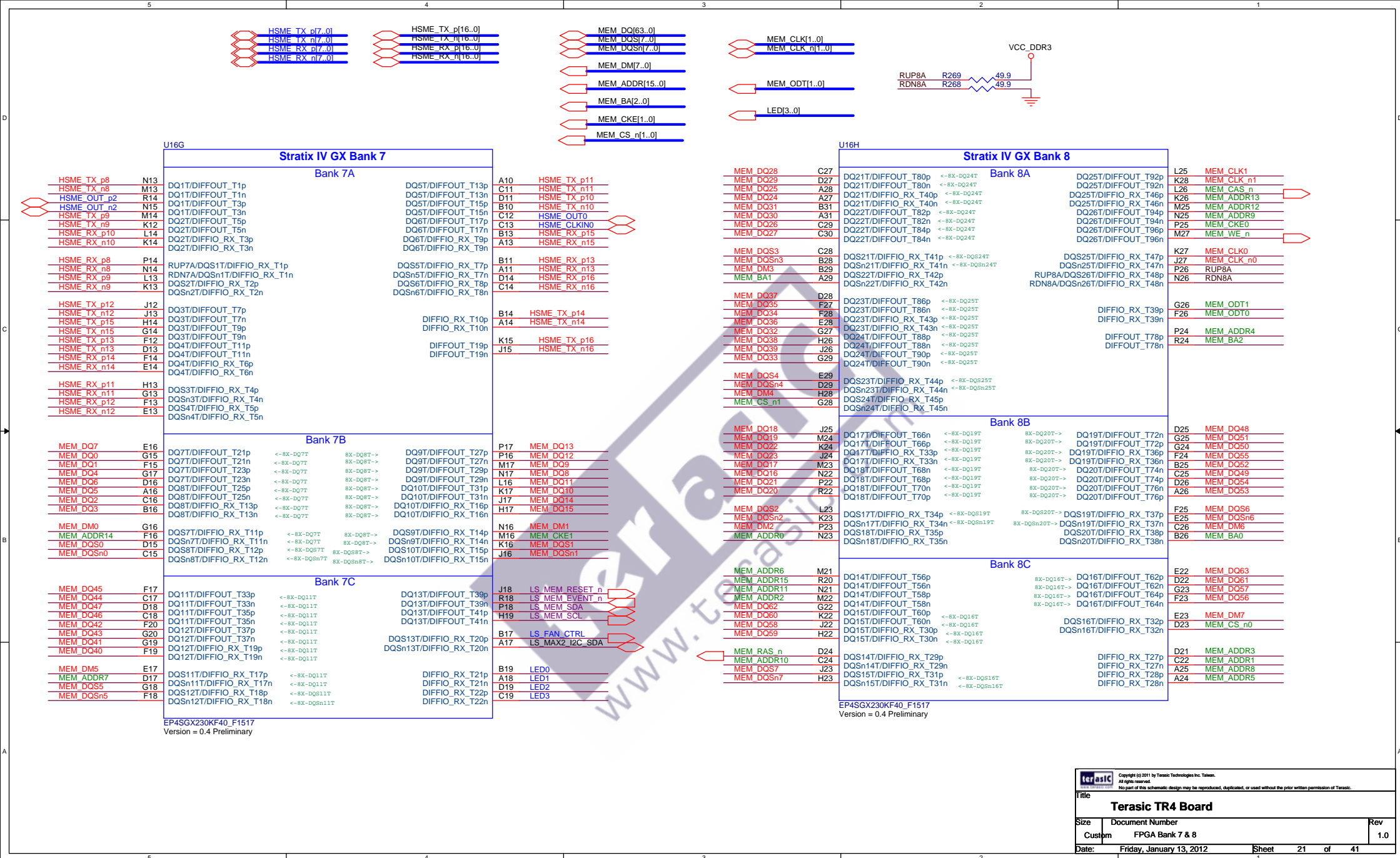








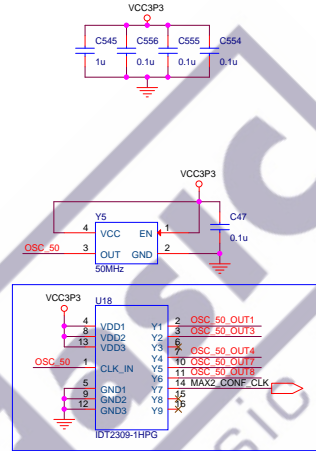
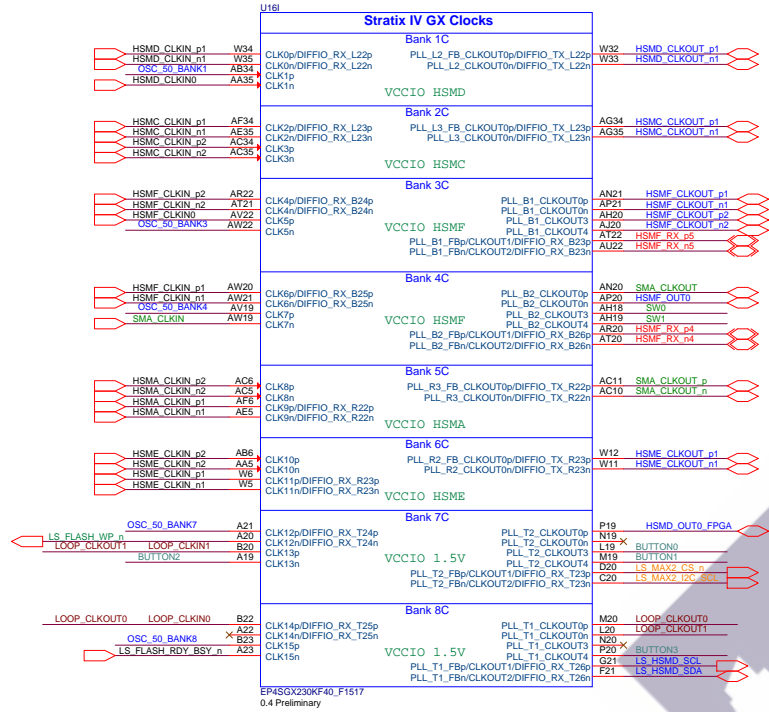




On-chip differential termination is supported on all row I/O pins and dedicated clock input pins (CLK[0,2,3,11]). It is not supported for column I/O pins, dedicated clock input pins (CLK[1,3,8,10]), or the corner PLL clock inputs.

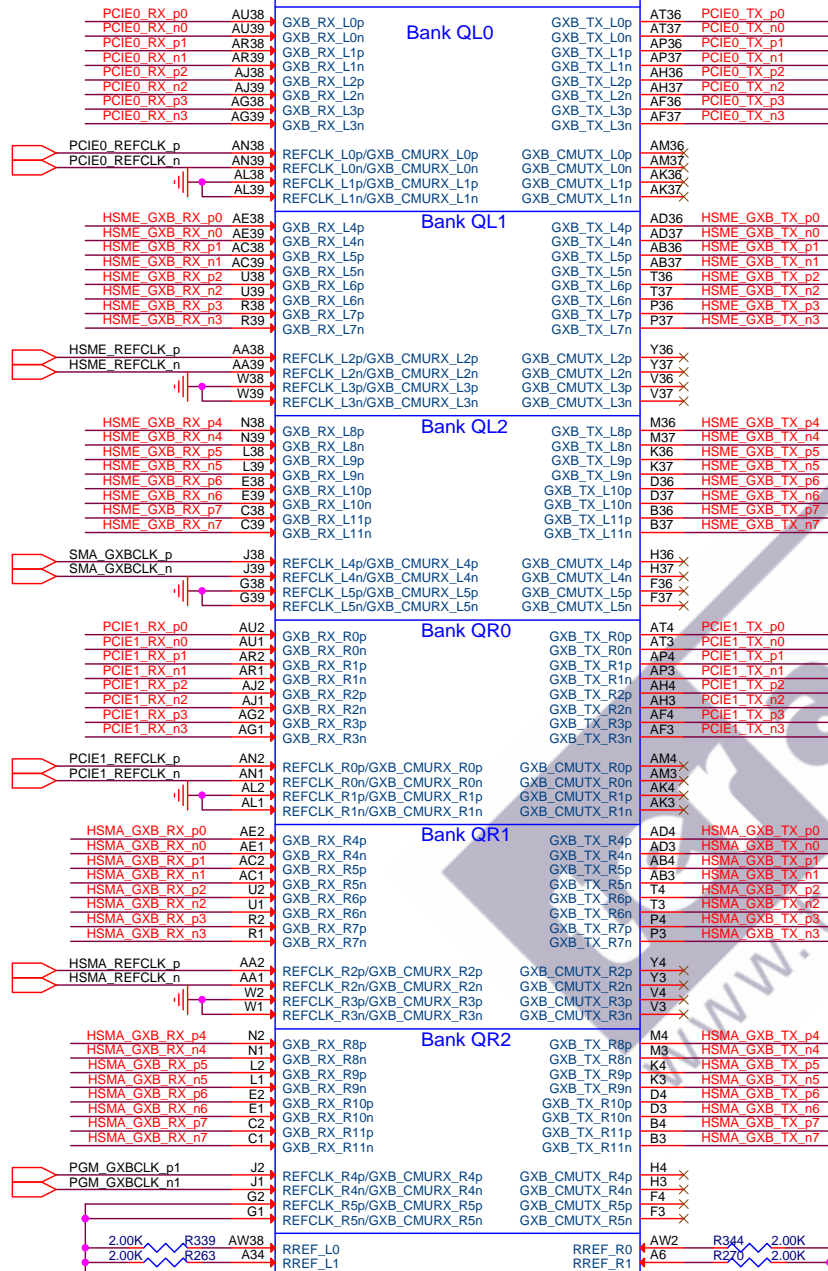
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HSMC\_CLKIN\_p2 R300 DN\_100 HSMC\_CLKIN\_n2  
HSMC\_CLKIN\_p2 R295 DN\_100 HSMC\_CLKIN\_n2  
HSMF\_CLKIN\_p2 R317 DN\_100 HSMF\_CLKIN\_n2  
HSMF\_CLKIN\_p1 R342 DN\_100 HSMF\_CLKIN\_n1

BUTTON3\_0  
SW1\_01



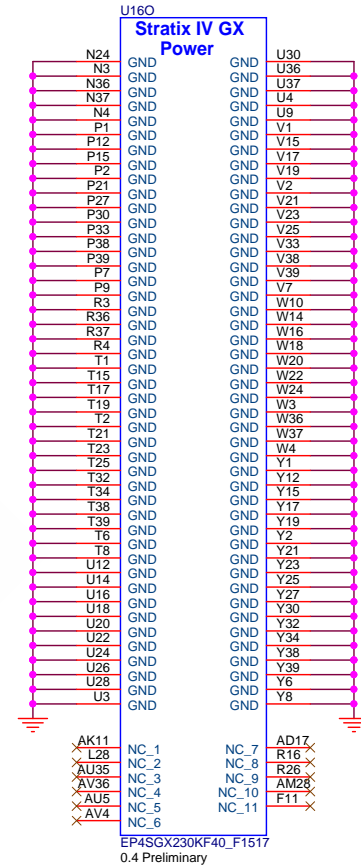
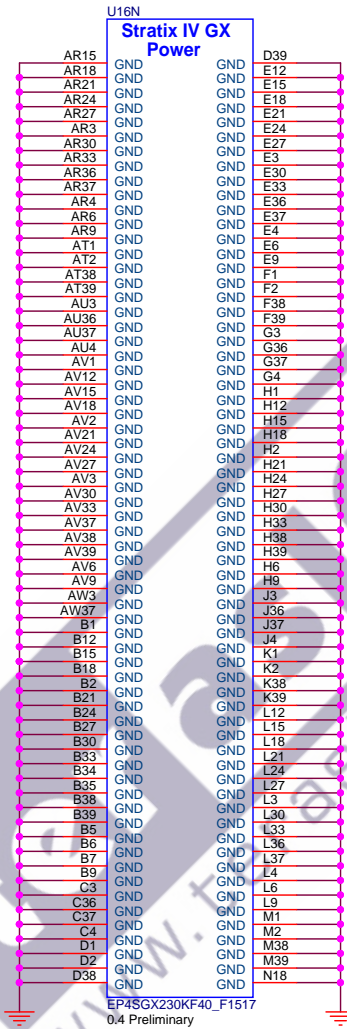
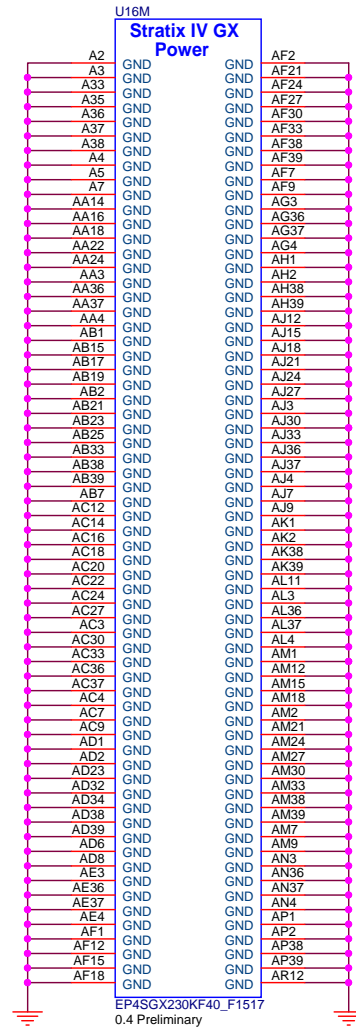


# Stratix IV GX Transceivers



set the REFCLK to LVDS I/O Standard

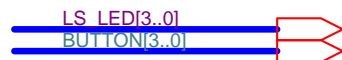
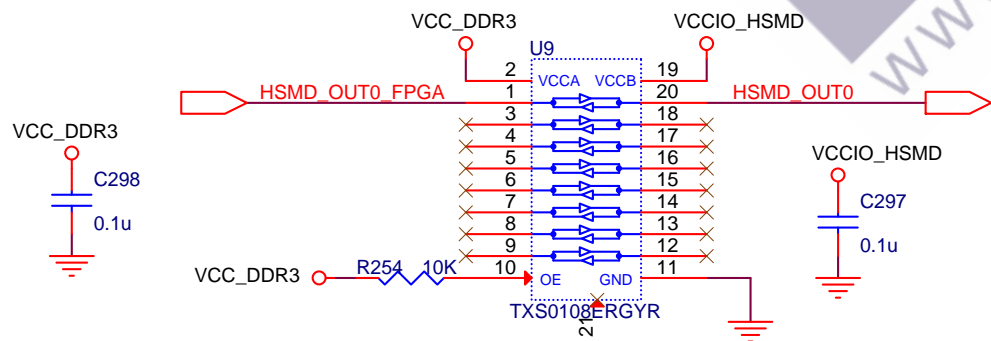
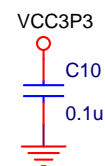
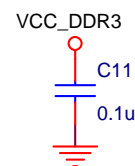
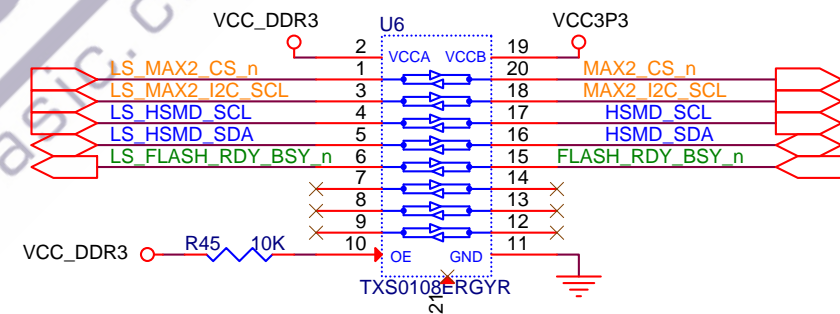
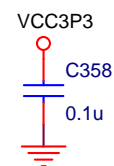
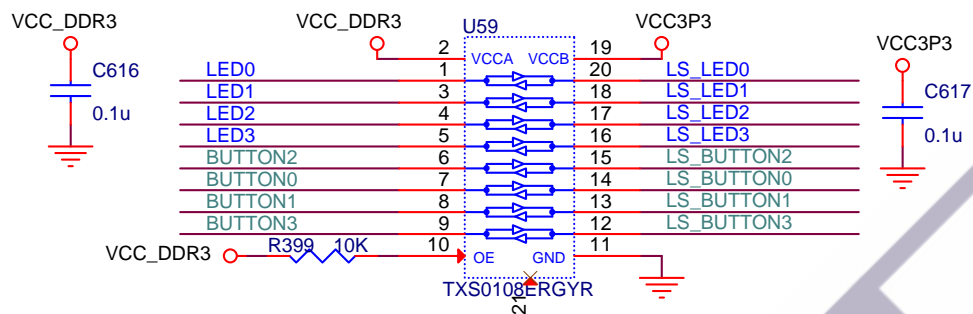
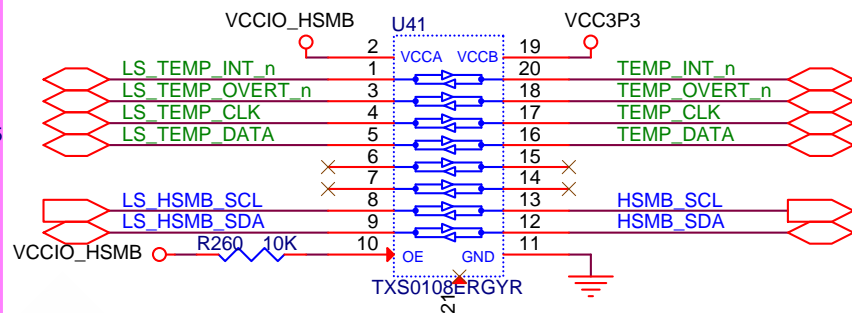
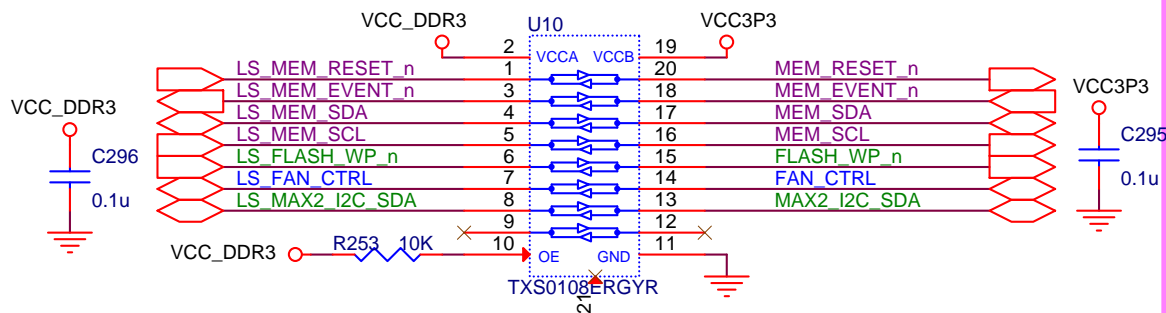
<div> <div>                     Copyright (c) 2011 by Terasic Technologies Inc. Taiwan.                      All rights reserved.                      No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.                 </div> </div>		
Title		
Terasic TR4 Board		
Size	Document Number	Rev
B	FPGA Bank QRL	1.0
Date:	Friday, January 13, 2012	Sheet 24 of 41





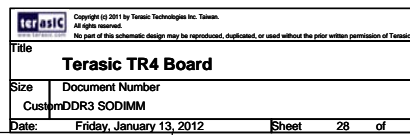
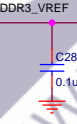
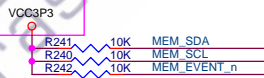
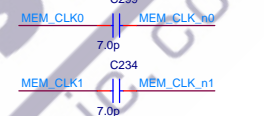
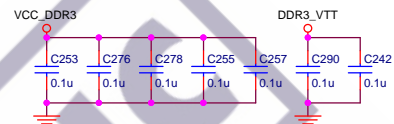
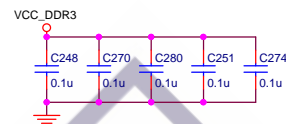
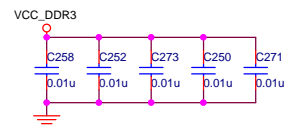
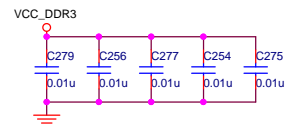
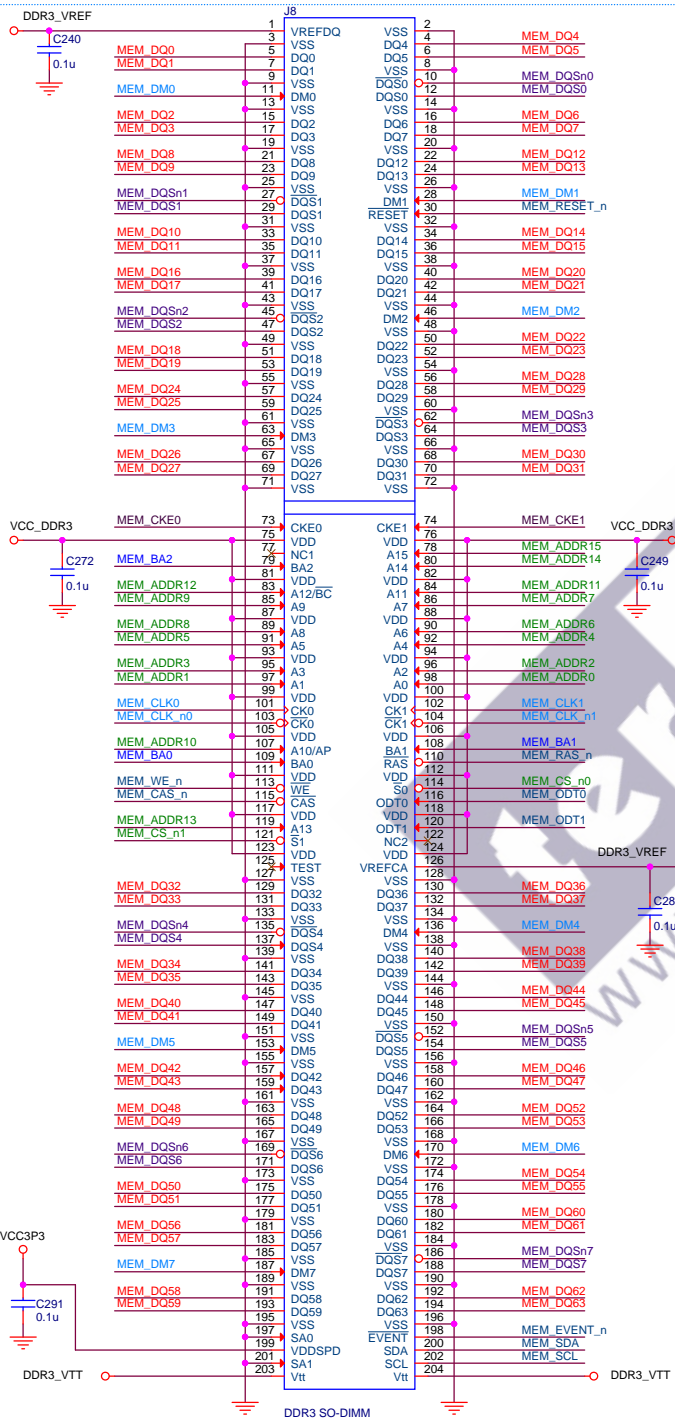
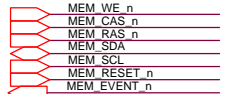
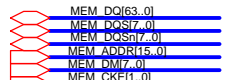
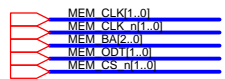


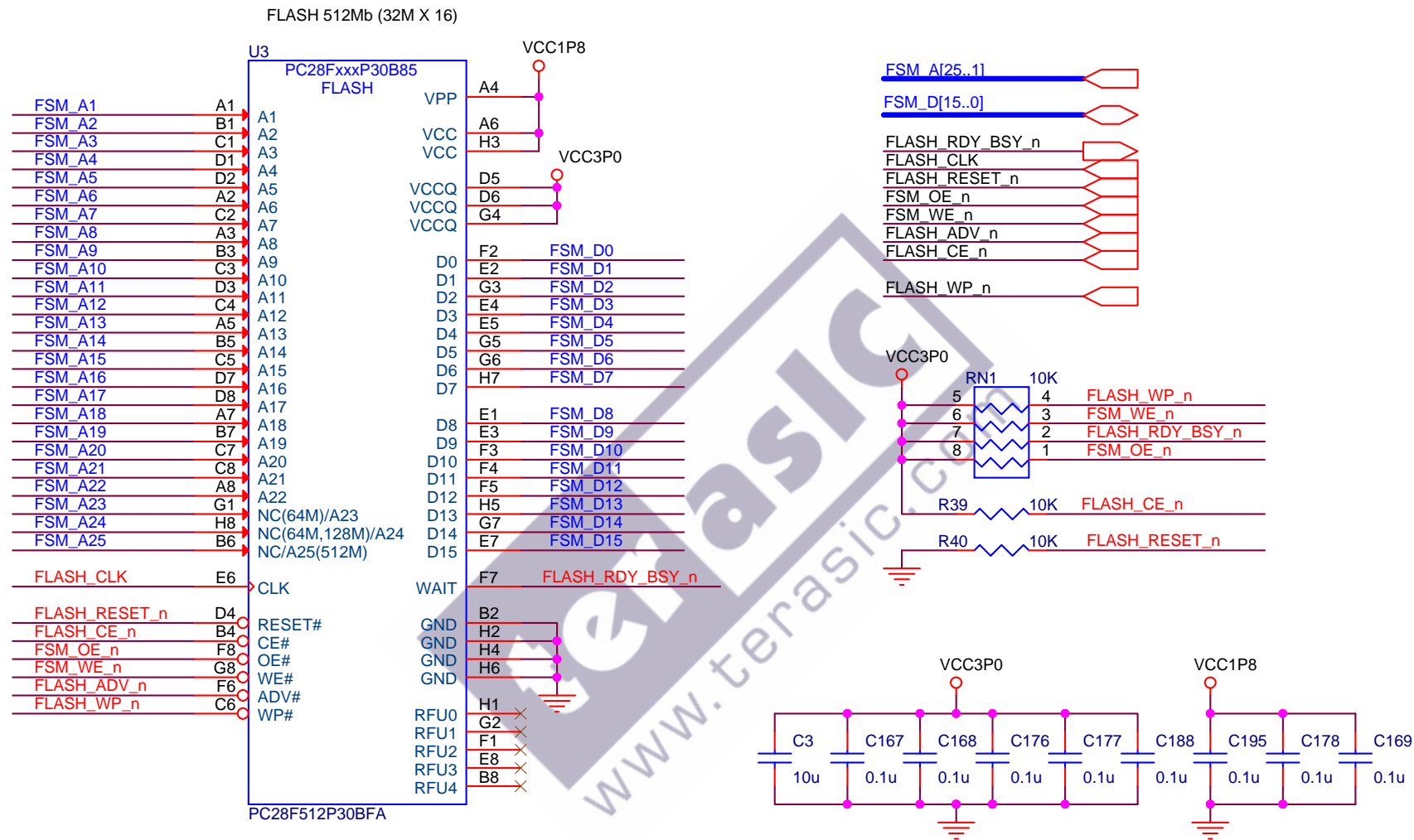


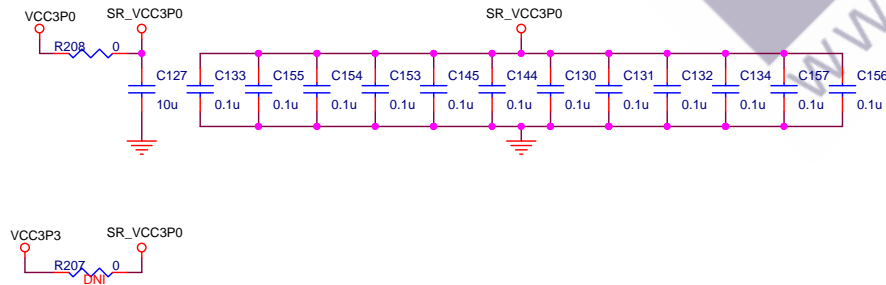
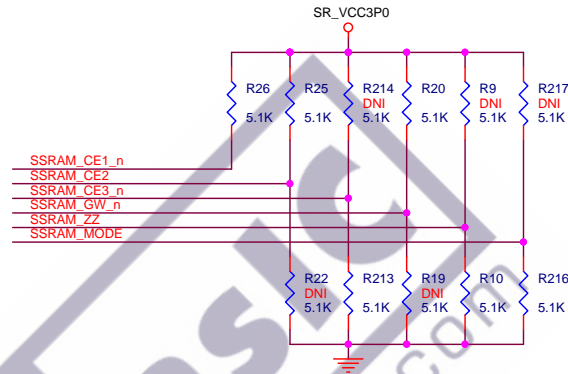
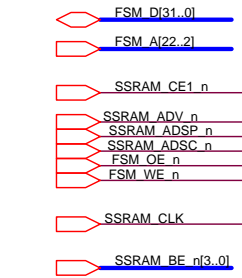
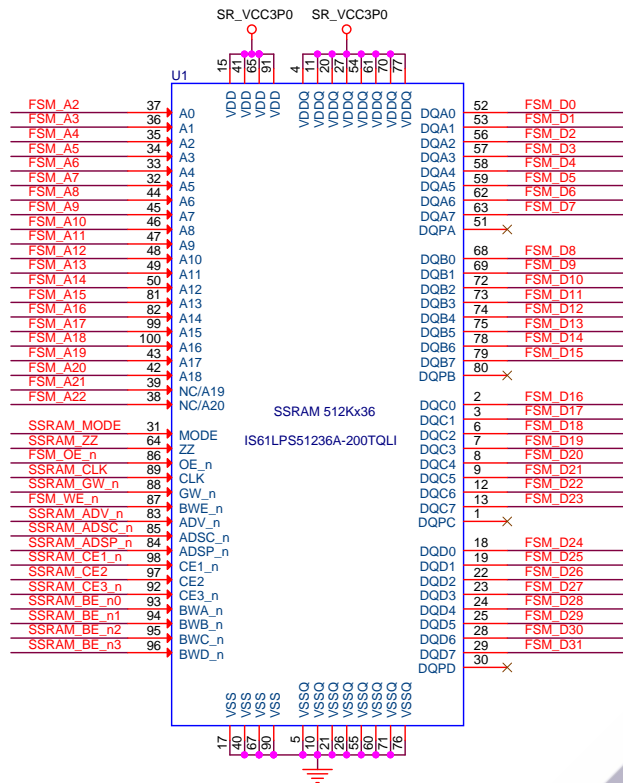


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## DDR3 SO-DIMM

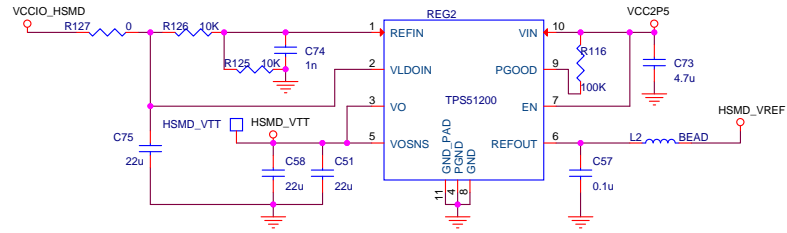




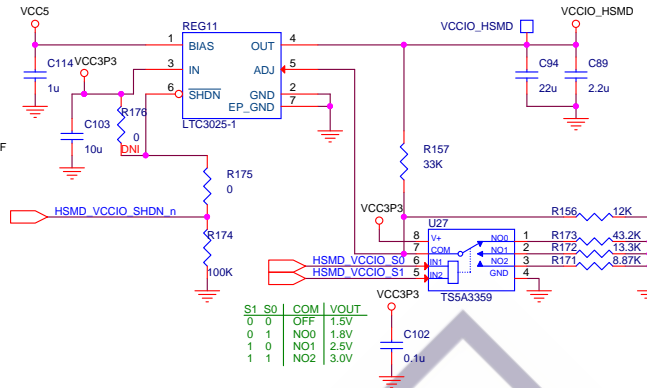




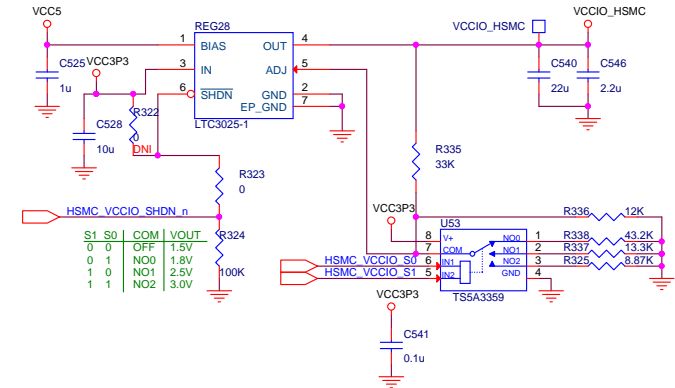
## HSMD VTT, VREF



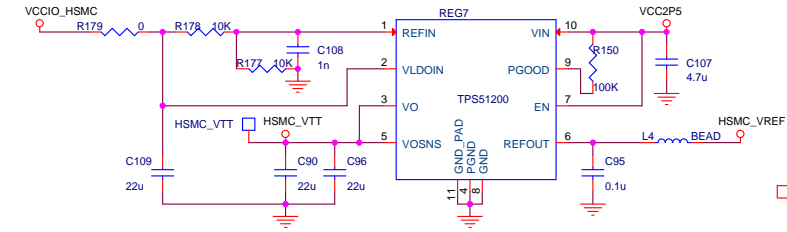
## VCCIO\_HSMD / 0.5A



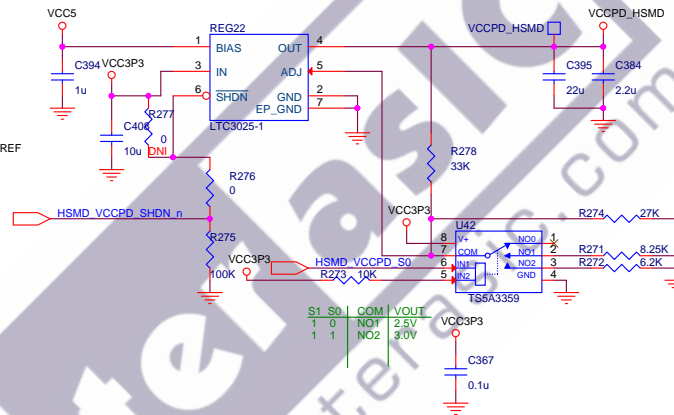
## VCCIO\_HSMC / 0.5A



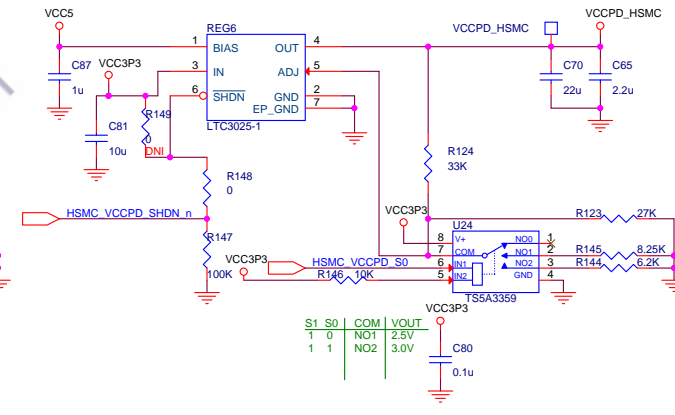
## HSMC VTT, VREF



## VCCPD\_HSMD / 0.5A

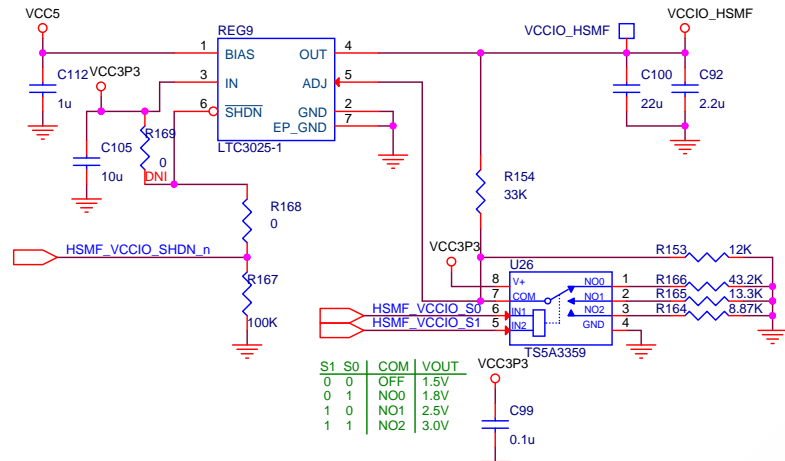


## VCCPD\_HSMC / 0.5A

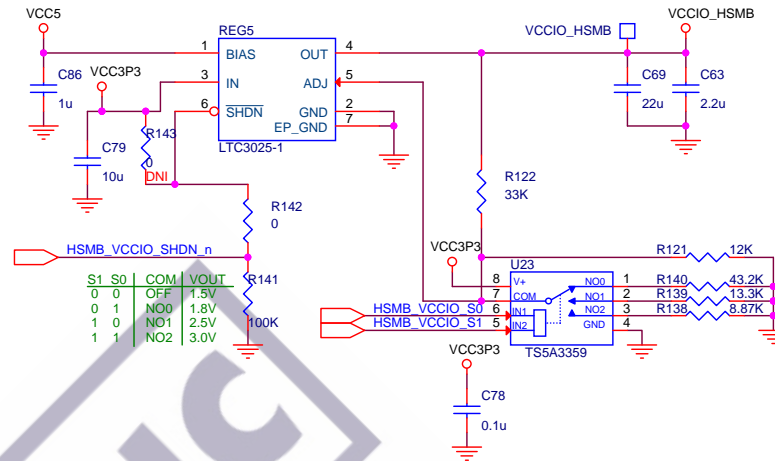




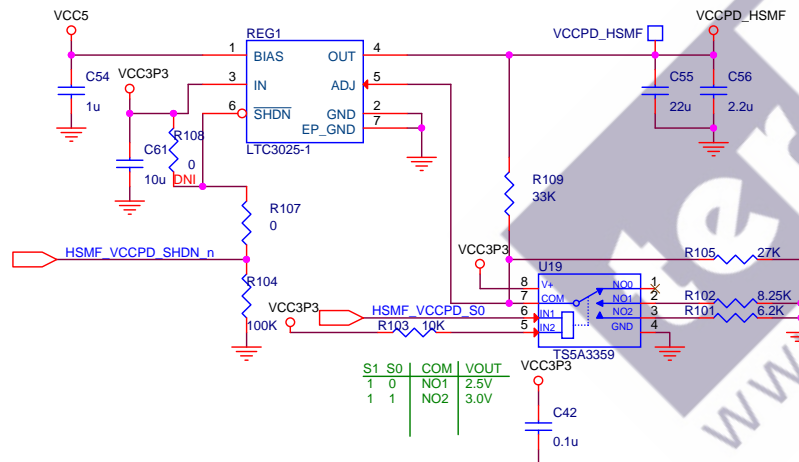
VCCIO\_HSMF / 0.5A



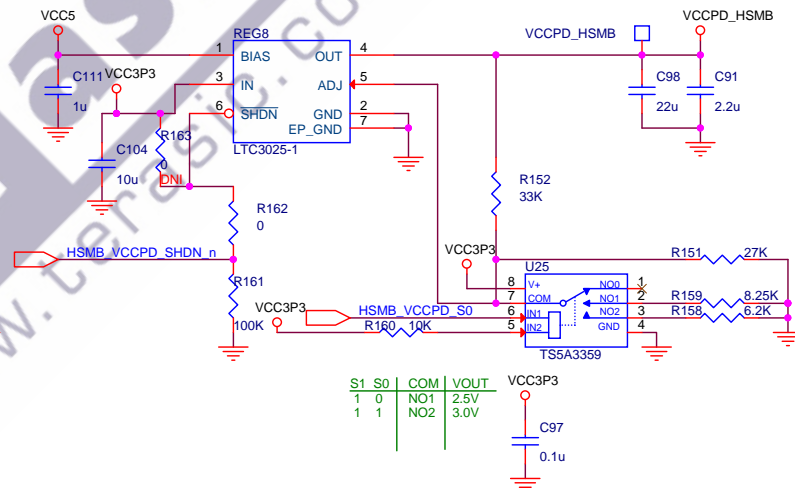
VCCIO\_HSMB / 0.5A



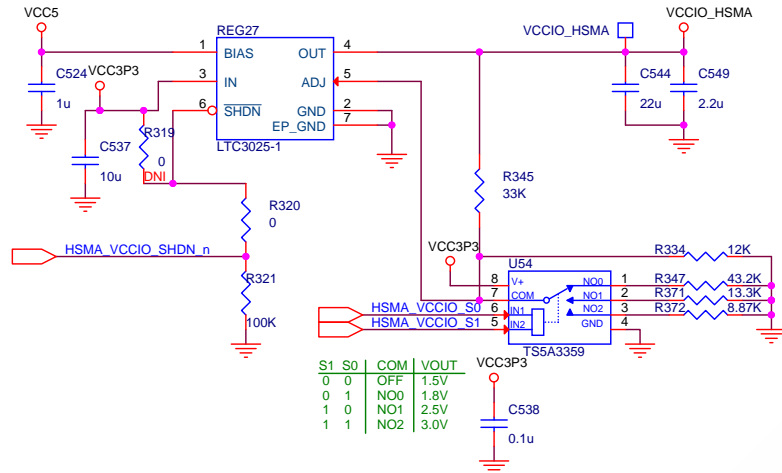
VCCPD\_HSMF / 0.5A



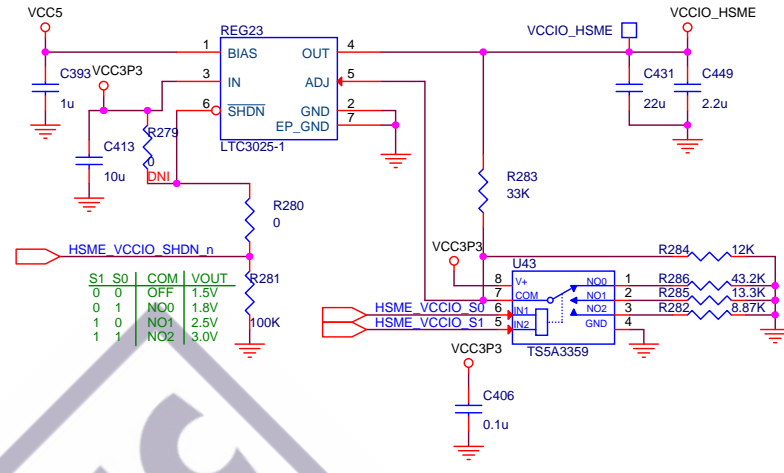
VCCPD\_HSMB / 0.5A



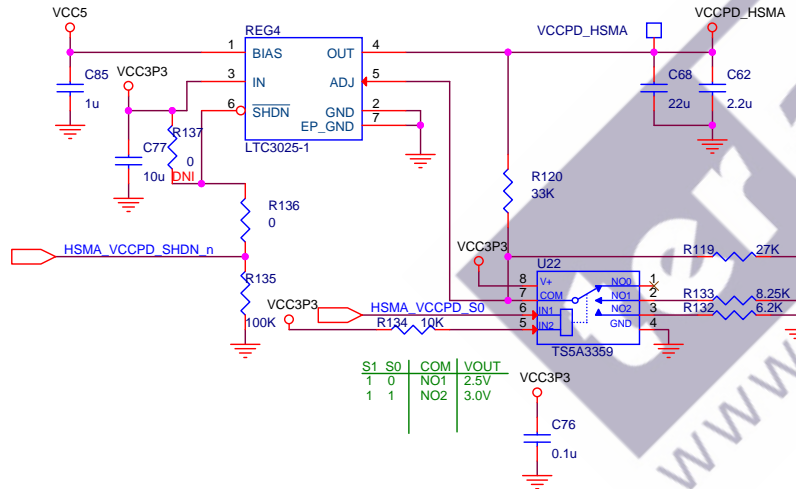
# VCCIO\_HSMA / 0.5A



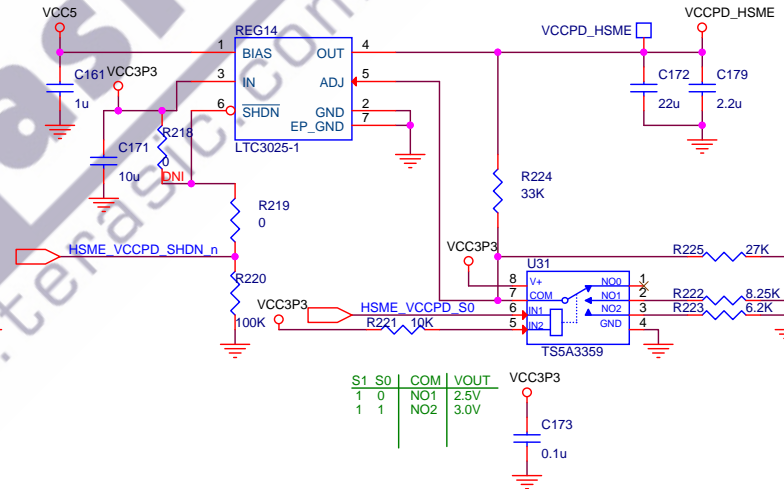
# VCCIO\_HSME / 0.5A

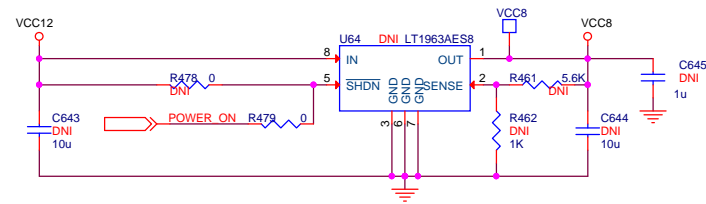


# VCCPD\_HSMA / 0.5A

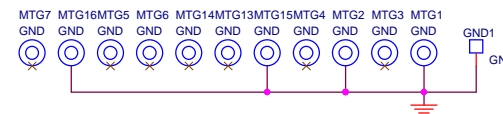
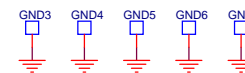
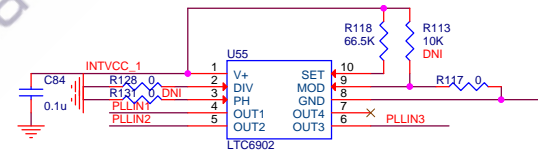
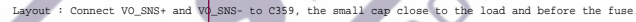


# VCCPD\_HSME / 0.5A

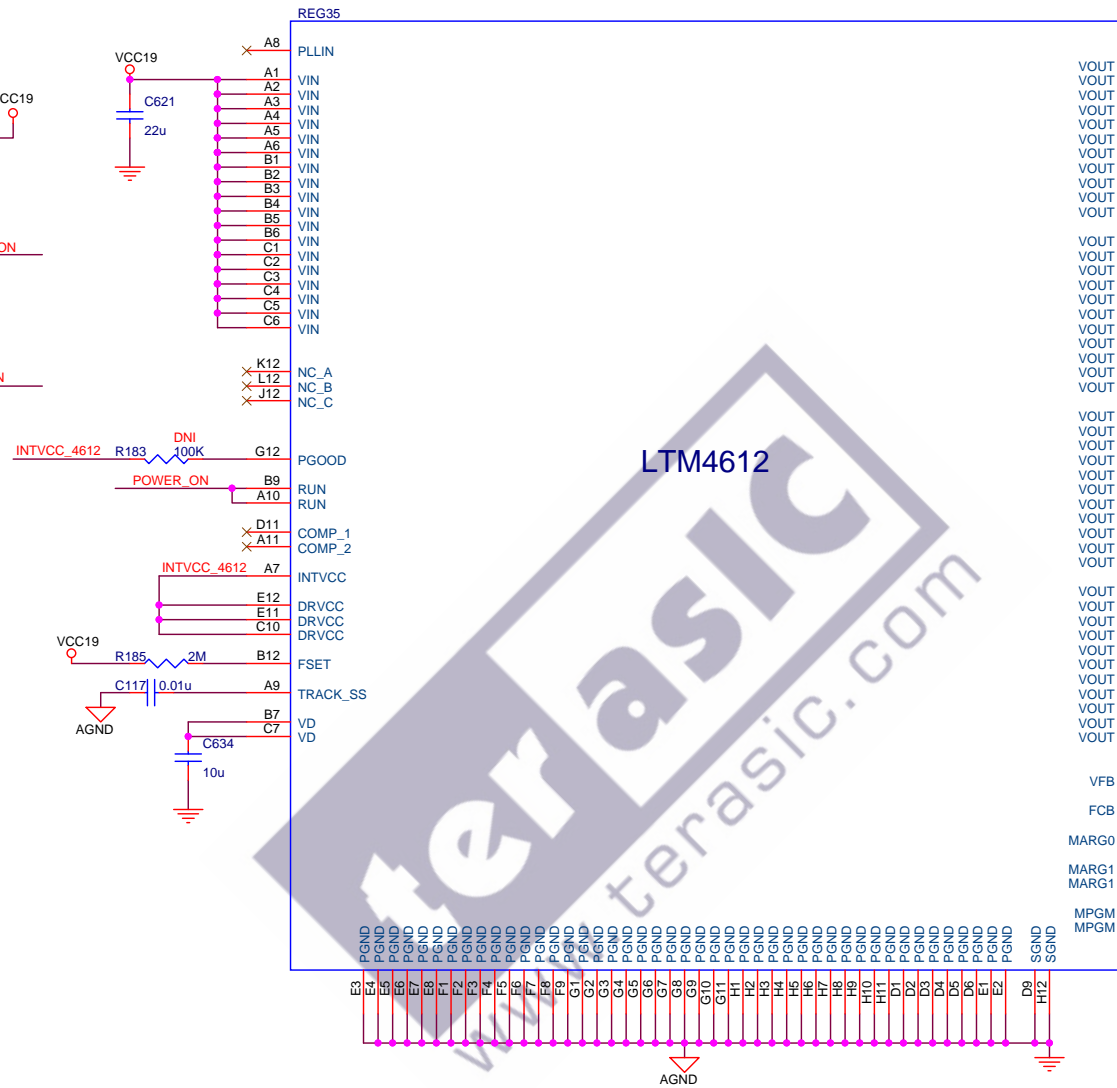
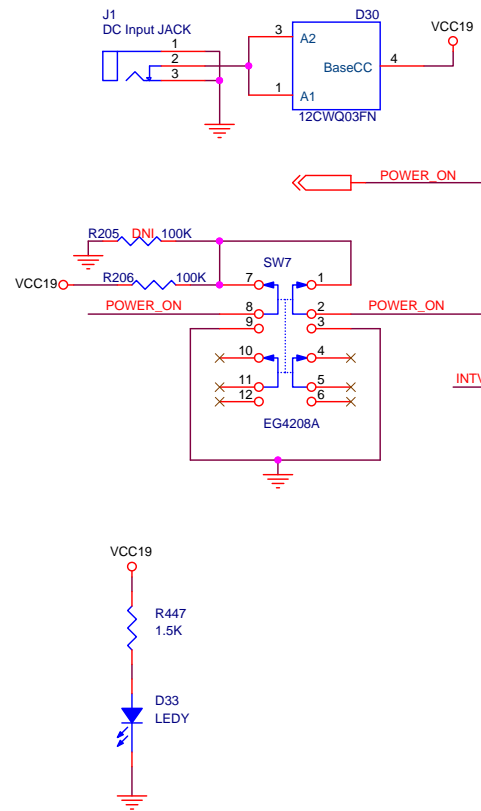




POWER\_ON

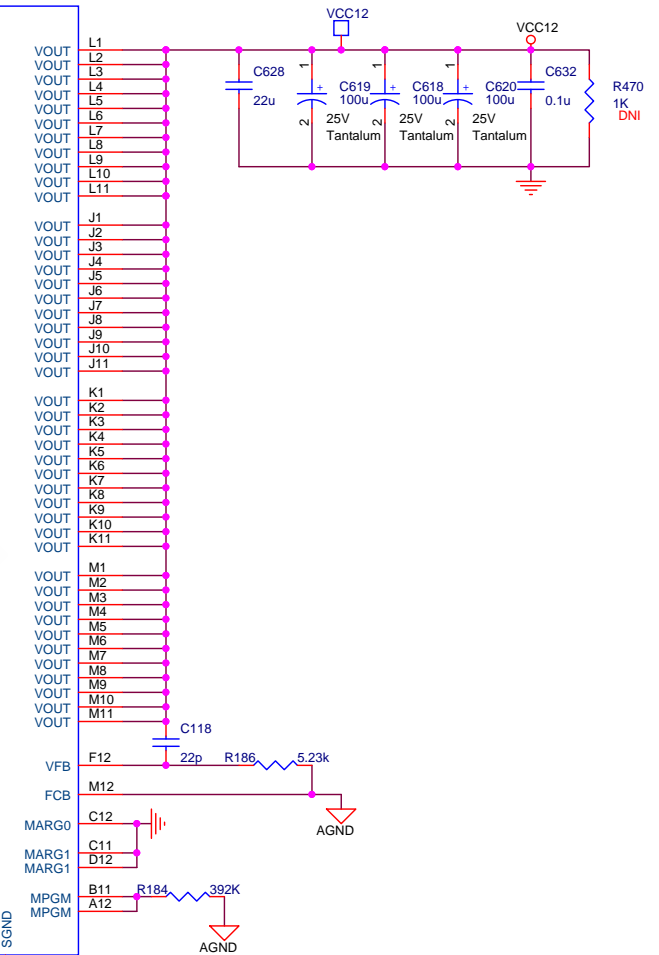


### 19V DC Input

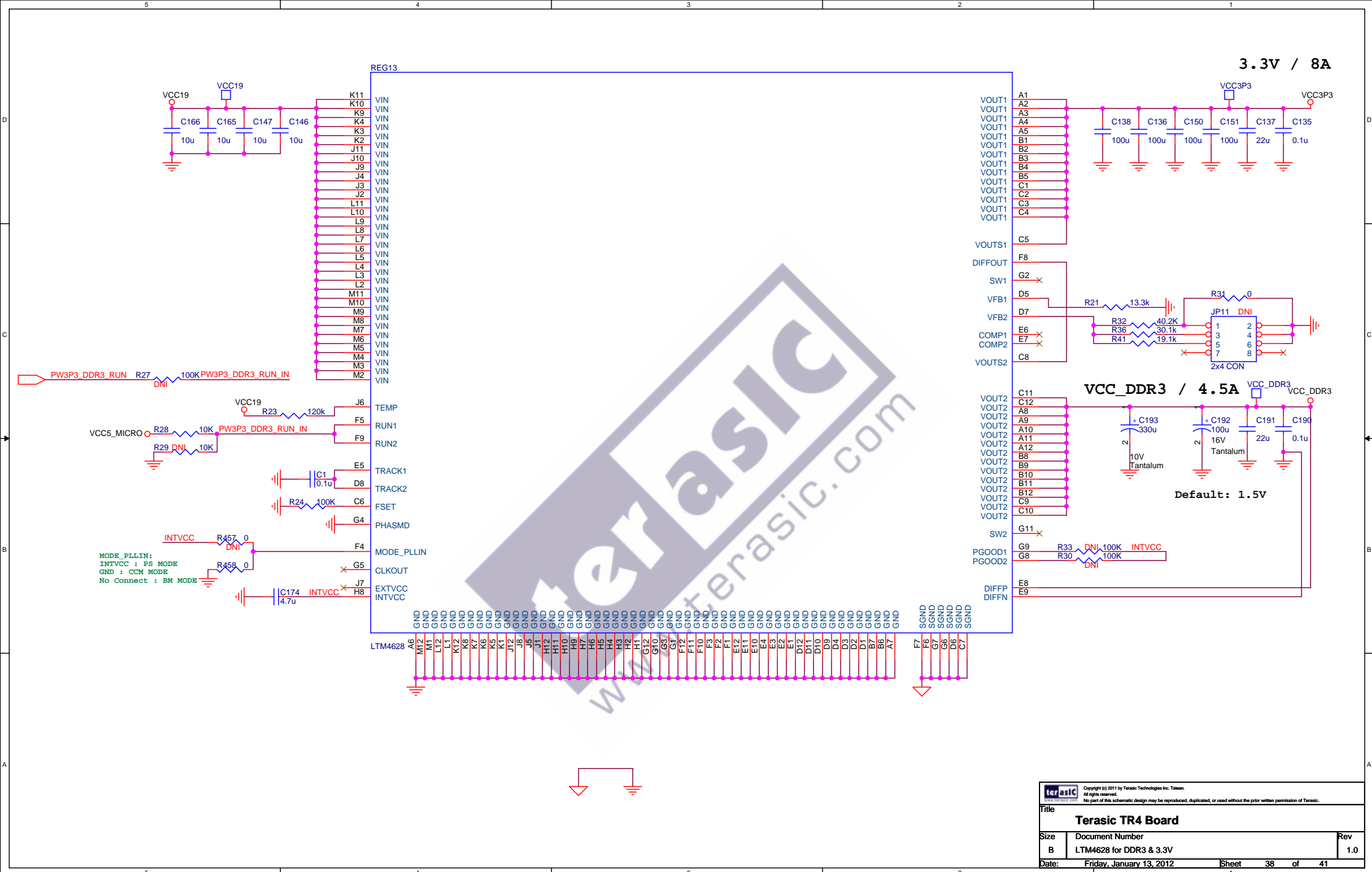


LTM4612

12V / 5A

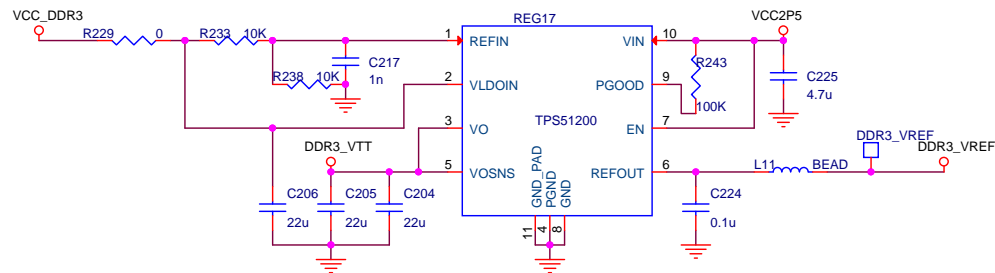




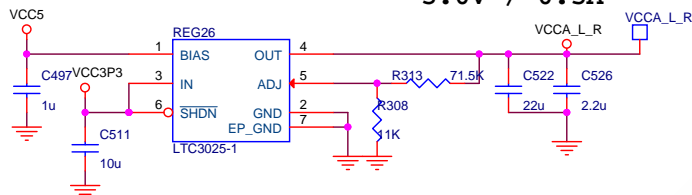




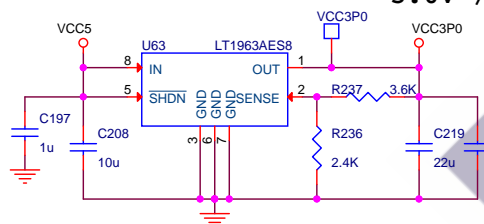
## DDR3 VTT, VREF



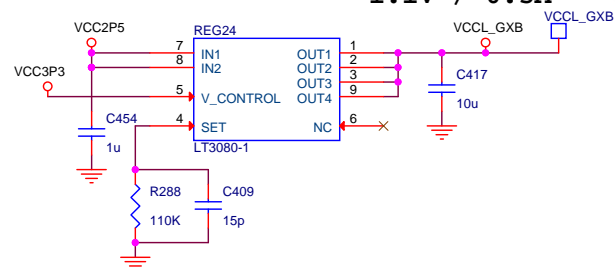
## 3.0V / 0.5A



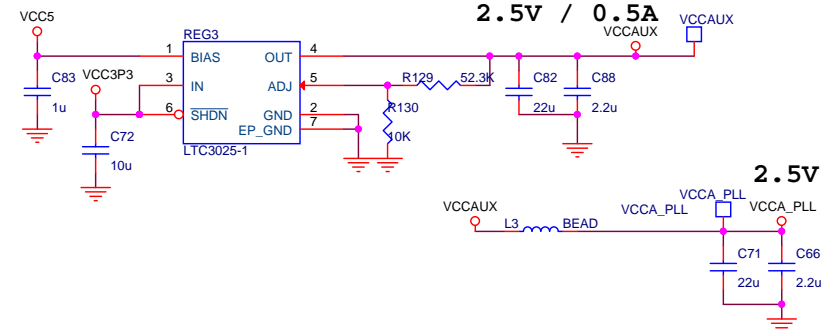
## 3.0V / 1.5A



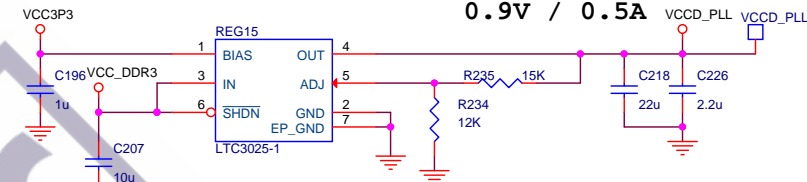
## 1.1V / 0.5A



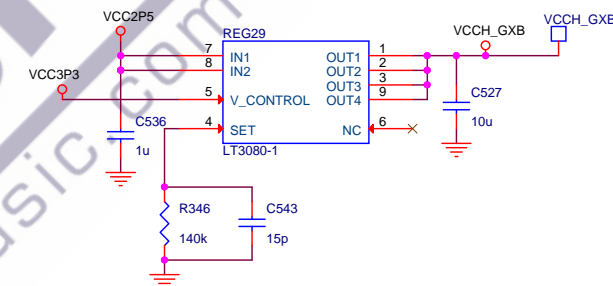
## 2.5V / 0.5A



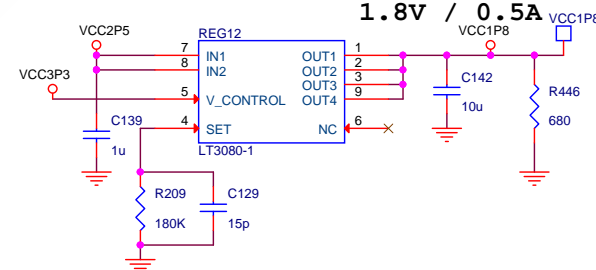
## 0.9V / 0.5A



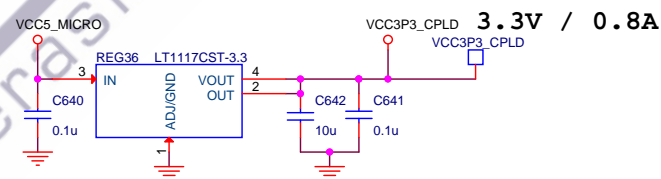
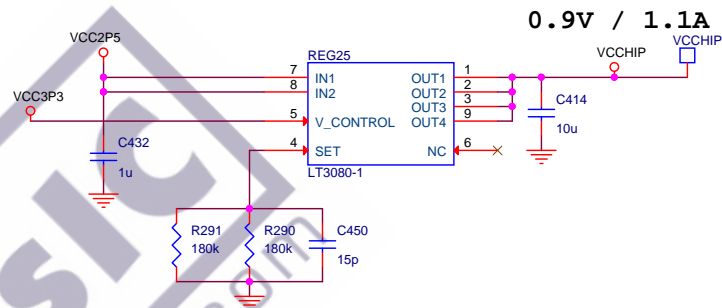
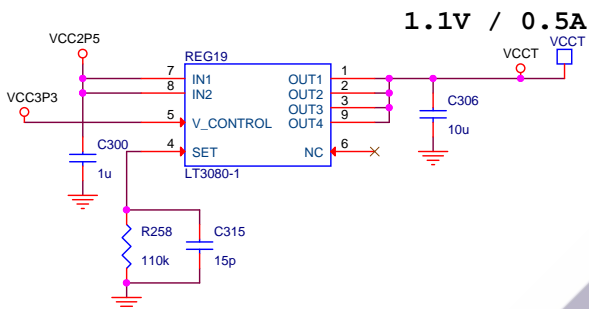
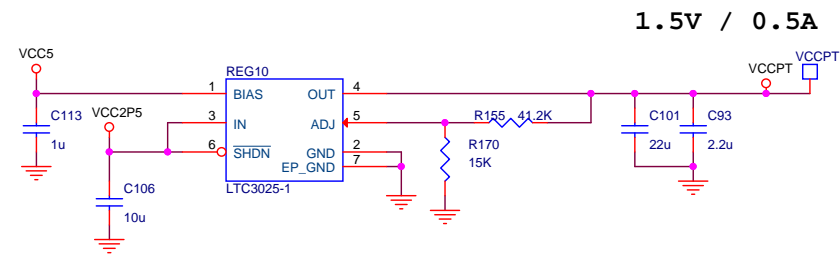
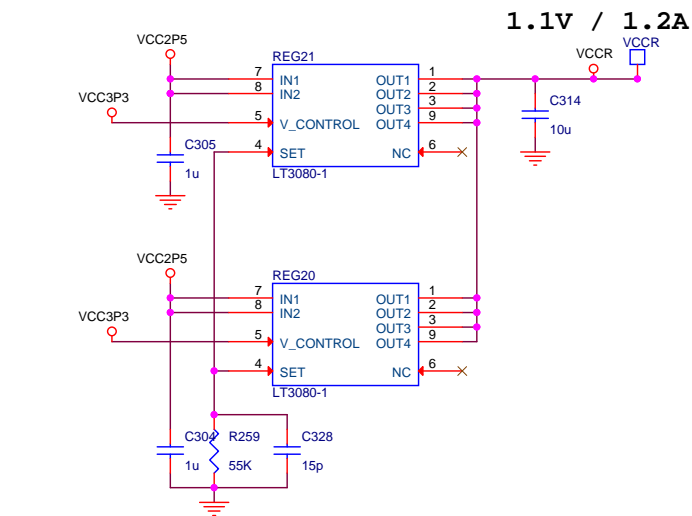
## 1.4V / 0.6A




## 1.8V / 0.5A

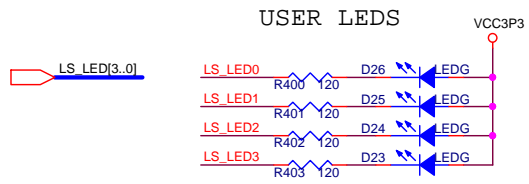


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Title		
Terasic TR4 Board		
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B	Others 1	1.0
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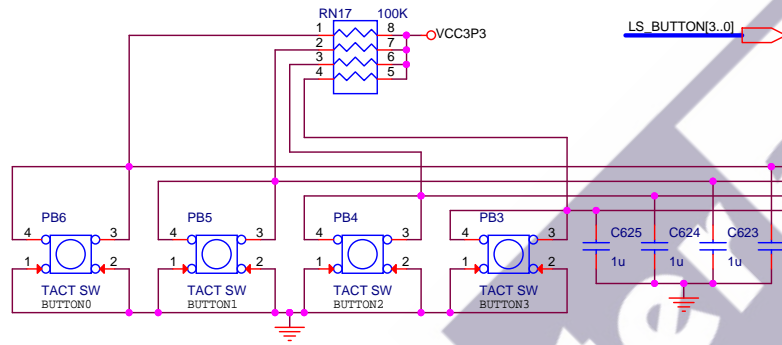


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Terasic TR4 Board		
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# USER LEDS



# USER PUSH BUTTON



LS\_BUTTON[3..0]

VCC3P3\_CPLD

R404 10K

PB2 CONFIG

C626 1u

VCC3P3\_CPLD

R405 10K

PB1 MAX\_RSTn

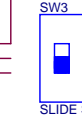
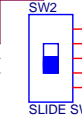
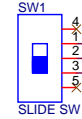
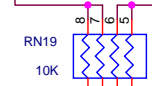
C627 1u

VCC3P3\_CPLD

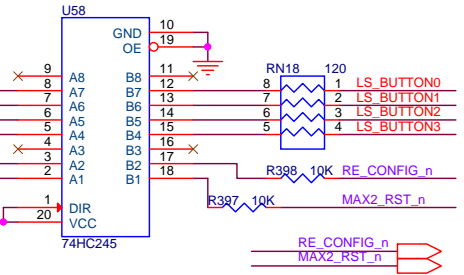
C614 0.1u

C613 0.1u

VCCIO\_HSMF VCCIO\_HSMA



SW[3..0]



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