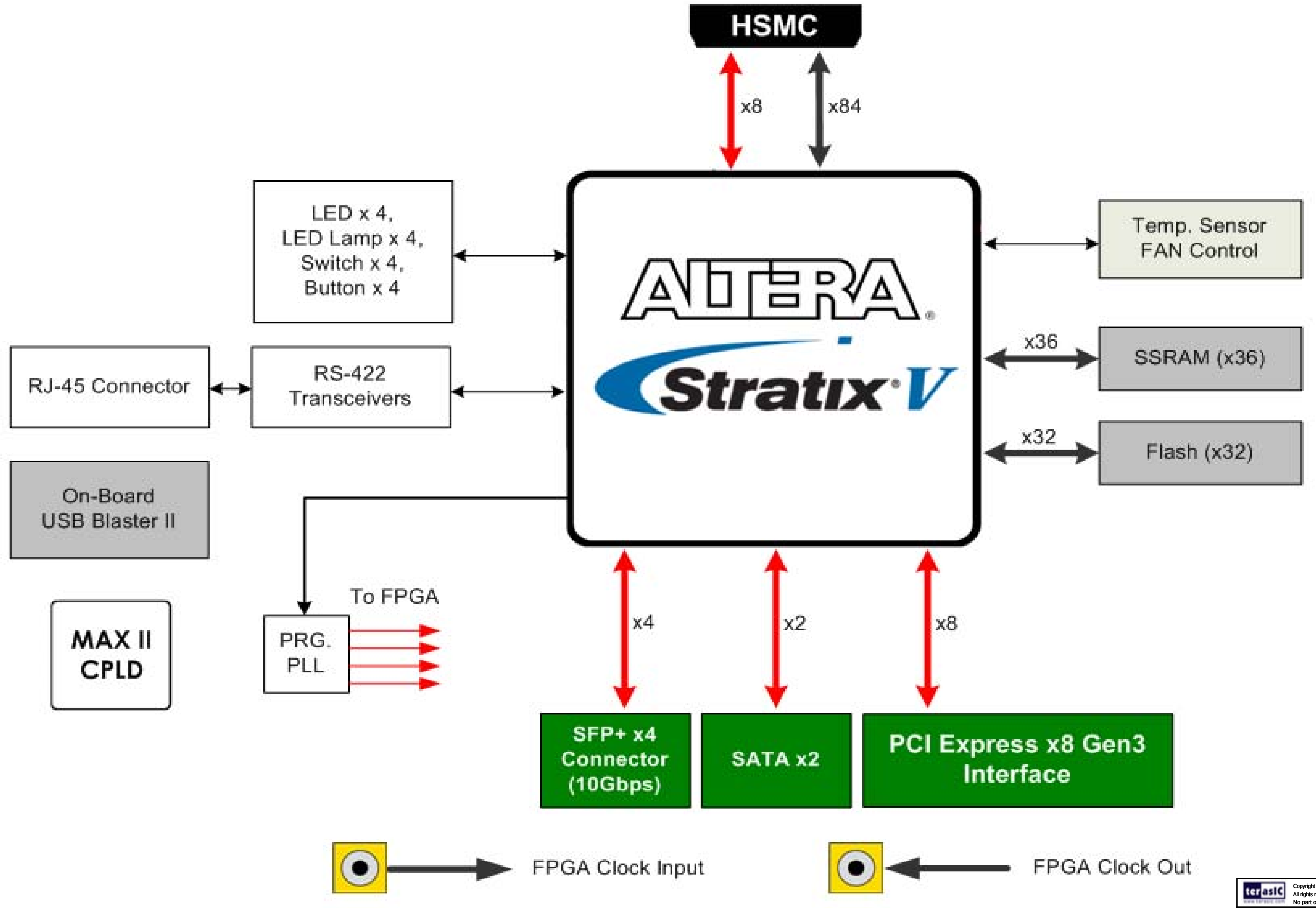
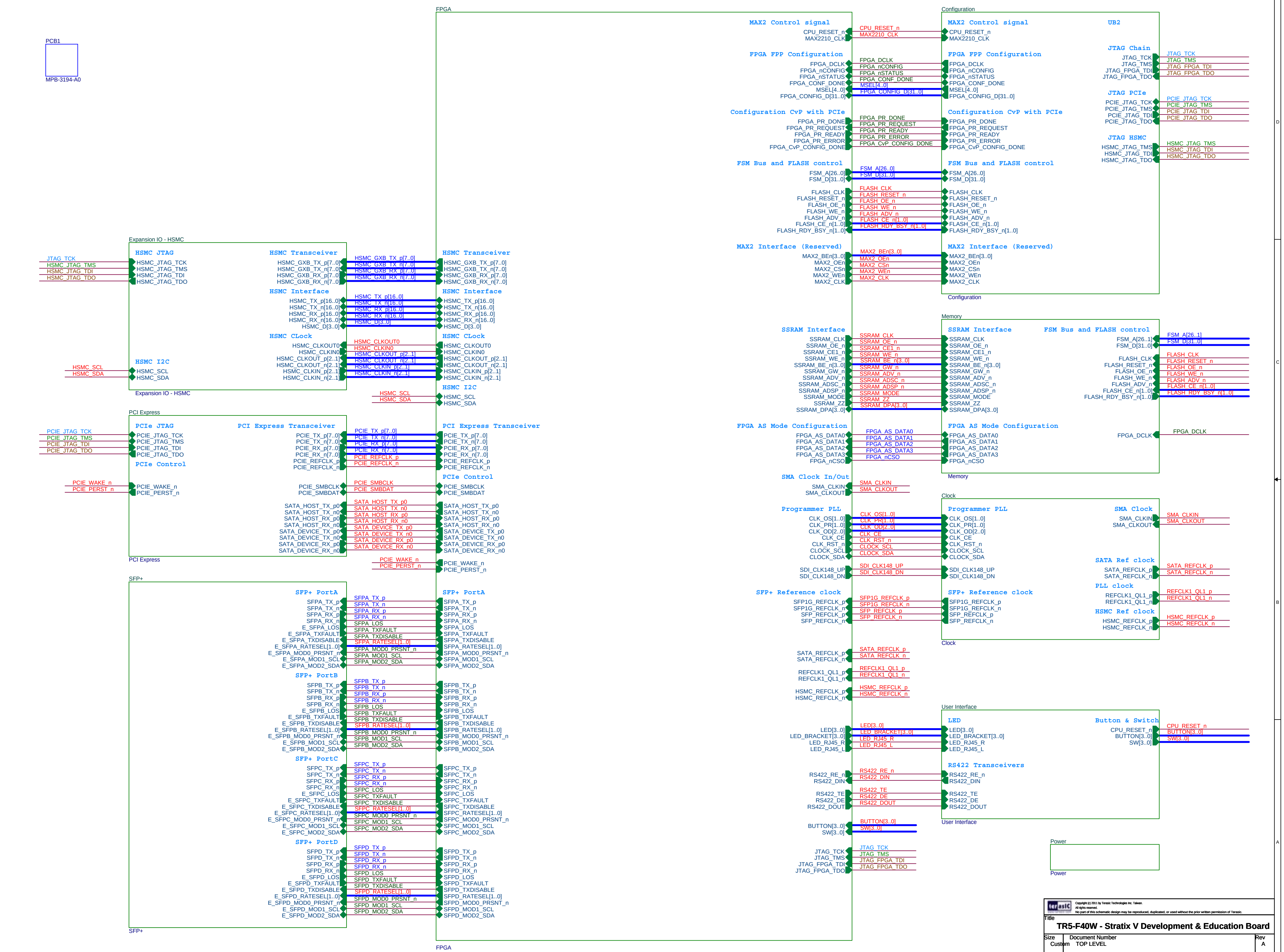
ALTERA Stratix V Development & Education Board (TR5-F40W)

Title	TR5-F40W - Stratix V Development & Education Board	
Size: B	Document Number: Cover Page	Rev: A
Date: Wednesday, July 11, 2012	Sheet 1 of 28	

Block Diagram



Title		
TR5-F40W - Stratix V Development & Education Board		
Size: B	Document Number: Block Diagram	Rev: A
Date: Thursday, July 12, 2012	Sheet 2 of 28	



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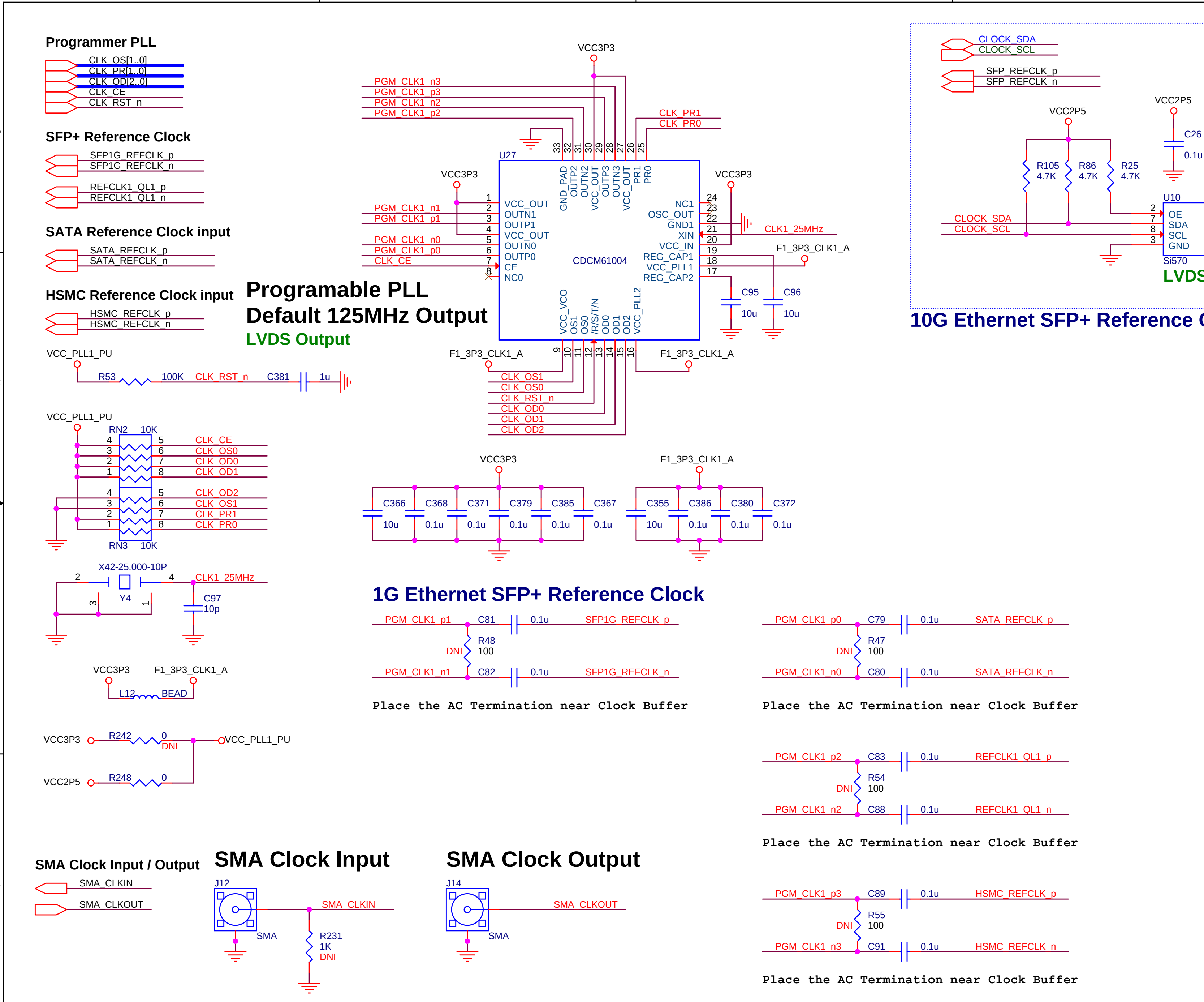
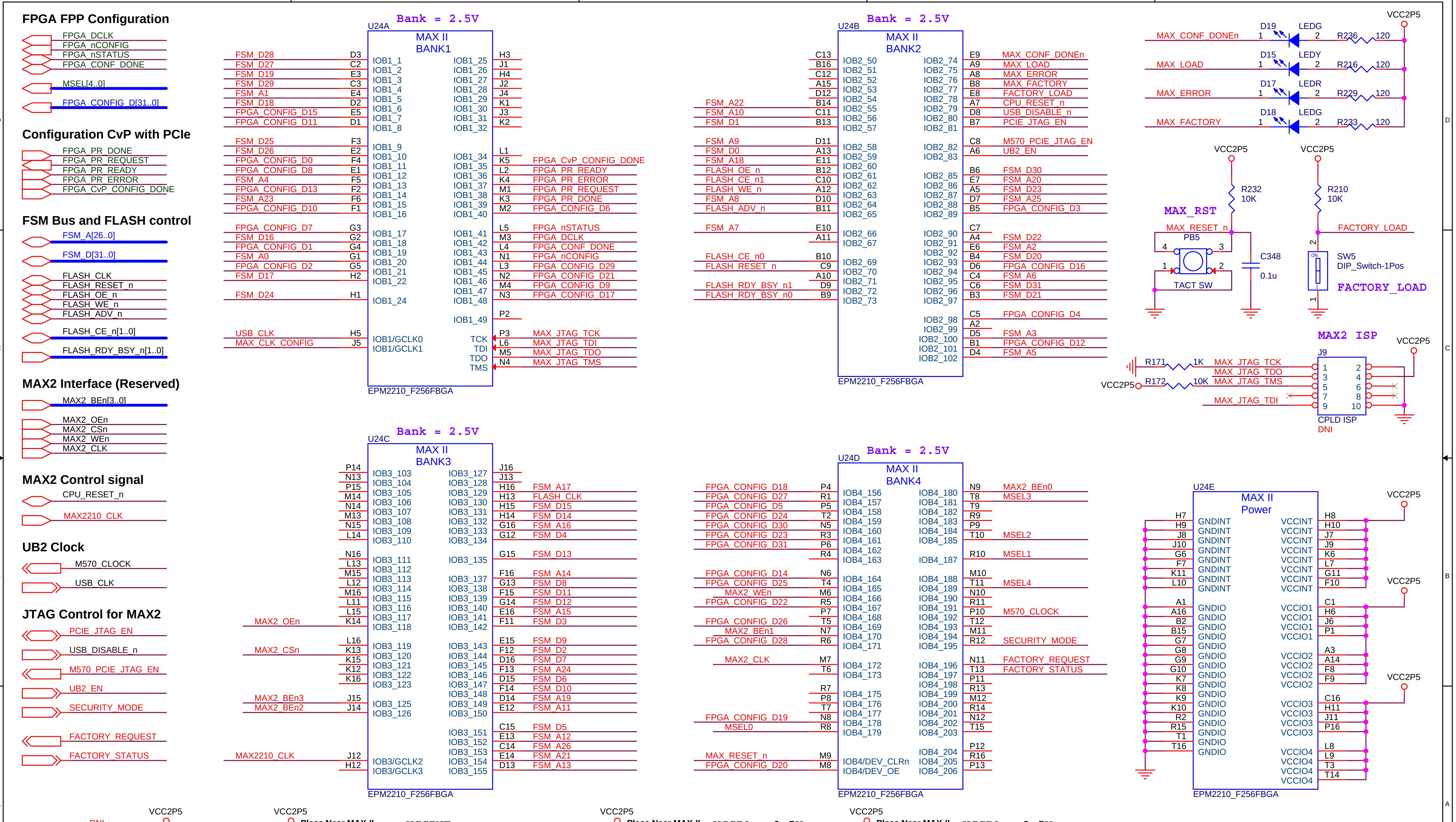
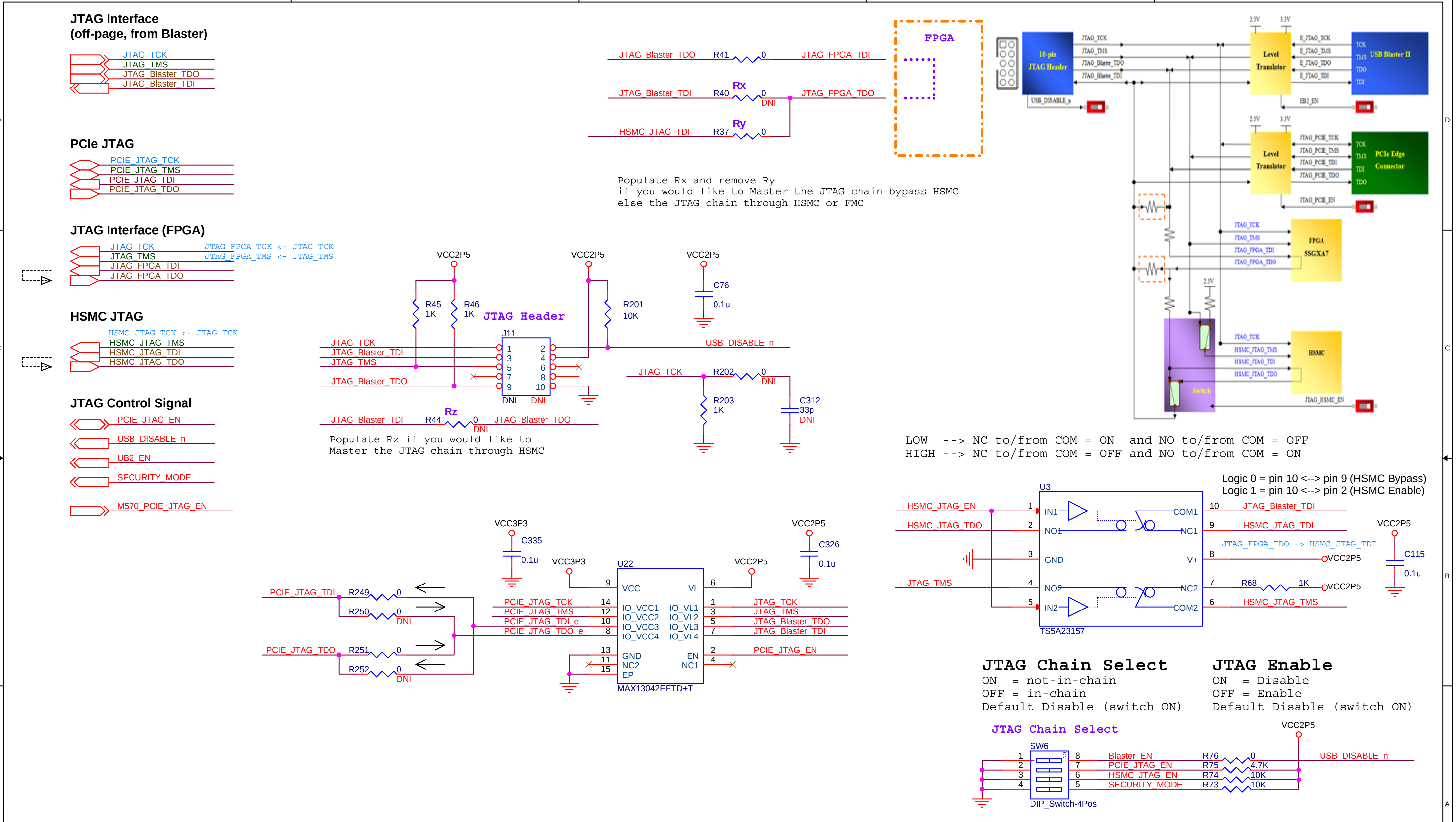
Title	TR5-F40W - Stratix V Development & Education Board		
Size: Custom	Document Number: TOP LEVEL		Rev: A
Date: Wednesday, July 11, 2012	Sheet 4 of 28		



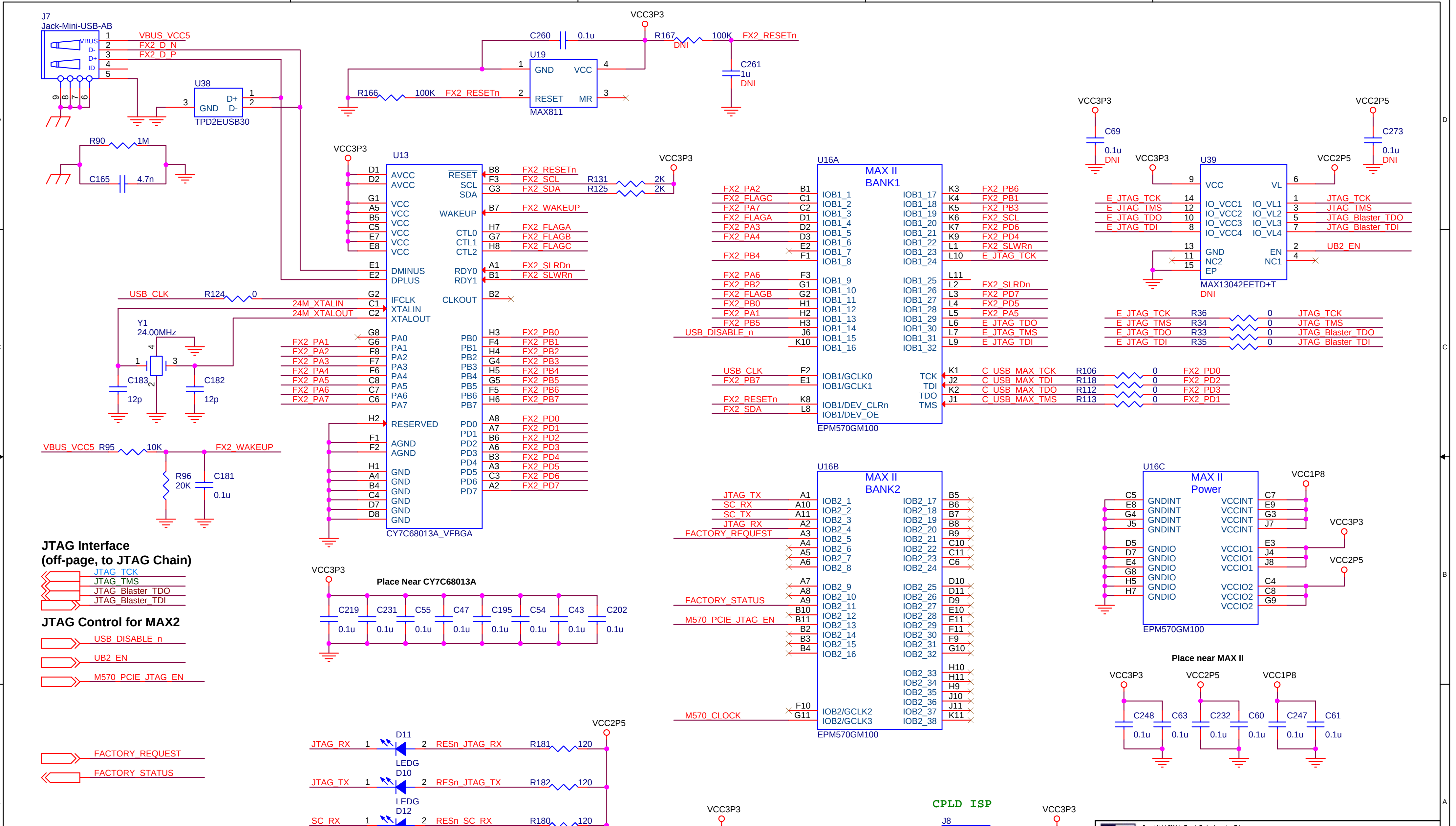
Title	TR5-F40W - Stratix V Development & Education Board	
Size B	Document Number: Programmable PLL Clock	Rev A
Date: Wednesday, July 11, 2012	Sheet 5 of 28	



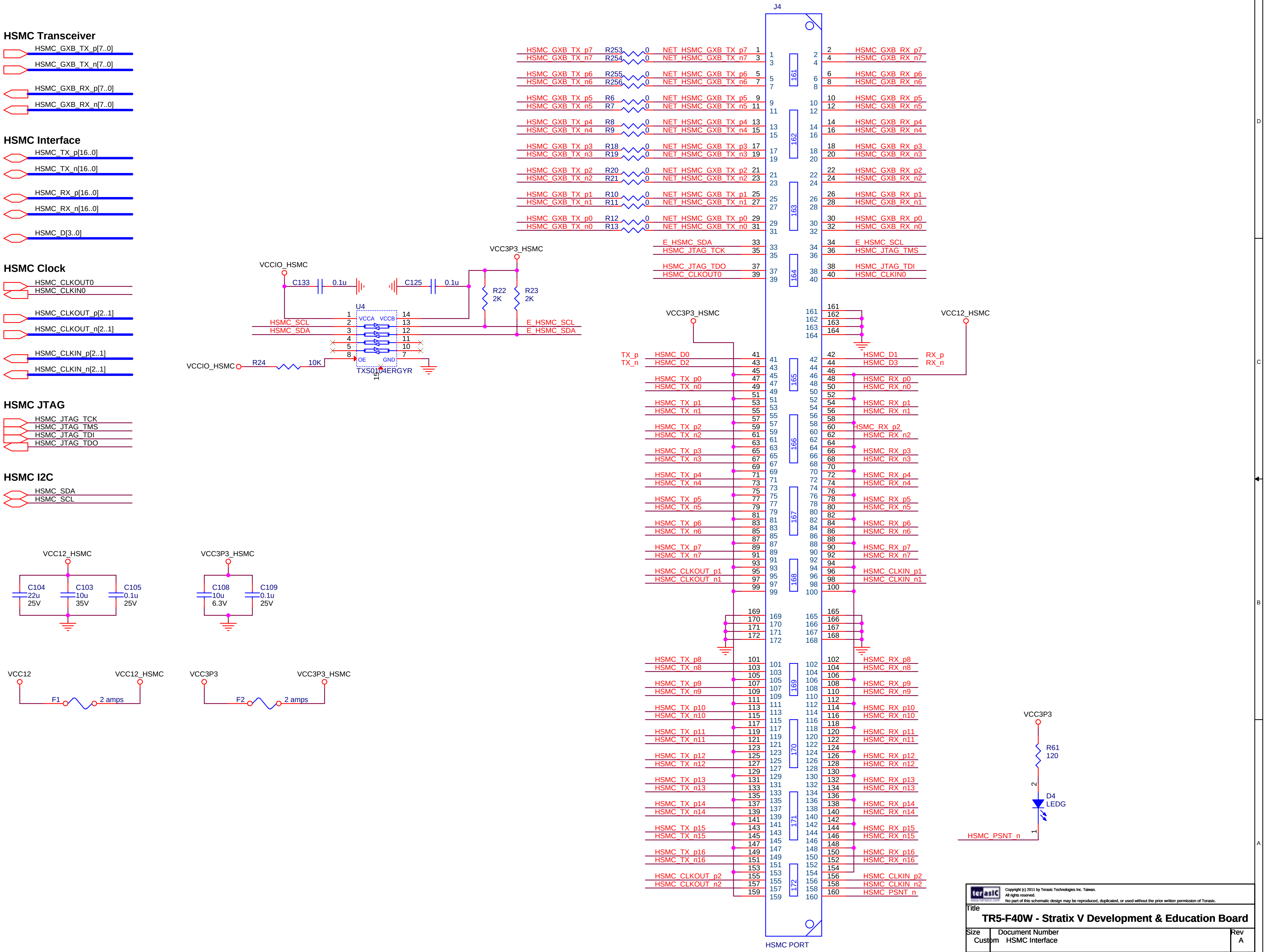
Title	TR5-F40W - Stratix V Development & Education Board	
Size B	Document Number EPM2210 Configuration	Rev A
Date: Wednesday, July 11, 2012	Sheet 6 of 28	



Title: TR5-F40W - Stratix V Development & Education Board		
Size: B	Document Number: JTAG Chain	Rev: A
Date: Thursday, July 12, 2012	Sheet 7 of 28	



Title		
TR5-F40W - Stratix V Development & Education Board		
Size: B	Document Number: USB Blaster II	Rev: A
Date: Thursday, July 12, 2012	Sheet 8 of 28	



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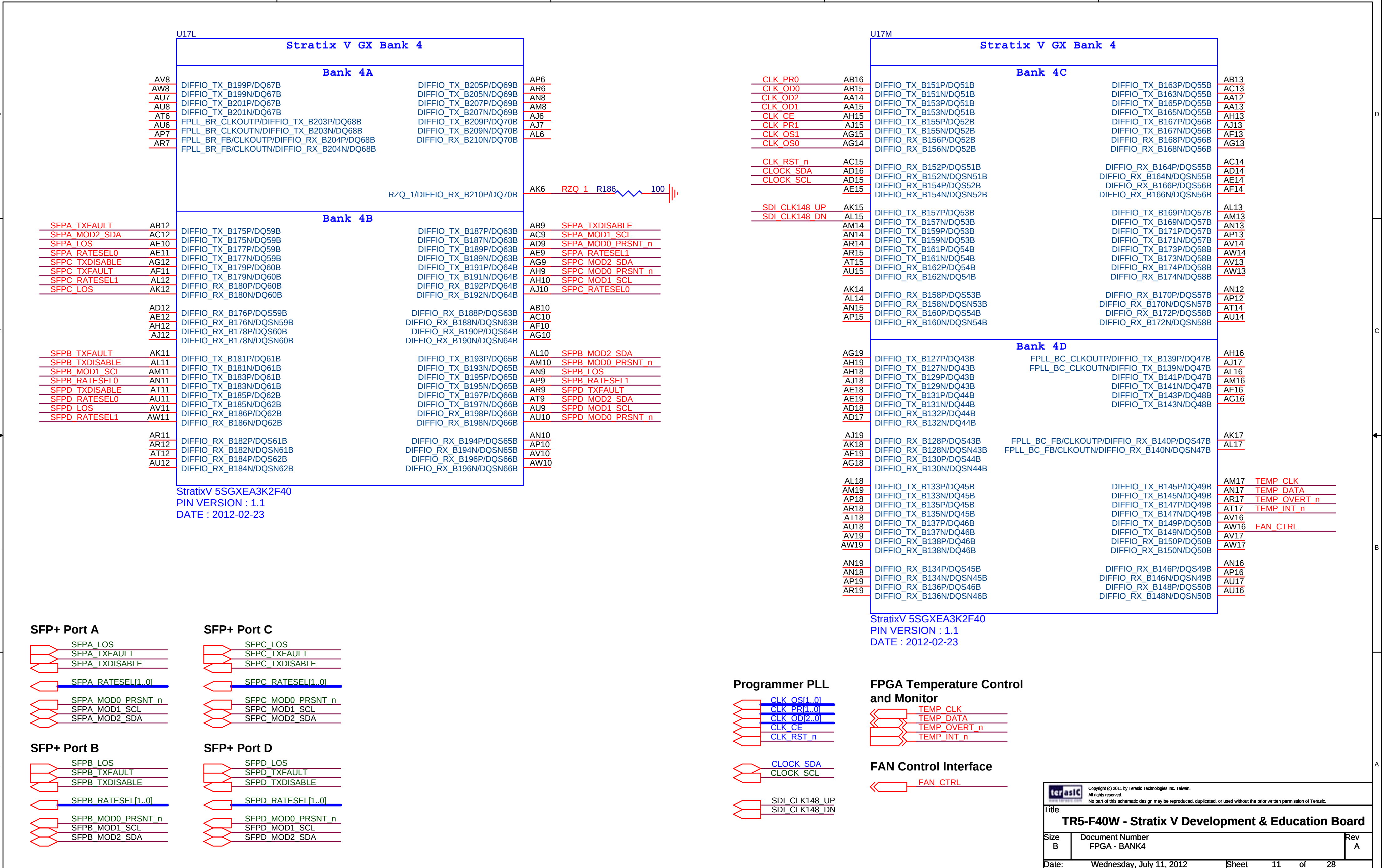
Title	TR5-F40W - Stratix V Development & Education Board	
Size: Custom	Document Number: HSMC Interface	Rev: A
Date: Wednesday, July 11, 2012	Sheet 9 of 28	

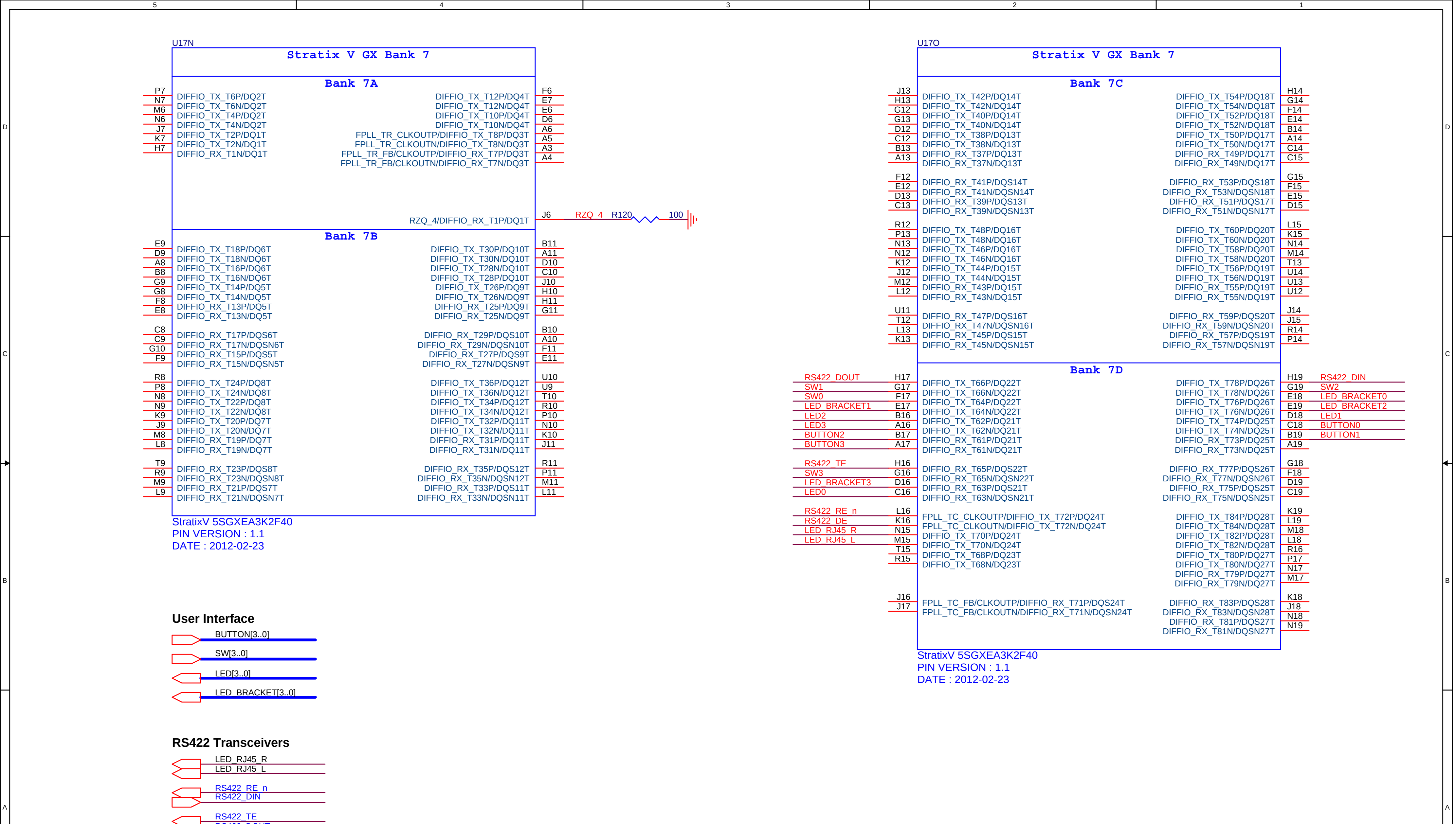
Title: **TR5-F40W - Stratix V Development & Education Board**

Size	Document Number	Rev
B	FPGA - BANK3	A

Date: Wednesday, July 11, 2012 — Sheet 10 of 28



Title	TR5-F40W - Stratix V Development & Education Board	
Size B	Document Number FPGA - BANK4	Rev A
Date: Wednesday, July 11, 2012	Sheet 11 of 28	



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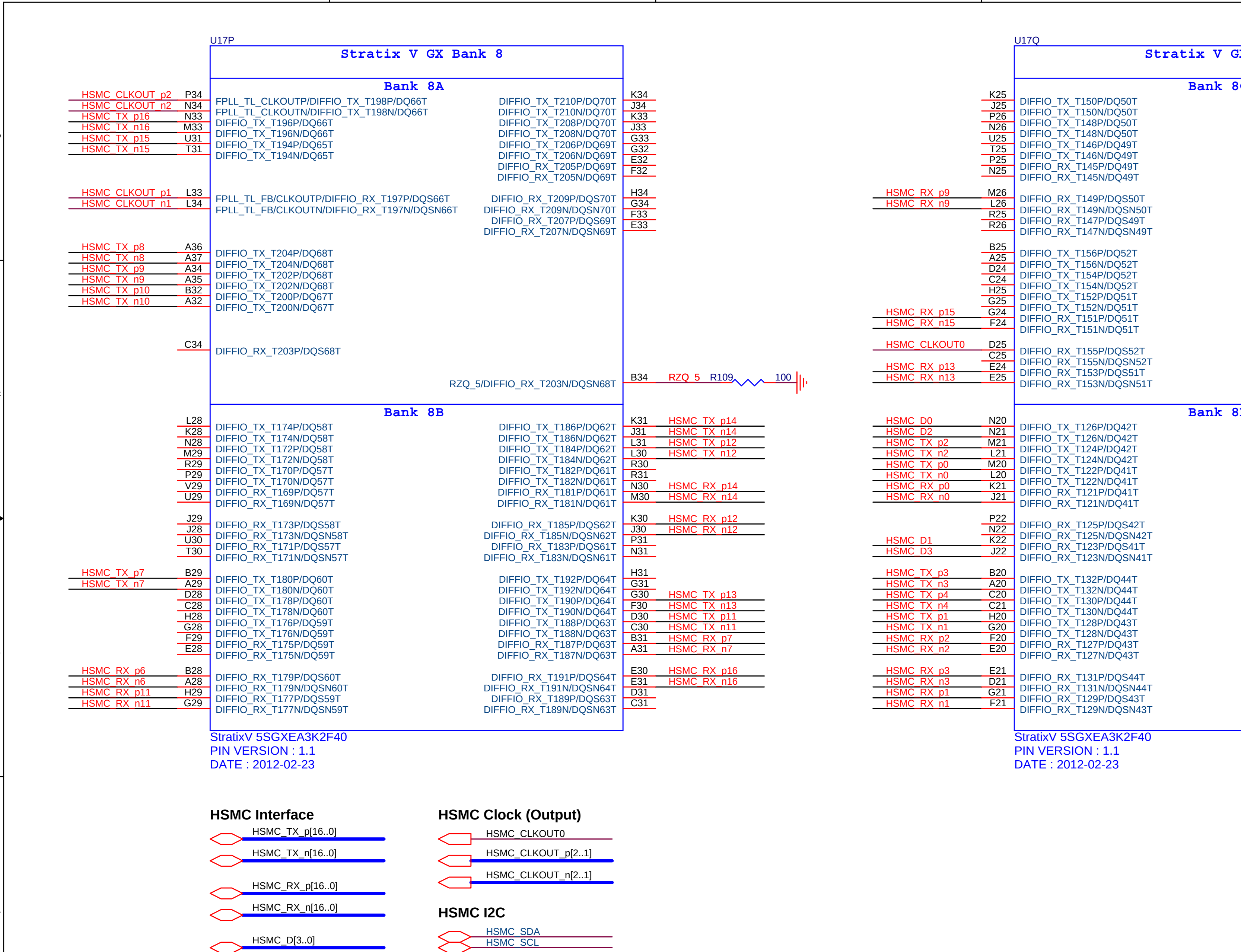
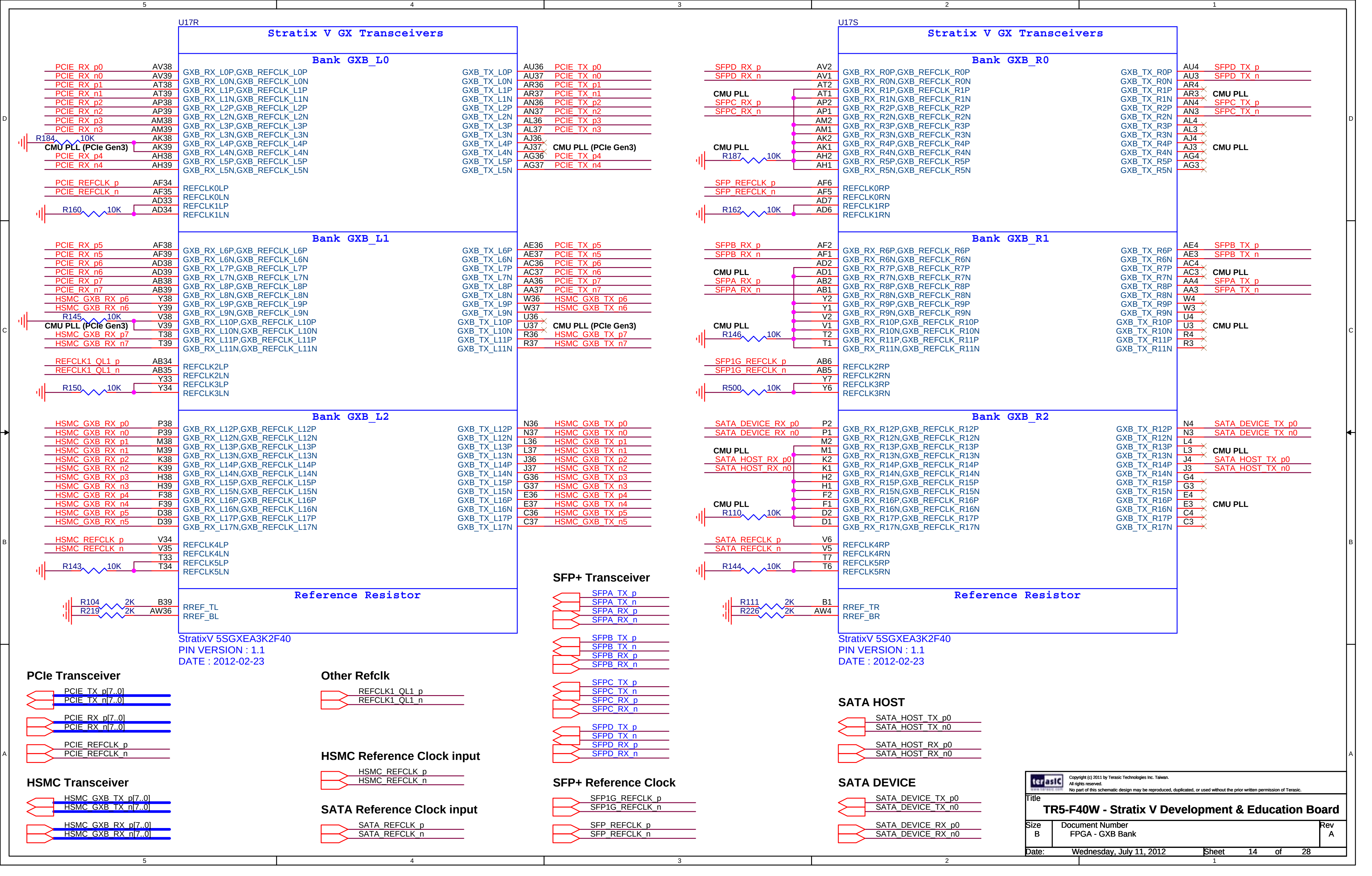
Title		
TR5-F40W - Stratix V Development & Education Board		
Size: B	Document Number: FPGA - BANK7	Rev: A
Date: Wednesday, July 11, 2012	Sheet 12 of 28	



Title: **TR5-F40W - Stratix V Development & Education Board**

Size	Document Number	Rev
B	FPGA - BANK8	A

Date: Thursday, July 12, 2012 — Sheet 13 of 28


U17R
Stratix V GX Transceivers
Bank GXB_L0
PCIE_RX_p0 AV38 GXB_RX_L0P,GXB_REFCLK_L0P
PCIE_RX_n0 AV39 GXB_RX_L0N,GXB_REFCLK_L0N
PCIE_RX_p1 AT38 GXB_RX_L1P,GXB_REFCLK_L1P
PCIE_RX_n1 AT39 GXB_RX_L1N,GXB_REFCLK_L1N
PCIE_RX_p2 AP38 GXB_RX_L2P,GXB_REFCLK_L2P
PCIE_RX_n2 AP39 GXB_RX_L2N,GXB_REFCLK_L2N
PCIE_RX_p3 AM38 GXB_RX_L3P,GXB_REFCLK_L3P
PCIE_RX_n3 AM39 GXB_RX_L3N,GXB_REFCLK_L3N
R184 10K AK38 GXB_RX_L4P,GXB_REFCLK_L4P
CMU PLL (PCIe Gen3) AK39 GXB_RX_L4N,GXB_REFCLK_L4N
PCIE_RX_p4 AH38 GXB_RX_L5P,GXB_REFCLK_L5P
PCIE_RX_n4 AH39 GXB_RX_L5N,GXB_REFCLK_L5N
GXB_TX_L0P AU36 PCIE_TX_p0
GXB_TX_L0N AU37 PCIE_TX_n0
GXB_TX_L1P AR36 PCIE_TX_p1
GXB_TX_L1N AR37 PCIE_TX_n1
GXB_TX_L2P AN36 PCIE_TX_p2
GXB_TX_L2N AN37 PCIE_TX_n2
GXB_TX_L3P AL36 PCIE_TX_p3
GXB_TX_L3N AL37 PCIE_TX_n3
GXB_TX_L4P AJ36
GXB_TX_L4N AJ37 CMU PLL (PCIe Gen3)
GXB_TX_L5P AG36 PCIE_TX_p4
GXB_TX_L5N AG37 PCIE_TX_n4
PCIE_REFCLK_p AF34 REFCLK0LP
PCIE_REFCLK_n AF35 REFCLK0LN
AD33 REFCLK1LP
R160 10K AD34 REFCLK1LN
Bank GXB_L1
PCIE_RX_p5 AF38 GXB_RX_L6P,GXB_REFCLK_L6P
PCIE_RX_n5 AF39 GXB_RX_L6N,GXB_REFCLK_L6N
PCIE_RX_p6 AD38 GXB_RX_L7P,GXB_REFCLK_L7P
PCIE_RX_n6 AD39 GXB_RX_L7N,GXB_REFCLK_L7N
PCIE_RX_p7 AB38 GXB_RX_L8P,GXB_REFCLK_L8P
PCIE_RX_n7 AB39 GXB_RX_L8N,GXB_REFCLK_L8N
HSMC_GXB_RX_p6 Y38 GXB_RX_L9P,GXB_REFCLK_L9P
HSMC_GXB_RX_n6 Y39 GXB_RX_L9N,GXB_REFCLK_L9N
R145 10K V38 GXB_RX_L10P,GXB_REFCLK_L10P
CMU PLL (PCIe Gen3) V39 GXB_RX_L10N,GXB_REFCLK_L10N
HSMC_GXB_RX_p7 T38 GXB_RX_L11P,GXB_REFCLK_L11P
HSMC_GXB_RX_n7 T39 GXB_RX_L11N,GXB_REFCLK_L11N
GXB_TX_L6P AE36 PCIE_TX_p5
GXB_TX_L6N AE37 PCIE_TX_n5
GXB_TX_L7P AC36 PCIE_TX_p6
GXB_TX_L7N AC37 PCIE_TX_n6
GXB_TX_L8P AA36 PCIE_TX_p7
GXB_TX_L8N AA37 PCIE_TX_n7
GXB_TX_L9P W36 HSMC_GXB_TX_p6
GXB_TX_L9N W37 HSMC_GXB_TX_n6
GXB_TX_L10P U36
GXB_TX_L10N U37 CMU PLL (PCIe Gen3)
GXB_TX_L11P R36 HSMC_GXB_TX_p7
GXB_TX_L11N R37 HSMC_GXB_TX_n7
REFCLK1_QL1_p AB34 REFCLK2LP
REFCLK1_QL1_n AB35 REFCLK2LN
Y33 REFCLK3LP
R150 10K Y34 REFCLK3LN
Bank GXB_L2
HSMC_GXB_RX_p0 P38 GXB_RX_L12P,GXB_REFCLK_L12P
HSMC_GXB_RX_n0 P39 GXB_RX_L12N,GXB_REFCLK_L12N
HSMC_GXB_RX_p1 M38 GXB_RX_L13P,GXB_REFCLK_L13P
HSMC_GXB_RX_n1 M39 GXB_RX_L13N,GXB_REFCLK_L13N
HSMC_GXB_RX_p2 K38 GXB_RX_L14P,GXB_REFCLK_L14P
HSMC_GXB_RX_n2 K39 GXB_RX_L14N,GXB_REFCLK_L14N
HSMC_GXB_RX_p3 H38 GXB_RX_L15P,GXB_REFCLK_L15P
HSMC_GXB_RX_n3 H39 GXB_RX_L15N,GXB_REFCLK_L15N
HSMC_GXB_RX_p4 F38 GXB_RX_L16P,GXB_REFCLK_L16P
HSMC_GXB_RX_n4 F39 GXB_RX_L16N,GXB_REFCLK_L16N
HSMC_GXB_RX_p5 D38 GXB_RX_L17P,GXB_REFCLK_L17P
HSMC_GXB_RX_n5 D39 GXB_RX_L17N,GXB_REFCLK_L17N
GXB_TX_L12P N36 HSMC_GXB_TX_p0
GXB_TX_L12N N37 HSMC_GXB_TX_n0
GXB_TX_L13P L36 HSMC_GXB_TX_p1
GXB_TX_L13N L37 HSMC_GXB_TX_n1
GXB_TX_L14P J36 HSMC_GXB_TX_p2
GXB_TX_L14N J37 HSMC_GXB_TX_n2
GXB_TX_L15P G36 HSMC_GXB_TX_p3
GXB_TX_L15N G37 HSMC_GXB_TX_n3
GXB_TX_L16P E36 HSMC_GXB_TX_p4
GXB_TX_L16N E37 HSMC_GXB_TX_n4
GXB_TX_L17P C36 HSMC_GXB_TX_p5
GXB_TX_L17N C37 HSMC_GXB_TX_n5
HSMC_REFCLK_p V34 REFCLK4LP
HSMC_REFCLK_n V35 REFCLK4LN
T33 REFCLK5LP
R143 10K T34 REFCLK5LN
Reference Resistor
R104 2K B39 RREF_TL
R219 2K AW36 RREF_BL
StratixV 5SGXEA3K2F40
PIN VERSION : 1.1
DATE : 2012-02-23
U17S
Stratix V GX Transceivers
Bank GXB_R0
SFPD_RX_p AV2 GXB_RX_R0P,GXB_REFCLK_R0P
SFPD_RX_n AV1 GXB_RX_R0N,GXB_REFCLK_R0N
AT2 GXB_RX_R1P,GXB_REFCLK_R1P
CMU PLL AT1 GXB_RX_R1N,GXB_REFCLK_R1N
SFPC_RX_p AP2 GXB_RX_R2P,GXB_REFCLK_R2P
SFPC_RX_n AP1 GXB_RX_R2N,GXB_REFCLK_R2N
AM2 GXB_RX_R3P,GXB_REFCLK_R3P
AM1 GXB_RX_R3N,GXB_REFCLK_R3N
AK2 GXB_RX_R4P,GXB_REFCLK_R4P
CMU PLL AK1 GXB_RX_R4N,GXB_REFCLK_R4N
R187 10K AH2 GXB_RX_R5P,GXB_REFCLK_R5P
AH1 GXB_RX_R5N,GXB_REFCLK_R5N
GXB_TX_R0P AU4 SFPD_TX_p
GXB_TX_R0N AU3 SFPD_TX_n
GXB_TX_R1P AR4
GXB_TX_R1N AR3 CMU PLL
GXB_TX_R2P AN4 SFPC_TX_p
GXB_TX_R2N AN3 SFPC_TX_n
GXB_TX_R3P AL4
GXB_TX_R3N AL3
GXB_TX_R4P AJ4
GXB_TX_R4N AJ3 CMU PLL
GXB_TX_R5P AG4
GXB_TX_R5N AG3
SFP_REFCLK_p AF6 REFCLK0RP
SFP_REFCLK_n AF5 REFCLK0RN
AD7 REFCLK1RP
R162 10K AD6 REFCLK1RN
Bank GXB_R1
SFPB_RX_p AF2 GXB_RX_R6P,GXB_REFCLK_R6P
SFPB_RX_n AF1 GXB_RX_R6N,GXB_REFCLK_R6N
AD2 GXB_RX_R7P,GXB_REFCLK_R7P
CMU PLL AD1 GXB_RX_R7N,GXB_REFCLK_R7N
SFPA_RX_p AB2 GXB_RX_R8P,GXB_REFCLK_R8P
SFPA_RX_n AB1 GXB_RX_R8N,GXB_REFCLK_R8N
Y2 GXB_RX_R9P,GXB_REFCLK_R9P
Y1 GXB_RX_R9N,GXB_REFCLK_R9N
V2 GXB_RX_R10P,GXB_REFCLK_R10P
CMU PLL V1 GXB_RX_R10N,GXB_REFCLK_R10N
R146 10K T2 GXB_RX_R11P,GXB_REFCLK_R11P
T1 GXB_RX_R11N,GXB_REFCLK_R11N
GXB_TX_R6P AE4 SFPB_TX_p
GXB_TX_R6N AE3 SFPB_TX_n
GXB_TX_R7P AC4
GXB_TX_R7N AC3 CMU PLL
GXB_TX_R8P AA4 SFPA_TX_p
GXB_TX_R8N AA3 SFPA_TX_n
GXB_TX_R9P W4
GXB_TX_R9N W3
GXB_TX_R10P U4
GXB_TX_R10N U3 CMU PLL
GXB_TX_R11P R4
GXB_TX_R11N R3
SFP1G_REFCLK_p AB6 REFCLK2RP
SFP1G_REFCLK_n AB5 REFCLK2RN
Y7 REFCLK3RP
R500 10K Y6 REFCLK3RN
Bank GXB_R2
SATA_DEVICE_RX_p0 P2 GXB_RX_R12P,GXB_REFCLK_R12P
SATA_DEVICE_RX_n0 P1 GXB_RX_R12N,GXB_REFCLK_R12N
M2 GXB_RX_R13P,GXB_REFCLK_R13P
CMU PLL M1 GXB_RX_R13N,GXB_REFCLK_R13N
SATA_HOST_RX_p0 K2 GXB_RX_R14P,GXB_REFCLK_R14P
SATA_HOST_RX_n0 K1 GXB_RX_R14N,GXB_REFCLK_R14N
H2 GXB_RX_R15P,GXB_REFCLK_R15P
H1 GXB_RX_R15N,GXB_REFCLK_R15N
F2 GXB_RX_R16P,GXB_REFCLK_R16P
CMU PLL F1 GXB_RX_R16N,GXB_REFCLK_R16N
R110 10K D2 GXB_RX_R17P,GXB_REFCLK_R17P
D1 GXB_RX_R17N,GXB_REFCLK_R17N
GXB_TX_R12P N4 SATA_DEVICE_TX_p0
GXB_TX_R12N N3 SATA_DEVICE_TX_n0
GXB_TX_R13P L4
GXB_TX_R13N L3 CMU PLL
GXB_TX_R14P J4 SATA_HOST_TX_p0
GXB_TX_R14N J3 SATA_HOST_TX_n0
GXB_TX_R15P G4
GXB_TX_R15N G3
GXB_TX_R16P E4
GXB_TX_R16N E3 CMU PLL
GXB_TX_R17P C4
GXB_TX_R17N C3
SATA_REFCLK_p V6 REFCLK4RP
SATA_REFCLK_n V5 REFCLK4RN
T7 REFCLK5RP
R144 10K T6 REFCLK5RN
Reference Resistor
R111 2K B1 RREF_TR
R226 2K AW4 RREF_BR
StratixV 5SGXEA3K2F40
PIN VERSION : 1.1
DATE : 2012-02-23
SFP+ Transceiver
SFPA_TX_p
SFPA_TX_n
SFPA_RX_p
SFPA_RX_n
SFPB_TX_p
SFPB_TX_n
SFPB_RX_p
SFPB_RX_n
SFPC_TX_p
SFPC_TX_n
SFPC_RX_p
SFPC_RX_n
SFPD_TX_p
SFPD_TX_n
SFPD_RX_p
SFPD_RX_n
PCIe Transceiver
PCIE_TX_p[7..0]
PCIE_TX_n[7..0]
PCIE_RX_p[7..0]
PCIE_RX_n[7..0]
PCIE_REFCLK_p
PCIE_REFCLK_n
Other Refclk
REFCLK1_QL1_p
REFCLK1_QL1_n
HSMC Reference Clock input
HSMC_REFCLK_p
HSMC_REFCLK_n
SATA Reference Clock input
SATA_REFCLK_p
SATA_REFCLK_n
HSMC Transceiver
HSMC_GXB_TX_p[7..0]
HSMC_GXB_TX_n[7..0]
HSMC_GXB_RX_p[7..0]
HSMC_GXB_RX_n[7..0]
SFP+ Reference Clock
SFP1G_REFCLK_p
SFP1G_REFCLK_n
SFP_REFCLK_p
SFP_REFCLK_n
SATA HOST
SATA_HOST_TX_p0
SATA_HOST_TX_n0
SATA_HOST_RX_p0
SATA_HOST_RX_n0
SATA DEVICE
SATA_DEVICE_TX_p0
SATA_DEVICE_TX_n0
SATA_DEVICE_RX_p0
SATA_DEVICE_RX_n0
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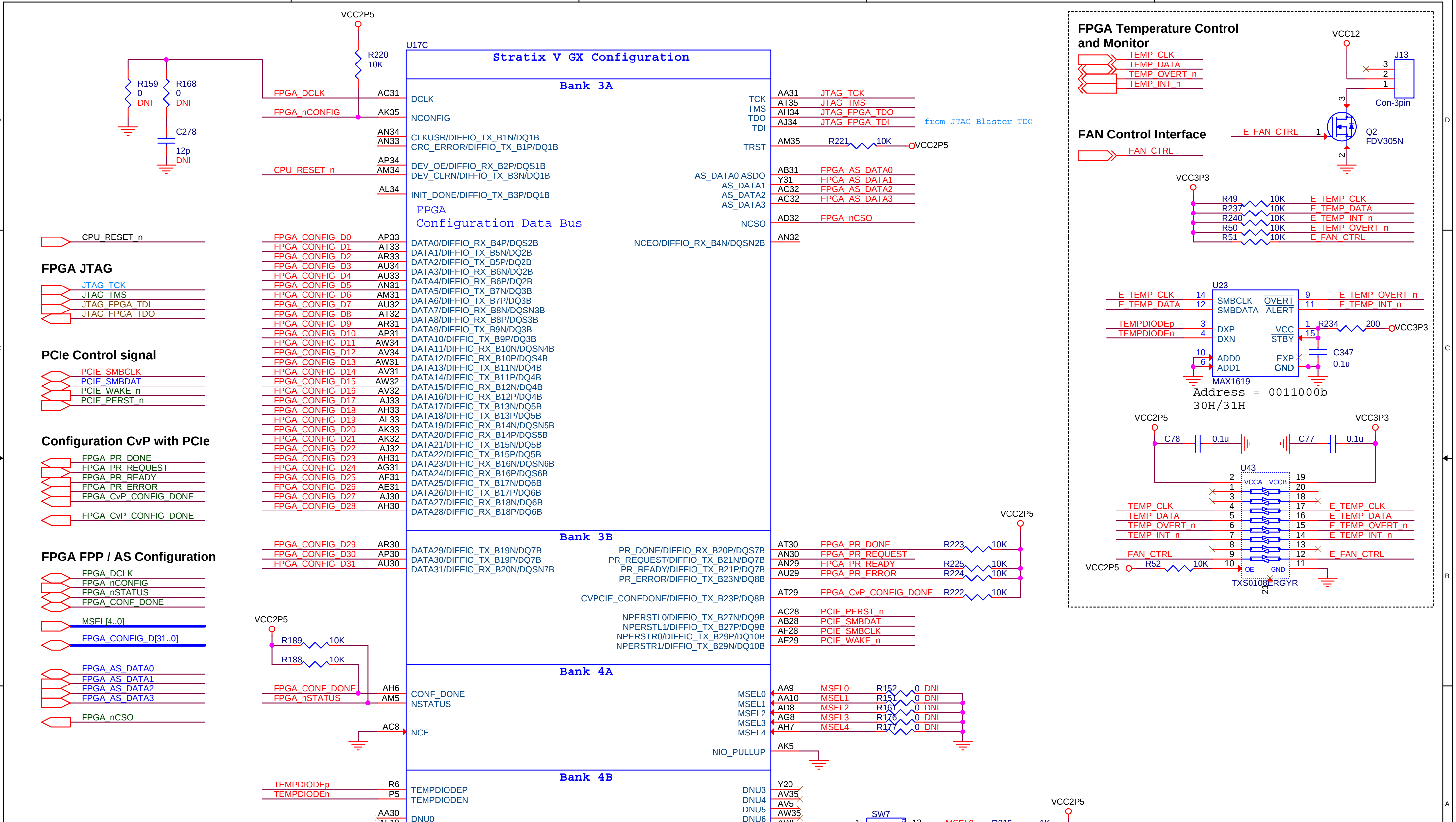
Title
TR5-F40W - Stratix V Development & Education Board
Size B
Document Number FPGA - GXB Bank
Rev A
Date: Wednesday, July 11, 2012
Sheet 14 of 28



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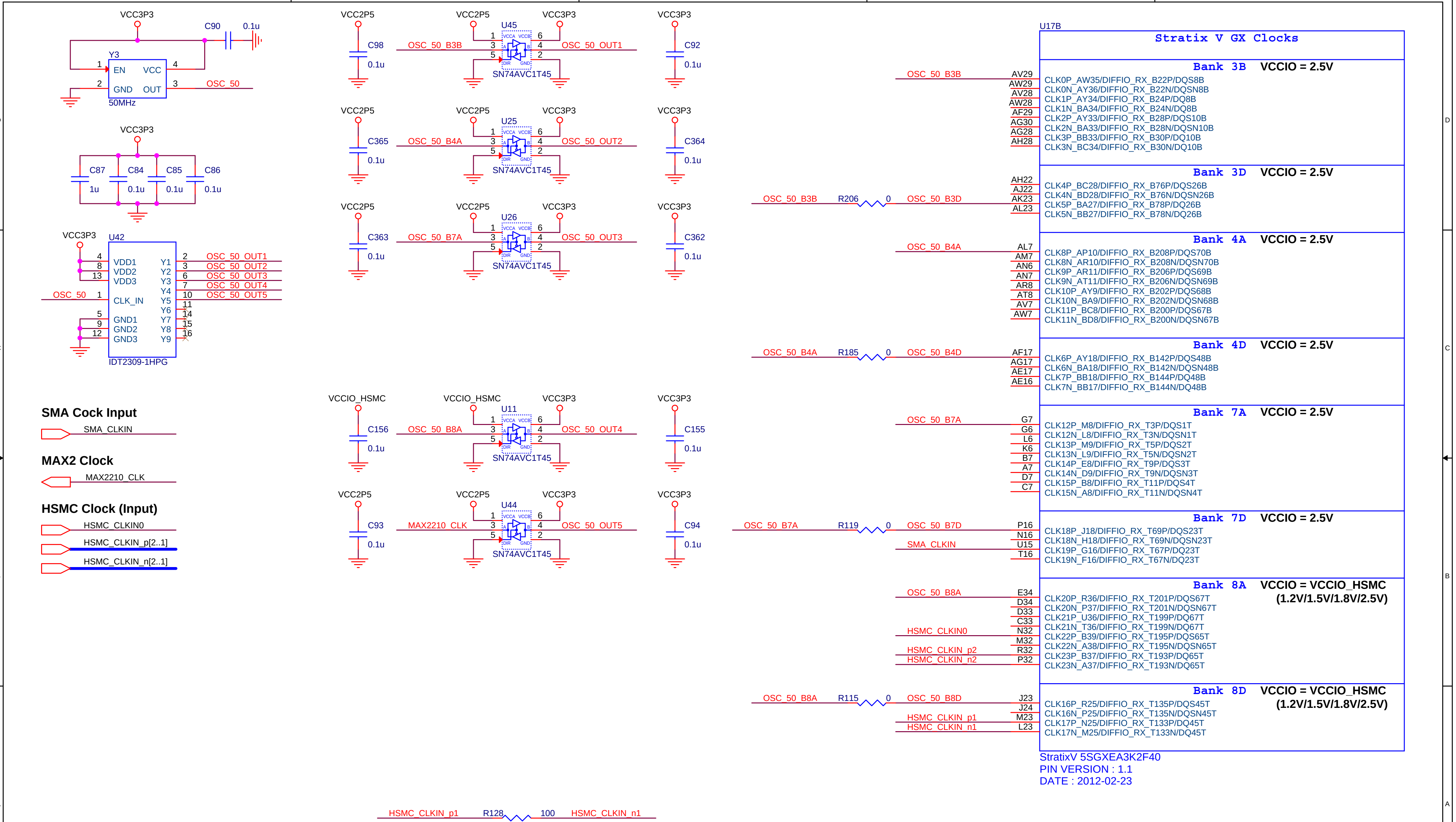
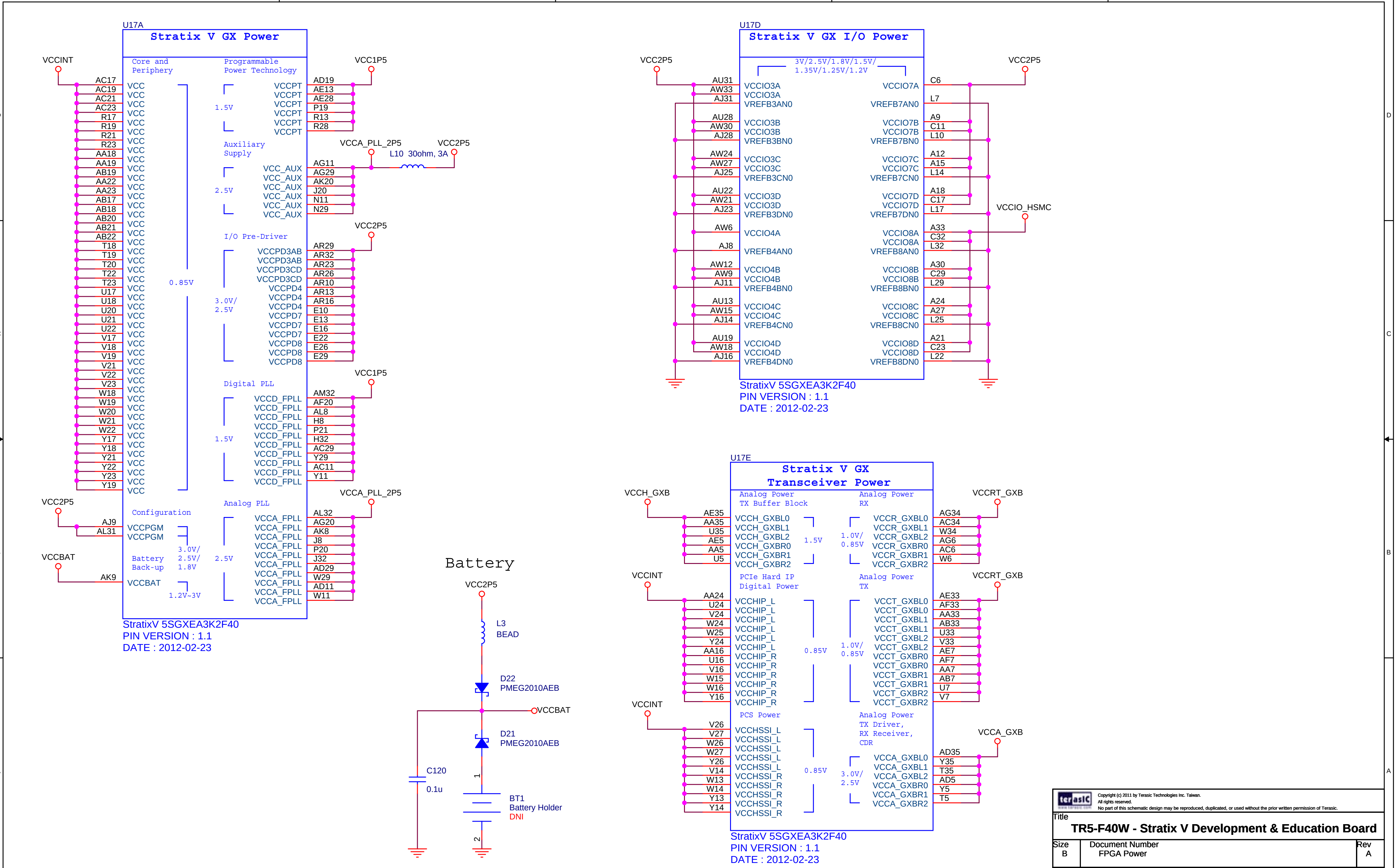
Title		
TR5-F40W - Stratix V Development & Education Board		
Size: B	Document Number: FPGA Configuration and Temperature	Rev: A
Date: Thursday, July 12, 2012	Sheet 15 of 28	



Title: **TR5-F40W - Stratix V Development & Education Board**

Size	Document Number	Rev
B	FPGA - Clock Bank	A

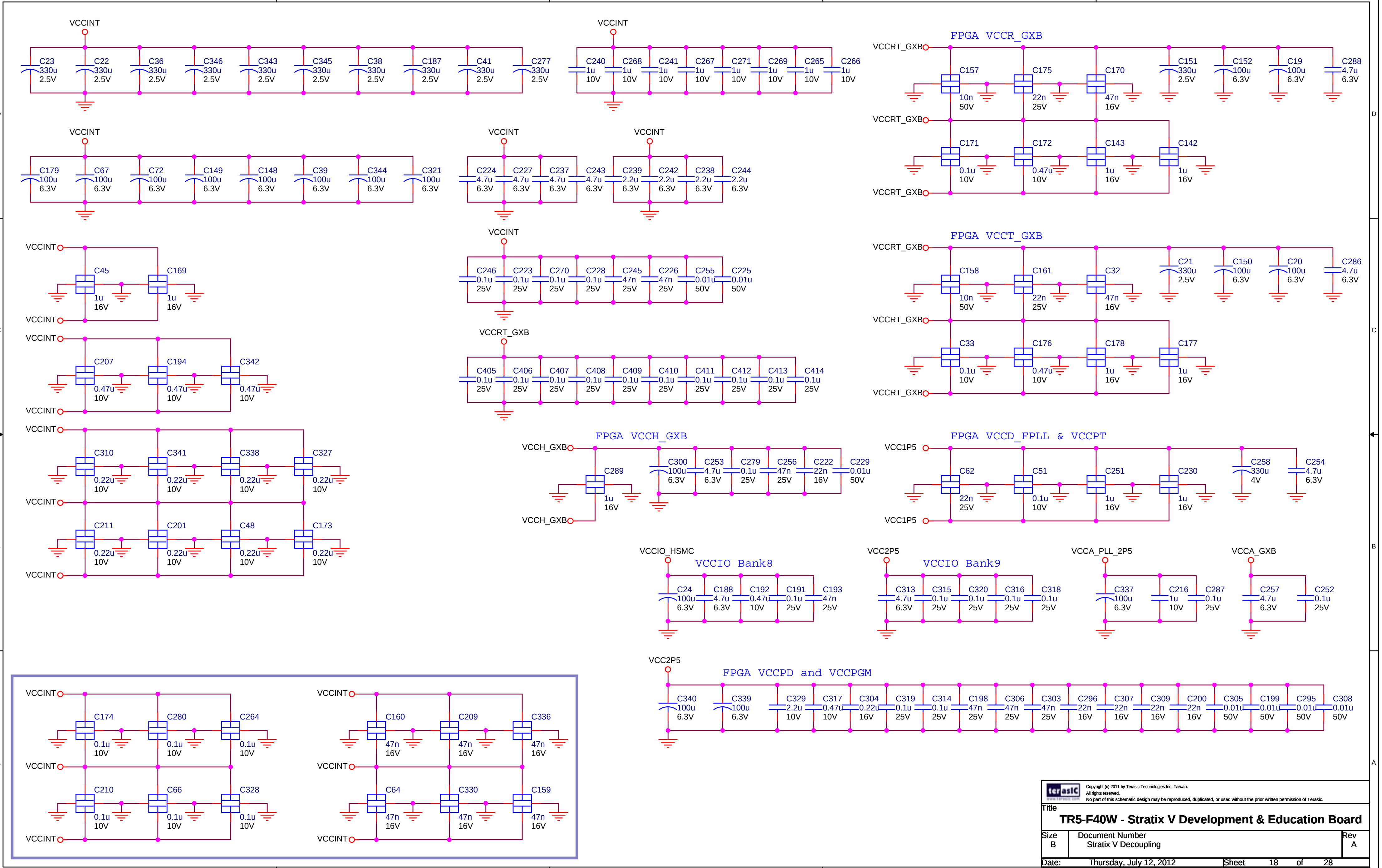
Date: Thursday, July 12, 2012 Sheet 16 of 28



Title: **TR5-F40W - Stratix V Development & Education Board**

Size	Document Number	Rev
B	FPGA Power	A

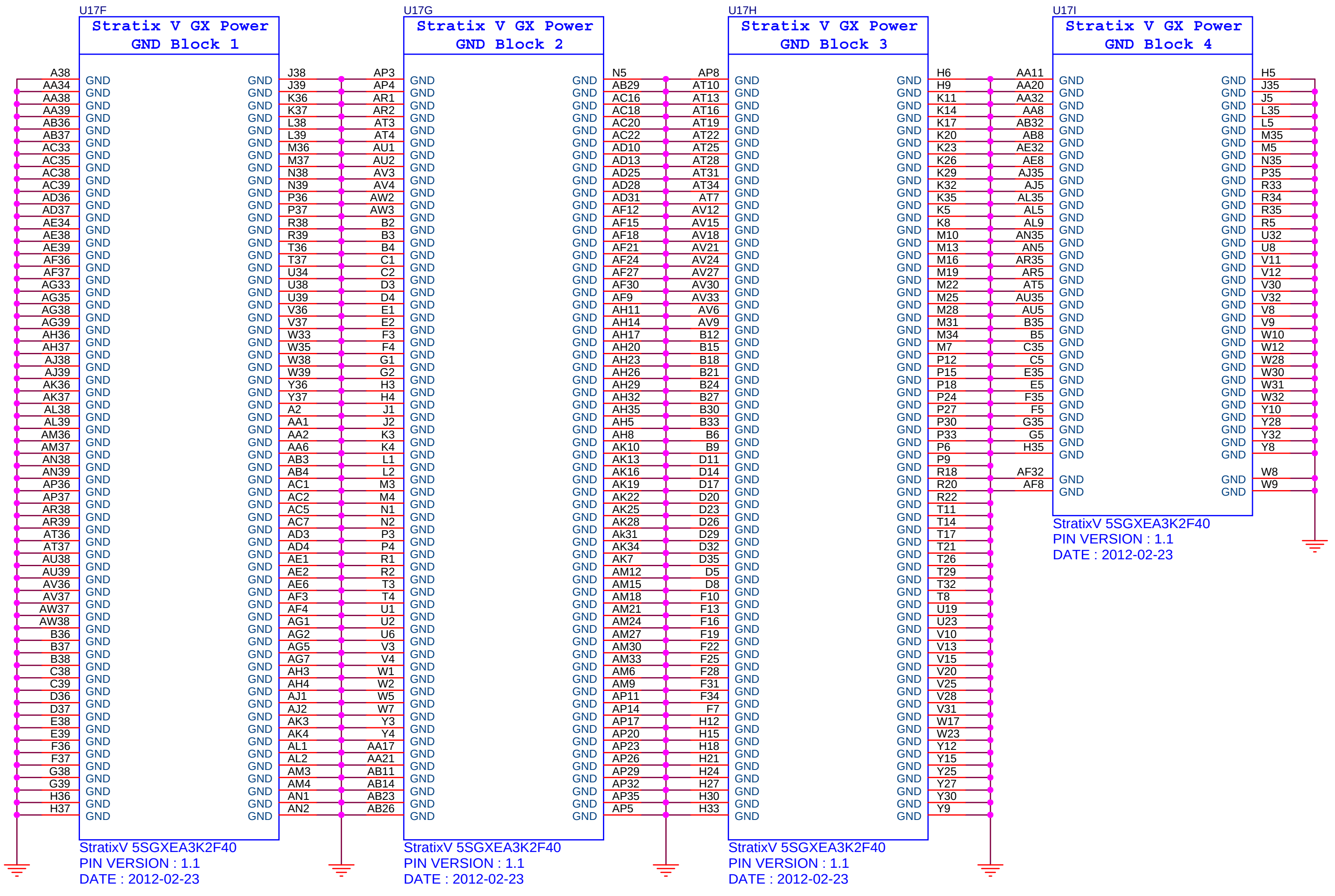
Date: Wednesday, July 11, 2012 — Sheet 17 of 28



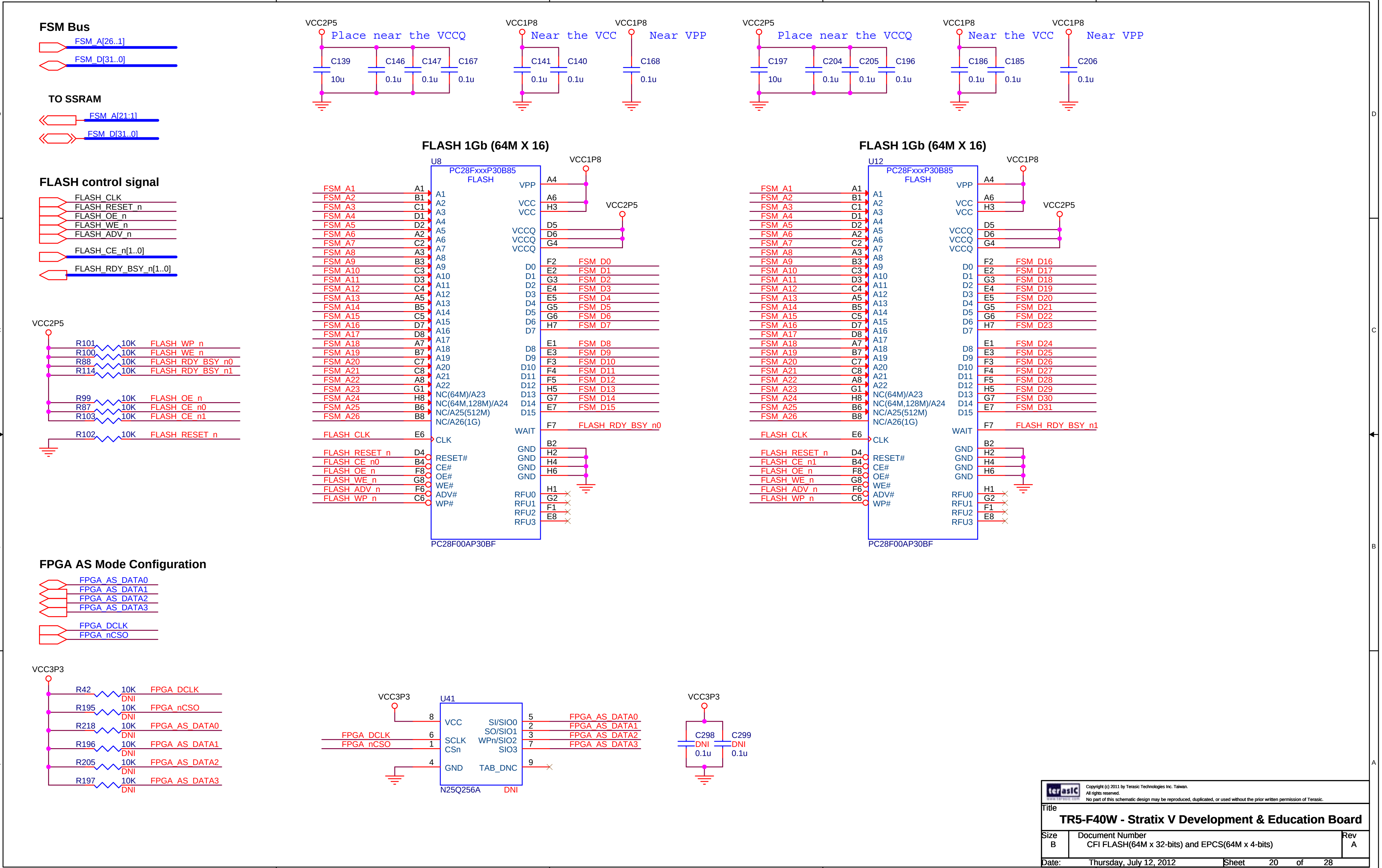
Title: TR5-F40W - Stratix V Development & Education Board

Size	Document Number	Rev
B	Stratix V Decoupling	A

Date: Thursday, July 12, 2012 — Sheet 18 of 28



Title: TR5-F40W - Stratix V Development & Education Board		
Size: B	Document Number: FPGA GND	Rev: A
Date: Wednesday, July 11, 2012	Sheet 19 of 28	



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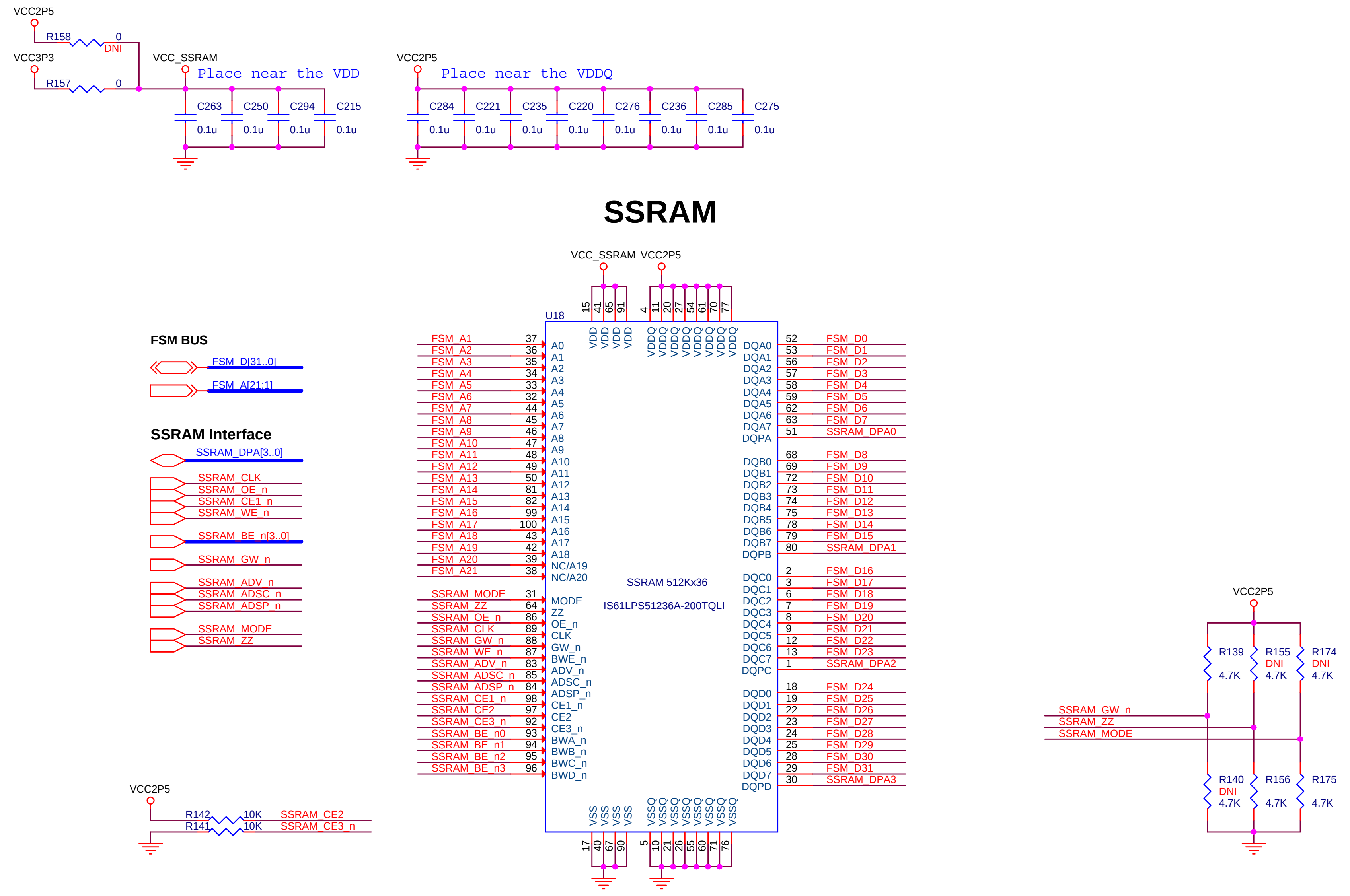
Title: TR5-F40W - Stratix V Development & Education Board

Size	Document Number	Rev
B	CFI FLASH(64M x 32-bits) and EPCS(64M x 4-bits)	A

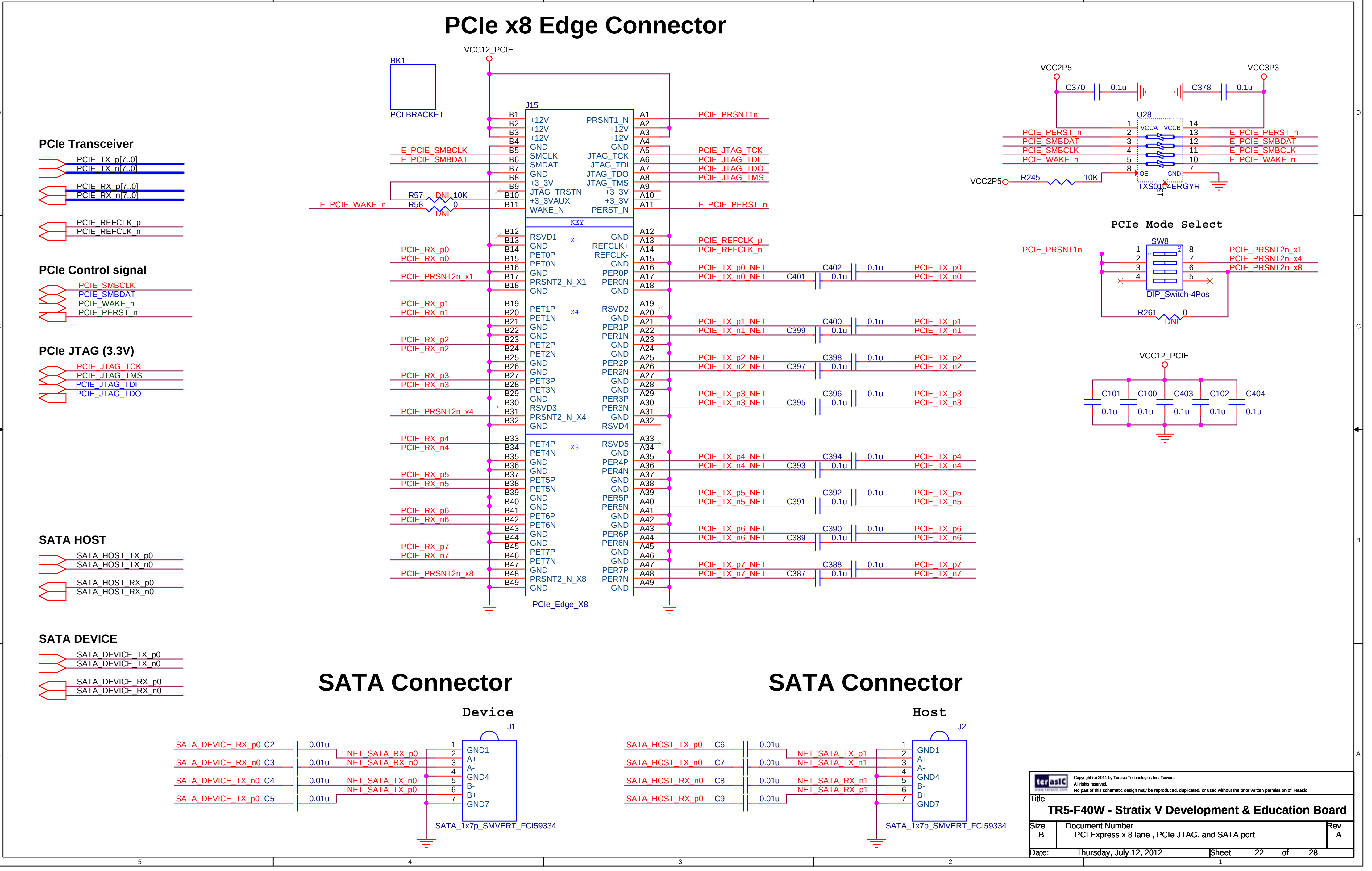
Date: Thursday, July 12, 2012 — Sheet 20 of 28



Title: TR5-F40W - Stratix V Development & Education Board

Size	Document Number	Rev
B	SSRAM 512K x 36bits	A

Date: Thursday, July 12, 2012 | Sheet 21 of 28



Title	TR5-F40W - Stratix V Development & Education Board
Size	B
Document Number	PCI Express x 8 lane , PCIe JTAG, and SATA port
Rev	A
Date:	Thursday, July 12, 2012
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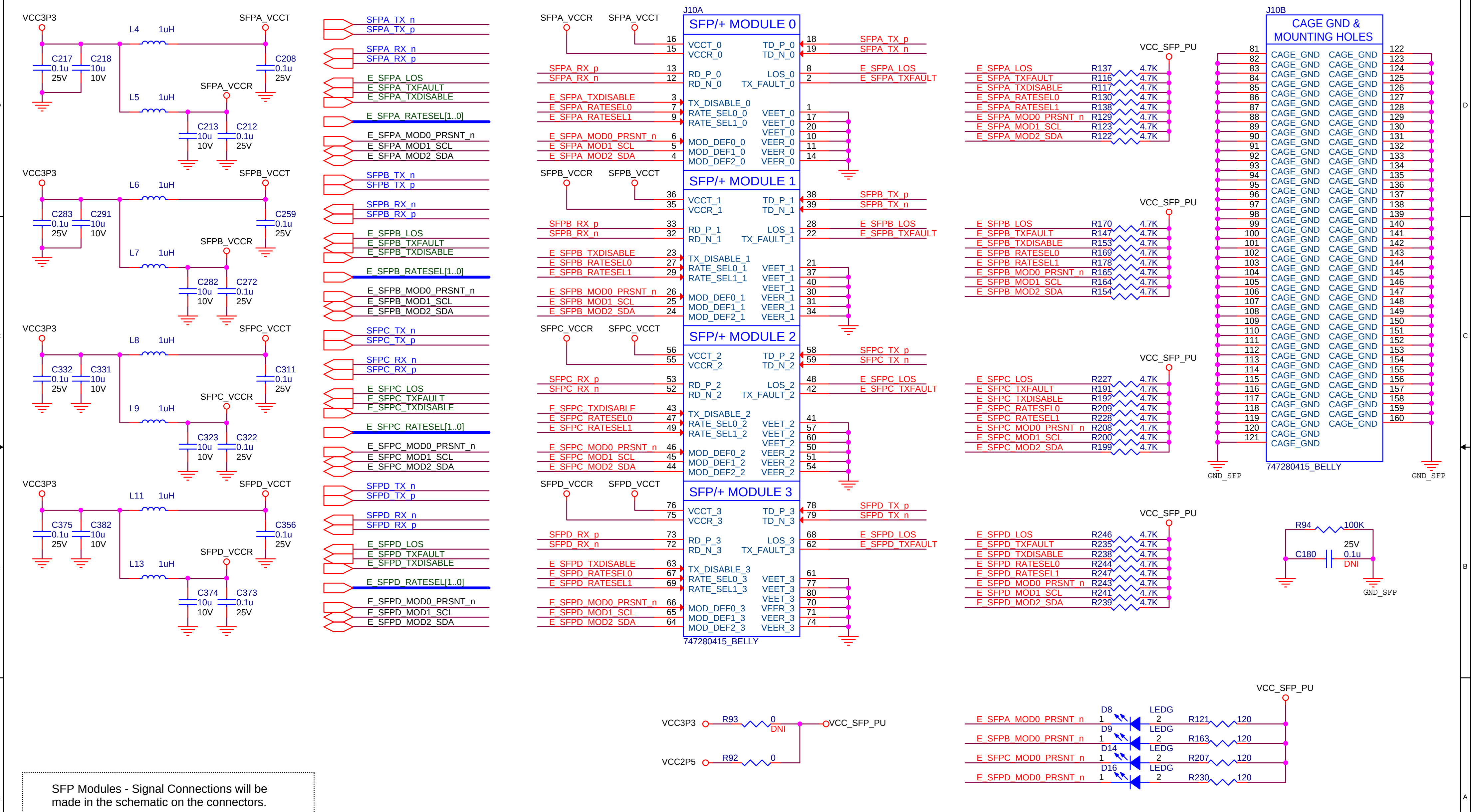
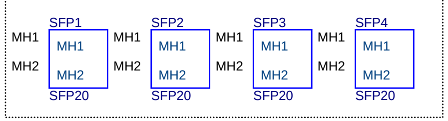


SFP Modules - Signal Connections will be made in the schematic on the connectors.



Title
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Size	Document Number	Rev
B	Quad SFP+ Interface	A

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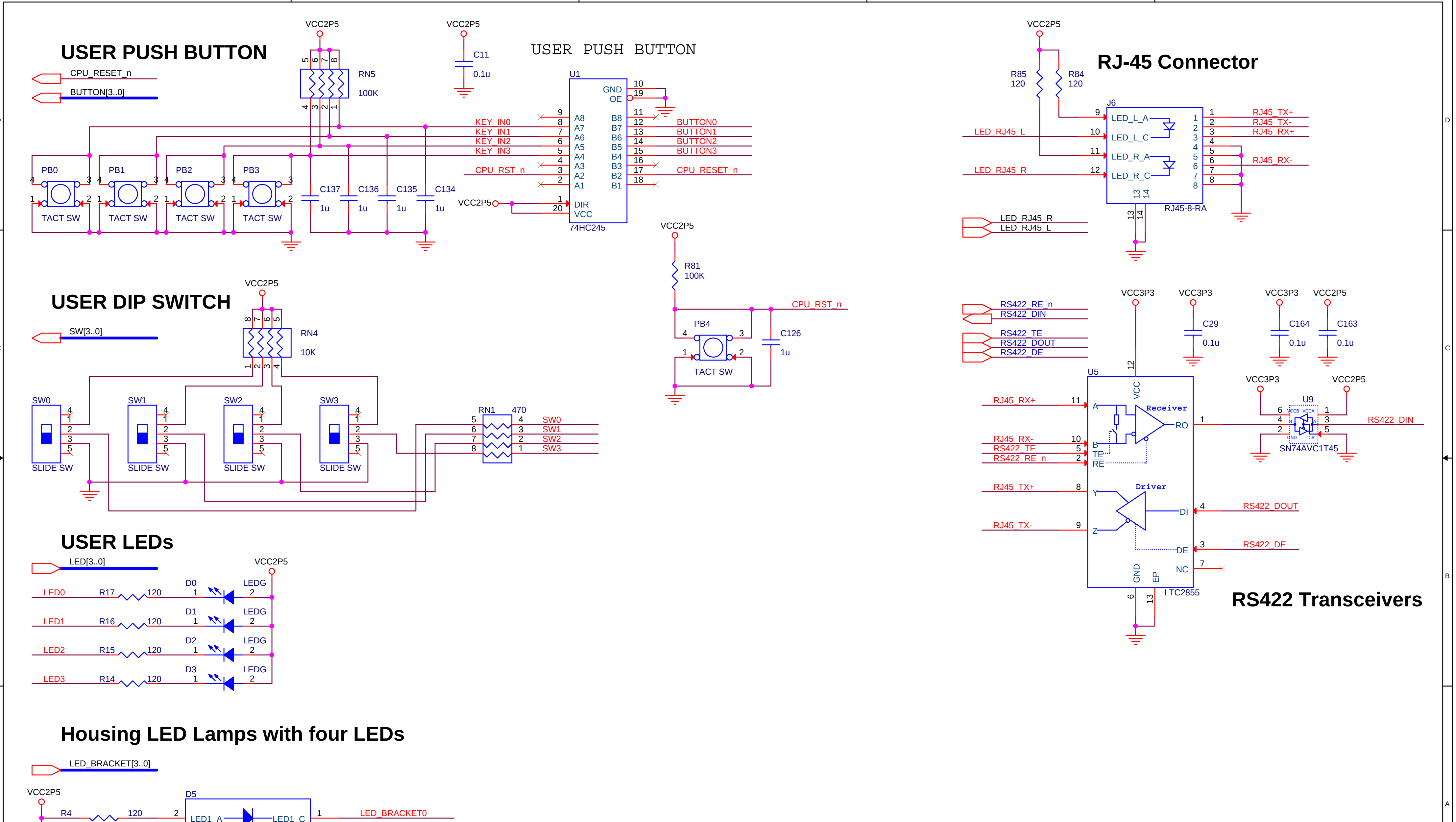

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