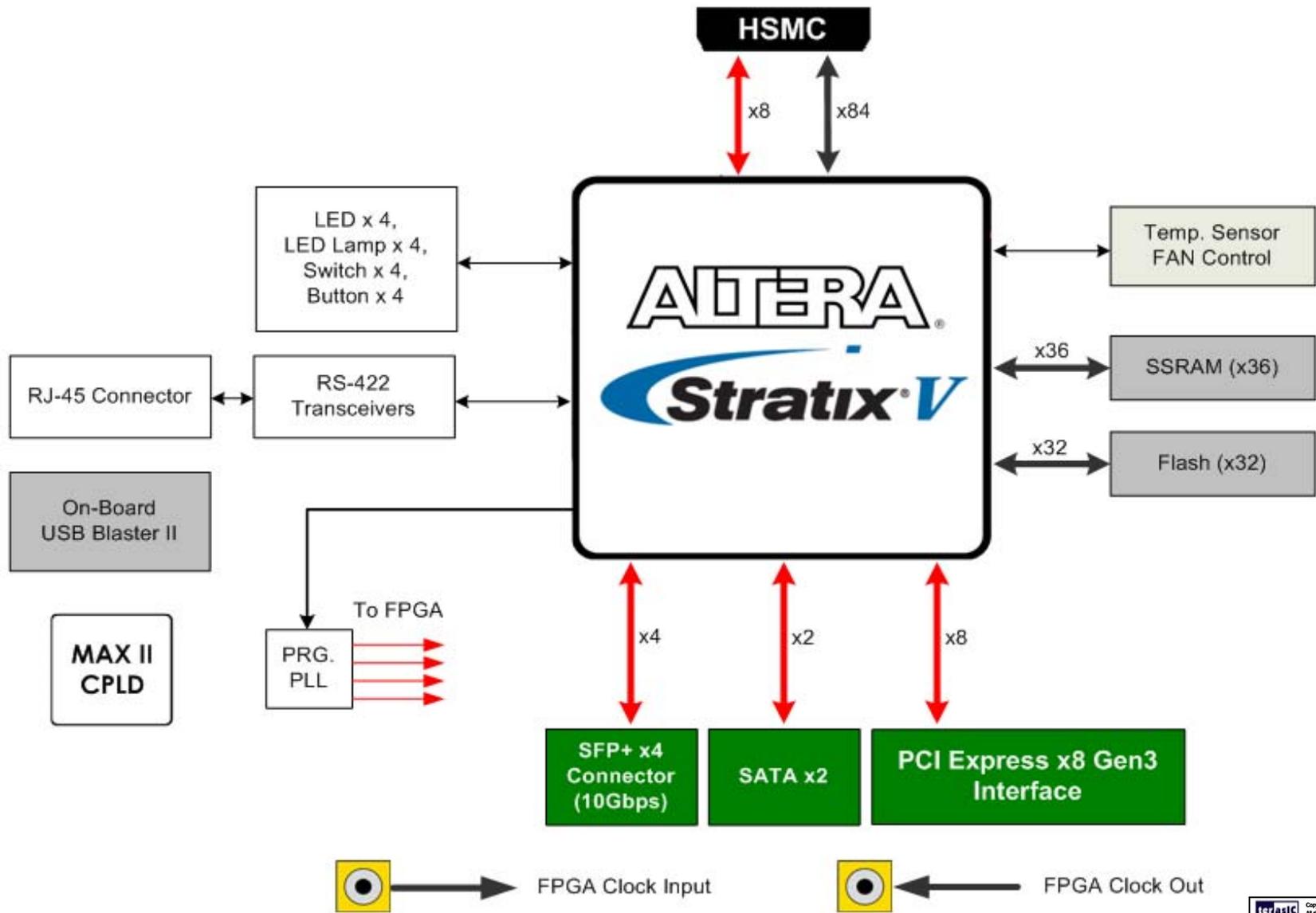


ALTERA Stratix V Development & Education Board (TR5-F40W)

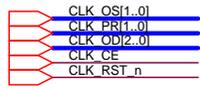
SCHEMATIC	CONTENT	PAGE
01 TOP	Cover Page, Placement, TOP	01 ~ 04
02 CLOCK	CLOCK	05
03 Configuration	Configuration	06 ~ 08
04 HSMC	HSMC Interface	09
05 FPGA	FPGA	10 ~ 19
06 Memory	CFI FLASH, SPI FLASH, SSRAM	20 ~ 21
07 PCI Express	PCI Express and SATA interface	22
08 Power	Power System	23 ~ 26
09 SFP+	Quan SFP+ Interface	27
10 User Interface	RS422 / Button / Switch / User LED	28

Block Diagram

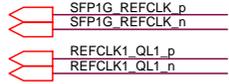


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Title TR5-F40W - Stratix V Development & Education Board		
Size B	Document Number Block Diagram	Rev A
Date: Thursday, July 12, 2012	Sheet 2	of 28

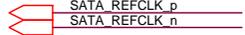
Programmer PLL



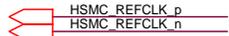
SFP+ Reference Clock



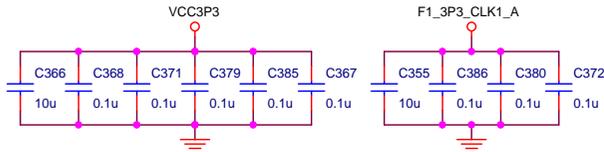
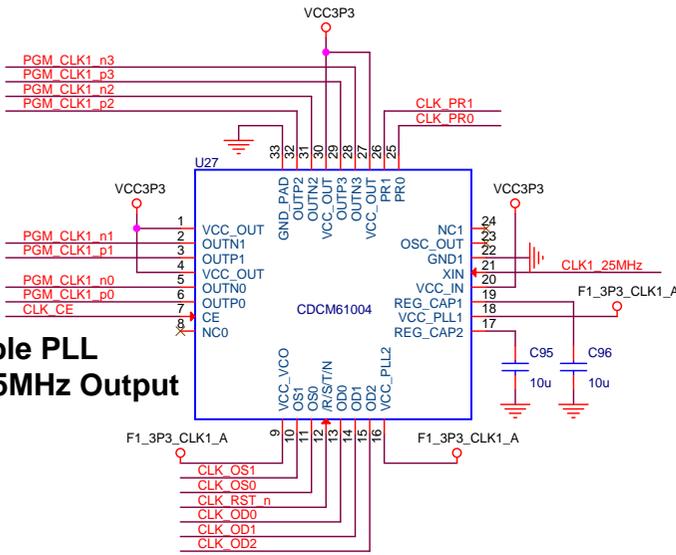
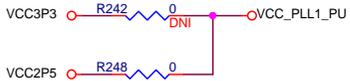
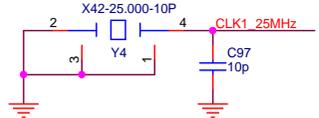
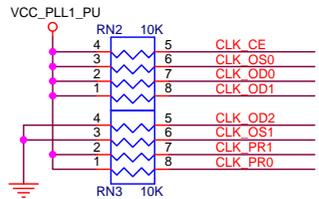
SATA Reference Clock input



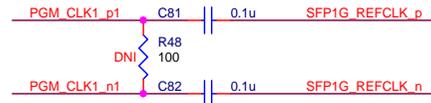
HSMC Reference Clock input



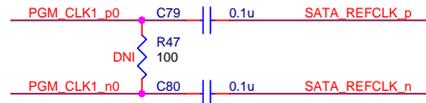
**Programmable PLL
Default 125MHz Output
LVDS Output**



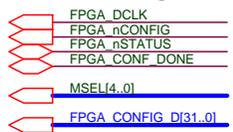
1G Ethernet SFP+ Reference Clock



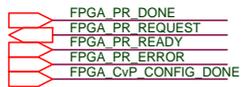
Place the AC Termination near Clock Buffer



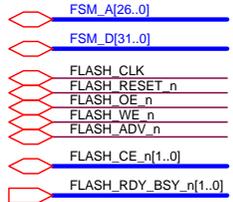
FPGA FPP Configuration



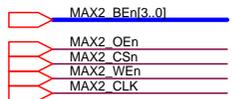
Configuration CvP with PCIe



FSM Bus and FLASH control



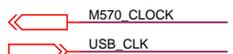
MAX2 Interface (Reserved)



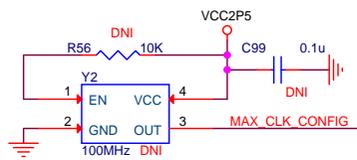
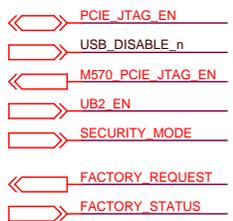
MAX2 Control signal



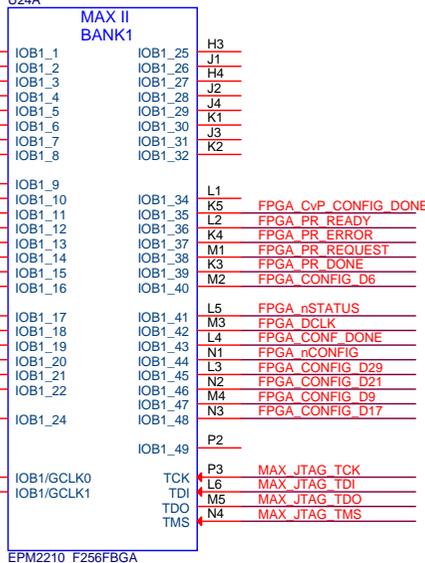
UB2 Clock



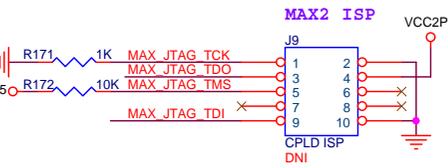
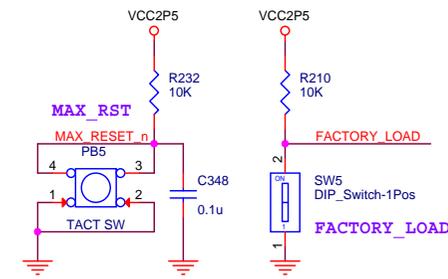
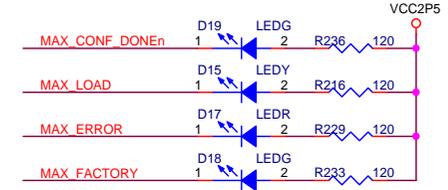
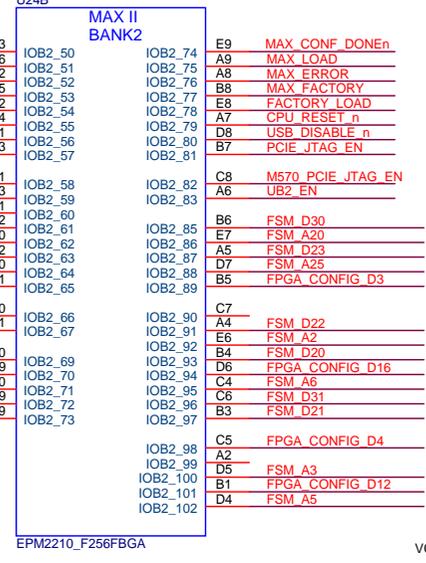
JTAG Control for MAX2



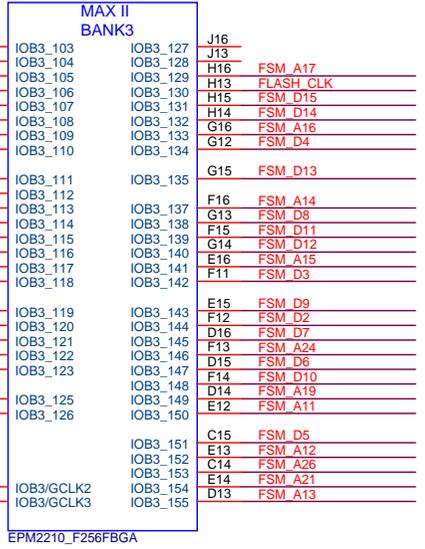
Bank = 2.5V



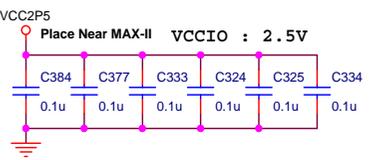
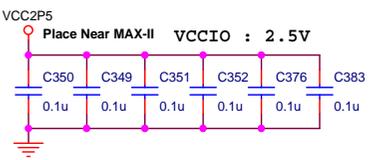
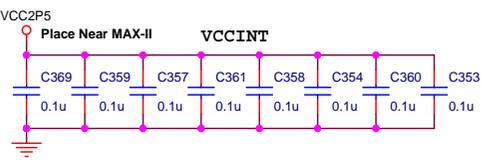
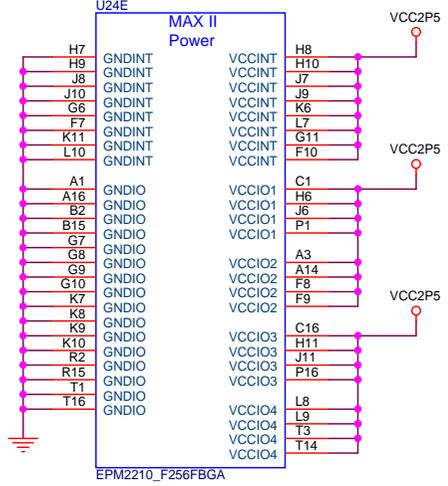
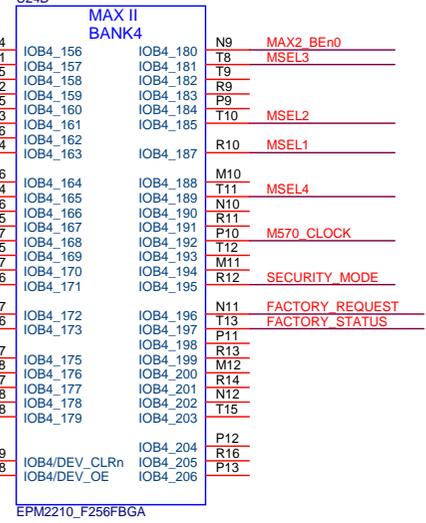
Bank = 2.5V



Bank = 2.5V

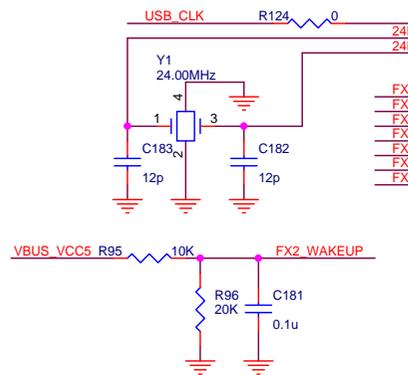
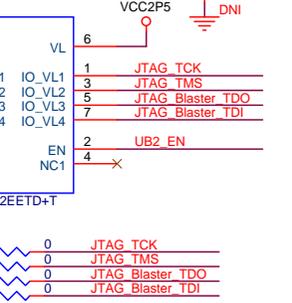
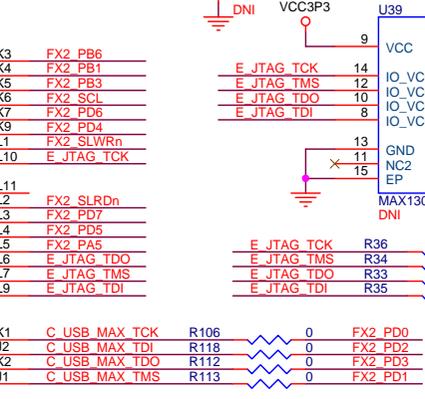
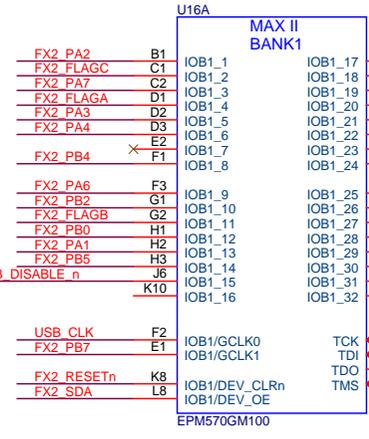
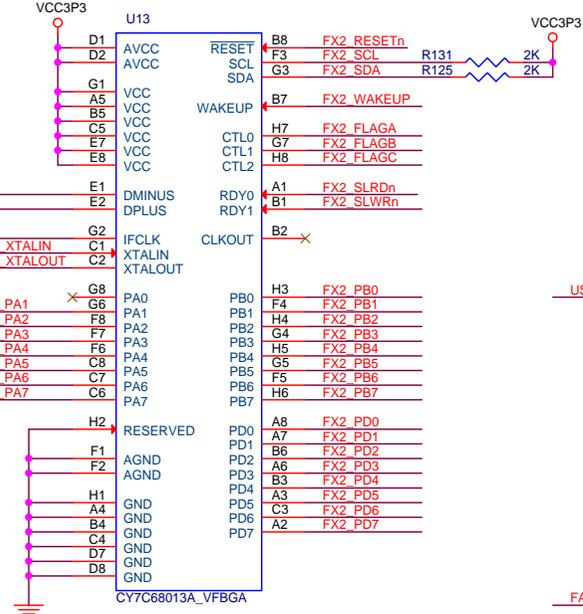
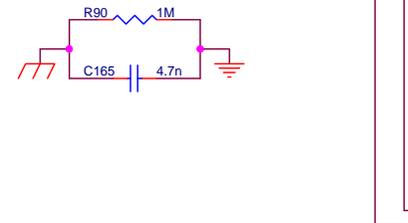
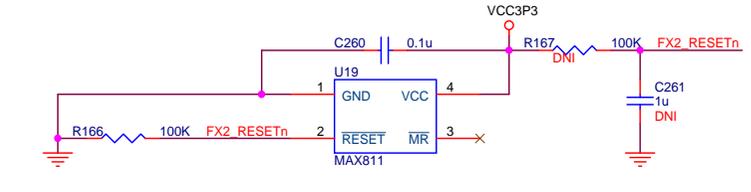
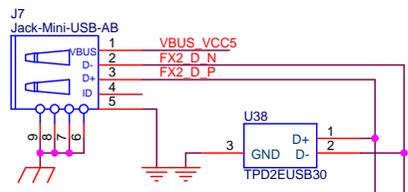


Bank = 2.5V

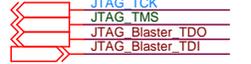


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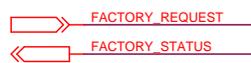
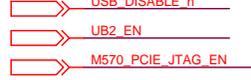
Title TR5-F40W - Stratix V Development & Education Board
Document Number EPM2210 Configuration
Rev A
Date Wednesday, July 11, 2012 **Sheet** 6 of 28



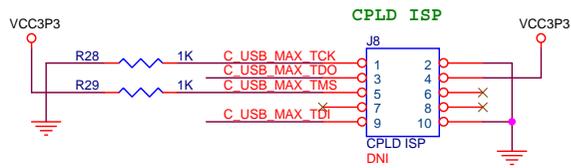
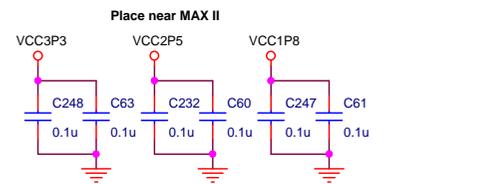
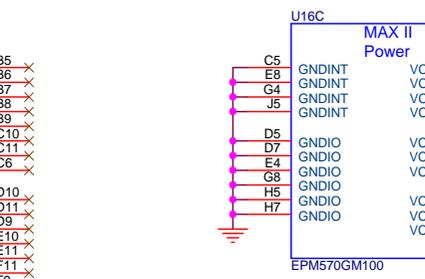
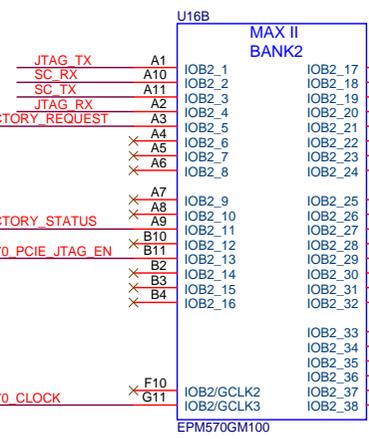
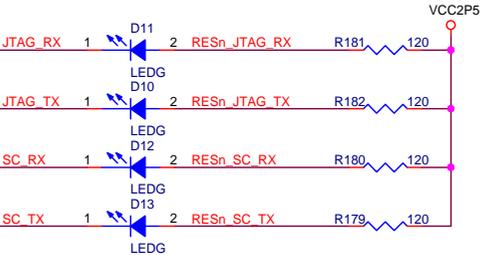
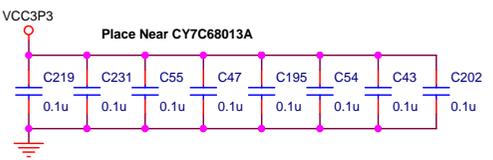
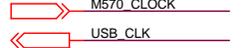
JTAG Interface (off-page, to JTAG Chain)



JTAG Control for MAX2



UB2 Clock

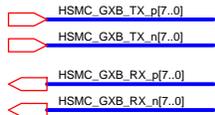


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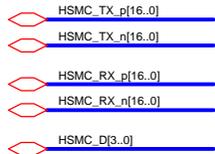
Title
TR5-F40W - Stratix V Development & Education Board

Size B	Document Number USB Blaster II	Rev A
Date: Thursday, July 12, 2012		Sheet 8 of 28

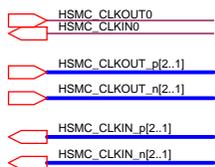
HSMC Transceiver



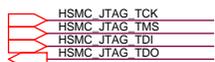
HSMC Interface



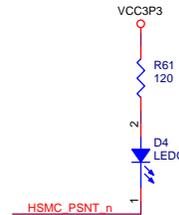
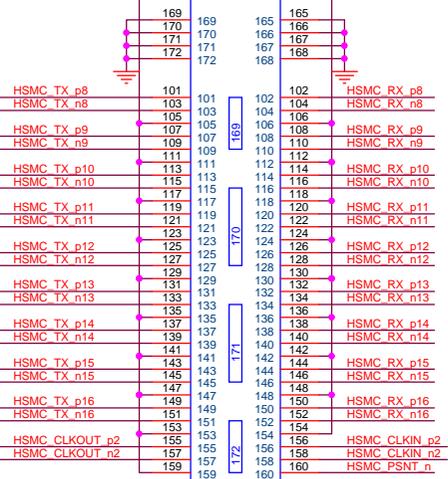
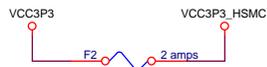
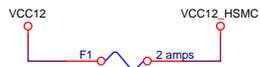
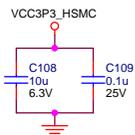
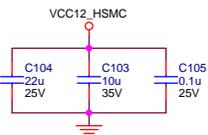
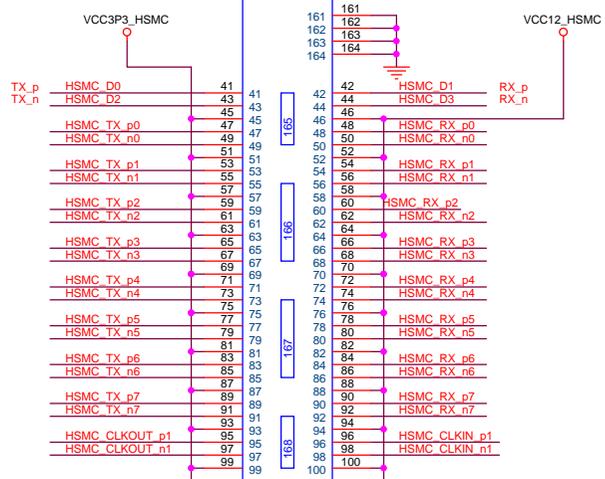
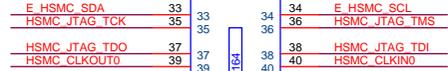
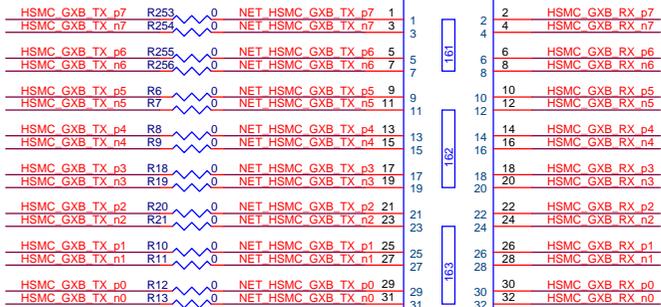
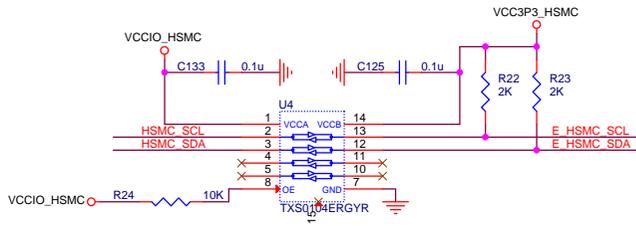
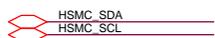
HSMC Clock



HSMC JTAG



HSMC I2C



U17J

Stratix V GX Bank 3

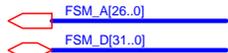
Bank 3A VCCIO = 2.5V
RZQ_0/DIFFIO_RX_B2N/DQS1B

Bank 3B VCCIO = 2.5V

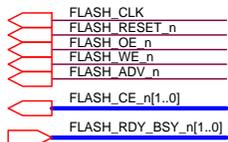
SMA_CLKOUT	AD30	DIFFIO_TX_B25P/DQ9B/FPLL_BL_CLKOUTP
SSRAM_CLK	AE30	DIFFIO_TX_B25N/DQ9B/FPLL_BL_CLKOUTN
FLASH_CLK	AB30	
	AC30	DIFFIO_RX_B26P/DQS9B/FPLL_BL_FB
		DIFFIO_RX_B26N/DQS9B/FPLL_BL_FB
SSRAM_DPA0	AK30	DIFFIO_TX_B31P/DQ11B
SSRAM_GW_n	AL30	DIFFIO_TX_B31N/DQ11B
SSRAM_WE_n	AK29	DIFFIO_TX_B33N/DQ11B
SSRAM_BE_n0	AJ29	DIFFIO_TX_B33P/DQ11B
SSRAM_DPA2	AL27	DIFFIO_TX_B33N/DQ12B
SSRAM_BE_n1	AL28	DIFFIO_TX_B35N/DQ12B
SSRAM_OE_n	AM28	DIFFIO_RX_B36P/DQ12B
SSRAM_ADSP_n	AN28	DIFFIO_RX_B36N/DQ12B
SSRAM_ZZ	AL29	
SSRAM_ADSC_n	AM29	DIFFIO_RX_B32P/DQS11B
FLASH_WE_n	AP28	DIFFIO_RX_B32N/DQS11B
FLASH_RDY_BSY_n1	AR28	DIFFIO_RX_B34P/DQS12B
		DIFFIO_RX_B34N/DQS12B

StratixV 5SGXEA3K2F40
PIN VERSION : 1.1
DATE : 2012-02-23

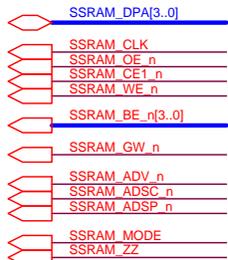
FLASH / SSRAM Share Bus



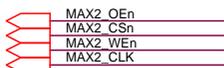
FLASH control



SSRAM Interface



MAX2 Interface (Reserved)



MAX2_BE[3..0]

SMA Cock Output



AR34 RZQ_0 R198 100

AA26	FSM_D8
AA27	FSM_D30
AB27	FSM_D31
AC27	FSM_D6
AG27	FSM_D2
AH27	FSM_D1
AJ27	SSRAM_MODE
AK27	SSRAM_BE_n2
AA28	
AA29	
AD27	
AE27	

U17K

Stratix V GX Bank 3

Bank 3C VCCIO = 2.5V

FLASH_RESET_n	AT27
FSM_A21	AU27
FLASH_RDY_BSY_n0	AT26
SSRAM_CE1_n	AU26
FSM_A9	AL26
SSRAM_ADV_n	AM26
SSRAM_DPA3	AN26
	AN27
	AV26
	AW26
FLASH_OE_n	AP27
FLASH_ADV_n	AR27
FSM_D25	AD26
FSM_D26	AE26
FSM_D23	AC25
FSM_D7	AC26
FSM_D29	AF26
FSM_D3	AG26
FSM_A15	AG25
SSRAM_BE_n3	AH25
FSM_D22	AB25
FSM_D21	AA25
FSM_A20	AJ26
	AK26

FSM_A1	AV23
FSM_A5	AW23
FSM_A19	AT23
FSM_A6	AU23
FSM_A17	AM22
FSM_A25	AN22
FSM_A13	AM23
FSM_A4	AN23

FSM_A0	AV22
FSM_A11	AP22
FSM_A22	AR22

FSM_D17	AD23
FSM_D16	AE23
FSM_D11	AF22
FSM_D10	AG22

FSM_D9	AF23
FSM_D5	AG23

DIFFIO_TX_B43P/DQ15B	
DIFFIO_TX_B43N/DQ15B	
DIFFIO_TX_B45P/DQ15B	
DIFFIO_TX_B45N/DQ15B	
DIFFIO_TX_B47P/DQ16B	
DIFFIO_TX_B47N/DQ16B	
DIFFIO_RX_B48P/DQ16B	
DIFFIO_RX_B48N/DQ16B	
DIFFIO_RX_B44P/DQS15B	
DIFFIO_RX_B44N/DQS15B	
DIFFIO_RX_B46P/DQS16B	
DIFFIO_RX_B46N/DQS16B	
DIFFIO_TX_B49P/DQ17B	
DIFFIO_TX_B49N/DQ17B	
DIFFIO_TX_B51P/DQ17B	
DIFFIO_TX_B51N/DQ17B	
DIFFIO_TX_B53P/DQ18B	
DIFFIO_TX_B53N/DQ18B	
DIFFIO_RX_B54P/DQ18B	
DIFFIO_RX_B54N/DQ18B	
DIFFIO_RX_B50P/DQS17B	
DIFFIO_RX_B50N/DQS17B	
DIFFIO_RX_B52P/DQS18B	
DIFFIO_RX_B52N/DQS18B	

Bank 3D VCCIO = 2.5V

DIFFIO_TX_B67P/DQ23B	
DIFFIO_TX_B67N/DQ23B	
DIFFIO_TX_B69P/DQ23B	
DIFFIO_TX_B69N/DQ23B	
DIFFIO_TX_B71P/DQ24B	
DIFFIO_TX_B71N/DQ24B	
DIFFIO_RX_B72P/DQ24B	
DIFFIO_RX_B72N/DQ24B	
DIFFIO_RX_B68P/DQS23B	
DIFFIO_RX_B68N/DQS23B	
DIFFIO_RX_B70P/DQS24B	
DIFFIO_RX_B70N/DQS24B	
DIFFIO_TX_B73P/DQ25B	
DIFFIO_TX_B73N/DQ25B	
DIFFIO_TX_B75P/DQ25B	
DIFFIO_TX_B75N/DQ25B	
DIFFIO_TX_B77P/DQ26B	
DIFFIO_TX_B77N/DQ26B	

DIFFIO_RX_B86P/DQS27B	
DIFFIO_RX_B86N/DQS27B	
DIFFIO_RX_B82P/DQS28B	
DIFFIO_RX_B82N/DQS28B	
DIFFIO_TX_B85P/DQ29B	
DIFFIO_TX_B85N/DQ29B	
DIFFIO_TX_B87P/DQ29B	
DIFFIO_TX_B87N/DQ29B	
DIFFIO_TX_B89P/DQ30B	
DIFFIO_TX_B89N/DQ30B	
DIFFIO_RX_B90P/DQ30B	
DIFFIO_RX_B90N/DQ30B	
DIFFIO_RX_B86P/DQS29B	
DIFFIO_RX_B86N/DQS29B	
DIFFIO_RX_B88P/DQS30B	
DIFFIO_RX_B88N/DQS30B	

DIFFIO_TX_B79P/DQ27B	
DIFFIO_TX_B79N/DQ27B	
DIFFIO_TX_B81P/DQ27B	
DIFFIO_TX_B81N/DQ27B	
DIFFIO_TX_B83P/DQ28B	
DIFFIO_TX_B83N/DQ28B	
DIFFIO_RX_B84P/DQ28B	
DIFFIO_RX_B84N/DQ28B	
DIFFIO_RX_B80P/DQS27B	
DIFFIO_RX_B80N/DQS27B	
DIFFIO_RX_B82P/DQS28B	
DIFFIO_RX_B82N/DQS28B	
DIFFIO_TX_B85P/DQ29B	
DIFFIO_TX_B85N/DQ29B	
DIFFIO_TX_B87P/DQ29B	
DIFFIO_TX_B87N/DQ29B	
DIFFIO_TX_B89P/DQ30B	
DIFFIO_TX_B89N/DQ30B	
DIFFIO_RX_B90P/DQ30B	
DIFFIO_RX_B90N/DQ30B	

DIFFIO_RX_B74P/DQS25B	
DIFFIO_RX_B74N/DQS25B	

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DIFFIO_TX_B55P/DQ19B	
DIFFIO_TX_B55N/DQ19B	
DIFFIO_TX_B57P/DQ19B	
DIFFIO_TX_B57N/DQ19B	
DIFFIO_TX_B59P/DQ20B	
DIFFIO_TX_B59N/DQ20B	
DIFFIO_RX_B60P/DQ20B	
DIFFIO_RX_B60N/DQ20B	
DIFFIO_RX_B56P/DQS19B	
DIFFIO_RX_B56N/DQS19B	
DIFFIO_RX_B46P/DQS20B	
DIFFIO_RX_B58N/DQS20B	
DIFFIO_TX_B61P/DQ21B	
DIFFIO_TX_B61N/DQ21B	
DIFFIO_TX_B63P/DQ21B	
DIFFIO_TX_B63N/DQ21B	
DIFFIO_TX_B65P/DQ22B	
DIFFIO_TX_B65N/DQ22B	
DIFFIO_RX_B66P/DQ22B	
DIFFIO_RX_B66N/DQ22B	
DIFFIO_RX_B62P/DQS21B	
DIFFIO_RX_B62N/DQS21B	
DIFFIO_RX_B64P/DQS22B	
DIFFIO_RX_B64N/DQS22B	

DIFFIO_TX_B67P/DQ23B	
DIFFIO_TX_B67N/DQ23B	
DIFFIO_TX_B69P/DQ23B	
DIFFIO_TX_B69N/DQ23B	
DIFFIO_TX_B71P/DQ24B	
DIFFIO_TX_B71N/DQ24B	
DIFFIO_RX_B72P/DQ24B	
DIFFIO_RX_B72N/DQ24B	
DIFFIO_RX_B86P/DQS27B	
DIFFIO_RX_B86N/DQS27B	
DIFFIO_RX_B82P/DQS28B	
DIFFIO_RX_B82N/DQS28B	
DIFFIO_TX_B85P/DQ29B	
DIFFIO_TX_B85N/DQ29B	
DIFFIO_TX_B87P/DQ29B	
DIFFIO_TX_B87N/DQ29B	
DIFFIO_TX_B89P/DQ30B	
DIFFIO_TX_B89N/DQ30B	
DIFFIO_RX_B90P/DQ30B	
DIFFIO_RX_B90N/DQ30B	

DIFFIO_RX_B80P/DQS27B	
DIFFIO_RX_B80N/DQS27B	
DIFFIO_RX_B82P/DQS28B	
DIFFIO_RX_B82N/DQS28B	
DIFFIO_TX_B85P/DQ29B	
DIFFIO_TX_B85N/DQ29B	
DIFFIO_TX_B87P/DQ29B	
DIFFIO_TX_B87N/DQ29B	
DIFFIO_TX_B89P/DQ30B	
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DIFFIO_RX_B90P/DQ30B	
DIFFIO_RX_B90N/DQ30B	

DIFFIO_RX_B86P/DQS29B	
DIFFIO_RX_B86N/DQS29B	
DIFFIO_RX_B88P/DQS30B	
DIFFIO_RX_B88N/DQS30B	

DIFFIO_RX_B86P/DQS29B	
DIFFIO_RX_B86N/DQS29B	
DIFFIO_RX_B88P/DQS30B	
DIFFIO_RX_B88N/DQS30B	

AV25	FSM_A2
AW25	
AT24	FSM_A24
AR24	FSM_A3
AM25	FSM_A8
AN25	SSRAM_DPA1
AN24	FLASH_CE_n1
AP24	FSM_A7
AU24	FSM_A23
AU25	FLASH_CE_n0
AP25	FSM_A10
AR25	FSM_A26
AB24	FSM_D18
AC24	FSM_D20
AD24	FSM_D19
AE24	FSM_D27
AJ24	FSM_D0
AK24	FSM_A16
AL25	FSM_A18
AL24	FSM_A12
AE25	FSM_D24
AF25	FSM_D28
AH24	FSM_A14
AG24	FSM_D4

AV20	MAX2_OEn
AW20	MAX2_CSn
AT20	MAX2_CLK
AU20	MAX2_BE_n0
AM20	MAX2_BE_n1
AN20	MAX2_BE_n2
AP21	MAX2_BE_n3

AT21	
AU21	
AR20	
AR21	
AD20	FSM_D15
AD21	FSM_D12
AE20	FSM_D14
AE21	FSM_D13
AJ20	
AJ21	
AL20	
AL21	
AH21	
AG21	
AK21	
AL22	

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Title: **TR5-F40W - Stratix V Development & Education Board**

Size B Document Number FPGA - BANK3 Rev A

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U17L

Stratix V GX Bank 4

Bank 4A		
AV8	DIFFIO_TX_B199P/DQ67B	DIFFIO_TX_B205P/DQ69B
AW8	DIFFIO_TX_B199N/DQ67B	DIFFIO_TX_B205N/DQ69B
AU7	DIFFIO_TX_B201P/DQ67B	DIFFIO_TX_B207P/DQ69B
AU8	DIFFIO_TX_B201N/DQ67B	DIFFIO_TX_B207N/DQ69B
AT6	FPLL_BR_CLKOUTP/DIFFIO_TX_B203P/DQ68B	DIFFIO_TX_B209P/DQ70B
AU6	FPLL_BR_CLKOUTN/DIFFIO_TX_B203N/DQ68B	DIFFIO_TX_B209N/DQ70B
AP7	FPLL_BR_FB/CLKOUTP/DIFFIO_RX_B204P/DQ68B	DIFFIO_RX_B210N/DQ70B
AR7	FPLL_BR_FB/CLKOUTN/DIFFIO_RX_B204N/DQ68B	

RZQ_1/DIFFIO_RX_B210P/DQ70B

AP6
AR6
AN8
AM8
AJ6
AJ7
AL6

AK6 RZQ_1 R186 100

Bank 4B

SFPA_TXFAULT	AB12	DIFFIO_TX_B175P/DQ59B	DIFFIO_TX_B187P/DQ63B
SFPA_MOD2_SDA	AC12	DIFFIO_TX_B175N/DQ59B	DIFFIO_TX_B187N/DQ63B
SFPA_LOS	AE10	DIFFIO_TX_B177P/DQ59B	DIFFIO_TX_B189P/DQ63B
SFPA_RATESELO	AE11	DIFFIO_TX_B177N/DQ59B	DIFFIO_TX_B189N/DQ63B
SFPC_TXDISABLE	AG12	DIFFIO_TX_B179P/DQ60B	DIFFIO_TX_B191P/DQ64B
SFPC_TXFAULT	AF11	DIFFIO_TX_B179N/DQ60B	DIFFIO_TX_B191N/DQ64B
SFPC_RATESEL1	AL12	DIFFIO_RX_B180P/DQ60B	DIFFIO_RX_B192P/DQ64B
SFPC_LOS	AK12	DIFFIO_RX_B180N/DQ60B	DIFFIO_RX_B192N/DQ64B

AB9 SFPA_TXDISABLE
AC9 SFPA_MOD1_SCL
AD9 SFPA_MOD0_PRSNT_n
AE9 SFPA_RATESEL1
AG9 SFPC_MOD2_SDA
AH9 SFPC_MOD0_PRSNT_n
AJ9 SFPC_MOD1_SCL
AK9 SFPC_RATESELO

AD12	DIFFIO_RX_B176P/DQS59B	DIFFIO_RX_B188P/DQS63B
AE12	DIFFIO_RX_B176N/DQS59B	DIFFIO_RX_B188N/DQS63B
AH12	DIFFIO_RX_B178P/DQS60B	DIFFIO_RX_B190P/DQS64B
AJ12	DIFFIO_RX_B178N/DQS60B	DIFFIO_RX_B190N/DQS64B

AB10
AC10
AF10
AG10

SFPB_TXFAULT	AK11	DIFFIO_TX_B181P/DQ61B	DIFFIO_TX_B193P/DQ65B
SFPB_TXDISABLE	AL11	DIFFIO_TX_B181N/DQ61B	DIFFIO_TX_B193N/DQ65B
SFPB_MOD1_SCL	AM11	DIFFIO_TX_B183P/DQ61B	DIFFIO_TX_B195P/DQ65B
SFPB_RATESELO	AN11	DIFFIO_TX_B183N/DQ61B	DIFFIO_TX_B195N/DQ65B
SFPD_TXDISABLE	AT11	DIFFIO_TX_B185P/DQ62B	DIFFIO_TX_B197P/DQ66B
SFPD_RATESELO	AU11	DIFFIO_TX_B185N/DQ62B	DIFFIO_TX_B197N/DQ66B
SFPD_LOS	AV11	DIFFIO_RX_B186P/DQ62B	DIFFIO_RX_B198P/DQ66B
SFPD_RATESEL1	AW11	DIFFIO_RX_B186N/DQ62B	DIFFIO_RX_B198N/DQ66B

AL10 SFPB_MOD2_SDA
AM10 SFPB_MOD0_PRSNT_n
AN9 SFPB_LOS
AP9 SFPB_RATESEL1
AE18 SFPD_TXFAULT
AT9 SFPD_MOD2_SDA
AU9 SFPD_MOD1_SCL
AW10 SFPD_MOD0_PRSNT_n

AR11	DIFFIO_RX_B182P/DQS61B	DIFFIO_RX_B194P/DQS65B
AR12	DIFFIO_RX_B182N/DQS61B	DIFFIO_RX_B194N/DQS65B
AT12	DIFFIO_RX_B184P/DQS62B	DIFFIO_RX_B196P/DQS66B
AU12	DIFFIO_RX_B184N/DQS62B	DIFFIO_RX_B196N/DQS66B

AN10
AP10
AV10
AW10

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Stratix V GX Bank 4

Bank 4C			
CLK_PRO	AB16	DIFFIO_TX_B151P/DQ51B	DIFFIO_TX_B163P/DQ55B
CLK_OD0	AB15	DIFFIO_TX_B151N/DQ51B	DIFFIO_TX_B163N/DQ55B
CLK_OD2	AA14	DIFFIO_TX_B153P/DQ51B	DIFFIO_TX_B165P/DQ55B
CLK_OD1	AA15	DIFFIO_TX_B153N/DQ51B	DIFFIO_TX_B165N/DQ55B
CLK_CE	AH15	DIFFIO_TX_B155P/DQ52B	DIFFIO_TX_B167P/DQ56B
CLK_PR1	AJ15	DIFFIO_TX_B155N/DQ52B	DIFFIO_TX_B167N/DQ56B
CLK_OS1	AG15	DIFFIO_RX_B156P/DQ52B	DIFFIO_RX_B168P/DQ56B
CLK_OS0	AG14	DIFFIO_RX_B156N/DQ52B	DIFFIO_RX_B168N/DQ56B

AB13
AC13
AA12
AA13
AH13
AJ13
AF13
AG13

CLK_RST_n	AC15	DIFFIO_RX_B152P/DQS51B	DIFFIO_RX_B164P/DQS55B
CLOCK_SDA	AD16	DIFFIO_RX_B152N/DQS51B	DIFFIO_RX_B164N/DQS55B
CLOCK_SCL	AD15	DIFFIO_RX_B154P/DQS52B	DIFFIO_RX_B166P/DQS56B
	AE15	DIFFIO_RX_B154N/DQS52B	DIFFIO_RX_B166N/DQS56B

AC14
AD14
AE14
AF14

SDI_CLK148_UP	AK15	DIFFIO_TX_B157P/DQ53B	DIFFIO_TX_B169P/DQ57B
SDI_CLK148_DN	AL15	DIFFIO_TX_B157N/DQ53B	DIFFIO_TX_B169N/DQ57B
	AM14	DIFFIO_TX_B158P/DQ53B	DIFFIO_TX_B171P/DQ57B
	AN14	DIFFIO_TX_B158N/DQ53B	DIFFIO_TX_B171N/DQ57B
	AR14	DIFFIO_TX_B161P/DQ54B	DIFFIO_TX_B173P/DQ58B
	AR15	DIFFIO_TX_B161N/DQ54B	DIFFIO_TX_B173N/DQ58B
	AT15	DIFFIO_RX_B162P/DQ54B	DIFFIO_RX_B174P/DQ58B
	AU15	DIFFIO_RX_B162N/DQ54B	DIFFIO_RX_B174N/DQ58B

AL13
AM13
AN13
AP13
AV14
AW14
AX13
AY13

AK14	DIFFIO_RX_B158P/DQS53B	DIFFIO_RX_B170P/DQS57B
AL14	DIFFIO_RX_B158N/DQS53B	DIFFIO_RX_B170N/DQS57B
AN15	DIFFIO_RX_B160P/DQS54B	DIFFIO_RX_B172P/DQS58B
AP15	DIFFIO_RX_B160N/DQS54B	DIFFIO_RX_B172N/DQS58B

AN12
AP12
AT12
AU12

Bank 4D

AG19	DIFFIO_TX_B127P/DQ43B	FPLL_BC_CLKOUTP/DIFFIO_TX_B139P/DQ47B	AH16
AH19	DIFFIO_TX_B127N/DQ43B	FPLL_BC_CLKOUTN/DIFFIO_TX_B139N/DQ47B	AJ17
AH18	DIFFIO_TX_B129P/DQ43B	DIFFIO_TX_B141P/DQ47B	AL16
AJ18	DIFFIO_TX_B129N/DQ43B	DIFFIO_TX_B141N/DQ47B	AM16
AE18	DIFFIO_TX_B131P/DQ44B	DIFFIO_TX_B143P/DQ48B	AF16
AE19	DIFFIO_TX_B131N/DQ44B	DIFFIO_TX_B143N/DQ48B	AG16
AD18	DIFFIO_RX_B132P/DQ44B		
AD17	DIFFIO_RX_B132N/DQ44B		

AH16
AJ17
AL16
AM16
AF16
AG16

AJ19	DIFFIO_RX_B128P/DQ43B	FPLL_BC_FB/CLKOUTP/DIFFIO_RX_B140P/DQS47B	AK17
AK18	DIFFIO_RX_B128N/DQ43B	FPLL_BC_FB/CLKOUTN/DIFFIO_RX_B140N/DQS47B	AL17
AF19	DIFFIO_RX_B130P/DQS44B		
AG18	DIFFIO_RX_B130N/DQS44B		

AK17
AL17

AL18	DIFFIO_TX_B133P/DQ45B	DIFFIO_TX_B145P/DQ49B	AM17 TEMP_CLK
AM19	DIFFIO_TX_B133N/DQ45B	DIFFIO_TX_B145N/DQ49B	AN17 TEMP_DATA
AP18	DIFFIO_TX_B135P/DQ45B	DIFFIO_TX_B147P/DQ49B	AR17 TEMP_OVERT_n
AR18	DIFFIO_TX_B135N/DQ45B	DIFFIO_TX_B147N/DQ49B	AT17 TEMP_INT_n
AT18	DIFFIO_TX_B137P/DQ46B	DIFFIO_TX_B149P/DQ50B	AV16
AU18	DIFFIO_TX_B137N/DQ46B	DIFFIO_TX_B149N/DQ50B	AW16 FAN_CTRL
AV19	DIFFIO_RX_B138P/DQ46B	DIFFIO_RX_B150P/DQ50B	AX17
AW19	DIFFIO_RX_B138N/DQ46B	DIFFIO_RX_B150N/DQ50B	AY17

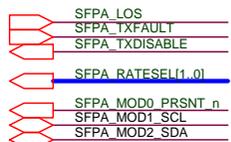
AM17 TEMP_CLK
AN17 TEMP_DATA
AR17 TEMP_OVERT_n
AT17 TEMP_INT_n
AV16
AW16 FAN_CTRL
AX17
AY17

AN19	DIFFIO_RX_B134P/DQS45B	DIFFIO_RX_B146P/DQS49B	AN16
AN18	DIFFIO_RX_B134N/DQS45B	DIFFIO_RX_B146N/DQS49B	AP16
AP19	DIFFIO_RX_B136P/DQS46B	DIFFIO_RX_B148P/DQS50B	AU17
AR19	DIFFIO_RX_B136N/DQS46B	DIFFIO_RX_B148N/DQS50B	AU16

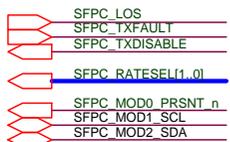
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AP16
AU17
AU16

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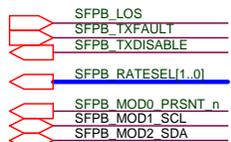
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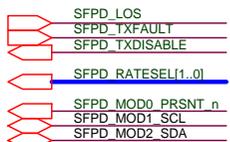
SFP+ Port C



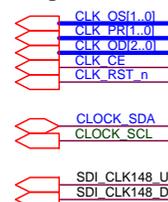
SFP+ Port B



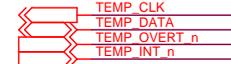
SFP+ Port D



Programmer PLL



FPGA Temperature Control and Monitor



FAN Control Interface

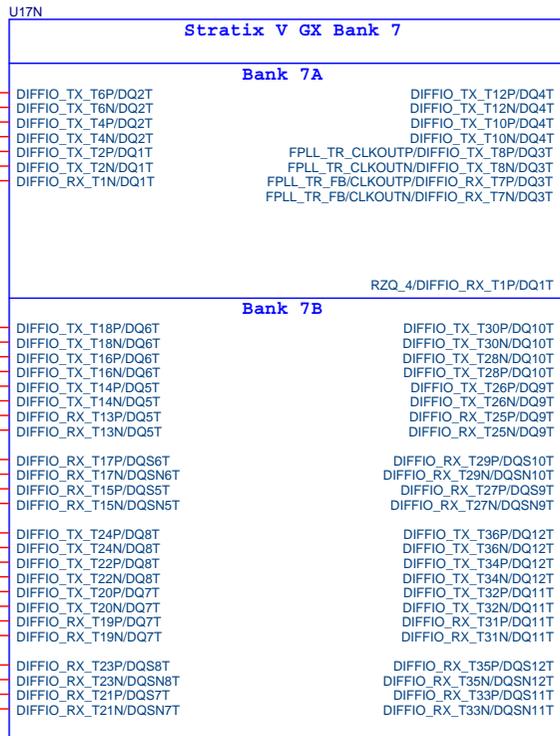


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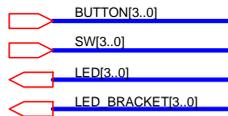
Size B	Document Number FPGA - BANK4	Rev A
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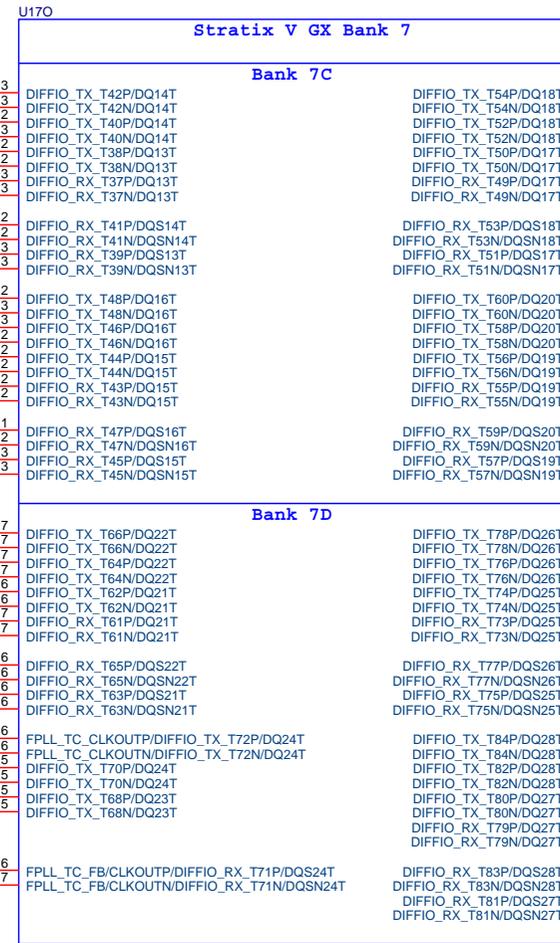
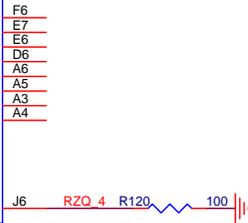


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PIN VERSION : 1.1
DATE : 2012-02-23

User Interface



RS422 Transceivers

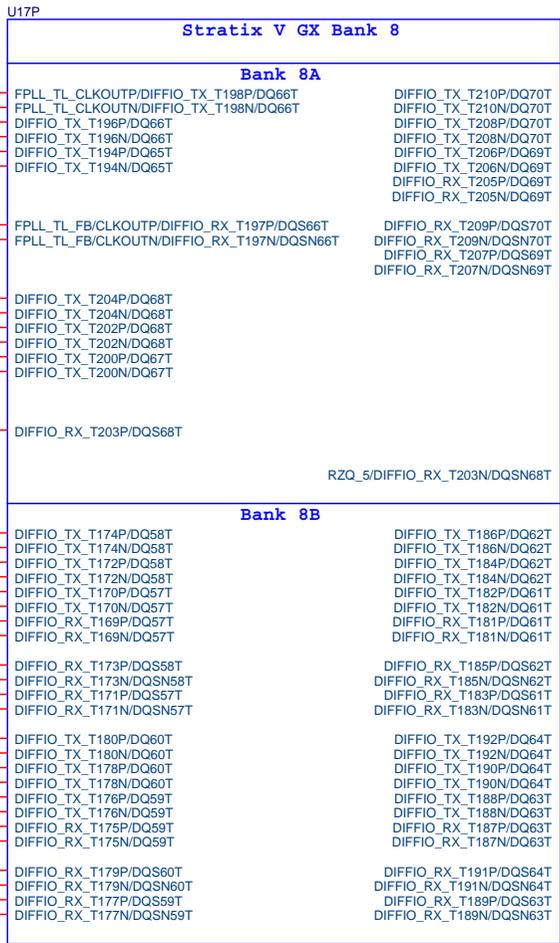


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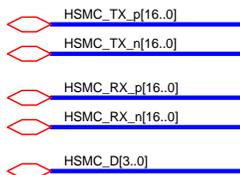
TR5-F40W - Stratix V Development & Education Board

Size B	Document Number FPGA - BANK7	Rev A
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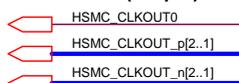


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DATE : 2012-02-23

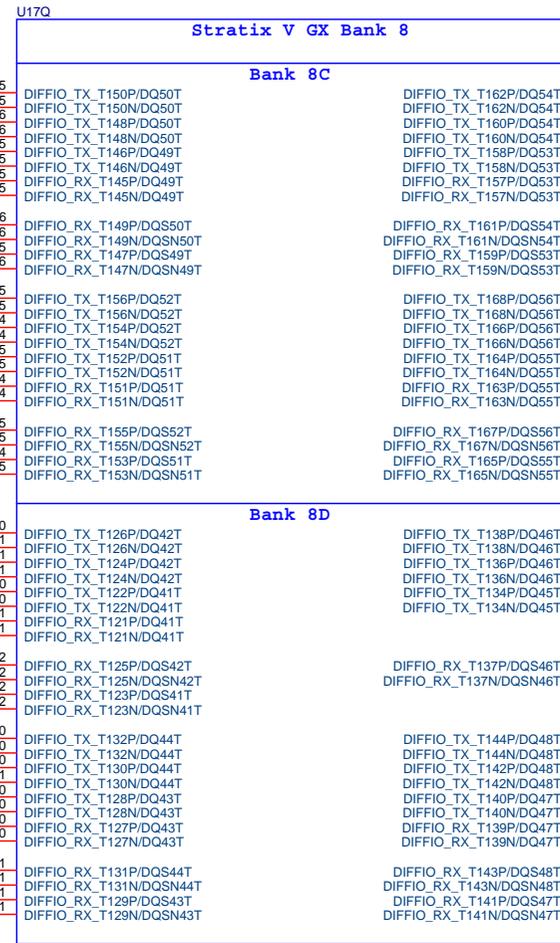
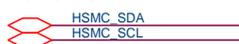
HSMC Interface



HSMC Clock (Output)



HSMC I2C



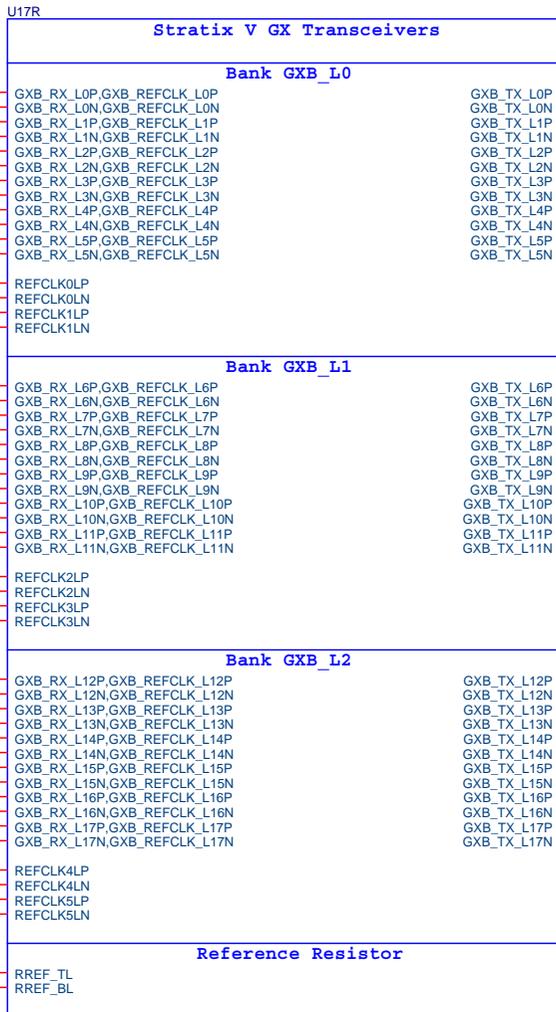
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PIN VERSION : 1.1
DATE : 2012-02-23

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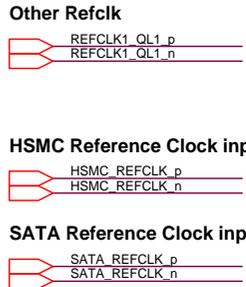
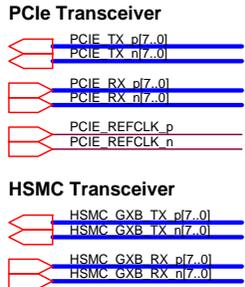
TR5-F40W - Stratix V Development & Education Board

Size	Document Number	Rev
B	FPGA - BANK8	A

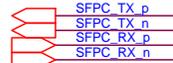
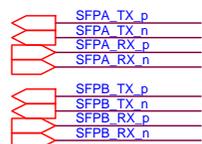
Date: Thursday, July 12, 2012 Sheet 13 of 28



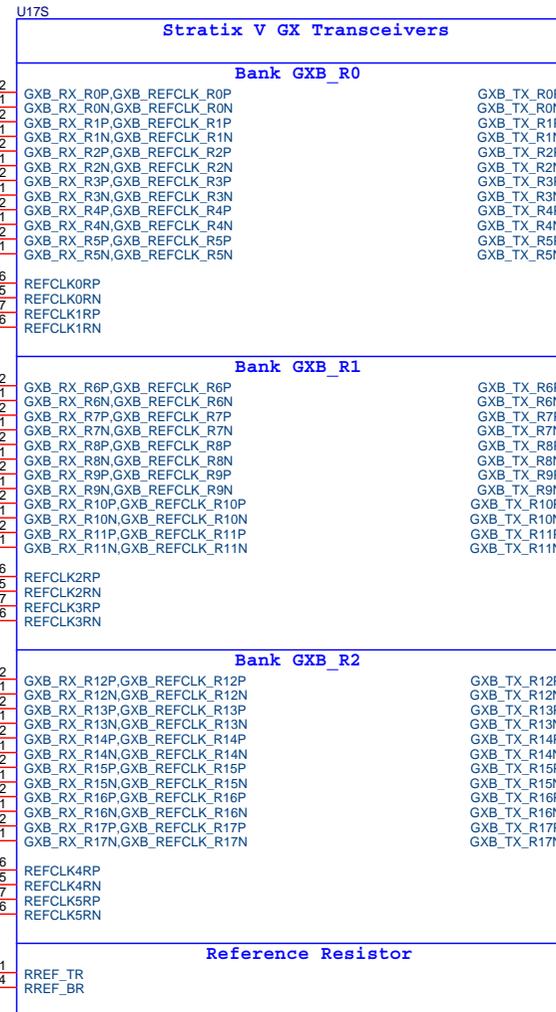
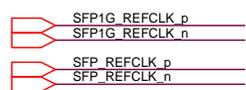
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PIN VERSION : 1.1
DATE : 2012-02-23



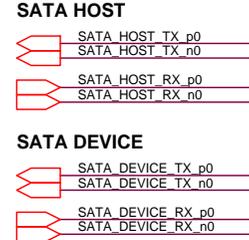
SFP+ Transceiver



SFP+ Reference Clock



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PIN VERSION : 1.1
DATE : 2012-02-23

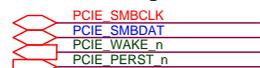


TR5-F40W - Stratix V Development & Education Board			
Size B	Document Number FPGA - GXB Bank	Rev A	
Date:	Wednesday, July 11, 2012	Sheet	14 of 28

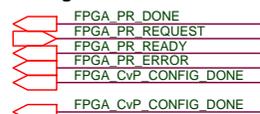
FPGA JTAG



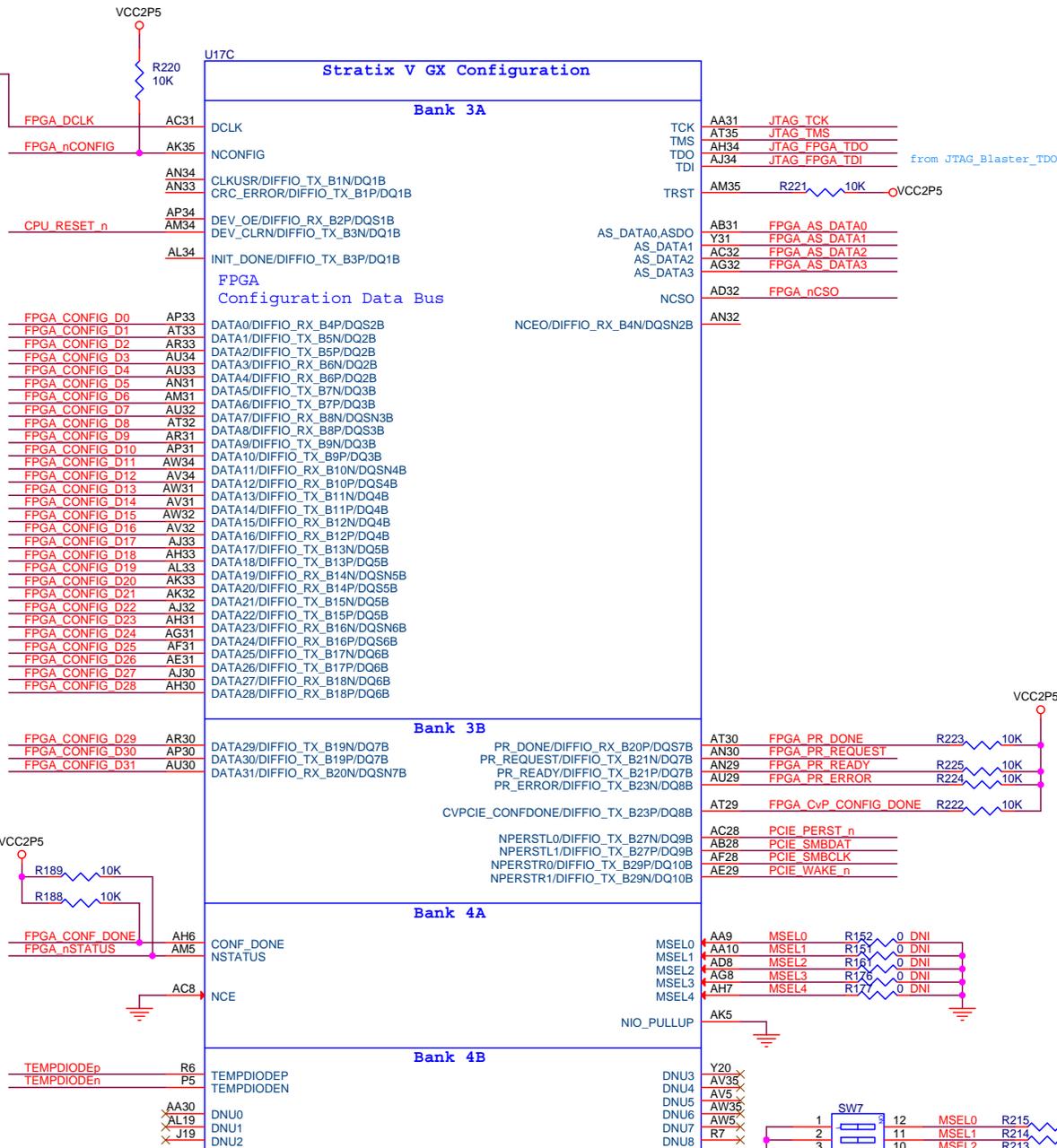
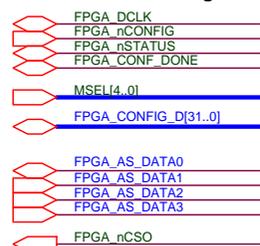
PCIe Control signal



Configuration CvP with PCIe

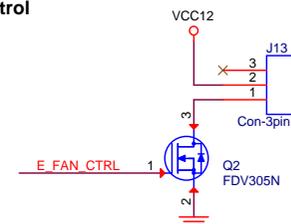
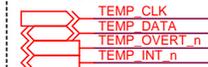


FPGA FPP / AS Configuration

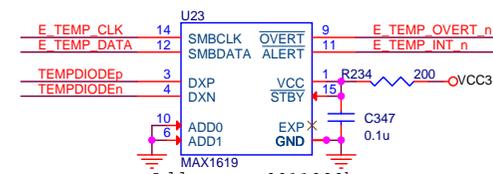
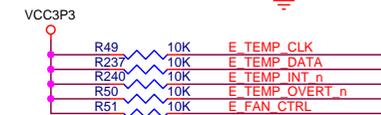


Stratix V 5SGXEA3K2F40
PIN VERSION : 1.1
DATE : 2012-02-23

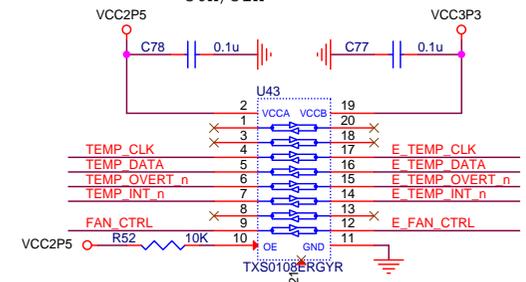
FPGA Temperature Control and Monitor



FAN Control Interface



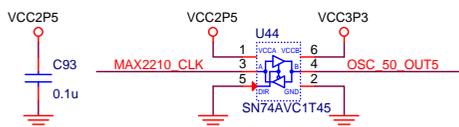
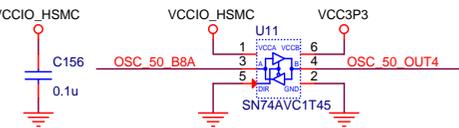
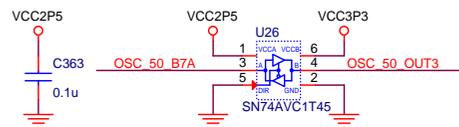
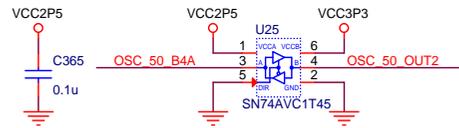
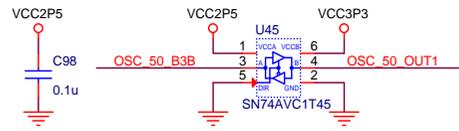
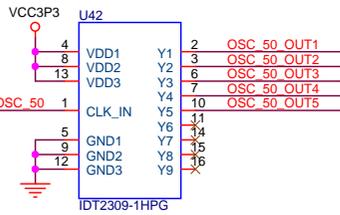
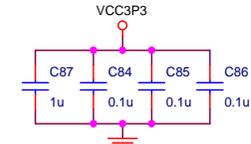
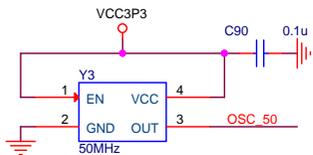
Address = 0011000b
30H/31H



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TR5-F40W - Stratix V Development & Education Board

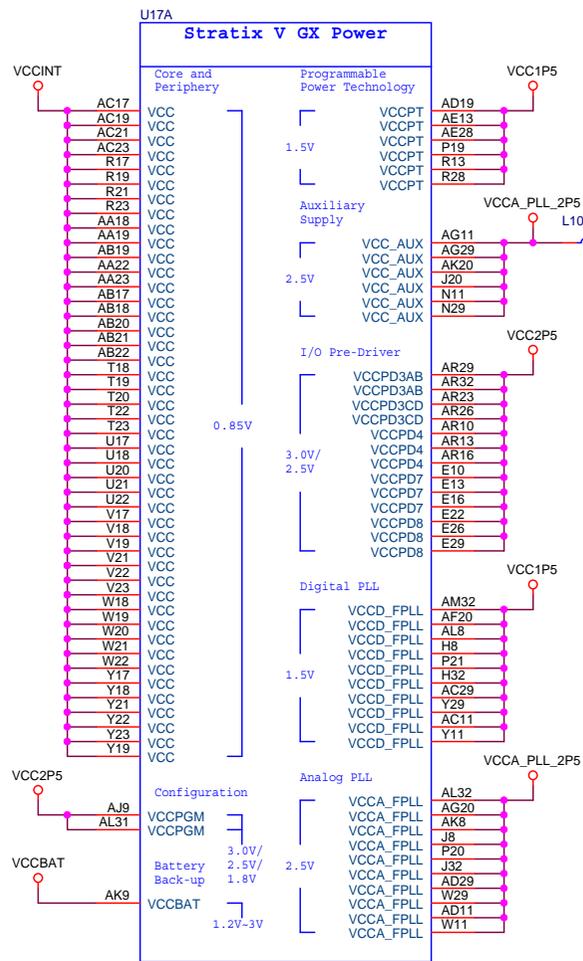
Size B	Document Number FPGA Configuration and Temperature	Rev A
Date:	Thursday, July 12, 2012	Sheet 15 of 28



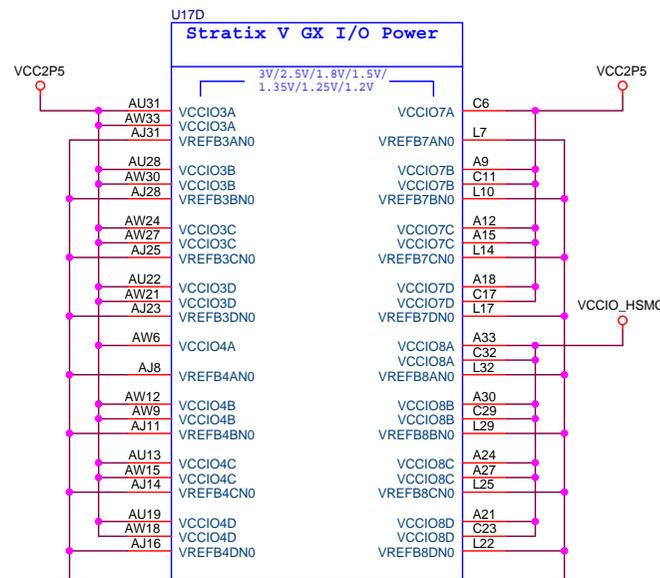
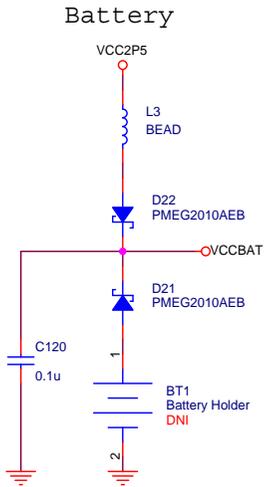
U17B	
Stratix V GX Clocks	
Bank 3B VCCIO = 2.5V	
OSC_50_B3B	AV29 AW29 AV28 AW28 AF29 AG30 AG28 AH28
	CLK0P_AW35/DIFFIO_RX_B22P/DQS88B CLK0N_AY36/DIFFIO_RX_B22N/DQS88B CLK1P_AY34/DIFFIO_RX_B24P/DQ8B CLK1N_BA34/DIFFIO_RX_B24N/DQ8B CLK2P_AY33/DIFFIO_RX_B28P/DQS10B CLK2N_BA33/DIFFIO_RX_B28N/DQS10B CLK3P_BB33/DIFFIO_RX_B30P/DQ10B CLK3N_BC34/DIFFIO_RX_B30N/DQ10B
Bank 3D VCCIO = 2.5V	
OSC_50_B3B	R206
	AH22 AJ22 AK23 AL23
	CLK4P_BC28/DIFFIO_RX_B76P/DQS26B CLK4N_BD28/DIFFIO_RX_B76N/DQS26B CLK5P_BA27/DIFFIO_RX_B78P/DQ26B CLK5N_BD27/DIFFIO_RX_B78N/DQ26B
Bank 4A VCCIO = 2.5V	
OSC_50_B4A	AL7 AM7 AN7 AR7 AT8 AV7 AW7
	CLK8P_AP10/DIFFIO_RX_B208P/DQS70B CLK8N_AR10/DIFFIO_RX_B208N/DQS70B CLK9P_AR11/DIFFIO_RX_B206P/DQS69B CLK9N_AT11/DIFFIO_RX_B206N/DQS69B CLK10P_AY9/DIFFIO_RX_B202P/DQS68B CLK10N_BA9/DIFFIO_RX_B202N/DQS68B CLK11P_BC8/DIFFIO_RX_B200P/DQS67B CLK11N_BD8/DIFFIO_RX_B200N/DQS67B
Bank 4D VCCIO = 2.5V	
OSC_50_B4A	R185
	AF17 AG17 AE17 AE16
	CLK6P_AY18/DIFFIO_RX_B142P/DQS48B CLK6N_BA18/DIFFIO_RX_B142N/DQS48B CLK7P_BB17/DIFFIO_RX_B144P/DQ48B CLK7N_BB17/DIFFIO_RX_B144N/DQ48B
Bank 7A VCCIO = 2.5V	
OSC_50_B7A	G7 G6 L6 K6 B7 A7 D7 C7
	CLK12P_M8/DIFFIO_RX_T3P/DQS1T CLK12N_L8/DIFFIO_RX_T3N/DQS1T CLK13P_M9/DIFFIO_RX_T5P/DQS2T CLK13N_L9/DIFFIO_RX_T5N/DQS2T CLK14P_E8/DIFFIO_RX_T9P/DQS3T CLK14N_D9/DIFFIO_RX_T9N/DQS3T CLK15P_B8/DIFFIO_RX_T11P/DQS4T CLK15N_A8/DIFFIO_RX_T11N/DQS4T
Bank 7D VCCIO = 2.5V	
OSC_50_B7A	R119
	P16 N16 U15 T16
	CLK18P_J18/DIFFIO_RX_T69P/DQS23T CLK18N_H18/DIFFIO_RX_T69N/DQS23T CLK19P_G16/DIFFIO_RX_T67P/DQ23T CLK19N_F16/DIFFIO_RX_T67N/DQ23T
Bank 8A VCCIO = VCCIO_HSMC (1.2V/1.5V/1.8V/2.5V)	
OSC_50_B8A	E34 D34 D33 C33 N32 M32 R32 P32
	CLK20P_R36/DIFFIO_RX_T201P/DQS67T CLK20N_P37/DIFFIO_RX_T201N/DQS67T CLK21P_U36/DIFFIO_RX_T199P/DQ67T CLK21N_T36/DIFFIO_RX_T199N/DQ67T CLK22P_B39/DIFFIO_RX_T195P/DQS65T CLK22N_A38/DIFFIO_RX_T195N/DQS65T CLK23P_B37/DIFFIO_RX_T193P/DQ65T CLK23N_A37/DIFFIO_RX_T193N/DQ65T
Bank 8D VCCIO = VCCIO_HSMC (1.2V/1.5V/1.8V/2.5V)	
OSC_50_B8A	R115
	J23 J24 M23 L23
	CLK16P_R25/DIFFIO_RX_T135P/DQS45T CLK16N_P25/DIFFIO_RX_T135N/DQS45T CLK17P_N25/DIFFIO_RX_T133P/DQ45T CLK17N_M25/DIFFIO_RX_T133N/DQ45T

StratixV 5SGXEA3K2F40
PIN VERSION : 1.1
DATE : 2012-02-23

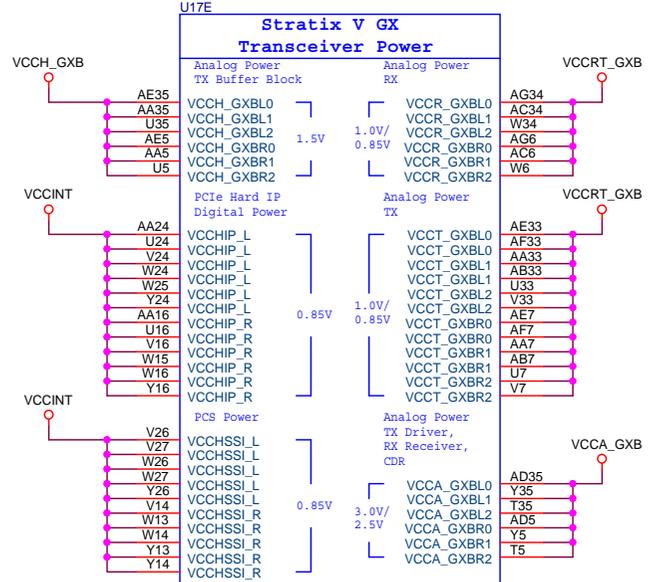
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Title TR5-F40W - Stratix V Development & Education Board		
Size B	Document Number FPGA - Clock Bank	Rev A
Date: Thursday, July 12, 2012		Sheet 16 of 28



StratixV 5SGXEA3K2F40
PIN VERSION : 1.1
DATE : 2012-02-23

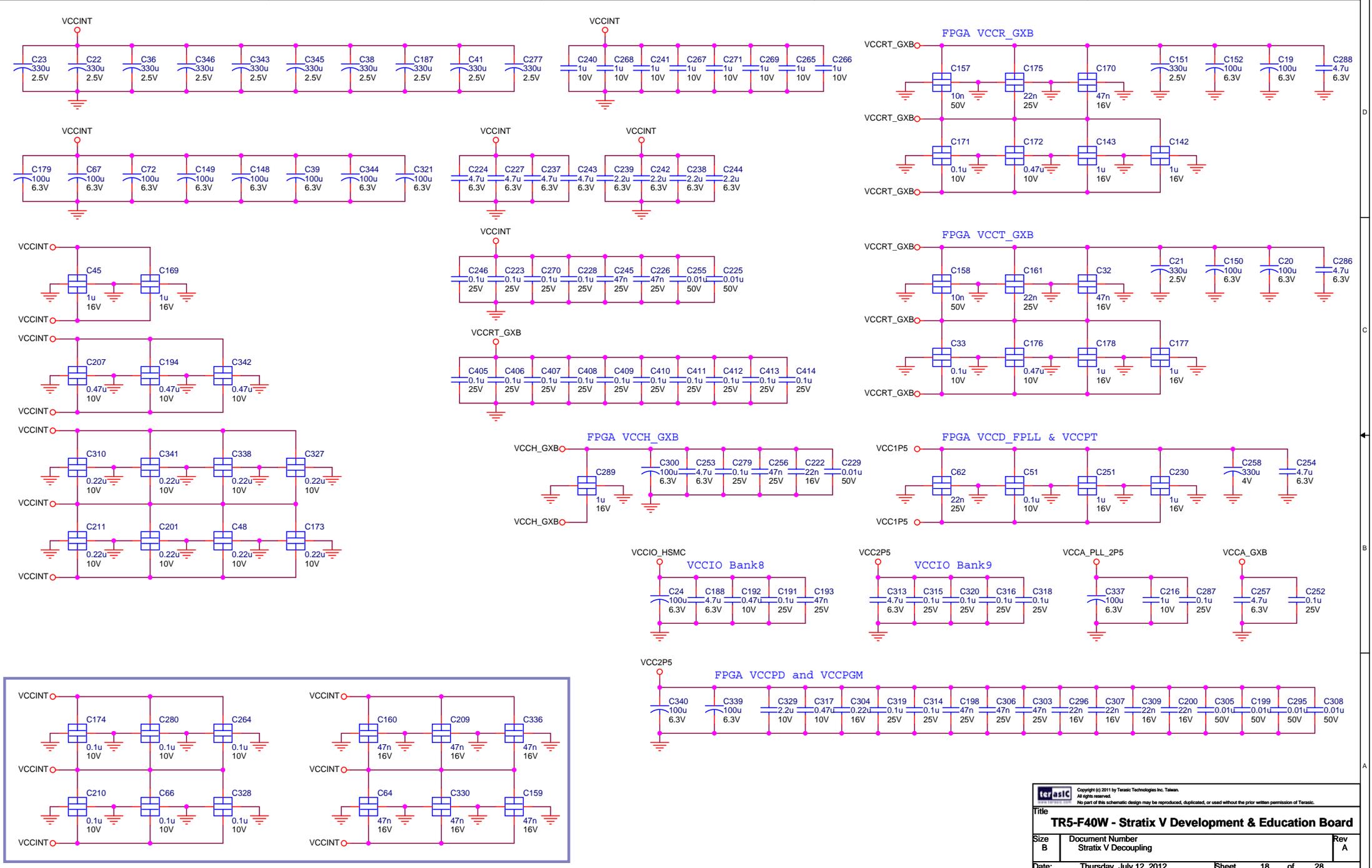


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PIN VERSION : 1.1
DATE : 2012-02-23

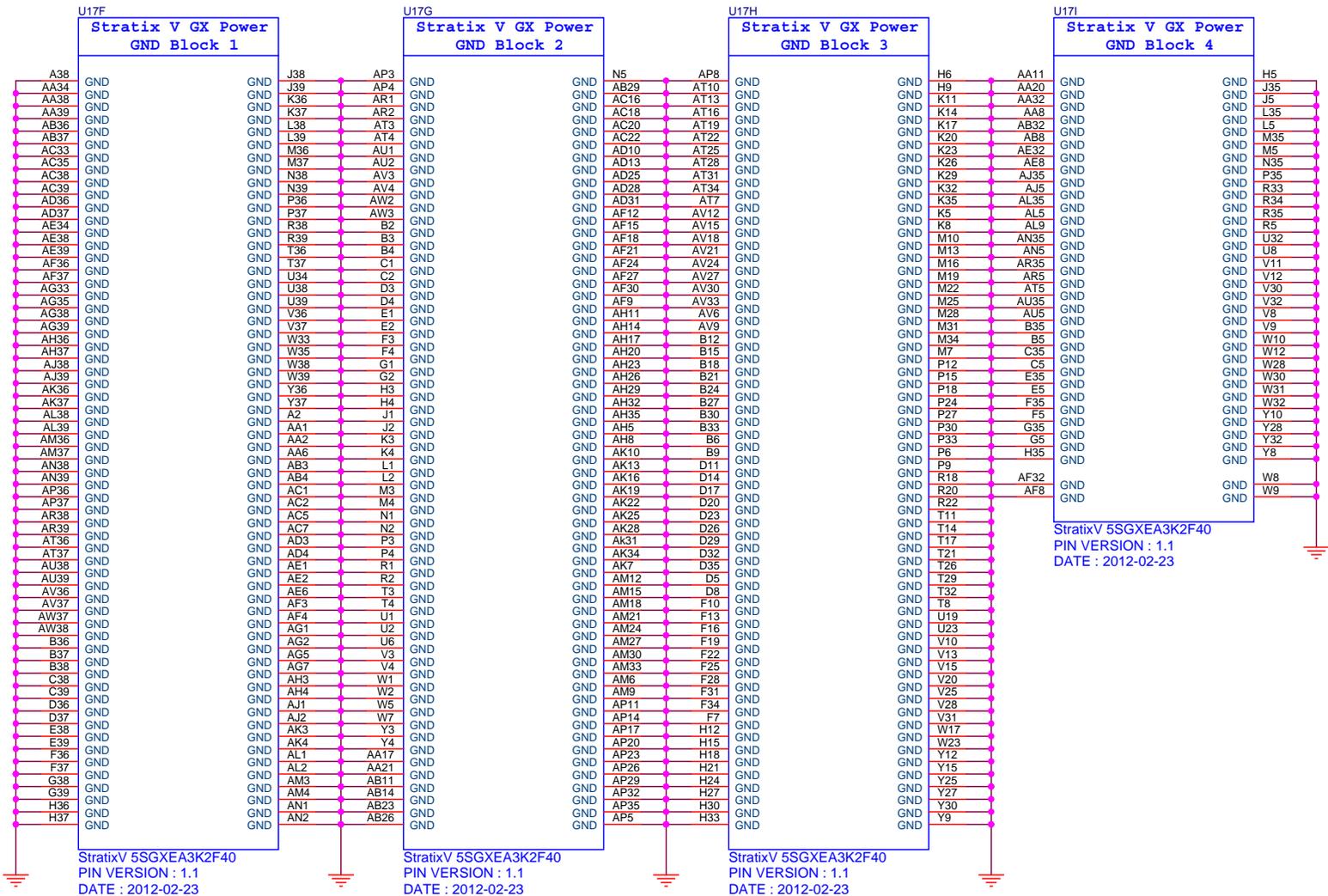


StratixV 5SGXEA3K2F40
PIN VERSION : 1.1
DATE : 2012-02-23

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Title TR5-F40W - Stratix V Development & Education Board		
Size B	Document Number FPGA Power	Rev A
Date: Wednesday, July 11, 2012 Sheet 17 of 28		



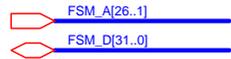
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Title TR5-F40W - Stratix V Development & Education Board		
Size B	Document Number Stratix V Decoupling	Rev A
Date: Thursday, July 12, 2012	Sheet 18	of 28



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PIN VERSION : 1.1
DATE : 2012-02-23

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Title TR5-F40W - Stratix V Development & Education Board		
Size B	Document Number FPGA GND	Rev A
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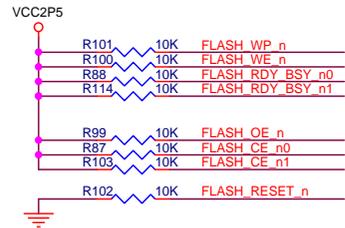
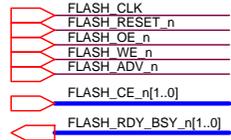
FSM Bus



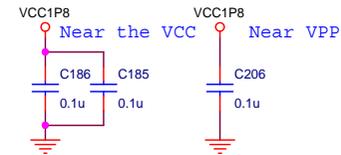
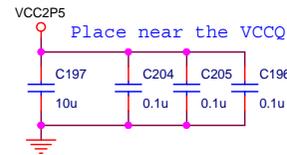
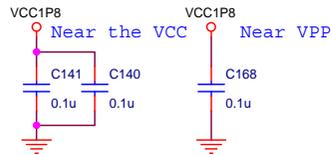
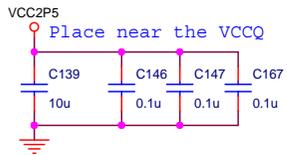
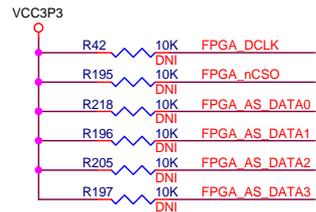
TO SSRAM



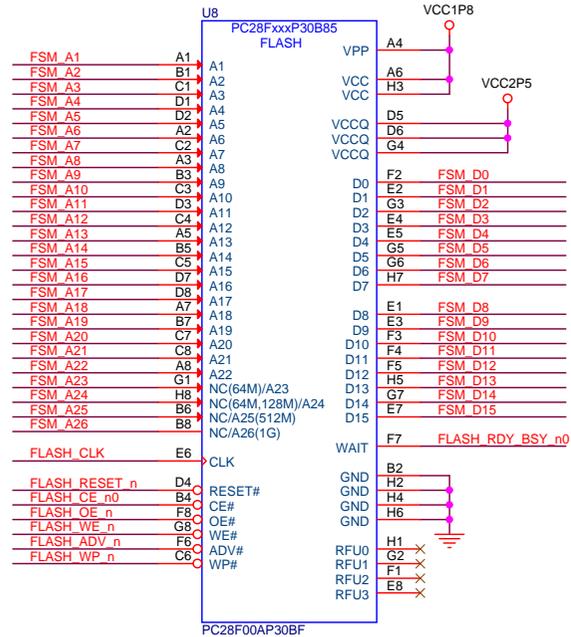
FLASH control signal



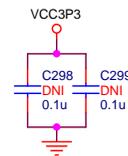
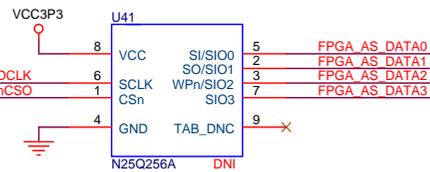
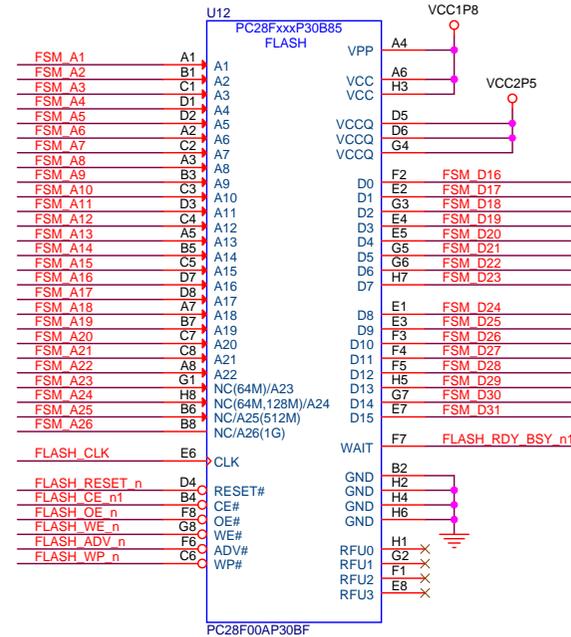
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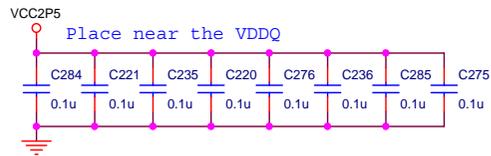
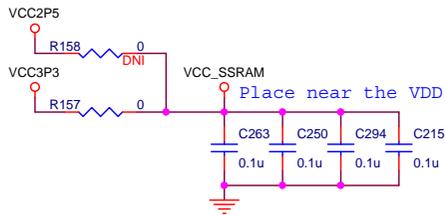


FLASH 1Gb (64M X 16)



FLASH 1Gb (64M X 16)



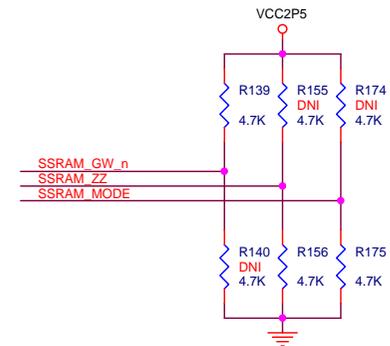
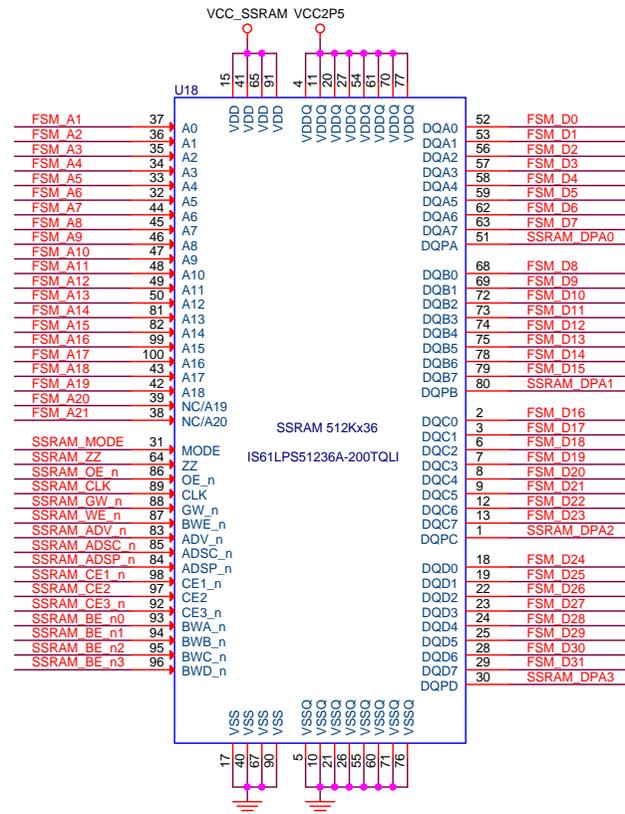
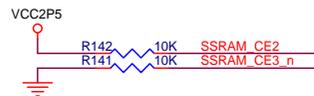
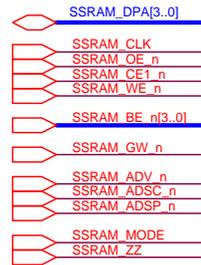


SSRAM

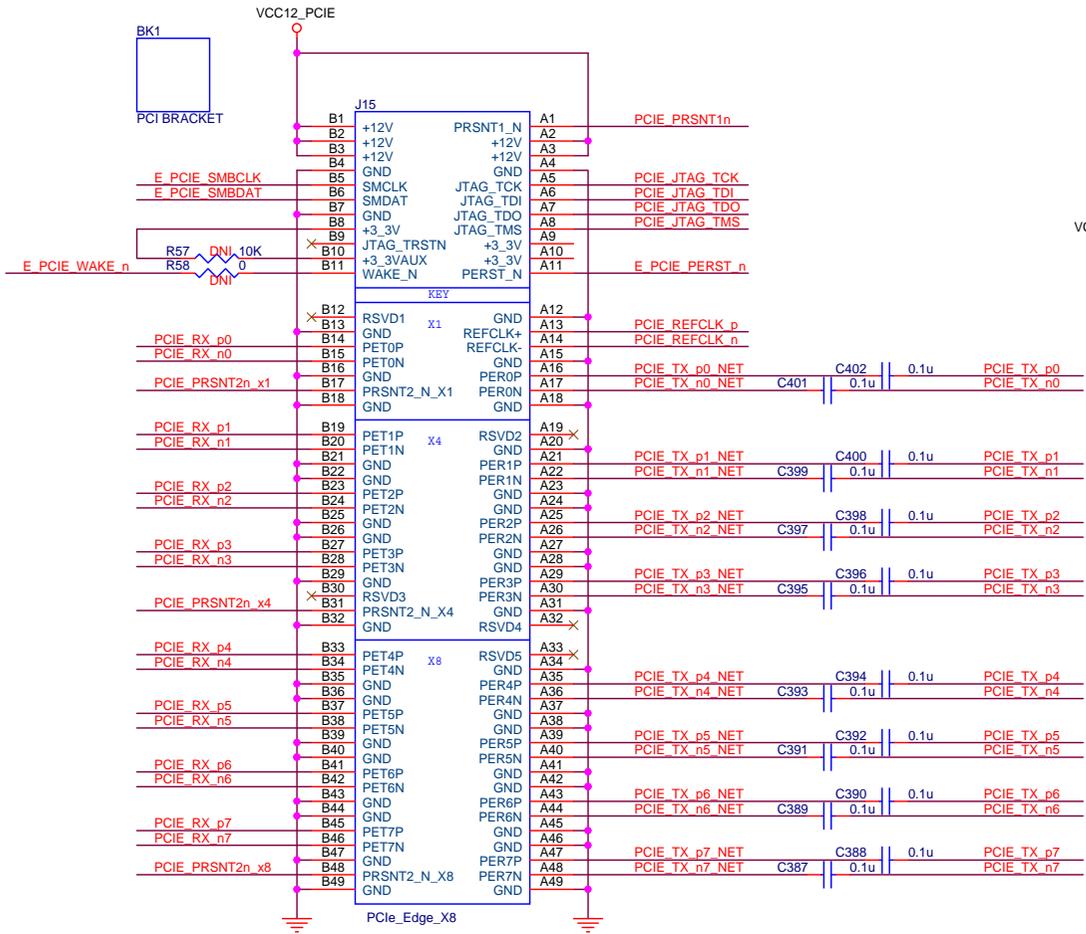
FSM BUS



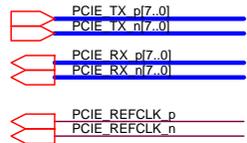
SSRAM Interface



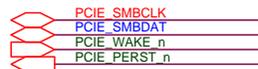
PCIe x8 Edge Connector



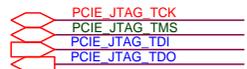
PCIe Transceiver



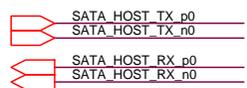
PCIe Control signal



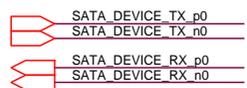
PCIe JTAG (3.3V)



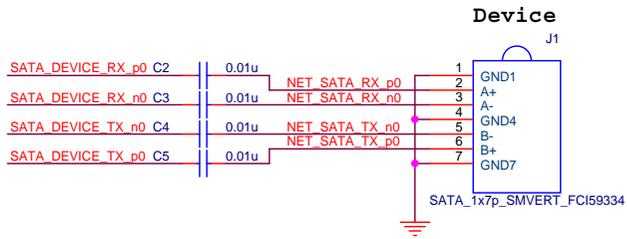
SATA HOST



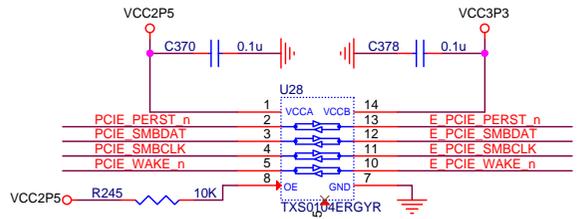
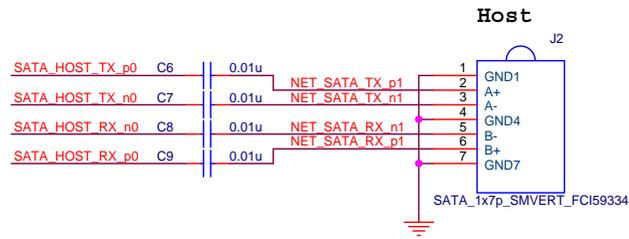
SATA DEVICE



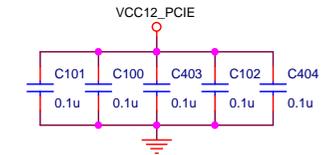
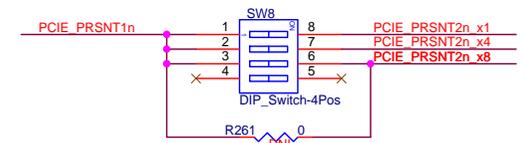
SATA Connector



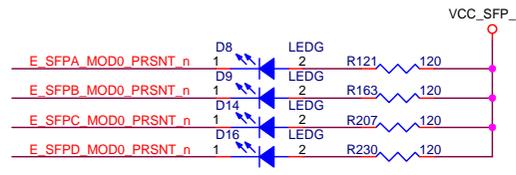
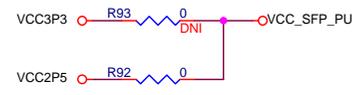
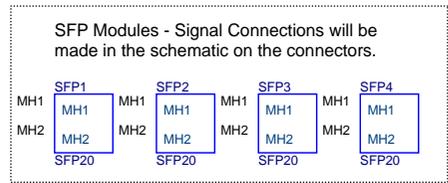
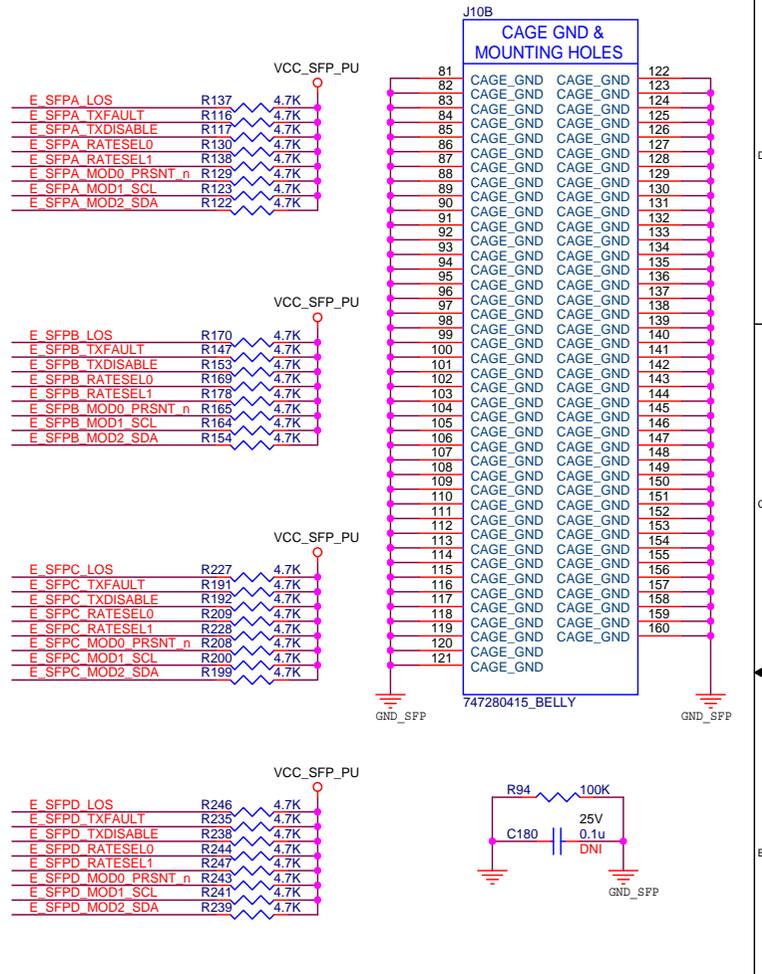
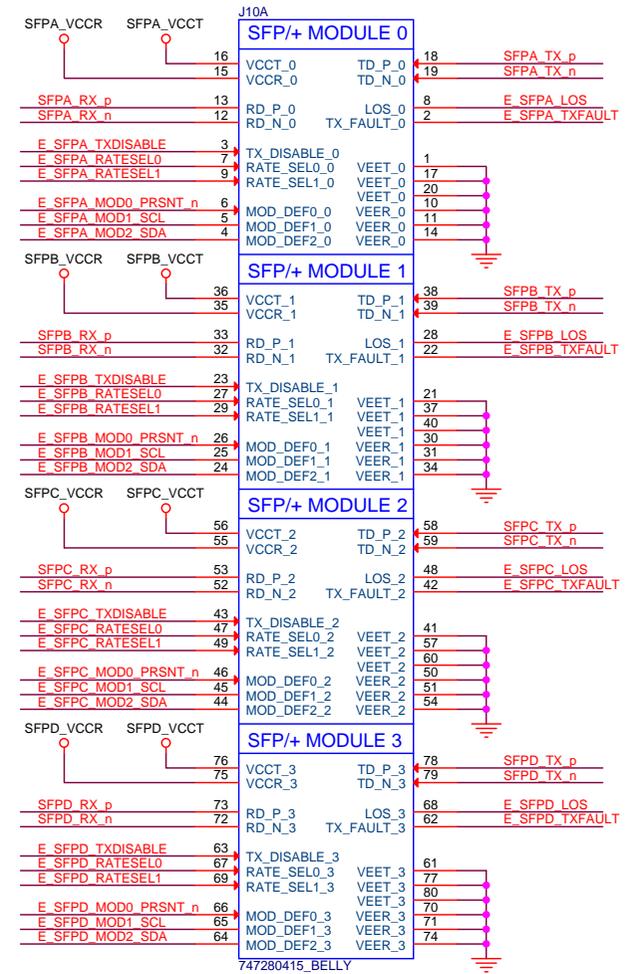
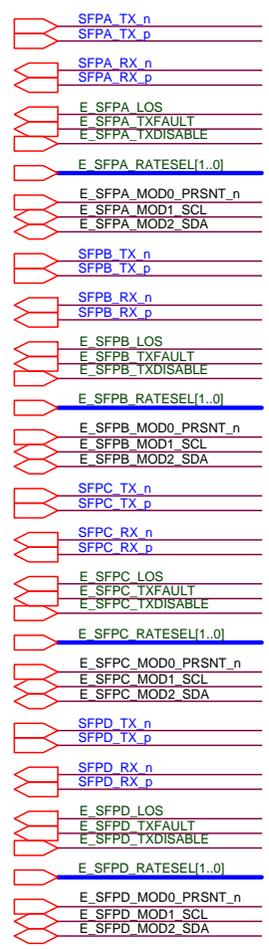
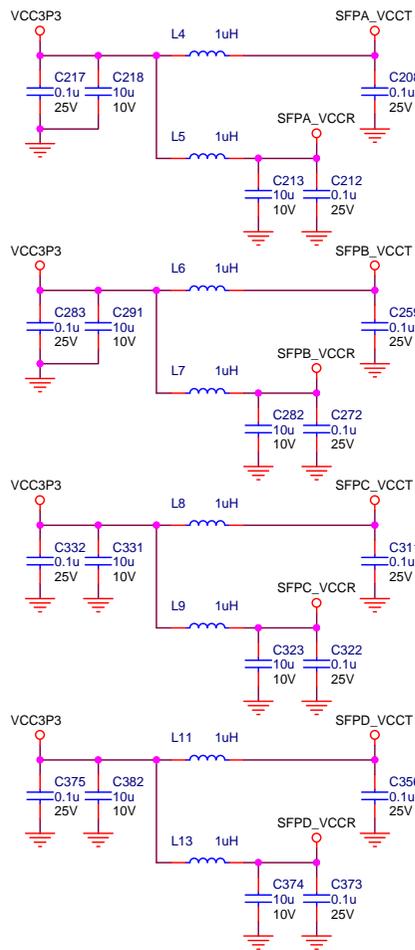
SATA Connector



PCIe Mode Select



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Title TR5-F40W - Stratix V Development & Education Board		
Size B	Document Number PCI Express x8 lane, PCIe JTAG, and SATA port	Rev A
Date: Thursday, July 12, 2012	Sheet 22	of 28



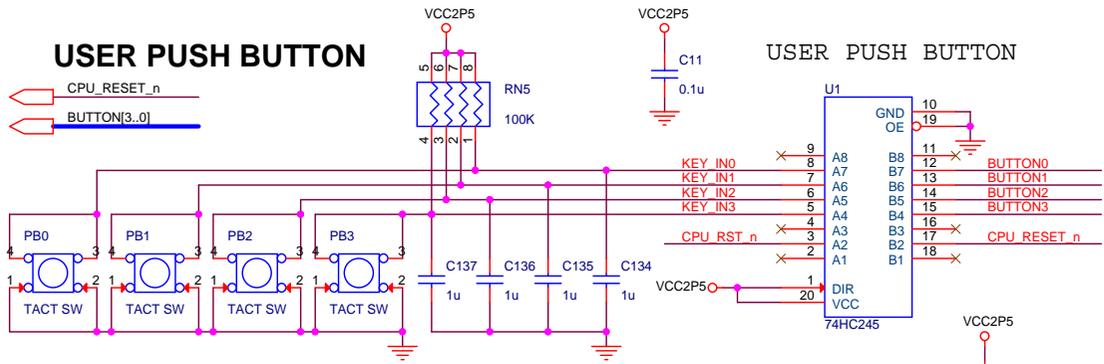
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Title: **TR5-F40W - Stratix V Development & Education Board**

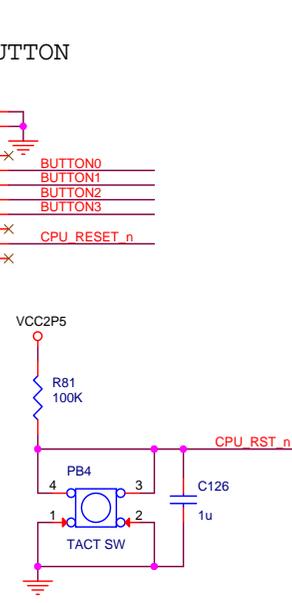
Size B Document Number: Quad SFP+ Interface Rev A

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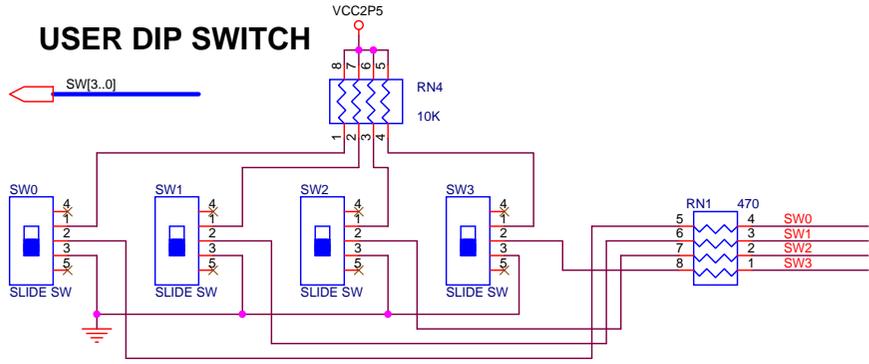
USER PUSH BUTTON



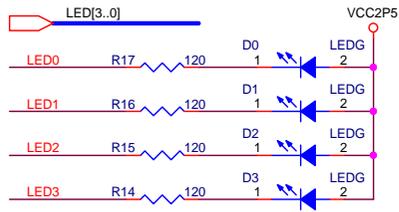
USER PUSH BUTTON



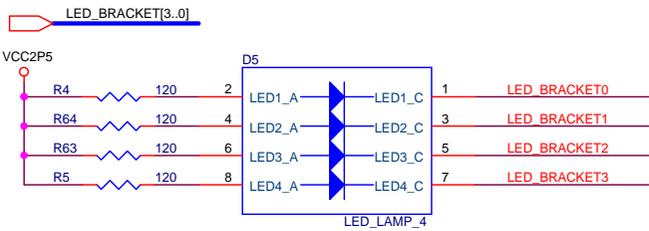
USER DIP SWITCH



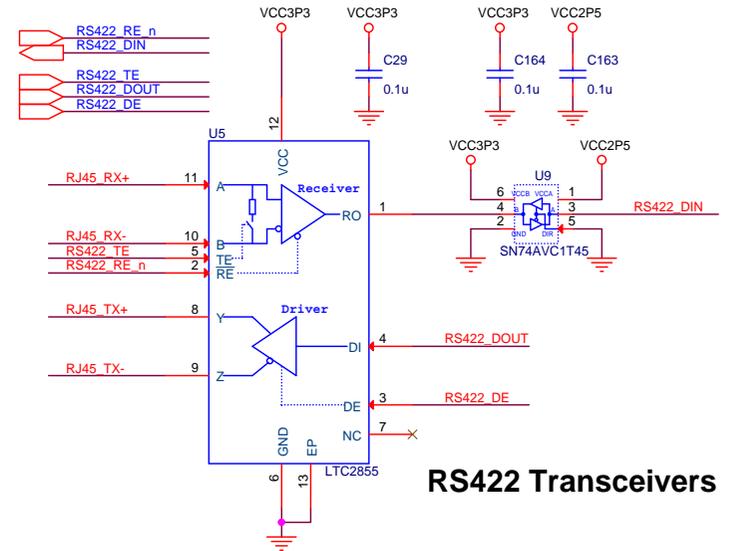
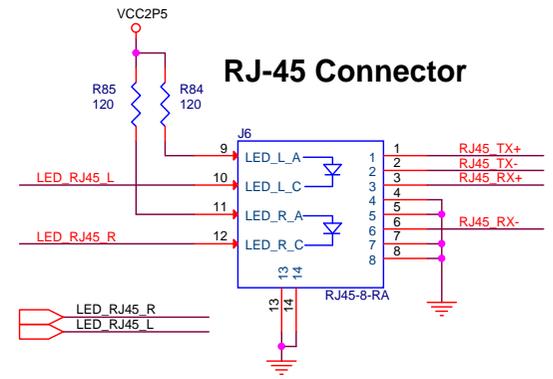
USER LEDs



Housing LED Lamps with four LEDs



RJ-45 Connector



RS422 Transceivers