TR5-Lite Board

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Title	**TR5-Lite Board**	
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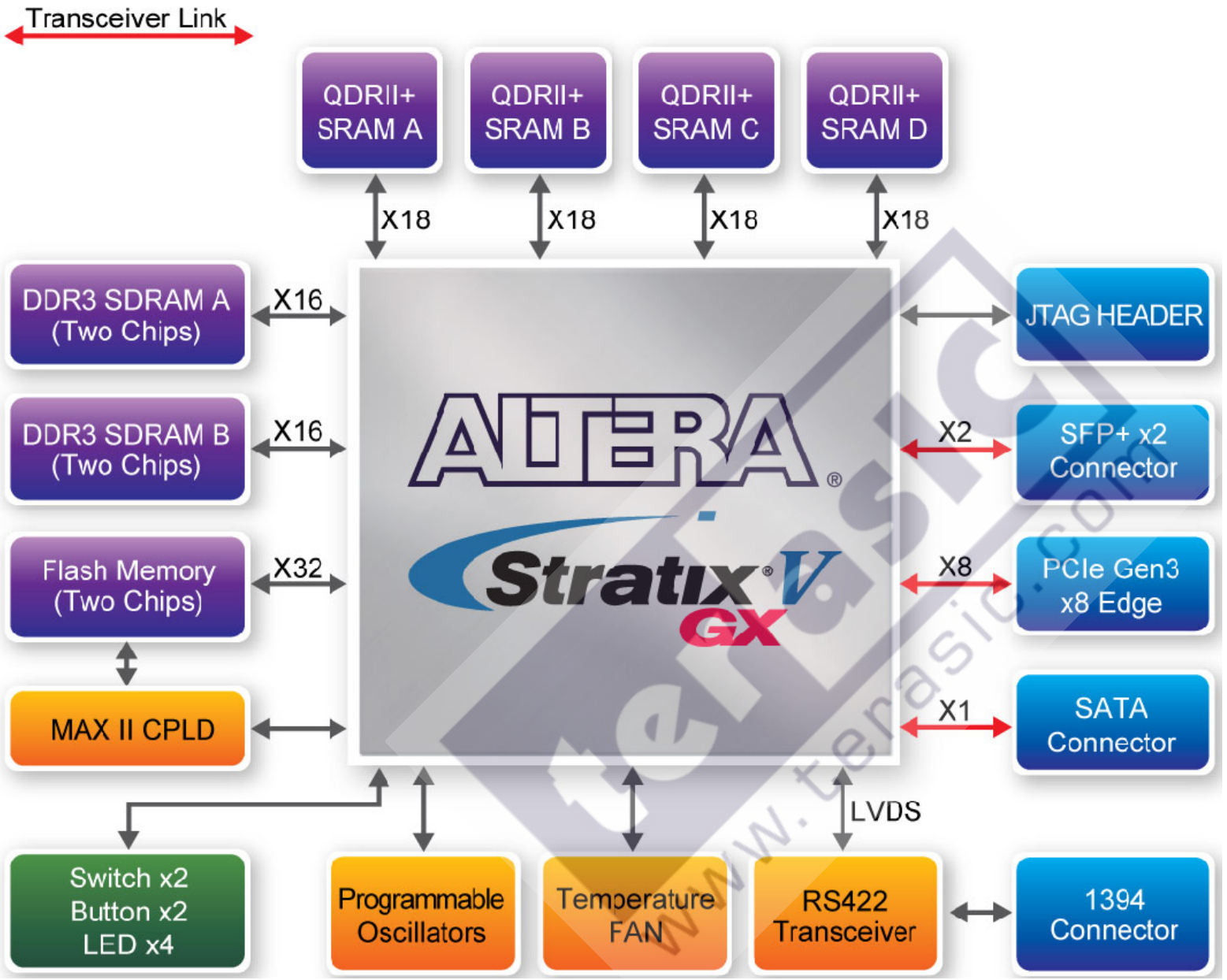

Title	TR5-Lite Board	
Size B	Document Number Block Diagram	Rev D
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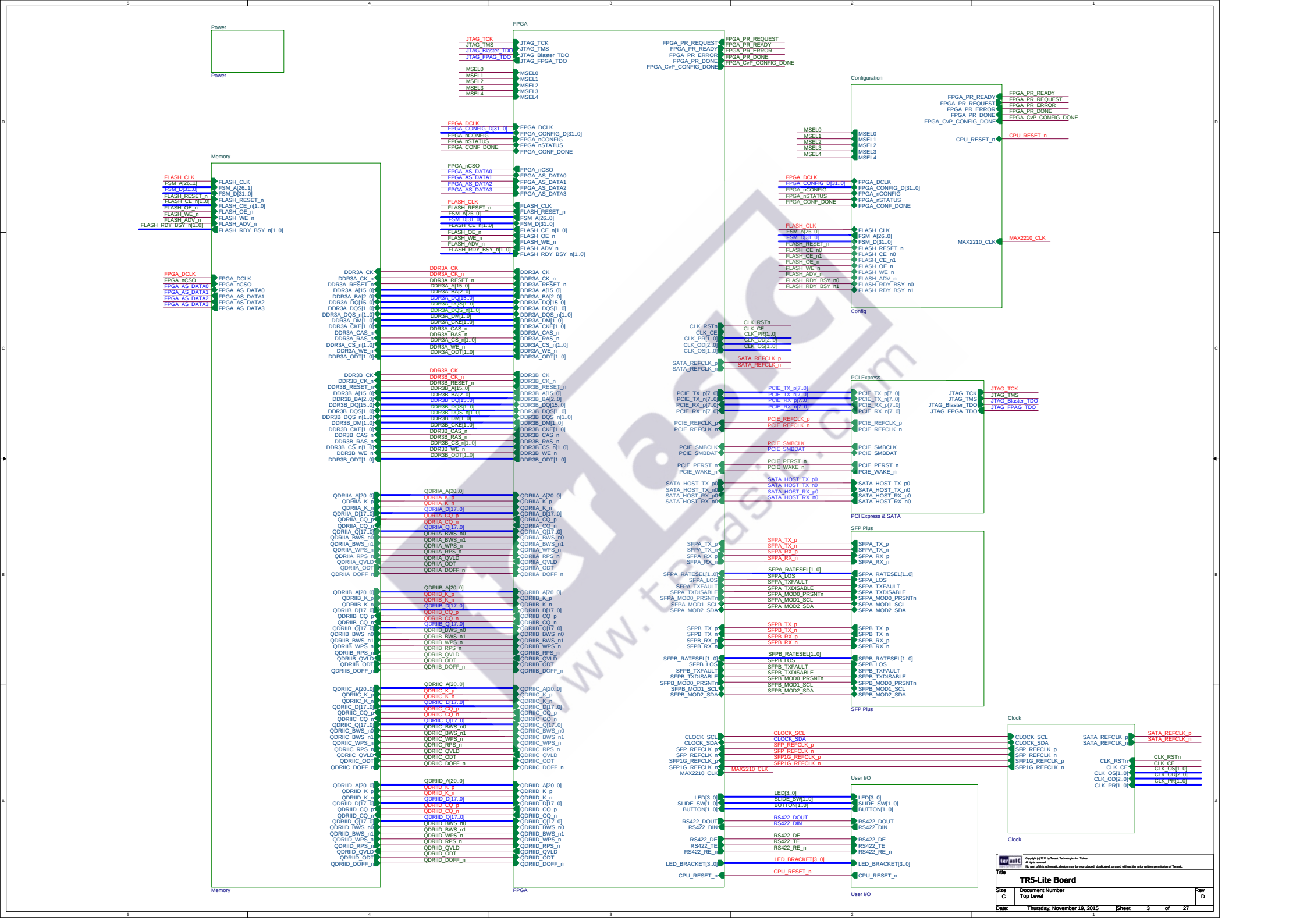
Power
Power
FPGA
JTAG_TCK
JTAG_TMS
JTAG_Blaster_TDO
JTAG_FPAG_TDO
JTAG_FPGA_TDO
MSEL0
MSEL1
MSEL2
MSEL3
MSEL4
FPGA_DCLK
FPGA_CONFIG_D[31..0]
FPGA_nCONFIG
FPGA_nSTATUS
FPGA_CONF_DONE
FPGA_nCSO
FPGA_AS_DATA0
FPGA_AS_DATA1
FPGA_AS_DATA2
FPGA_AS_DATA3
FLASH_CLK
FLASH_RESET_n
FSM_A[26..0]
FSM_D[31..0]
FLASH_CE_n[1..0]
FLASH_OE_n
FLASH_WE_n
FLASH_ADV_n
FLASH_RDY_BSY_n[1..0]
FPGA_PR_REQUEST
FPGA_PR_READY
FPGA_PR_ERROR
FPGA_PR_DONE
FPGA_CvP_CONFIG_DONE
Configuration
CPU_RESET_n
MAX2210_CLK
Config
Memory
DDR3A_CK
DDR3A_CK_n
DDR3A_RESET_n
DDR3A_A[15..0]
DDR3A_BA[2..0]
DDR3A_DQ[15..0]
DDR3A_DQS[1..0]
DDR3A_DQS_n[1..0]
DDR3A_DM[1..0]
DDR3A_CKE[1..0]
DDR3A_CAS_n
DDR3A_RAS_n
DDR3A_CS_n[1..0]
DDR3A_WE_n
DDR3A_ODT[1..0]
DDR3B_CK
DDR3B_CK_n
DDR3B_RESET_n
DDR3B_A[15..0]
DDR3B_BA[2..0]
DDR3B_DQ[15..0]
DDR3B_DQS[1..0]
DDR3B_DQS_n[1..0]
DDR3B_DM[1..0]
DDR3B_CKE[1..0]
DDR3B_CAS_n
DDR3B_RAS_n
DDR3B_CS_n[1..0]
DDR3B_WE_n
DDR3B_ODT[1..0]
QDRIIA_A[20..0]
QDRIIA_K_p
QDRIIA_K_n
QDRIIA_D[17..0]
QDRIIA_CQ_p
QDRIIA_CQ_n
QDRIIA_Q[17..0]
QDRIIA_BWS_n0
QDRIIA_BWS_n1
QDRIIA_WPS_n
QDRIIA_RPS_n
QDRIIA_QVLD
QDRIIA_ODT
QDRIIA_DOFF_n
QDRIIB_A[20..0]
QDRIIB_K_p
QDRIIB_K_n
QDRIIB_D[17..0]
QDRIIB_CQ_p
QDRIIB_CQ_n
QDRIIB_Q[17..0]
QDRIIB_BWS_n0
QDRIIB_BWS_n1
QDRIIB_WPS_n
QDRIIB_RPS_n
QDRIIB_QVLD
QDRIIB_ODT
QDRIIB_DOFF_n
QDRIIC_A[20..0]
QDRIIC_K_p
QDRIIC_K_n
QDRIIC_D[17..0]
QDRIIC_CQ_p
QDRIIC_CQ_n
QDRIIC_Q[17..0]
QDRIIC_BWS_n0
QDRIIC_BWS_n1
QDRIIC_WPS_n
QDRIIC_RPS_n
QDRIIC_QVLD
QDRIIC_ODT
QDRIIC_DOFF_n
QDRIID_A[20..0]
QDRIID_K_p
QDRIID_K_n
QDRIID_D[17..0]
QDRIID_CQ_p
QDRIID_CQ_n
QDRIID_Q[17..0]
QDRIID_BWS_n0
QDRIID_BWS_n1
QDRIID_WPS_n
QDRIID_RPS_n
QDRIID_QVLD
QDRIID_ODT
QDRIID_DOFF_n
CLK_RSTn
CLK_CE
CLK_PR[1..0]
CLK_OD[2..0]
CLK_OS[1..0]
SATA_REFCLK_p
SATA_REFCLK_n
PCIE_TX_p[7..0]
PCIE_TX_n[7..0]
PCIE_RX_p[7..0]
PCIE_RX_n[7..0]
PCIE_REFCLK_p
PCIE_REFCLK_n
PCIE_SMBCLK
PCIE_SMBDAT
PCIE_PERST_n
PCIE_WAKE_n
SATA_HOST_TX_p0
SATA_HOST_TX_n0
SATA_HOST_RX_p0
SATA_HOST_RX_n0
PCI Express
PCI Express & SATA
JTAG_TCK
JTAG_TMS
JTAG_Blaster_TDO
JTAG_FPAG_TDO
SFP Plus
SFPA_TX_p
SFPA_TX_n
SFPA_RX_p
SFPA_RX_n
SFPA_RATESEL[1..0]
SFPA_LOS
SFPA_TXFAULT
SFPA_TXDISABLE
SFPA_MOD0_PRSNTn
SFPA_MOD1_SCL
SFPA_MOD2_SDA
SFPB_TX_p
SFPB_TX_n
SFPB_RX_p
SFPB_RX_n
SFPB_RATESEL[1..0]
SFPB_LOS
SFPB_TXFAULT
SFPB_TXDISABLE
SFPB_MOD0_PRSNTn
SFPB_MOD1_SCL
SFPB_MOD2_SDA
SFP Plus
Clock
CLOCK_SCL
CLOCK_SDA
SFP_REFCLK_p
SFP_REFCLK_n
SFP1G_REFCLK_p
SFP1G_REFCLK_n
MAX2210_CLK
CLK_RSTn
CLK_CE
CLK_OS[1..0]
CLK_OD[2..0]
CLK_PR[1..0]
Clock
User I/O
LED[3..0]
SLIDE_SW[1..0]
BUTTON[1..0]
RS422_DOUT
RS422_DIN
RS422_DE
RS422_TE
RS422_RE_n
LED_BRACKET[3..0]
CPU_RESET_n
User I/O
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Title
TR5-Lite Board
Size C
Document Number Top Level
Rev D
Date: Thursday, November 19, 2015
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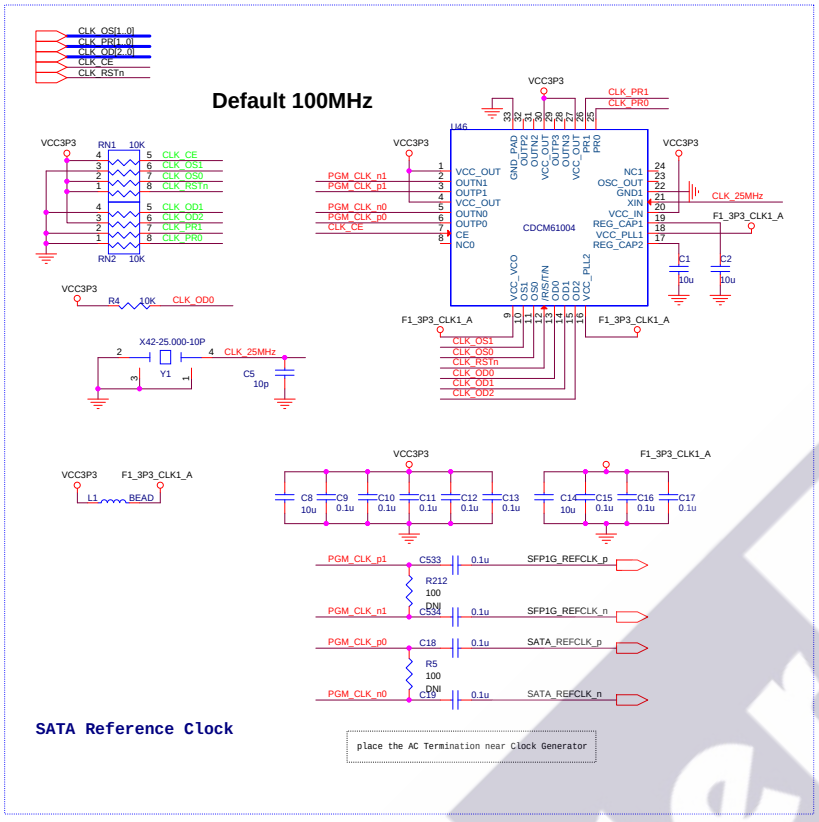
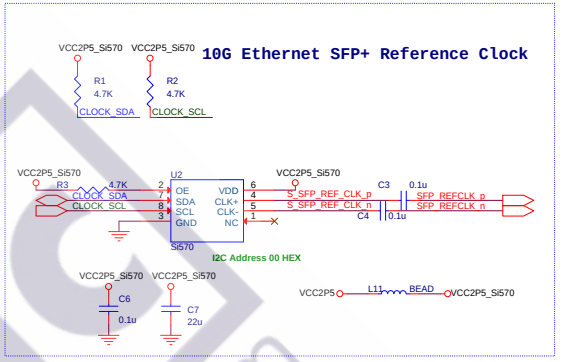
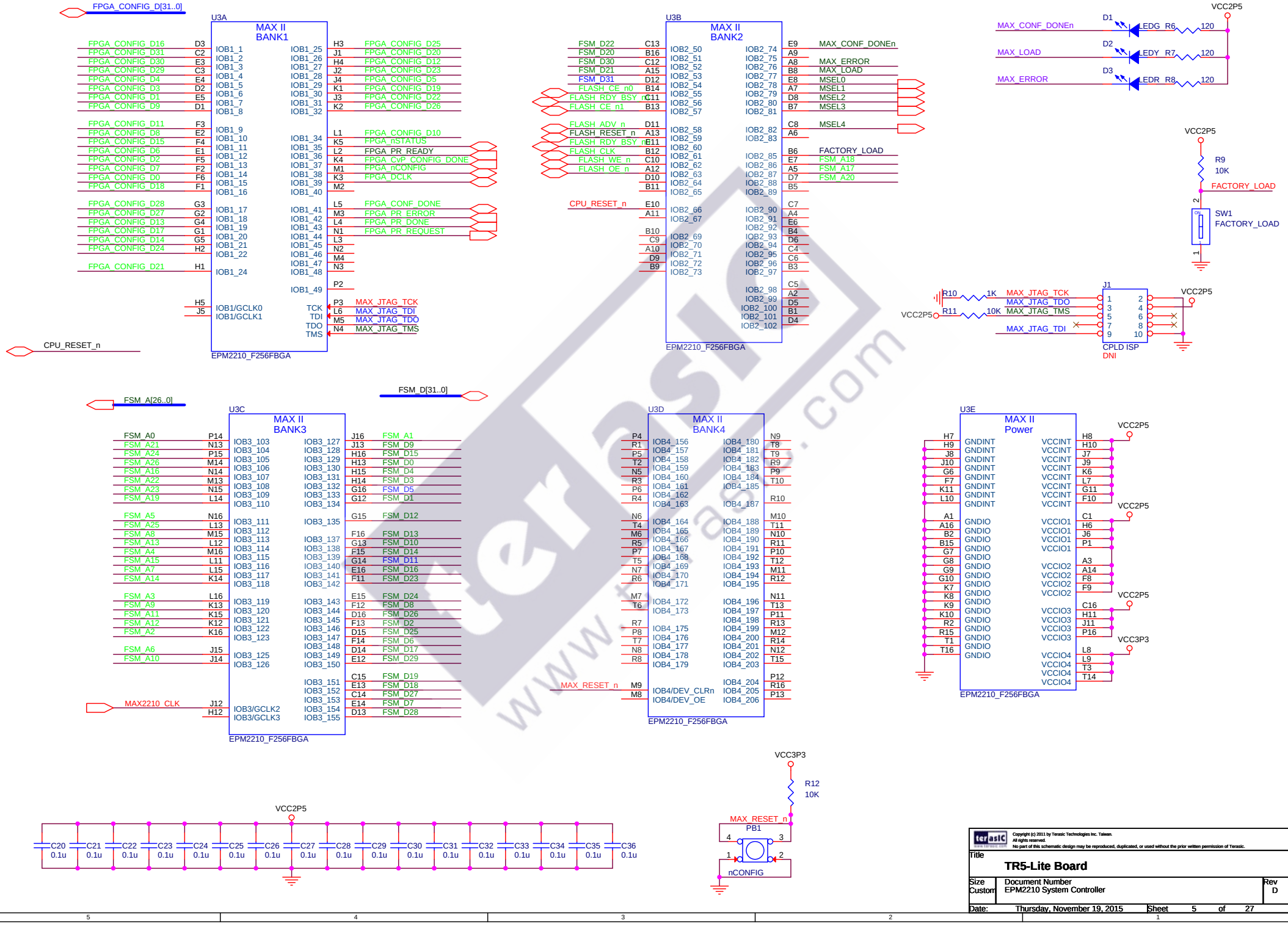




Title	TR5-Lite Board	
Size C	Document Number Programmable Clock	Rev D
Date: Thursday, November 19, 2015	Sheet 4 of 27	



Title
TR5-Lite Board

Size	Document Number	Rev
Custom	EPM2210 System Controller	D

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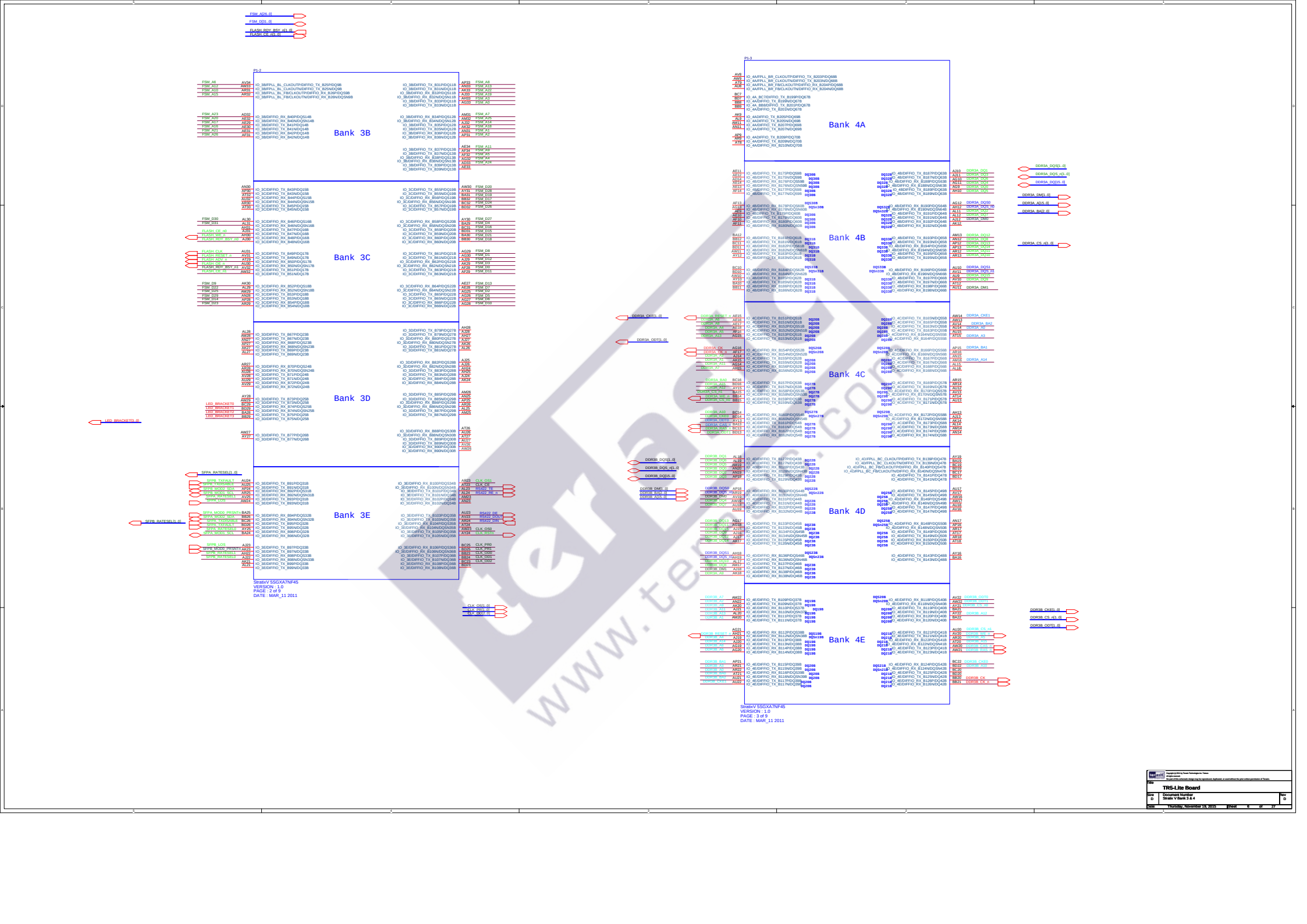
Bank 3B
Bank 3C
Bank 3D
Bank 3E
Bank 4A
Bank 4B
Bank 4C
Bank 4D
Bank 4E
P1-2
P1-3
FSM_A[26..0]
FSM_D[31..0]
FLASH_RDY_BSY_r[1..0]
FLASH_CE_r[1..0]
LED_BRACKET0_r[0..2]
SFPA_RATESEL0_r[1..0]
SFPB_RATESEL0_r[1..0]
DDR3A_DQS[1..0]
DDR3A_DQS_n[1..0]
DDR3A_DQS[15..0]
DDR3A_DM[1..0]
DDR3A_A[15..0]
DDR3A_BA[2..0]
DDR3A_CS_n[1..0]
DDR3A_CKE[1..0]
DDR3A_CK[1..0]
DDR3A_CK_n[1..0]
DDR3A_ODT[1..0]
DDR3A_RESET_n
DDR3B_DQS[1..0]
DDR3B_DQS_n[1..0]
DDR3B_DQS[15..0]
DDR3B_DM[1..0]
DDR3B_A[15..0]
DDR3B_BA[2..0]
DDR3B_CS_n[1..0]
DDR3B_CKE[1..0]
DDR3B_CK[1..0]
DDR3B_CK_n[1..0]
DDR3B_ODT[1..0]
DDR3B_RESET_n
CLK_DS[1..0]
CLK_DS[1..0]_n
CLK_DS[2..0]
StratixV 5SGXA7NF45
VERSION : 1.0
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StratixV 5SGXA7NF45
VERSION : 1.0
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TRS-Lite Board
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Stratix V Bank 3 & 4
Rev
D
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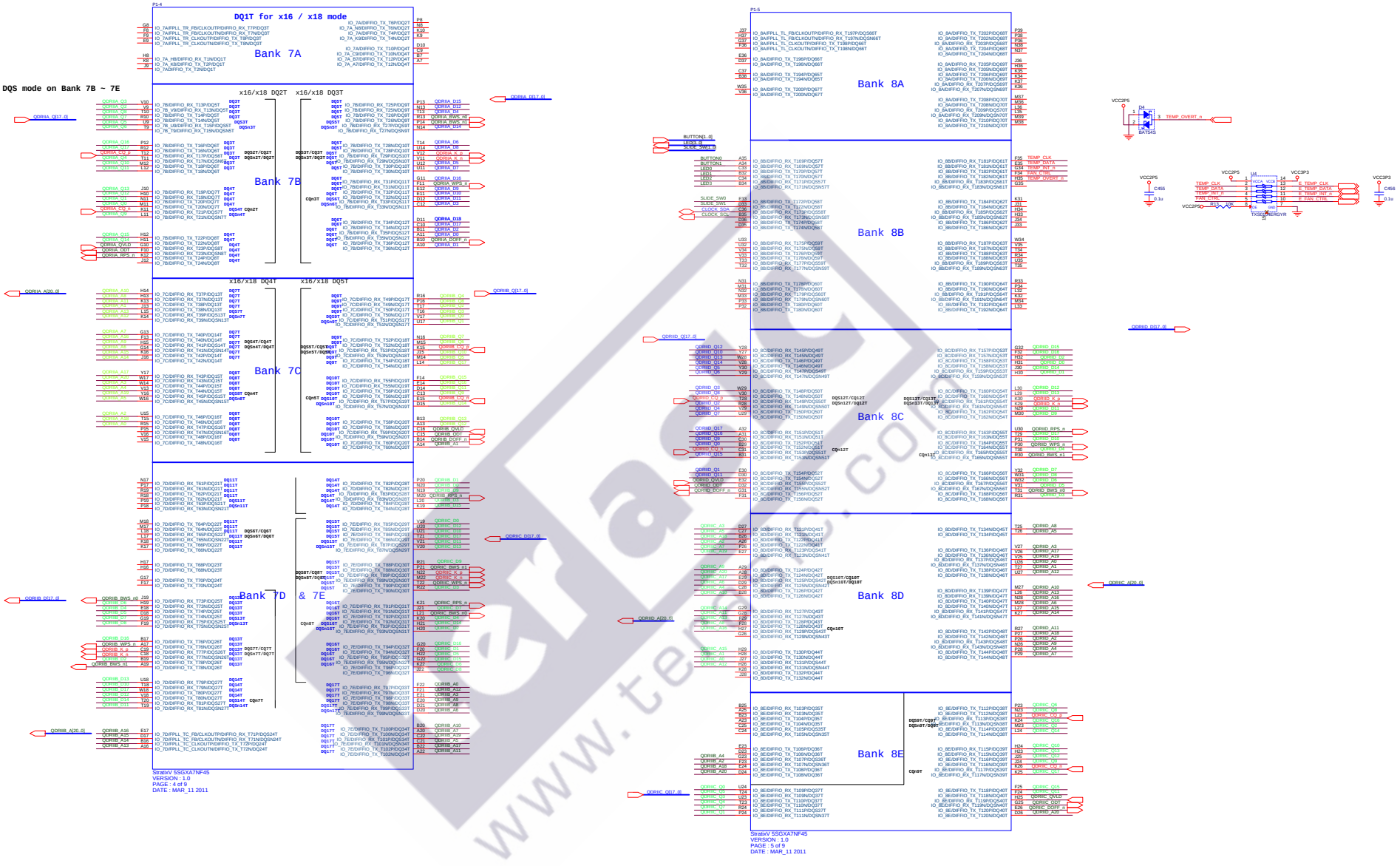
CQ_p & CQ_n is used for x16/x18 DQS mode on Bank 7B ~ 7E




P1-8
Bank BL0
Bank BL1
Bank BL2
Bank BL3
Bank BR0
Bank BR1
Bank BR2
Bank BR3
PCIE_RX_p[7..0]
PCIE_RX_n[7..0]
PCIE_TX_p[7..0]
PCIE_TX_n[7..0]
PCIE_REFCLK_p
PCIE_REFCLK_n
SFPA_RX_p
SFPA_RX_n
SFPB_RX_p
SFPB_RX_n
SFPA_TX_p
SFPA_TX_n
SFPB_TX_p
SFPB_TX_n
SFP_REFCLK_p
SFP_REFCLK_n
SFPTG_REFCLK_p
SFPTG_REFCLK_n
SATA_HOST_RX_p0
SATA_HOST_RX_n0
SATA_HOST_TX_p0
SATA_HOST_TX_n0
SATA_REFCLK_p
SATA_REFCLK_n
TEMPDIODEp
TEMPDIODEn
StratixV 5SGXA7NF45
VERSION : 1.0
PAGE : 8 of 9
DATE : MAR_11 2011
VCC12
Power - FAN
VCC3P3
E_TEMP_CLK
E_TEMP_DATA
E_TEMP_INT_n
E_FAN_CTRL
TEMP_OVERT_n
MAX1619
Address = 0011000b
Title
TR5-Lite Board
Size
Custom
Document Number
Stratix V GXB Bank
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D
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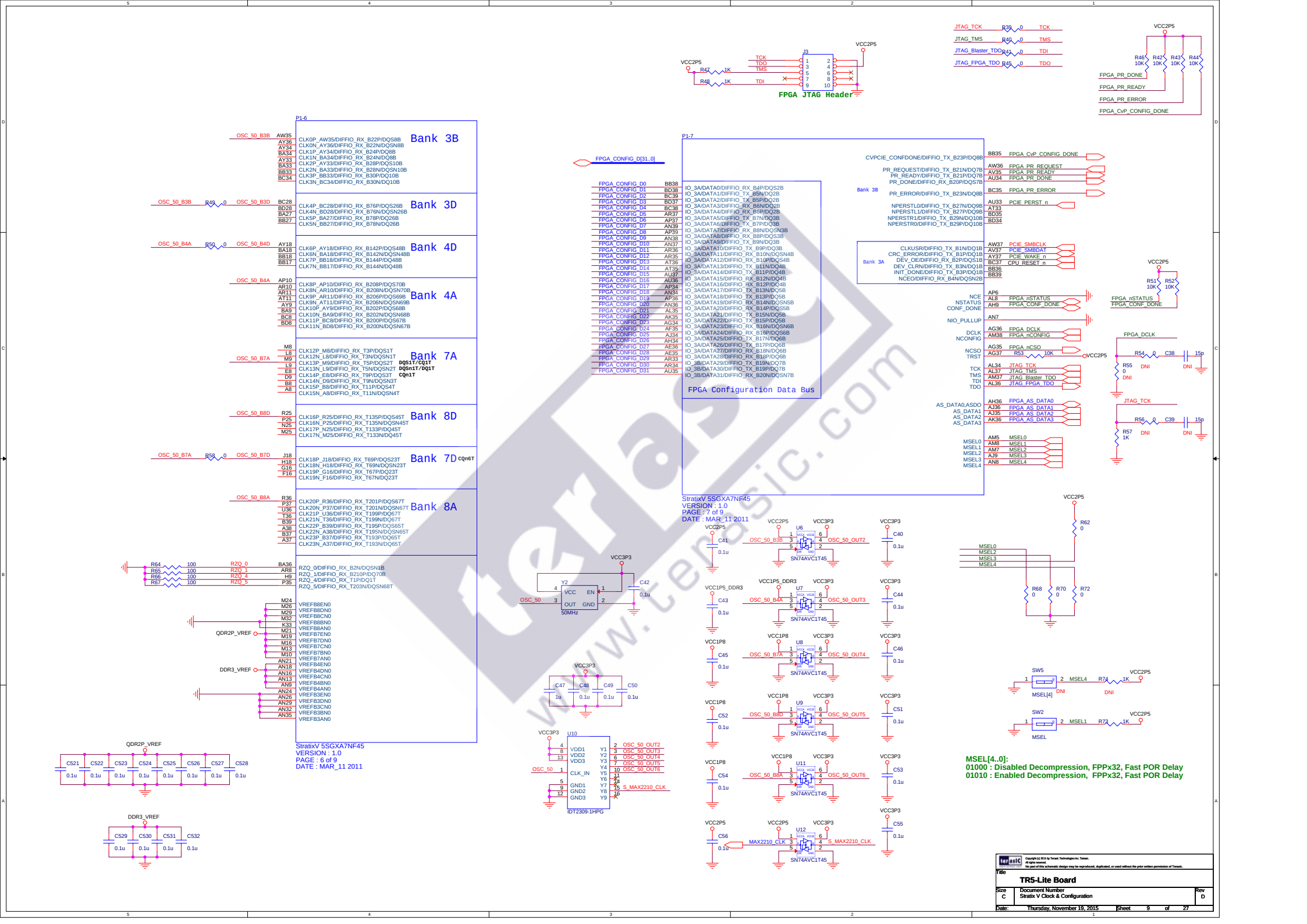
FPGA JTAG Header
Bank 3B
Bank 3D
Bank 4D
Bank 4A
Bank 7A
Bank 8D
Bank 7D
Bank 8A
FPGA Configuration Data Bus
StratixV 5SGXA7NF45
VERSION : 1.0
PAGE : 7 of 9
DATE : MAR_11 2011
StratixV 5SGXA7NF45
VERSION : 1.0
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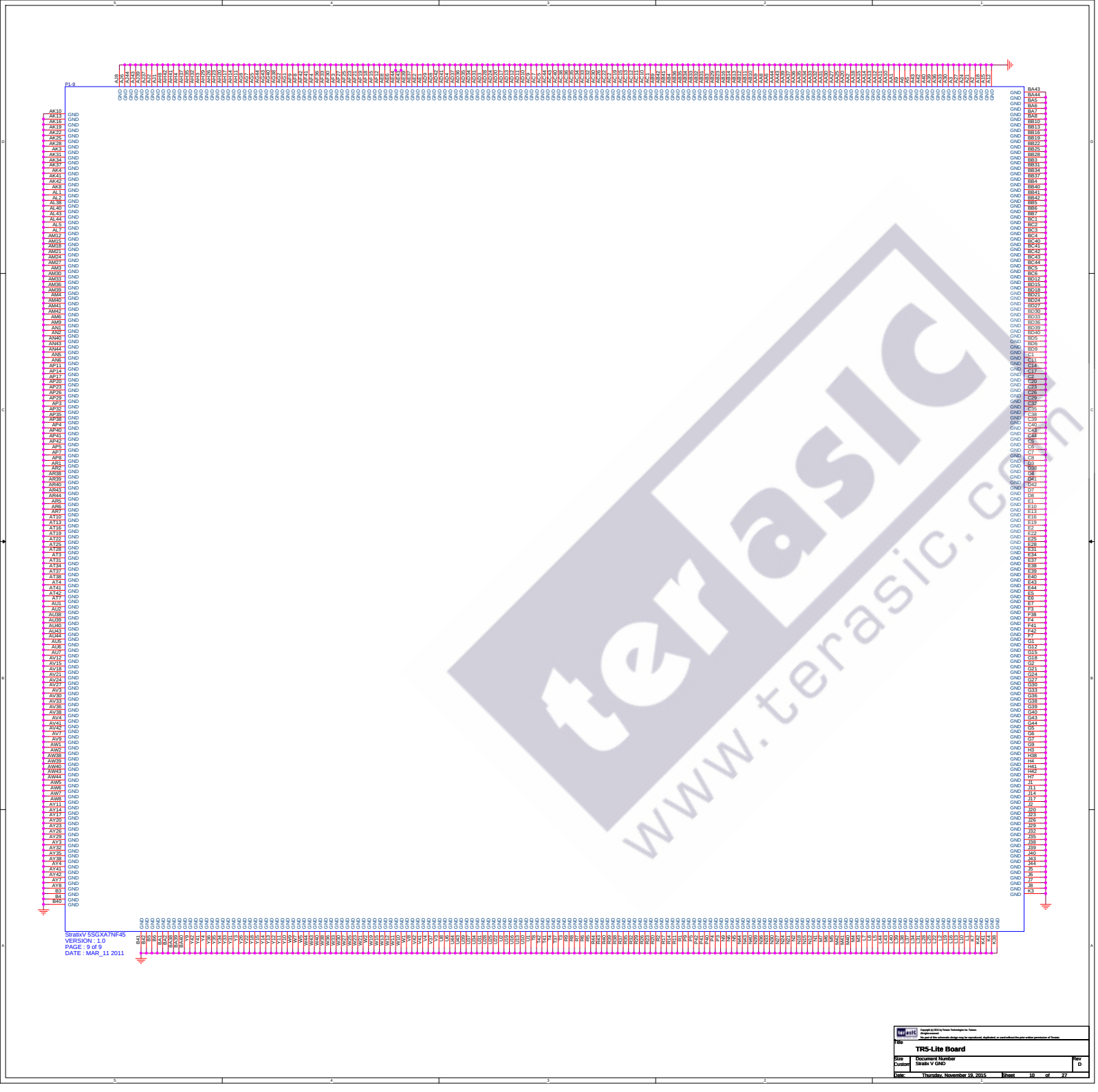
DATE : MAR_11 2011
MSEL[4..0]:
01000 : Disabled Decompression, FPPx32, Fast POR Delay
01010 : Enabled Decompression, FPPx32, Fast POR Delay
TR5-Lite Board
Stratix V Clock & Configuration
Thursday, November 19, 2015



Title: **TR5-Lite Board**

Size	Document Number	Rev
Custom	Stratix V GND	D

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VCC0P85 is set to 0.9V

P1-1

VCC Core: AF20 AF22 AF24 AF26 W20 W22 W24 W26 AA19 AA21 AA22 AA23 AA24 AA26 AB19 AB20 AB21 AB22 AB24 AB25 AB26 AC20 AC21 AC25 AD19 AD21 AD22 AD23 AD25 AD26 AE19 AE20 AE21 AE22 AE23 AE24 AE25 AE26 Y19 Y20 Y21 Y23 Y24 Y25 AC24

VCCPT: AG24 AG31 AH16 V14 V22 V32

VCCPGM: AL33 AL10

VCCBAT: AL13

VCCIO: BA37 BC36 BA35 BC33 BA32 BC30 BA26 BC27 BA23 BC24 BC9 BA11 BC12 BA14 BC15 BA17 BC18 BA20 BC21 B9 B12 D13 B15 D16 B18 D19 B21 D22 B36 F37 B33 D34 B30 D31 B27 D28 B24 D25

VCCPD: AW31 AW34 AW25 AW28 AW12 AW15 AW18 F12 F15 F18 F27 F30 F33

VCCH_GXB: AJ40 AE40 AA40 U40 AJ5 AE5 AA5 U5

VCCR_GXB: AL39 AG39 AC39 W39 AL6 AG6 AC6 W6

VCCT_GXB: AH38 AJ38 AD38 AE38 AA38 AB38 U38 V38 AH7 AJ7 AD7 AE7 AA7 AB7 U7 V7

VCCHIP_L: AA28 AB27 AB28 AC27 AC28 AD27 AA17 AB17

VCCHIP_R: AB18 AC17 AC18 AD18

VCCA_FPLL: AM34 AG22 AM10 P10 V23 N35 AB37 Y37 AB8 Y8

VCCA_GXB: AK40 AF40 Y40 T40 AK5 AF5 Y5 T5

VCCHSSI_L: AA29 AB30 AC29 AC31 AD29 AD30 AA16 AB15

VCCHSSI_R: AC14 AC16 AD15 AD16

VCCD_FPLL: AM35 AG23 AN10 N10 V24 M35 AC37 W37 AC8 W8

VCC_AUX: AK11 AL22 AL32 N34 P11 P22

StratixV 5SGXA7NF45
VERSION : 1.0
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VCC0P85 — Johanson Dielectrics 160X14X224MV4T: C63 0.22u, C58 0.22u, C59 0.22u

VCC0P85 — Johanson Dielectrics 160X18W474MV4E: C60 0.47u, C61 0.47u, C62 0.47u

VCC0P85 — Johanson Dielectrics 160X14W104MV4T: C68 0.1u, C65 0.1u, C66 0.1u, C67 0.1u

VCC0P85: C73 2.2u, C69 2.2u, C70 2.2u, C71 2.2u, C72 2.2u

VCC0P85 — Johanson Dielectrics 160X41W105MV4E: C80 1u, C75 1u, C76 1u, C77 1u, C78 1u, C79 1u

VCC0P85 — Panasonic 2R5TPE330MAZB: C574 330u, C575 330u, C576 330u, C577 330u

VCC0P85 — Panasonic 6TPE100MPB: C90 100u, C87 100u, C88 100u, C89 100u

VCC0P85: C95 10u, C92 10u, C93 10u, C94 10u, C606 10u, C607 10u

VCC0P85: C100 4.7u, C97 4.7u, C98 4.7u, C99 4.7u

VCC0P85: C549 0.1u, C550 0.1u, C551 0.1u, C552 0.1u, C553 0.1u

VCCH_GXB: C594 4.7u, C538 0.1u, C539 0.1u, C540 0.1u, C541 0.1u, C542 0.1u, C595 0.01u, C596 0.01u

VCC0P85 — Panasonic 4TPE470ML: C105 470u, C102 470u, C103 470u, C104 470u

VCC0P85 — Panasonic 2R5TPE330MAZB: C578 330u, C579 330u, C580 330u, C581 330u

VCC0P85: C554 0.1u, C555 0.1u, C556 0.1u, C557 0.1u, C558 0.1u

VCC0P85: C608 0.1u, C609 0.1u, C610 0.1u, C611 0.1u, C612 0.1u

Panasonic 2R5TPE330MAZB: C584 330u, C111 4.7u

VCC1P5_FPGA — Johanson Dielectrics: 500X14W103MV4T C112 10n; 100X14W104MV4T C113 0.1u; 250X14W223MV4T C114 22n; 160X14W473MV4T C115 47n; 160X41W105MV4E C116 1u

VCC1P5_FPGA — R217 0 — VCCH_GXB

VCC2P5: C117 2.2u, C118 22n, C119 0.01u, C120 0.01u, C121 0.01u, C122 4.7n, C123 4.7n, C124 4.7n, C125 4.7n, C126 4.7n, C127 4.7n, C128 4.7n, C129 4.7n, C130 4.7n, C131 4.7n, C132 4.7n, C133 4.7n, C134 0.1u, C135 0.22u, C136 0.22u, C137 100u

VCC1P0_VCCRT: C550 0.1u, C561 0.1u, C562 0.1u, C563 0.1u, C564 0.1u, C565 0.1u, C566 0.1u, C567 0.1u, C568 0.1u

VCCA_PLL: C139 0.1u

VCCA_GXBRL: C138 0.1u, C140 0.1u, C141 4.7u

VCC1P8: C142 47n, C143 1u, C144 100u

VCC1P5_DDR3: C145 0.47u, C146 0.1u, C147 47n, C148 22n, C149 100u, C150 0.47u, C151 0.1u

Panasonic 2R5TPE330MAZB: C152 4.7n, C153 4.7n, C597 330u, C583 330u, C582 330u

Johanson Dielectrics — 250X14W223MV4T C156 22n; 160X14W473MV4T C157 22n, C158 47n, C159 47n; 160X41W105MV4E C160 1u, C161 1u, C162 1u, C163 1u

VCC1P0_VCCRT: C598 4.7u, C599 4.7u, C600 4.7u, C601 4.7u, C602 2.2u, C603 2.2u, C604 2.2u, C605 2.2u

Johanson Dielectrics 160X14X474MV4T: C613 0.47u, C614 0.47u

VCC1P0_VCCRT: DNI C154 330uF, DNI C155 330uF

VCC1P5_FPGA: DNI C110 330uF

VCC0P85: DNI C85 330uF, DNI C82 330uF, DNI C83 330uF, DNI C84 330uF

VCC0P85: DNI C451 330uF, DNI C107 330uF, DNI C108 330uF, DNI C109 330uF

Title: **TR5-Lite Board**

Size	Document Number	Rev
Custom	Stratix V Power	D

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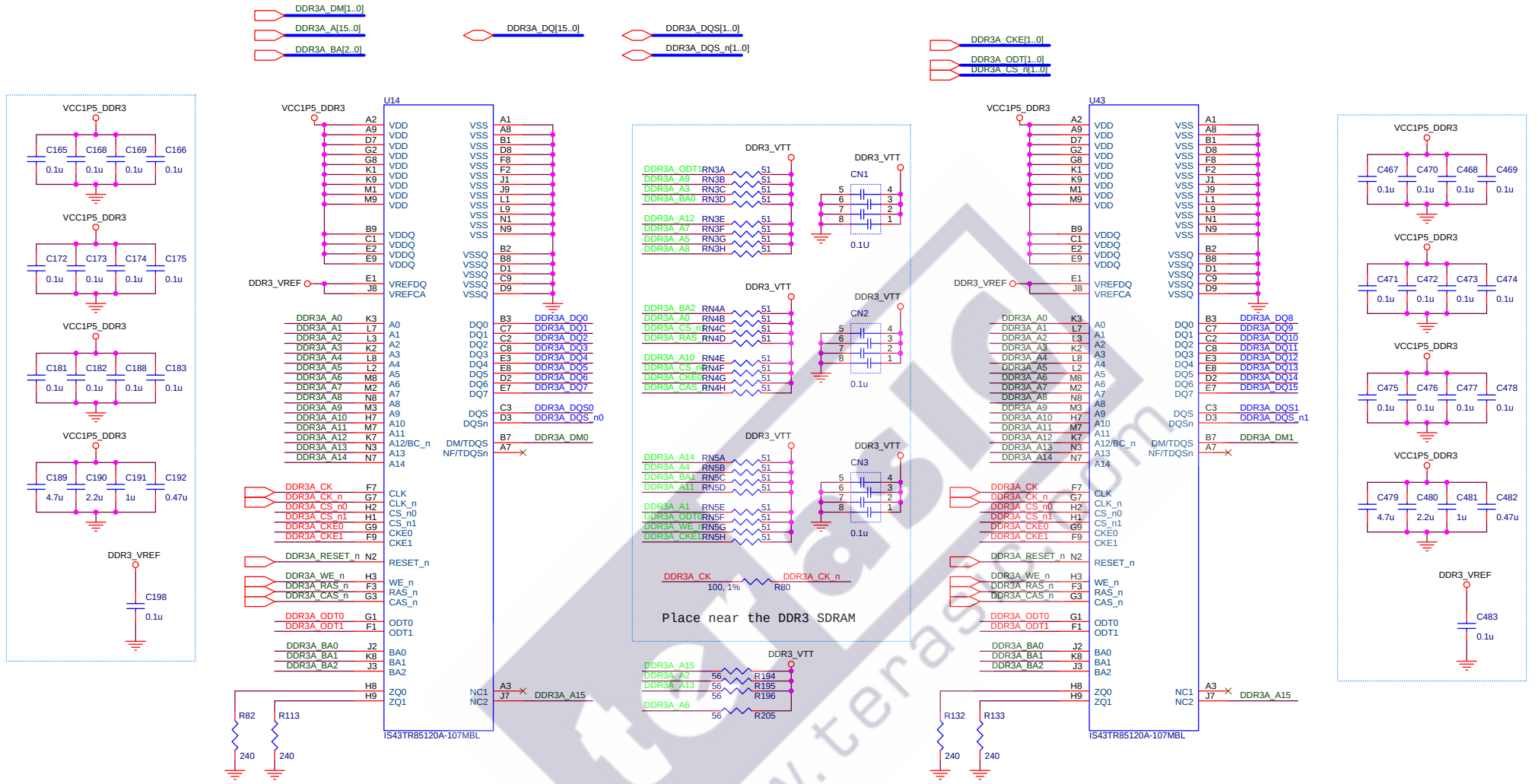

Title	TR5-Lite Board
Size: Custom	Document Number: DDR3 SDRAM Bank A
Rev	D
Date:	Thursday, November 19, 2015
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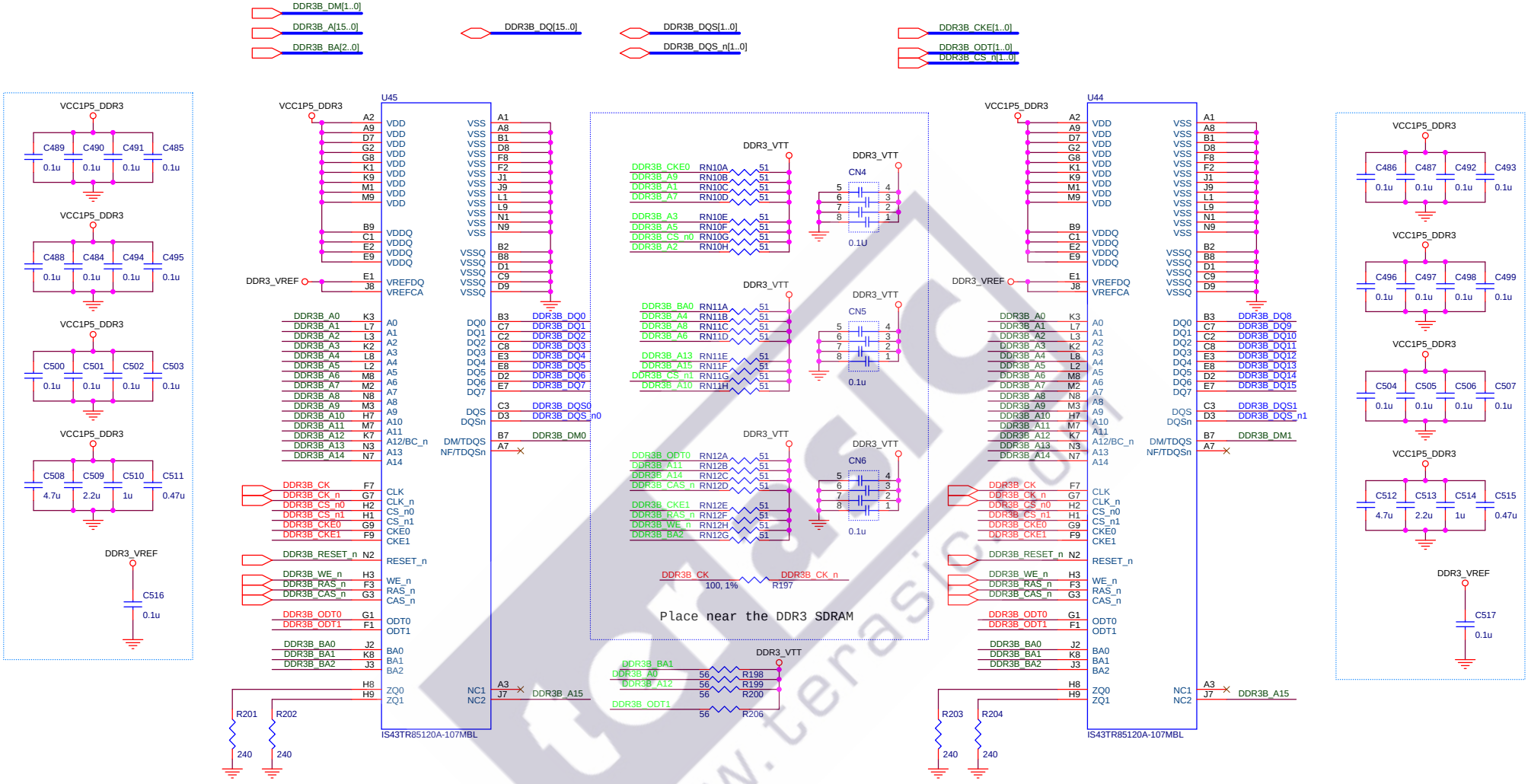

Title	TR5-Lite Board
Size: Custom	Document Number: DDR3 SDRAM Bank B
Rev	D
Date:	Thursday, November 19, 2015
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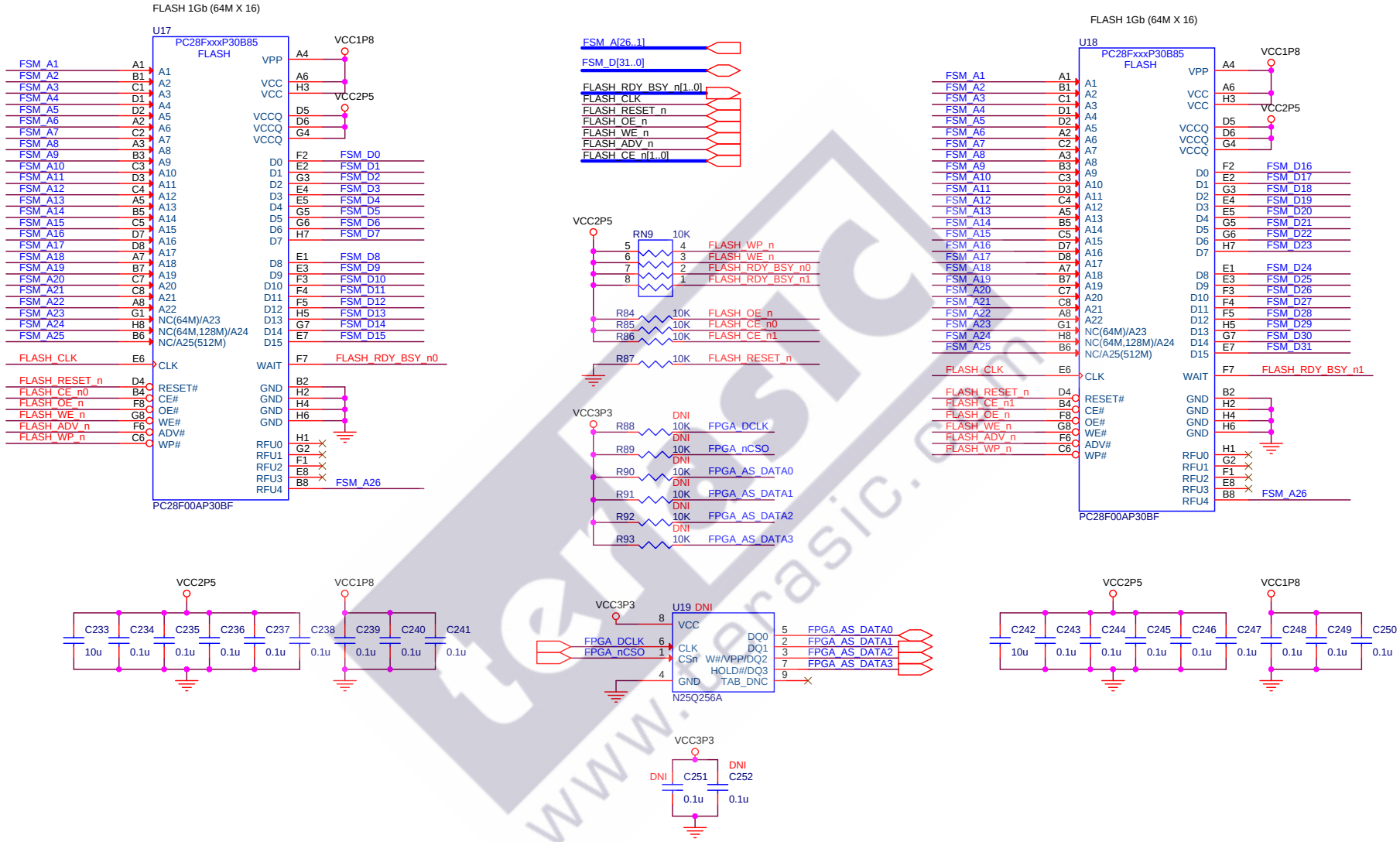

Title: **TR5-Lite Board**

Size	Document Number	Rev
B	CFI FLASH(64M x 32-bits) and EPCS(4-bits)	D

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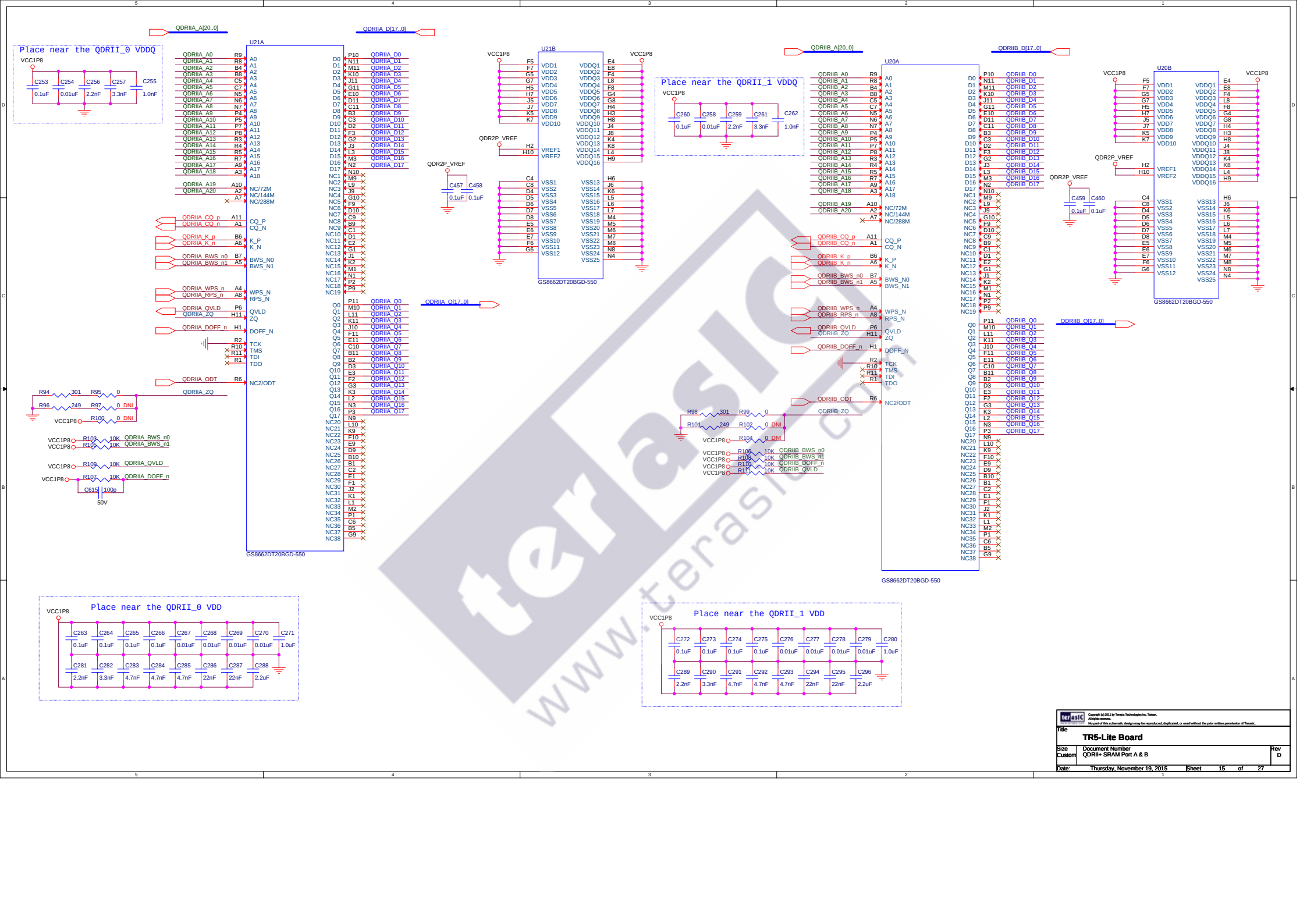
Place near the QDRII_0 VDDQ
Place near the QDRII_1 VDDQ
Place near the QDRII_0 VDD
Place near the QDRII_1 VDD
U21A
U21B
U20A
U20B
GS8662DT20BGD-550
QDRIIA_A[20..0]
QDRIIA_D[17..0]
QDRIIA_Q[17..0]
QDRIIB_A[20..0]
QDRIIB_D[17..0]
QDRIIB_Q[17..0]
QDR2P_VREF
VCC1P8
Title
TR5-Lite Board
Size
Custom
Document Number
QDRII+ SRAM Port A & B
Rev
D
Date:
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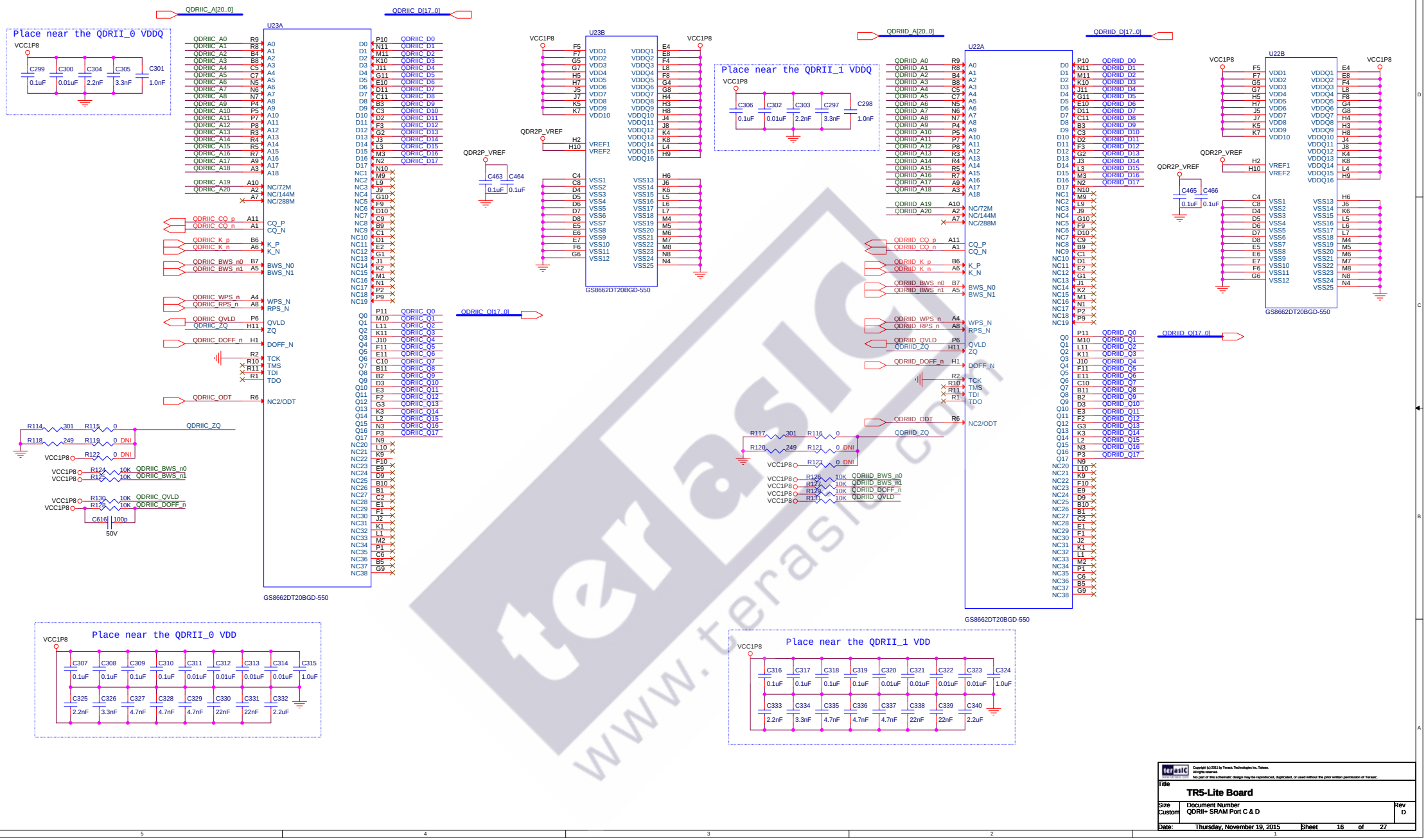
Place near the QDRII_0 VDDQ
Place near the QDRII_1 VDDQ
Place near the QDRII_0 VDD
Place near the QDRII_1 VDD
U23A
U23B
U22A
U22B
GS8662DT20BGD-550
QDRIIC_A[20..0]
QDRIIC_D[17..0]
QDRIIC_Q[17..0]
QDRIID_A[20..0]
QDRIID_D[17..0]
QDRIID_Q[17..0]
QDR2P_VREF
VCC1P8
QDRIIC_ZQ
QDRIID_ZQ
QDRIIC_BWS_n0
QDRIIC_BWS_n1
QDRIIC_QVLD
QDRIIC_DOFF_n
QDRIID_BWS_n0
QDRIID_BWS_n1
QDRIID_QVLD
QDRIID_DOFF_n
Title
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Size
Custom
Document Number
QDRII+ SRAM Port C & D
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D
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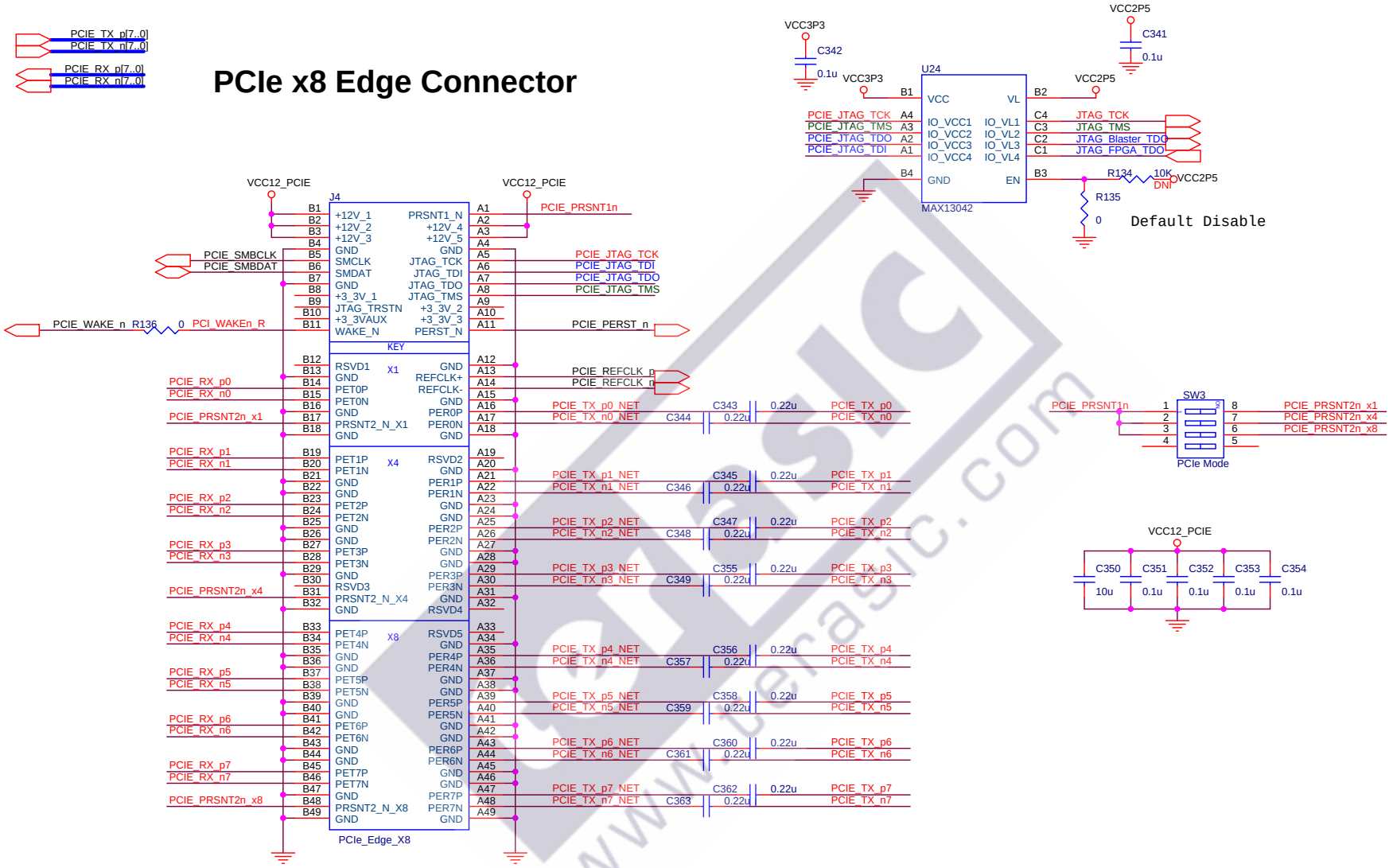
PCIE_TX_p[7..0]
PCIE_TX_n[7..0]
PCIE_RX_p[7..0]
PCIE_RX_n[7..0]
PCIe x8 Edge Connector
VCC3P3
C342
0.1u
VCC2P5
C341
0.1u
U24
MAX13042
VCC
VL
GND
EN
IO_VCC1
IO_VCC2
IO_VCC3
IO_VCC4
IO_VL1
IO_VL2
IO_VL3
IO_VL4
PCIE_JTAG_TCK
PCIE_JTAG_TMS
PCIE_JTAG_TDO
PCIE_JTAG_TDI
JTAG_TCK
JTAG_TMS
JTAG_Blaster_TDO
JTAG_FPGA_TDO
R134
10K
DNI
R135
0
Default Disable
VCC12_PCIE
J4
PCIE_SMBCLK
PCIE_SMBDAT
PCIE_WAKE_n
R136
0
PCI_WAKEn_R
PCIE_PRSNT1n
PCIE_JTAG_TCK
PCIE_JTAG_TDI
PCIE_JTAG_TDO
PCIE_JTAG_TMS
PCIE_PERST_n
PCIE_REFCLK_p
PCIE_REFCLK_n
KEY
X1
X4
X8
PCIe_Edge_X8
SW3
PCIe Mode
C350
C351
C352
C353
C354
10u
0.1u
0.22u
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Title
TR5-Lite Board
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PCI Express x 8
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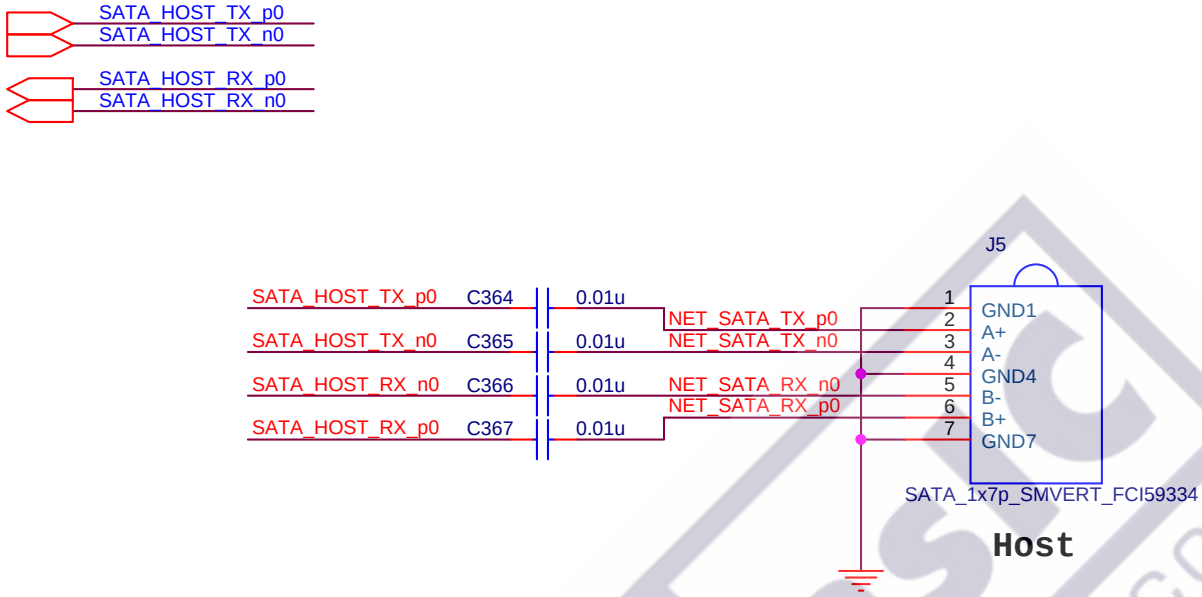

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Size: A	Document Number: SATA x1	Rev: D
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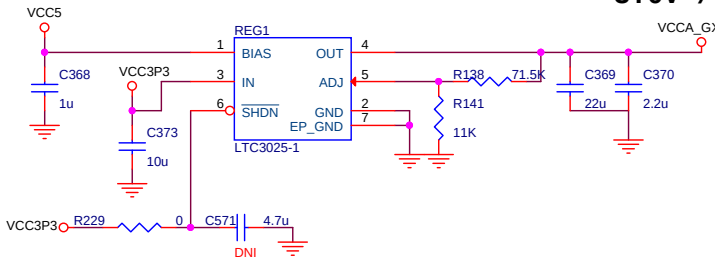
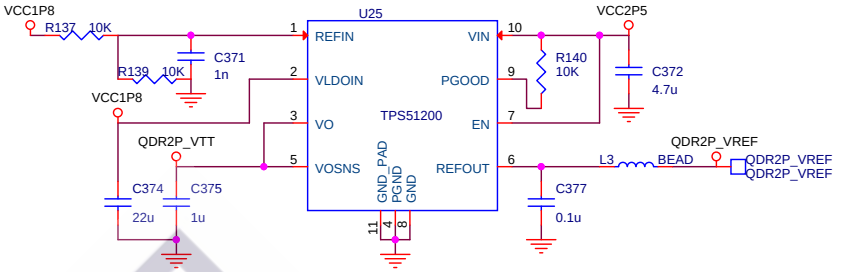
3.0V / 0.5A

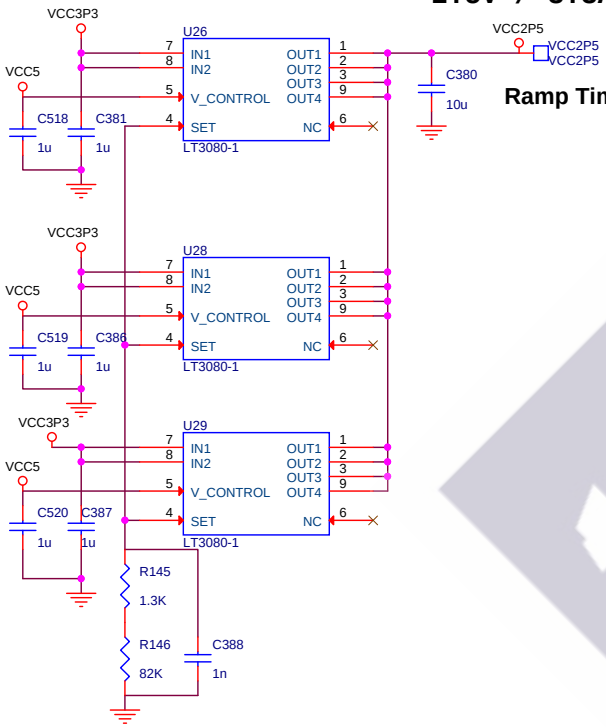


Ramp Time = 2 msec

QDRII+ VTT, VREF

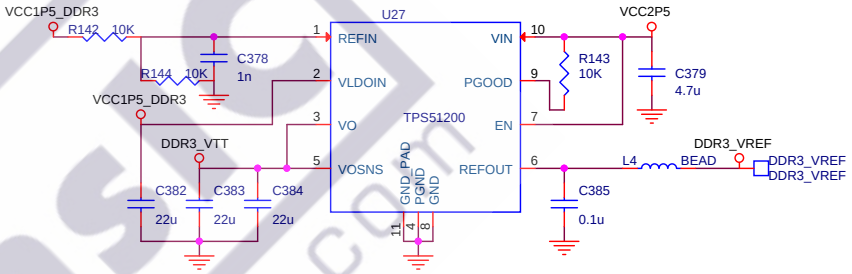


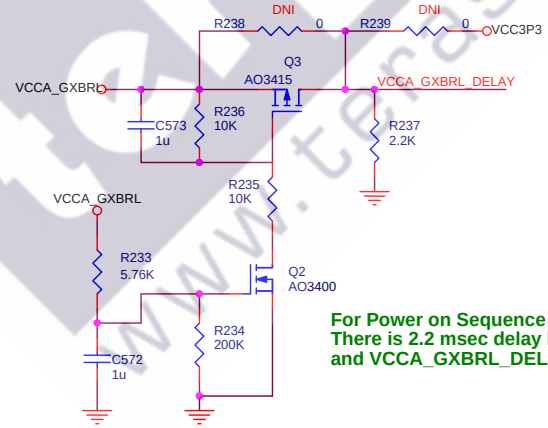
2.5V / 3.3A

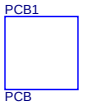


Ramp Time = 1.1 msec

DDR3 VTT, VREF







For Power on Sequence
There is 2.2 msec delay between VCCA_GXBRL and VCCA_GXBRL_DELAY

Title	TR5-Lite Board	
Size B	Document Number LDO 1	Rev D
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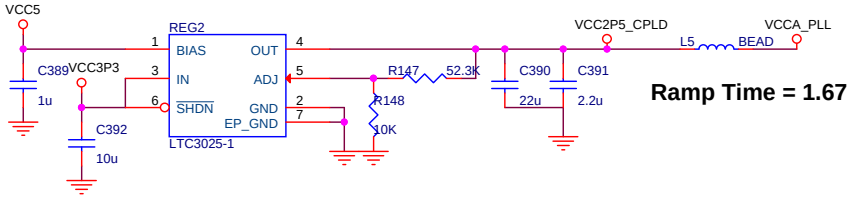
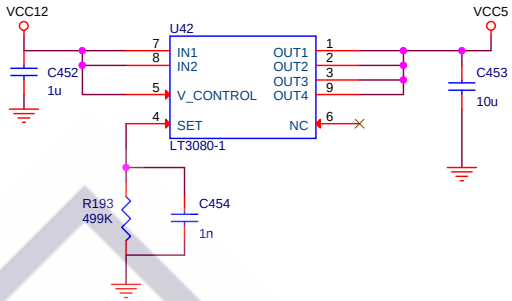
2.5V / 0.5A



Ramp Time = 1.67 msec

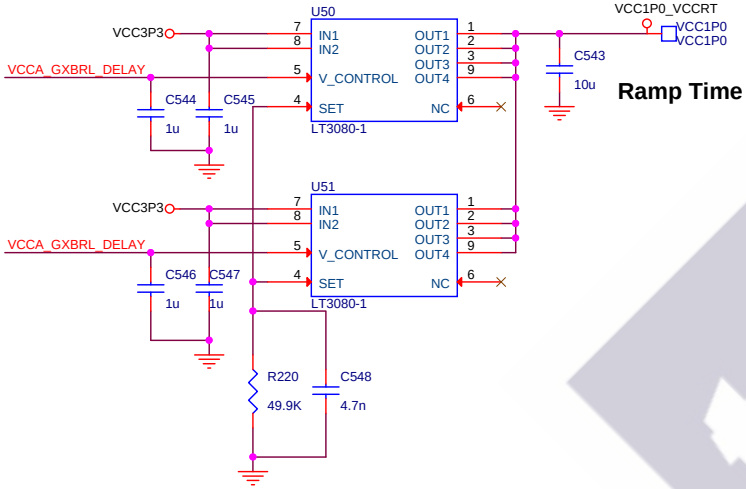
5.0V / 100mA



Ramp Time = 5 msec

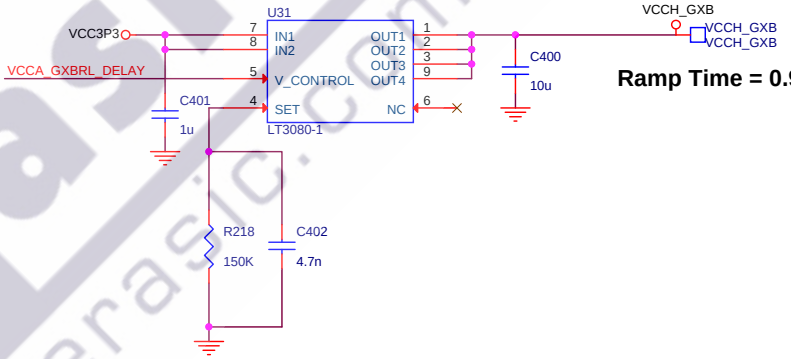
VCCA_GXBRL_DELAY

1.0V / 2.2A



Ramp Time = 2.4 msec

1.5V / 0.7A



Ramp Time = 0.96 msec

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Size B	Document Number LDO 2	Rev D
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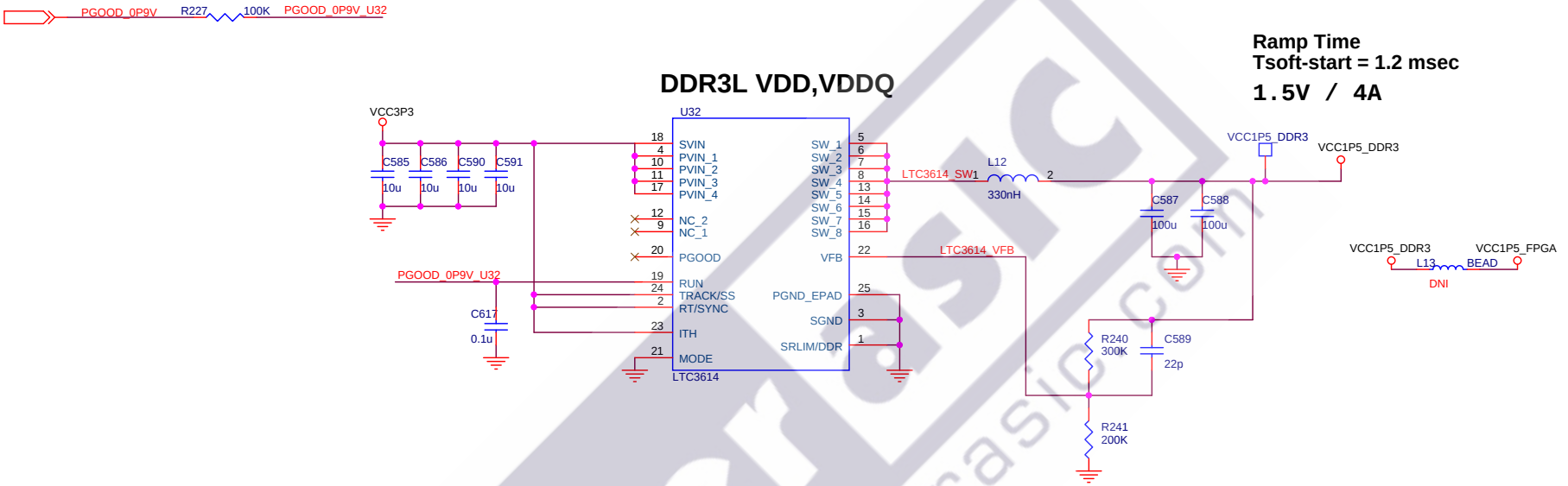

Title	TR5-Lite Board	
Size B	Document Number DDR3 VDD 1.5V	Rev D
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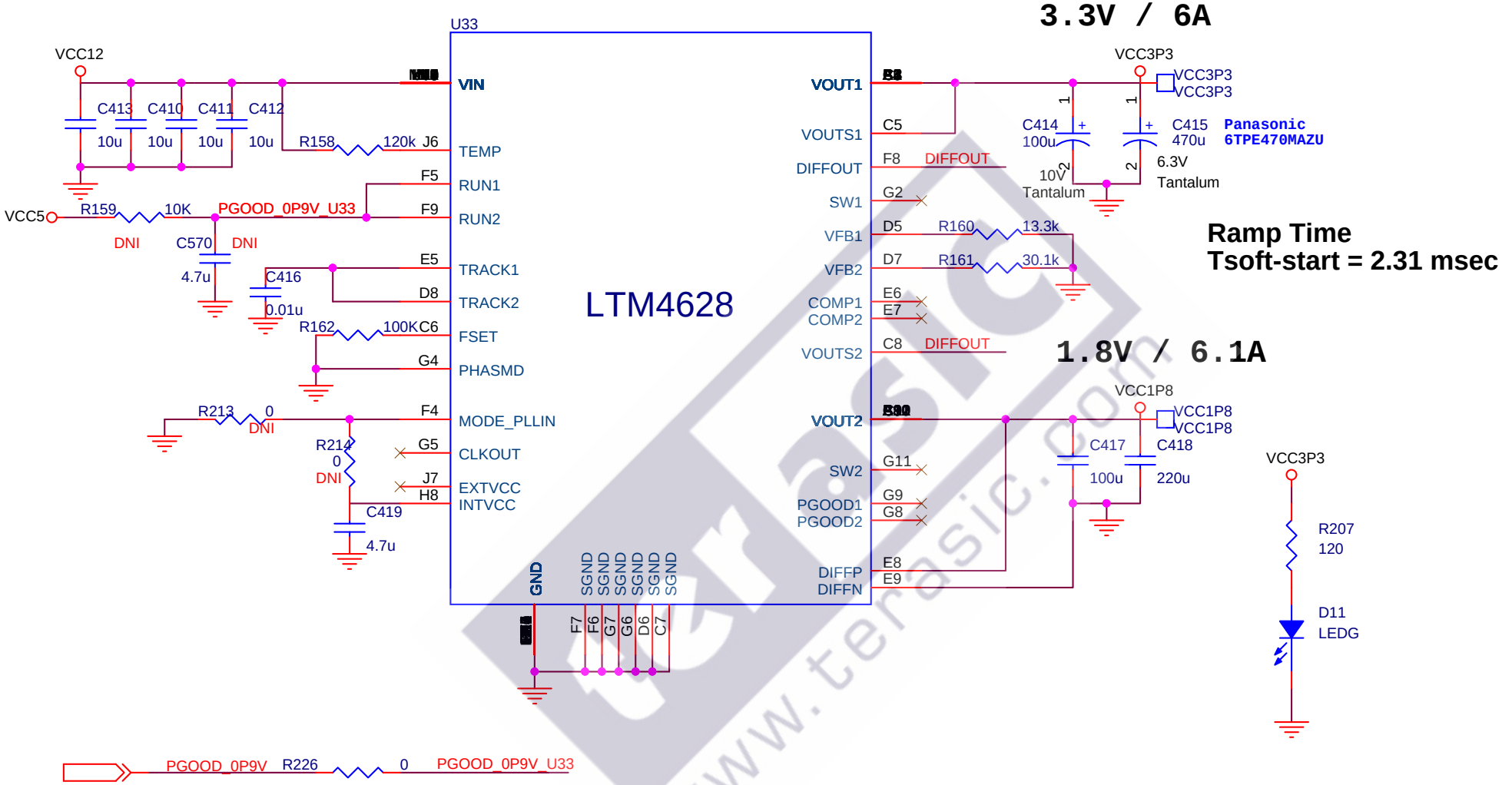

Title	TR5-Lite Board	
Size A	Document Number 3.3V & 1.8V	Rev D
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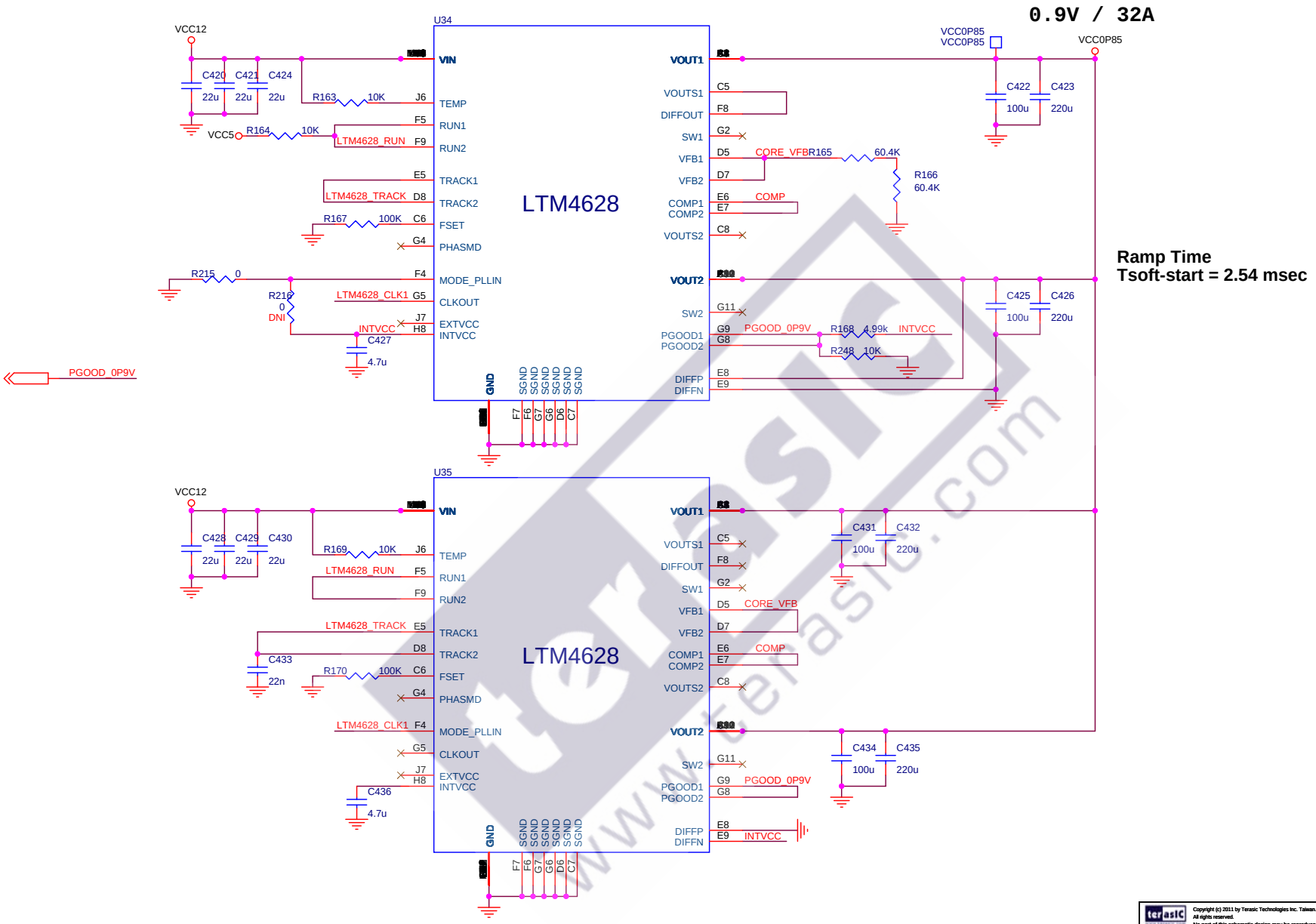

Title	TR5-Lite Board	
Size B	Document Number 0.85V VCCINT	Rev D
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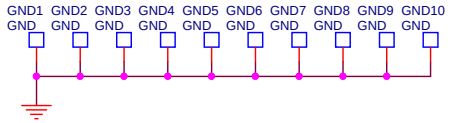

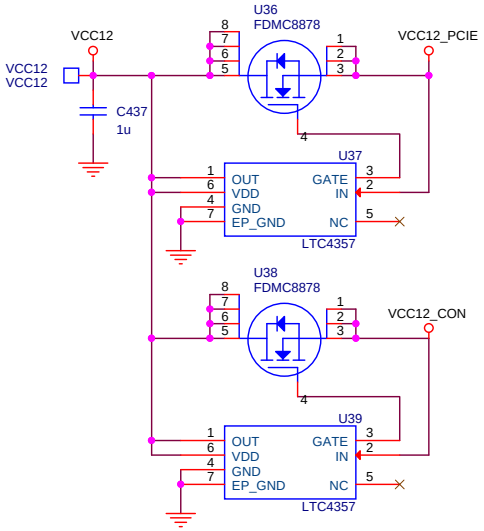

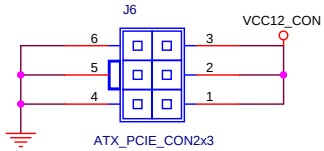

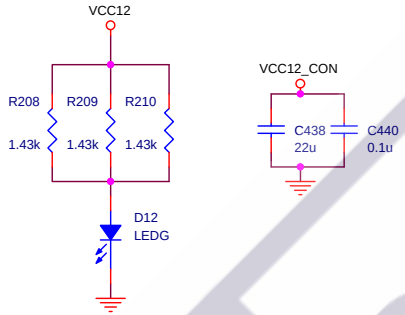

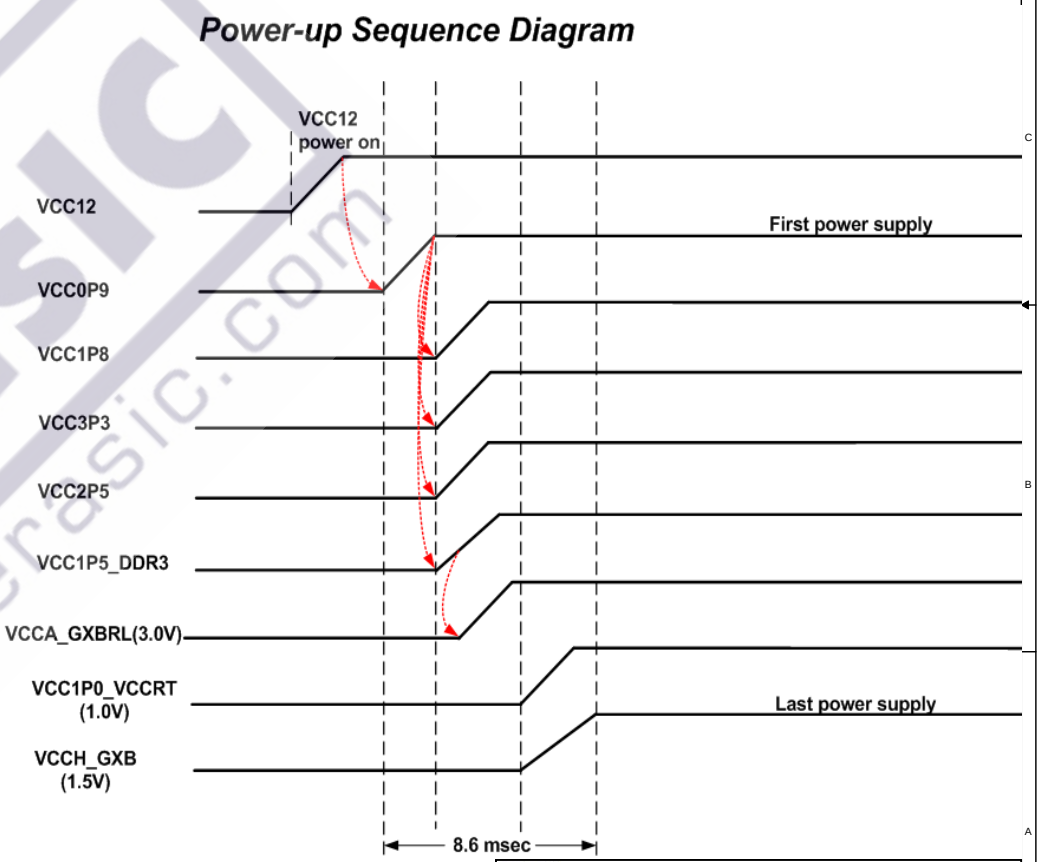

Title	TR5-Lite Board	
Size B	Document Number 12V Power Mux	Rev D
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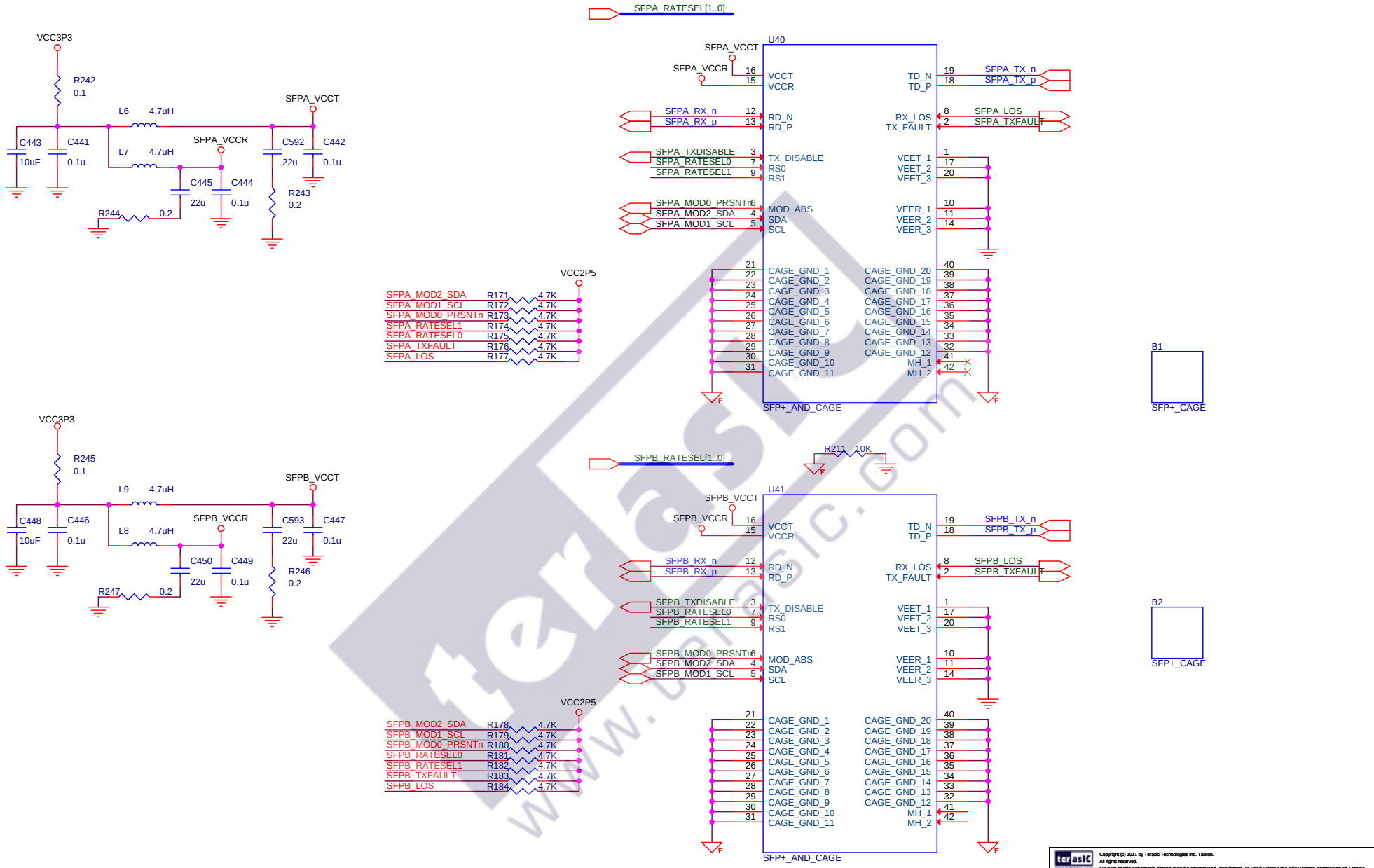

Title: **TR5-Lite Board**

Size	Document Number	Rev
B	SFP+ Interface	D

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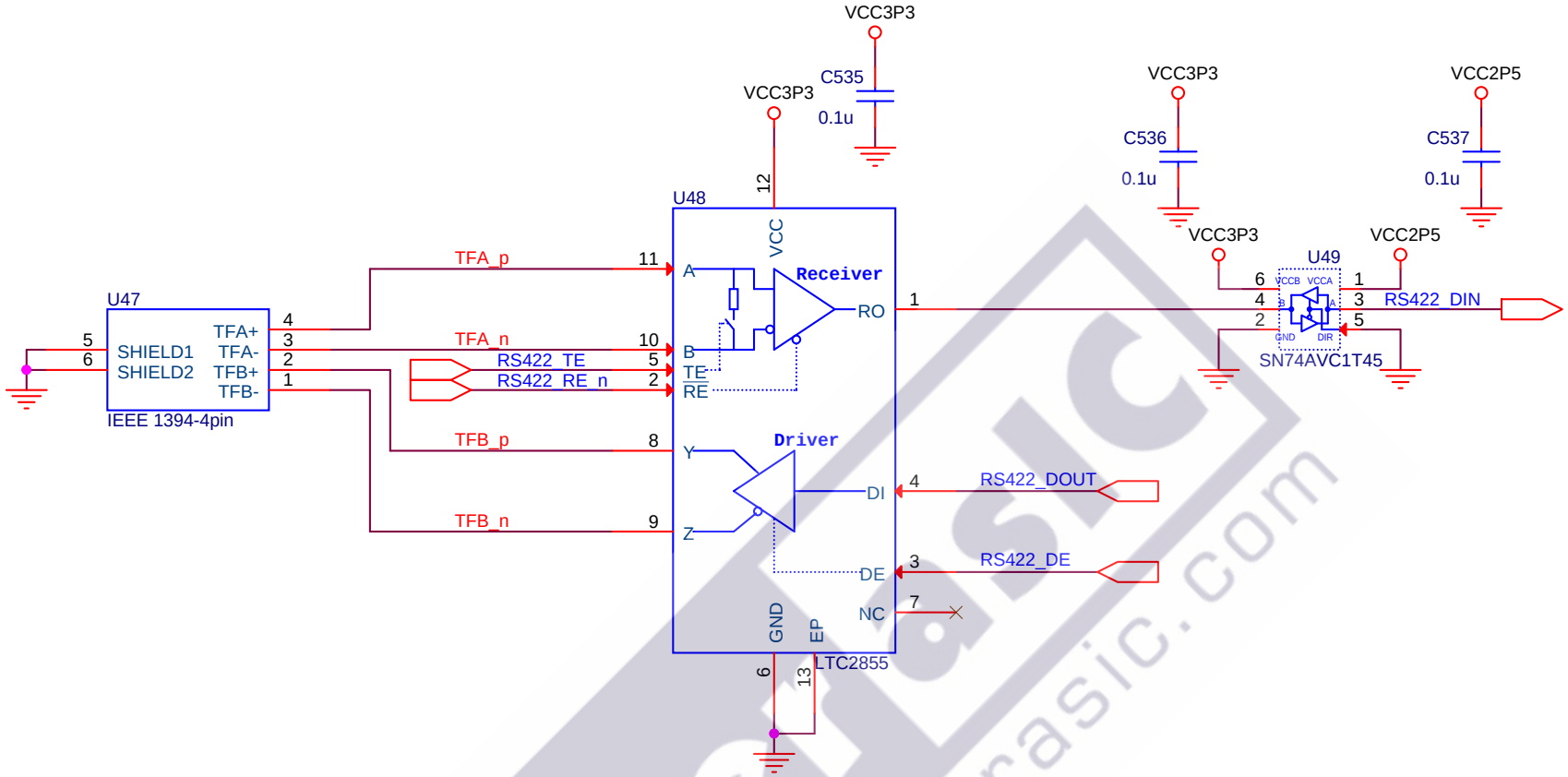

Title
TR5-Lite Board

Size	Document Number	Rev
A	RS422 Interface	D

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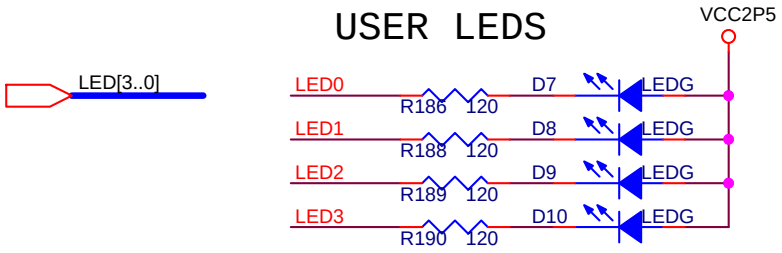
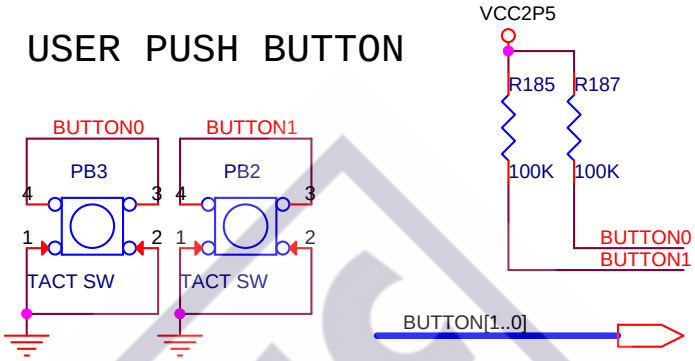
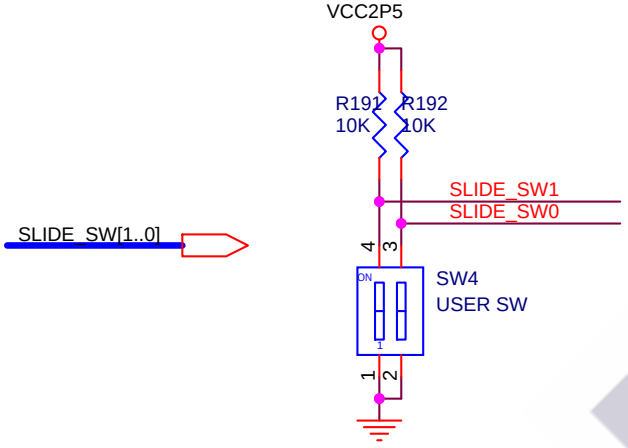
USER LEDS

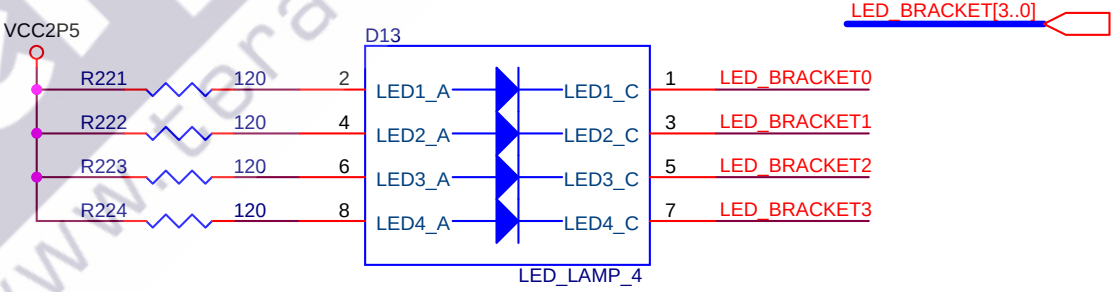


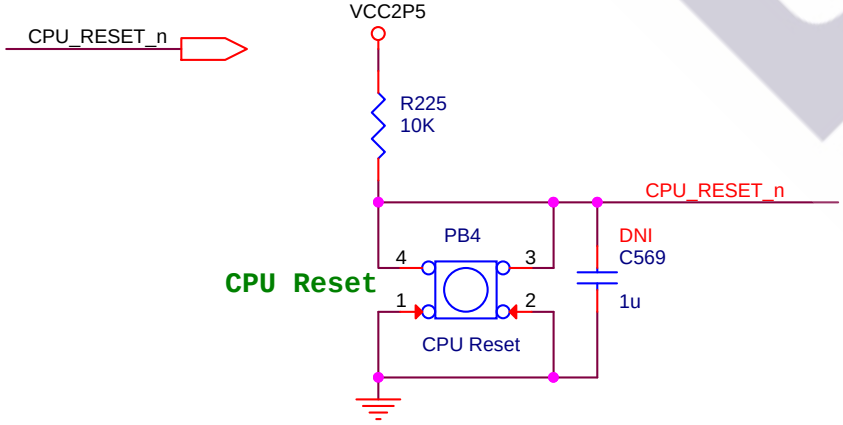
USER PUSH BUTTON





Housing LED Lamps with four LEDs





Title: **TR5-Lite Board**

Size	Document Number	Rev
A	Button & Switch & User LED	D

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