Cyclone V SoC System on module Board

Title: **Cyclone V - System on Module**

Size	Document Number	Rev
B	Cover Page	B0

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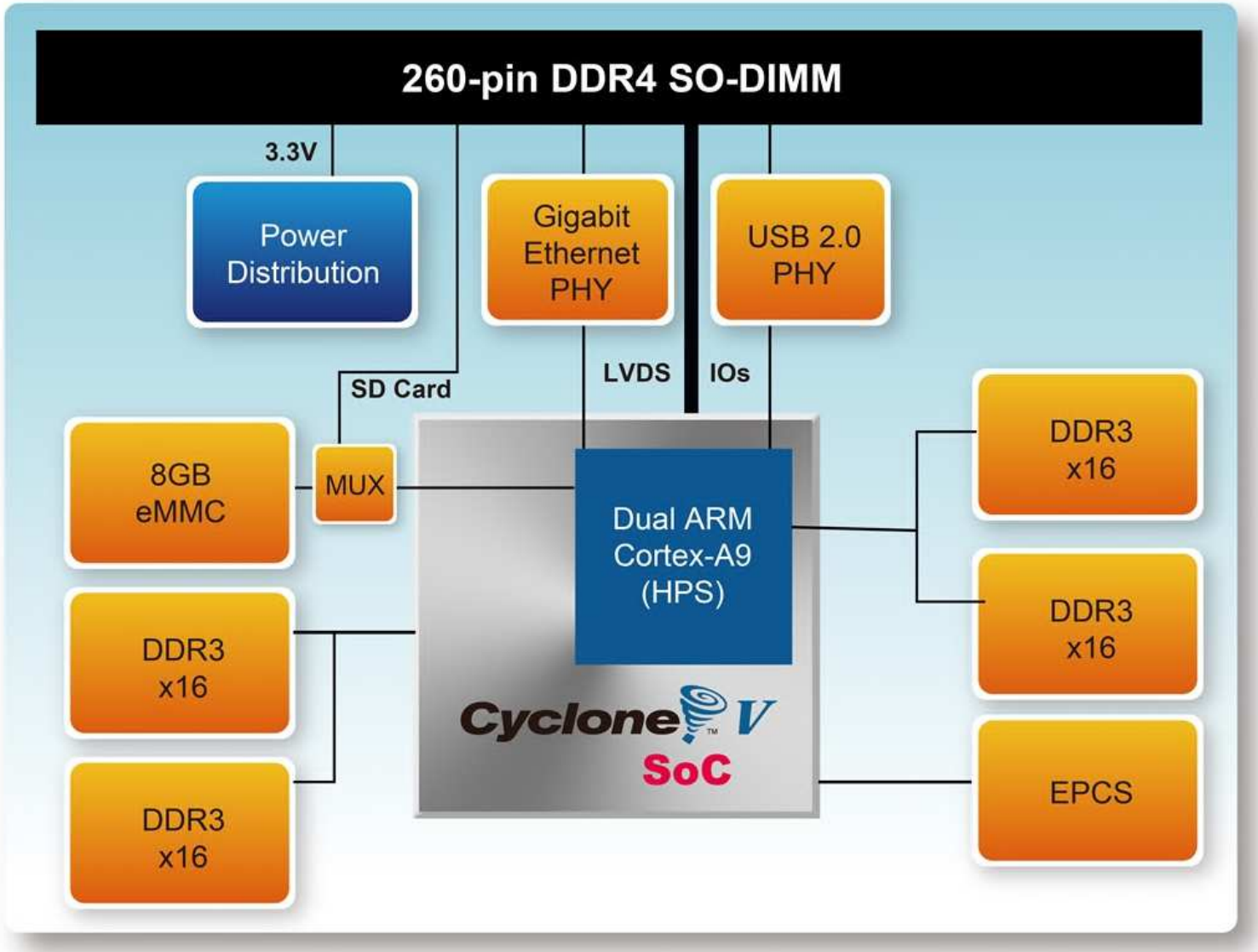

Title: **Cyclone V - System on Module**

Size	Document Number	Rev
B	Block Diagram	B0

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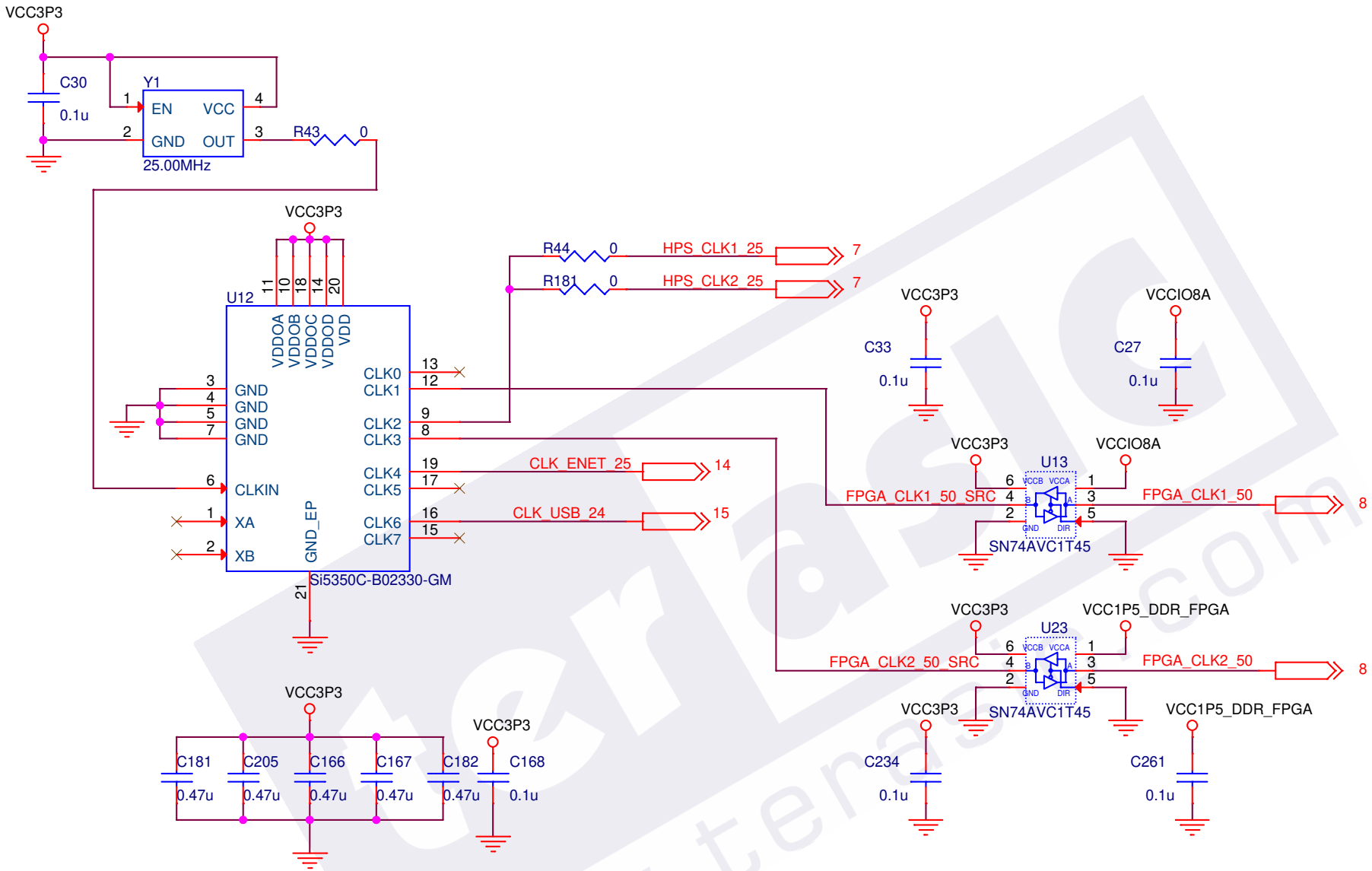

Title
Cyclone V - System on Module

Size	Document Number	Rev
A	Clock Generator	B0

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Blaster

16 JTAG_Blaster_TCK
16 JTAG_Blaster_TMS
16 JTAG_Blaster_TDO
16 JTAG_Blaster_TDI

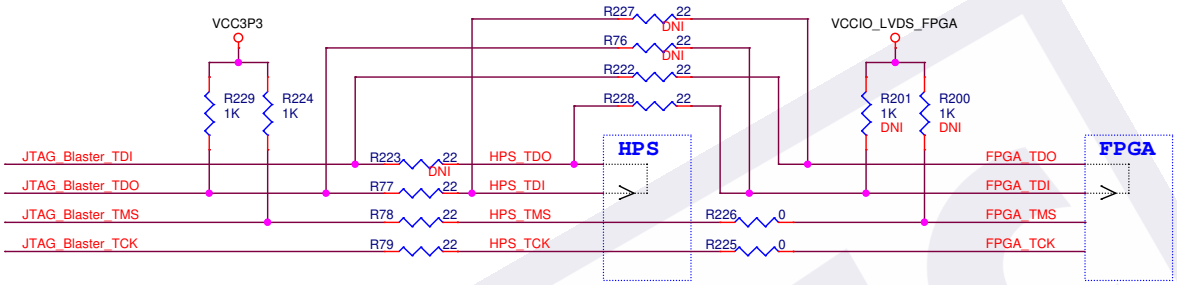
FPGA JTAG INTERFACE

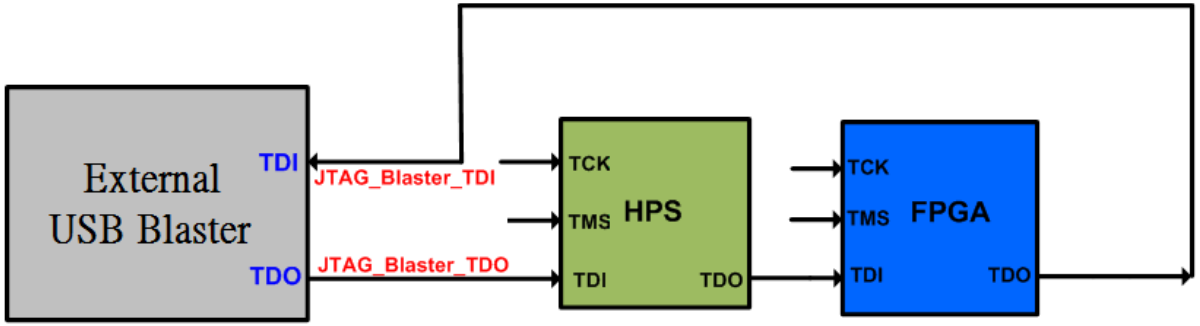
8 FPGA_TCK
8 FPGA_TMS
8 FPGA_TDI
8 FPGA_TDO

HPS JTAG INTERFACE

7 HPS_TCK
7 HPS_TMS
7 HPS_TDI
7 HPS_TDO

JTAG Chain





Title: Cyclone V - System on Module

Size	Document Number	Rev
B	SYSTEM : JTAG Chain	B0

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DDR3 Interface (HPS)

12 HPS_DDR3_ADDR[15..0]
12 HPS_DDR3_BA[2..0]
12 HPS_DDR3_DM[3..0]
12 HPS_DDR3_DQ[31..0]
12 HPS_DDR3_DQS_P[3..0]
12 HPS_DDR3_DQS_N[3..0]
12 HPS_DDR3_RESET_N
12 HPS_DDR3_CK_P
12 HPS_DDR3_CK_N
12 HPS_DDR3_CAS_N
12 HPS_DDR3_RAS_N
12 HPS_DDR3_CS_N0
12 HPS_DDR3_WE_N
12 HPS_DDR3_ODT0
12 HPS_DDR3_CKE0
12 HPS_DDR3_CS_N1
12 HPS_DDR3_CKE1
12 HPS_DDR3_ODT1

8,16 LVDS_TX_p[10..0]
8,16 LVDS_TX_n[10..0]
8,16 LVDS_RX_p[9..0]
8,16 LVDS_RX_n[9..0]

R149 100 HPS_DDR3_RZQ D25

U14L

CYCLONE V SoC BANK 6 (HPS)

Bank 6A

VCCIO = 1.5V

	HPS_RZQ_0	
HPS_DDR3_ADDR0	HPS_DDR/HPS_A_0	C28
HPS_DDR3_ADDR1	HPS_DDR/HPS_A_1	B28
HPS_DDR3_ADDR2	HPS_DDR/HPS_A_2	E26
HPS_DDR3_ADDR3	HPS_DDR/HPS_A_3	D26
HPS_DDR3_ADDR4	HPS_DDR/HPS_A_4	J21
HPS_DDR3_ADDR5	HPS_DDR/HPS_A_5	J20
HPS_DDR3_ADDR6	HPS_DDR/HPS_A_6	C26
HPS_DDR3_ADDR7	HPS_DDR/HPS_A_7	B26
HPS_DDR3_ADDR8	HPS_DDR/HPS_A_8	F26
HPS_DDR3_ADDR9	HPS_DDR/HPS_A_9	F25
HPS_DDR3_ADDR10	HPS_DDR/HPS_A_10	A24
HPS_DDR3_ADDR11	HPS_DDR/HPS_A_11	B24
HPS_DDR3_ADDR12	HPS_DDR/HPS_A_12	D24
HPS_DDR3_ADDR13	HPS_DDR/HPS_A_13	C24
HPS_DDR3_ADDR14	HPS_DDR/HPS_A_14	G23
HPS_DDR3_ADDR15	HPS_DDR/HPS_A_15	F24
HPS_DDR3_CK_P	HPS_DDR/HPS_CK	N21
HPS_DDR3_CK_N	HPS_DDR/HPS_CKn	N20
HPS_DDR3_CKE0	HPS_DDR/HPS_CKE_0	L28
HPS_DDR3_CKE1	HPS_DDR/HPS_CKE_1	K28
HPS_DDR3_BA0	HPS_DDR/HPS_BA_0	A27
HPS_DDR3_BA1	HPS_DDR/HPS_BA_1	H25
HPS_DDR3_BA2	HPS_DDR/HPS_BA_2	G25
HPS_DDR3_RAS_N	HPS_DDR/HPS_RASn	A25
HPS_DDR3_CAS_N	HPS_DDR/HPS_CASn	A26
HPS_DDR3_WE_N	HPS_DDR/HPS_WEn	E25
HPS_DDR3_CS_N0	HPS_DDR/HPS_CSn_0	L21
HPS_DDR3_CS_N1	HPS_DDR/HPS_CSn_1	L20
HPS_DDR3_ODT0	HPS_DDR/HPS_ODT_0	D28
HPS_DDR3_ODT1	HPS_DDR/HPS_ODT_1	G26

HPS_DDR/HPS_DQ_0	J25	HPS_DDR3_DQ0
HPS_DDR/HPS_DQ_1	J24	HPS_DDR3_DQ1
HPS_DDR/HPS_DQ_2	E28	HPS_DDR3_DQ2
HPS_DDR/HPS_DQ_3	D27	HPS_DDR3_DQ3
HPS_DDR/HPS_DQ_4	J26	HPS_DDR3_DQ4
HPS_DDR/HPS_DQ_5	K26	HPS_DDR3_DQ5
HPS_DDR/HPS_DQ_6	G27	HPS_DDR3_DQ6
HPS_DDR/HPS_DQ_7	F28	HPS_DDR3_DQ7
HPS_DDR/HPS_DQS_0	R17	HPS_DDR3_DQS_P0
HPS_DDR/HPS_DQSn_0	R16	HPS_DDR3_DQS_N0
HPS_DDR/HPS_DM_0	G28	HPS_DDR3_DM0
HPS_DDR/HPS_DQ_8	K25	HPS_DDR3_DQ8
HPS_DDR/HPS_DQ_9	L25	HPS_DDR3_DQ9
HPS_DDR/HPS_DQ_10	J27	HPS_DDR3_DQ10
HPS_DDR/HPS_DQ_11	J28	HPS_DDR3_DQ11
HPS_DDR/HPS_DQ_12	M27	HPS_DDR3_DQ12
HPS_DDR/HPS_DQ_13	M26	HPS_DDR3_DQ13
HPS_DDR/HPS_DQ_14	M28	HPS_DDR3_DQ14
HPS_DDR/HPS_DQ_15	N28	HPS_DDR3_DQ15
HPS_DDR/HPS_DQS_1	R19	HPS_DDR3_DQS_P1
HPS_DDR/HPS_DQSn_1	R18	HPS_DDR3_DQS_N1
HPS_DDR/HPS_DM_1	P28	HPS_DDR3_DM1
HPS_GPI10	U15	HPS_V1P5_GPI0 16
HPS_GPI11	U16	HPS_V1P5_GPI1 16
HPS_GPI12	AC27	HPS_V1P5_GPI2 16
HPS_GPI13	V24	HPS_V1P5_GPI3 16

Bank 6B

VCCIO = 1.5V

HPS_DDR3_DQ16	HPS_DDR/HPS_DQ_16	N24
HPS_DDR3_DQ17	HPS_DDR/HPS_DQ_17	N25
HPS_DDR3_DQ18	HPS_DDR/HPS_DQ_18	T28
HPS_DDR3_DQ19	HPS_DDR/HPS_DQ_19	U28
HPS_DDR3_DQ20	HPS_DDR/HPS_DQ_20	N26
HPS_DDR3_DQ21	HPS_DDR/HPS_DQ_21	N27
HPS_DDR3_DQ22	HPS_DDR/HPS_DQ_22	R27
HPS_DDR3_DQ23	HPS_DDR/HPS_DQ_23	V27
HPS_DDR3_DQS_P2	HPS_DDR/HPS_DQS_2	T19
HPS_DDR3_DQS_N2	HPS_DDR/HPS_DQSn_2	T18
HPS_DDR3_DM2	HPS_DDR/HPS_DM_2	W28
HPS_DDR3_DQ24	HPS_DDR/HPS_DQ_24	R26
HPS_DDR3_DQ25	HPS_DDR/HPS_DQ_25	R25
HPS_DDR3_DQ26	HPS_DDR/HPS_DQ_26	AA28
HPS_DDR3_DQ27	HPS_DDR/HPS_DQ_27	W26
HPS_DDR3_DQ28	HPS_DDR/HPS_DQ_28	R24
HPS_DDR3_DQ29	HPS_DDR/HPS_DQ_29	T24
HPS_DDR3_DQ30	HPS_DDR/HPS_DQ_30	Y27
HPS_DDR3_DQ31	HPS_DDR/HPS_DQ_31	AA27
HPS_DDR3_DQS_P3	HPS_DDR/HPS_DQS_3	U19
HPS_DDR3_DQS_N3	HPS_DDR/HPS_DQSn_3	T20
HPS_DDR3_DM3	HPS_DDR/HPS_DM_3	AB28

HPS_DDR/HPS_DQ_32	T26	
HPS_DDR/HPS_DQ_33	U25	
HPS_DDR/HPS_DQ_34	AC28	
HPS_DDR/HPS_DQ_35	V25	
HPS_DDR/HPS_DQ_36	V19	
HPS_DDR/HPS_DQ_37	V20	
HPS_DDR/HPS_DQ_38	AE27	
HPS_DDR/HPS_DQ_39	AD28	
HPS_DDR/HPS_DQS_4	V18	
HPS_DDR/HPS_DQSn_4	V17	
HPS_DDR/HPS_DM_4	AE28	
HPS_GPI0	M25	
HPS_GPI1	K27	
HPS_GPI2	R20	
HPS_GPI3	R21	
HPS_GPI4	R28	
HPS_GPI5	P26	
HPS_GPI6	T17	
HPS_GPI7	T16	
HPS_GPI8	Y28	
HPS_GPI9	Y26	
HPS_DDR/HPS_RESETn	V28	HPS_DDR3_RESET_N

5CSEBA6U23I7

U14I

CYCLONE V SoC BANK 3

Bank 3A VCCIO = 1.8V/2.5V

LVDS_RX_p4	Y11	IO_3A/PR_ERROR/DIFFIO_RX_B7P
LVDS_RX_n4	AA11	IO_3A/PR_DONE/DIFFIO_RX_B7N
LVDS_TX_p4	AD5	IO_3A/DIFFIO_TX_B8P/DQ1B
LVDS_TX_n4	AE6	IO_3A/PR_READY/DIFFIO_TX_B8N/DQ1B

Bank 3B VCCIO = 1.8V/2.5V

LVDS_TX_p9	AE4	IO_3B/DIFFIO_TX_B9P/B_WEN/DQ2B	IO_3B/DIFFIO_TX_B17P/B_BA_0/DQ3B	AF7	LVDS_TX_p1
LVDS_TX_n9	AF4	IO_3B/DIFFIO_TX_B9N/GND	IO_3B/DIFFIO_TX_B17N/GND	AG6	LVDS_TX_n1
LVDS_RX_p0	AD10	IO_3B/DIFFIO_RX_B10P/B_A_14/DQ2B	IO_3B/DIFFIO_RX_B18P/B_BA_1/DQ3B	AF11	LVDS_RX_p2
LVDS_RX_n0	AE9	IO_3B/DIFFIO_RX_B10N/B_A_15/DQ2B	IO_3B/DIFFIO_RX_B18N/B_BA_2/DQ3B	AF10	LVDS_RX_n2
LVDS_RX_p8	T11	IO_3B/DIFFIO_RX_B11P/B_CSN_0/DQS2B	IO_3B/DIFFIO_RX_B19P/B_CK/DQS3B	T13	LVDS_RX_p9
LVDS_RX_n8	U11	IO_3B/DIFFIO_RX_B11N/B_CSN_1/DQSN2B	IO_3B/DIFFIO_RX_B19N/B_CKN/DQSN3B	T12	LVDS_RX_n9
LVDS_TX_p8	AE7	IO_3B/DIFFIO_TX_B12P/B_A_12	IO_3B/DIFFIO_TX_B20P/B_A_6	AH3	LVDS_TX_p10
LVDS_TX_n8	AF8	IO_3B/DIFFIO_TX_B12N/B_A_13/DQ2B	IO_3B/DIFFIO_TX_B20N/B_A_7/DQ3B	AH2	LVDS_TX_n10
LVDS_TX_p0	AE8	IO_3B/DIFFIO_TX_B13P/B_A_10/DQ2B			
LVDS_TX_n0	AF9	IO_3B/DIFFIO_TX_B13N/B_A_11/DQ2B			
LVDS_RX_p3	AD11	IO_3B/DIFFIO_RX_B14P/B_A_8/DQ2B	IO_3B/DIFFIO_RX_B22P/B_A_4/DQ3B	AE12	LVDS_RX_p1
LVDS_RX_n3	AE11	IO_3B/DIFFIO_RX_B14N/B_A_9/DQ2B	IO_3B/DIFFIO_RX_B22N/B_A_5/DQ3B	AD12	LVDS_RX_n1
LVDS_TX_p3	AF5	IO_3B/DIFFIO_TX_B16P/B_CASN/DQ2B	IO_3B/DIFFIO_TX_B24P/B_A_0/DQ3B	AH6	LVDS_TX_p2
LVDS_TX_n3	AF6	IO_3B/DIFFIO_TX_B16N/B_RASN/DQ2B	IO_3B/DIFFIO_TX_B24N/B_A_1/DQ3B	AH5	LVDS_TX_n2

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Title: Cyclone V - System on Module

Size	Document Number	Rev
B	FPGA : Bank 3 and 6	B0

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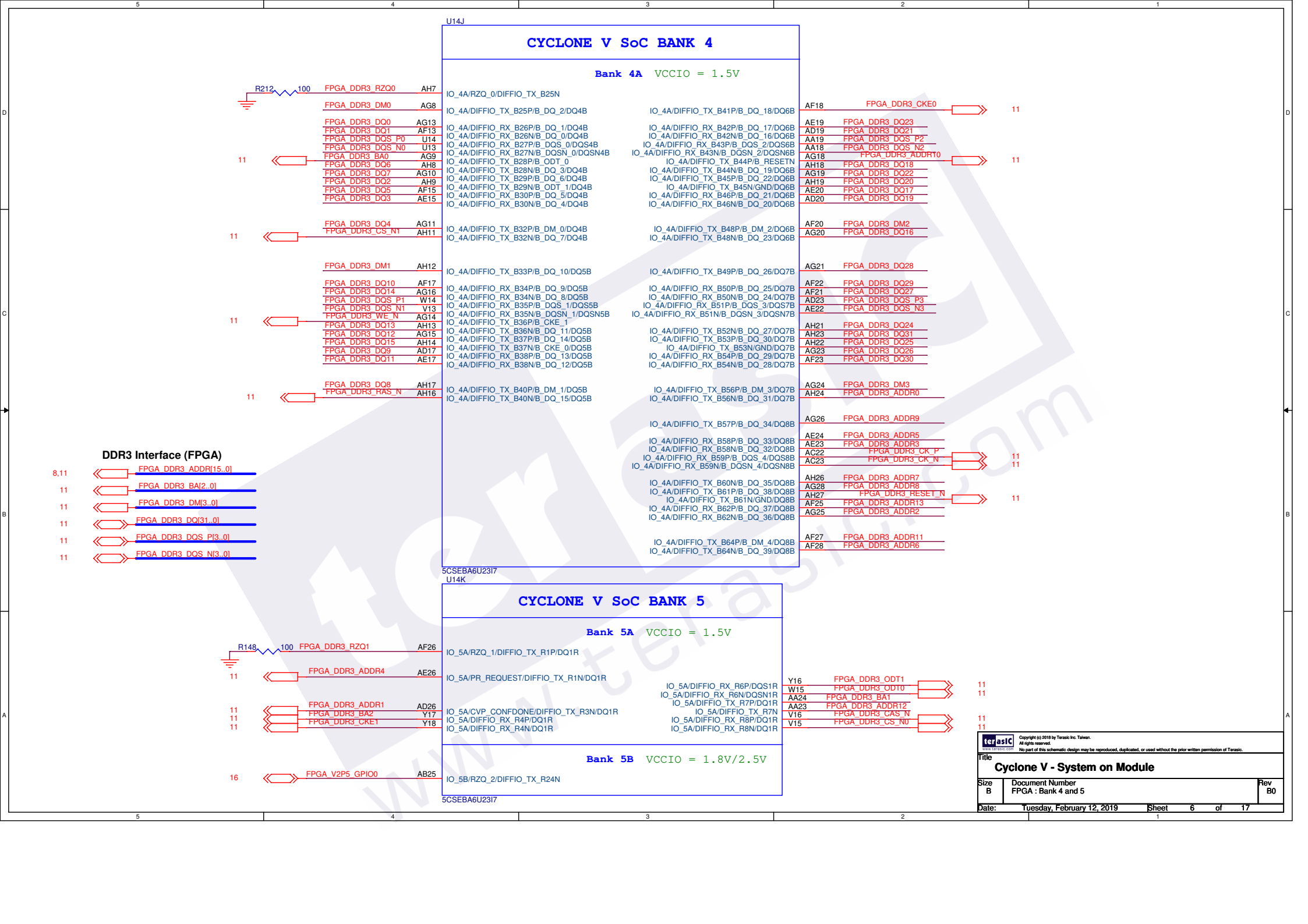
U14J
CYCLONE V SoC BANK 4
Bank 4A VCCIO = 1.5V
R212 100 FPGA_DDR3_RZQ0 AH7 IO_4A/RZQ_0/DIFFIO_TX_B25N
FPGA_DDR3_DM0 AG8 IO_4A/DIFFIO_TX_B25P/B_DQ_2/DQ4B
FPGA_DDR3_DQ0 AG13 IO_4A/DIFFIO_RX_B26P/B_DQ_1/DQ4B
FPGA_DDR3_DQ1 AF13 IO_4A/DIFFIO_RX_B26N/B_DQ_0/DQ4B
FPGA_DDR3_DQS_P0 U14 IO_4A/DIFFIO_RX_B27P/B_DQS_0/DQS4B
FPGA_DDR3_DQS_N0 U13 IO_4A/DIFFIO_RX_B27N/B_DQSN_0/DQSN4B
11 FPGA_DDR3_BA0 AG9 IO_4A/DIFFIO_TX_B28P/B_ODT_0
FPGA_DDR3_DQ6 AH8 IO_4A/DIFFIO_TX_B28N/B_DQ_3/DQ4B
FPGA_DDR3_DQ7 AG10 IO_4A/DIFFIO_TX_B29P/B_DQ_6/DQ4B
FPGA_DDR3_DQ2 AH9 IO_4A/DIFFIO_TX_B29N/B_ODT_1/DQ4B
FPGA_DDR3_DQ5 AF15 IO_4A/DIFFIO_RX_B30P/B_DQ_5/DQ4B
FPGA_DDR3_DQ3 AE15 IO_4A/DIFFIO_RX_B30N/B_DQ_4/DQ4B
FPGA_DDR3_DQ4 AG11 IO_4A/DIFFIO_TX_B32P/B_DM_0/DQ4B
11 FPGA_DDR3_CS_N1 AH11 IO_4A/DIFFIO_TX_B32N/B_DQ_7/DQ4B
FPGA_DDR3_DM1 AH12 IO_4A/DIFFIO_TX_B33P/B_DQ_10/DQ5B
FPGA_DDR3_DQ10 AF17 IO_4A/DIFFIO_RX_B34P/B_DQ_9/DQ5B
FPGA_DDR3_DQ14 AG16 IO_4A/DIFFIO_RX_B34N/B_DQ_8/DQ5B
FPGA_DDR3_DQS_P1 W14 IO_4A/DIFFIO_RX_B35P/B_DQS_1/DQS5B
FPGA_DDR3_DQS_N1 V13 IO_4A/DIFFIO_RX_B35N/B_DQSN_1/DQSN5B
11 FPGA_DDR3_WE_N AG14 IO_4A/DIFFIO_TX_B36P/B_CKE_1
FPGA_DDR3_DQ13 AH13 IO_4A/DIFFIO_TX_B36N/B_DQ_11/DQ5B
FPGA_DDR3_DQ12 AG15 IO_4A/DIFFIO_TX_B37P/B_DQ_14/DQ5B
FPGA_DDR3_DQ15 AH14 IO_4A/DIFFIO_TX_B37N/B_CKE_0/DQ5B
FPGA_DDR3_DQ9 AD17 IO_4A/DIFFIO_RX_B38P/B_DQ_13/DQ5B
FPGA_DDR3_DQ11 AE17 IO_4A/DIFFIO_RX_B38N/B_DQ_12/DQ5B
FPGA_DDR3_DQ8 AH17 IO_4A/DIFFIO_TX_B40P/B_DM_1/DQ5B
11 FPGA_DDR3_RAS_N AH16 IO_4A/DIFFIO_TX_B40N/B_DQ_15/DQ5B
IO_4A/DIFFIO_TX_B41P/B_DQ_18/DQ6B AF18 FPGA_DDR3_CKE0 11
AE19 FPGA_DDR3_DQ23
AD19 FPGA_DDR3_DQ21
AA19 FPGA_DDR3_DQS_P2
AA18 FPGA_DDR3_DQS_N2
IO_4A/DIFFIO_RX_B42P/B_DQ_17/DQ6B
IO_4A/DIFFIO_RX_B42N/B_DQ_16/DQ6B
IO_4A/DIFFIO_RX_B43P/B_DQS_2/DQS6B
IO_4A/DIFFIO_RX_B43N/B_DQSN_2/DQSN6B
AG18 FPGA_DDR3_ADDR10 11
IO_4A/DIFFIO_TX_B44P/B_RESETN
AH18 FPGA_DDR3_DQ18
IO_4A/DIFFIO_TX_B44N/B_DQ_19/DQ6B
AG19 FPGA_DDR3_DQ22
IO_4A/DIFFIO_TX_B45P/B_DQ_22/DQ6B
AH19 FPGA_DDR3_DQ20
IO_4A/DIFFIO_TX_B45N/GND/DQ6B
AE20 FPGA_DDR3_DQ17
IO_4A/DIFFIO_RX_B46P/B_DQ_21/DQ6B
AD20 FPGA_DDR3_DQ19
IO_4A/DIFFIO_RX_B46N/B_DQ_20/DQ6B
IO_4A/DIFFIO_TX_B48P/B_DM_2/DQ6B AF20 FPGA_DDR3_DM2
IO_4A/DIFFIO_TX_B48N/B_DQ_23/DQ6B AG20 FPGA_DDR3_DQ16
IO_4A/DIFFIO_TX_B49P/B_DQ_26/DQ7B AG21 FPGA_DDR3_DQ28
IO_4A/DIFFIO_RX_B50P/B_DQ_25/DQ7B AF22 FPGA_DDR3_DQ29
IO_4A/DIFFIO_RX_B50N/B_DQ_24/DQ7B AF21 FPGA_DDR3_DQ27
IO_4A/DIFFIO_RX_B51P/B_DQS_3/DQS7B AD23 FPGA_DDR3_DQS_P3
IO_4A/DIFFIO_RX_B51N/B_DQSN_3/DQSN7B AE22 FPGA_DDR3_DQS_N3
AH21 FPGA_DDR3_DQ24
IO_4A/DIFFIO_TX_B52N/B_DQ_27/DQ7B AH23 FPGA_DDR3_DQ31
IO_4A/DIFFIO_TX_B53P/B_DQ_30/DQ7B AH22 FPGA_DDR3_DQ25
IO_4A/DIFFIO_TX_B53N/GND/DQ7B AG23 FPGA_DDR3_DQ26
IO_4A/DIFFIO_RX_B54P/B_DQ_29/DQ7B AF23 FPGA_DDR3_DQ30
IO_4A/DIFFIO_RX_B54N/B_DQ_28/DQ7B
IO_4A/DIFFIO_TX_B56P/B_DM_3/DQ7B AG24 FPGA_DDR3_DM3
IO_4A/DIFFIO_TX_B56N/B_DQ_31/DQ7B AH24 FPGA_DDR3_ADDR0
IO_4A/DIFFIO_TX_B57P/B_DQ_34/DQ8B AG26 FPGA_DDR3_ADDR9
IO_4A/DIFFIO_RX_B58P/B_DQ_33/DQ8B AE24 FPGA_DDR3_ADDR5
IO_4A/DIFFIO_RX_B58N/B_DQ_32/DQ8B AE23 FPGA_DDR3_ADDR3
IO_4A/DIFFIO_RX_B59P/B_DQS_4/DQS8B AC22 FPGA_DDR3_CK_P 11
IO_4A/DIFFIO_RX_B59N/B_DQSN_4/DQSN8B AC23 FPGA_DDR3_CK_N 11
IO_4A/DIFFIO_TX_B60N/B_DQ_35/DQ8B AH26 FPGA_DDR3_ADDR7
IO_4A/DIFFIO_TX_B61P/B_DQ_38/DQ8B AG28 FPGA_DDR3_ADDR8
IO_4A/DIFFIO_TX_B61N/GND/DQ8B AH27 FPGA_DDR3_RESET_N 11
IO_4A/DIFFIO_RX_B62P/B_DQ_37/DQ8B AF25 FPGA_DDR3_ADDR13
IO_4A/DIFFIO_RX_B62N/B_DQ_36/DQ8B AG25 FPGA_DDR3_ADDR2
IO_4A/DIFFIO_TX_B64P/B_DM_4/DQ8B AF27 FPGA_DDR3_ADDR11
IO_4A/DIFFIO_TX_B64N/B_DQ_39/DQ8B AF28 FPGA_DDR3_ADDR6
5CSEBA6U23I7
U14K
CYCLONE V SoC BANK 5
Bank 5A VCCIO = 1.5V
R148 100 FPGA_DDR3_RZQ1 AF26 IO_5A/RZQ_1/DIFFIO_TX_R1P/DQ1R
11 FPGA_DDR3_ADDR4 AE26 IO_5A/PR_REQUEST/DIFFIO_TX_R1N/DQ1R
11 FPGA_DDR3_ADDR1 AD26
11 FPGA_DDR3_BA2 Y17 IO_5A/CVP_CONFDONE/DIFFIO_TX_R3N/DQ1R
11 FPGA_DDR3_CKE1 Y18 IO_5A/DIFFIO_RX_R4P/DQ1R
IO_5A/DIFFIO_RX_R4N/DQ1R
IO_5A/DIFFIO_RX_R6P/DQS1R Y16 FPGA_DDR3_ODT1 11
IO_5A/DIFFIO_RX_R6N/DQSN1R W15 FPGA_DDR3_ODT0 11
IO_5A/DIFFIO_TX_R7P/DQ1R AA24 FPGA_DDR3_BA1
IO_5A/DIFFIO_TX_R7N AA23 FPGA_DDR3_ADDR12
IO_5A/DIFFIO_RX_R8P/DQ1R V16 FPGA_DDR3_CAS_N 11
IO_5A/DIFFIO_RX_R8N/DQ1R V15 FPGA_DDR3_CS_N0 11
Bank 5B VCCIO = 1.8V/2.5V
16 FPGA_V2P5_GPIO0 AB25 IO_5B/RZQ_2/DIFFIO_TX_R24N
5CSEBA6U23I7
DDR3 Interface (FPGA)
8,11 FPGA_DDR3_ADDR[15..0]
11 FPGA_DDR3_BA[2..0]
11 FPGA_DDR3_DM[3..0]
11 FPGA_DDR3_DQ[31..0]
11 FPGA_DDR3_DQS_P[3..0]
11 FPGA_DDR3_DQS_N[3..0]
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Title
Cyclone V - System on Module
Size B
Document Number
FPGA : Bank 4 and 5
Rev B0
Date: Tuesday, February 12, 2019
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U14M

CYCLONE V SoC BANK 7 (HPS)

Bank 7A VCCIO = 3.3V

15,16	HPS_nRST	A23	HPS_NRST		
15,16	HPS_nPOR	H19	HPS_NPOR		
3,7	HPS_CLK1_25	E20	HPS_CLK1		
3	HPS_CLK2_25	D20	HPS_CLK2		
VCC3P3					
R180 4.7K	HPS_PORSEL	E18	HPS_PORSEL		
R152 4.7K	JTAG_TRST	C22	HPS_TRST		
R178 0 DNI	HPS_TCK	K19	HPS_TCK		
	HPS_TMS	C23	HPS_TMS		
C232 33p 50V DNI	HPS_TDI	D22	HPS_TDI		
	HPS_TDO	B23	HPS_TDO		

TRACE_CLK/ - / - /HPS_GPIO48 — C21 HPS_V3P3_GPIO0 — 16
TRACE_D0/SPIS0_CLK/UART0_RX/HPS_GPIO49 — A22 HPS_V3P3_GPIO1 — 16
TRACE_D1/SPIS0_MOSI/UART0_TX/HPS_GPIO50 — B21 HPS_V3P3_GPIO2 — 16
TRACE_D2/SPIS0_MISO/I2C1_SDA/HPS_GPIO51 — A21 HPS_V3P3_GPIO3 — 16
TRACE_D3/SPIS0_SS0/I2C1_SCL/HPS_GPIO52 — K18 HPS_V3P3_GPIO4 — 16
TRACE_D4/SPIS1_CLK/CAN1_RX/HPS_GPIO53 — A20 HPS_V3P3_GPIO5 — 16
TRACE_D5/SPIS1_MOSI/CAN1_TX/HPS_GPIO54 — J18 HPS_V3P3_GPIO6 — 16
TRACE_D6/SPIS1_SS0/I2C0_SDA/HPS_GPIO55 — A19 HPS_V3P3_GPIO7 — 16
TRACE_D7/SPIS1_MISO/I2C0_SCL/HPS_GPIO56 — C18 HPS_V3P3_GPIO8 — 16

SPIM0_CLK/I2C1_SDA/UART0_CTS/HPS_GPIO57 — A18 HPS_V3P3_GPIO9 — 16
SPIM0_MOSI/I2C1_SCL/UART0_RTS/HPS_GPIO58 — C17 HPS_V3P3_GPIO10 — 16
SPIM0_MISO/CAN1_RX/UART1_CTS/HPS_GPIO59 — B18 HPS_V3P3_GPIO11 — 16
SPIM0_SS0,BOOTSEL0/CAN1_TX/UART1_RTS/HPS_GPIO60 — J17 HPS_V3P3_GPIO12 — 16
UART0_RX/CAN0_RX/SPIM0_SS1/HPS_GPIO61 — A17 HPS_V3P3_GPIO13 — 16
UART0_TX,CLKSEL1/CAN0_TX/SPIM1_SS1/HPS_GPIO62 — H17 HPS_V3P3_GPIO14 — 16
I2C0_SDA/UART1_RX/SPIM1_CLK/HPS_GPIO63 — C19 HPS_V3P3_GPIO15 — 16
I2C0_SCL/UART1_TX/SPIM1_MOSI/HPS_GPIO64 — B16 HPS_V3P3_GPIO16 — 16
CAN0_RX/UART0_RX/SPIM1_MISO/HPS_GPIO65 — B19 HPS_V3P3_GPIO17 — 16
CAN0_TX,CLKSEL0/UART0_TX/SPIM1_SS0/HPS_GPIO66 — C16 HPS_V3P3_GPIO18 — 16

Bank 7B VCCIO = 3.3V

14	HPS_ENET_TX_DATA[3..0]				
14	HPS_ENET_RX_DATA[3..0]				
14	HPS_ENET_GTX_CLK	J15	NAND_ALE/RGMII1_TX_CLK/QSPI_SS3/HPS_GPIO14	QSPI_IO0/ - /USB1_CLK/HPS_GPIO29	A8 HPS_V3P3_GPIO19
	HPS_ENET_TX_DATA0	A16	NAND_CE/RGMII1_TXD0/USB1_D0/HPS_GPIO15	QSPI_IO1/ - /USB1_STP/HPS_GPIO30	H16 HPS_V3P3_GPIO20
	HPS_ENET_TX_DATA1	J14	NAND_CLE/RGMII1_TXD1/USB1_D1/HPS_GPIO16	QSPI_IO2/ - /USB1_DIR/HPS_GPIO31	A7 HPS_V3P3_GPIO21
	HPS_ENET_TX_DATA2	A15	NAND_RE/RGMII1_TXD2/USB1_D2/HPS_GPIO17	QSPI_IO3/ - /USB1_NXT/HPS_GPIO32	J16 HPS_V3P3_GPIO22
	HPS_ENET_TX_DATA3	D17	NAND_RB/RGMII1_TXD3/USB1_D3/HPS_GPIO18	QSPI_SS0,BOOTSEL1/ - / - /HPS_GPIO33	A6 HPS_V3P3_GPIO23
	HPS_ENET_RX_DATA0	A14	NAND_DQ0/RGMII1_RXD0/ - /HPS_GPIO19	QSPI_CLK/ - / - /HPS_GPIO34	C14 HPS_V3P3_GPIO24
14	HPS_ENET_MDIO	E16	NAND_DQ1/RGMII1_MDIO/I2C3_SDA/HPS_GPIO20	QSPI_SS1/ - / - /HPS_GPIO35	B14 HPS_ENET_INT_N
14	HPS_ENET_MDC	A13	NAND_DQ2/RGMII1_MDC/I2C3_SCL/HPS_GPIO21		
14	HPS_ENET_RX_DV	J13	NAND_DQ3/RGMII1_RX_CTL/USB1_D4/HPS_GPIO22		
14	HPS_ENET_TX_EN	A12	NAND_DQ4/RGMII1_TX_CTL/USB1_D5/HPS_GPIO23		
14	HPS_ENET_RX_CLK	J12	NAND_DQ5/RGMII1_RX_CLK/USB1_D6/HPS_GPIO24		
	HPS_ENET_RX_DATA1	A11	NAND_DQ6/RGMII1_RXD1/USB1_D7/HPS_GPIO25		
	HPS_ENET_RX_DATA2	C15	NAND_DQ7/RGMII1_RXD2/ - /HPS_GPIO26		
	HPS_ENET_RX_DATA3	A9	NAND_WP/RGMII1_RXD3/QSPI_SS2/HPS_GPIO27		
	HPS_BOOTSEL2	D15	NAND_WE,BOOTSEL2/QSPI_SS1/ - /HPS_GPIO28		

Bank 7C VCCIO = 3.3V

13	HPS_SDMMC_CMD	D14	SDMMC_CMD/USB0_D0/ - /HPS_GPIO36	SDMMC_PWREN/USB0_D1/ - /HPS_GPIO37	A5 HPS_EMMC_RST_N 13
13	HPS_SDMMC_DATA0	C13	SDMMC_D0/USB0_D2/ - /HPS_GPIO38	SDMMC_D4/USB0_D4/ - /HPS_GPIO40	H13 HPS_SDMMC_DATA4 13
13	HPS_SDMMC_DATA1	B6	SDMMC_D1/USB0_D3/ - /HPS_GPIO39	SDMMC_D5/USB0_D5/ - /HPS_GPIO41	A4 HPS_SDMMC_DATA5 13
13	HPS_SDMMC_DATA2	B11	SDMMC_D2/USB0_DIR/ - /HPS_GPIO46	SDMMC_D6/USB0_D6/ - /HPS_GPIO42	H12 HPS_SDMMC_DATA6 13
13	HPS_SDMMC_DATA3	B9	SDMMC_D3/USB0_NXT/ - /HPS_GPIO47	SDMMC_D7/USB0_D7/ - /HPS_GPIO43	B4 HPS_SDMMC_DATA7 13
13	HPS_EMMC_SEL	B12	SDMMC_FB_CLK_IN/USB0_CLK/ - /HPS_GPIO44	SDMMC_CCLK_OUT/USB0_STP/ - /HPS_GPIO45	B8 HPS_SDMMC_CLK 13

Bank 7D VCCIO = 3.3V

	HPS_USB_DATA4	C8	RGMII0_RXD0/USB1_D4/ - /HPS_GPIO5	RGMII0_TXD0/USB1_D0/ - /HPS_GPIO1	C10 HPS_USB_DATA0
15	HPS_USB_STP	C5	RGMII0_RXD1/USB1_STP/ - /HPS_GPIO11	RGMII0_TXD1/USB1_D1/ - /HPS_GPIO2	F5 HPS_USB_DATA1
15	HPS_USB_DIR	E5	RGMII0_RXD2/USB1_DIR/ - /HPS_GPIO12	RGMII0_TXD2/USB1_D2/ - /HPS_GPIO3	C9 HPS_USB_DATA2
15	HPS_USB_NXT	D5	RGMII0_RXD3/USB1_NXT/ - /HPS_GPIO13	RGMII0_TXD3/USB1_D3/ - /HPS_GPIO4	C4 HPS_USB_DATA3
15	HPS_USB_CLKOUT	G4	RGMII0_RX_CLK/USB1_CLK/ - /HPS_GPIO10	RGMII0_TX_CTL/ - / - /HPS_GPIO9	C6
	HPS_USB_DATA7	F4	RGMII0_RX_CTL/USB1_D7/ - /HPS_GPIO8	RGMII0_TX_CLK/ - / - /HPS_GPIO0	E4
	HPS_USB_DATA5	D4	RGMII0_MDIO/USB1_D5/I2C2_SDA/HPS_GPIO6		
	HPS_USB_DATA6	C7	RGMII0_MDC/USB1_D6/I2C2_SCL/HPS_GPIO7		

5CSEBA6U23I7

UBS PHY Interface (ULPI)

15 HPS_USB_DATA[7..0]

Ethernet PHY Interface (RGMII)

HPS Clock

3,7 HPS_CLK1_25

HPS JTAG INTERFACE

4 HPS_TCK
4 HPS_TMS
4 HPS_TDI
4 HPS_TDO
16 JTAG_TRST

Default Setting: BOOTSEL[2:0]=101 (from eMMC or SD Card)

HPS_V3P3_GPIO12 — DNI R146 1K — HPS_BOOTSEL0 (BOOTSEL0) R21 10K
HPS_V3P3_GPIO23 — R220 1K — HPS_BOOTSEL1 (BOOTSEL1) R216 10K DNI
VCC3P3 — DNI R29 1K — HPS_BOOTSEL2 (BOOTSEL2) R158 10K

CLKSEL[1:0] =00

VCC3P3
R153 1K — HPS_V3P3_GPIO18 (CLOCKSEL0) R27 10K DNI
R150 1K — HPS_V3P3_GPIO14 (CLOCKSEL1) R28 10K DNI

U14N

CYCLONE V SoC BANK XCVR

Bank GXB_L0

AF1	GXB_RX_L0n,GXB_REFCLK_L0n	GXB_TX_L0p AD2
AF2	GXB_RX_L0p,GXB_REFCLK_L0p	GXB_TX_L0n AD1
AB1	GXB_RX_L1n,GXB_REFCLK_L1n	GXB_TX_L1p Y2
AB2	GXB_RX_L1p,GXB_REFCLK_L1p	GXB_TX_L1n Y1
V1	GXB_RX_L2n,GXB_REFCLK_L2n	GXB_TX_L2p T2
V2	GXB_RX_L2p,GXB_REFCLK_L2p	GXB_TX_L2n T1
V5	REFCLK0Lp	
V4	REFCLK0Ln	

Bank GXB_L1

P1	GXB_RX_L3n,GXB_REFCLK_L3n	GXB_TX_L3p M2
P2	GXB_RX_L3p,GXB_REFCLK_L3p	GXB_TX_L3n M1
K1	GXB_RX_L4n,GXB_REFCLK_L4n	GXB_TX_L4p H2
K2	GXB_RX_L4p,GXB_REFCLK_L4p	GXB_TX_L4n H1
F1	GXB_RX_L5n,GXB_REFCLK_L5n	GXB_TX_L5p D2
F2	GXB_RX_L5p,GXB_REFCLK_L5p	GXB_TX_L5n D1
P8	REFCLK1Lp	
N8	REFCLK1Ln	

5CSEBA6U23I7

Title: Cyclone V - System on Module

Size	Document Number	Rev
B	FPGA : Bank 7	B0

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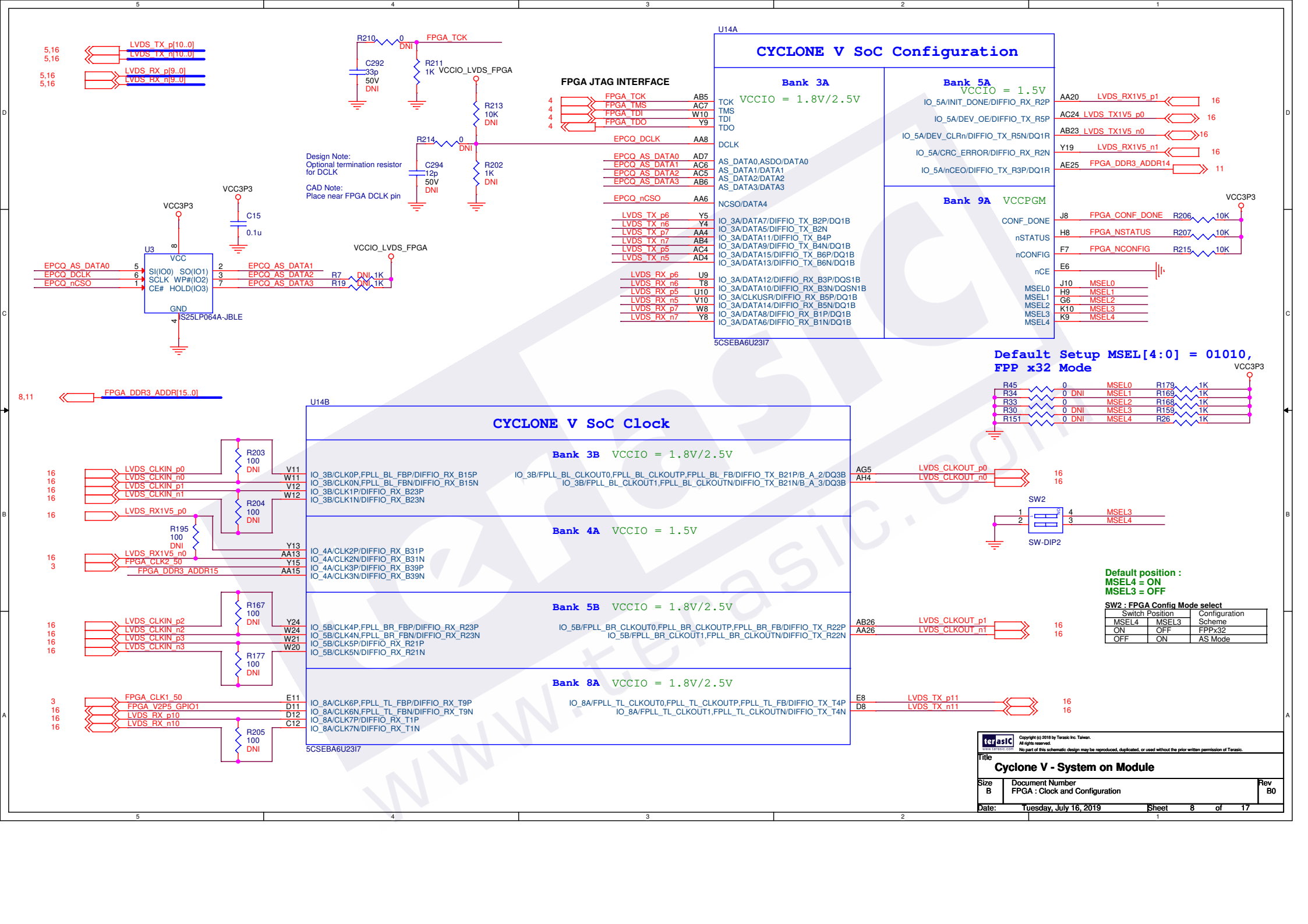
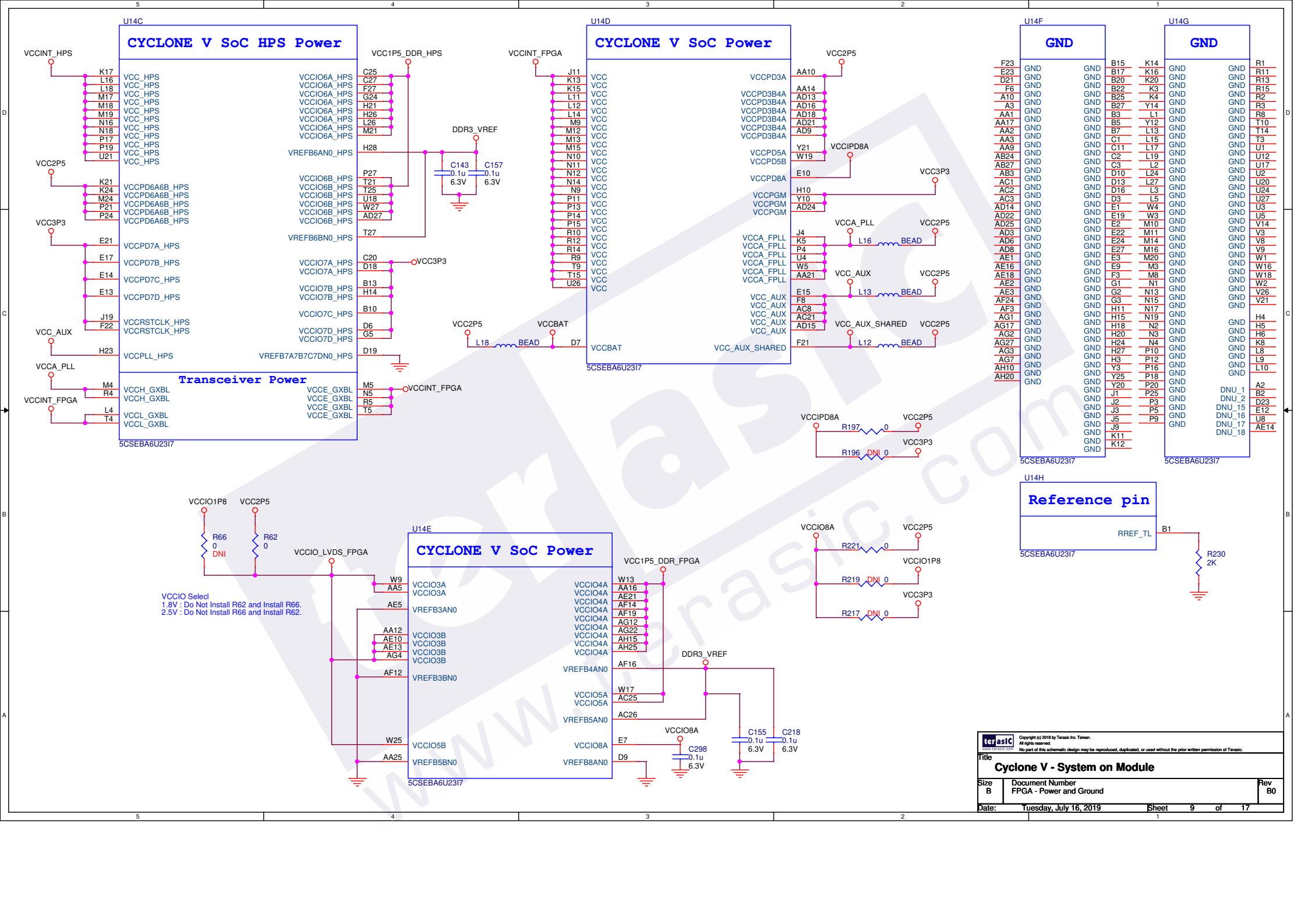

U14A
CYCLONE V SoC Configuration
Bank 3A
VCCIO = 1.8V/2.5V
Bank 5A
VCCIO = 1.5V
Bank 9A
VCCPGM
FPGA JTAG INTERFACE
5CSEBA6U23I7
U14B
CYCLONE V SoC Clock
Bank 3B
VCCIO = 1.8V/2.5V
Bank 4A
VCCIO = 1.5V
Bank 5B
VCCIO = 1.8V/2.5V
Bank 8A
VCCIO = 1.8V/2.5V
5CSEBA6U23I7
U3
IS25LP064A-JBLE
Design Note:
Optional termination resistor for DCLK
CAD Note:
Place near FPGA DCLK pin
Default Setup MSEL[4:0] = 01010,
FPP x32 Mode
SW2
SW-DIP2
Default position :
MSEL4 = ON
MSEL3 = OFF
SW2 : FPGA Config Mode select
Switch Position
MSEL4 MSEL3
ON OFF FPPx32
OFF ON AS Mode
Cyclone V - System on Module
FPGA : Clock and Configuration
Tuesday, July 16, 2019


U14C
CYCLONE V SoC HPS Power
VCC_HPS
VCCPD6A6B_HPS
VCCPD7A_HPS
VCCPD7B_HPS
VCCPD7C_HPS
VCCPD7D_HPS
VCCRSTCLK_HPS
VCCPLL_HPS
VCCIO6A_HPS
VCCIO6B_HPS
VCCIO7A_HPS
VCCIO7B_HPS
VCCIO7C_HPS
VCCIO7D_HPS
VREFB6AN0_HPS
VREFB6BN0_HPS
VREFB7A7B7C7DN0_HPS
Transceiver Power
VCCH_GXBL
VCCL_GXBL
VCCE_GXBL
5CSEBA6U23I7
U14D
CYCLONE V SoC Power
VCC
VCCPD3A
VCCPD3B4A
VCCPD5A
VCCPD5B
VCCPD8A
VCCPGM
VCCA_FPLL
VCC_AUX
VCC_AUX_SHARED
VCCBAT
U14F
GND
U14G
U14H
Reference pin
RREF_TL
U14E
CYCLONE V SoC Power
VCCIO_LVDS_FPGA
VCC1P5_DDR_FPGA
VCCIO1P8
VCCIO8A
VCCIO3A
VCCIO3B
VCCIO4A
VCCIO5A
VCCIO5B
VCCIO8A
VREFB3AN0
VREFB3BN0
VREFB4AN0
VREFB5AN0
VREFB5BN0
VREFB8AN0
VCCINT_HPS
VCCINT_FPGA
VCC2P5
VCC3P3
VCC_AUX
VCCA_PLL
VCCIPD8A
DDR3_VREF
VCCIO Select
1.8V : Do Not Install R62 and Install R66.
2.5V : Do Not Install R66 and Install R62.
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Title
Cyclone V - System on Module
Size B
Document Number
FPGA - Power and Ground
Rev B0
Date: Tuesday, July 16, 2019
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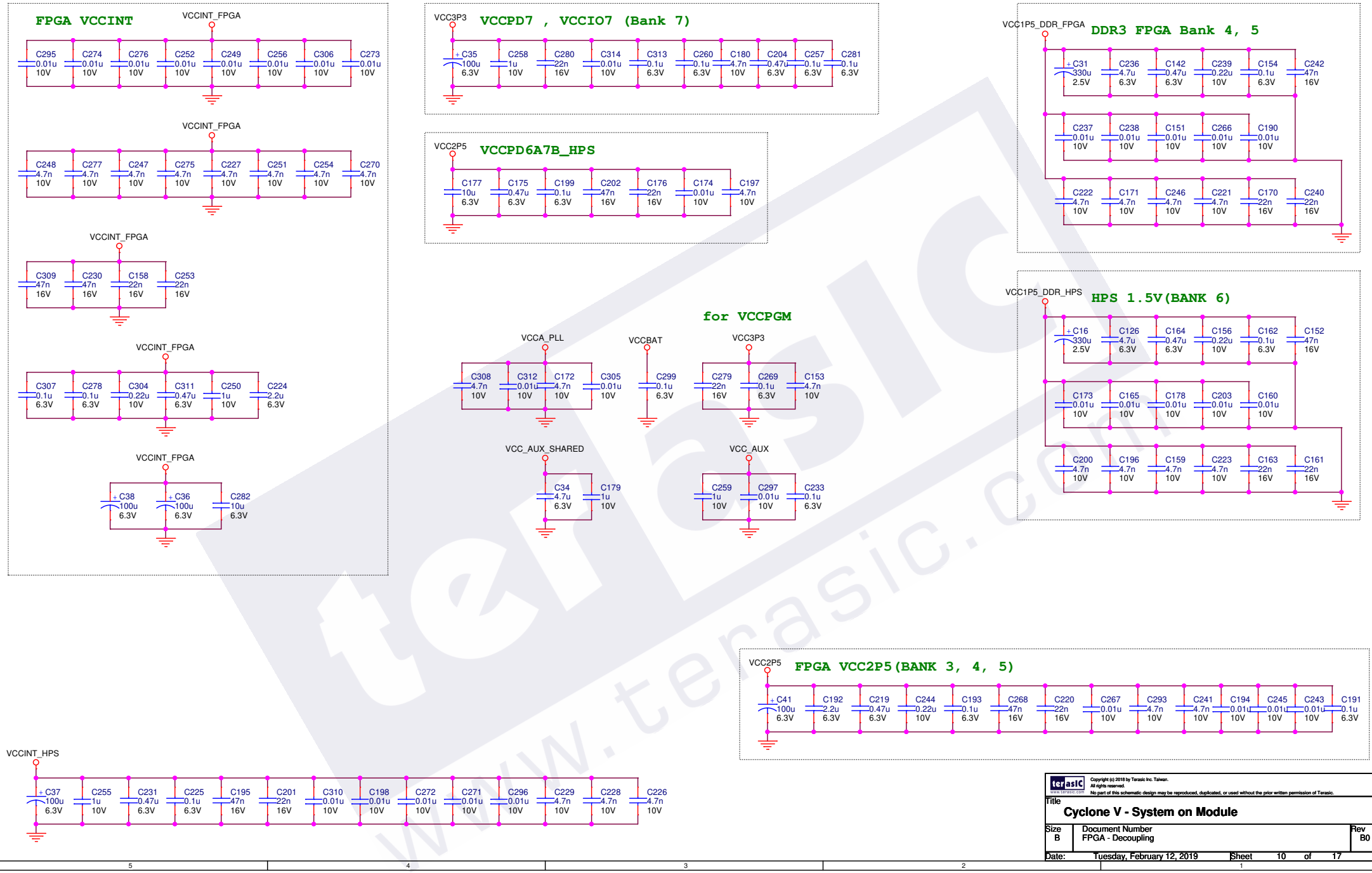

Title
Cyclone V - System on Module

Size	Document Number	Rev
B	FPGA - Decoupling	B0

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DDR3 Interface (FPGA)

Note :
you can only swap the DQ signals
within x8 group (e.g. 0-7,8-15,16-23,24-31)
on the DDR3 chips

Note : you can swap the signals on the OCT resistor array
(include NC pin)

6,8 FPGA_DDR3_ADDR[15..0]
6 FPGA_DDR3_DQ[31..0]
6 FPGA_DDR3_BA[2..0]
6 FPGA_DDR3_DM[3..0]
6 FPGA_DDR3_DQS_P[3..0]
6 FPGA_DDR3_DQS_N[3..0]
6 FPGA_DDR3_CK_P
6 FPGA_DDR3_CK_N
6 FPGA_DDR3_CKE0
6 FPGA_DDR3_CS_N0
6 FPGA_DDR3_RESET_N
6 FPGA_DDR3_WE_N
6 FPGA_DDR3_RAS_N
6 FPGA_DDR3_CAS_N
6 FPGA_DDR3_ODT0
6 FPGA_DDR3_CS_N1
6 FPGA_DDR3_CKE1
6 FPGA_DDR3_ODT1

VCC1P5_DDR_FPGA
R199 2K FPGA_DDR3_RESET_N
FPGA_DDR3_CK_P R166 100 FPGA_DDR3_CK_N
CAD Note:
Place close to DDR3 chip

U10 IS43TR16256A-15HBL
U15 IS43TR16256A-15HBL
DDR3_VREF
VDD VDDQ VREFDQ VREFCA VSS VSSQ
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12/BC_n A13 A14
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15
CLK CLK_n CKE CS RESET WE RAS CAS
LDQS LDQSn UDQS UDQSn
BA0 BA1 BA2
NC1 NC2 NC3 NC4 NC5
LDM UDM ODT ZQ

R134 240 DNI
R135 240
R185 240 DNI
R194 240

DDR3_VTT
0.1u C26 C20 C210 C109
0.1u C25 C108 C138 C186
0.1u C21 C19 C133 C134

R40 51 FPGA_DDR3_ADDR11
R32 51 FPGA_DDR3_ADDR14
R36 51 FPGA_DDR3_CAS_N
R37 51 FPGA_DDR3_WE_N
R39 51 FPGA_DDR3_ADDR0
R41 51 FPGA_DDR3_ADDR9
R42 51 FPGA_DDR3_ADDR13
R46 51 FPGA_DDR3_ADDR2
R163 51 FPGA_DDR3_ADDR10
R160 51 FPGA_DDR3_ADDR12
R156 51 FPGA_DDR3_BA1
R161 51 FPGA_DDR3_ADDR1
R154 51 FPGA_DDR3_ADDR4
R155 51 FPGA_DDR3_ADDR6
R35 51 FPGA_DDR3_RAS_N
R31 51 FPGA_DDR3_ADDR8
R47 51 FPGA_DDR3_ADDR7
R172 51 FPGA_DDR3_ADDR5
R184 51 FPGA_DDR3_ADDR3
R173 51 FPGA_DDR3_BA2
R174 51 FPGA_DDR3_BA0
R175 51 FPGA_DDR3_CS_N0
R176 51 FPGA_DDR3_ODT0
R165 51 FPGA_DDR3_ODT1
R38 51 DNI FPGA_DDR3_CS_N1
R162 51 DNI FPGA_DDR3_ADDR15
R157 4.7K DNI FPGA_DDR3_CKE1
R164 4.7K FPGA_DDR3_CKE0

VCC1P5_DDR_FPGA
C114 C118 C117 C115 C116 C113 C112 C110 C149 C148 C147
2.2n 2.2n 2.2n 2.2n 2.2n 2.2n 3.3n 4.7n 0.01u 0.01u 0.01u
50V
C215 C214 C217 C187 C188 C213 C212 C216 C265 C291 C189
2.2n 2.2n 2.2n 2.2n 2.2n 2.2n 3.3n 4.7n 0.01u 0.01u 0.01u
50V

VCC1P5_DDR_FPGA
DDR3_VREF
C139 C150 C145 C94 C141 C140
0.1u 0.47u 0.47u
16V 10V
C146 C111
0.1u
16V
VCC1P5_DDR_FPGA
DDR3_VREF
C289 C290 C264 C263 C286 C287
0.1u 0.47u 0.47u
16V 10V
C288 C211
0.1u
16V

Title: Cyclone V - System on Module
Size: B
Document Number: FPGA : DDR3 SDRAM
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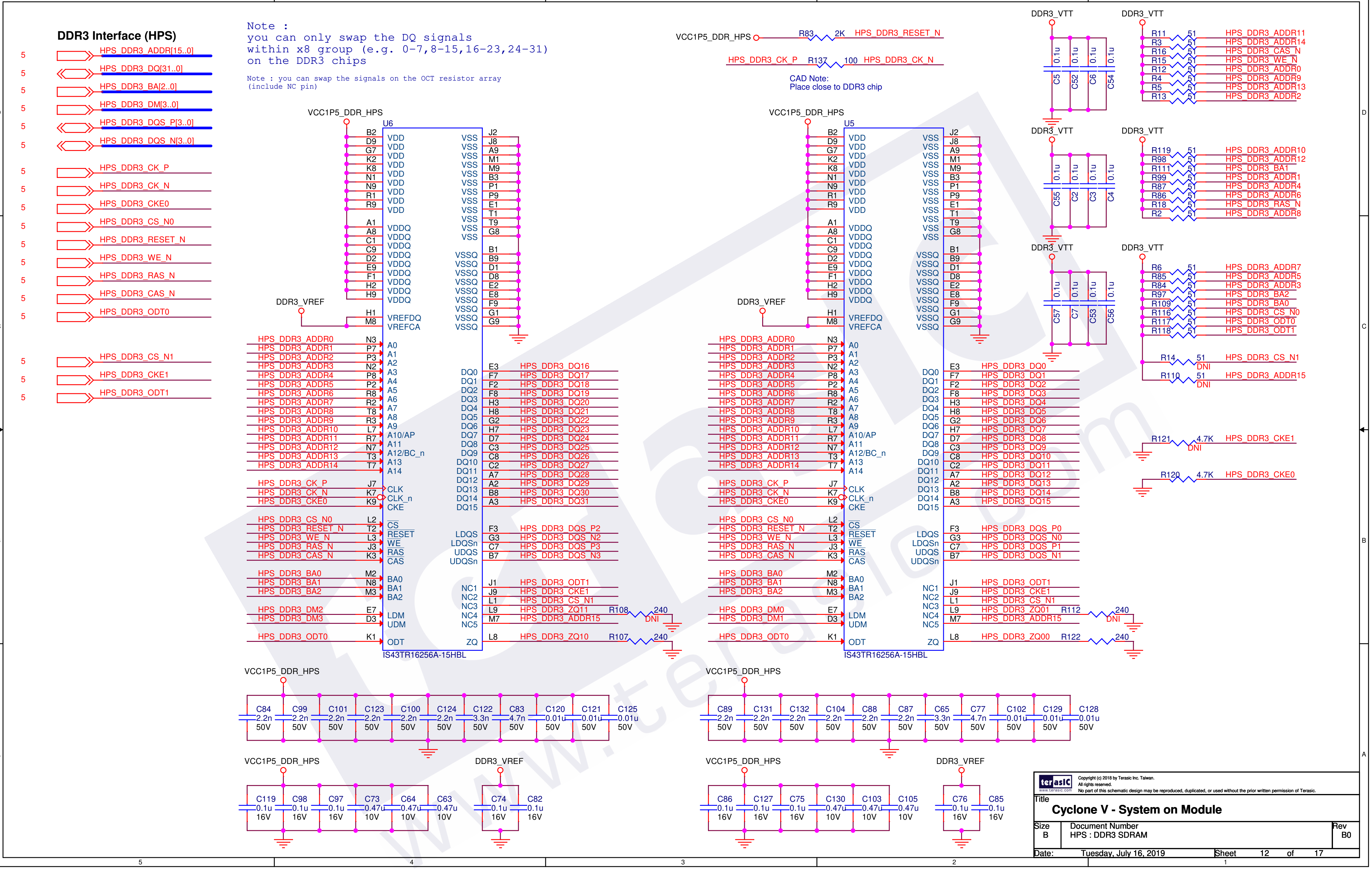
DDR3 Interface (HPS)
HPS_DDR3_ADDR[15..0]
HPS_DDR3_DQ[31..0]
HPS_DDR3_BA[2..0]
HPS_DDR3_DM[3..0]
HPS_DDR3_DQS_P[3..0]
HPS_DDR3_DQS_N[3..0]
HPS_DDR3_CK_P
HPS_DDR3_CK_N
HPS_DDR3_CKE0
HPS_DDR3_CS_N0
HPS_DDR3_RESET_N
HPS_DDR3_WE_N
HPS_DDR3_RAS_N
HPS_DDR3_CAS_N
HPS_DDR3_ODT0
HPS_DDR3_CS_N1
HPS_DDR3_CKE1
HPS_DDR3_ODT1
Note : you can only swap the DQ signals within x8 group (e.g. 0-7,8-15,16-23,24-31) on the DDR3 chips
Note : you can swap the signals on the OCT resistor array (include NC pin)
VCC1P5_DDR_HPS
R83 2K HPS_DDR3_RESET_N
HPS_DDR3_CK_P R137 100 HPS_DDR3_CK_N
CAD Note: Place close to DDR3 chip
DDR3_VTT
DDR3_VREF
U6
U5
IS43TR16256A-15HBL
R108 240 DNI
R107 240
R112 240 DNI
R122 240
R14 51 DNI
R110 51 DNI
R121 4.7K DNI HPS_DDR3_CKE1
R120 4.7K HPS_DDR3_CKE0
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Title: Cyclone V - System on Module
Size: B
Document Number: HPS : DDR3 SDRAM
Rev: B0
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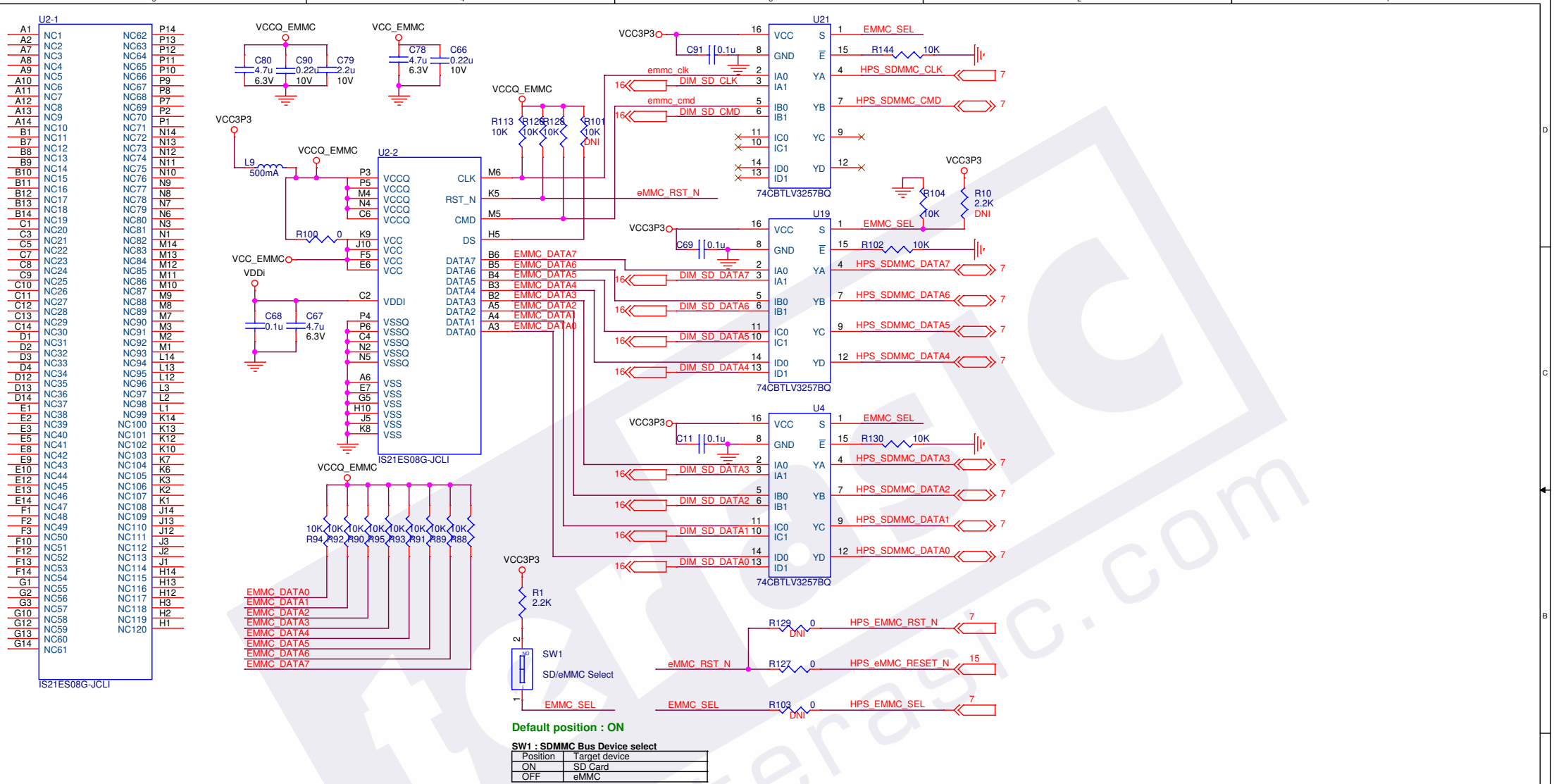

Default position : ON

SW1 : SDMMC Bus Device select

Position	Target device
ON	SD Card
OFF	eMMC

Title: **Cyclone V - System on Module**

Size	Document Number	Rev
B	HPS : eMMC and MUX	B0

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Ethernet PHY Interface (RGMII)

7 HPS_ENET_TX_DATA[3..0]
7 HPS_ENET_GTX_CLK
7 HPS_ENET_TX_EN
7 HPS_ENET_RX_DATA[3..0]
7 HPS_ENET_RX_CLK
7 HPS_ENET_RX_DV
7 HPS_ENET_INT_N
7 HPS_ENET_MDC
7 HPS_ENET_MDIO
15 HPS_ENET_RESET_N
3 CLK_ENET_25

Ethernet Interface (MDI)

16 ETH_HPS_P[3..0]
16 ETH_HPS_N[3..0]
16 ETH_LED1
16 ETH_LED2

U16 KSZ9031RNX

ENET_PLL, ENET_VCCA, ENET_DVDDL, ENET_AVDD, ENET_DVDDH
HPS_ENET_LDO_O
AVDDL_PLL, AVDDL, DVDDL, AVDDH, DVDDH, LDO_O

HPS_ENET_GTX_CLK 24 GTX_CLK
HPS_ENET_TX_EN 25 TX_EN
HPS_ENET_TX_DATA0 19 TXD0
HPS_ENET_TX_DATA1 20 TXD1
HPS_ENET_TX_DATA2 21 TXD2
HPS_ENET_TX_DATA3 22 TXD3
HPS_ENET_RX_CLK 35 RX_CLK/PHYAD2
HPS_ENET_RX_DV 33 RX_DV/CLK125_EN
HPS_ENET_RX_DATA0 32 RXD0/MODE0
HPS_ENET_RX_DATA1 31 RXD1/MODE1
HPS_ENET_RX_DATA2 28 RXD2/MODE2
HPS_ENET_RX_DATA3 27 RXD3/MODE3
CLK125_NDO_LED_MODE 41 CLK125_NDO/LED_MODE
HPS_ENET_INT_N 38 INT_N
HPS_ENET_RESET_N 42 RESET_N
HPS_ENET_MDC 36 MDC
HPS_ENET_MDIO 37 MDIO

TXRXP_A 2 ETH_HPS_P0
TXRXM_A 3 ETH_HPS_N0
TXRXP_B 5 ETH_HPS_P1
TXRXM_B 6 ETH_HPS_N1
TXRXP_C 7 ETH_HPS_P2
TXRXM_C 8 ETH_HPS_N2
TXRXP_D 10 ETH_HPS_P3
TXRXM_D 11 ETH_HPS_N3
LED1/PHYAD0 17 ETH_LED1
LED2/PHYAD1 15 ETH_LED2
ISET 48 R67 12.1K
XI 46 R60 0 CLK_ENET_25
XO 45
R63 0 DNI
CAD Note: Place near XI pin
C40 33p 50V DNI
VSS 29, VSS_PS 13, PADDLE 49

C46 10n 50V DNI — R68 49.9 DNI ETH_HPS_P0, R69 49.9 DNI ETH_HPS_N0
C47 10n 50V DNI — R70 49.9 DNI ETH_HPS_P1, R71 49.9 DNI ETH_HPS_N1
C48 10n 50V DNI — R72 49.9 DNI ETH_HPS_P2, R73 49.9 DNI ETH_HPS_N2
C49 10n 50V DNI — R74 49.9 DNI ETH_HPS_P3, R75 49.9 DNI ETH_HPS_N3

VCC3P3
R48 4.7K HPS_ENET_INT_N
R50 4.7K HPS_ENET_MDC
R198 4.7K HPS_ENET_MDIO
R58 4.7K HPS_ENET_RESET_N

PHY Address is 00001

ENET_DVDDH
R61 4.7K ETH_LED1 — R209 1K DNI
R64 4.7K DNI ETH_LED2 — R65 1K
R191 4.7K DNI HPS_ENET_RX_CLK — R51 1K

VCC3P3
R57 4.7K DNI CLK125_NDO_LED_MODE — R49 4.7K
R190 4.7K DNI HPS_ENET_RX_DV — R52 4.7K
R59 4.7K DNI HPS_ENET_GTX_CLK — R208 4.7K DNI
R189 4.7K HPS_ENET_RX_DATA0 — R53 4.7K DNI
R188 4.7K HPS_ENET_RX_DATA1 — R54 4.7K DNI
R187 4.7K HPS_ENET_RX_DATA2 — R55 4.7K DNI
R186 4.7K HPS_ENET_RX_DATA3 — R56 4.7K DNI

VCC3P3 — L17 100ohm, 1.2A — ENET_AVDD
C302 0.22u 50V, C318 1u 10V, C319 10u 6.3V

VCC3P3 — L14 100ohm, 1.2A — ENET_DVDDH
C300 0.22u 50V, C284 1u 10V, C262 10u 6.3V

VCC1P2 — L19 100ohm, 1.2A — ENET_VCCA
C317 0.22u 50V, C316 1u 10V, C320 10u 6.3V

VCC1P2 — L15 100ohm, 1.2A — ENET_PLL
C301 0.22u 50V, C285 1u 10V, C303 10u 6.3V

VCC1P2 — L5 100ohm, 1.2A — ENET_DVDDL
C283 0.22u 50V, C315 1u 10V, C235 10u 6.3V

ENET_AVDD — Q2 AO3415 DNI — VCC1P2
HPS_ENET_LDO_O

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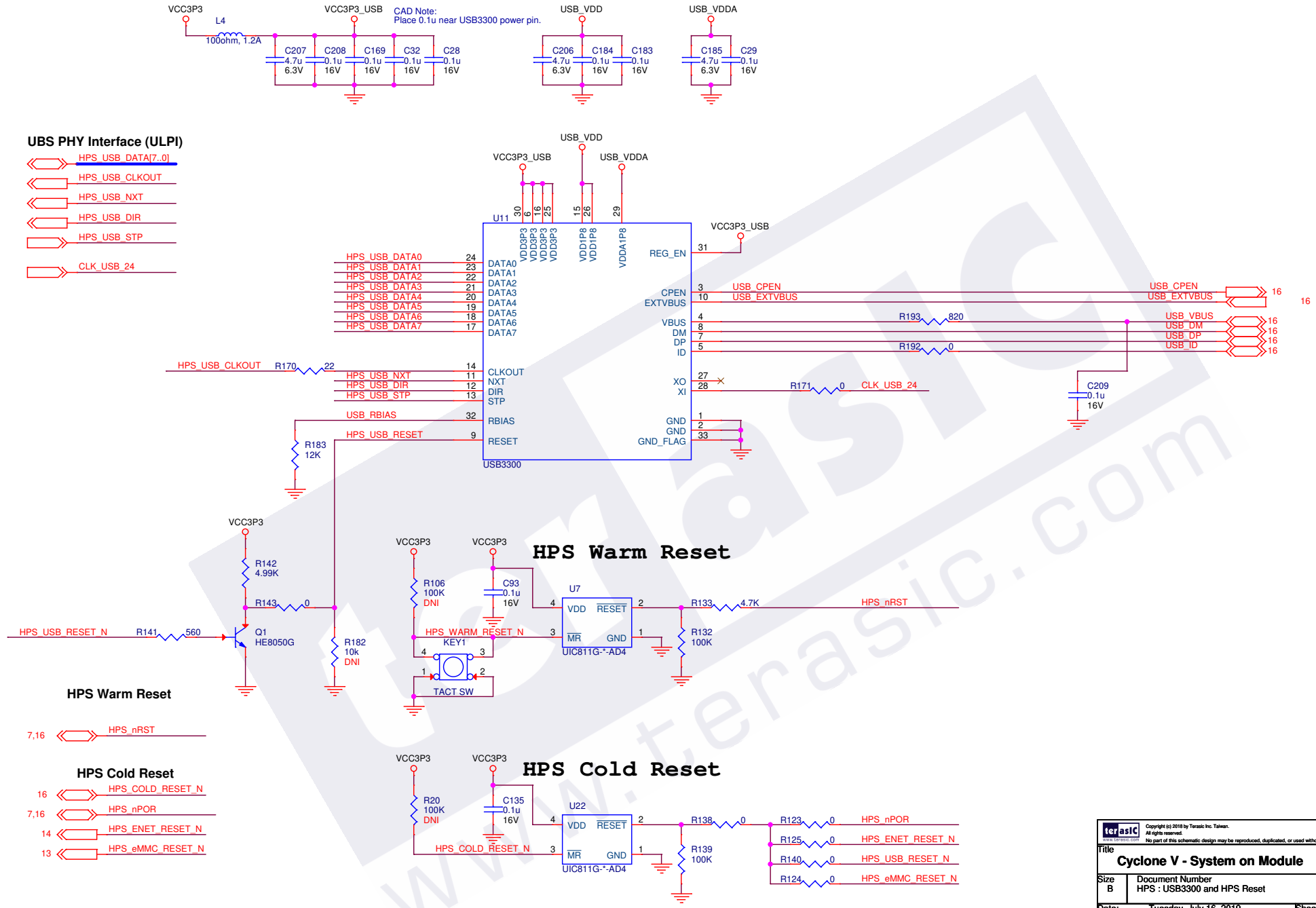

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Size: B | Document Number: HPS : USB3300 and HPS Reset | Rev: B0

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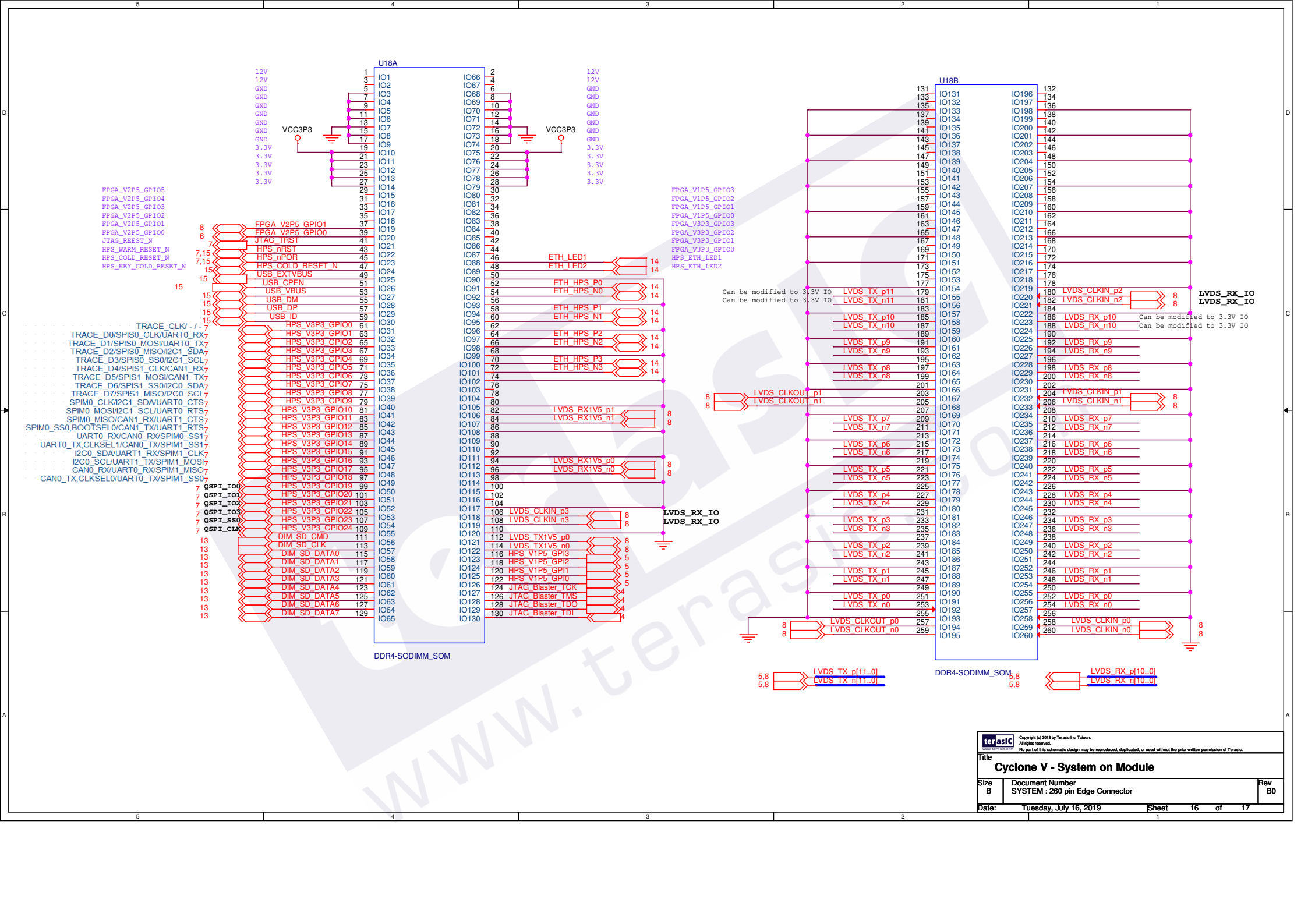
U18A
U18B
DDR4-SODIMM_SOM
DDR4-SODIMM_SOM
VCC3P3
VCC3P3
FPGA_V2P5_GPIO1
FPGA_V2P5_GPIO0
JTAG_TRST
HPS_nRST
HPS_nPOR
HPS_COLD_RESET_N
USB_EXTVBUS
USB_CPEN
USB_VBUS
USB_DM
USB_DP
USB_ID
HPS_V3P3_GPIO0
HPS_V3P3_GPIO1
HPS_V3P3_GPIO2
HPS_V3P3_GPIO3
HPS_V3P3_GPIO4
HPS_V3P3_GPIO5
HPS_V3P3_GPIO6
HPS_V3P3_GPIO7
HPS_V3P3_GPIO8
HPS_V3P3_GPIO9
HPS_V3P3_GPIO10
HPS_V3P3_GPIO11
HPS_V3P3_GPIO12
HPS_V3P3_GPIO13
HPS_V3P3_GPIO14
HPS_V3P3_GPIO15
HPS_V3P3_GPIO16
HPS_V3P3_GPIO17
HPS_V3P3_GPIO18
HPS_V3P3_GPIO19
HPS_V3P3_GPIO20
HPS_V3P3_GPIO21
HPS_V3P3_GPIO22
HPS_V3P3_GPIO23
HPS_V3P3_GPIO24
DIM_SD_CMD
DIM_SD_CLK
DIM_SD_DATA0
DIM_SD_DATA1
DIM_SD_DATA2
DIM_SD_DATA3
DIM_SD_DATA4
DIM_SD_DATA5
DIM_SD_DATA6
DIM_SD_DATA7
ETH_LED1
ETH_LED2
ETH_HPS_P0
ETH_HPS_N0
ETH_HPS_P1
ETH_HPS_N1
ETH_HPS_P2
ETH_HPS_N2
ETH_HPS_P3
ETH_HPS_N3
LVDS_RX1V5_p1
LVDS_RX1V5_n1
LVDS_RX1V5_p0
LVDS_RX1V5_n0
LVDS_CLKIN_p3
LVDS_CLKIN_n3
LVDS_TX1V5_p0
LVDS_TX1V5_n0
HPS_V1P5_GPI3
HPS_V1P5_GPI2
HPS_V1P5_GPI1
HPS_V1P5_GPI0
JTAG_Blaster_TCK
JTAG_Blaster_TMS
JTAG_Blaster_TDO
JTAG_Blaster_TDI
LVDS_TX_p11
LVDS_TX_n11
LVDS_TX_p10
LVDS_TX_n10
LVDS_TX_p9
LVDS_TX_n9
LVDS_TX_p8
LVDS_TX_n8
LVDS_CLKOUT_p1
LVDS_CLKOUT_n1
LVDS_TX_p7
LVDS_TX_n7
LVDS_TX_p6
LVDS_TX_n6
LVDS_TX_p5
LVDS_TX_n5
LVDS_TX_p4
LVDS_TX_n4
LVDS_TX_p3
LVDS_TX_n3
LVDS_TX_p2
LVDS_TX_n2
LVDS_TX_p1
LVDS_TX_n1
LVDS_TX_p0
LVDS_TX_n0
LVDS_CLKOUT_p0
LVDS_CLKOUT_n0
LVDS_CLKIN_p2
LVDS_CLKIN_n2
LVDS_RX_p10
LVDS_RX_n10
LVDS_RX_p9
LVDS_RX_n9
LVDS_RX_p8
LVDS_RX_n8
LVDS_CLKIN_p1
LVDS_CLKIN_n1
LVDS_RX_p7
LVDS_RX_n7
LVDS_RX_p6
LVDS_RX_n6
LVDS_RX_p5
LVDS_RX_n5
LVDS_RX_p4
LVDS_RX_n4
LVDS_RX_p3
LVDS_RX_n3
LVDS_RX_p2
LVDS_RX_n2
LVDS_RX_p1
LVDS_RX_n1
LVDS_RX_p0
LVDS_RX_n0
LVDS_CLKIN_p0
LVDS_CLKIN_n0
LVDS_RX_IO
LVDS_RX_IO
LVDS_TX_p[11..0]
LVDS_TX_n[11..0]
LVDS_RX_p[10..0]
LVDS_RX_n[10..0]
Can be modified to 3.3V IO
Can be modified to 3.3V IO
Can be modified to 3.3V IO
Can be modified to 3.3V IO
TRACE_CLK/ - / -
TRACE_D0/SPIS0_CLK/UART0_RX
TRACE_D1/SPIS0_MOSI/UART0_TX
TRACE_D2/SPIS0_MISO/I2C1_SDA
TRACE_D3/SPIS0_SS0/I2C1_SCL
TRACE_D4/SPIS1_CLK/CAN1_RX
TRACE_D5/SPIS1_MOSI/CAN1_TX
TRACE_D6/SPIS1_SS0/I2C0_SDA
TRACE_D7/SPIS1_MISO/I2C0_SCL
SPIM0_CLK/I2C1_SDA/UART0_CTS
SPIM0_MOSI/I2C1_SCL/UART0_RTS
SPIM0_MISO/CAN1_RX/UART1_CTS
SPIM0_SS0,BOOTSEL0/CAN1_TX/UART1_RTS
UART0_RX/CAN0_RX/SPIM0_SS1
UART0_TX,CLKSEL1/CAN0_TX/SPIM1_SS1
I2C0_SDA/UART1_RX/SPIM1_CLK
I2C0_SCL/UART1_TX/SPIM1_MOSI
CAN0_RX/UART0_RX/SPIM1_MISO
CAN0_TX,CLKSEL0/UART0_TX/SPIM1_SS0
QSPI_IO0
QSPI_IO1
QSPI_IO2
QSPI_IO3
QSPI_SS0
QSPI_CLK
FPGA_V2P5_GPIO5
FPGA_V2P5_GPIO4
FPGA_V2P5_GPIO3
FPGA_V2P5_GPIO2
FPGA_V2P5_GPIO1
FPGA_V2P5_GPIO0
JTAG_REEST_N
HPS_WARM_RESET_N
HPS_COLD_RESET_N
HPS_KEY_COLD_RESET_N
FPGA_V1P5_GPIO3
FPGA_V1P5_GPIO2
FPGA_V1P5_GPIO1
FPGA_V1P5_GPIO0
FPGA_V3P3_GPIO3
FPGA_V3P3_GPIO2
FPGA_V3P3_GPIO1
FPGA_V3P3_GPIO0
HPS_ETH_LED1
HPS_ETH_LED2
12V
GND
3.3V
terasic
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Title
Cyclone V - System on Module
Size
B
Document Number
SYSTEM : 260 pin Edge Connector
Rev
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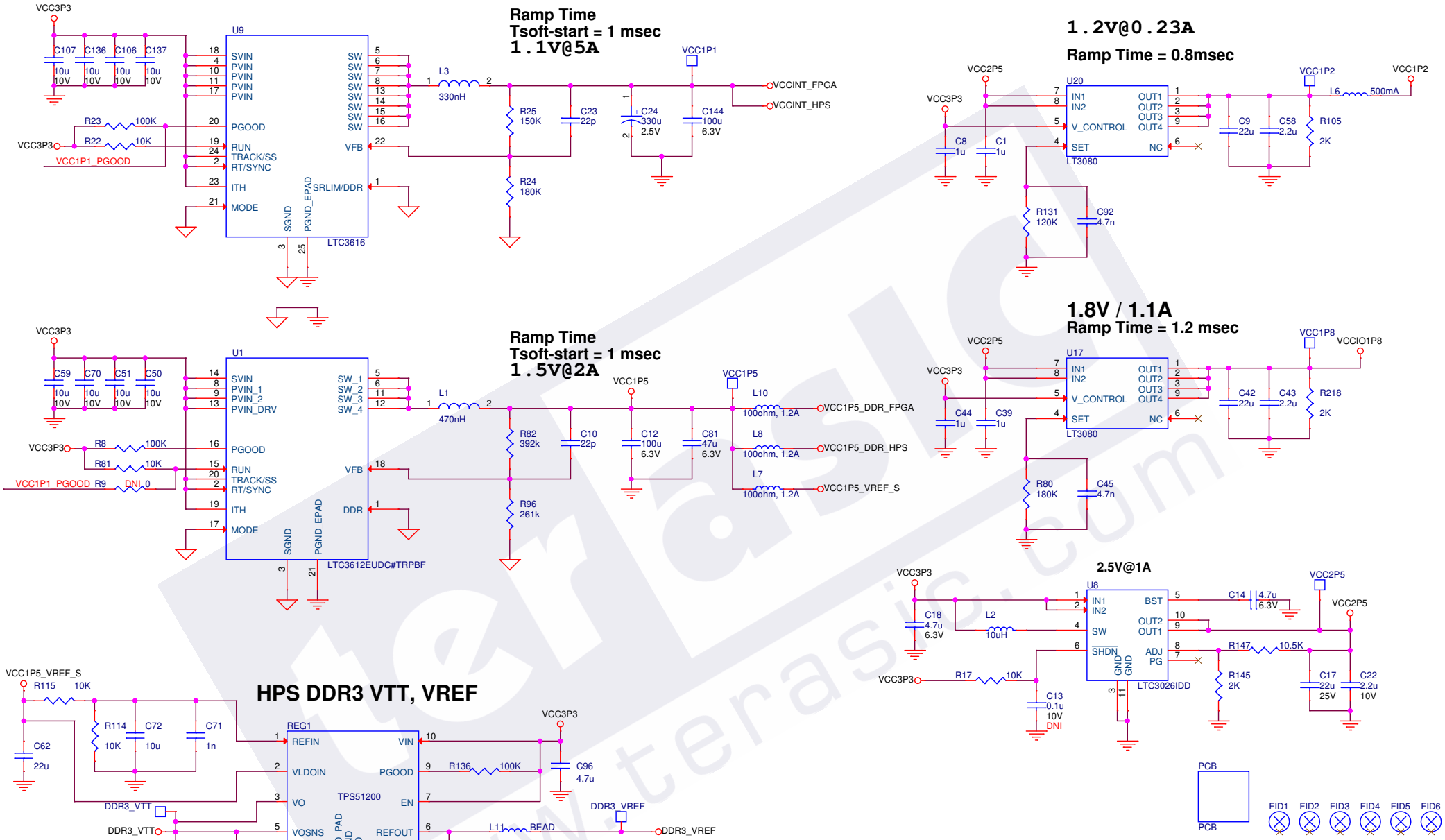

Title
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