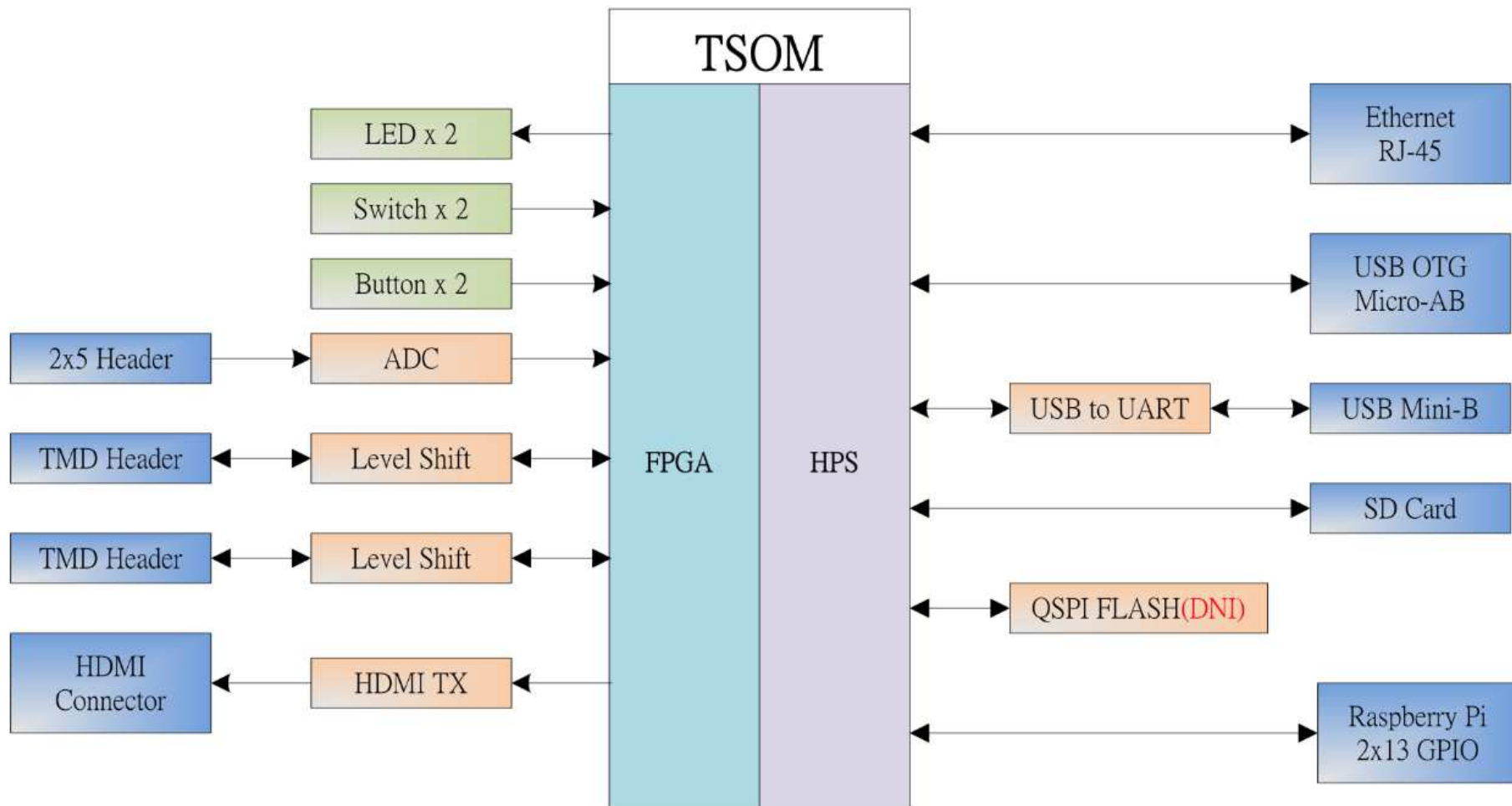


# Cyclone V SoC System on module Base Board

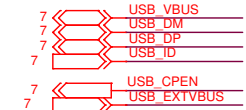
PAGE	CONTENT
01	Cover Page
02	Block Diagram
03	SOM connector
04	FPGA : ADC1 (LTC2308) for 8-channel Analog Expansion Header
05	FPGA : HDMI TX
06	HPS : UART to USB, QSPI Flash & SD CARD
07	FPGA : LED, KEY, SW / HPS : USB-OTG, Ethernet and Reset
08	Expansion IO
09	Power System
10	USB Blaster II
11	
12	
13	
14	
15	
16	
17	
18	
19	
20	
21	
22	
23	
24	



## JTAG Interface



## USB OTG Interface



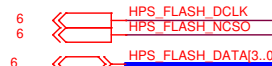
## Ethernet Interface (MDI)



## SD Card Interface



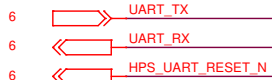
## QSPI FLASH Interface



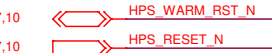
## HPS GPIO



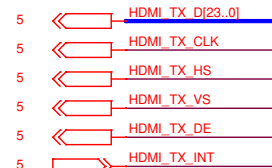
## UART Interface



## HPS Reset



## HDMI TX



## User Interface



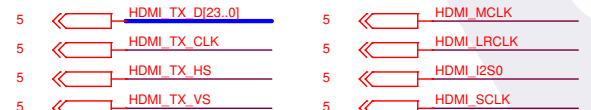
## TMD Interface



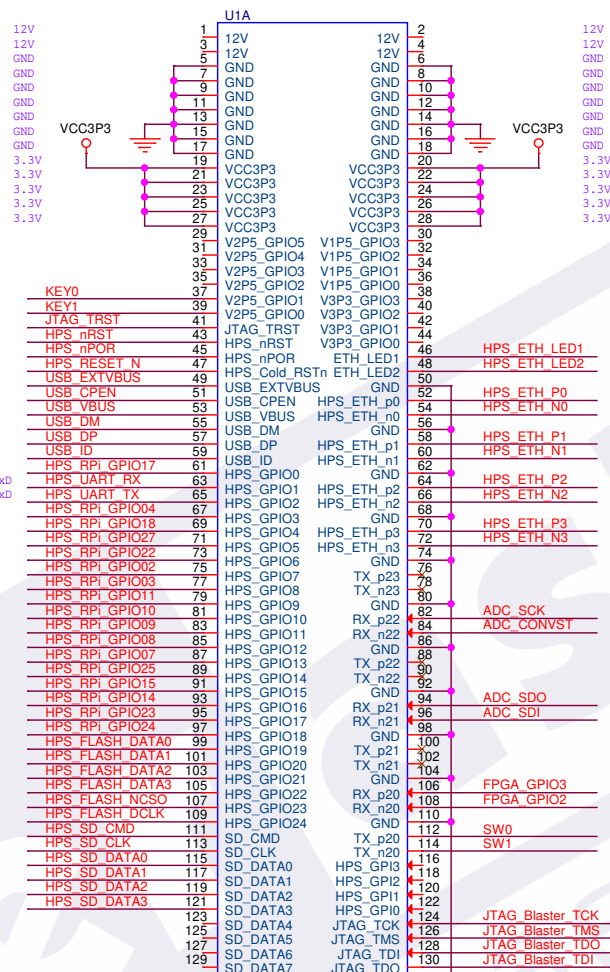
## ADC Interface



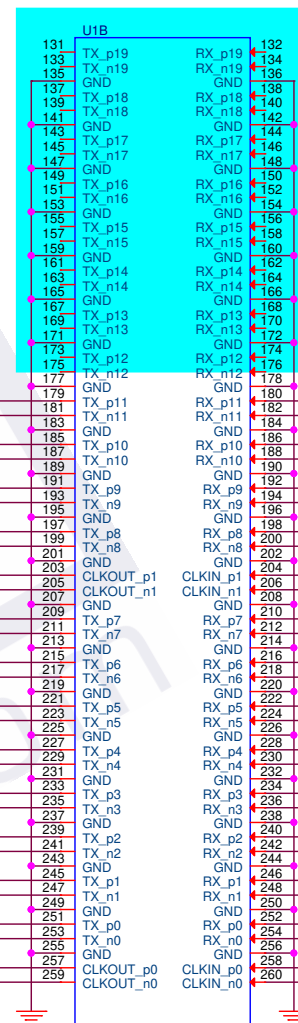
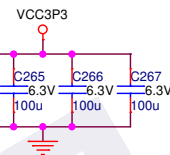
## HDMI Audio Interface



## HDMI I2C Interface



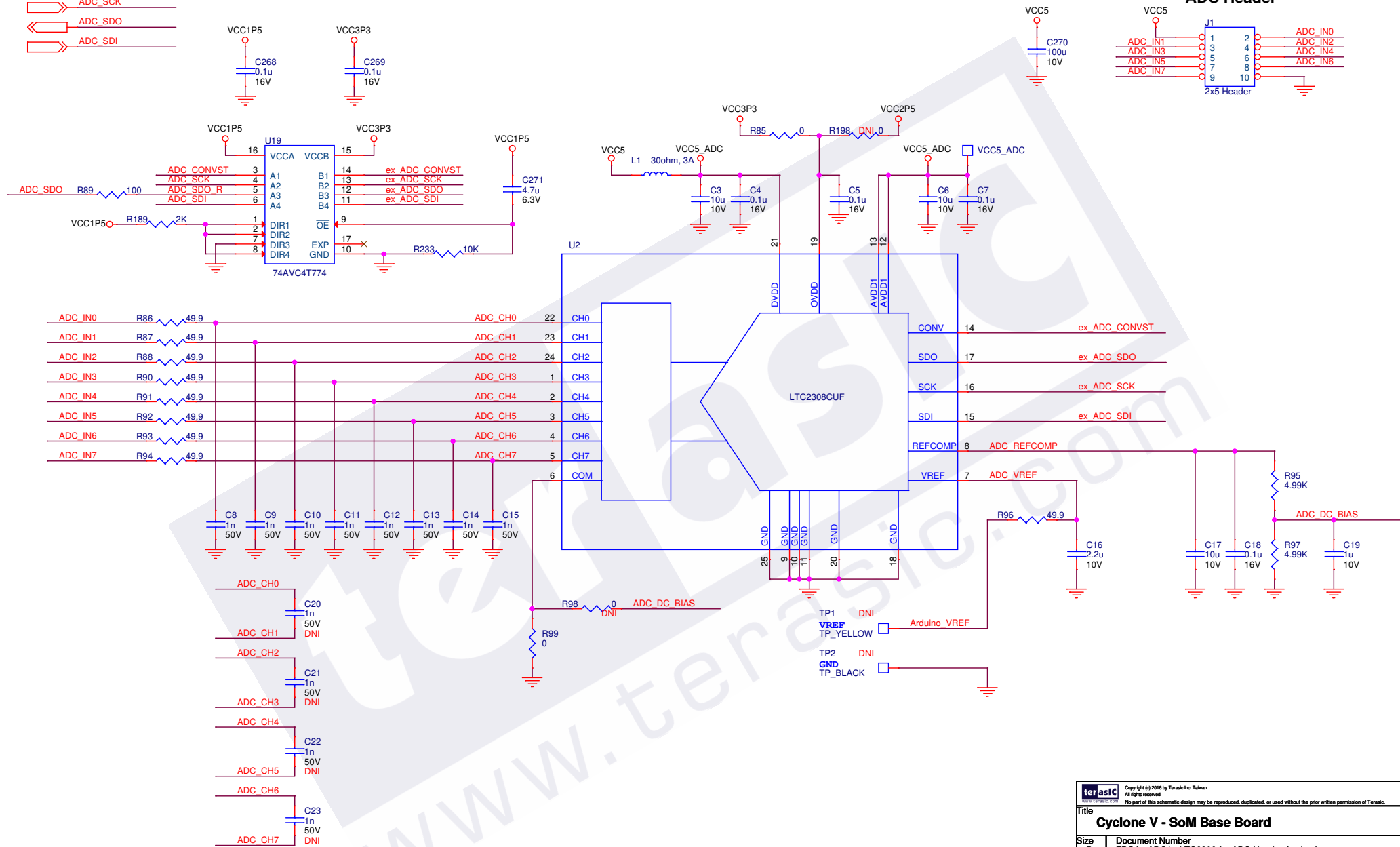
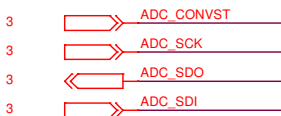
DDR4-SODIMM



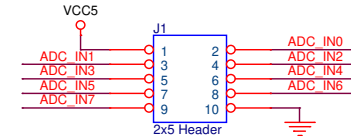
DDR4-SODIMM

<b>terasic</b> Copyright (c) 2015 by Terasic Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.			
Title			
Size B	Document Number SOM Connector		Rev B0
Date:	Tuesday, July 16, 2019		Sheet 3 of 10

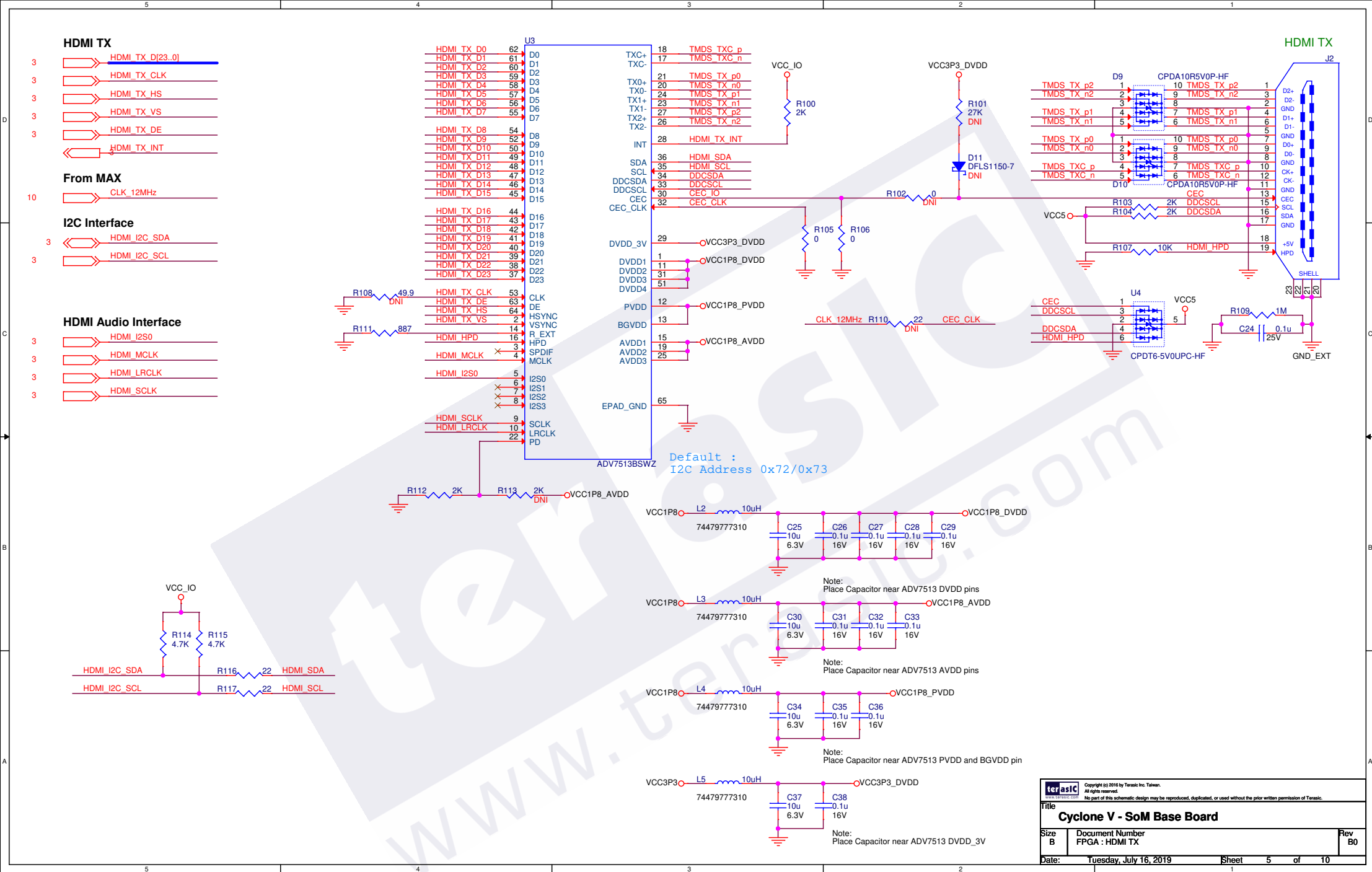
# ADC Interface



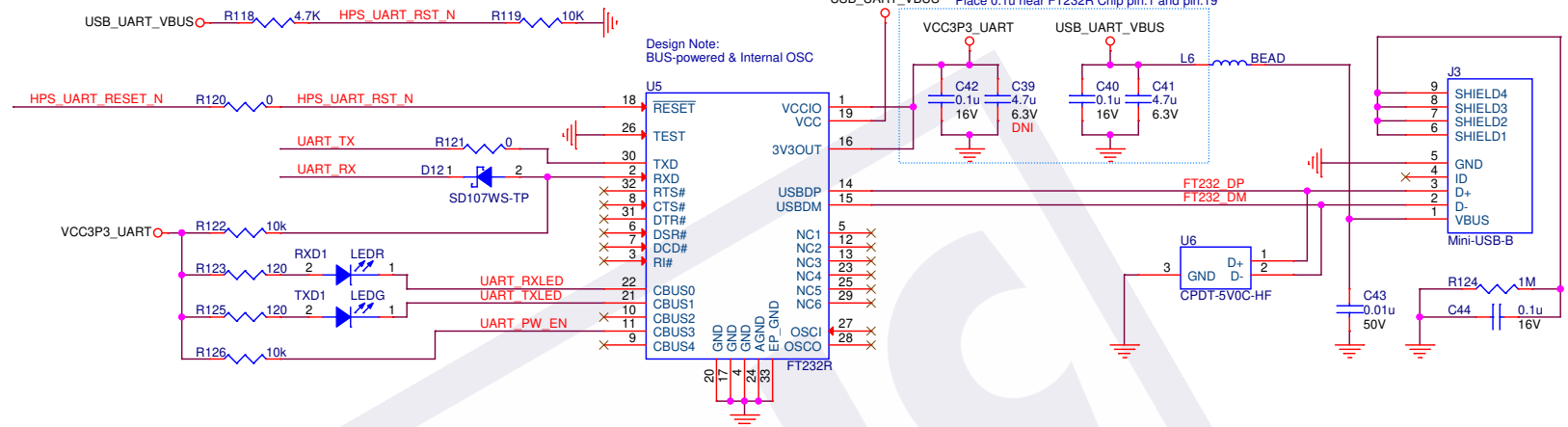
## ADC Header



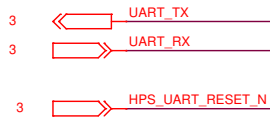




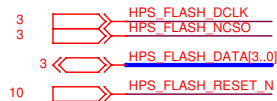
Design Note:  
BUS-powered & Internal OSC



## UART Interface



## QSPI FLASH Interface

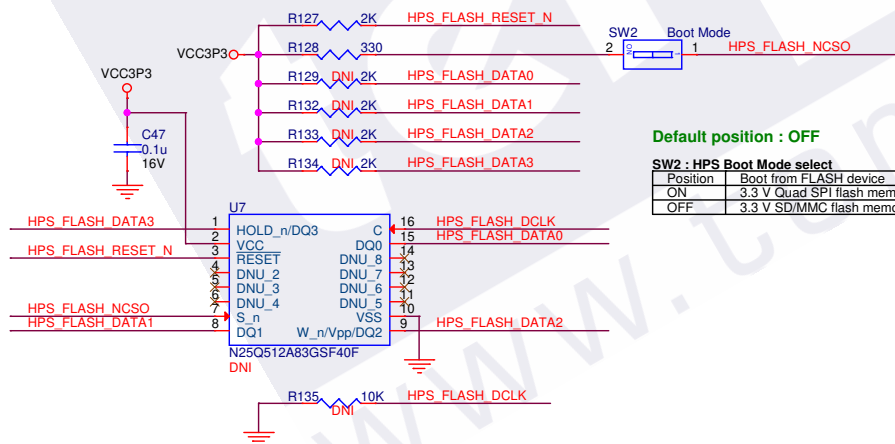


## SD Card Interface



## QSPI FLASH

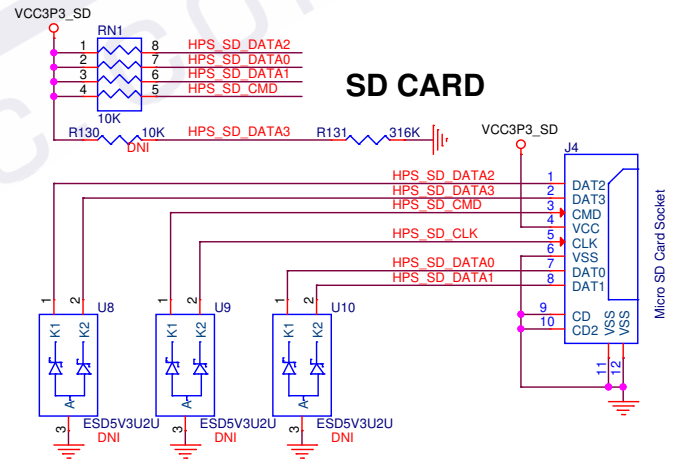
Note: place a pull down resistor on the FLASH\_DCLK wire at the Master



**Default position : OFF**

Position	Boot from FLASH device
ON	3.3 V Quad SPI flash memory
OFF	3.3 V SD/MMC flash memory

## SD CARD



## User Interface

### KEY

KEY[1..0]

### SWITCH

SW[1..0]

### LED

LED[1..0]

## HPS Reset

HPS\_WARM\_RST\_N

HPS\_RESET\_N

## USB OTG Interface

USB\_VBUS

USB\_DM

USB\_DP

USB\_ID

USB\_OPEN

USB\_EXTVBUS

## Ethernet Interface (MDI)

HPS\_ETH\_P[3..0]

HPS\_ETH\_N[3..0]

HPS\_ETH\_LED1

HPS\_ETH\_LED2

## User Button

## User LED and Switch

## HPS Reset Button

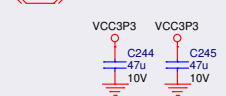
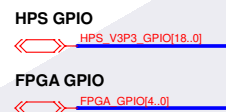
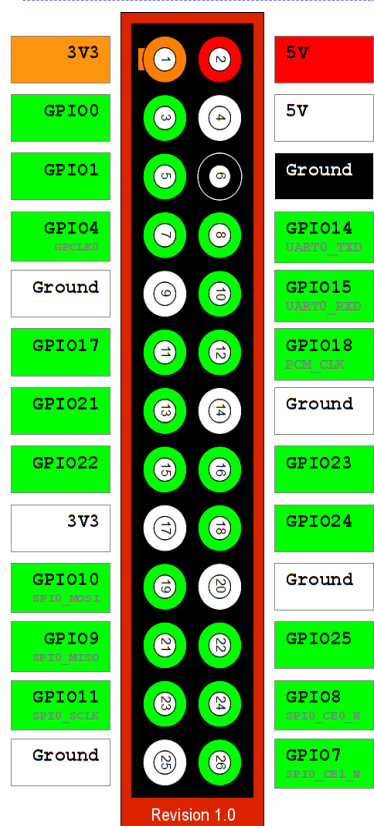
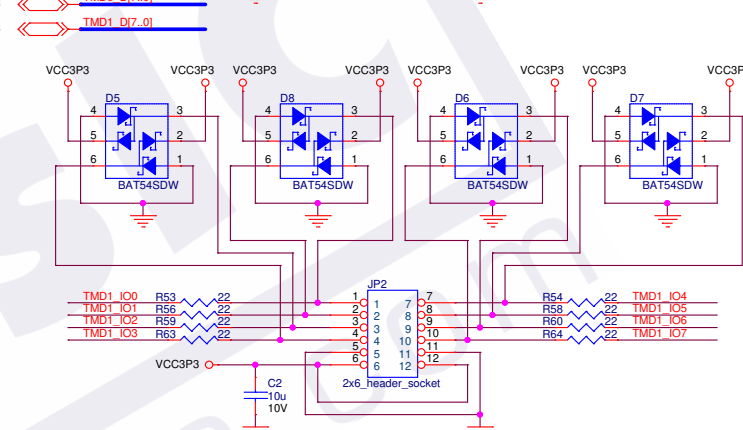
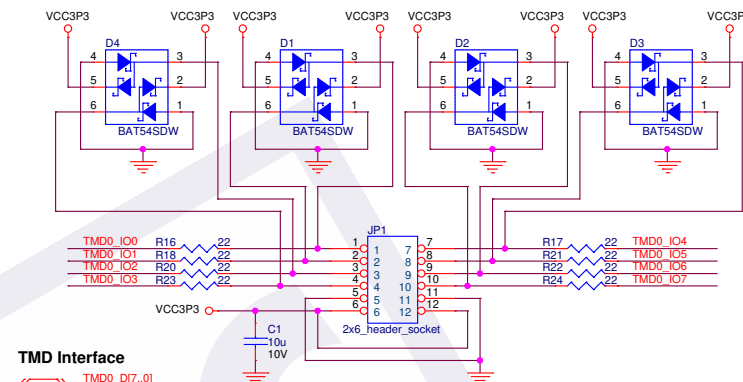
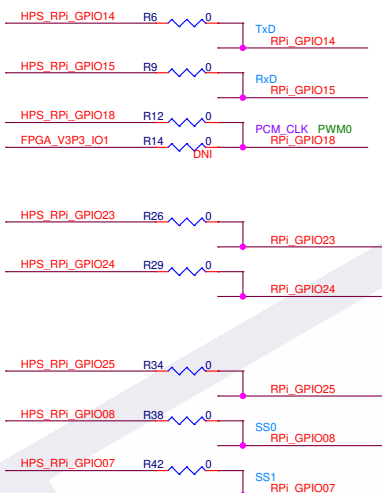
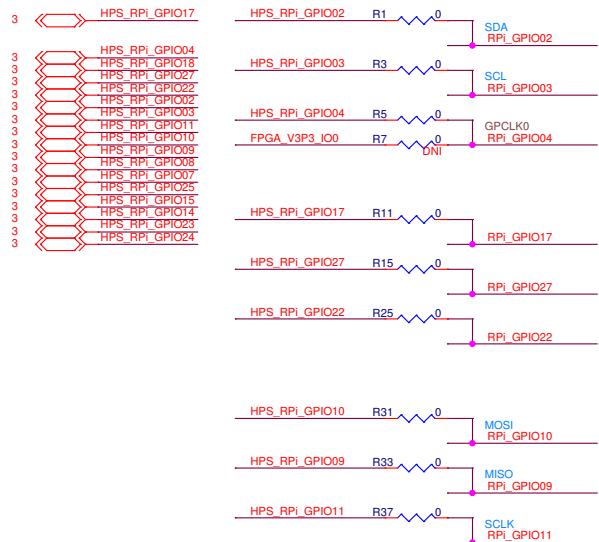
### Cold Reset

### Warm Reset

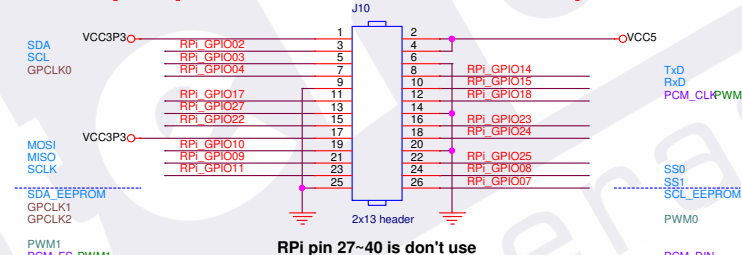
## USB OTG

## Ethernet RJ-45

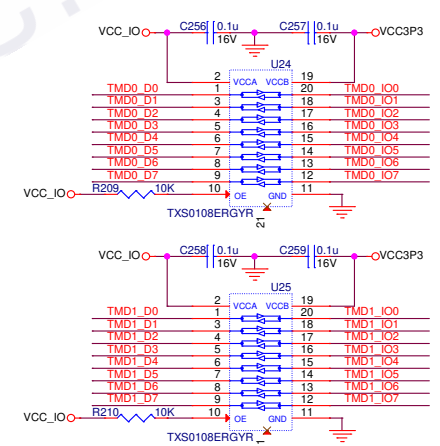
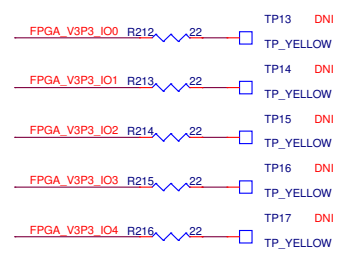
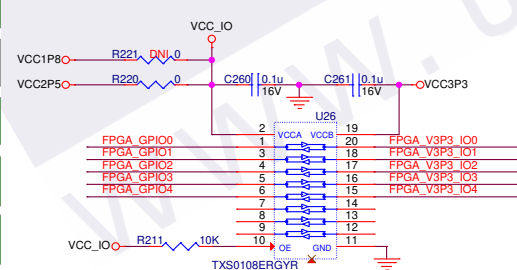
<b>terasic</b> Copyright (c) 2016 by Terasic Inc. Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.		
Title <b>Cyclone V - SoM Base Board</b>		
Size B	Document Number FPGA : LED, KEY, SW and HPS USB-OTG, Ethernet and Reset	Rev B0
Date: Tuesday, July 16, 2019	Sheet 7	of 10

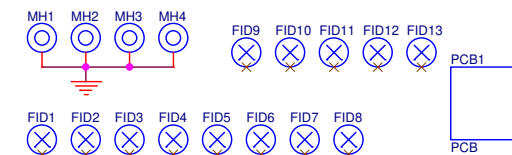
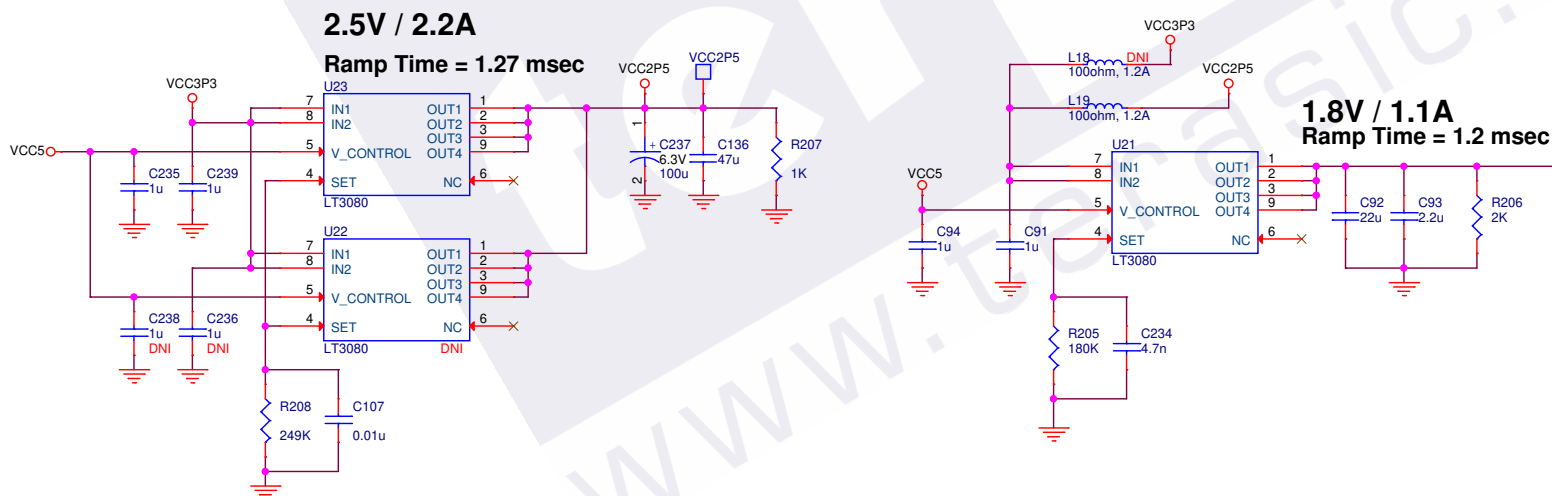
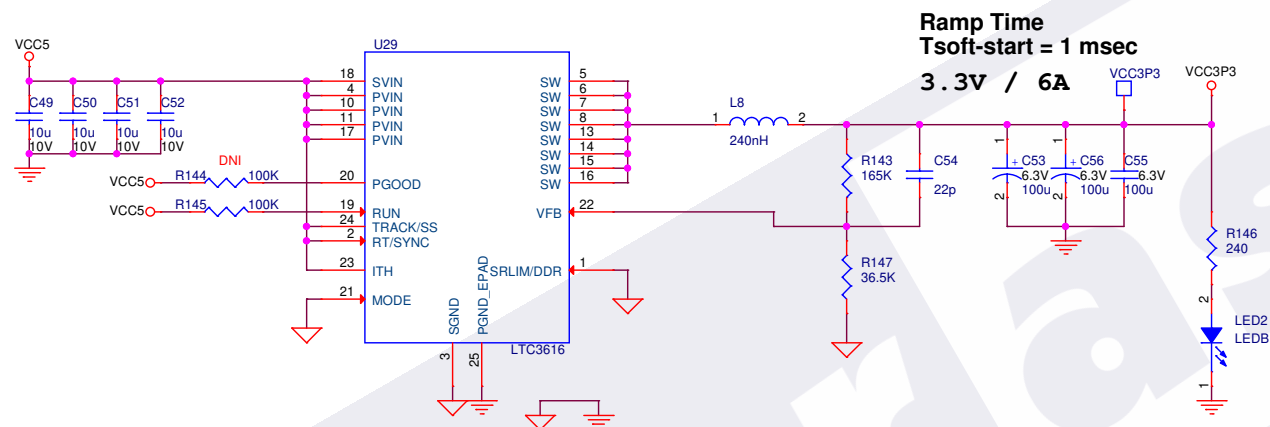
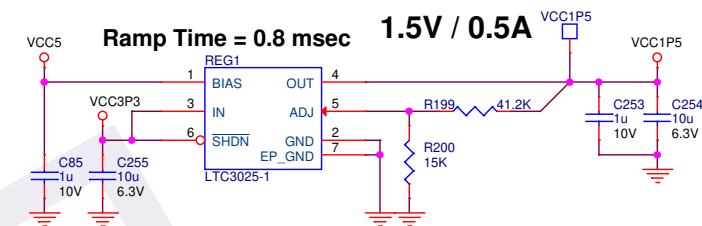
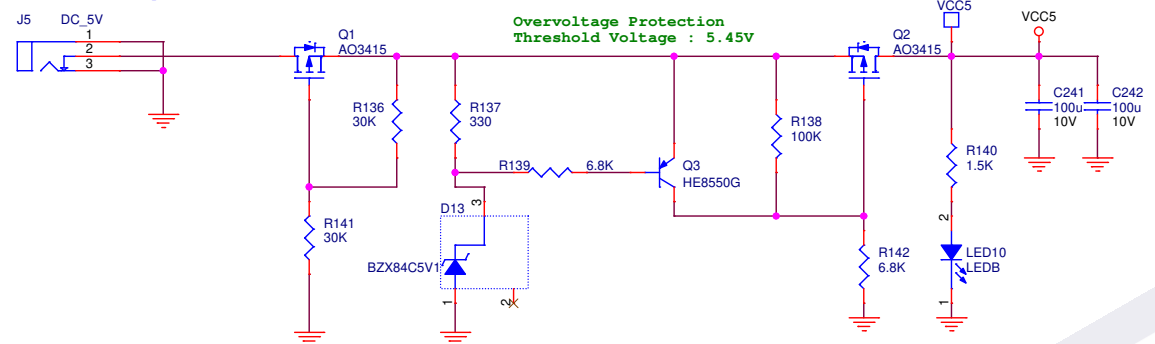


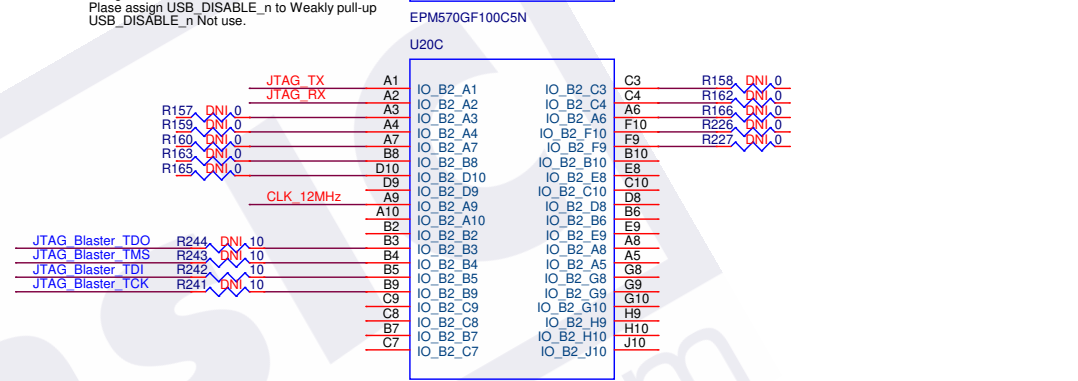
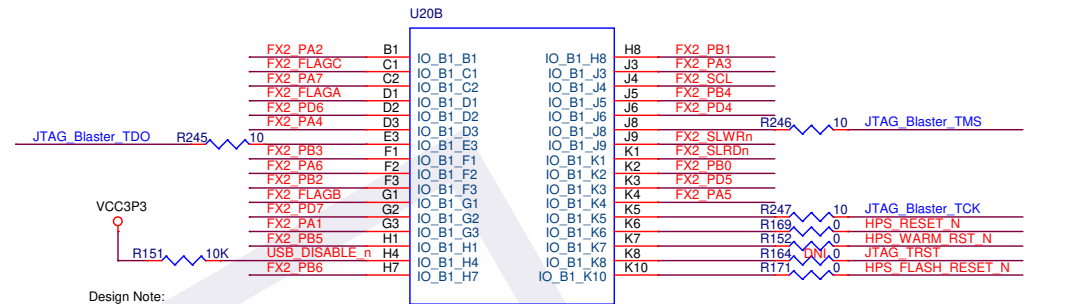
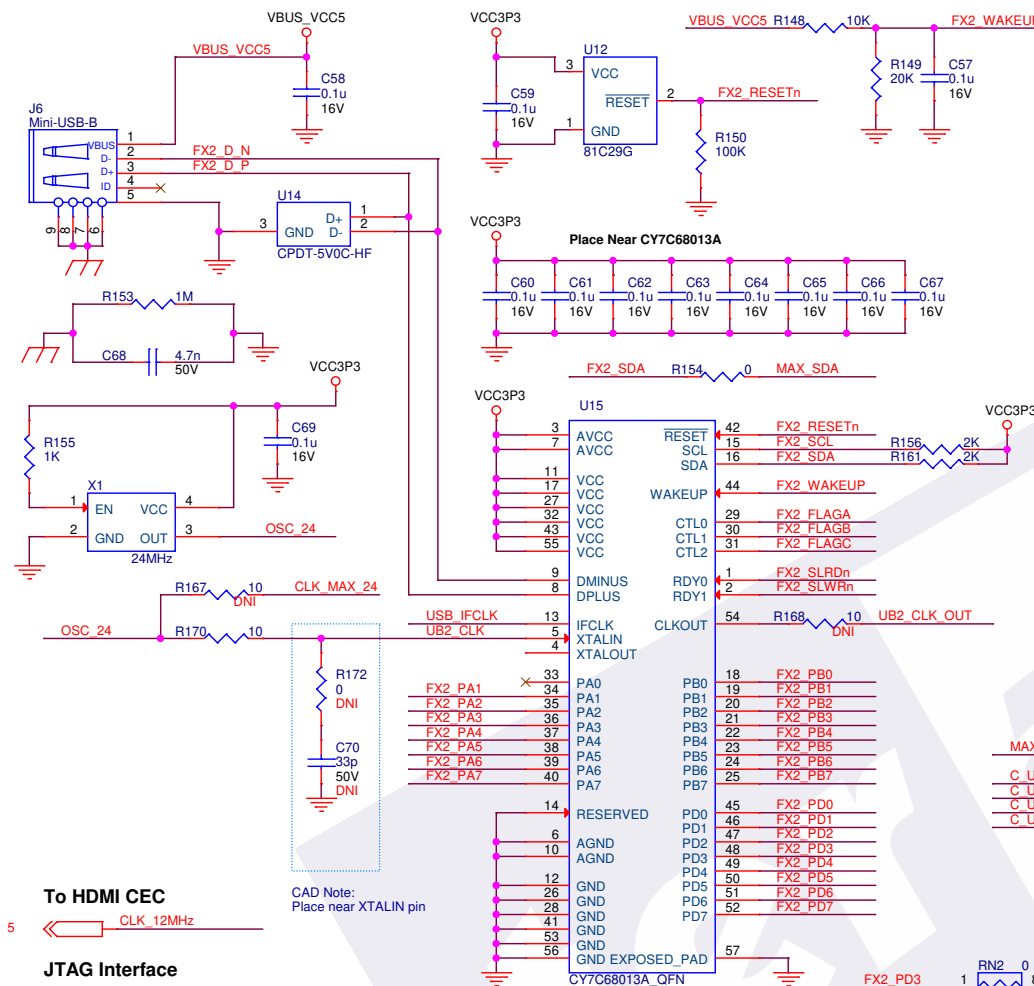
### HPS GPIO Header for RPI



RPI pin 27~40 is don't use



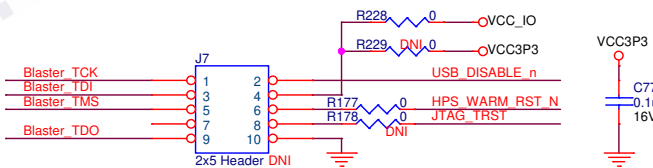




- To HDMI CEC**
- CLK 12MHz
- JTAG Interface**
- JTAG Blaster TCK
  - JTAG Blaster TMS
  - JTAG Blaster TDO
  - JTAG Blaster TDI
  - JTAG TRST
- HPS Reset**
- HPS\_WARM\_RST\_N
  - HPS\_RESET\_N
  - HPS\_FLASH\_RESET\_N

CAD Note:  
Place near XTALIN pin

**USB Blaster Programming Header**  
Default for FPGA/HPS JTAG Chain



terasic

Copyright (c) 2016 by Terasic Inc. Taiwan.  
All rights reserved.  
No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.

**Cyclone V - SoM Base Board**

Size B Document Number USB Blaster II Rev B0

Date: Tuesday, July 16, 2019 Sheet 10 of 10