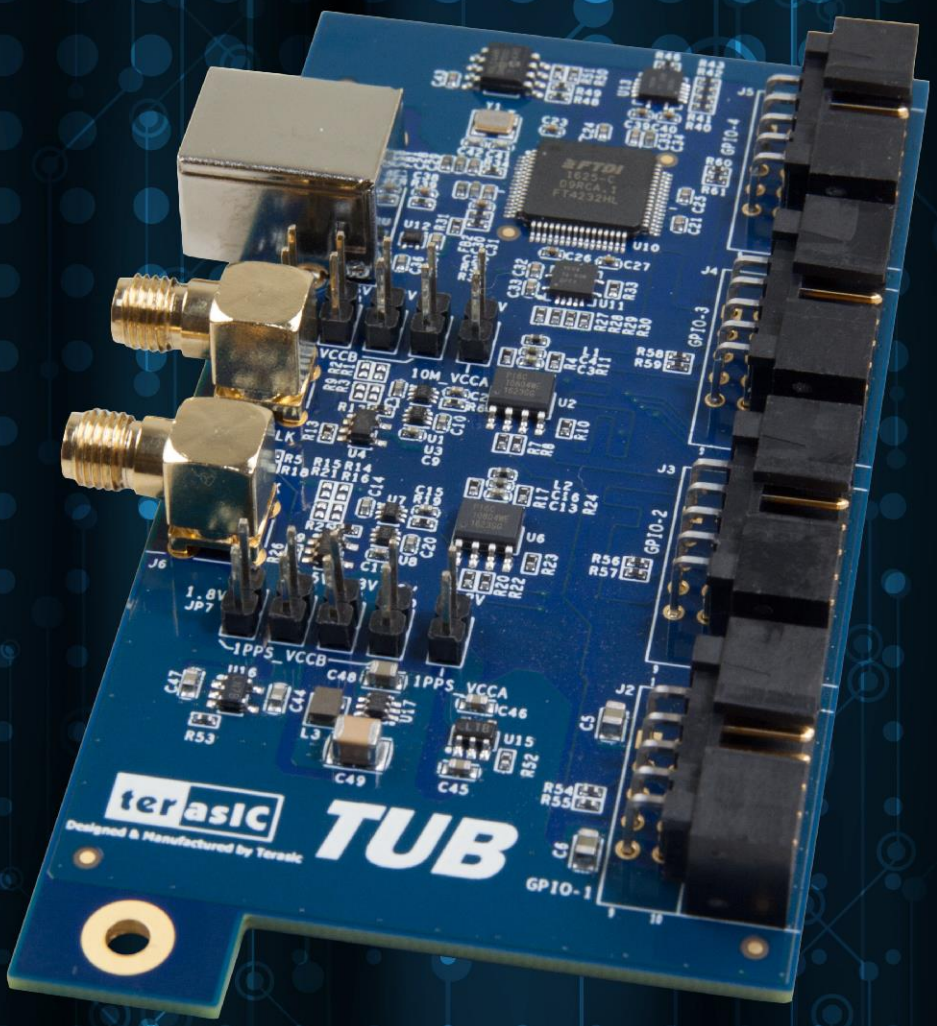
TUB

UserManual



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CONTENTS

Chapter 1

Timing and UART Board

The Timing and UART board (TUB) provides two channels of clock transfer function and one 1 to 4 USB to UART function. These two identical channels of clock transfer circuits support clock input signals with 1.2, 1.8, 2.5, 3.3 and 5 V voltage levels. By soldering divider resistors, these two clock transfer channels also support zero bias clocks with 1.2, 1.8, 2.5, 3.3 and 5 Vpp. Each clock transfer channel provides four clock fan-outs for four DE5a-Net boards through the 2x5 cable. The 1 to 4 USB to UART circuit provides users to communicate with four DE5a-Net boards.

1.1 Package Contents

Figure 1-1 shows a photograph of the TUB package.

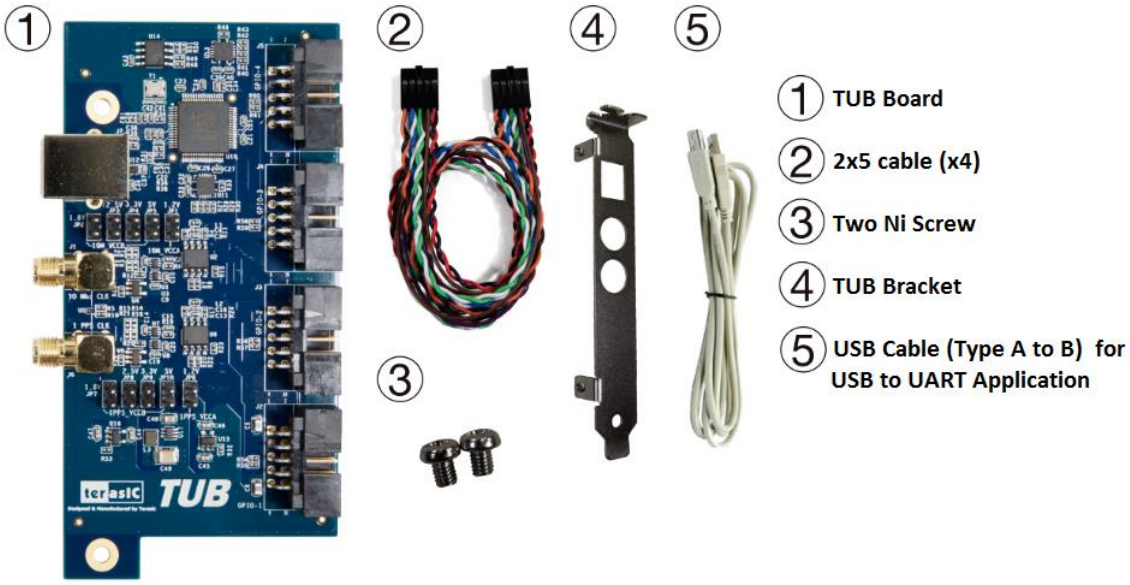

Figure 1-1 The TUB package contents

The TUB package includes:

- The TUB board
- 2x5 cable (x4)
- Two Ni Screw (Installed)
- TUB Bracket (Installed)
- USB cable (Type A to B) for USB to UART application

1.2 Getting Help

Here are the addresses where you can get help if you encounter any problems:

- Terasic Technologies
- 9F., No.176, Sec.2, Gongdao 5th Rd, East Dist, Hsinchu City, 30070. Taiwan

Email: support@terasic.com

Tel.: +886-3-575-088()

Chapter 2

Introduction of the TUB Board

This chapter provides an introduction to the features and design characteristics of the board.

2.1 Layout and Components

Figure 2-1 shows a photograph of the board. It depicts the layout of the board and indicates the location of the connectors and key components.

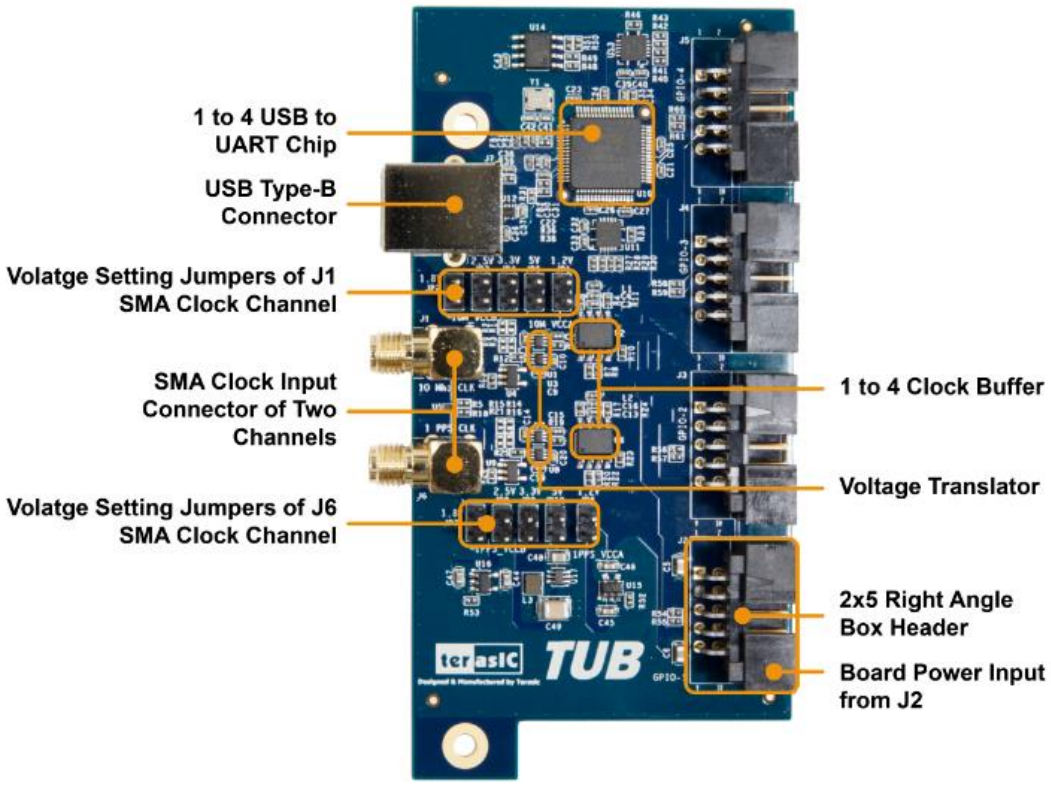

Figure 2-1 TUB board (top view)

Figure 2-2 TUB board (bottom view)

2.2 Block Diagram of the TUB Board

Figure 2-3 is the block diagram of the board.

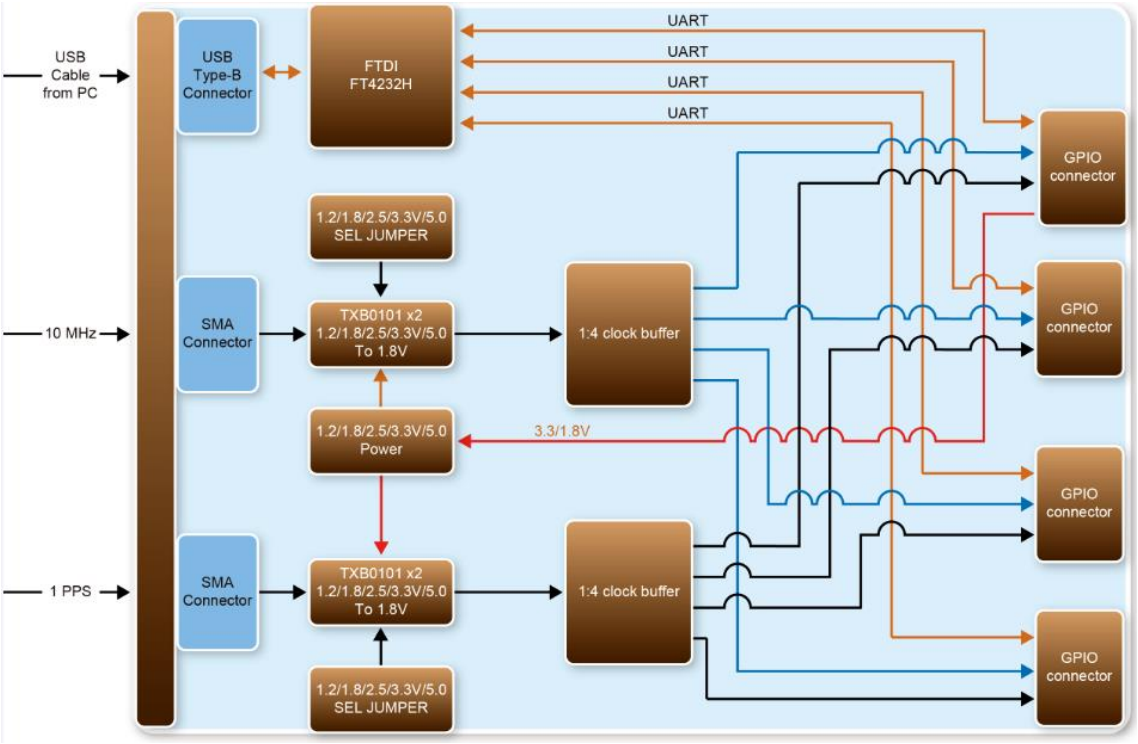

Figure 2-3 Block diagram of TUB

Detailed information about **Figure 2-3** are listed below.

Clock Transfer Circuits

- Two SMA connectors
- Four voltage translate chips (TXB0101)
- Two clock buffer (PI6C10804WE)
- Four 2x5 right angle box header
- Ten Jumpers

1 to 4 USB to UART Circuits

- One USB Type-B connector
- 1 to 4 USB to UART chip (FT4232H)
- 2-pin UART

Chapter 3

Using the TUB Board

This chapter provides an instruction to use the board. **The power of TUB is provided from J2 2x5 header, please keep in mind to connect TUB J2 header and DE5a-Net board with a 2x5 cable at all times (connection shown in section 3.6)**. Before using the TUB board, user have to make sure input clock format and then set correct jumpers setting for different clock formats.

3.1 Settings for Octoclock Distribution Module (Default)

10MHz clock

The 10MHz clock output from the Octoclock module is zero DC bias clock, as shown in **Figure 3-1**

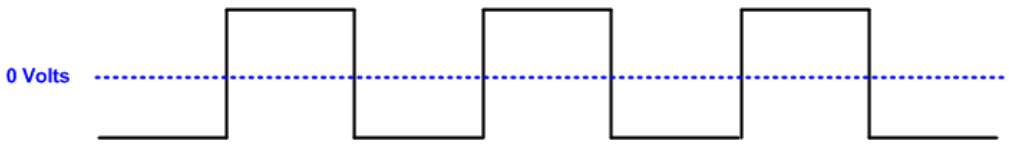

Figure 3-1 Clock signal with zero DC bias

First, make sure the pin 1 and pin 2 of JP11 are shorted with a jumper, the pin 5 and pin 6 of JP11 are shorted with a jumper. It will create a 1.65V DC bias incorporating into the input clock, and then the input clock will become a normal clock with 1.65V DC bias. The JP11 position is shown as **Figure 3-2**.

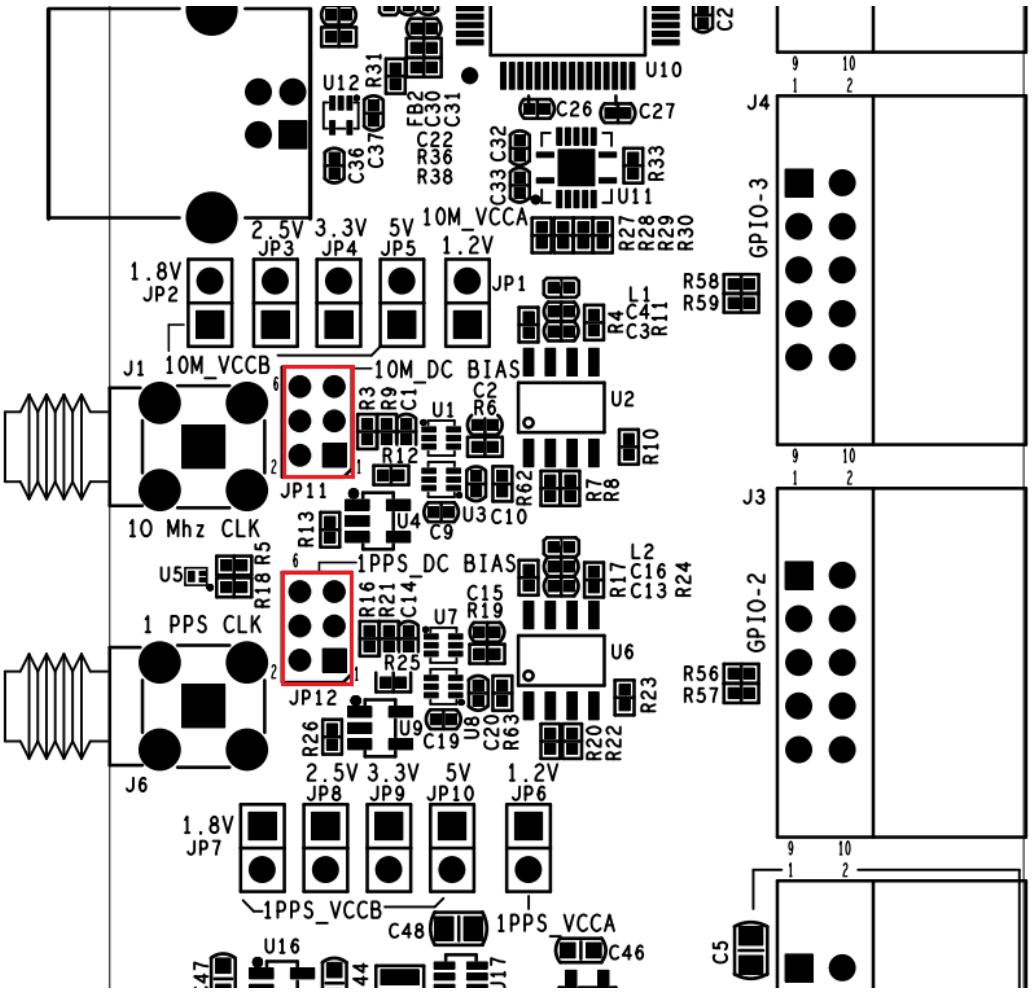

Figure 3-2 DC bias header positions

Second, a jumper has to be inserted on JP4 header. **All of JP1 ~ JP5 headers, only one header can be inserted with jumper at the same time.** Now, 10MHz clock from Octoclock module can be connected to J1 SMA connector.

1PPS Clock

The 1PPS clock output from Octoclock module is a 0 ~ 5V clock signal.

Make sure the pin 1 and pin 2 of JP12 are not shorted, the pin 3 and pin 4 of JP12 are shorted with a jumper. A jumper has to be inserted on JP10 header. **All of JP6 ~ JP10 headers, only one header can be inserted with jumper at the same time.** Now, 1PPS clock from Octoclock module can be connected to J6 SMA connector. The JP12 position is shown as **Figure 3-2**

3.2 Settings for Normal clock inputs (with DC bias)

If the input clock is a normal clock with DC bias, as shown in **Figure 3-3.**

Figure 3-3 Normal Clock signal with DC bias

First, make sure the pin 1 and pin 2 of JP11 are not shorted, the pin 1 and pin 2 of JP12 are not shorted. The positions of JP11 and JP12 are shown as **Figure 3-2**.

The following steps are the settings for clock signals with 1.2, 1.8, 2.5, 3.3 and 5V voltage levels.

1. Clock signal with 1.2V voltage level:

   For J1 SMA channel, JP1 header has to be inserted with jumper.

   For J6 SMA channel, JP6 header has to be inserted with jumper.

2. Clock signal with 1.8V voltage level:

   For J1 SMA channel, JP2 header has to be inserted with jumper.

   For J6 SMA channel, JP7 header has to be inserted with jumper.

3. Clock signal with 2.5V voltage level:

   For J1 SMA channel, JP3 header has to be inserted with jumper.

   For J6 SMA channel, JP8 header has to be inserted with jumper.

4. Clock signal with 3.3V voltage level:

   For J1 SMA channel, JP4 header has to be inserted with jumper.

   For J6 SMA channel, JP9 header has to be inserted with jumper.

5. Clock signal with 5V voltage level:

   For J1 SMA channel, JP5 header has to be inserted with jumper.

   For J6 SMA channel, JP10 header has to be inserted with jumper.

3.3 Settings for clock inputs with zero DC bias

If the clock input is a zero DC bias clock, as shown in **Figure 3-1**. At first, users have to make sure the values of Vpp

The following steps are the settings for zero DC bias clock signals with 1.2, 1.8, 2.5, 3.3 and 5V Vpp.

1. Zero DC bias clock signal with 1.2 Vpp:

   For J1 SMA channel, make sure the pin 1 and pin 2 of JP11 are shorted with a jumper, the pin 3 and pin 4 of JP11 are shorted with a jumper, JP1 header has to be inserted with jumper.

   For J6 SMA channel, make sure the pin 1 and pin 2 of JP12 are shorted with a jumper, the pin 3 and pin 4 of JP12 are shorted with a jumper, JP6 header has to be inserted with jumper.

2. Zero DC bias clock signal with 1.8 Vpp:

   For J1 SMA channel, make sure the pin 1 and pin 2 of JP11 are shorted with a jumper, the pin 5 and pin 6 of JP11 are shorted with a jumper, JP2 header has to be inserted with jumper.

   For J6 SMA channel, make sure the pin 1 and pin 2 of JP12 are shorted with a jumper, the pin 5 and pin 6 of JP12 are shorted with a jumper, JP7 header has to be inserted with jumper.

3. Zero DC bias clock signal with 2.5 Vpp:

   For J1 SMA channel, make sure the pin 1 and pin 2 of JP11 are shorted with a jumper, the pin 5 and pin 6 of JP11 are shorted with a jumper, JP3 header has to be inserted with jumper.

   For J6 SMA channel, make sure the pin 1 and pin 2 of JP12 are shorted with a jumper, the pin 5 and pin 6 of JP12 are shorted with a jumper, JP8 header has to be inserted with jumper.

4. Zero DC bias clock signal with 3.3 Vpp:

   For J1 SMA channel, make sure the pin 1 and pin 2 of JP11 are shorted with a jumper, the pin 5 and pin 6 of JP11 are shorted with a jumper, JP4 header has to be inserted with jumper.

   For J6 SMA channel, make sure the pin 1 and pin 2 of JP12 are shorted with a jumper, the pin 5 and pin 6 of JP12 are shorted with a jumper, JP9 header has to be inserted with jumper.

5. Zero DC bias clock signal with 5 Vpp:

   For J1 SMA channel, make sure the pin 1 and pin 2 of JP11 are shorted with a jumper, the pin 5

and pin 6 of JP11 are shorted with a jumper, JP5 header has to be inserted with jumper.

For J6 SMA channel, make sure the pin 1 and pin 2 of JP12 are shorted with a jumper, the pin 5 and pin 6 of JP12 are shorted with a jumper, JP10 header has to be inserted with jumper.

3.4 Jumpers Setting Table

Users can clearly implement the jumpers setting with different clock inputs from **Table 3-1.**

Table 3-1 Jumper Setting Table

Clock Inputs		JP11-1&2	JP11-3&4	JP11-5&6	JP12-1&2	JP12-3&4	JP12-5&6	JP1	JP2	JP3	JP4	JP5	JP6	JP7	JP8	JP9	JP10
OctoClock	J1 ch(10/MHz)	short		short							short						
	J6 ch(1PPS)					short											short
Normal Clocks (With DC bias, 0~Vpp)	J1 ch (1.2V)							short									
	J1 ch (1.8V)								short								
	J1 ch (2.5V)									short							
	J1 ch (3.3V)										short						
	J1 ch (5V)											short					
	J6 ch (1.2V)												short				
	J6 ch (1.8V)													short			
	J6 ch (2.5V)														short		
	J6 ch (3.3V)															short	
	J6 ch (5V)																short
No DC bias Clocks (+-0.5 Vpp)	J1 ch (Vpp:1.2V)	short	short					short									
	J1 ch (Vpp:1.8V)	short		short					short								
	J1 ch (Vpp:2.5V)	short		short						short							
	J1 ch (Vpp:3.3V)	short		short							short						
	J1 ch (Vpp:5V)	short		short								short					
	J6 ch (Vpp:1.2V)				short	short							short				
	J6 ch (Vpp:1.8V)				short		short							short			
	J6 ch (Vpp:2.5V)				short		short								short		
	J6 ch (Vpp:3.3V)				short		short									short	
	J6 ch (Vpp:5V)				short		short										short

3.5 USB to UART

The board has one 1 to 4 USB to UART interface for communication with four DE5a-Net boards. The physical interface is implemented by UART-USB onboard bridge from a FT4232H chip to the host with an USB B-type connector. More information about the chip is available on the manufacturer's website. Users can find the drivers for the USB-serial adapter from http://www.ftdichip.com/Drivers/VCP.htm.

3.6 Connecting DE5a-Net with 2x5 Cable

When connecting TUB and DE5a-Net board, there is a foolproof design on TUB 2x5 Box header

but not on DE5a-Net 2x5 header. Connecting 2x5 RS422 header of DE5a-Net with 2x5 cable, please follow the below steps:

1. Make sure the pin 1 position of J1 RS422 header on DE5a-Net board, as shown in **Figure 3-4**.

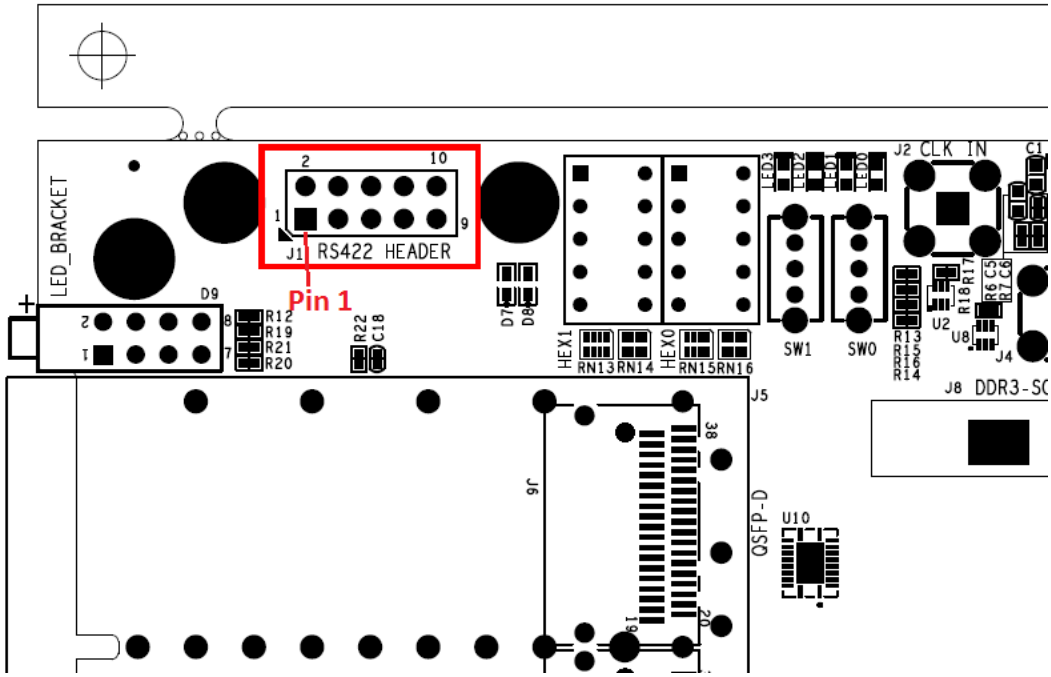

Figure 3-4 Location of RS422 header (J1) on DE5a-Net board

2. Make sure the pin 1 position of 2x5 cable, as shown in **Figure 3-5**.

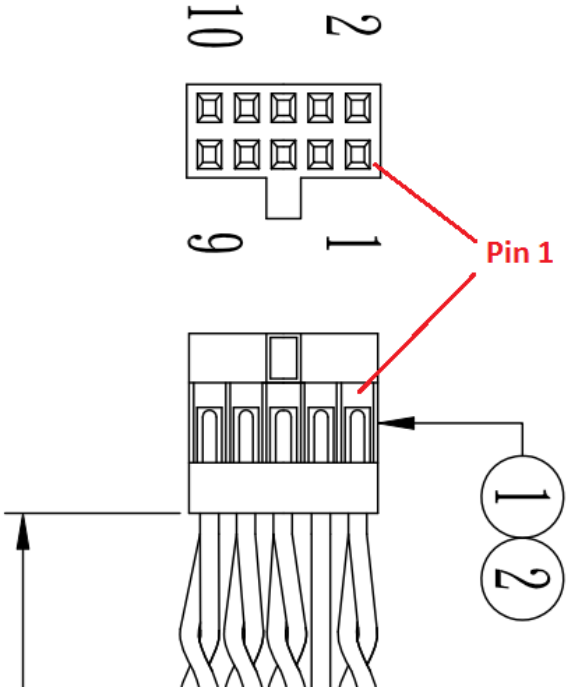

Figure 3-5 Pin 1 location of 2x5 cable

3. Follow the inserting direction of 2x5 cable, as shown in **Figure 3-6**.

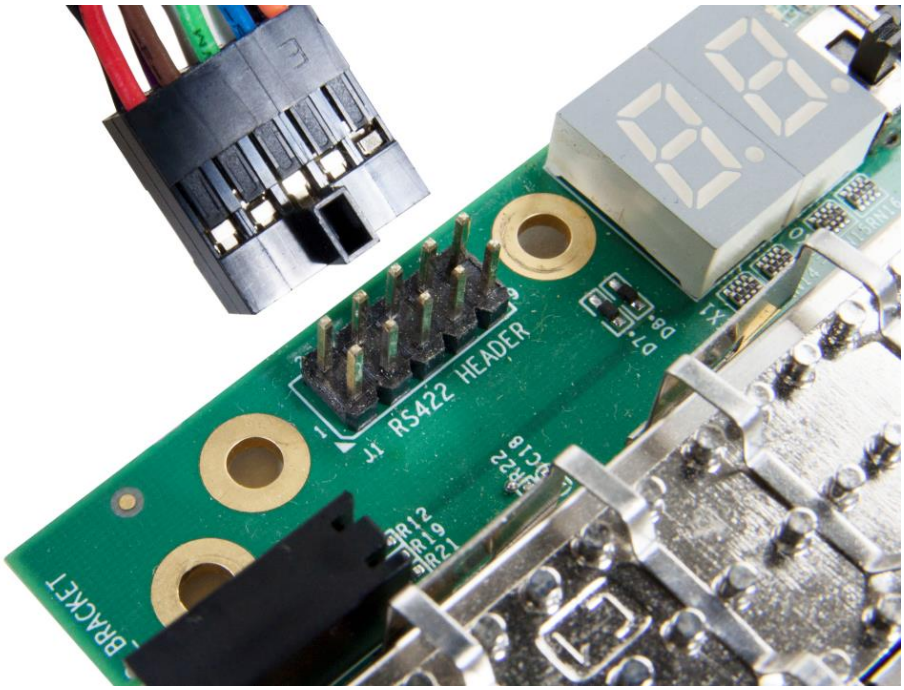

Figure 3-6 Inserting direction of 2x5 cable

4. Make sure the finial connection between 2x5 cable and DE5a-Net board as shown in **Figure 3-7**.

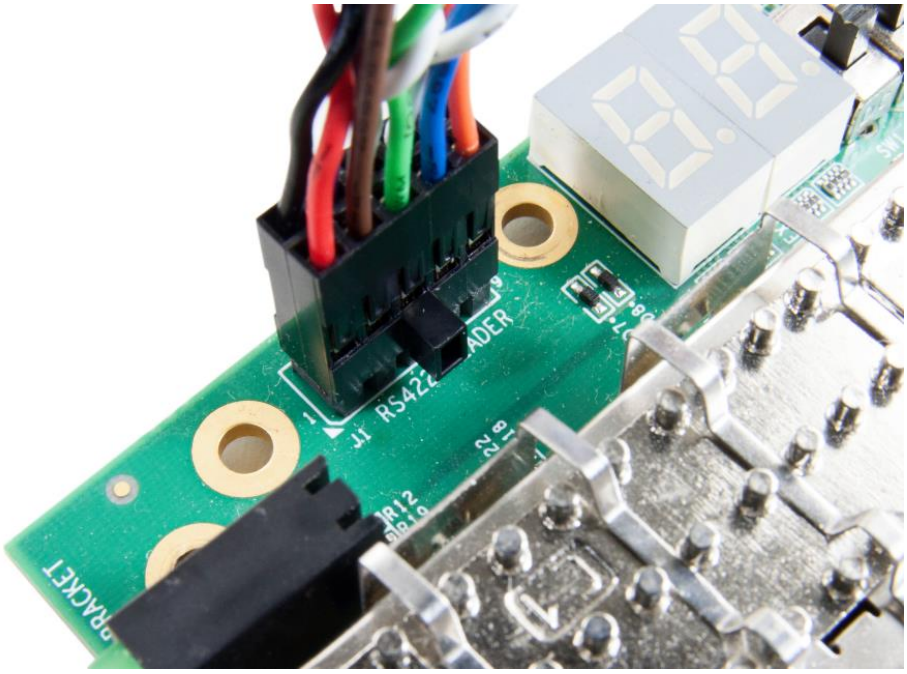

Figure 3-7 Finial connection between 2x5 cable and DE5a-Net board

Chapter 4

Test Code

This chapter describe how to use the test code, included in SYSTEM-CD, to verify the TUB board. There are two test code include in this kit. TUB_CLK_VERIFY board is designed to verify 1PPS and 10MHz clock. The TUB_UART_PPS10MHz is designed to test clock and UART. It will report the 10MHz counter to the UART port.

4.1 TUB_CLK_VERIFY

This code is designed to verify the 1PPS and 100MHz clock. The functions includes:

- **1 PPS LED**: Pulse LED0 when the 1 PPS clock goes high.
- **Count 10 MHz**: Count 10 MHz clock between two 1 PPS clock goes high
- **SMA Output**: Rout 1PPS or 10MHz to SMA output

■ Setup the Test

Figure 4-1 shows the screenshot of the demo setup. Here are the step by step procedure to perform the test:

1. Make sure your Host PC had Quartus Prime 16.1 installed.
2. Make sure the USB-Blaster II driver is installed on your Host PC.
3. Power off the DE5a-NET board.
4. Connect DE5a-NET and your Host PC USB port with an USB cable. (see Figure 4-1)
5. Connect TUB GPIO-1(J2) port and DE5a-NET with the 2x5 Cable came with this kit. (see Figure 4-1)
6. Provide 1PPS and 10MHz clock to TUB. (see Figure 4-1)
7. Power on the DE5a-NET.
8. Execute test.bat on the folder System-CD/TUB_CLK_VERIFY/demo_batch
9. Your will see the LED0 blink every 1 second.
10. Your will see the LED3/2/1 = unlight/light/light.
11. The SMA-Out will output 1 PPS or 10Mhz clock

12. Press CPU_RST button on DE5a-NET will reset the test code. When CPU_RST is pressed, LED3/2/1/0 will be turn on. When CPU_RST is release, the test code start to fucntion.

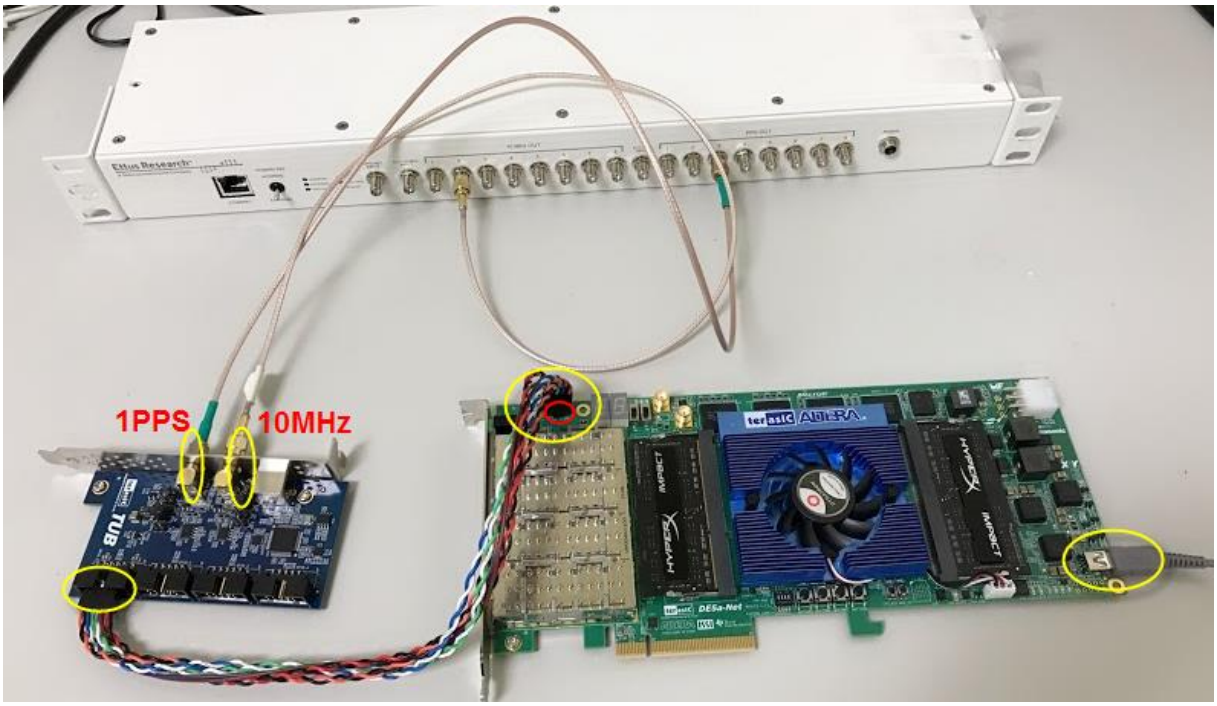

Figure 4-1 Setup TUB_CLK_VERIFY Demo

■ Function: 1 PPS LED Heartbeat

The **LED0** on DE5a-NET is turn on when 1 PPS clock goes high. At the same time, a counter with 10MHz clock is started to count. When counter reach count 5,000,000, the LED0 is turn off. The 10MHz clock is generated from a FPG internal PLL which use the 10MHz reference clock from TUB board. **Figure 4-2** shows the shows the block diagram of this function. The Rising Edge Detector is used to generate a sync reset pulse for the counter. If 1PPS or 10MHz clock is missed, the led will be untighten.

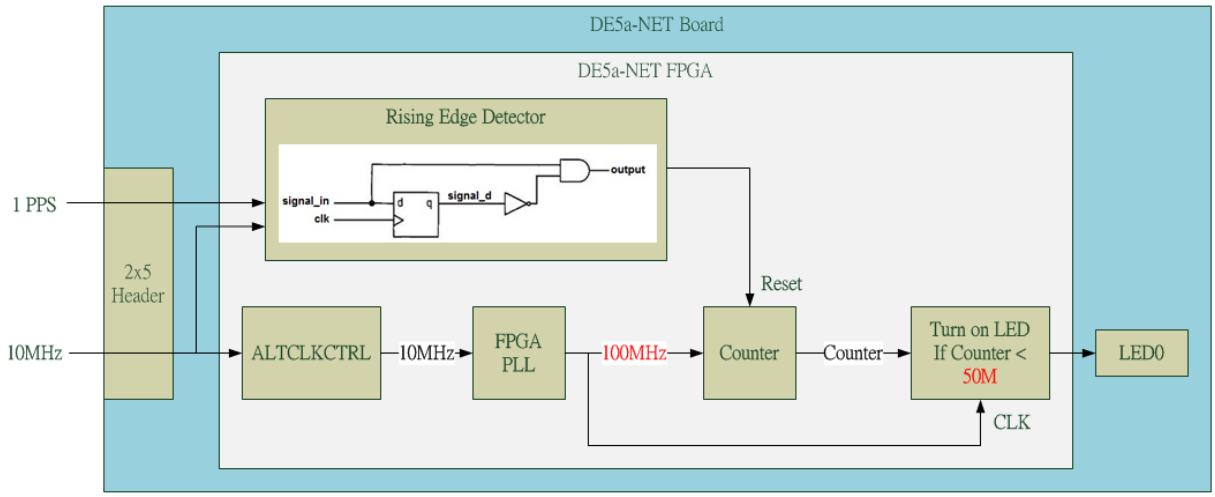

Figure 4-2 Block Diagram of 1 PPS LED

■ Function: Count 10 MHz

Count 10 MHz clock between two 1 PPS clock goes high, and show the count result in LED 3/2/1 three LED. **Figure 4-3** shows the block diagram of this function. The LED indication information is shown in table below. The 1 PPS and 10 MHz clock source should be ready before running this function. If the Counter result is not equal to 10,000,000, the LED state will be kept until users press CPU_RESET button to restart the counting function.

Counter	LED3	LED2	LED1
< 9,999,999	ON	OFF	OFF
= 9,999,999	ON	ON	OFF
= 10,000,000	OFF	ON	OFF
= 10,000,001	OFF	ON	ON
>10,000,001	OFF	OFF	ON
1 PPS or 10MH missed	OFF	OFF	OFF

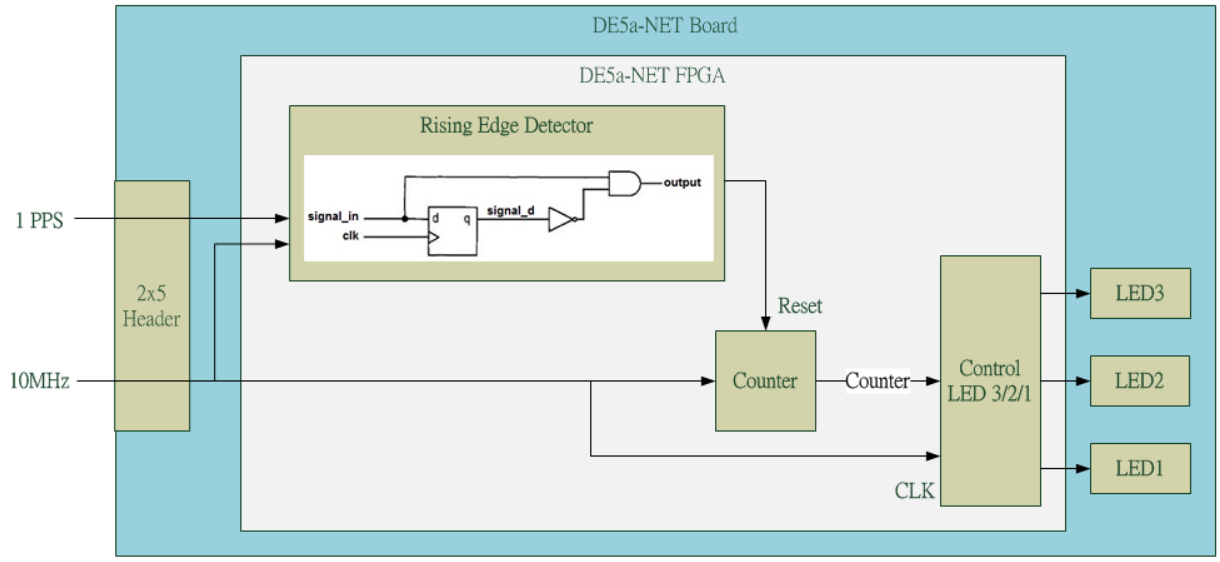

Figure 4-3 Block Diagram of 1 PPS LED Heartbeat

■ Function: SMA Output

The SMA output will internal loopback the 10MHz or 1 PPS clock. When SW0 is set to up positon, 1 PPS clock is loopback, otherwise, 10MHz clock is loopback. Figure 4-4 shows the block diagram of this function.

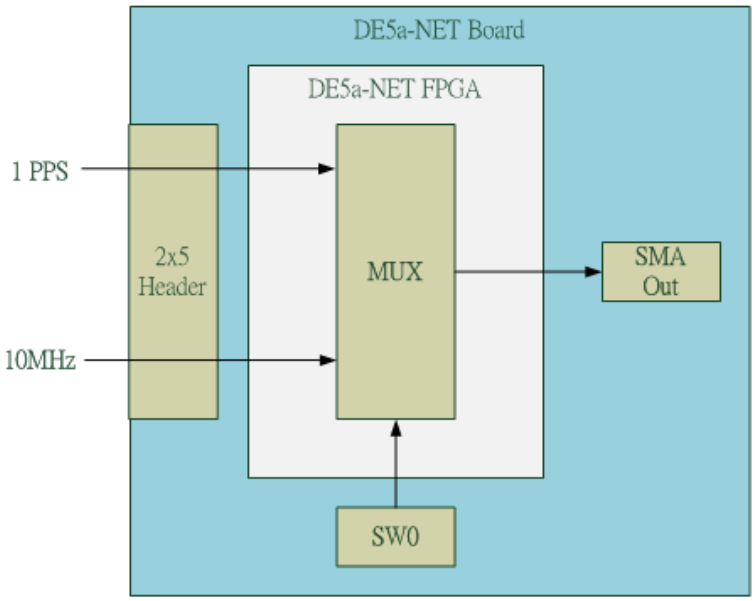

Figure 4-4 Block Diagram of 1 SMA Output

Quartus Project Information

- Tool: Quartus Prime 16.1.2 Standard Edition
- Project directory:

  Demonstrations\TUB_CLK_VERIFY
- Demo batch file folder:

  Demonstrations\TUB_CLK_VERIFY \demo_batch

4.2 TUB_UART_PPS10MHz

This project is coded in Verilog. Its purpose is for the testing of bundling TUB and DE5a-Net with E1 device. An external clock generator such as Octoclock CDA-2990 is required to generate 1PPS and 10MHz and outputs the clock signal into DE5a-Net via SMA connector. The accuracy of 1PPS/10MHz/1PPS vs. 10MHz can be tested by observing the LEDs and 7-segments on DE5a-Net. Alternatively, the test result can be uploaded to the host PC through UART. The following sections describe the setup of this project, as well as the instructions on how to execute the project on DE5a-Net.

Block Diagram

Figure 4-5 shows the function block diagram of this project.

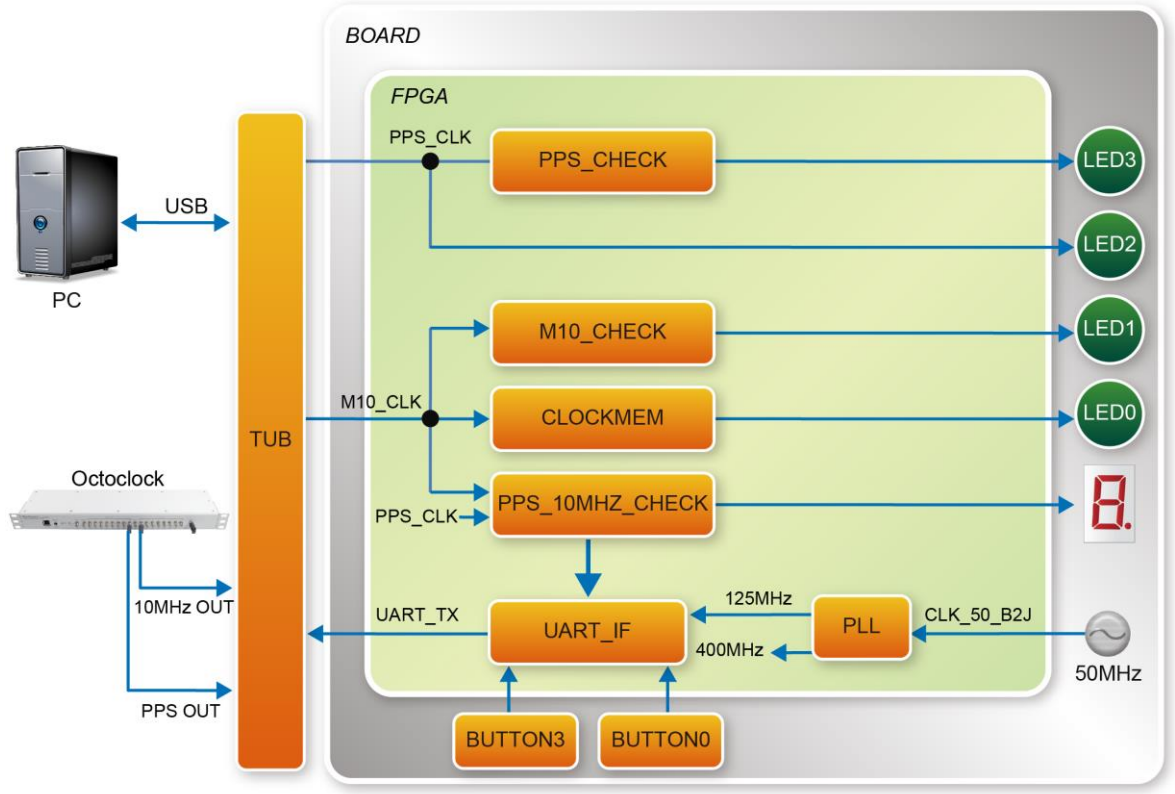

Figure 4-5 Function block diagram

PLL: This module generates 125MHz from the 50MHz oscillator onboard to the UART IP in UART_IF. It also generates 400MHz for the comparison with 10MHz and 1pps.

PPS_CHECK: This module compares the incoming 1pps signal with 400MHz generated from the PLL module. When the margin of error is below the threshold, the LED3 will lit. The 1pps signal is connected directly to the LED2 and it will flash in 1Hz.

M10_CHECK: This module compares the incoming 10MHz signal with 400MHz generated from the PLL module. When the margin of error is below the threshold, the LED1 will lit.

CLOCK_MEM: This module takes 10MHz signal and outputs 1Hz to the LED0 by dividing 10MHz.

PPS_10MHZ_CHECK: This module compares the incoming 1pps and 10MHz signals. The margin of error count will be displayed on the 7-segment. Alternatively, the count of 1 pps by 10MHz can be uploaded to the host PC through the UART IP.

UART_IF: This modules includes an Altera UART IP which is set to 115200 baud rate and its sequence controller, which can upload the result to the host PC.

This project can be realized on DE5a-Net. Please follow the steps below for running the demo on

the board.

Quartus Project Information

- Tool: Quartus Prime V16.0 Standard Edition
- Project directory:

  Demonstrations\TUB_UART_PPS10MHZ
- Demo batch file folder:

  Demonstrations\ TUB_UART_PPS10MHZ\demo_batch

Demonstration Setup for DE5a-Net

Please follow the procedures below to setup the demonstration, as shown in **Figure 4-6**.

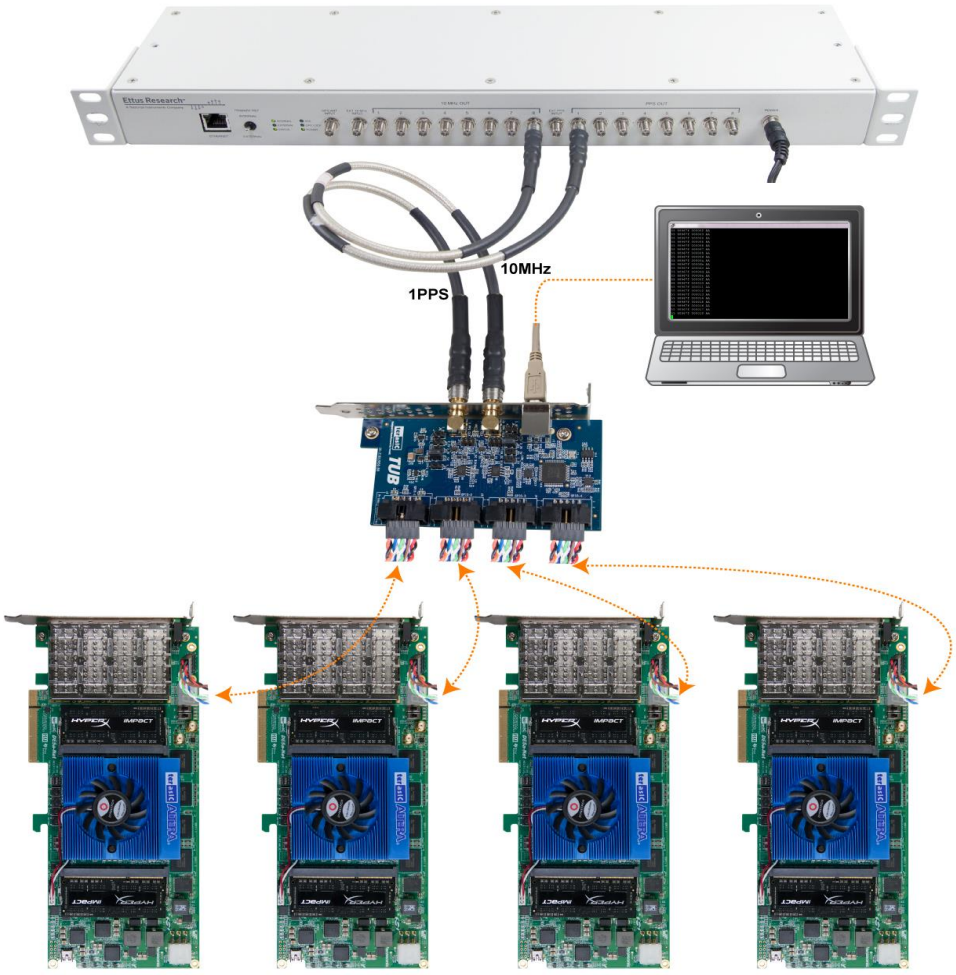

Figure 4-6 Hardware setup for the demo

1. Connect the RS422 expansion header 1 (J2) of TUB to the RS422 expansion header (J1) of DE5a-Net via a 10-pin cable included.
2. Connect 1 pps and 10MHz from the signal generator to the EXT CLOCK (J6) and EXT CLOCK (J1) via SMA cables, respectively. Connect the USB Type-B of TUB board to the host PC through an USB cable.
3. Plug in 12 V DC to DE2a-Net.
4. Connect the host PC to the USB connector (J14) on DE2a-Net via USB cable.
5. Please make sure Quartus II has been installed on the host PC.
6. Execute the batch file " test.bat" under the demo_batch folder of TUB_UART_PPS10MHZ project.
7. Both LED2 and LED0 flashing in 1Hz indicate the feed of 1pp and 10MHz from Ettus is ongoing.
8. Press BUTTON[0] once to reset the system.
9. When BUTTON[3] is pressed, LED1 and LED3 will lit. After 1 ~ 2 seconds, if LED1 and/or LED3 doesn't lit, it indicates 1 pps and/or 10MHz are abnormal, respectively, as shown in **Table 4-1**.

Table 4-1 The Status of LED0~3 after Pressing BUTTON[3]

Corresponding Item	Description	Status
10MHz	LED[0] flashes in 1Hz and LED[1] keeps ON	10MHz is normal
10MHz	LED[0] flashes in 1Hz and LED[1] is lit then dim	10MHz is entered but the frequency is not right
10MHz	LED[0] doesn't flash and LED[1] is lit then dim	10MHz is not entered
1 pps	LED[2] flashes in 1Hz and LED[3] keeps ON	1 pps is normal
1 pps	LED[2] flashes in 1Hz and LED[3] is lit then dim	1 pps is entered but the frequency is not right
1 pps	LED[2] doesn't flash and LED[3] is lit then dim	1 pps is not entered

10. The two 7-segments on DE5a-Net show the margin of error count between 1 pps and 10MHz.
11. The count of 1 pps by 10MHz can be uploaded to the host PC through PuTTY. The COM port needs to set to 115200 baud rate. **Figure 4-7** shows the count of 1 pps by 10MHz in the terminal window of PuTTY. The format 55 xxxxxx yyyyyy AA can be broken into 55 AA as the identification code for the beginning and the end; xxxxxx is the count value of 10MHz for 1 pps in hexadecimal ; yyyyyy represents the current time in second in hexadecimal.

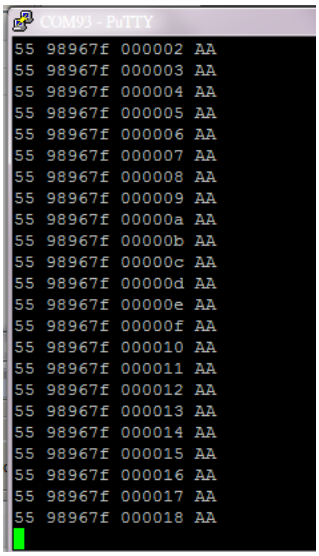

Figure 4-7 Terminal display on PuTTY

Chapter 5

Appendix

5.1 Revision History

Version	*Change Log*
V1.0.0	Initial Version (Preliminary)
V1.1.0	Add Example Designs
V1.1.1	Page 7:0.6V DC bias → 1.65V DC bias Table 3-1: OctoClock J6 ch(1PPS)→ short JP12-3&4

5.2 Jumpers Setting for Rev A

Clock Inputs		R1	R2	R3	R9	R14	R15	R16	R21	JP1	JP2	JP3	JP4	JP5	JP6	JP7	JP8	JP9	JP10
OctoClock	J1 ch(10/MHz)	Insert		Insert	Insert					short									
	J6 ch(1PPS)																		short
Normal Clocks (With DC bias, 0~Vpp)	J1 ch (1.2V)									short									
	J1 ch (1.8V)										short								
	J1 ch (2.5V)											short							
	J1 ch (3.3V)												short						
	J1 ch (5V)													short					
	J6 ch (1.2V)														short				
	J6 ch (1.8V)															short			
	J6 ch (2.5V)																short		
	J6 ch (3.3V)																	short	
	J6 ch (5V)																		short
No DC bias Clocks (+-0.5 Vpp)	J1 ch (Vpp:1.2V)	Insert		Insert	Insert					short									
	J1 ch (Vpp:1.8V)		Insert	Insert	Insert						short								
	J1 ch (Vpp:2.5V)		Insert	Insert	Insert							short							
	J1 ch (Vpp:3.3V)		Insert	Insert	Insert								short						
	J1 ch (Vpp:5V)		Insert	Insert	Insert									short					
	J6 ch (Vpp:1.2V)					Insert		Insert	Insert						short				
	J6 ch (Vpp:1.8V)						Insert	Insert	Insert							short			
	J6 ch (Vpp:2.5V)						Insert	Insert	Insert								short		
	J6 ch (Vpp:3.3V)						Insert	Insert	Insert									short	
	J6 ch (Vpp:5V)						Insert	Insert	Insert										short

Note: 1. R1/R2/R14/R15: 0 ohm
2. R3/R9/R16/R21: 100 ohm for VPP=1.2/1.8/2.5/3.3V clcok input (no DC bias)
3. R3/R9/R16/R21: 10K ohm for VPP=5V clock input (no DC bias)