CMOS Digital Integrated Circuit Silicon Monolithic

# TC358746AXBG/TC358748XBG
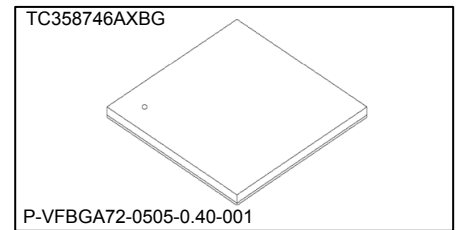
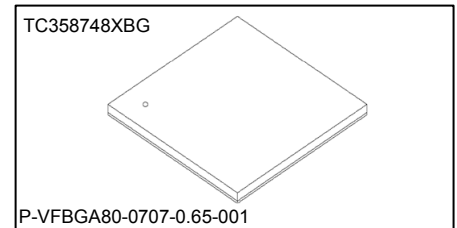**Mobile Peripheral Devices**

## Overview

The MIPI® CSI-2 to Parallel port and Parallel port to CSI-2 (TC358746AXBG/TC358748XBG) is a bridge device that converts MIPI data transfers from devices such as a camera to an application processor over a Parallel port interface. All internal registers can be access through I²C or SPI (in CSI out case only).

TC358746AXBG

P-VFBGA72-0505-0.40-001

Weight: 32.0 mg (Typ.)

TC358748XBG

P-VFBGA80-0707-0.65-001

Weight: 68.8 mg (Typ.)

## Features

● CSI-2 TX/RX Interface
  ✧ MIPI CSI-2 compliant (Version 1.01 Revision 0.04 – 2 April 2009)
  ✧ Configurable to TX or RX controller
  ✧ Supports up to 1Gbps per data lane
  ✧ Supports up to 4 data lanes
  ✧ Supports video data formats
  - RX: RAW8/10/12/14, YUV422 (CCIR/ITU 8/10-bit), RGB888/666/565 and User-Defined 8-bit
  - TX: YUV422 (CCIR/ITU 8/10-bit), YUV444, RGB888/666/565 and RAW8/10/12/14

● Parallel Port Interface
  ✧ Supports data formats
  - 24-bit bus – un-packed format (Both Input and Output mode)
    ➢ RGB888/666/565, RAW8/10/12/14 and YUV422 8-bit (on 8/16-bit data bus) and 10-bit data formats.
    ➢ YUV444 (Parallel Input mode only)
  - YUV422 8-bit – ITU BT.656 and ITU BT.601 (Parallel input mode only)
    ➢ Up to 100 MHz PCLK frequency for Output mode, and 166 MHz for Input mode.

● I²C Slave Interface (CS = L)
  ✧ Support for normal (100 kHz), fast mode (400 kHz) and special mode (1 MHz)
  ✧ Configure all TC358746AXBG/TC358748XBG internal registers

● SPI Slave Interface (Only applicable in CSIOut configuration, MSEL = H, and CS = H)
  ✧ SPI interface support for up to 25 MHz operation.
  ✧ Configure all TC358746AXBG/TC358748XBG internal registers

● GPIO signals
  ✧ 3 GPIO signals
  - Three GPIO signals can be configured as control signals (MCLK, CXRST, XShutdown) for CSI-2 RX device.
  - Or one GPIO signal can be configured as INT signal for Parallel interface.

● System
  ✧ Clock and power management support to achieve low power states.

● Power supply inputs
  ✧ Core and MIPI D-PHY: 1.2V
  ✧ I/O: 1.8V – 3.3V

2014-05-29

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**REFERENCES**

1. MIPI D-PHY, "MIPI_D-PHY_specification_v01-00-00, May 14, 2009"
2. MIPI CSI-2, "MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) Version 1.01 Revision   Nov 2010"
3. $I^2C$ bus specification, version 2.1, January 2000, Philips Semiconductor

2014-05-29

# 1. Overview

The MIPI CSI-2 to Parallel port and Parallel port to CSI-2 (TC358746AXBG/TC358748XBG) is a bridge device that converts MIPI data transfers from devices such as a camera to an application processor over a Parallel port interface. All internal registers can be access through I$^2$C or SPI (in CSI out case only).

There are several system configurations where TC358746AXBG/TC358748XBG are typically be used

- CSI-2 TX with Parallel Input mode for Analog TV, Tele-presence Type, and Specialty/Older Cameras application. In this mode, TC358746AXBG/TC358748XBG (Parallel to CSI-2 converter) is a bridge device that converts parallel data transfers to an application over a MIPI CSI-2 interface. Toshiba Bridge Chip provides a low power bridge solution to efficiently translate parallel transfers to serial transfers.
- CSI-2 RX with Parallel output mode for scanner application. In this mode, TC358746AXBG/TC358748XBG (CSI-2 to Parallel converter) is a bridge device that converts serial data transfers from devices such as a camera to an application processor over a parallel interface. Toshiba Bridge Chip provides a low power bridge solution to efficiently translate serial transfers to parallel transfers.



**Figure 1.1   System Overview with TC358746AXBG/TC358748XBG in CSI-2 RX to Parallel Port Configuration**

**I2C**

| Mobile Analog TV or Telepresence or Mobile Phone Specialty cams | Parallel Port 24-bit data (RAW, YUV, RGB) | TC358746AXBG Parallel Port To MIPI Converter | MIPI Link Quad Data Lanes | Application Processor Or Baseband |

Figure 1.2    System Overview with TC358746AXBG/TC358748XBG in Parallel Port to CSI-2 TX Configuration

# 2. Features

Below are the main features supported by TC358746AXBG/TC358748XBG.

- CSI-2 TX/RX Interface

    ◇ MIPI CSI-2 compliant (Version 1.01 Revision 0.04 – 2 April 2009)

    ◇ Configurable to TX or RX controller

    ◇ Supports up to 1Gbps per data lane

    ◇ Supports up to 4 data lanes

    ◇ Supports video data formats
        - RX: RAW8/10/12/14, YUV422 (CCIR/ITU 8/10-bit), RGB888/666/565 and User-Defined 8-bit
        - TX: YUV422 (CCIR/ITU 8/10-bit), YUV444, RGB888/666/565 and RAW8/10/12/14

- Parallel Port Interface

    ◇ Supports data formats
        - 24-bit bus – un-packed format (Both Input and Output mode)
        ➢ RGB888/666/565, RAW8/10/12/14 and YUV422 8-bit (on 8/16-bit data bus) and 10-bit data formats.
        ➢ YUV444 (Parallel Input mode only)
        - YUV422 8-bit – ITU BT.656 and ITU BT.601 (Parallel input mode only)

    ◇ Up to 100 MHz PCLK frequency for Output mode, and 166 MHz for Input mode.

- I$^2$C Slave Interface (CS = L)

    ◇ Support for normal (100 kHz), fast mode (400 kHz) and special mode (1 MHz)

    ◇ Configure all TC358746AXBG/TC358748XBG internal registers

- SPI Slave Interface (Only applicable in CSIOut configuration, MSEL = H, and CS = H)

    ◇ SPI interface support for up to 25 MHz operation.

    ◇ Configure all TC358746AXBG/TC358748XBG internal registers

- GPIO signals

    ◇ 3 GPIO signals
        - Three GPIO signals can be configured as control signals (MCLK, CXRST, XShutdown) for CSI-2 RX device.
        - Or one GPIO signal can be configured as INT signal for Parallel interface.

- System

    ◇ Clock and power management support to achieve low power states.

- Power supply inputs

    ◇ Core and MIPI D-PHY: 1.2V

    ◇ I/O: 1.8V – 3.3V

## 2.1. Typical Power Consumption

**Parallel_In → CSI_Out,** 500MHz CSICLk, 1080P @60fps

|  | VDDIO (3.3V) | VDDC (1.2V) | VDD_MIPI (1.2V) | Total Power |
|---|---|---|---|---|
| **Current (mA)** | 0.44 | 40.4 | 24.5 | |
| **Power (mW)** | 1.452 | 48.48 | 29.4 | 79.33 |

**CSI_In → Parallel_Out**, 500MHz CSICLk, 114MHz PClk ColorBar @60fps

|  | VDDIO (3.3V) | VDDC (1.2V) | VDD_MIPI (1.2V) | Total Power |
|---|---|---|---|---|
| **Current (mA)** | 18.9 | 13.9 | 12.3 | |
| **Power (mW)** | 62.37 | 16.68 | 14.76 | 93.81 |

# 3. External Pins

## 3.1. TC358746AXBG pinout description

TC358746AXBG/TC358748XBG resides in BGA pin packages. The following table gives the signals of TC358746AXBG/TC358748XBG and their function.

**Table 3.1   TC358746AXBG/ TC358748XBG Functional Signal List**

| Group | Pin Name | I/O | Type | Function | Note |
|---|---|---|---|---|---|
| System: Reset & Clock (4) | RESX | I | Sch | System reset input, active low | |
| | REFCLK | I | N | Reference clock input (6MHz – 40MHz) | |
| | MSEL | I | N | Mode Select<br>1'b0: CSI-2 RX in –> Par_out<br>1'b1: Par_in -> CSI-2 TX | |
| | CS | I | N | Chip Select, active low<br>MSEL= 0 (CSI-2 RX in –> Par_out)<br> - When CS = 0, chip selected<br>Normal operation<br> - When CS = 1, chip not selected<br>Cannot access to internal registers and optionally Parallel output ports can be tri-state when 0x0004[15] is set<br>MSEL= 1 (Par_in -> CSI-2 TX)<br>    -   CS = 0, I$^2$C I/F is selected<br>    -   CS = 1, SPI I/F is chosen | |
| MIPI-CSI (10) | MIPI_CP | | PHY | MIPI-CSI    clock positive | |
| | MIPI_CN | | PHY | MIPI-CSI    clock negative | |
| | MIPI_D0P | | PHY | MIPI-CSI    Data 0 positive | |
| | MIPI_D0N | | PHY | MIPI-CSI    Data 0 negative | |
| | MIPI_D1P | | PHY | MIPI-CSI    Data 1 positive | |
| | MIPI_D1N | | PHY | MIPI-CSI    Data 1 negative | |
| | MIPI_D2P | | PHY | MIPI-CSI    Data 2 positive | |
| | MIPI_D2N | | PHY | MIPI-CSI    Data 2 negative | |
| | MIPI_D3P | | PHY | MIPI-CSI    Data 3 positive | |
| | MIPI_D3N | | PHY | MIPI-CSI    Data 3 negative | |
| I2C I/F (2) | I2C_SCL | OD | Sch | I$^2$C serial clock or SPI_SCLK | 4mA |
| | I2C_SDA | OD | Sch | I$^2$C serial data or SPI_MOSI | 4mA |
| Parallel Port I/F (27) | PD[23:0] | I/O | N | Parallel Port Data<br>    - PD[23:12] can configs to be GPIO[15:4] | 4mA |
| | VSYNC | I/O | N | Parallel port   VSYNC signal | 4mA |
| | HSYNC | I/O | N | Parallel port   HSYNC signal<br>    - HSYNC will be use as "DE" | 4mA |
| | PCLK | I/O | N |  Parallel Port   Clock signal | 4mA |
| GPIO (3) | GPIO[2:0] | I/O | N | **GPIO[2:0] signals**<br>    CSI-2 RX in –> Par_out<br>    - (GPIO[0] option to become MCLK signal)<br>    - (GPIO[1] option to become CXRST or INT)<br>- (GPIO[2] option to become XShutdown)<br>    Par_in -> CSI-2 TX<br>    - (GPIO[1] option to become SPI_SS or INT)<br>- (GPIO[2] option to become SPI_MISO) | 4mA |
| POWER (9) | VDDC (1.2V) | NA | | VDD for Internal Core (2) | |
| | VDDIO (1.8V – 3.3V) | NA | | VDDIO is for IO power supply (3) | |
| | VDD_MIPI (1.2V) | NA | | VDD for the MIPI CSI2 (2) | |
| Ground NOTE1 | VSS | NA | | Ground | |

NOTE1 : TC358746AXBG=17, TC358748XBG=25

## 3.2. TC358746AXBG BGA72 pin Count Summary

**Table 3.2   TC358746AXBG BGA 72Pin Count Summary**

| Group Name | Pin Count | Notes |
|---|---|---|
| SYSTEM | 4 | |
| MIPI-CSI | 10 | |
| I2C I/F | 2 | |
| GPIO | 3 | |
| Parallel Port I/F | 27 | |
| POWER | 9 | IO, MIPI and Core Power |
| GROUND | 17 | |
| **TOTAL** | **72** | |

## 3.3. TC358748XBG BGA80 Pin Count Summary

**Table 3.3   TC358748XBG BGA 80 Pin Count Summary**

| Group Name | Pin Count | Notes |
|---|---|---|
| SYSTEM | 4 | |
| MIPI-CSI | 10 | |
| I2C I/F | 2 | |
| GPIO | 2 | |
| Parallel Port I/F | 28 | |
| POWER | 9 | IO, MIPI and Core Power |
| GROUND | 25 | |
| **TOTAL** | **80** | |

## 3.4. TC358746AXBG Pin Layout

| A1 | A2 | A3 | A4 | A5 | A6 | A7 | A8 | A9 |
|----|----|----|----|----|----|----|----|----|
| VSS | PD17 | PD19 | PD21 | PD23 | GPIO2 | I2C_SCL | MSEL | VSS |
| **B1** | **B2** | **B3** | **B4** | **B5** | **B6** | **B7** | **B8** | **B9** |
| VDDC | PD16 | PD18 | PD20 | PD22 | GPIO1 | I2C_SDA | RESX | VDDIO |
| **C1** | **C2** | **C3** | **C4** | **C5** | **C6** | **C7** | **C8** | **C9** |
| PD15 | PD14 | VSS | VSS | VSS | VSS | VDD_MIPI | MIPI_D3P | MIPI_D3N |
| **D1** | **D2** | **D3** | | | | **D7** | **D8** | **D9** |
| PD13 | PD12 | VSS | | | | VSS | MIPI_D2P | MIPI_D2N |
| **E1** | **E2** | **E3** | | | | **E7** | **E8** | **E9** |
| VSS | VSS | VDDC | | | | VDD_MIPI | MIPI_CP | MIPI_CN |
| **F1** | **F2** | **F3** | | | | **F7** | **F8** | **F9** |
| VSS | VSS | VSS | | | | VSS | MIPI_D1P | MIPI_D1N |
| **G1** | **G2** | **G3** | **G4** | **G5** | **G6** | **G7** | **G8** | **G9** |
| PD11 | PD10 | VDDIO | VSS | VSS | VDDIO | VDDIO | MIPI_D0P | MIPI_D0N |
| **H1** | **H2** | **H3** | **H4** | **H5** | **H6** | **H7** | **H8** | **H9** |
| VDDC | PD8 | PD6 | PD4 | PD2 | PD0 | PCLK | HSYNC | CS |
| **J1** | **J2** | **J3** | **J4** | **J5** | **J6** | **J7** | **J8** | **J9** |
| VSS | PD9 | PD7 | PD5 | PD3 | PD1 | REFCLK | VSYNC | GPIO0 |

**Figure 3.1   TC358746AXBG BGA72-Pin Layout (Top View)**

## 3.5. TC358748XBG Pin Layout

| A1 | A2 | A3 | A4 | A5 | A6 | A7 | A8 | A9 | A10 |
|---|---|---|---|---|---|---|---|---|---|
| VSS | PD17 | PD19 | PD21 | PD23 | GPIO2 | VDDC | I2C_SCL | MSEL | VSS |
| **B1** | **B2** | **B3** | **B4** | **B5** | **B6** | **B7** | **B8** | **B9** | **B10** |
| VDDC | PD16 | PD18 | PD20 | PD22 | GPIO1 | VSS | I2C_SDA | RESX | VDDIO |
| **C1** | **C2** | **C3** | **C4** | **C5** | **C6** | **C7** | **C8** | **C9** | **C10** |
| PD15 | PD14 | | | | | | | MIPI_D3P | MIPI_D3N |
| **D1** | **D2** | **D3** | **D4** | **D5** | **D6** | **D7** | **D8** | **D9** | **D10** |
| PD13 | PD12 | | VSS | VSS | VSS | VSS | | MIPI_D2P | MIPI_D2N |
| **E1** | **E2** | **E3** | **E4** | **E5** | **E6** | **E7** | **E8** | **E9** | **E10** |
| PD11 | PD10 | | VSS | VSS | VSS | VSS | | VSS | VDD_MIPI |
| **F1** | **F2** | **F3** | **F4** | **F5** | **F6** | **F7** | **F8** | **F9** | **F10** |
| PD9 | PD8 | | VSS | VSS | VSS | VSS | | MIPI_CP | MIPI_CN |
| **G1** | **G2** | **G3** | **G4** | **G5** | **G6** | **G7** | **G8** | **G9** | **G10** |
| PD7 | PD6 | | VSS | VSS | VSS | VSS | | MIPI_D1P | MIPI_D1N |
| **H1** | **H2** | **H3** | **H4** | **H5** | **H6** | **H7** | **H8** | **H9** | **H10** |
| VDDIO | VSS | | | | | | | VSS | VDD_MIPI |
| **J1** | **J2** | **J3** | **J4** | **J5** | **J6** | **J7** | **J8** | **J9** | **J10** |
| PD4 | PD2 | PD0 | VSS | VSS | PCLK | HSYNC | CS | MIPI_D0P | MIPI_D0N |
| **K1** | **K2** | **K3** | **K4** | **K5** | **K6** | **K7** | **K8** | **K9** | **K10** |
| PD5 | PD3 | PD1 | VDDC | VDDIO | REFCLK | VSYNC | GPIO0 | VDDIO | VSS |

**Figure 3.2    TC358748XBG 80-Pin Layout (Top View)**
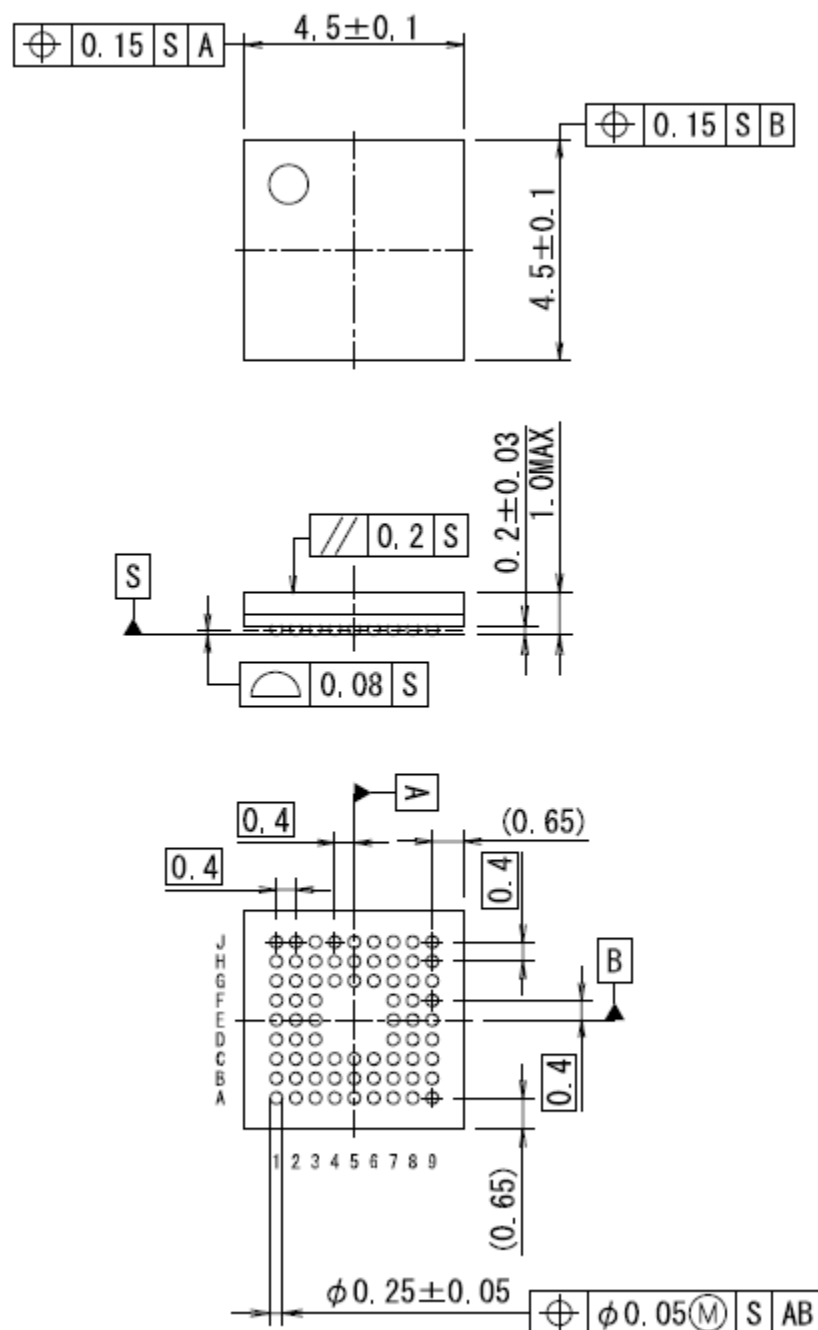
# 4. Package

## 4.1. TC358746AXBG Package

The packages for TC358746AXBG are described in the figures below.

P-VFBGA72-0505-0.40-001                                    "Unit;mm"



Weight: 32.0 mg (Typ.)

**Figure 4.1    TC358746AXBG P-VFBGA72-0505-0.40-001    package**

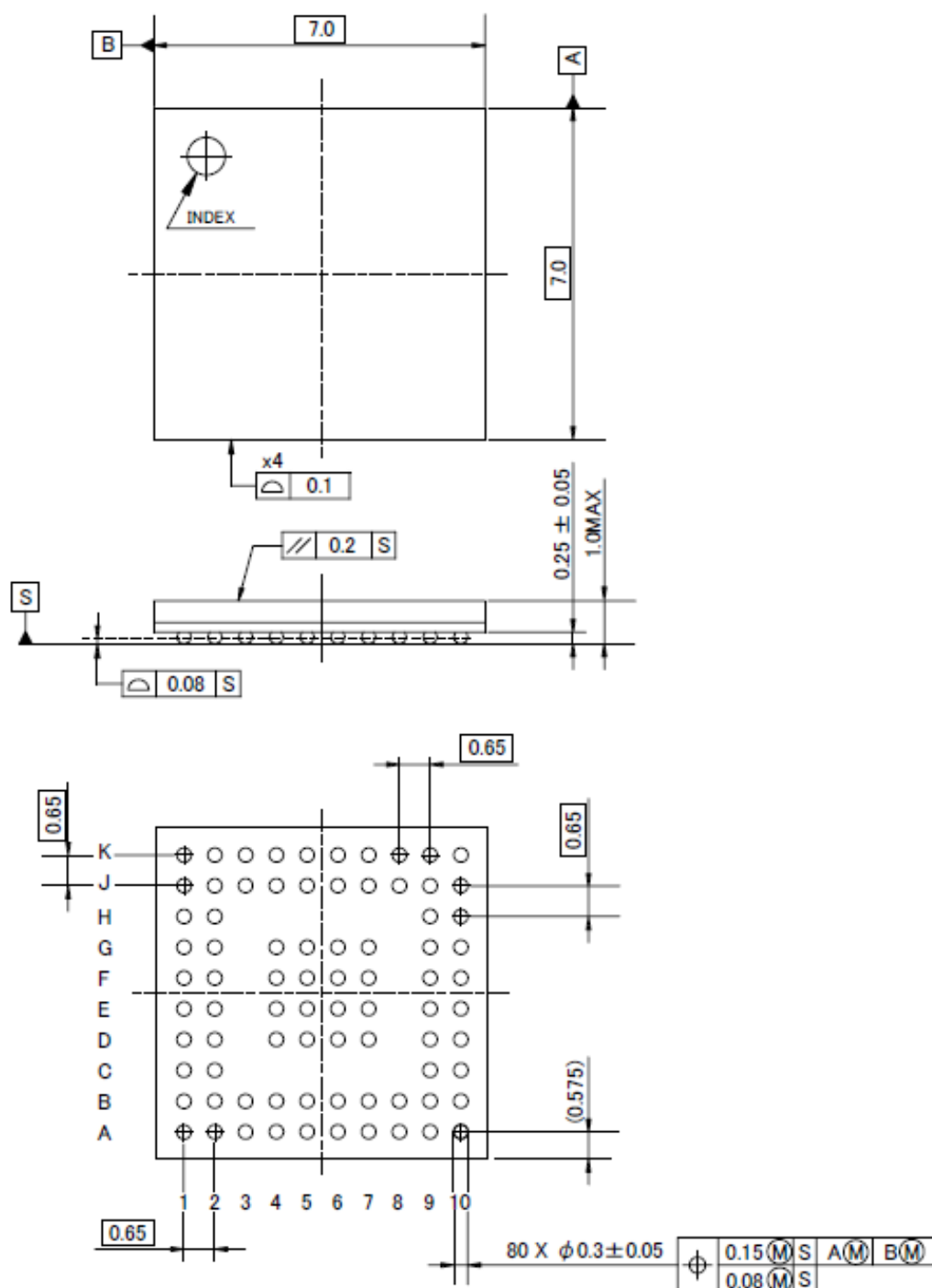**Table 4.1    TC358746AXBG P-VFBGA72-0505-0.40-001 Mechanical Dimension**

| Dimension | Min | Typ. | Max |
|---|---|---|---|
| Solder ball pitch | - | 0.4 mm | - |
| Solder ball height | 0.15 mm | 0.2 mm | 0.205 mm |
| Package dimension | - | 4.5 x 4.5 mm$^2$ | - |
| Package height | - | - | 1.0 mm |

## 4.2. TC358748XBG Package

The packages for TC358748XBG are described in the figures below.

P-VFBGA80-0707-0.65-001                                                    "Unit:mm"



Weight: 68.8 mg (Typ.)

**Figure 4.2    TC358748XBG P-VFBGA80-0707-0.65-001 package**

**Table 4.2    TC358748XBG P-VFBGA80-0707-0.65 Mechanical Dimension**

| Dimension | Min | Typ. | Max |
|---|---|---|---|
| Solder ball pitch | - | 0.65 mm | - |
| Solder ball height | 0.20 mm | 0.25 mm | 0.30 mm |
| Package dimension | - | $7.0 \times 7.0 \text{ mm}^2$ | - |
| Package height | - | - | 1.0 mm |

# 5. Electrical Characteristics

## 5.1. Absolute Maximum Ratings

VSS= 0V reference

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage (1.8V - Digital IO) | VDDIO | -0.3 to +3.9 | V |
| Supply voltage (1.2V – Digital Core) | VDDC | -0.3 to +1.8 | V |
| Supply voltage (1.2V – MIPI CSI PHY) | VDD_MIPI | -0.3 to +1.8 | V |
| Input voltage (CSI IO) | $V_{IN\_CSI}$ | -0.3 to VDD_MIPI+0.3 | V |
| Output voltage (CSI IO) | $V_{OUT\_CSI}$ | -0.3 to VDD_MIPI+0.3 | V |
| Input voltage (Digital IO) | $V_{IN\_IO}$ | -0.3 to VDDIO+0.3 | V |
| Output voltage (Digital IO) | $V_{OUT\_IO}$ | -0.3 to VDDIO+0.3 | V |
| Junction temperature | Tj | 125 | $^{o}$C |
| Storage temperature | Tstg | -40 to +125 | $^{o}$C |

## 5.2. Operating Condition

VSS= 0V reference

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Supply voltage (1.8V – Digital IO) | VDDIO | 1.65 | 1.8 | 1.95 | V |
| Supply voltage (3.3V – Digital IO) | VDDIO | 3.0 | 3.3 | 3.6 | V |
| Supply voltage (1.2V – Digital Core) | VDDC | 1.1 | 1.2 | 1.3 | V |
| Supply voltage (1.2V – MIPI CSI PHY) | VDD_MIPI | 1.1 | 1.2 | 1.3 | V |
| Operating temperature (ambient temperature with voltage applied) | Ta | -30 | +25 | +85 | $^{o}$C |
| Supply Noise Voltage | $V_{SN}$ | - | - | 100 | $mV_{pp}$ |

TOSHIBA

TC358746AXBG/TC358748XBG

## 5.3. DC Electrical Specification

| Parameter | Symbol | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|
| Input voltage, High levelinput Note1 | $V_{IH}$ | 0.7 VDDIO | - | VDDIO | V |
| Input voltage, Low levelinput Note1 | $V_{IL}$ | 0 | - | 0.3 VDDIO | V |
| Input voltage High level CMOS Schmitt Trigger Note1,Note2 | $V_{IHS}$ | 0.7 VDDIO | - | VDDIO | V |
| Input voltage Low level CMOS Schmitt Trigger Note1,Note2 | $V_{ILS}$ | 0 | - | 0.3 VDDIO | V |
| Output voltage High level Note1, Note2 (Condition: IOH = -0.4mA) | $V_{OH}$ | 0.8 VDDIO | - | VDDIO | V |
| Output voltage Low level Note1, Note2 (Condition: IOL = 2mA) | $V_{OL}$ | 0 | - | 0.2 VDDIO | V |
| Input leak current, High level (Normal IO or Pull-up IO) (Condition: VIN = +VDDIO, VDDIO = 3.6V) | $I_{ILH1}$ (Note4) | -10 | - | 10 | µA |
| Input leak current,High level (Pull-down IO) (Condition: VIN = +VDDIO, VDDIO = 3.6V) | $I_{ILH2}$ (Note4) | - | - | 100 | µA |
| Input leak current,Low level (Normal IO or Pull-down IO) (Condition: VIN = 0V, VDDIO = 3.6V) | $I_{ILL1}$ (Note5) | -10 | - | 10 | µA |
| Input leak current,Low level (Pull-up IO) (Condition: VIN = 0V, VDDIO = 3.6V) | $I_{ILL2}$ (Note5) | - | - | 200 | µA |

Note1:     Each power source is operating within recommended operation condition.

Note2:     Current output value is specified to each IO buffer individually. Output voltage changes with output current value.

Note4:     Normal pin or Pull-up IO pin applied VDDIO supply voltage to Vin (input voltage)

Note5:     Normal pin or Pull-down IO pin applied VSSIO (0V) to Vin (input voltage)

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2014-05-29

# 6. Revision History

**Table 6.1   Revision History**

| Revision | Date | Description |
|---|---|---|
| 0.91 | 2014-05-29 | Newly released |

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