TC358746AXBG/TC358748XBG

Functional Specification

TOSHIBA

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HISTORY

Revision	Date	Note
Rev 0.1	11/02/2012	Copy from tc358746 Rev 034 Spec 1. Change I2C slave address from 0x0000_111x to 0x0001_110x 2. Modify bit 0x0004[6] to turn on/off Parallel port properly with register 0x0032[15:14] 3. Remove PClk toggle requirement when RefClk is used 4. No need to toggle RefClk to get out of reset. 5. Update Revision ID to 0x01
Rev 0.2	03/18/2013	Add TC358748XBG for new package (section3.3,3.4.3.6) Add Package (80 ball, 7.0 x 7.0 mm, 0.65 mm pitch) section7.2
Rev 0.3	04/21/2013	Corrected TC358748XBG ball assign
Rev 0.4	05/08/2013	Typo Correction
Rev 0.5	05/29/2013	Update Footer page
Rev 0.6	07/19/2013	1. Correct typo in Parallel In max PClk Freq to be 166 MHz 2. Add “Note” after Table 4-3 for packing muti-pixel/PClk possibility
Rev 0.7	08/13/2013	Remove 748 PinOut description, which should the same as those of 746A
Rev 0.8	11/18/2013	Update Fig 5-2 to indicate RefClk is required
Rev 0.9	03/28/2014	1. Remove Fail safe I2C pad operation 2. MClk can be output from GPIO0 in either mode 3. RefClk is not necessary, if not present/toggle, PClk/4 will be used to dirve PLL 4. Change HSync/VSync to HValid/VValid 5. Update Fig. 5-2 and adding Fig 5-3 to indicate RefClk is Not required in CSI-2 Tx mode

REFERENCES

1. MIPI D-PHY, “MIPI_D-PHY_specification_v01-00-00, May 14, 2009"
2. MIPI CSI-2, "MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) Version 1.01 Revision Nov 2010"
3. I2C bus specification, version 2.1, January 2000, Philips Semiconductor

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1 Overview

The MIPI CSI-2 to Parallel port and Parallel port to CSI-2 (TC358746AXBG/TC358748XBG) is a bridge device that converts MIPI data transfers from devices such as a camera to an application processor over a Parallel port interface. All internal registers can be access through I2C or SPI (in CSI out case only).

There are several system configurations where TC358746AXBG/TC358748XBG are typically be used

- CSI-2 TX with Parallel Input mode for Analog TV, Tele-presence Type, and Specialty/Older Cameras application. In this mode, TC358746AXBG/TC358748XBG (Parallel to CSI-2 converter) is a bridge device that converts parallel data transfers to an application over a MIPI CSI-2 interface. Toshiba Bridge Chip provides a low power bridge solution to efficiently translate parallel transfers to serial transfers.
- CSI-2 RX with Parallel output mode for scanner application. In this mode, TC358746AXBG/TC358748XBG (CSI-2 to Parallel converter) is a bridge device that converts serial data transfers from devices such as a camera to an application processor over a parallel interface. Toshiba Bridge Chip provides a low power bridge solution to efficiently translate serial transfers to parallel transfers.

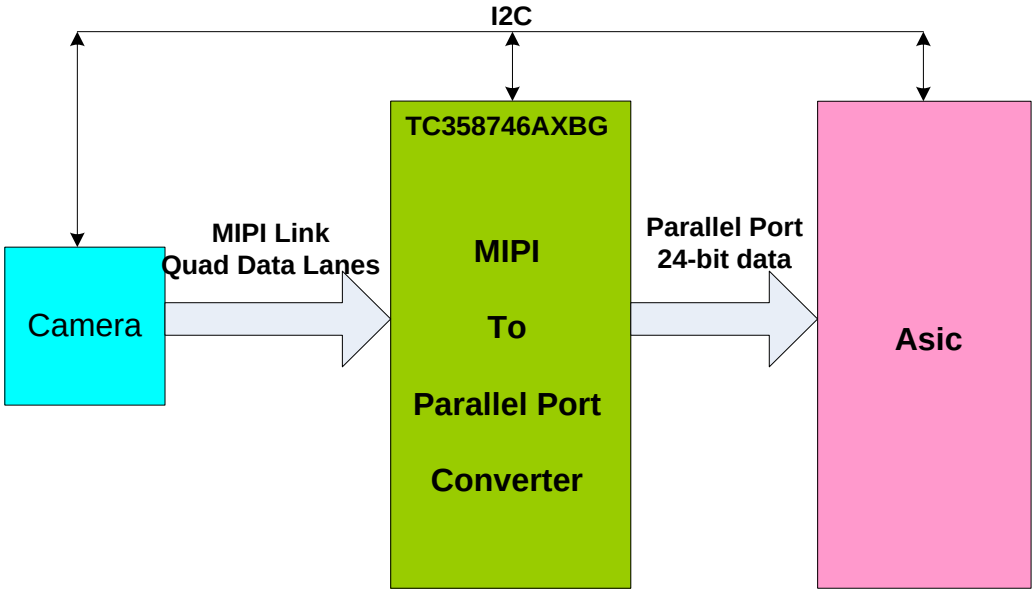

Figure 1-1 System Overview with TC358746AXBG/TC358748XBG in CSI-2 RX to Parallel Port Configuration

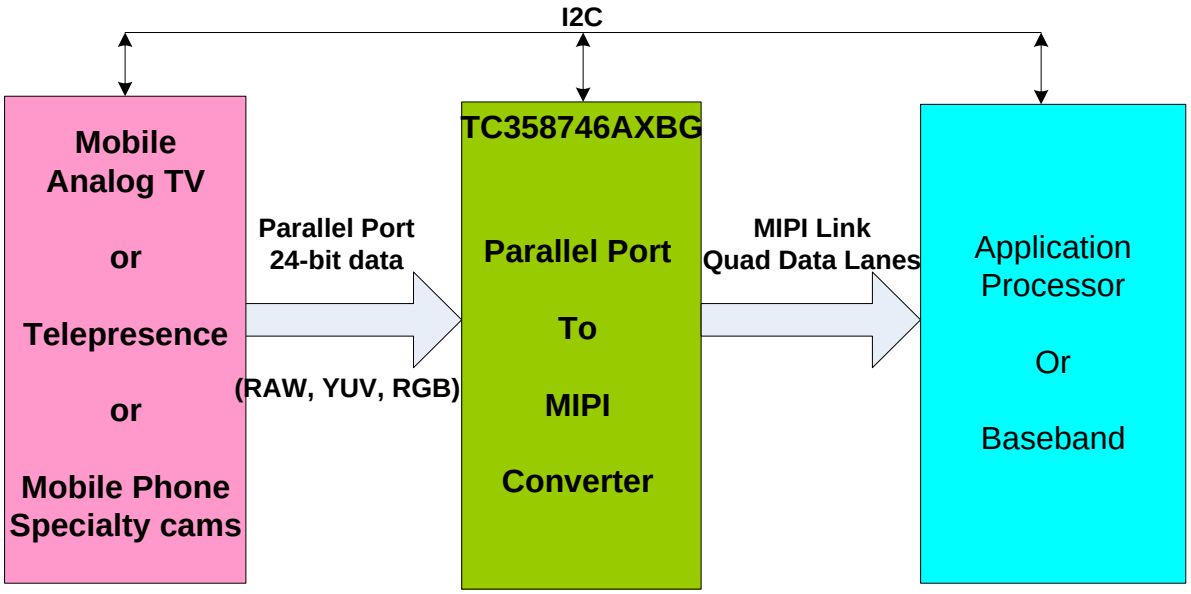

Figure 1-2 System Overview with TC358746AXBG/TC358748XBG in Parallel Port to CSI-2 TX Configuration

2 Features

Below are the main features supported by TC358746AXBG/TC358748XBG.

CSI-2 TX/RX Interface

- MIPI CSI-2 compliant (Version 1.01 Revision 0.04 – 2 April 2009)
- Configurable to TX or RX controller
- Supports up to 1Gbps per data lane
- Supports up to 4 data lanes
- Supports video data formats
  - RX: RAW8/10/12/14, YUV422 (CCIR/ITU 8/10-bit), RGB888/666/565 and User-Defined 8-bit
  - TX: YUV422 (CCIR/ITU 8/10-bit), YUV444, RGB888/666/565 and RAW8/10/12/14

Parallel Port Interface

- Supports data formats
  - 24-bit bus – un-packed format (Both Input and Output mode)
    - RGB888/666/565, RAW8/10/12/14 and YUV422 8-bit (on 8/16-bit data bus) and 10-bit data formats.
    - YUV444 (Parallel Input mode only)
  - YUV422 8-bit – ITU BT.656 and ITU BT.601 (Parallel input mode only)
- Up to 100 MHz PCLK frequency for Output mode, and 166 MHz for Input mode.

I2C Slave Interface (CS = L)

- Support for normal (100KHz), fast mode (400 KHz) and special mode (1 MHz)
- Configure all TC358746AXBG/TC358748XBG internal registers

SPI Slave Interface (Only applicable in CSIOut configuration, MSEL = H, and CS = H)

- SPI interface support for up to 25 MHz operation.
- Configure all TC358746AXBG/TC358748XBG internal registers

GPIO signals

- 3 GPIO signals
  - Three GPIO signals can be configured as control signals (MCLK, CXRST, XShutdown) for CSI-2 RX device.
  - Or one GPIO signal can be configured as INT signal for Parallel interface.

System

- ✧ Clock and power management support to achieve low power states.

Power supply inputs

- ✧ Core and MIPI D-PHY: 1.2V
- ✧ I/O: 1.8V – 3.3V

2.1 Typical Power Consumption

Parallel_In → CSI_Out, 500MHz CSICLk, 1080P @60fps				
	VDDIO (3.3V)	VDDC (1.2V)	VDD_MIPI (1.2V)	Total Power
Current (mA)	0.44	40.4	24.5	
Power (mW)	1.452	48.48	29.4	79.33

CSI_In → Parallel_Out, 500MHz CSICLk, 114MHz PClk ColorBar @60fps				
	VDDIO (3.3V)	VDDC (1.2V)	VDD_MIPI (1.2V)	Total Power
Current (mA)	18.9	13.9	12.3	
Power (mW)	62.37	16.68	14.76	93.81

3 External Pins

3.1 TC358746A pinout desctription

TC358746AXBG/TC358748XBG resides in BGA pin packages. The following table gives the signals of TC358746AXBG/TC358748XBG and their function.

Table 3-1 TC358746A/748XBG Functional Signal List

Group	Pin Name	I/O	Type	Initial	Function	Note
System: Reset & Clock (4)	RESX	I	Sch	-	System reset input, active low	
	REFCLK	I	N	-	Reference clock input (6MHz – 40MHz)	
	MSEL	I	N	-	Mode Select 1'b0: CSI-2 RX in –> Par_out 1'b1: Par_in -> CSI-2 TX	
	CS	I	N	-	Chip Select, active low MSEL= 0 (CSI-2 RX in –> Par_out) - When CS = 0, chip selected Normal operation - When CS = 1, chip not selected Cannot access to internal registers and optionally Parallel output ports can be tri-state when 0x0004[15] is set MSEL= 1 (Par_in -> CSI-2 TX) - CS = 0, I2C I/F is selected - CS = 1, SPI I/F is chosen	
MIPI-CSI (10)	MIPI_CP		PHY		MIPI-CSI clock positive	
	MIPI_CN		PHY		MIPI-CSI clock negative	
	MIPI_D0P		PHY		MIPI-CSI Data 0 positive	
	MIPI_D0N		PHY		MIPI-CSI Data 0 negative	
	MIPI_D1P		PHY		MIPI-CSI Data 1 positive	
	MIPI_D1N		PHY		MIPI-CSI Data 1 negative	
	MIPI_D2P		PHY		MIPI-CSI Data 2 positive	
	MIPI_D2N		PHY		MIPI-CSI Data 2 negative	
	MIPI_D3P		PHY		MIPI-CSI Data 3 positive	
	MIPI_D3N		PHY		MIPI-CSI Data 3 negative	
I2C (2)	I2C_SCL	OD	Sch		I2C serial clock or SPI_SCLK	4mA
	I2C_SDA	OD	Sch		I2C serial data or SPI_MOSI	4mA
Parallel Port (27)	PD[23:0]	I/O	N		Parallel Port Data - PD[23:12] can configs to be GPIO[15:4]	4mA
	VVALID	I/O	N		Parallel port VVALID signal	4mA
	HVALID	I/O	N		Parallel port HVALID signal	4mA
	PCLK	I/O	N		Parallel Port Clock signal	4mA
GPIOx (3)	GPIO[2:0]	I/O	N		**GPIO[2:0] signals** CSI-2 RX in –> Par_out - (GPIO[0] option to become MCLK signal) - (GPIO[1] option to become CXRST or INT) - (GPIO[2] option to become XShutdown) Par_in -> CSI-2 TX - (GPIO[0] option to become MCLK signal) - (GPIO[1] option to become SPI_SS or INT) - (GPIO[2] option to become SPI_MISO)	4mA
POWER	VDDC (1.2V)	NA			VDD for Internal Core (2)	

Group	Pin Name	I/O	Type	Initial	Function	Note
(9)	VDDIO (1.8V – 3.3V)	NA			VDDIO is for IO power supply (3)	
	VDD_MIPI (1.2V)	NA			VDD for the MIPI CSI2 (2)	
Ground (17)	VSS	NA			Ground	

3.2 TC358746AXBG BGA72 pin Count Summary

Table 3-2 BGA 72Pin Count Summary

Group Name	Pin Count	Notes
SYSTEM	4	
CSI2 IF	10	
I2C	2	
GPIOx	3	
Parallel Port IF	27	
POWER	9	IO, MIPI and Core Power
GROUND	17	
TOTAL	**72**	

3.3 TC358748 BGA80 Pin Count Summary

Table 3-3 TC358748 BGA 80 Pin Count Summary

Group Name	Pin Count	Notes
SYSTEM	4	
CSI IF	10	
I2C	2	
GPIOx	3	
Parallel Port IF	27	
POWER	9	IO, MIPI and Core Power
GROUND	25	
TOTAL	**80**	

3.4 TC358746A Pin Layout

A1	**A2**	**A3**	**A4**	**A5**	**A6**	**A7**	**A8**	**A9**
VSS	PD17	PD19	PD21	PD23	GPIO2	I2C_SCL	MSEL	VSS
B1	**B2**	**B3**	**B4**	**B5**	**B6**	**B7**	**B8**	**B9**
VDDC	PD16	PD18	PD20	PD22	GPIO1	I2C_SDA	RESX	VDDIO
C1	**C2**	**C3**	**C4**	**C5**	**C6**	**C7**	**C8**	**C9**
PD15	PD14	VSS	VSS	VSS	VSS	VDD_MIPI	MIPI_D3P	MIPI_D3N
D1	**D2**	**D3**				**D7**	**D8**	**D9**
PD13	PD12	VSS				VSS	MIPI_D2P	MIPI_D2N
E1	**E2**	**E3**				**E7**	**E8**	**E9**
VSS	VSS	VDDC				VDD_MIPI	MIPI_CP	MIPI_CN
F1	**F2**	**F3**				**F7**	**F8**	**F9**
VSS	VSS	VSS				VSS	MIPI_D1P	MIPI_D1N
G1	**G2**	**G3**	**G4**	**G5**	**G6**	**G7**	**G8**	**G9**
PD11	PD10	VDDIO	VSS	VSS	VDDIO	VDDIO	MIPI_D0P	MIPI_D0N
H1	**H2**	**H3**	**H4**	**H5**	**H6**	**H7**	**H8**	**H9**
VDDC	PD8	PD6	PD4	PD2	PD0	PCLK	HVALID	CS
J1	**J2**	**J3**	**J4**	**J5**	**J6**	**J7**	**J8**	**J9**
VSS	PD9	PD7	PD5	PD3	PD1	REFCLK	VVALID	GPIO0

Figure 3-1 TC358746AXBG BGA72-Pin Layout

3.5 TC358748 Pin Layout

A1	**A2**	**A3**	**A4**	**A5**	**A6**	**A7**	**A8**	**A9**	**A10**
VSS	PD17	PD19	PD21	PD23	GPIO2	VDDC	I2C_SCL	MSEL	VSS
B1	**B2**	**B3**	**B4**	**B5**	**B6**	**B7**	**B8**	**B9**	**B10**
VDDC	PD16	PD18	PD20	PD22	GPIO1	VSS	I2C_SDA	RESX	VDDIO
C1	**C2**	**C3**	**C4**	**C5**	**C6**	**C7**	**C8**	**C9**	**C10**
PD15	PD14							MIPI_D3P	MIPI_D3N
D1	**D2**	**D3**	**D4**	**D5**	**D6**	**D7**	**D8**	**D9**	**D10**
PD13	PD12		VSS	VSS	VSS	NC		MIPI_D2P	MIPI_D2N
E1	**E2**	**E3**	**E4**	**E5**	**E6**	**E7**	**E8**	**E9**	**E10**
PD11	PD10		VSS	VSS	VSS	NC		VSS	VDD_MIPI
F1	**F2**	**F3**	**F4**	**F5**	**F6**	**F7**	**F8**	**F9**	**F10**
PD9	PD8		VSS	VSS	NC	NC		MIPI_CP	MIPI_CN
G1	**G2**	**G3**	**G4**	**G5**	**G6**	**G7**	**G8**	**G9**	**G10**
PD7	PD6		NC	NC	NC	NC		MIPI_D1P	MIPI_D1N
H1	**H2**	**H3**	**H4**	**H5**	**H6**	**H7**	**H8**	**H9**	**H10**
VDDIO	VSS							VSS	VDD_MIPI
J1	**J2**	**J3**	**J4**	**J5**	**J6**	**J7**	**J8**	**J9**	**J10**
PD4	PD2	PD0	VSS	VSS	PCLK	HVALID	CS	MIPI_D0P	MIPI_D0N
K1	**K2**	**K3**	**K4**	**K5**	**K6**	**K7**	**K8**	**K9**	**K10**
PD5	PD3	PD1	VDDC	VDDIO	REFCLK	VVALID	GPIO0	VDDIO	VSS

Figure 3-2 TC358748XBG 80-Pin Layout (Top View)

3.6 System Overview

The TC358746AXBG/TC358748XBG has two major modes of operation that determine how data and control may be passed from the application processor to peripheral devices. The sections below describe each mode of operation.

3.6.1 CSI-2 RX to Parallel Port Operation

In this mode, TC358746AXBG/TC358748XBG received the data/controls from CSI-2 RX then transmits them out to Parallel port interface. Host uses I2C interface to configure all TC358746AXBG/TC358748XBG internal registers. TC358746AXBG/TC358748XBG has option to generate XShutdown/CXRST/MCLK signals for camera device through GPIO[2:0] signals.

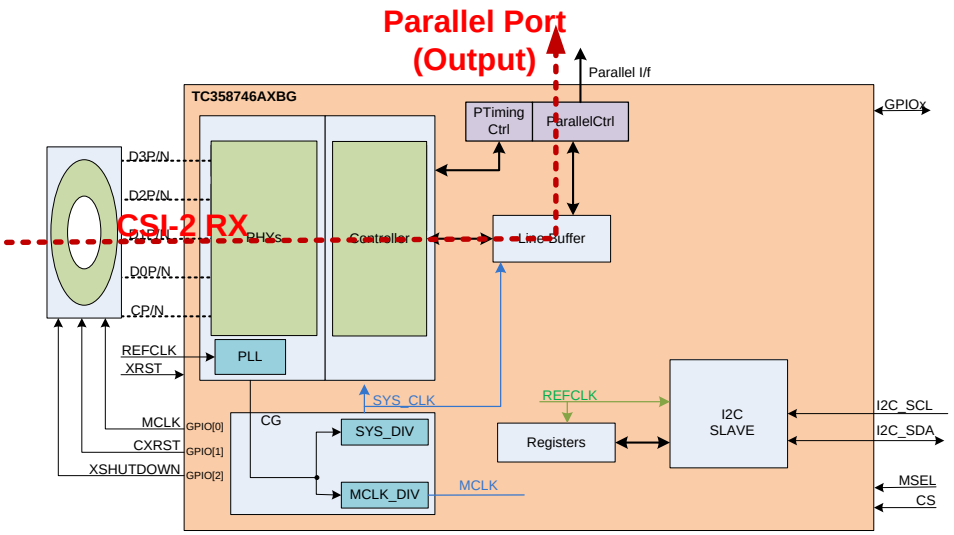

Figure 3-2 TC358746AXBG/TC358748XBGData/Control Flow in CSI-2 RX to Parallel Port configuration

3.6.2 Parallel Port to CSI-2 TX Operation

In this mode, TC358746AXBG/TC358748XBG received the data/controls from Parallel port then transmits them out to MIPI CSI-2/CSI2 TX. Host uses I2C/SPI interface to configure all TC358746AXBG/TC358748XBG internal registers.

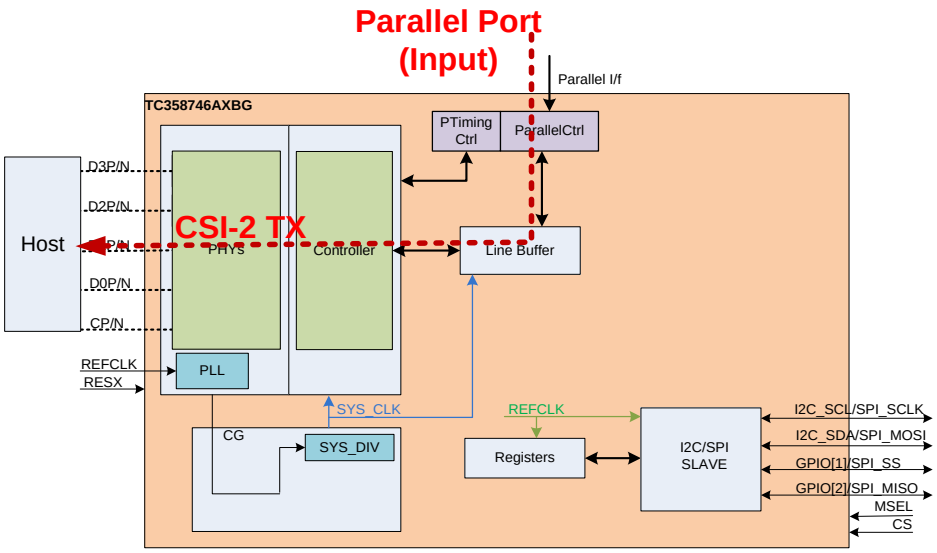

Figure 3-3 TC358746AXBG/TC358748XBGData/Controls Flow in Parallel Port to CSI-2 TX configuration

4 Function of Major Blocks

TC358746AXBG/TC358748XBG consists of the following major blocks: Rx/TxD-PHY, CSI-2 Rx/Tx Controller, Parallel port i/f and I2C i/f. Certain blocks are enabled and certain blocks are disabled depends on mode of operation.

Below are more information of which block is enabled or disabled based on the mode of operation.

1) CSI-2 RX with Parallel Output: CSI-2RX and Parallel port output blocks are enabled. Parallel input and CSI-2 TX block are disabled.
2) CSI-2 TX with Parallel Input: CSI-2 TX and Parallel port input blocks are enabled. And CSI-2 RX and Parallel port output blocks are disabled.

I2C slave block is always enabled which is required for configure the TC358746AXBG/TC358748XBG registers.

The following sections describe each block in detail. Addition, there is a section describes Clock generation block.

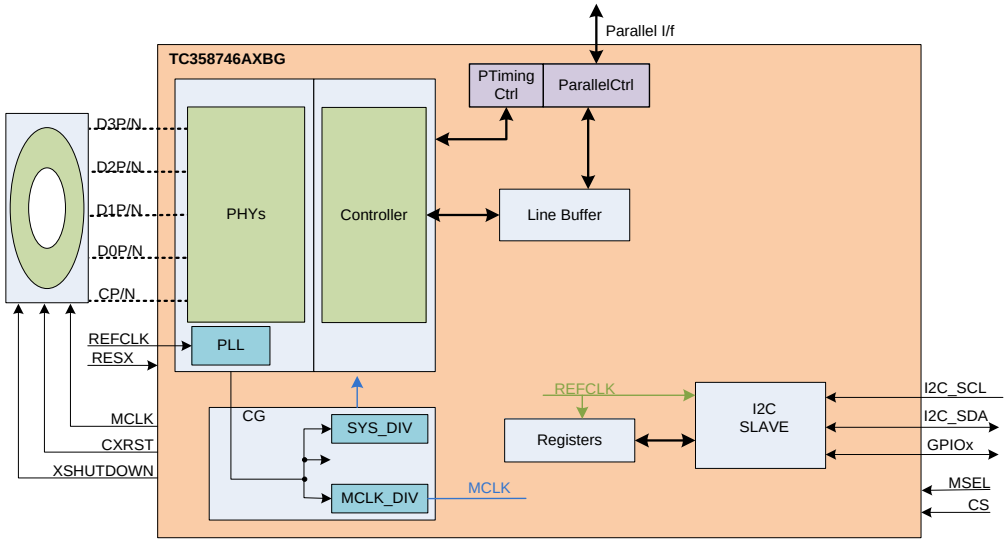

Figure 4-1 Block Diagram of TC358746AXBG/TC358748XBG

4.1 CSI-2 TX/RX Protocol

Table below shows all the data types that supported in TC358746AXBG/TC358748XBG.

Table 4-1 Supports Data Types

Data Type		Description
0x00		Frame Start Code
0x01		Frame End Code
0x22		RGB565 Data Type
0x23		RGB666 Data Type
0x24		RGB888 Data Type
0x1E		YUV422 8-bit Data Type
0x1F		YUV422 10-bit Data Type
0x2A		RAW8 Data Type
0x2B		RAW10 Data Type
0x2C		RAW12 Data Type
0x2D		RAW14 Data Type

VVALID, HVALID and Line# signals in figure below shows conceptual how frame start/end and line start/end related to HVALID, VVALID and Line#.

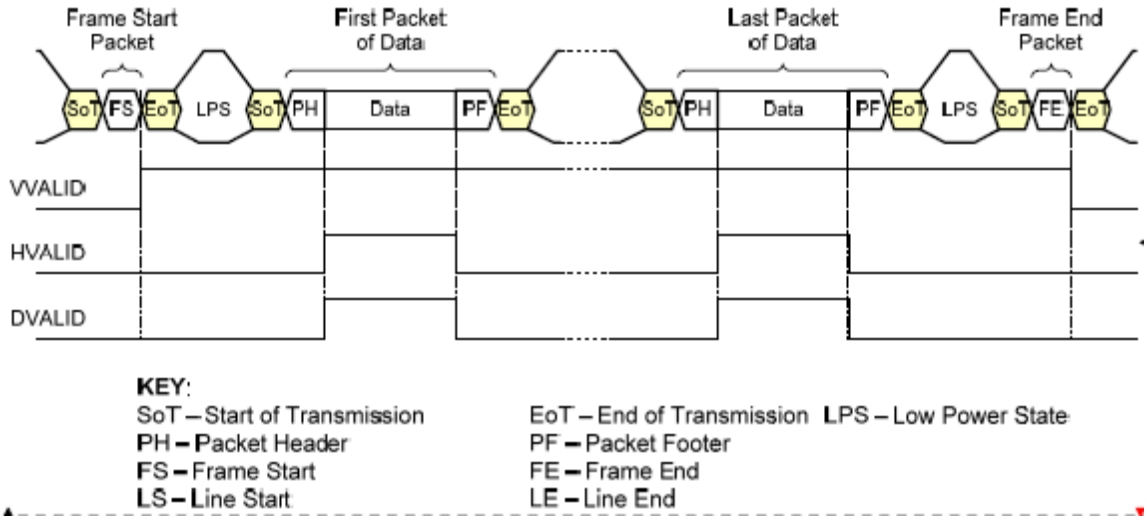

Figure 4-2 Multiple Packet Examle

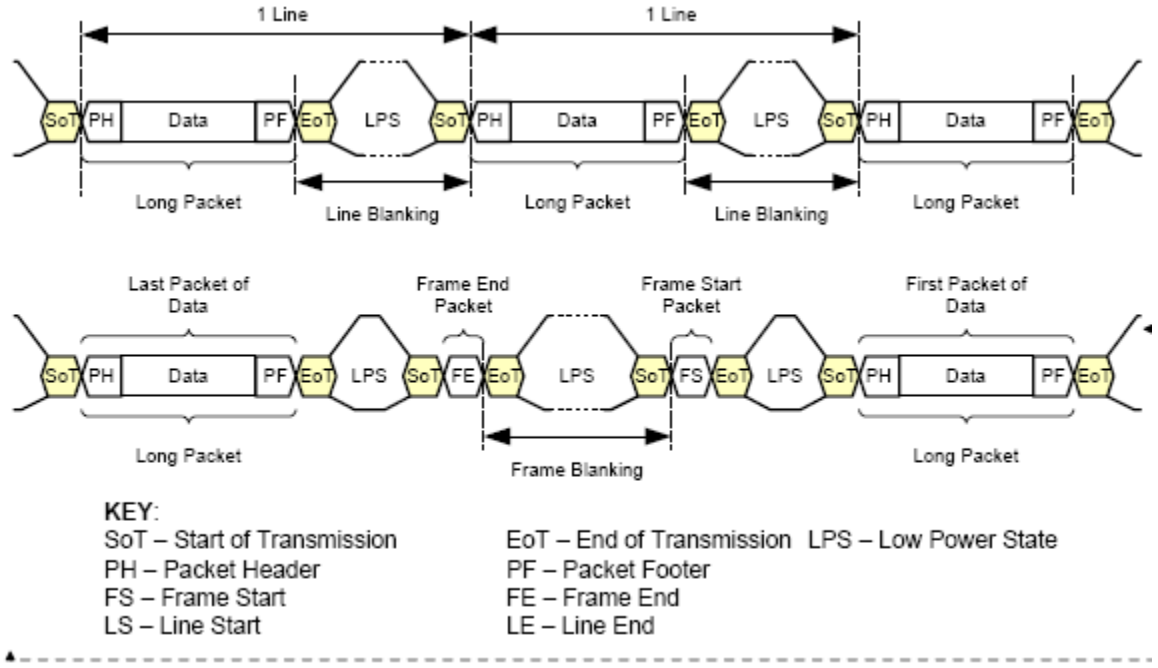

Figure 4-3 Line and Frame Blanking Definitions

CSI-2 terminology:

- Line Blanking Period is the period between the Packet Footer of one long packet and the Packet Header.
- Frame Blanking Period is the period between the Frame End packet in frame N and the Frame Start packet in frame N+1.

The Line Blanking Period is not fixed and may vary in length.

4.2 CSI-2 RX Interface Block

TheCSI2RX consists of CSI2 D-PHY and Receive Serial Protocol Layer blocks. CSI2 RX supports one clock lane and up to four data lanes which interface with a quad lane Serial Interface.

CSI2 Rx supports the following video data format

- YUV422 (CCIR/ITU 8/10-bit)
- RGB888/666/565
- RAW8/10/12/14 and
- User-Defined 8-bit

A lane merger block in Serial Protocol layer is for merging the two to four data lanes from Serial Rx PHY.

In Serial link, video data is transferred in byte oriented with LSB shifted out first for transmission. The data transmission format of each of video formats in Serial link are shown in Figures below.

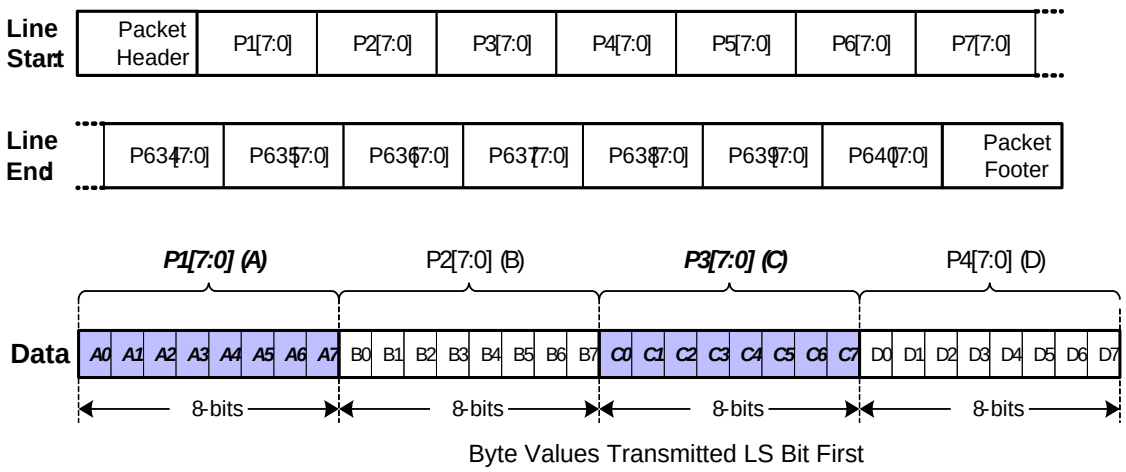

Figure 4-4 RAW8 Data Transmission

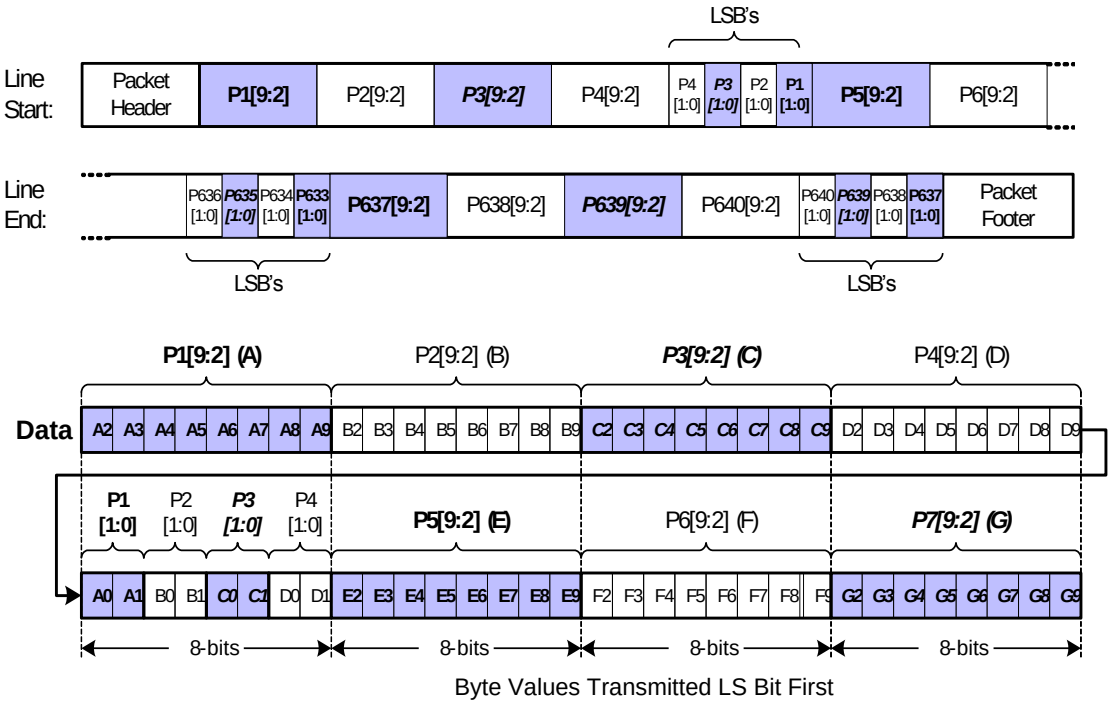

Figure 4-5 RAW10 Data Transmission

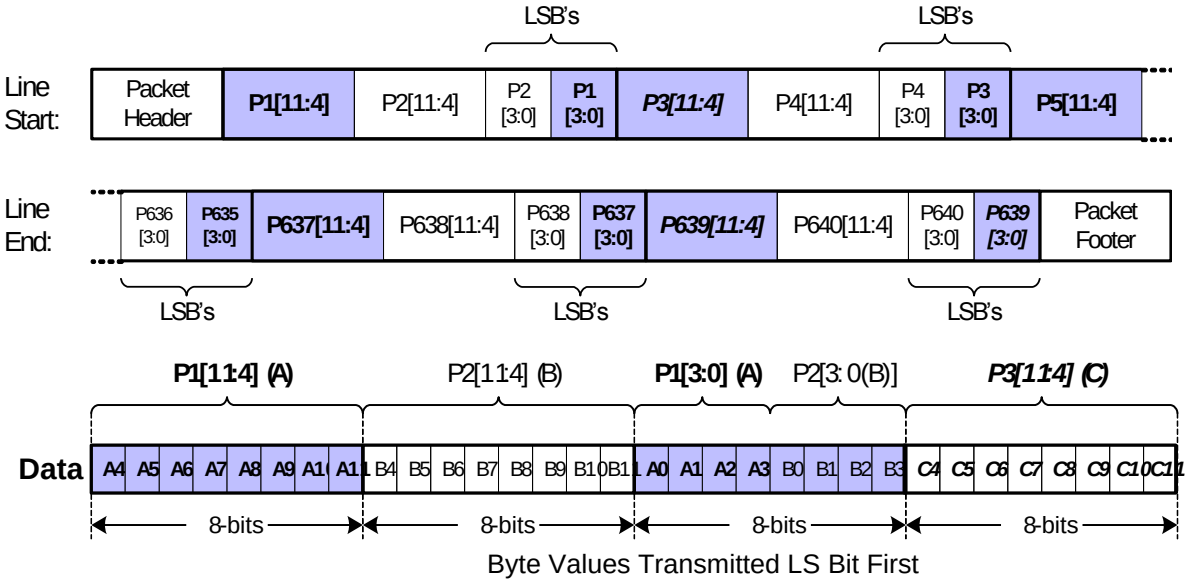

Figure 4-6 RAW12 Data Transmission

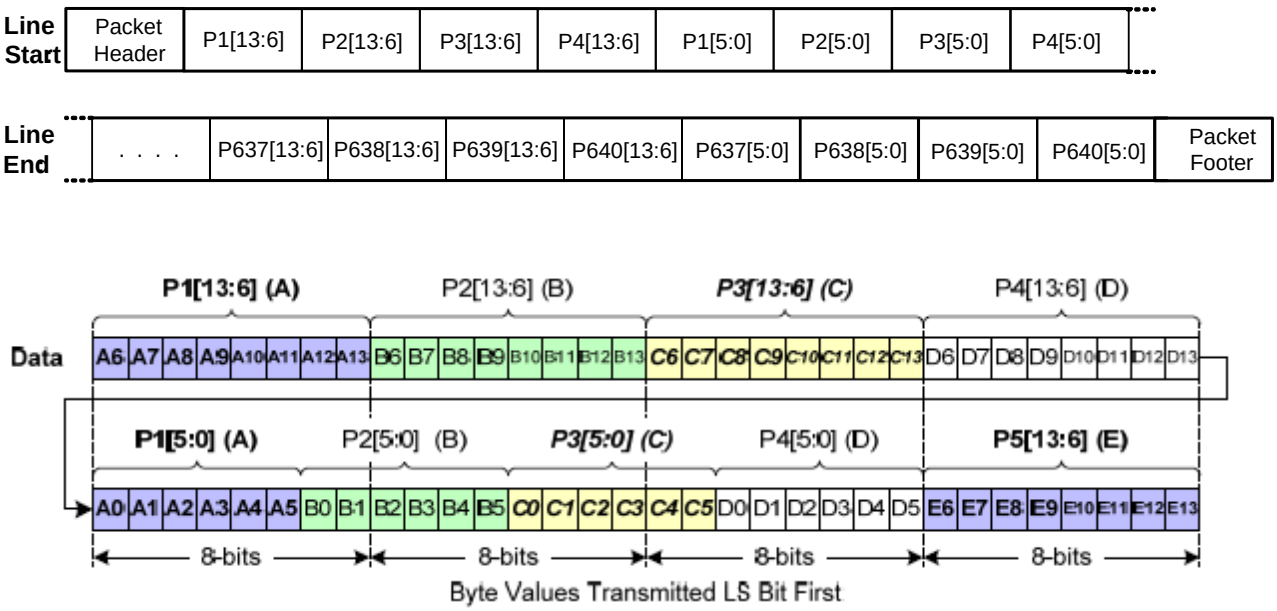

Figure 4-7 RAW14 Data Transmission

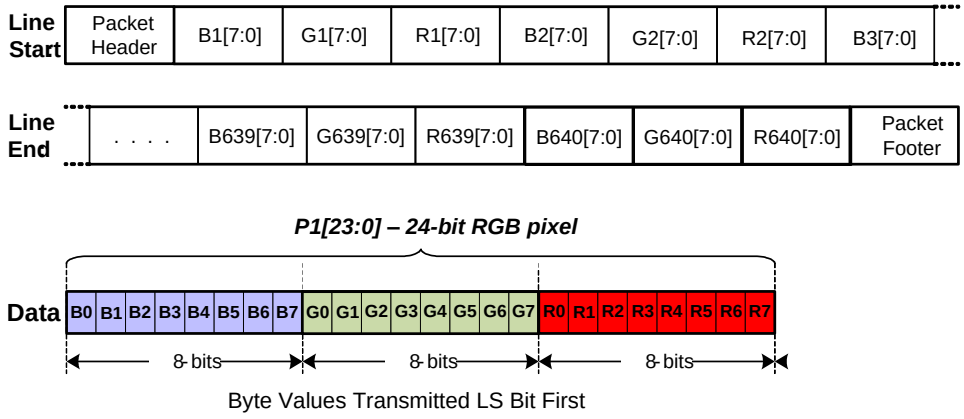

Figure 4-8 RGB888 Data Transmission

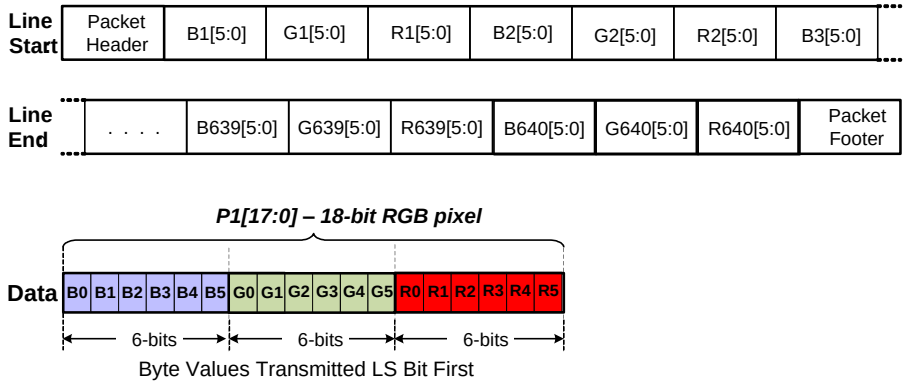

Figure 4-9 RGB666 Data Transmission

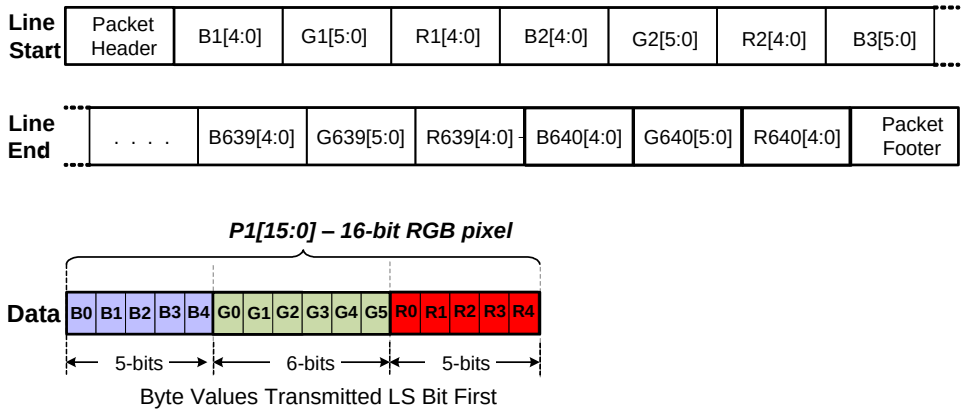

Figure 4-10 RGB565 Data Transmission

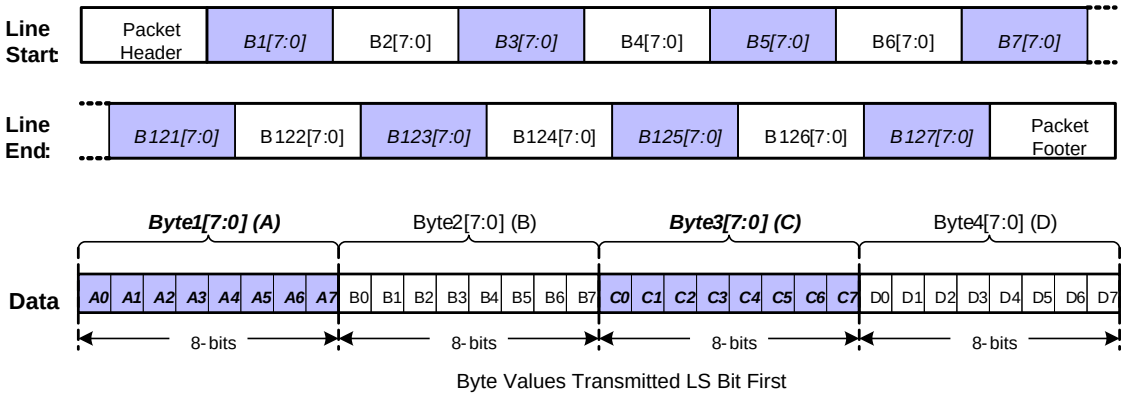

Figure 4-11 User Defined 8-bit Data Transmission

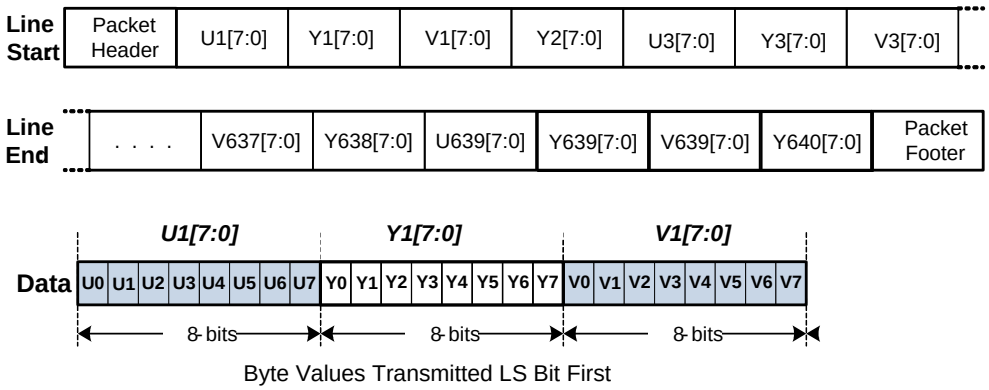

Figure 4-12 YUV422 8-bit Data Transmission

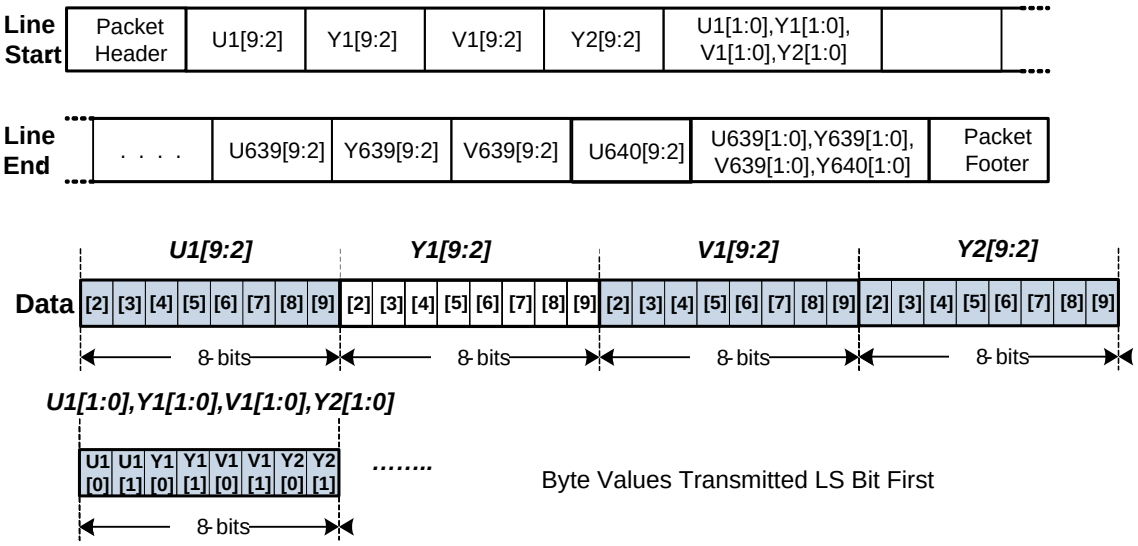

Figure 4-13 YUV422 10-bit Data Transmission

All serial byte data will be pack into 32-bit word data before write into the line buffer.

4.3 CSI-2 TX Interface Block

TheCSI-2TX consists of CSI-2 D-PHY and Transmit Serial Protocol Layer blocks. The CSI-2 TXsupports one clock lane and up to four data lanes which interface with a quad lane Serial Interface.

CSI-2 Tx supports the following video data format

- RAW8, RAW10, RAW12, RAW14, YUV422 8-bit, RGB888, RGB666, RGB565 and 8-bit User-Defined

A lane merger block in Serial Protocol layer is fetching the 32-bit data from VB module and splitting data to two to four data lanes - CSI-2 D- PHY.

The CSI-2 TX serial video data format is transferred in byte oriented with LSB shifted out first for transmission. These data transmission formats (RAW8/10/12/14, YUV422 8-bit, RGB888/666/565 and 8-bit User-Defined) are same as described in section 4.1.

4.4 CSI-2 Packet Format

The CSI-2 packet data formats are showed in Figure 4-2 and Figure 4-3. The Frame format is showed in below Figure

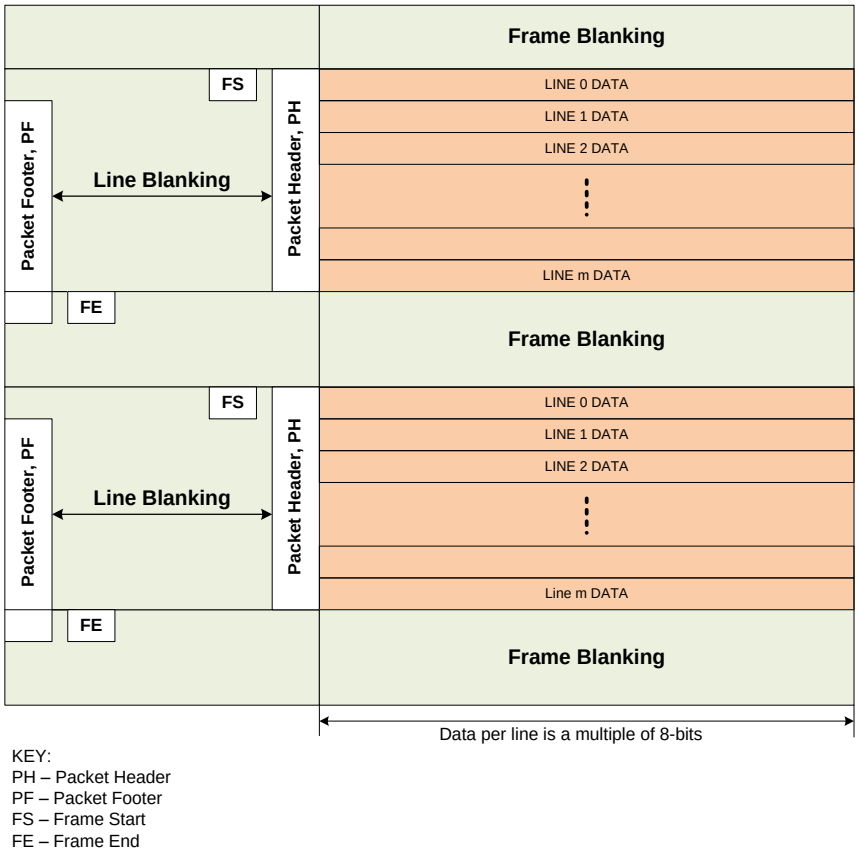

Figure 4-14 Frame Format

The CSI-2 TX transmits data based on these data formats and Frame format.

4.5 Checksum Generation

Checksum is calculated over each data packet. The checksum is realized as 16-bit CRC. The generator polynomial is $x^{16} + x^{12} + x^5 + x^0$.

The transmission of the checksum is showed in below Figure.

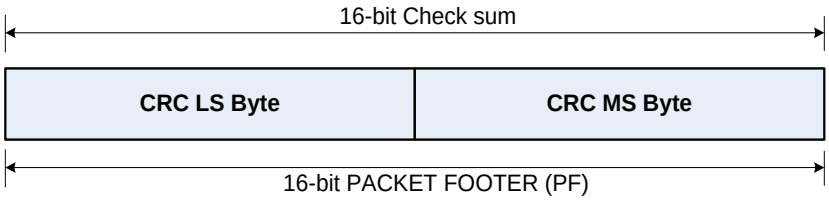

Figure 4-15 Checksum Transmission

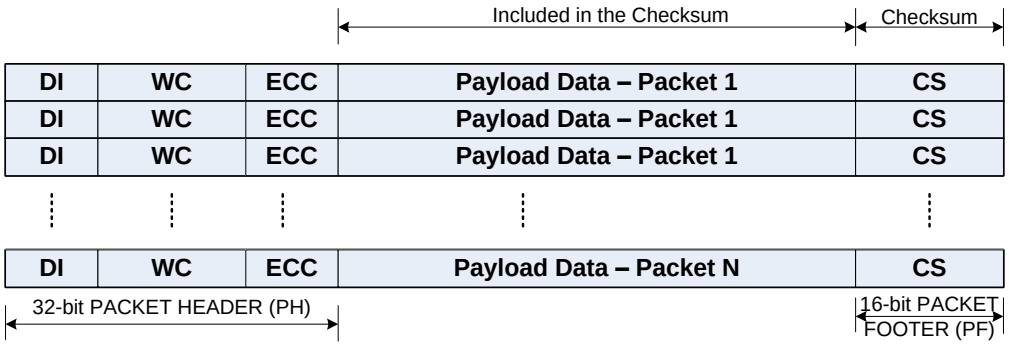

Figure 4-16 Checksum Generation for Packet Data

The 16-bit checksum sequence is transmitted as part of the Packet Footer. When Word Count is zero, the CRC shall be 0xFFFF.

4.6 CSI-2 TX One Frame Operation

Below describes the TC358746AXBG/TC358748XBG sequence for transmit out the video data onto CSI-2 TX.

1) Enable CSI-2 TX and Parallel Input port.
2) TC358746AXBG/TC358748XBG wait for assertion of VVALID (indicates beginning of frame)
3) TC358746AXBG/TC358748XBG wait for the Line buffer reaches the programmable “FIFO Level”.

4) Then transmit “FS” packet for 1st line only
5) Transmit “PH” packet – follow by Line Data until “pixel count” reached
6) Transmit “PF” packet then
    a. If Vvalid is not active, go to step “7”
    b. Otherwise, wait Line buffer reaches the programmable FIFO level then loop back to step “5”
7) Transmit “FE” packet, then loop back to step “3”

4.6.1 Enable and Disable Parallel Input (Video)

While TC358746A is running, the following procedures need to perform in order to stop and re-start video operation without reset. Otherwise, TC358746A might be hung, which needs to be reset.

Three registers bits, 0x0032[15] (FrmStop), 0x0032[14] (RstPtr) and 0x0004[6] (PP_En) needs to be programmed sequentially.

To stop TC358746A (video):

1 Set FrmStop to 1’b1, wait for at least one frame time for TC358746A to stop properly
2 Clear PP_En to 1’b0
3 Set RstPtr to 1’b1
4 Stop Video to TC358746A (optional)

To re-start TC358746A (video):

1 Start Video to TC358746A
2 Clear RstPtr and FrmStop to 1’b0
3 Set PP_En to 1’b1

4.7 Video Buffer Controller

TC358746AXBG/TC358748XBG contains integrate avideo buffer. Depends on mode of operation, input video data can be from either Serial RX controller or Parallel Input Port controller. Output video data (vb_out[31:0] connects to Parallel Output Port controller. Below is vb_top block diagram.

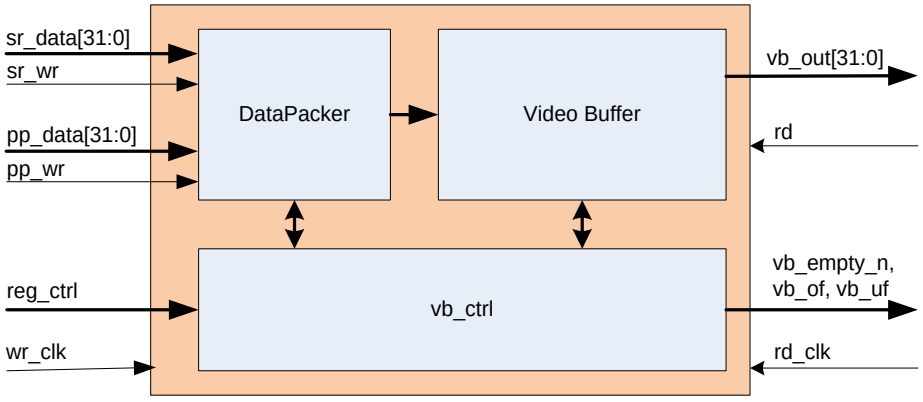

Figure 4-17 vb_top Block Diagram

Video data are always stored in the video line buffer as 32 bits data. Below table shows how the video data of each format map into the video line buffer.

Table 4-2 Data Packing in Video Line Buffer

Format	Data Packing in Video Line Buffer: vd[31:0]
RAW8	{P4[7:0], P3[7:0], P2[7:0], P1[7:0]}
RAW10	{P4[9:2], P3[9:2], P2[9:2], P1[9:2]} {P7[9:2], P6[9:2], P5[9:2], P4[1:0],P3[1:0],P2[1:0],P1[1:0]} {P10[9:2], P9[9:2], P8[1:0], P7[1:0], P6[1:0], P5[1:0], P8[9:2]} {P13[9:2], P12[1:0], P11[1:0], P10[1:0], P9[1:0], P12[9:2], P11[9:2]} {P16[1:0], P15[1:0], P14[1:0], P13[1:0],P16[9:2], P15[9:2], P14[9:2]}
RAW12	{P3[11:4], P2[3:0], P1[3:0], P2[11:4], P1[11:4]} {P6[11:4], P5[11:4], P4[3:0], P3[3:0], P4[11:4]} {P8[3:0], P7[3:0], P8[11:4], P7[11:4], P6[3:0], P5[3:0]}
RAW14	{ P4[13:6], P3[13:6], P2[13:6], P1[13:6] } { P5[13:6], (P4[5:0],P3[5:0],P2[5:0],P1[5:0]) } { (P6[1:0],P5[5:0]), P8[13:6], P7[13:6], P6[13:6] } { P10[13:6], P9[13:6], (P8(5:0],P7[5:0],P6[5:2]) } { (P11[3:0],P10[5:0],P9[5:0]), P12[13:6],P11[13:6] } { P15[13:6], P14[13:6], P13[13:6], (P12(5:0],P11[5:4]) }

	{ (P16[5:0],P15[5:0],P14[5:0],P13[5:0]),P16[13:6]}
RGB888	{B2[7:0], R1[7:0], G1[7:0], B1[7:0]} {G3[7:0], B3[7:0], R2[7:0], G2[7:0]} {R4[7:0], G4[7:0], B4[7:0], R3[7:0]}
RGB666	{R2[1:0], G2[5:0], B2[5:0], R1[5:0], G1[5:0], B1[5:0]} {G4[3:0], B4[5:0], R3[5:0], G3[5:0], B3[5:0],R2[5:2]} {B6[5:0], R5[5:0], G5[5:0], B5[5:0], R4[5:0], G4[5:4]} {B8[1:0], R7[5:0], G7[5:0], B7[5:0], R6[5:0], G6[5:0]} {R9[3:0], G9[5:0], B9[5:0], R8[5:0], G8[5:0], B8[5:2]} {G11[5:0], B11[5:0], R10[5:0], G10[5:0], B10[5:0], R9[5:4]} {G13[1:0], B13[5:0], R12[5:0], G12[5:0], B12[5:0], R11[5:0]} {B15[3:0], R14[5:0], G14[5:0], B14[5:0], R13[5:0], G13[5:2]} {R16[5:0], G16[5:0], B16[5:0], R15[5:0], G15[5:0], B15[5:4]}
RGB565	{R2[4:0], G2[5:0], B2[4:0], R1[4:0], G1[5:0], B1[4:0]}
YUV422 8-bit	{Y2, V1, Y1, U1} {Y4, V3, Y3, U3}
YUV422 10-bit	{ Y2[9:2], V1[9:2], Y1[9:2], U1[9:2] } {V3[9:2], Y3[9:2], U3[9:2], (Y2[1:0],V1[1:0],Y1[1:0],U1[1:0]) } { Y5[9:2], U5[9:2], (Y4[1:0],V3[1:0],Y3[1:0],U3[1:0]) Y4[9:2] } { U7[9:2], (Y4[1:0],V3[1:0],Y3[1:0],U3[1:0]), Y6[9:2] ,V5[9:2] } { (Y4[1:0],V3[1:0],Y3[1:0],U3[1:0]), Y8[9:2], V7[9:2], Y7[9:2] }
YUV444	{V2[7:0],Y1[7:0], U1[7:0], V1[7:0]} {U3[7:0], V3[7:0], Y2[7:0], U2[7:0]} {Y4[7:0], U4[7:0], V4[7:0], Y3[7:0]}
User Defined	{B4[7:0], B3[7:0], B2[7:0], B1[7:0]}

4.8 Parallel Output mode

4.8.1 Overview

TC358746AXBG/TC358748XBG supports 8-bit data bus (PD[7:0])or 24-bit data bus (PD[23:0]).

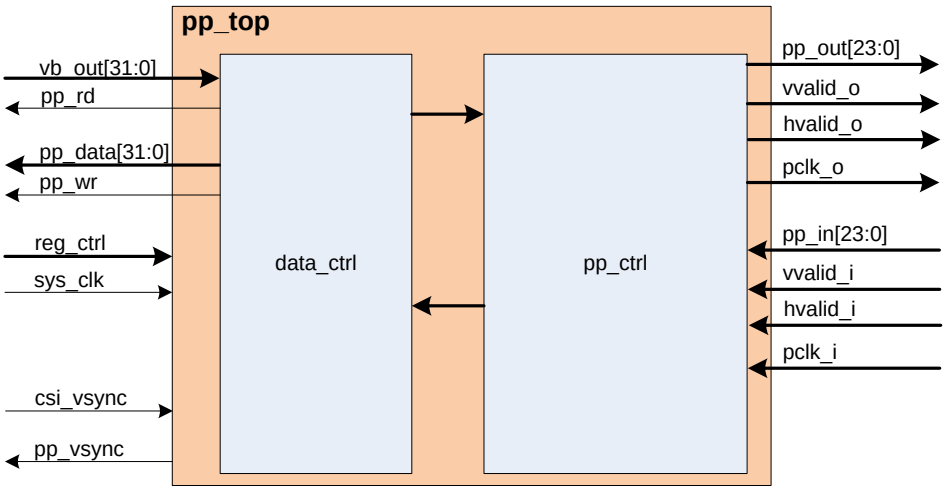

Figure 4-18 Block Diagram of Parallel portcontroller

4.8.2 24-bit Un-Packed Data Format

24-bit parallel output interface is capable to transfer various types of data formats (RAW8/10/12/14, RGB888/666/565, YUV422 8-bit on 8/16-bit bus and YUV422 10-bit). The signal connections for these types are shown in below Table.

Table 4-3 24-bit Unpacked Data bus

Data Type	Mode	Pin Usage	
		PD[23:0]	Comment
RAW8	X	{16'b0, P[7:0]}	1 pixel/ PClk
RAW10	X	{14'b0, P[9:0]}	1 pixel/ PClk
RAW12	X	{12'b0, P[11:0]}	1 pixel/PClk
RAW14	X	{10'b0, P[13:0]}	1 pixel/PClk
RGB888	X	{R[7:0],G[7:0],B[7:0]}	1 pixel/PClk
RGB666	0	{2'b0,R[5:0],2'b0,G[5:0],2'b0,B[5:0]}	1 pixel/PClk
RGB666	1	{6'b0,R[5:0],G[5:0],B[5:0]}	1 pixel/PClk
RGB565	0	{2'b0,R[4:0],3'b0,G[5:0],2'b0,B[4:0],1'b0}	1 pixel/PClk
RGB565	1	{3'b0,R[4:0],2'b0,G[5:0],3'b0,B[4:0]}	1 pixel/PClk

RGB565	2	{8'b0,R[4:0],G[5:0],B[4:0]}	1 pixel/PClk
YUV422 8-bit (8bit bus)	0	{16'b0,P[7:0]}	U1, Y1, V1, Y2, U3, Y3, V3, Y4 …
YUV422 8-bit (16bit bus)	1	{8'b0,P[15:0]}	{U1,Y1}, {V1,Y2}, {U3,Y3}, {V3,Y4}, ….
YUV422 8-bit (16bit bus)	2	{8'b0,P[15:0]} (Internal swap byte order)	{Y1,U1}, {Y2,V1}, {Y3,U3}, {Y4,V3}, ….
YUV422 10-bit	X	{14'b0, P9:0]}	U1, Y1, V1, Y2, U3, Y3, V3, Y4 …

Note: Pixel packed might be possible in certain conditions. Please contact Toshiba for details

4.8.3 Timing Diagrams for Video signals (Vvalid and Hvalid)

Parallel output signals are generated based on the CSI-2 packets received.

1. The receiving of FS, Frame Start, packet triggers the assertion of Vvalid. ①
2. The payload of a Data packet is streamed into the video buffer (FiFo).
3. When the video buffer reached the user-defined level, programmed in register 0x0006, Hvalid is asserted and data starts outputting. ②
4. Hvalid de-asserts when all the data within one Data packet has been output as shown in ③
5. Repeating steps 2 to 4 until FE, Frame End, packets arrived. Vvalid is de-asserted. ④
6. Loop back to step one.

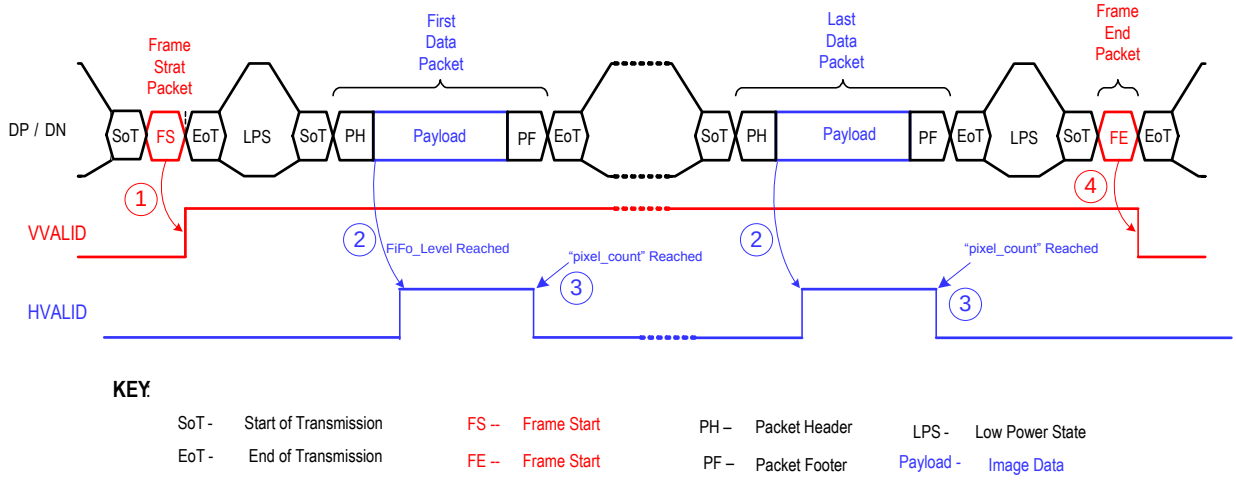

Figure 4-19 VVALID/HVALID Timing Diagram for Parallel Output mode

4.9 Parallel Input mode

4.9.1 Overview

24-bit parallel input interface is capable to transfer various types of data formats (RAW8/10/12/14, RGB888/666/565, YUV422 8-bit on 8/16-bit bus and YUV422 10-bit). The signal connections for these types are shown in below Table.

Table 4-4 24-bit Unpacked Data bus

Data Type	Mode	Pin Usage	
		PD[23:0]	Comment
RAW8	X	{16'b0, P[7:0]}	1 pixel/ PClk
RAW10	X	{14'b0, P[9:0]}	1 pixel/ PClk
RAW12	X	{12'b0, P[11:0]}	1 pixel/PClk
RAW14	X	{10'b0, P[13:0]}	1 pixel/PClk
RGB888	0	{R[7:0],G[7:0],B[7:0]}	1 pixel/PClk
RGB888	1	{R[1:0]G[1:0],B[1:0],R[7:2],G[7:2],B[7:2]}	1 pixel/PClk
RGB666	0	{2'b0,R[5:0],2'b0,G[5:0],2'b0,B[5:0]}	1 pixel/PClk
RGB666	1	{6'b0,R[5:0],G[5:0],B[5:0]}	1 pixel/PClk
RGB565	0	{2'b0,R[4:0],3'b0,G[5:0],2'b0,B[4:0],1'b0}	1 pixel/PClk
RGB565	1	{3'b0,R[4:0],2'b0,G[5:0],3'b0,B[4:0]}	1 pixel/PClk
RGB565	2	{8'b0,R[4:0],G[5:0],B[4:0]}	1 pixel/PClk
YUV422 8-bit (8-bit)[note]	0	{16'b0,P[7:0]}	U1, Y1, V1, Y2, U3, Y3, V3, Y4 …
YUV422 8-bit (16-bit)	1	{8'b0,P[15:0]}	{U1,Y1}, {V1,Y2}, {U3,Y3}, {V3,Y4}, ….
YUV422 8-bit (16-bit)	2	{8'b0,P[15:0]} (internal swap byte order)	{Y1,U1}, {Y2,V1}, {Y3,U3}, {Y4,V3}, ….
YUV422 10-bit	X	{14'b0, P9:0]}	U1, Y1, V1, Y2, U3, Y3, V3, Y4 …
YUV444	X	{Y[7:0],U[7:0],V[7:0]}	1 pixel/PCLK (Y=G, U=B, V=R)

Note: When input is BT656 format, as enabled in register bit 0x0004[12], bit[9:2] should be used as per Rec. ITU-R BT656-4.

The Parallel Input controller received the video data from external. It then packed these into 32-bit data format then transfers the packed data into the Line buffer. The 32-bit data format is showed in Table 4-3.

Parallel Input controller is operated with PCLK only. All asynchronous logic is handled inside Video buffer Controller

4.9.2 Timing Diagrams for Video signals (Vvalid and Hvalid)

Below Figures show the timing relationship between HVALID, VVALID and DP/DN.

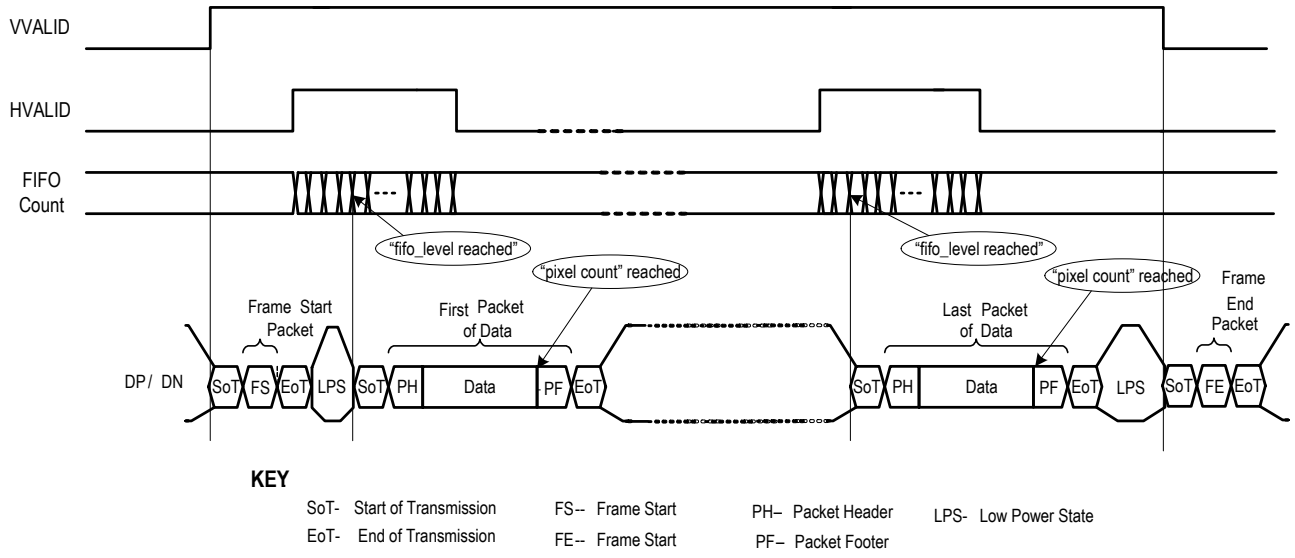

Figure 4-20 VVALID/HVALID Timing Diagram (for Parallel Input mode)

4.10 I2C

4.10.1 Overview

TC358746AXBG/TC358748XBG supports an I2C slave function. The I2C module supports the following features:

- Fail safe I2C pad operation
- Up to 1MHz mode operation (1MHz: Special mode, 400KHz: fast mode, 100KHz: normal mode)
- Supports 7 bit slave addresses recognition (slave address=8'b0001_110X)
- No support for general call address
- Supports 16 bit index value for TC358746AXBG/TC358748XBG I2C slave access

The I2C slave function supports a fixed slave address only and does not support general call address. The I2C slave function does not require any programmable configuration parameters.

4.10.2 I2C Write Access

Registers in TC358746AXBG/TC358748XBG are 16-bit aligned. This implies that I2C accesses to registers are recommended to be done on 16-bit boundaries. Note that data transferred on the I2C bus is sent MSB first. For 32-bit addressable registers listed in Table 6-1, two back-to-back 16-bit write operations (lower address one first) are necessary in order to update the 32-bit registers.

Alternatively, for 32-bit registers can be written in 32-bit in one access with byte order shown below.

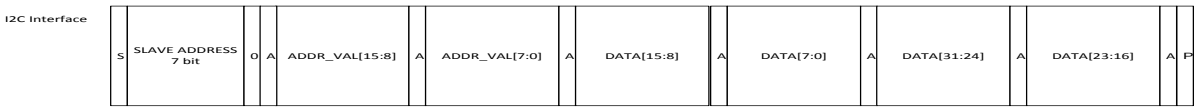

Figure 4-21 32-bit Write Transfers Byte Order

4.10.3 I2C Read Access

Registers in TC358746AXBG/TC358748XBG are 16-bit aligned. This implies that I2C accesses to registers should always be done on 16 bit boundaries, Figure 4-22. Note that data transferred on the I2C bus is sent MSB first. For continuously reading, a 32-bit register data byte order is shown in Figure 4-23 below.

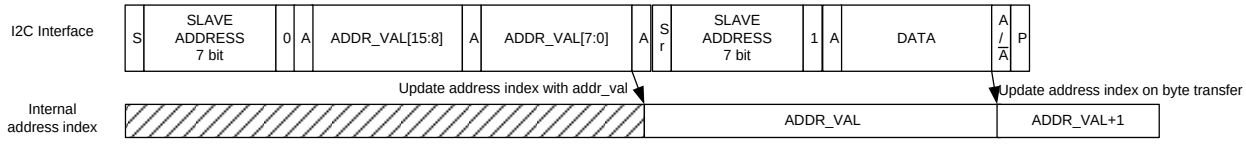

Figure 4-22 I2C Read Transfers over I2C Bus

. Note that data transferred on the I2C bus is sent MSB first. For continuously reading, a 32-bit register data byte order is shown below.

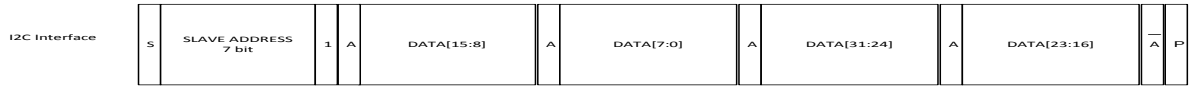

Figure 4-23 I2C 32-bit Read Transfers Byte Order

4.11 SPI Slave Interface

The TC358746AXBG/TC358748XBG Bridge Chip incorporates a SPI Slave Interface port which Host can drive to configure registers in the chip if Par_In → CSIOut configuration is select by driving MSEL = H.

The following features are supported:

- Slave select pin supported
- Clock Polarity and Phase selectable
- Transfer Frame size of 32 bits
- Slave speed is up to 25 MHz
- Supports 16 bit index value for TC358746AXBG/TC358748XBG SPI slave access

The basic operation of SPI interface is shown below where the standard 4-wire interface is used for transactions between the Host (SPI Master) and TC358746AXBG/TC358748XBG (SPI Slave).
The Host asserts (active low) the Slave Select signal (SPI_SS) when it wants to initiate a read or write transaction. This is followed by the Host sending 32 pulses on the SPI Clock signal (SPI_SCK). In this spec., the bit slots are assumed numbered 31 to 0 from left to right.
Once the intended 16 bits (for TC358746AXBG/TC358748XBG register address and command) and the additional data bits have been transferred, the Host de-asserts the Slave Select signal (SPI_SS) to indicate end of frame transfer.
This is shown in a simplistic way in the figure below (16bits transfer size shown in the figure).

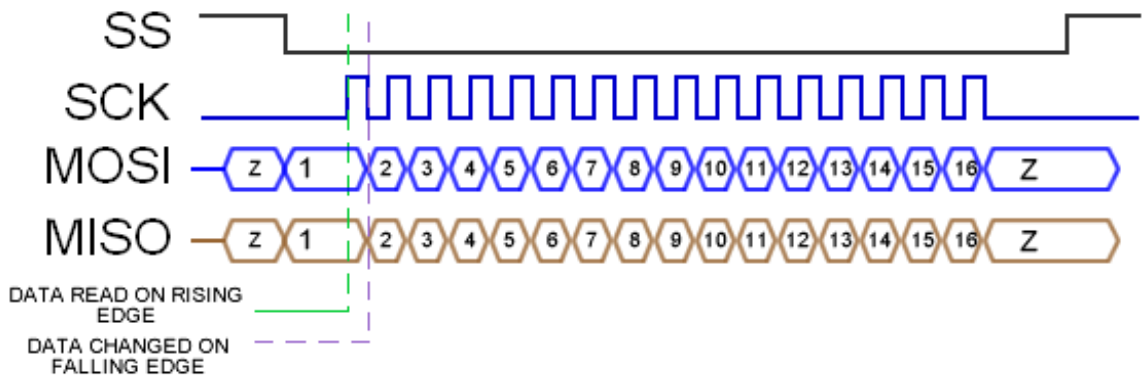

Figure 4-24 SPI basic operation

4.11.1 Clocking Modes

The SPI slave function supports one clocking mode which shown below.

Table 4-5 SPI Clocking modes

Mode	SPOL	SPHA	Drive Edge	Sample Edge	Comments
3	1	1	negedge	posedge	Master/Slave drive first data on first active clock edge

4.11.1.1 Timing Diagram

In this transfer format, the first bit value is captured on the second clock edge. This will be on a rising edge. The levels on the MOSI and MISO signals always change with the inactive clock edges on SCLK. The inactive clock edge will be the falling edge. It will idle high.

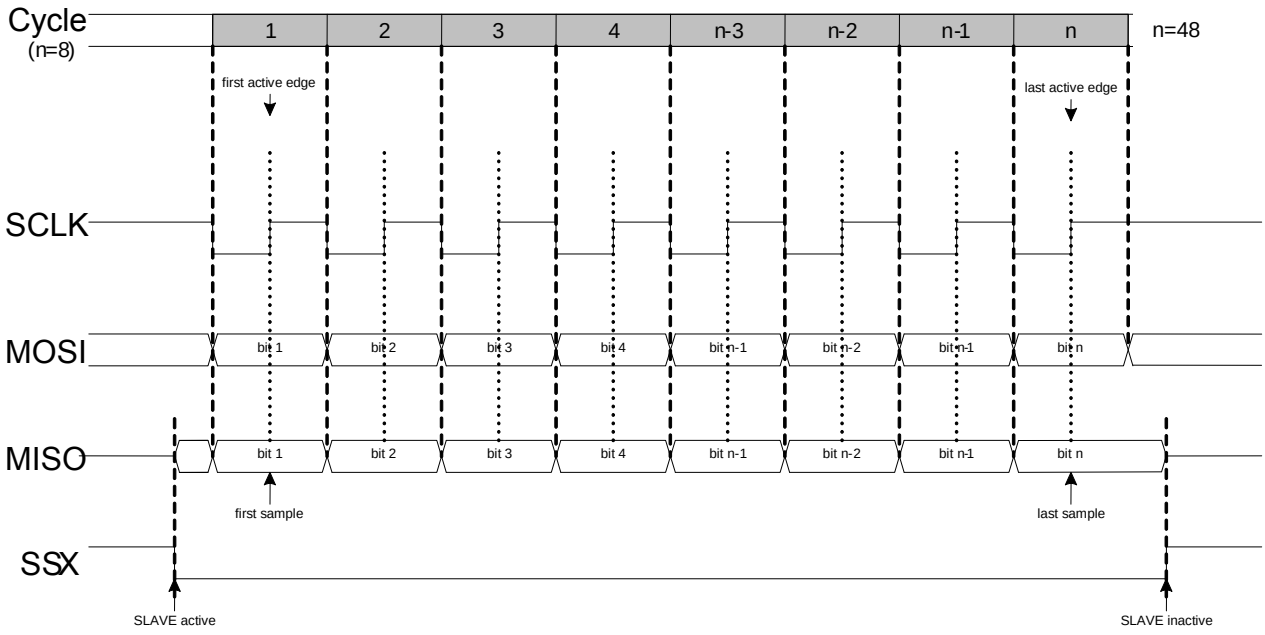

Figure 4-25 SPI Transfer

4.11.1.2 Providing Register Address over SPI Interface

The SPI transactions are performed in 32 bits wide frames. The SPI master drives the command and address of the TC358746AXBG/TC358748XBG register to be accessed. The first 15 bits provide the register address bits 15 to 1. The 16th bit of a frame is the command: 0=Write / 1=Read. Meaning of rest of the bits is based on transaction type. This frame structure is shown in the figure below for a write transaction.

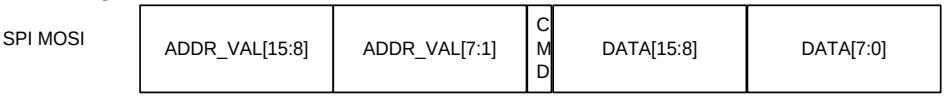

Figure 4-26 Register Write Transfer over SPI (transfer size=32 bits)

CMD = Command: 1=Read / 0=Write
SPI slave function supports random write and read accesses.

4.11.1.3 SPI Write Access Translation

Registers in TC358746AXBG/TC358748XBG are 16 bit aligned. This implies that SPI accesses to registers should always be done on 16 bit boundaries. The SPI slave will update an internal 16-bit write data register indexed by the address in the SPI frame. The data in bit slots 15 to 0 (after the first 16 bits of address and command) on MOSI line is used as the write data for these writes. Write access to TC358746AXBG/TC358748XBG registers over the register interface is performed when a frame transfer is completed with command bit set to 0. During the write transaction, the data on the MISO line is not related to the write transaction. How to handle the data on MISO line during write transactions is discussed more in section on full-duplex mode.

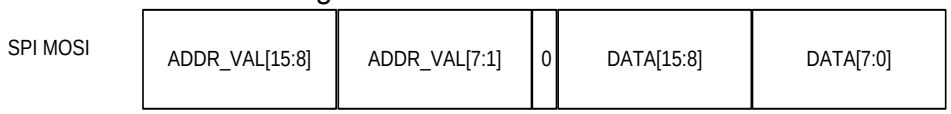

Figure 4-27 Register Write Transfer over SPI (transfer size=32 bits)

4.11.1.4 SPI Read Access Translation

Registers in TC358746AXBG/TC358748XBG are 16 bit aligned. This implies that SPI accesses to registers should always be done on 16 bit boundaries. The SPI slave will access an internal 16-bit data register indexed by the address in the SPI frame.

Read access to TC358746AXBG/TC358748XBG registers is completed in two frames. The first frame is similar to a write frame (as shown above) but with the 16 bits of data on MOSI line ignored by TC358746AXBG/TC358748XBG. This step provides the 15 bits index address of the TC358746AXBG/TC358748XBG register to be accessed. The only difference in this step from Write frame is that the command bit is set to 1 (Read command). During the second frame period, the TC358746AXBG/TC358748XBG stuffs the read data into the bit slots 15 to 0 based on the data from the TC358746AXBG/TC358748XBG register indexed by the read command address in the first frame as shown below. Handling of MISO line during first frame period and MOSI line during the second frame period is discussed further in full-duplex mode section.

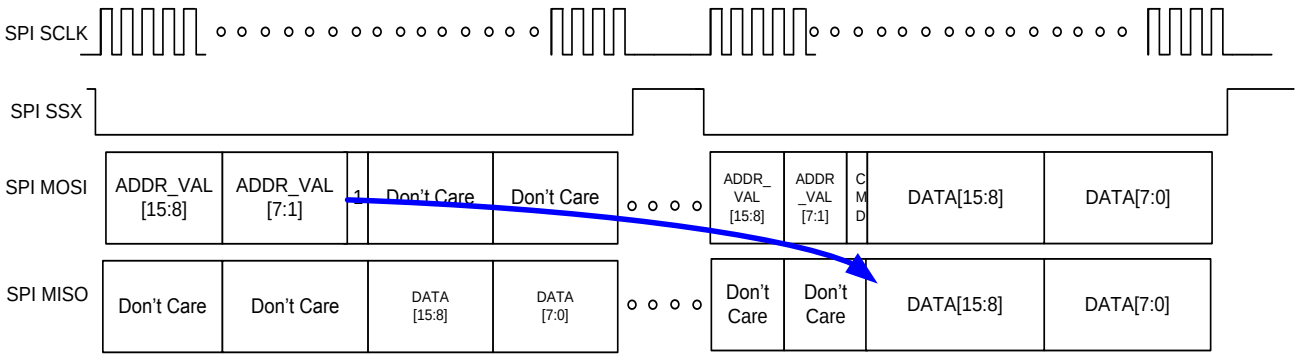

Figure 4-28 Register Read (Normal) Transfer over SPI (transfer size=32 bits)

4.11.2 Full Duplex

All above transactions are considered as full duplex by TC358746AXBG/TC358748XBG by default. During any frame, TC358746AXBG/TC358748XBG inserts the data from the TC358746AXBG/TC358748XBG register that was last addressed by the read command from the SPI master into the bit slots 15 to 0 of the frame on MISO line. During any frame, the bits on the MOSI line bit slots 31 to 17 are considered as the address with the bit slot 16 providing the command. Data on MOSI line during bit slots 15 to 0 are used as write data.

The data on MISO line during bit slots 15 to 0 always corresponds to the previous frame's read command and can be ignored by the SPI Master if the previous frame command was a read command.

The data on MOSI line during bit slots 31 to 17 always provides the address for the TC358746AXBG/TC358748XBG register for the current frame command.

The data on MOSI line during bit slots 15 to 0 will always be written into the TC358746AXBG/TC358748XBG register addressed by current frame's address bits (bit slots 31 to 17) if the command in the current frame is a write command.

Four scenarios are possible for back to back transactions as explained below.

4.11.2.1 Back-2-back writes

In this case, the data on the MOSI line is always valid during both back-2-back frames and used for TC358746AXBG/TC358748XBG register writes. The data on the MISO line in first frame might correspond to a read command issued in the previous frame. Data on the MISO line in 2nd frame is redundant (corresponds to the TC358746AXBG/TC358748XBG register addressed by the last read command some frames ago).

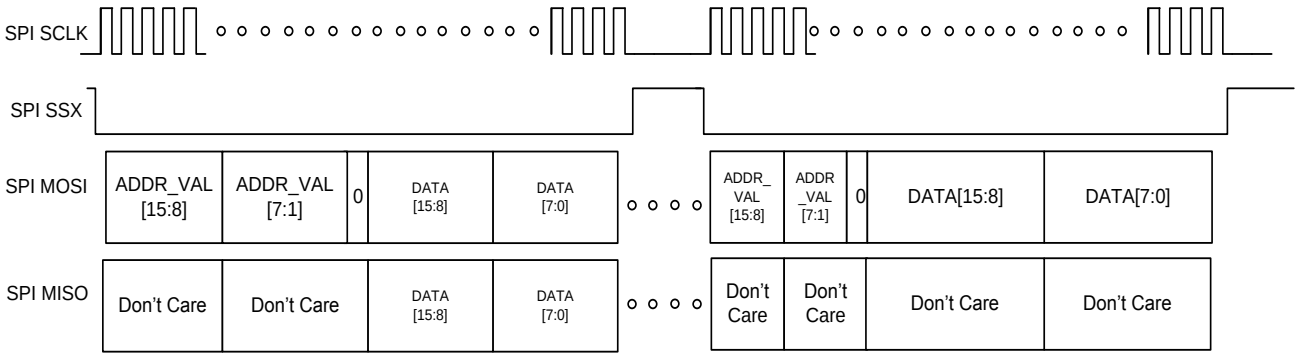

Figure 4-29 Back-2-Back Write Transfers over SPI

4.11.2.2 Back-2-back reads

In this case, the data on the MOSI line is always valid only during first 16 bits (bit slots 31 to 16) in both back-2-back frames and used for TC358746AXBG/TC358748XBG register reads. The data on the MISO line in first frame might correspond to a read command issued in the previous frame. Data on the MISO line in 2nd frame corresponds to the TC358746AXBG/TC358748XBG register addressed by the read command in 1st frame. The read data corresponding to the register addressed by the read command in 2nd frame shall be available in the next (3rd) frame on MISO line.

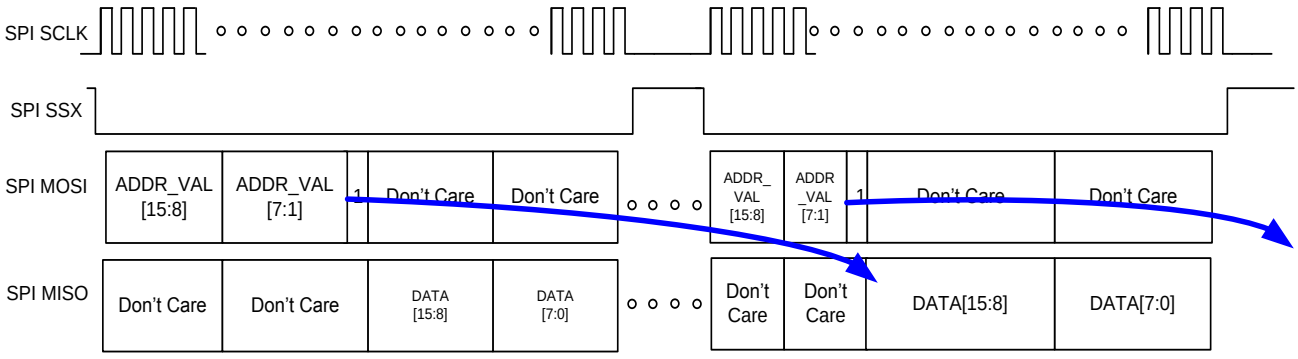

Figure 4-30 Back-2-Back Read Transfers over SPI

4.11.2.3 Write-after-Read

In this case, the handling of data on MISO and MOSI lines during first frame is similar to the "Back-to-Back reads" case. Data on the MOSI line during first 16 bits (bit slots 31 to 16) in 2nd frame provides the address and command for the write (write-after-read). Data on the MOSI line during bit slots 15 to 0 in 2nd frame provides the write data for the write command. Data on the MISO line in 2nd frame corresponds to the TC358746AXBG/TC358748XBG register addressed by the read command in 1st frame.

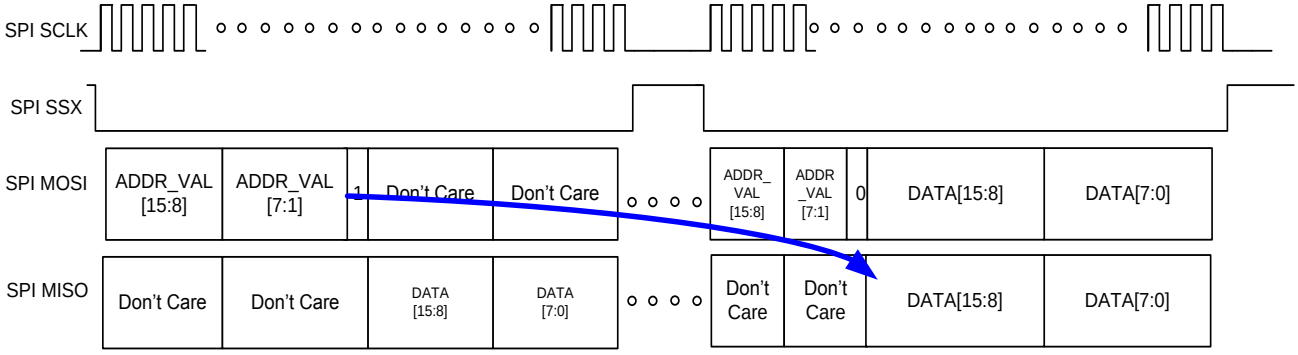

Figure 4-31 Write-after-Read Transfer over SPI

4.11.2.4 Read-after-Write

In this case, the handling of data on MISO and MOSI lines during first frame is similar to the "Back-to-Back writes" case. Data on the MOSI line during first 16 bits (bit slots 31 to 16) in 2nd frame provides the address and command for the read (read-after-write). Data on the MOSI line during bit slots 15 to 0 in 2nd frame is redundant. Data on the MISO line in 2nd frame is redundant.The read data corresponding to the register addressed by the read command in 2nd frame shall be available in the next (3rd) frame on MISO line.

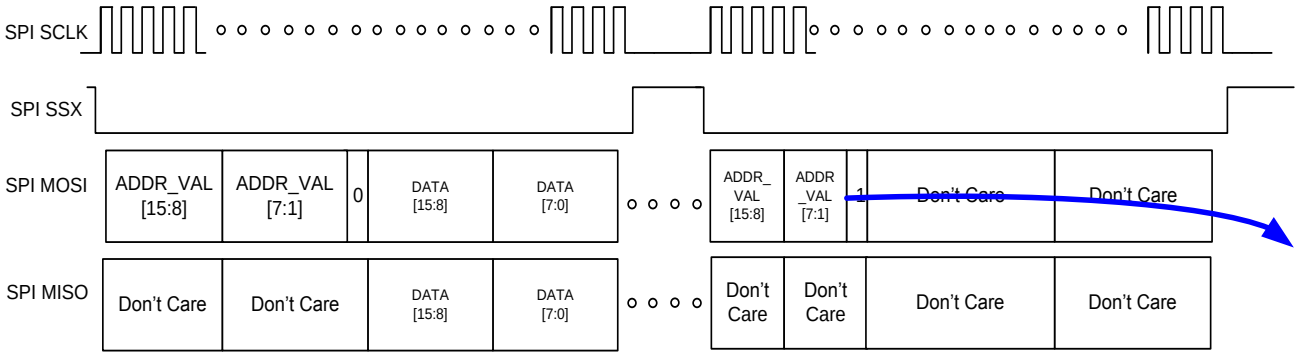

Figure 4-32 Read-after-Write Transfer over SPI

4.11.2.5 NOP-after-Read

In this case, where there is a read alone followed by no more immediate request, the handling of data on MISO and MOSI lines during first frame is similar to the “Back-to-Back reads” case. Data on the MOSI line during first 16 bits (bit slots 31 to 16) in 2nd frame should contain all 1’s to point to a dummy address for SPI and command for the write. Data on the MOSI line during bit slots 15 to 0 in 2nd frame is redundant. Data on the MISO line in 2nd frame corresponds to the TC358746AXBG/TC358748XBG register addressed by the read command in 1st frame. The write on MOSI line in 2nd frame points to a dummy address (all 1’s) and so is redundant.

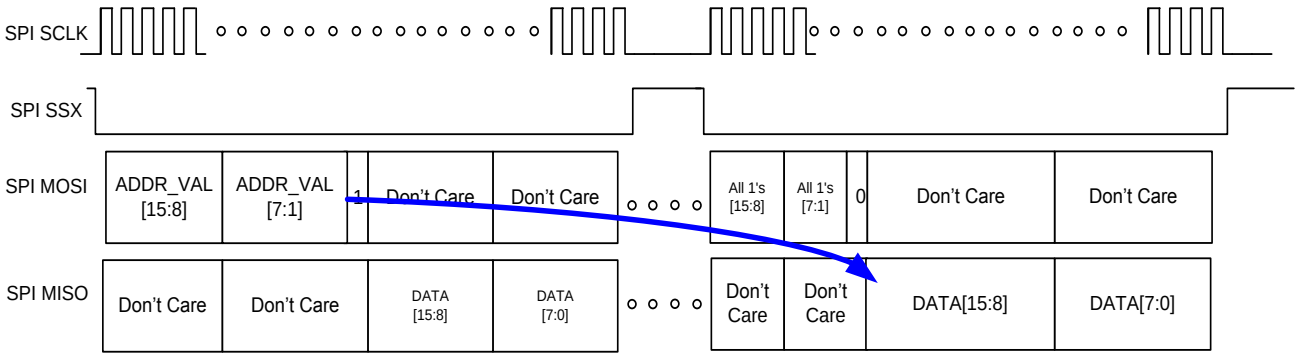

Figure 4-33 NOP-after-Read Transfer over SPI

5 Clock and System

The clock generation unit (CG) makes use of a single PLL and the clock extracted from the camera interface as the source for all other clocks used in TC358746AXBG/TC358748XBG. CG supports threepowers states RESET, FULLY ACTIVE and SLEEP where clocks are disabled or PLL is disabled to reduce power consumption. SLEEP state is controlled by register bit (reg_sleep).

In RESET: PLL is disabled and no clocks are output.
During this state, TC358746AXBG/TC358748XBG will not be able to function.

In FULLY ACTIVE: PLL and TC358746AXBG/TC358748XBG system clock are enabled.
Depending on the configuration, CSI-2 RX, and Parallel port clocks may also be enabled.

In SLEEP: PLL is disabled and no clocks are output.
During this state,

- I2C slave interface is enabled. Application processor can wake up TC358746AXBG/TC358748XBG by program “0” to SLEEP bit (reg_sleep).
- This state may be used by TC358746AXBG/TC358748XBG to safely update PLL parameters when required by the application processor.

5.1 CG Block diagram

The block diagram of CG is shown below. The divisors for each block is controlled by registers ClkCtl and MClkCtl as described in register section.

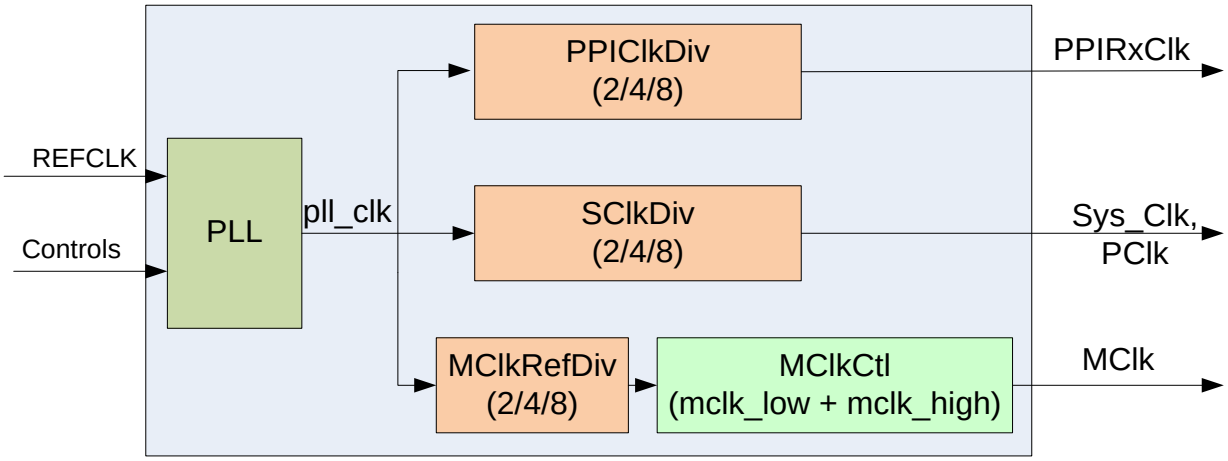

Figure 5-1 CG Block diagram

CG uses an external input clock REFCLK (6MHz to 40 MHz) to generate clocks required by internal controllers and output externally. .

5.2 Example of PLL Generated Clock Frequency

The possible clock frequencies generated from the PLL are achieved by varying the values in registers PLLCtl0 and PLLCtl1.

Pll_clk = RefClk [(FBD + 1)/ (PRD + 1)] * [1 / (2^FRS)]*

Table 5-1 provides possible frequencies that may be used in TC358746AXBG/TC358748XBG.

Table 5-1 Possible PLL parameters

Reference clock (MHz)	FBD	PRD	FRS	pll_clk (MHz)
16.6	255	7	1	265.60
	319	5	2	221.33
	319	6	2	189.71
	319	7	2	166.00

5.3 Output Clocks Generation

PPIRxClk

PPIRxClk is used in CSIRx for detecting CSI Link LP ←→HS transition.

PClk (Parallel Output Clock):

PClk is generated from either pll_clk divides by 2, 4 or 8 options.

Its maximum frequency is 100MHz

CSITxClk

CSITxClk is obtained by dividing pll_clk by 2.

MClk(Reference Clock to Senser):

MClk is generated in two steps.

1) Its source is divided down from Pll_Clk either by 2, 4 or 8 as specified in ClkCtl[MclkRefDiv].
2) The MClkCtl specifies the MClk high and low time counted by the divided down pll_Clk. There are two parameters in register MClkCtl:
   a) reg_mclkh[7:0] contains the mclk HIGH time count (counts with MCLKS). HIGH time has range of 1 to 256 MclkRefclock.
   b) reg_mclkl[7:0] contains the mclk LOW time count (counts with MCLKS). LOW time has range of 1 to 256 MclkRefclock .

Notes: See Registers ClkCtl and MClkCtl for more description

Table 5-2 Controllers' Operating Frequency

Controllers	Operating Frequency		Source
	min (MHz)	max (MHz)	
CSI2 RX controller	10	125	CSI2 RX Byte clock
VB controller (Write port)	10	166	CSI2 RX Byte clock or Input PCLK
VB controller (Read port)	---	125	CSI2RX Byte clock or PLL clock source
Parallel Output controller	---	100	PLL
Parallel Input controller	---	166	Input PCLK
I2C controller	6	40	Input REFCLK
Register module	6	40	Input REFCLK

5.4 TC358746AXBG/TC358748XBG Power Up Procedure

The following sequence should happen before TC358746AXBG/TC358748XBG is able to operate properly:

1. Provide voltage and clock sources to TC358746AXBG/TC358748XBG.
   - Please keep all the input signals at either "Hi-z" or "logic low" state before powering on TC358746AXBG/TC358748XBG.
2. For voltage source, it is desired to turn on core power (1.2) source first, then Analog PHY and IO power as shown in Figure 5-2 Power On Sequence. RefClk can be provided either before or after the de-assertion of RESX as indicated by the dash line.
3. In CSI-2 Tx mode, RefClk can be tie to ground. In this case, PClk/4 will be used to drive PLL, Figure 5-3.
4. The timing parameters for Figure 5-2 and Figure 5-3 are tabulated in Table 5-3.

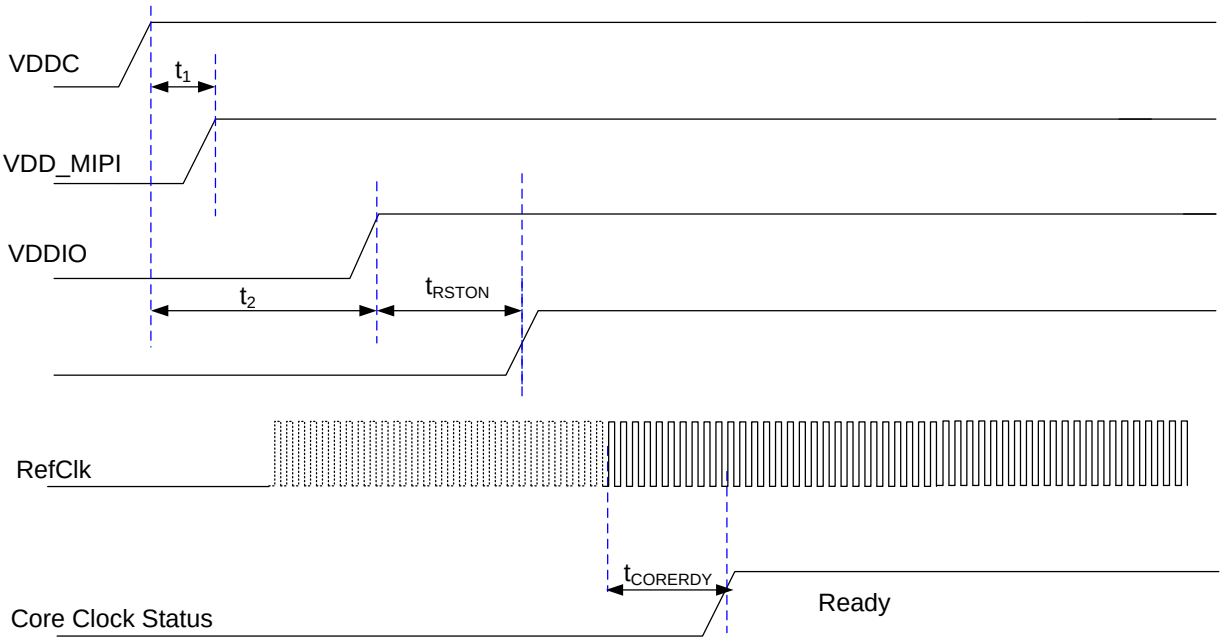

Figure 5-2 Power On Sequence (When RefClk is Available to Drive PLL)

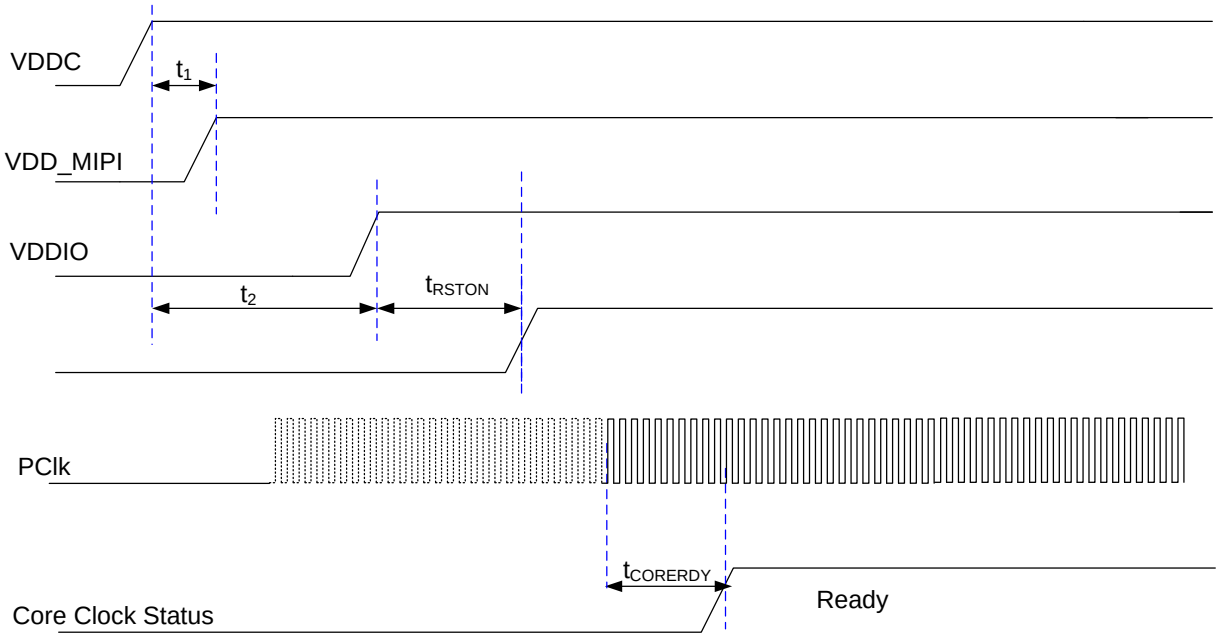

Figure 5-3 Power On Sequence (When PClk is used to Drive PLL in Parallel In Mode)

Table 5-3 Power On Sequence Timing

Parameters	Description	Min.	Typ.	Max.	Units
RefClk	Reference clock frequency	6	---	40	MHz

t_1	VDD_MIPI on delay from VDDC.	0	---	10	msec
t_2	VDDIOon delay from VDDC	0	---	10	msec
t_{RSTON}	RESET width period	200	---	---	nsec
$t_{CORERDY}$	Period after reset de-assertion when TC358746AXBG/TC358748XBG clocks are stable (Dependent on REFCLK frequency)	.7	---	1	msec

5.5 TC358746AXBG/TC358748XBG Power Down Procedure

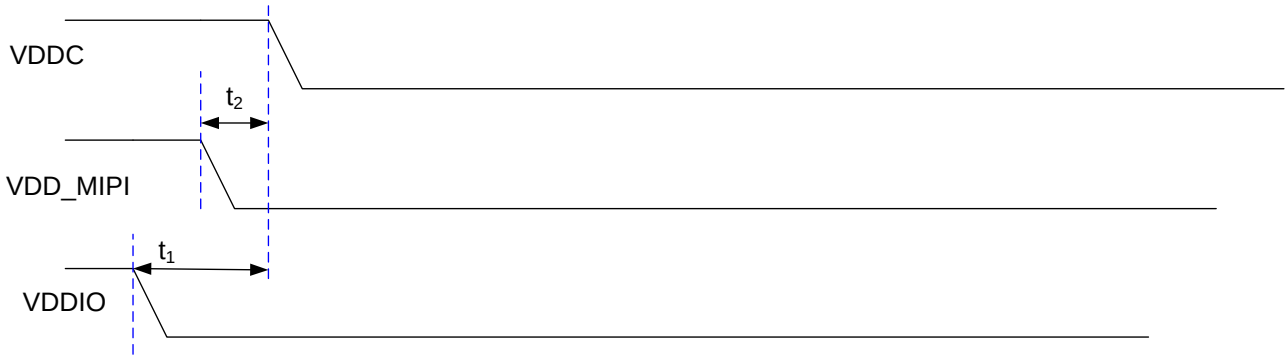

Figure 5-4 Power Down Sequence

Table 5-4 Power Down Sequence Timing

Parameters	Description	Min.	Typ.	Max.	Units
t_1	VDD_MIPI off delay from VDDIOoff	0	---	10	msec
t_2	VDDC off delay from VDD_MIPI off	0	---	10	msec

6 RegFile Block (Reg)

The application processor (ISP) accesses TC358746AXBG/TC358748XBG RegFile block to read status and/or write control registers through the I2C/SPI slave interface.

6.1 Register Map

The control and status registers in TC358746AXBG/TC358748XBG is provided in Table 6-1.

Table 6-1 Register Map

Group	Address	Register	Description
Global (16-bit Address)	0x0000	ChipID	TC358746AXBG/TC358748XBG Chip and Revision ID
	0x0002	SysCtl	System Control Register
	0x0004	ConfCtl	Configuration Control Register
	0x0006	FiFoCtl	FiFo Control Register
	0x0008	DataFmt	Data Format Control Register
	0x000C	MclkCtl	Mclk control register
	0x000E	GPIOEn	GPIO Enable Control Register
	0x0010	GPIODir	GPIO Pin Direction Control Register
	0x0012	GPIOIn	GPIO Input Pin Value
	0x0014	GPIOOut	GPIO Output Pin Value
	0x0016	PLLCtl0	PLL control Register 0
	0x0018	PLLCtl1	PLL control Register 1
	0x0020	CLKCtrl	Clock Control Register
	0x0022	WordCnt	Word Count Register
	0x0032	PP_MISC	Parallel Input Port Miscellaneous Register
	0x0050	CSITX_DT	User Defined CSI Tx Data Type
	0x0056	PHYClkCtl	CSI2RX PHY clock control Register
	0x0058	PHYData0Ctl	CSI2RX PHY data 0 control Register
	0x005A	PHYData1Ctl	CSI2RX PHY data 1 control Register
	0x005C	PHYData2Ctl	CSI2RX PHY data 2 control Register
	0x005E	PHYData3Ctl	CSI2RX PHY data 3 control Register
	0x0060	PHYTimDly	CSI2RXPHY Time delay Register
	0x0062	PHYSta	CSI2RX PHY status Register
	0x0064	CSIStatus	CSI2RX Error status Register
	0x0066	CSIErrEn	CSI2RX Error Enable Register
	0x0068	MDLSynErr	CSI2RX Multi-Data Lane Sync Byte Detected Error Register
	0x006A	CSIDID	CSI2RX data Type ID Register
	0x006C	CSIDIDErr	CSI2RX Data Type ID Error Register
	0x006E	CSIPktLen	CSI2RX data length Register
	0x0070	CSIRX_DPCtl	CSI2RX Dphy control Register
CSI2-RX Status Counters (16-bit Address)	0x0080	FrmErrCnt	CSI2RX Frame error counter
	0x0082	CRCErrCnt	CSI2RX CRC error counter
	0x0084	CorErrCnt	CSI2RX Recoverable Packet Header error counter
	0x0086	HdrErrCnt	CSI2RX Unrecoverable Packet Header error counter
	0x0088	EIDErrCnt	CSI2RX Unsupported Packet ID error counter
	0x008A	CtlErrCnt	CSI2RX Escape Mode error counter
	0x008C	SotErrCnt	CSI2RX Recoverable Sync Byte error counter
	0x008E	SynErrCnt	CSI2RX unrecoverable Sync Byte error counter
	0x0090	MDLErrCnt	CSI2RX Multi-Data Lane Sync Byte error counter
	0x00F8	FIFOStatus	FiFo Underflow/Overflow Status Register
TX	0x0100	CLW_DPHYCONTTX	Clock Lane DPHY Tx Control Register

PHY (32-bit Address)	0x0104	D0W_DPHYCONTTX	Data Lane0 DPHY Tx Control Register
	0x0108	D1W_DPHYCONTTX	Data Lane1 DPHY Tx Control Register
	0x010C	D2W_DPHYCONTTX	Data Lane2 DPHY Tx Control Register
	0x0110	D3W_DPHYCONTTX	Data Lane3 DPHY Tx Control Register
	0x0140	CLW_CNTRL	Clock Lane DPHY Control Register
	0x0144	D0W_CNTRL	Data Lane 0 DPHY Control Register
	0x0148	D1W_CNTRL	Data Lane 1 DPHY Control Register
	0x014C	D2W_CNTRL	Data Lane 2 DPHY Control Register
	0x0150	D3W_CNTRL	Data Lane 3 DPHY Control Register
	0x0204	STARTCNTRL	CSI2-TX Start Control Register
	0x0208	STATUS	CSI2-TX Status Register
	0x0210	LINEINITCNT	CSI2-TX Line Initialization Control Register
	0x0214	LPTXTIMECNT	SYSLPTX Timing Generation Counter
	0x0218	TCLK_HEADERCNT	TCLK_ZERO and TCLK_PREPARE Counter
	0x021C	TCLK_TRAILCNT	TCLK_TRAIL Counter
	0x0220	THS_HEADERCNT	THS_ZERO and THS_PREPARE Counter
	0x0224	TWAKEUP	TWAKEUP Counter
	0x0228	TCLK_POSTCNT	TCLK_POST Counter
	0x022C	THS_TRAILCNT	THS_TRAIL Counter
	0x0230	HSTXVREGCNT	TX Voltage Regulator setup Wait Counter
	0x0234	HSTXVREGEN	Voltage regulator enable for HSTX Data Lanes
TX CTRL (32-bit Address)	0x040C	CSI_CONTROL	CSI2TXControl Register
	0x0410	CSI_STATUS	CSI2TXStatus Register
	0x0414	CSI_INT	CSI2TX – Presents interrupts currently being held
	0x0418	CSI_INT_ENA	CSI2TX – Enables CSI_INT interrupt source
	0x044C	CSI_ERR	CSI2TX – transfer general errors
	0x0450	CSI_ERR_INTENA	CSI2TX – interrupt enable bits of the CSI_ERR register
	0x0454	CSI_ERR_HALT	CSI2TX – stop on error bit set in the CSI_ERR register
	0x0500	CSI_CONFW	CSI TX Configure Write Register
	0x0504	CSI_RESET	CSI2TX – reset he module and the Receive FIFO content
	0x050C	CSI_INT_CLR	CSI2TX – Clears particular bits of the CSI_INT register
	0x0518	CSI_START	CSI2-TX – Starts CSI2-TX operation
Debug Tx (Color Bar, 16-bit Address))	0x00e0	DBG_LCNT	Color Bar Generation Setting for Line Count
	0x00e2	DBG_WIDTH	Color Bar Generation Setting for Line Width
	0x00e4	DBG_VBlank	Color Bar Generation Setting for Vertical Blank lines
	0x00e8	DBG_Data	Color Bar Generation Setting for Data Written into FIFO

6.2 Global Registers

6.2.1 Chip and Revision ID (ChipID: 0x0000)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	ChipID							
Type	RO							
Default	0x44							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	RevID							
Type	RO							
Default	0x1							

Table 6-2 Chip and Revision ID

Register Field	Bit	Default	Description
ChipID	[15:8]	0x44	**Chip ID** Chip ID assigned for this device by Toshiba.
RevID	[7:0]	0x1	**Revision ID** Revision ID for this device assigned by Toshiba.

6.2.1 System Control Register (SysCtl: 0x0002)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved						SLEEP	Sreset
Type	RO						R/W	R/W
Default	0x0						0x1	0x0

Table 6-3 System Control Register

Register Field	Bit	Description
Reserved	[15:2]	
SLEEP	1	**SLEEP** control 0: Normal operation 1: Sleep mode Note: This bit is applicable only in CSI-In ➔ Parallel-Out mode
Sreset	0	**Software Reset (Active high)** This bit is set to force TC358746AXBG/TC358748XBG logic to reset state except all configuration registers content (regFile) and I2C slave module. 0: Normal operation 1: Reset operation Software needs to clear Sreset when set.

6.2.2 Configuration Control Register (ConfCtl: 0x0004)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	TriEn	Reserved	INTE2n	Bt656En	Reserved		PdataF	
Type	R/W	RO	R/W	R/W	RO		R/W	
Default	0x1	0x0	0x0	0x0	0x0		0x0	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	PPEn	VvalidP	HvalidP	PCLKP	Auto	DataLane	

Type	RO	R/W	R/W	R/W	R/W	R/W	R/W
Default	0x0	0x0	0x0	0x0	0x0	0x1	0x0

Table 6-4 Configuration Control Register

Register Field	Bit	Description
TriEn	[15]	**Parallel Out (MSEL = 0) and CS = 1, Tri-State Enable** 0: Disable, parallel port H/Vvalid and PClk are driven 1: Enable, parallel ports, including data, H/Vvalid and PClk are tri-state **Note:** CS needed to be asserted (CS = 0) before programming
Reserved	[14]	**Reserved, please set both bits to "0"**
INTE2n	[13]	**INT Output Enable 2** 0: Normal (Default to GPIO1 function) 1: Enable (output INT to GPIO1)
Bt656En	[12]	**Parallel Input Port BT656 Enable** 0: Disable 1: Enable Note: 1) Only valid when Parallel Input port data format is YUV422 2) Please use PD[9:2] for 8-bit data bus 3) Please make sure bit[5:4] below is set to '0'
Reserved	[11:10]	Reserved
PdataF	[9:8]	**Parallel Data Format Option** 2'b00: Mode 0 2'b01: Mode 1 2'b10: Mode 2 2'b11: Reserved Note: See Table 4-3 and Table 4-4 for more information
Reserved	[7]	Reserved
PPEn	[6]	**Parallel Port Enable** 0: Parallel Port Disable 1: Parallel Port Enable
VvalidP	[5]	**Vvalid Polarity Control** 0: Vvalid active high 1: Vvalid active low
HvalidP	[4]	**Hvalid Polarity Control** 0: Hvalid active high 1: Hvalid active low
PCLKP	[3]	**Parallel Clock (PCLK) Polarity Select** 0: Normal 1: Inverted Note: See Parallel Port Output Timing section for more information. Valid for Parallel port output mode only.
Auto	[2]	**I2C slave index increment** 0: I2C address index does not increment on every data byte transfer 1: I2C address index increments on every data byte transfer
DataLane	[1:0]	**CSI-2 Data Lane Select (CSI2 Rx Only)** Selects the number data lane activated during data transfer 2'b00:1 data lane 2'b01:2 data lanes 2'b10:3 data lanes 2'b11:4 data lanes

6.2.3 FiFo Control Register (FiFoCtl: 0x0006)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							FiFoLevel[8]
Type	RO							R/W
Default	0x0							0x0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	FiFoLevel[7:0]							
Type	R/W							
Default	0x1							

Table 6-5 FiFo Control Register

Register Field	Bit	Description
Reserved	[15:9]	Reserved
FiFo_Level	[8:0]	**FiFo Level** This field determines the FiFo write data level, when reaches to this level FiFo controller asserts FiFoRdy for Parallel portto startoutput data

6.2.4 Data Format Control Register (DataFmt: 0x0008)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	PDFormat				Reserved			UDT_en
Type	R/W				RO			R/W
Default	0x0				0x0			0x0

Table 6-6 Data FormatControl Register

Register Field	Bit	Description
Resserved	[15:8]	Reserved
PDFormat	[7:4]	Peripheral Data Format 0000: RAW8 0001: RAW10 0010: RAW12 0011: RGB888 0100: RGB666 0101: RGB565 0110: YUV422 8-bit 0111: Reserved 1000: RAW14 1001: YUV422 10-bit 1010: YUV444 (Parallel input mode only – CSITX Data Type ID defined in CSITX_DT register) 1011 – 1111: Reserved Notes: For CSIRX: This field used only when Udt_en = 1 For CSITX: This field used for parallel input port
Resserved	[3:1]	Reserved
UDT_en	[0]	User Data Type ID enable 0: CSIRX: use Data Type ID detected from CSI Bus

Register Field	Bit	Description
		CSITX: use Data Type ID defined in PDFormat register bits 1: CSIRX: Use Data Type ID defined PDFormat register bits CSITX: Use Data Type ID defined in CSITX_DT register

6.2.5 MCLK Control Register (MclkCtl: 0x000C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	mclk_high							
Type	R/W							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	mclk_low							
Type	R/W							
Default	0x0							

Table 6-7 MCLK Control Register

Register Field	Bit	Description
mclk_high	[15:8]	Mclk HIGH time count Counts with MclkRef clock (from Register ClkCtl) mclk_high, mclk_low> 0: Mclk logic enable, GPIO[0] outputs MCLK
mclk_low	[7:0]	Mclk LOW time count Counter counts from 0, i.e. 0→ low count = 1 MclkRef Count, 1→ low count = 2 MclkRef Counts, N → low count = N+1MclkRef Counts, 255 → low count = 256 MclkRef Counts Total MClk divider = (mclk_high + 1) + (mclk_low + 1)

6.2.6 GPIO Enable

6.2.7 Register (GPIOEn: 0x000E)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	GPIOEn[15:8]							
type	R/W							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	GPIOEn[7:4]				Reserved			
type	R/W				RO			
Default	0x0				0x0			

Table 6-8 GPIO Direction Register

Register Field	Bit	Description
GPIOEn	[15:4]	**GPIO Enable** 0:Disable (GPIOx function depend on mode of operation) 1: Enable (GPIOx function depend on GPIODir)
Resserved	[3:0]	Reserved

6.2.8 GPIO Direction Register (GPIODir: 0x0010)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	GPIODir[15:8]							
type	R/W							
Default	0xFF							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	GPIODir[7:0]							
type	R/W							
Default	0xFF							

Table 6-9 GPIO Direction Register

Register Field	Bit	Description
GPIODir	[15:0]	**GPIO Pin Direction** 0:GPIO Pin is set to Output Mode 1: GPIO Pin is set to Input Mode

6.2.9 GPIO Pin Value Register (GPIOPin: 0x0012)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	GPIOIn[15:8]							
type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	GPIOIn[11:8]							
type	RO							
Default	0x0							

Table 6-10 GPIO Pin Value Register

Register Field	Bit	Default	Description
GPIOPin	[15:0]	0xX	**GPIO Pin Value**

6.2.10 GPIO Output Value Register (GPIOOut: 0x0014)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	GPIOOut[15:8]							
type	R/W							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	GPIOOut[7:0]							
type	R/W							
Default	0x0							

Table 6-11 GPIO Output Value Register

Register Field	Bit	Default	Description
GPIOOut	[15:0]	0xX	**GPIO Output Register Value**

6.2.11 PLL Control Register 0 (PLLCtl0: 0x0016)

Bit	B15	B14	B13	B12	B11	B10	B9	B8

Name	PLL_PRD				Reserved			PLL_FBD[8]
Type	R/W				RO			R/W
Default	0x4				0x00			0x0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	PLL_FBD[7:0]							
Type	R/W							
Default	0x63							

Table 6-12 PLL Control Register 0

Register Field	Bit	Description
PLL_PRD	[15:12]	Input divider setting Division ratio = (PRD3..0) + 1
Reserved	[11:9]	
PLL_FBD	[8:0]	Feedback divider setting Division ratio = (FBD8…0) + 1

6.2.12 PLL Control Register 1 (PLLCtl1: 0x0018)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				PLL_FRS		PLL_LBWS	
Type	RO				R/W		R/W	
Default	0x0				0x1		0x2	
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Revsd	LFBREN	BYPCKEN	CKEN	Reserved		RESETB	PLL_EN
Type	RO	R/W	R/W	R/W	RO		R/W	R/W
Default	0x0	0x0	0x0	0x0	0x0		0x0	0x0

Table 6-13 PLL Control Register 1

Register Field	Bit	Description
Reserved	[15:12]	
PLL_FRS	[11:10]	Frequency range setting (post divider) for HSCK frequency 2'b00: 500MHz – 1GHz HSCK frequency 2'b01: 250MHz – 500MHz HSCK frequency 2'b10: 125 MHz – 250MHz HSCK frequency 2'b11: 62.5MHz – 125MHz HSCK frequency
PLL_LBWS	[9:8]	Loop bandwidth setting 2'b00: 25% of maximum loop bandwidth 2'b01: 33% of maximum loop bandwidth 2'b10: 50% of maximum loop bandwidth (default) 2'b11: maximum loop bandwidth
Reserved	[7]	
PLL_LFBREN	[6]	Lower Frequency Bound Removal Enable 1'b0: REFCLK toggling –> normal operation, REFCLK stops -> no oscillation 1'b1: REFCLK toggling -> normal operation, REFLCK stops -> free running PLL
PLL_BYPCKEN	[5]	Bypass clock enable 1'b0: Normal operation 1'b1: bypass mode, REFCLK is used instead of PLL_VCO output
PLL_CKEN	[4]	Clock enable 1'b0: clocks switched off (output LOW) 1'b1: clocks switched on

Reserved	[3:2]	
PLL_RESETB	[1]	PLL Reset 1'b0: Reset 1'b1: Normal operation
PLL_EN	[0]	PLL Enable 1'b0: PLL off 1'b1: PLL on

6.2.13 CLK Control Register (ClkCtl: 0x0020)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved		PPIclkDiv		MclkRefDiv		SclkDiv	
Type	RO		R/W		R/W		R/W	
Default	0x0		0x2		0x0		0x0	

Table 6-14 CLK Control Register 1

Register Field	Bit	Description
Reserved	[15:6]	
PPIclkDiv	[5:4]	PPI Output Divider Selection 2'b00: ppi_clk = PLL_CLK DIV 8 2'b01: ppi_clk = PLL_CLK DIV 4 2'b10: ppi_clk = PLL_CLK DIV 2 2'b11: Reserved Note: ppi_clk clock frequency range must be between 66 – 125MHz
MclkRefDiv	[3:2]	MclkRef Output Divider Selection 2'b00: MclkRef = PLL_CLK DIV 8 2'b01: MclkRef = PLL_CLK DIV 4 2'b10: MclkRef = PLL_CLK DIV 2 2'b11: Reserved Note: MclkRef clock frequency can not be greater than 125 MHz
SclkDiv	[1:0]	Sys_clk Output Divider Selection (same as parallel output clock, PClk) 2'b00: sys_clk = PLL_CLK DIV 8 2'b01: sys_clk = PLL_CLK DIV 4 2'b10: sys_clk = PLL_CLK DIV 2 2'b11: Reserved Note: sys_clk clock frequency cannot be greater than 100 MHz

Please refer to Figure 5-1 for clarification.

6.2.14 Word Count Register (WordCnt: 0x0022)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	WordCnt[15:8]							
Type	R/W							
Default	0x01							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	WordCnt[7:0]							

Type	R/W
Default	0x00

Table 6-15 Word Count Register

Register Field	Bit	Description
WordCnt	[15:0]	**Word Count** Defined total number of byte for each line.

6.2.15 Parallel In Miscellaneous Register (PP_MISC)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	FrmStop	RstPtr	Reserved					
Type	R/W	R/W	RO					
Default	0x0	0x0	0x00					
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved							
Type	RO							
Default	0x00							

Table 6-16 CSI TX Data Type Register

Register Field	Bit	Description
FrmStop	15	**Frame Stop** When this bit is asserted, TC358746A will stop outputting at the next Vvalid
RstPtr	14	**Reset Pointers** When this bit is asserted, TC358746A resets its write/read pointers to Video Buffer
Reserved	[13:0]	

Please refer to section 4.6.1 for the usage of bits [15:14].

6.2.16 User Data Type Register (CSITX_DT: 0x0050)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	CSITX_DT[7:0]							
Type	R/W							
Default	0x30							

Table 6-17 User Defined CSITX Data Type Register

Register Field	Bit	Default	Description
CSITX_DT	[7:0]	0x30	CSITX Data Type ID, from CSI-2 Spec. This field is used for CSITX Data Type ID when DataFmt[UDT_en] = 1;

6.3 Rx Control Registers

6.3.1 MIPI PHYClock Lane Control Register (PHYClkCtl: 0x0056)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Cap		HsRxRs		ClkDly			
Type	R/W		R/W		R/W			
Default	0x0		0x2		0x0			

Table 6-18 MIPI PHYClock Control Register

Register Field	Bit	Description
Reserved	[15:8]	Reserved
Cap	[7:6]	**Selection of Capacitance** 00: no additional capacitance 01: 2.4pF additional capacitance 10: 2.6pF additional capacitance 11: 2.8pF additional capacitance
HsRxRs	[5:4]	**Selection of HSRX bias resistance** 2'b00: 1.5k 2'b01: 1.75k 2'b10: 2.00k 2'b11: 2.25 k
ClkDly	[3:0]	**Clock skew control** This field may be used to control data lane 0 skew in Rx. Skew delay = ClkDlyx 25ps

6.3.2 MIPI PHY Data Lane 0 Control Register (PHYData0Ctl: 0x0058)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Cap		HsRxRs		DataDly			
Type	R/W		R/W		R/W			
Default	0x0		0x2		0x0			

Table 6-19 MIPI PHY Data Lane 0 Control Register

Register Field	Bit	Description
Reserved	[15:8]	Reserved
Cap	[7:6]	**Selection of Capacitance** 00: no additional capacitance 01: 2.4pF additional capacitance 10: 2.6pF additional capacitance 11: 2.8pF additional capacitance
HsRxRs	[5:4]	**Selection of HSRX bias resistance** 2'b00: 1.5k 2'b01: 1.75k 2'b10: 2.00k 2'b11: 2.25 k
DataDly	[3:0]	**Data skew control** This field may be used to control data lane 0 skew in Rx. Skew delay = DataDlyx 25ps

6.3.3 MIPI PHY Data Lane 1 Control Register (PHYData1Ctl: 0x005A)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Cap		HsRxRs		DataDly			
Type	R/W		R/W		R/W			
Default	0x0		0x2		0x0			

Table 6-20 MIPI PHY Data Lane 1 Control Register

Register Field	Bit	Description
Reserved	[15:8]	Reserved
Cap	[7:6]	**Selection of Capacitance** 00: no additional capacitance 01: 2.4pF additional capacitance 10: 2.6pF additional capacitance 11: 2.8pF additional capacitance
HsRxRs	[5:4]	**Selection of HSRX bias resistance** 2'b00: 1.5k 2'b01: 1.75k 2'b10: 2.00k 2'b11: 2.25 k
DataDly	[3:0]	**Data skew control** This field may be used to control data lane 1 skew in Rx. Skew delay = DataDlyx 25ps

6.3.4 MIPI PHY Data Lane 2 Control Register (PHYData2Ctl: 0x005C)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Cap		HsRxRs		DataDly			
Type	R/W		R/W		R/W			
Default	0x0		0x2		0x0			

Table 6-21 MIPI PHY Data Lane 2Control Register

Register Field	Bit	Description
Reserved	[15:8]	Reserved
Cap	[7:6]	**Selection of Capacitance** 00: no additional capacitance 01: 2.4pF additional capacitance 10: 2.6pF additional capacitance 11: 2.8pF additional capacitance
HsRxRs	[5:4]	**Selection of HSRX bias resistance** 2'b00: 1.5k 2'b01: 1.75k 2'b10: 2.00k 2'b11: 2.25 k
DataDly	[3:0]	**Data skew control** This field may be used to control data lane 2 skew in Rx. Skew delay = DataDlyx 25ps

6.3.5 MIPI PHY Data Lane 3 Control Register (PHYData3Ctl: 0x005E)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Cap		HsRxRs		DataDly			

Type	R/W	R/W	R/W
Default	0x0	0x2	0x0

Table 6-22 MIPI PHY Data Lane 3 Control Register

Register Field	Bit	Description
Reserved	[15:8]	Reserved
Cap	[7:6]	**Selection of Capacitance** 00: no additional capacitance 01: 2.4pF additional capacitance 10: 2.6pF additional capacitance 11: 2.8pF additional capacitance
HsRxRs	[5:4]	**Selection of HSRX bias resistance** 2'b00: 1.5k 2'b01: 1.75k 2'b10: 2.00k 2'b11: 2.25 k
DataDly	[3:0]	**Data skew control** This field may be used to control data lane 3 skew in Rx. Skew delay = DataDlyx 25ps

6.3.6 MIPI PHY Time Delay Register (PHYTimDly: 0x0060)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Tc_term_sel	Reserved						
Type	R/W	R/W						
Default	0x0	0xXX						
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Td_term_sel	DSettle						
Type	R/W	R/W						
Default	0x0	0x05						

Table 6-23 MIPI PHY Time Delay Register

Register Field	Bit	Description
Tc_term_sel	15	**TC TERM selection** Please set this bit to '1'
Reserved	[14:8]	
Td_term_sel	7	**TD TERM selection** 0: Data HS termination after (2, 3)*PPIRxClk when LP to HS transition 1: Data HS termination set immediately when LP to HS transition (preferred)
DSettle	[6:0]	**THS-SETTLE timer** This field may be used to control the delay between LP to HS transition 0x00-0x7f: valid Delay = (dsettle+1) x PPIRXCLK

6.3.7 MIPI PHY Status Register (PHYSta: 0x0062)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
type	RO							
Default								
Bit	B7	B6	B5	B4	B3	B2	B1	B0

Name	SoTErr3	SynErr3	SoTErr2	SynErr2	SoTErr1	SynErr1	SoTErr0	SynErr0
type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Table 6-24 MIPI PHY Error Status Register

Register Field	Bit	Description
Reserved	[15:8]	Reserved
SoTErr3	[7]	**Recoverable SyncByte error data lane 3** This bit is set to indicate that a SyncByte was received with correctable errors during HS transmission. This bit is set by Rx PPI data lane 3. 0: no error reported 1: error occurred This bit is cleared when software clears SotErr.
SynErr3	[6]	**Un-recoverable SyncByte Error data lane 3** This bit is set to indicate that a SyncByte was received with uncorrectable errors. This bit is set by Rx PPI data lane 3. 0: no error reported 1: error occurred This bit is cleared when software clears SynErr.
SoTErr2	[5]	**Recoverable SyncByte error data lane 2** This bit is set to indicate that a SyncByte was received with correctable errors during HS transmission. This bit is set by Rx PPI data lane 2. 0: no error reported 1: error occurred This bit is cleared when software clears SotErr.
SynErr2	[4]	**Un-recoverable SyncByte Error data lane 2** This bit is set to indicate that a SyncByte was received with uncorrectable errors. This bit is set by Rx PPI data lane 2. 0: no error reported 1: error occurred This bit is cleared when software clears SynErr.
SoTErr1	[3]	**Recoverable SyncByte error data lane 1** This bit is set to indicate that a SyncByte was received with correctable errors during HS transmission. This bit is set by Rx PPI data lane 1. 0: no error reported 1: error occurred This bit is cleared when software clears SotErr.
SynErr1	[2]	**Un-recoverable SyncByte Error data lane 1** This bit is set to indicate that a SyncByte was received with uncorrectable errors. This bit is set by Rx PPI data lane 1. 0: no error reported 1: error occurred This bit is cleared when software clears SynErr.
SoTErr0	[1]	**Recoverable SyncByte error data lane 0** This bit is set to indicate that a SyncByte was received with correctable errors during HS transmission. This bit is set by Rx PPI data lane 0. 0: no error reported 1: error occurred This bit is cleared when software clears SotErr.
SynErr0	[0]	**Un-recoverable SyncByte Error data lane 0** This bit is set to indicate that a SyncByte was received with uncorrectable errors. This bit is set by Rx PPI data lane 0.

Register Field	Bit	Description
		0: no error reported 1: error occurred This bit is cleared when software clears SynErr.

6.3.8 CSI-2 Error Status Register (CSIStatus: 0x0064)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							MDLErr
Type	RO							R/W1C
Default	0x0							0x0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	FrmErr	CRCErr	CorErr	HdrErr	EIDErr	CtlErr	SoTErr	SynErr
Type	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C	R/W1C
Default	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Table 6-25 CSI-2 Error Status Register

Register Field	Bit	Description
Reserved	[15:9]	Reserved
MDLErr	8	**Multi-Data Lane Sync Byte Error** This bit is set when Sync Bytes are Not received in the same ByteClk cycle for all the active data lanes. 0: no error occurred 1: error occurred Software may clear this bit by writing 1 to this field
FrmErr	7	**Frame Error** This bit is set when an un-expected Frame start or Frame end short packet is received. This bit is set by CSI-2 Low Level Protocol (LLP). 0: no error occurred 1: error occurred Software may clear this bit by writing 1 to this field
CRCErr	6	**CRC Error** This bit is set for crc error detected when receiving data packets. This bit is set by LLP. 0: no error occurred 1: error occurred Software may clear this bit by writing 1 to this field
CorErr	5	**Recoverable Packet header Error** This bit is set when a packet header is received with errors that cannot be corrected by the transmitted ECC. This bit is set by LLP. 0: no error occurred 1: error occurred Software may clear this bit by writing 1 to this field
HdrErr	4	**Un-recoverable Packet header Error** This bit is set when a packet header is received with errors that can be corrected by the transmitted ECC. This bit is set by LLP. 0: no error occurred 1: error occurred Software may clear this bit by writing 1 to this field
EIDErr	3	**Un-supported Packet ID Error** This bit is set when an unsupported Data type ID (i.e. the Data type ID is neither a supported CSI Data ID, nor specified in EB0Typ, EB1Typ or

Register Field	Bit	Description
		EB2Typ) is received. This bit is set by LLP. 0: no error occurred 1: error occurred Software may clear this bit by writing 1 to this field
CtlErr	2	**Control Error** This signal is asserted when an incorrect line state sequence is detected. This bit is set by Rx PPI. 0: no error reported 1: error occurred Software may clear this bit by writing 1 to this field
SoTErr	1	**Recoverable SyncByte error** This bit is set when either SoTErr3/2/1/0 is set. 0: no error reported 1: error occurred Software may clear this bit by writing 1 to this field.
SynErr	0	**Un-recoverable SyncByte Error** This bit is set when either SynErr3/2/1/0 is set. 0: no error reported 1: error occurred Software may clear this bit by writing 1 to this field.

6.3.9 CSI-2 Error Enable Register (CSIErrEn: 0x0066)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							MDLEn
Type	RO							R/W
Default	0x0							0x0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	FrmEn	CRCEn	CorEn	HdrEn	EIDEn	CtlEn	SoTEn	SynEn
type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0

Table 6-26 CSI-2 Error Enable Register

Register Field	Bit	Description
Reserved	[15:9]	Reserved
MDLEn	8	**MDL Error Enable** Setting this bit enables CSI-2 Rx block to assert CSIErr (to ISP) when MDLErr occurs. 0: do not assert CSIErr if MDLErr occurs 1:assert CSIErr if MDLErr occurs
FrmEn	7	**Frame Error Enable** Setting this bit enables CSI-2 Rx block to assert CSIErr (to ISP) when FrmErr occurs. 0: do not assert CSIErr if FrmErr occurs 1:assert CSIErr if FrmErr occurs
CRCEn	6	**CRC Error Enable** Setting this bit enables CSI-2 Rx block to assert CSIErr (to ISP) when CRCErr occurs. 0: do not assert CSIErr if CRCErr occurs 1:assert CSIErr if CRCErr occurs
CorEn	5	**Recoverable Packet header Error Enable**

Register Field	Bit	Description
		Setting this bit enables CSI-2 Rx block to assert CSIErr (to ISP) when CorErr occurs. 0: do not assert CSIErr if CorErr occurs 1:assert CSIErr if CorErr occurs
HdrEn	4	**Un-recoverable Packet header Error Enable** Setting this bit enables CSI-2 Rx block to assert CSIErr (to ISP) when HdrErr occurs. 0: do not assert CSIErr if HdrErr occurs 1:assert CSIErr if HdrErr occurs
EIDEn	3	**Un-supported Packet ID Error Enable** Setting this bit enables CSI-2 Rx block to assert CSIErr (to ISP) when EIDErr occurs. 0: do not assert CSIErr if EIDErr occurs 1:assert CSIErr if EIDErr occurs
CtlEn	2	**Control Error Enable** Setting this bit enables CSI-2 Rx block to assert CSIErr (to ISP) when CtlErr occurs. 0: do not assert CSIErr if CtlErr occurs 1:assert CSIErr if CtlErr occurs
SoTEn	1	**Recoverable SyncByte error Enable** Setting this bit enables CSI-2 Rx block to assert CSIErr (to ISP) when SoTErr occurs. 0: do not assert CSIErr if SoTErr occurs 1:assert CSIErr if SoTErr occurs
SynEn	0	**Un-recoverable SyncByte Error Enable** Setting this bit enables CSI-2 Rx block to assert CSIErr (to ISP) when SynErr occurs. 0: do not assert CSIErr if SynErr occurs 1:assert CSIErr if SynErr occurs

6.3.10 CSI-2 Multi-Data Lane SyncByte Error Register (MDLSynErr: 0x0068)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved				Sync3	Sync2	Sync1	Sync0
Type	RO				R/W	R/W	R/W	R/W
Default	0x0				0x0	0x0	0x0	0x0

Table 6-27 CSI-2 Multi-Data Lane Sync Byte Error Register

Register Field	Bit	Description
Reserved	[15:4]	Reserved
Sync3	3	**Data Lane 3 Sync Byte Detected** Data lane 3 Sync byte detected status. CSIStatus[MDLErr] is asserted when this bit is set. SW needs to clear this bit by writing '0'. 0: Data lane not active or No Sync Byte detected 1: Sync Byte Detected

Register Field	Bit	Description
Sync2	2	**Data Lane 2 Sync Byte Detected** Data lane 2 Sync byte detected status. CSIStatus[MDLErr] is asserted when this bit is set. SW needs to clear this bit by writing '0'. 0: Data lane not active or No Sync Byte detected 1: Sync Byte Detected
Sync1	1	**Data Lane 1 Sync Byte Detected** Data lane 1 Sync byte detected status. CSIStatus[MDLErr] is asserted when this bit is set. SW needs to clear this bit by writing '0'. 0: Data lane not active or No Sync Byte detected 1: Sync Byte Detected
Sync0	0	**Data Lane 0 Sync Byte Detected** Data lane 0 Sync byte detected status. CSIStatus[MDLErr] is asserted when this bit is set. SW needs to clear this bit by writing '0'. 0: Data lane not active or No Sync Byte detected 1: Sync Byte Detected

6.3.11 CSI-2 Data Type ID Register (CSIDID: 0x006A)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
type	RO							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	DataType							
type	RO							
Default	0xX							

Table 6-28 CSI-2 Data Type ID Register

Register Field	Bit	Description
Reserved	[15:8]	Reserved
DataType	[7:0]	**Data Type ID** This field indicates the type of HS packet that was received by Rx. Listed below is the CSI-2 Spec. defined data type ID supported by TC358746AXBG/TC358748XBG 0x00 Frame Start Code 0x01 Frame End Code 0x02 - 0x11 Reserved 0x12 Embedded 8-bit non-Image Data 0x13 - 0x1D Reserved 0x1E YUV422 8-bit 0x1F - 0x21 Reserved 0x22 RGB565 0x23 RGB666 0x24 RGB888 0x25 – 0x29 Reserved 0x2A RAW8 0x2B RAW10 0x2C RAW12 0x2D RAW14 0x2E - 0x2F Reserved 0x30 User Defined 8-bit Data Type 1

Register Field	Bit	Description
		0x31 User Defined 8-bit Data Type 2 0x32 User Defined 8-bit Data Type 3 0x33 User Defined 8-bit Data Type 4 0x34 User Defined 8-bit Data Type 5 0x35 User Defined 8-bit Data Type 6 0x36 User Defined 8-bit Data Type 7 0x37 User Defined 8-bit Data Type 8

6.3.12 CSI-2Data Type ID Error Register (CSIDIDErr: 0x006C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
type	RO							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	ErrType							
type	RO							
Default	0x00							

Table 6-29 CSI-2 Data Type ID Error Register

Register Field	Bit	Description
Reserved	[15:8]	Reserved
ErrType	[7:0]	**Error Data Type** This field copies/latches the value of CSIDatTyp[DataType] when error bit CSIStatus[EIDErr] is asserted. SW needs to clear this field by writing “0x00” to it.

6.3.13 CSI-2 Data Length Register (CSIPktLen: 0x006E)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	PktLen							
type	RO							
Default	0xX							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	PkLen							
type	RO							
Default	0xX							

Table 6-30 CSI-2 Data Length Register

Register Field	Bit	Description
PktLen	[15:0]	**Data length** This field contains the data length including 4 crc bytes that was received by CSI-2 Rx. This field is set by LLP when CRC error is received.

6.3.14 CSI-2 DPhy Control Register (CSIRX_DPCtl: 0x0070)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						rxck_cntrl	
type	RO						R/W	
Default	0x0						0x0	
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**

Name	rxch3_cntrl	rxch2_cntrl	rxch1_cntrl	rxch0_cntrl
type	R/W	R/W	R/W	R/W
Default	0x0	0x0	0x0	0x0

Table 6-31 CSI-2 Data Length Register

Register Field	Bit	Description
Reserved	[15:10]	Reserved
rxck_cntrl	[9:8]	Clock Dphy Control parameters
rxch3_cntrl	[7:6]	Data Lane 3Dphy Control parameters
rxch2_cntrl	[5:4]	Data Lane 2Dphy Control parameters
rxch1_cntrl	[3:2]	Data Lane 1Dphy Control parameters
rxch0_cntrl	[1:0]	Data Lane 0Dphy Control parameters

6.4 Rx StatusRegisters

6.4.1 Frame Error Counter (FrmErrCnt: 0x0080)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
type	RO							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	FrmErrCnt							
Type	R/W							
Default	0x0							

Table 6-32 Frame Error Counter

Register Field	Bit	Description
Reserved	[15:8]	Reserved
FrmErrCnt	[7:0]	**Frame Error counter** This field is incremented when an un-expected Frame start or Frame end short packet is received. This field is incremented by LLP. 0: no errors 0x1-0xFF: error count The counter does not wrap around and retains the maximum value until cleared by software.

6.4.2 CRC Error Counter (CRCErrCnt: 0x0082)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
type	RO							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	CRCErrCnt							
Type	R/W							
Default	0x0							

Table 6-33 CRC Error Counter

Register Field	Bit	Description

Register Field	Bit	Description
Reserved	[15:8]	Reserved
CRCErrCnt	[7:0]	**CRC Error Counter** This counter is incremented by LLP when a HS packet is received with crc errors. 0: no errors 0x1-0xFF: error count The counter does not wrap around and retains the maximum value until cleared by software.

6.4.3 Recoverable Packet Header Error Counter (CorErrCnt: 0x0084)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	CorErrCnt							
Type	R/W							
Default	0x0							

Table 6-34 Recoverable Packet Header Error Counter

Register Field	Bit	Description
Reserved	[15:8]	Reserved
CorErrCnt	[7:0]	**Recoverable Packet Header Error Counter** This counter is incremented by LLP when a HS packet header is received with errors that are correctable by ECC. 0: no errors 0x1-0xFF: error count The counter does not wrap around and retains the maximum value until cleared by software.

6.4.4 Un-recoverable Packet Header Error Counter (HdrErrCnt: 0x0086)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
type	RO							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	HdrErrCnt							
Type	R/W							
Default	0x0							

Table 6-35 Un-recoverable Packet Header Error Counter

Register Field	Bit	Description
Reserved	[15:8]	Reserved
HdrErrCnt	[7:0]	**Un-recoverable Packet Header Error Counter** This counter is incremented by LLP when a HS packet header is received with errors that are not correctable by ECC. 0: no errors 0x1-0xFF: error count The counter does not wrap around and retains the maximum value until

Register Field	Bit	Description
		cleared by software.

6.4.5 Un-supported Packet ID Error Counter (EIDErrCnt: 0x0088)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	EIDErrCnt							
Type	R/W							
Default	0x0							

Table 6-36 Un-supported Packet ID Error Counter

Register Field	Bit	Description
Reserved	[15:8]	Reserved
EIDErrCnt	[7:0]	**Un-supported Packet ID Error Counter** This counter is incremented by LLP when a HS packet that is not supported by CSI-2 Rx is received. 0: no errors 0x1-0xFF: error count The counter does not wrap around and retains the maximum value until cleared by software.

6.4.6 ControlError Counter (CtlErrCnt: 0x008A)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
type	RO							
Default	0x0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	CtlErrCnt							
Type	R/W							
Default	0x0							

Table 6-37 Escape Mode Error Counter

Register Field	Bit	Description
Reserved	[15:8]	Reserved
CtlErrCnt	[7:0]	**Control Error Counter** This counter is incremented when escape mode is exited using the wrong sequence. 0: no errors 0x1-0xFF: error count The counter does not wrap around and retains the maximum value until cleared by software.

6.4.7 Recoverable SyncByte Error Counter (SoTErrCnt: 0x008C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							

Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	SotErrCnt							
type	R/W							
Default	0x0							

Table 6-38 Recoverable Sync Byte Error Counter

Register Field	Bit	Description
Reserved	[15:8]	Reserved
SotErrCnt	[7:0]	**Recoverable Sync Byte Error Counter** This counter is incremented when a HS Sync Byte was received by Rx PPI with correctable errors. 0: no errors 0x1-0xFF: error count The counter does not wrap around and retains the maximum value until cleared by software.

6.4.8 Un-recoverable SyncByte Error Counter (SynErrCnt: 0x008E)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
type	RO							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	SynErrCnt							
type	R/W							
Default	0x0							

Table 6-39 Un-recoverable Sync Byte Error Counter

Register Field	Bit	Description
Reserved	[15:8]	Reserved
SynErrCnt	[7:0]	**Un-recoverable Sync Byte Error Counter** This counter is incremented when a HS Sync Byte was received by Rx PPI with uncorrectable errors. 0: no errors 0x1-0xFF: error count The counter does not wrap around and retains the maximum value until cleared by software.

6.4.9 Multi-Data Lane SyncByte Error Counter (MDLErrCnt: 0x0090)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
type	RO							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	MDLErrCnt							
type	R/W							
Default	0x0							

Table 6-40 Multi-Data Lane Sync Byte Error Counter

Register Field	Bit	Description

Register Field	Bit	Description
Reserved	[15:8]	Reserved
MDLErrCnt	[7:0]	**Multi-Data Lane Sync Byte Error Counter** This counter is incremented when HS Sync Bytes were not received at the same clock cycle by CSI2 Rx PPI. 0: no errors 0x1-0xFF: error count The counter does not wrap around and retains the maximum value until cleared by software.

6.4.10 FIFO Status Register(FIFOSTATUS: 0x00F8)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x00							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved						Vb_uflow	Vb_oflow
Type	RO						RO	RO
Default	0x00						0x0	0x0

Table 6-41 FIFO Status Register

Register Field	Bit	Default	Description
Reserved	[15:2]		
vb_uflow	1	0	VB Under Flow Status 0: Normal 1: Under flow Read this register will clear the status
vb_oflow	0	0	VB Over Flow Status 0: Normal 1: Over flow Read this register will clear the status

6.5 Tx D-PHY Registers

6.5.1 Clock Lane DPHY TX Control register (CLW_DPHYCONTTX: 0x0100)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						CLW_CAP1	CLW_CAP0
Type	RO	RO	RO	RO	RO	RO	R/W	R/W
Default	0	0	0	0	0	0	1	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	DLYCNTRL3	DLYCNTRL2	DLYCNTRL1	DLYCNTRL0	Reserved		CLW_LPTXCURR1EN	CLW_LPTXCURR0EN
Type	R/W	R/W	R/W	R/W	RO	RO	R/W	R/W
Default	0	0	0	0	0	0	1	0

Table 6-42 Clock Lane DPHY TX Control register

Register Field	Bit	Description

Register Field	Bit	Description
Reserved	[31:10]	
CLW_CAP1	[9]	Selection bit 1 of different HSTX output capacitors for Clock Lane
CLW_CAP0	[8]	Selection bit 0 of different HSTX output capacitors for Clock Lane (CAP1,CAP0): = (00): 0 [pF] (CAP1,CAP0): = (01): 2.8 [pF] (CAP1,CAP0): = (10): 3.2 [pF] (CAP1,CAP0): = (11): 3.6 [pF]
DLYCNTRL[3:0]	[7:4]	Tuning of transmit window position. The High Speed Clock output can be delayed according to the setting. The recommended value is determined by evaluating the LSI in which this module is implemented. Typical delay for rising/falling edge is about DLYCNTRL x 24ps/27ps. Rising edge : DLYCNTRL x 24ps, Falling edge : DLYCNTRL x 27ps.
Reserved	[3:2]	
CLW_LPTXCURR1EN	[1]	Selection bit-1 for LPTX output current (TRLP/TFLP tuning) for clock Lane
CLW_LPTXCURR0EN	[0]	Selection bit-0 for LPTX output current (TRLP/TFLP tuning) for clock Lane 00: no additional output current 01: 25% additional output current 10: 25% additional output current 11: 50% additional output current The default value is “10”. However, if “00” is set, the rise/fall time will become later and if “11” is set, the rise/fall time will become earlier.

6.5.2 Data Lane 0 DPHY TX Control register (D0W_DPHYCONTTX:0x0104)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						D0W_CAP1	D0W_CAP0
Type	RO	RO	RO	RO	RO	RO	R/W	R/W
Default	0	0	0	0	0	0	1	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	DLYCNTRL3	DLYCNTRL2	DLYCNTRL1	DLYCNTRL0	Reserved	Reserved	D0W_LPTXCURR1EN	D0W_LPTXCURR0EN
Type	R/W	R/W	R/W	R/W	RO	RO	R/W	R/W
Default	0	0	0	0	0	0	1	0

Table 6-43 Data Lane 0 DPHY TX Control register

Register Field	Bit	Description
Reserved	[31:10]	
D0W_CAP1	[9]	Selection bit 1 of different HSTX output capacitors for Data Lane 0.

Register Field	Bit	Description
D0W_CAP0	[8]	Selection bit 0 of different HSTX output capacitors for Data Lane 0. (CAP1,CAP0): = (00): 0 [pF] (CAP1,CAP0): = (01): 2.8 [pF] (CAP1,CAP0): = (10): 3.2 [pF] (CAP1,CAP0): = (11): 3.6 [pF]
DLYCNTRL[3:0]	[7:4]	Tuning of transmit window position. The High Speed Data output can be delayed according to the setting. The recommended value is determined by evaluating the LSI in which this module is implemented. Typical delay for rising/falling edge is about DLYCNTRL x 24ps/27ps. Rising edge : DLYCNTRL x 24ps, Falling edge : DLYCNTRL x 27ps.
Reserved	[3:2]	
D0W_LPTXCURR1EN	[1]	Selection bit-1 for LPTX output current (TRLP/TFLP tuning) for Data Lane 0.
D0W_LPTXCURR0EN	[0]	Selection bit-0 for LPTX output current (TRLP/TFLP tuning) for Data Lane 0. 00: no additional output current 01: 25% additional output current 10: 25% additional output current 11: 50% additional output current The default value is “10”. However, if “00” is set, the rise/fall time will become later and if “11” is set, the rise/fall time will become earlier.

6.5.3 Data Lane 1 DPHY TX Control Register (D1W_DPHYCONTTX: 0x0108)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						D1W_CAP1	D1W_CAP0
Type	RO	RO	RO	RO	RO	RO	R/W	R/W
Default	0	0	0	0	0	0	1	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	DLYCNTRL3	DLYCNTRL2	DLYCNTRL1	DLYCNTRL0	Reserved		D1W_LPTXCURR1EN	D1W_LPTXCURR0EN
Type	R/W	R/W	R/W	R/W	RO	RO	R/W	R/W
Default	0	0	0	0	0	0	1	0

Table 6-44 Data Lane 1 DPHY TX Control Register

Register Field	Bit	Description
Reserved	[31:10]	
D1W_CAP1	[9]	Selection bit 1 of different HSTX output capacitors for Data Lane 1.
D1W_CAP0	[8]	Selection bit 0 of different HSTX output capacitors for Data Lane 1. (CAP1,CAP0): = (00): 0 [pF] (CAP1,CAP0): = (01): 2.8 [pF] (CAP1,CAP0): = (10): 3.2 [pF]

Register Field	Bit	Description
		(CAP1,CAP0): = (11): 3.6 [pF]
DLYCNTRL[3:0]	[7:4]	Tuning of transmit window position. The High Speed Clock output can be delayed according to the setting. The recommended value is determined by evaluating the LSI in which this module is implemented. Typical delay for rising/falling edge is about DLYCNTRL x 24ps/27ps. Rising edge : DLYCNTRL x 24ps, Falling edge : DLYCNTRL x 7ps.
Reserved	[3:2]	
D1W_LPTXCURR1EN	[1]	Selection bit-1 for LPTX output current (TRLP/TFLP tuning) for Data Lane 1
D1W_LPTXCURR0EN	[0]	Selection bit-0 for LPTX output current (TRLP/TFLP tuning) for Data Lane 1 00: no additional output current 01: 25% additional output current 10: 25% additional output current 11: 50% additional output current The default value is “10”. However, if “00” is set, the rise/fall time will become later and if “11” is set, the rise/fall time will become earlier.

6.5.4 Data Lane 2 DPHY TX Control Register (D2W_DPHYCONTTX: 0x010C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						D2W_CAP1	D2W_CAP0
Type	RO	RO	RO	RO	RO	RO	RO	R/W
Default	0	0	0	0	0	0	1	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	DLYCNTRL3	DLYCNTRL2	DLYCNTRL1	DLYCNTRL0	Reserved		D2W_LPTXCURR1EN	D2W_LPTXCURR0EN
Type	R/W	R/W	R/W	R/W	RO	RO	R/W	R/W
Default	0	0	0	0	0	0	1	0

Table 6-45 Data Lane 2 DPHY TX Control Register

Register Field	Bit	Description
Reserved	[31:10]	
D2W_CAP1	[9]	Selection bit 1 of different HSTX output capacitors for Data Lane 2.

Register Field	Bit	Description
D2W_CAP0	[8]	Selection bit 0 of different HSTX output capacitors for Data Lane 2. (CAP1,CAP0): = (00): 0 [pF] (CAP1,CAP0): = (01): 2.8 [pF] (CAP1,CAP0): = (10): 3.2 [pF] (CAP1,CAP0): = (11): 3.6 [pF]
DLYCNTRL[3:0]	[7:4]	Tuning of transmit window position. The High Speed Clock output can be delayed according to the setting. The recommended value is determined by evaluating the LSI in which this module is implemented. Typical delay for rising/falling edge is about DLYCNTRL x 24ps/27ps. Rising edge : DLYCNTRL x 24ps, Falling edge : DLYCNTRL x 27ps.
Reserved	[3:2]	
D2W_LPTXCURR1EN	[1]	Selection bit-1 for LPTX output current (TRLP/TFLP tuning) for Data Lane 2.
D2W_LPTXCURR0EN	[0]	Selection bit-0 for LPTX output current (TRLP/TFLP tuning) for Data Lane 2 0: no additional output current 1: 25% additional output current 10: 25% additional output current 11: 50% additional output current The default value is “10”. However, if “00” is set, the rise/fall time will become later and if “11” is set, the rise/fall time will become earlier.

6.5.5 Data Lane 3 DPHY TX Control Register (D3W_DPHYCONTTX: 0x0110)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						D3W_CAP1	D3W_CAP0
Type	RO	RO	RO	RO	RO	RO	RO	R/W
Default	0	0	0	0	0	0	1	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	DLYCNTRL3	DLYCNTRL2	DLYCNTRL1	DLYCNTRL0	Reserved		D3W_LPTXCURR1EN	D3W_LPTXCURR0EN
Type	R/W	R/W	R/W	R/W	RO	RO	R/W	R/W
Default	0	0	0	0	0	0	1	0

Table 6-46 Data Lane 3 DPHY TX Control Register

Register Field	Bit	Description

Register Field	Bit	Description
Reserved	[31:10]	
D3W_CAP1	[9]	Selection bit 1 of different HSTX output capacitors for Data Lane 3.
D3W_CAP0	[8]	Selection bit 0 of different HSTX output capacitors for Data Lane 3. (CAP1,CAP0): = (00): 0 [pF] (CAP1,CAP0): = (01): 2.8 [pF] (CAP1,CAP0): = (10): 3.2 [pF] (CAP1,CAP0): = (11): 3.6 [pF]
DLYCNTRL[3:0]	[7:4]	Tuning of transmit window position. The High Speed Clock output can be delayed according to the setting. The recommended value is determined by evaluating the LSI in which this module is implemented. Typical delay for rising/falling edge is about DLYCNTRL x 24ps/27ps. Rising edge : DLYCNTRL x 24ps, Falling edge : DLYCNTRL x 27ps.
Reserved	[3:2]	
D3W_LPTXCURR1EN	[1]	Selection bit-1 for LPTX output current (TRLP/TFLP tuning) for Data Lane 3
D3W_LPTXCURR0EN	[0]	Selection bit-0 for LPTX output current (TRLP/TFLP tuning) for Data Lane 3 00: no additional output current 01: 25% additional output current 10: 25% additional output current 11: 50% additional output current The default value is “10”. However, if “00” is set, the rise/fall time will become later and if “11” is set, the rise/fall time will become earlier.

6.5.6 Clock Lane DPHY Control Register (CLW_CNTRL: 0x0140)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x00							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved							CLW_LaneDisable
Type	RO							R/W
Default	0x00							0

Table 6-47 Clock Lane DPHY Control Register

Register Field	Bit	Default	Description
Reserved	[15:1]	0x0	

Register Field	Bit	Default	Description
CLW_LaneDisable	[0]	0x0	Force Lane Disable for Clock Lane. 1'b1: Force Lane Disable 1'b0: Bypass Lane Enable from PPI Layer enable.

6.5.7 Data Lane 0 DPHY Control Register (D0W_CNTRL: 0x0144)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x00							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved							CLW_LaneDisable
Type	RO							R/W
Default	0x00							0

Table 6-48 Data Lane 0 DPHY Control Register

Register Field	Bit	Default	Description
Reserved	[15:1]	0x0	
D0W_LaneDisable	[0]	0x0	Force Lane Disable for Data Lane 0. 1'b1: Force Lane Disable 1'b0: Bypass Lane Enable from PPI Layer enable.

6.5.8 Data Lane 1 DPHY Control Register (D1W_CNTRL: 0x0148)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x00							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved							D1W_LaneDisable
Type	RO							R/W
Default	0x00							0

Table 6-49D ata Lane 1 DPHY Control Register

Register Field	Bit	Default	Description
Reserved	[15:1]	0x0	

Register Field	Bit	Default	Description
D1W_LaneDisable	[0]	0x0	Force Lane Disable for Data Lane 0. 1'b1: Force Lane Disable 1'b0: Bypass Lane Enable from PPI Layer enable.

6.5.9 Data Lane 2 DPHY Control Register (D2W_CNTRL: 0x014C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x00							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved							D2W_LaneDisable
Type	RO							R/W
Default	0x00							0

Table 6-50 Data Lane 2 DPHY Control Register

Register Field	Bit	Default	Description
Reserved	[15:1]	0x0	
D2W_LaneDisable	[0]	0x0	Force Lane Disable for Data Lane 2. 1'b1: Force Lane Disable 1'b0: Bypass Lane Enable from PPI Layer enable.

6.5.10 Data Lane 3 DPHY Control Register (D3W_CNTRL: 0x0150)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x00							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved							D3W_LaneDisable
Type	RO							R/W
Default	0x00							0

Table 6-51 Data Lane 3 DPHY Control Register

Register Field	Bit	Default	Description
Reserved	[15:1]	0x0	

Register Field	Bit	Default	Description
D3W_LaneDisable	[0]	0x0	Force Lane Disable for Data Lane 3. 1'b1: Force Lane Disable 1'b0: Bypass Lane Enable from PPI Layer enable.

6.6 Tx PPI Registers

6.6.1 PPI STARTCNTRL (STARTCNTRL: 0x0204)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							START
Type	RO	RO	RO	RO	RO	RO	RO	W
Default	0	0	0	0	0	0	0	0

Table 6-52 STARTCNTRL

Register Field	Bit	Description
Reserved	[31:1]	
START	[0]	START control bit of PPI-TX function. By writing 1 to this bit, PPI starts function. 0: Stop function. (default). Writing 0 is invalid and the bit can be set to zero by system reset only. 1: Start function. The following registers are set to appropriate value before starting any transmission by START bit in STARTCTRL register. Once START bit is set to high, the change of the register bits does not affect to function. In order to change the values, initialization by RESET_N is necessary.

6.6.2 PPI STATUS (PPISTATUS: 0x0208)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							BUSY
Type	RO	RO	RO	RO	RO	RO	RO	R
Default	0	0	0	0	0	0	0	0

Table 6-53 PPI STATUS

Register Field	Bit	Description
Reserved	[31:1]	
BUSY	[0]	After writing 1 to the START bit in the STARTCNTRL register, this bit is set until RESET_N is asserted. 0: Not Busy. (default) 1: Busy.

6.6.3 LINEINITCNT (LINEINITCNT: 0x0210)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	LINEINITCNT[15:8]							
Type	R/W							
Default	0x20							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	LINEINITCNT[7:0]							
Type	R/W							
Default	0x8E							

Table 6-54 LINEINITCNT

Register Field	Bit	Description
Reserved	[31:16]	
LINEINITCNT	[15:0]	Line Initialization Wait Counter This counter is used for line initialization. **Set this register before setting [STARTCNTRL].START = 1.** MIPI specification requires that the slave device needs to observe LP-11 for 100 us and ignore the received data before the period at initialization time. The count value depends on HFCLK and the value needs to be set to achieve more than 100 us. The counter starts after the START bit of the STARTCNTRL register is set. The Master device needs to output LP-11 for 100 us in order for the slave device to observe LP-11 for the period. For example, in order to set 100 us when the period of HFCLK is 12 ns, the counter value should be more than 8333.3 = 0x208D (100 us / 12 ns). Default is 0x208E.

6.6.4 LPTXTIMECNT (LPTXTIMECNT: 0x0214)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved					LPTXTIMECNT[10:8]		
Type	RO					R/W		
Default	0x00					0x0		
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	LPTXTIMECNT[7:0]							
Type	R/W							
Default	0x01							

Table 6-55 LPTXTIMECNT

Register Field	Bit	Description
Reserved	[15:11]	
LPTXTIMECNT	[10:0]	SYSLPTX Timing Generation Counter The counter generates a timing signal for the period of LPTX. This counter is counted using the HSByteClk (the Main Bus clock), and the value of (setting + 1) *HSByteClk Period becomes the period LPTX. Be sure to set the counter to a value greater than 50 ns.

Set this register before setting [STARTCNTRL].START = 1.

6.6.5 TCLK_HEADERCNT (TCLK_HEADERCNT: 0x0218)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	TCLK_ZEROCNT[7:0]							
Type	R/W							
Default	0x01							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	TCLK_PREPARECNT[6:0]						
Type	RO	R/W						
Default	0	0x01						

Table 6-56 TCLK_HEADERCNT

Register Field	Bit	Description
TCLK_ZEROCNT	[15:8]	**TCLK_ZERO Counter** This counter is used for Clock Lane control in the Master mode. In order to satisfy the timing parameter TCLK-PRE + TCLK-ZERO for Clock Lane, this counter is used. This counter is counted by HSBYTECLk. Set this register in order to set the minimum time (TCLK-PRE + TCLK-ZERO) to a value greater than 300 ns. The actual value is ((1 to 2) + (TCLK_ZEROCNT + 1)) x HSByteClkCycle + (PHY output delay). The PHY output delay is about (0 to 1) x HSByteClkCycle in the ByteClk conversion performed during RTL simulation, and is about (2 to 3) x MIPIBitClk cycle in the BitClk conversion.
Reserved	[7]	
TCLK_PREPARECNT	[6:0]	**TCLK_PREPARE Counter** This counter is used for Clock Lane control in the Master mode. In order to satisfy the timing parameter TCLK-PREPARE for Clock Lane, this counter is used. This counter is counted by HSBYTECLK. Set TCLK-PREPARE period that is greater than 38 ns but less than 95 ns. Calculating formula (TCLK_PREPARECNT + 1) x HSByteClkCycle

Set this register before setting [STARTCNTRL].START = 1.

6.6.6 TCLK_TRAILCNT (TCLK_TRAILCNT: 0x021C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x00							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	TCLKTRAILCNT[7:0]							
Type	R/W							
Default	0x01							

Table 6-57 TCLK_TRAILCNT

Register Field	Bit	Description
Reserved	[15:8]	
TCLK_TRAILCNT	[7:0]	**TCLK_TRAIL Counter** This counter is used for Clock Lane control in Master mode. In order to satisfy the timing parameter about TCLK-TRAIL and TEOT for Clock Lane, this counter is used. This counter is counted by HSBYTECLK. Set this register in order to set TCLK-TRAIL to a value greater than 60 ns and TEOT to a value less than 105 ns + 12 x UI The actual value is (TCLK_TRAILCNT + (1 to 2)) xHSByteClkCycle + (2+(1 to 2)) * HSBYTECLKCycle - (PHY output delay). The PHY output delay is about (0 to 1) xHSByteClkCycle in the ByteClk conversion performed during RTL simulation, and is about (2 to 3) xMIPIBitClk cycle in the BitClk conversion.

Set this register before setting [STARTCNTRL].START = 1.

6.6.7 THS_HEADERCNT (THS_HEADERCNT: 0x0220)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved	THS_ZEROCNT[6:0]						
Type	RO	R/W						
Default	0	0x01						
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved	THS_PREPARECNT[6:0]						
Type	RO	R/W						
Default	0	0x01						

Table 6-58 THS_HEADERCNT

Register Field	Bit	Description

Register Field	Bit	Description
THS_ZEROCNT	[14:8]	**THS_ZERO Counter** This counter is used for Data Lane control in Master mode. In order to satisfy the timing parameter about THS-PREPARE + THS-ZERO for Data Lane, this counter is used. This counter is counted by HSBYTECLK. Set this register to set the (THS-PREPARE + THS-ZERO) period, which should be greater than (145 ns + 10 x UI) results. The actual value is ((1 to 2) + 1 + (TCLK_ZEROCNT + 1) + (3 to 4)) x ByteClk cycle + HSByteClk x (2+(1 to 2)) +(PHY delay). The PHY output delay is about (1 to 2) x HSByteClkCycle in the ByteClk conversion performed during RTL simulation, and is about (8+(5 to 6)) x MIPIBitClk cycle in BitClk conversion.
Reserved	[7]	
THS_PREPARECNT	[6:0]	**THS_PREPARE Counter** This counter is used for Data Lane control in Master mode. In order to satisfy the timing parameter about THS-PREPARE for Data Lane, this counter is used. This counter is counted by HSBYTECLK. Set this register in order to set the THS-PREPARE period, which should be greater than (40 ns + 4xUI) and less than (8 5 ns + 6xUI) results. Calculating Formula: (THS_PREPARECNT + 1) x HSByteClkCycle

Set this register before setting [STARTCNTRL].START = 1.

6.6.8 TWAKEUP (TWAKEUP: 0x0224)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	TWAKEUPCNT[15:8]							
Type	R/W							
Default	0x4E							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	B0
Name	TWAKEUPCNT[7:0]							
Type	R/W							
Default	0x20							

Table 6-59 TWAKEUP

Register Field	Bit	Description
Reserved	[31:16]	
TWAKEUPCNT	[15:0]	**TWAKEUP Counter** This counter is used to exit ULPS state. Ultra-Low Power State is exited by means of a Mark-1 state with a length TWAKEUP followed by a Stop state. This counter is counted by the unit of LPTXTIMECNT.

Set this register before setting [STARTCNTRL].START = 1.

6.6.9 TCLK_POSTCNT (TCLK_POSTCNT: 0x0228)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved					TCLK_POSTCNT[10:8]		
Type	RO					R/W		
Default	0x00					0x2		
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	TCLK_POSTCNT[7:0]							
Type	R/W							
Default	0x00							

Table 6-60 TCLK_POSTCNT

Register Field	Bit	Description
Reserved	[15:11]	
TCLK_POSTCNT	[10:0]	**TCLK_POST Counter** This counter is used for Clock Lane control in Master mode. This counter is counted by the HSByteClk. Set a value greater than (60 ns + 52 x UI) results. The actual value is ((1 to 2) + (TCLK_POSTCNT + 1)) x HSByteClk cycle + (1) x HSBYTECLK cycle.

Set this register before setting [STARTCNTRL].START = 1.

6.6.10 THS_TRAILCNT (THS_TRAILCNT: 0x022C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0x00							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved				THS_TRAILCNT[3:0]			
Type	RO				R/W			
Default	0x0				0x2			

Table 6-61 THS_TRAILCNT

Register Field	Bit	Description
Reserved	[15:4]	

Register Field	Bit	Description
THS_TAILCNT	[3:0]	**THS_TRAIL Counter** This counter is used for Data Lane control in Master mode. This counter is counted by HSBYTECLK. Set a value greater 8 x UI or (60 ns + 4 x UI) and less than TEOT which is 105 ns + 12 x UI results. The actual value is (1 + THS_TRAILCNT) xByteClk cycle + ((1 to 2) + 2) xHSBYTECLK cycle - (PHY output delay). The PHY output delay is about (1 to 2) xHSByteClkCycle in ByteClk conversion performed during RTL simulation and is about (8+(5 to 6)) xMIPIBitClk cycle in BitClk conversion.

Set this register before setting [STARTCNTRL].START = 1.

6.6.11 HSTXVREGCNT (HSTXVREGCNT: 0x0230)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	HSTXVREGCNT[15:8]							
Type	R/W							
Default	0x00							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	HSTXVREGCNT[7:0]							
Type	R/W							
Default	0x20							

Table 6-62 HSTXVREGCNT

Register Field	Bit	Description
HSTXVREGCNT	[15:0]	TX Voltage Regulator setup Wait Counter This counter is used for all lanes of HSTXVREG commonly. Counter value is counted by HFCLK. The counter starts when START bit is set. After the counter is counted up, PPI-TX can change the line from LP mode to HS mode. If the counter value is set to zero, there is no wait by the counter. Recommended counter value will be decided by evaluation. It was determined that a value of 200 ns max in the ELDEC TEG skew evaluation results (5/21/2009) is sufficient. LINEINCNT is 100 us, so any value less than that will not affect the value of this counter. The value 1 us is used in the example setting.

Set this register before setting [STARTCNTRL].START = 1.

6.6.12 HSTXVREGEN (HSTXVREGEN: 0x0234)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved			D3M_HSTXVREGEN	D2M_HSTXVREGEN	D1M_HSTXVREGEN	D0M_HSTXVREGEN	CLM_HSTXVREGEN
Type	RO	RO	RO	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0

Table 6-63 HSTXVREGEN

Register Field	Bit	Description
Reserved	[15:5]	
D3M_HSTXVREGEN	[4]	Voltage regulator enable for HSTX Data Lane 3. In order to reduce power consumption, set to be “disable” when PPI-TX is not used. 0: Disable (Default) 1:Enable
D2M_HSTXVREGEN	[3]	Voltage regulator enable for HSTX Data Lane 2. In order to reduce power consumption, set to be “disable” when PPI-TX is not used. 0: Disable (Default) 1:Enable
D1M_HSTXVREGEN	[2]	Voltage regulator enable for HSTX Data Lane 1. In order to reduce power consumption, set to be “disable” when PPI-TX is not used. 0:Disable (Default) 1:Enable
D0M_HSTXVREGEN	[1]	Voltage regulator enable for HSTX Data Lane 0. In order to reduce power consumption, set to be “disable” when PPI-TX is not used. 0:Disable (Default) 1:Enable
CLM_HSTXVREGEN	[0]	Voltage regulator enable for HSTX Clock Lane. In order to reduce power consumption, set to be “disable” when PPI-TX is not used. 0:Disable (Default) 1:Enable

Set this register before setting [STARTCNTRL].START = 1.

6.6.13 TXOPTIONCNTRL (TXOPTIONCNTRL: 0x0238)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved							CONTCLK MODE
Type	RO	RO	RO	RO	RO	RO	RO	R/W
Default	0	0	0	0	0	0	0	0

Table 6-64 TXOPTIONCNTRL

Register Field	Bit	Description
Reserved	[15:1]	
CONTCLKMODE	[0]	**Set Continuous Clock Mode** Writing "1" to this bit will set the Clock Lane to the Continuous Clock mode regardless of the PPI interface signal and will maintain the Clock Lane output. 0: Non-continuous clock mode. Transitions into the LP11 state in coordination with the Data Lane operation. 1:Continuous clock mode. Maintains the Clock Lane output regardless of the Data Lane operation.

This bit can be rewritten when [STATUS].BUSY is set.
Set this register before setting [STARTCNTRL].START = 1. Do not change this register after START = 1 is set.

6.7 Tx Control Register

6.7.1 CSI Configuration Read Register(CSI_CONTROL: 0x040C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Csi_mode	Reserved				HtxToEn	Reserved	
Type	RO	RO				RO	RO	
Default	1	0	1	1	1	1	0	
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	TxMd	Reserved	HsCkMd	Reserved		NOL[1:0]		EoTDis
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Table 6-65 CSI Control Register

Register Field	Bit	Description
CSI_mode	15	**CSI Mode Selection** 0: Reserved 1: CSI MOde
Reserved	[14:11]	Reserved
HtxToEn	10	**HSTX_TO_EN** 0: Disables the HTX_TO timer. 1: Enables the HTX_TO timer.

Reserved	[9:8]	
TxMd	7	**TXMODE** 0: Low power transfer is performed to Tx. 1: High-Speed data transfer is performed to Tx.
Reserved	6	
HsCkMd	5	**HSCLOCKMODE** 0: Operation is in the discontinuous clock mode. 1: Operation is in the continuous clock mode.
Reserved	[4:3]	
NOL	[2:1]	**NOL** This field specifies the number of HS lanes. This field is also used as the LP Lane Enable setting. Data Lane 0 is used as the Enable for LP communication and ULPS. Data Lane 1 or higher is used as the Enable for ULPS. This setting can only be made during initial setup or during reset. 00: Only Data Lane 0 is used. 01: Data Lanes 0 and 1 are used. 10: Data Lanes from 0 to 2 are used. 11: Data Lanes 0 to 3 are used.
EoTDis	0	**EOT_DISABLE** 0: The EOT packet is automatically granted at the end of HS transfer then is transmitted. 1: The EOT packet is not automatically granted at the end of HS transfer and is not transmitted.

Only indirect writing, i.e. write to CSI_CONFW Register is possible.

6.7.2 CSI STATUS Register (CSI_STATUS: 0x0410)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved					WSync	TxAct	RxAct
Type	RO					RO	RO	RO
Default	0xX					0	0	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved							Hlt
Type	RO							RO
Default	0x0X							0

Table 6-66 CSI STATUS Register

Register Field	Bit	Default	Description
Reserved	[15:11]	X	
WSync	10	0	**Wait Sync Signal** This bit indicates that the CSI-TX module is waiting for a particular Sync signal
TxAct	9	0	**Transmitter Active** This bit indicates that the CSI-TX module is in the Transmit mode.
RxAct	8	0	**Receiver Active** This bit indicates that the CSI-TX module is in the Receive mode.
Reserved	[7:1]	X	

Register Field	Bit	Default	Description
Hlt	0	0	**Halted** The CSI-TX module is stopped by either an error or a pause request.

6.7.3 CSI_INT Register (CSI_INT: 0x0414)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0x00							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved					IntAck	Reserved	
Type	RO					RO	RO	
Default	0x00					0	0x00	
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved							
Type	RO							
Default	0x00							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved				IntHlt	IntEr	Reserved	
Type	RO				RO	RO	RO	
Default	0x00				0	0	0	

Table 6-67 CSI_INT Register

Register Field	Bit	Default	Description
Reserved	[31:19]	0x0	
IntAk	18	0x0	**INT_ACK** This bit indicates that the Acknowledge trigger has been received.
Reserved	[17:4]	0x0	
IntHlt	3	0x0	**INT_HALTED** The CSI-TX module was stopped by an error or a pause request.
IntEr	2	0x0	**INT_CSI_ERR** An interrupt was requested by a CSI_ERR register error.
Reserved	[1:0]	0x0	

Each bit can indirectly clear a register value either when “1” is written to the bit of each corresponding CSI_INT_CLR register.

6.7.4 CSI_INT_ENA Register (CSI_INT_ENA: 0x0418)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							

Default	0x00							
Bit	**B23**	**B22**	**B21**	**B20**	**B19**	**B18**	**B17**	**B16**
Name	Reserved					IEnAk	Reserved	
Type	RO					RO	RO	
Default	0x00					0	0x0	
Bit	**B15**	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
Name	Reserved							
Type	RO							
Default	0x00							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved				IEnHlt	IEnEr	Reserved	
Type	RO				RO	RO	RO	
Default	0x0				0	0	0x0	

Table 6-68 CSI_INT_ENA Register

Register Field	Bit	Default	Description
Reserved	[31:19]	0x0	
IEnAk	18	0x0	**INTENA_ACK** This bit enables interrupt notification by INT_ACK sources.
Reserved	[17:4]	0x0	
IEnHlt	3	0x0	**INTENA_HALTED** This bit enables interrupt notification by INT_HALTED sources.
IEnEr	2	0x0	**INTENA_CSI_ERR** This bit enables interrupt notification by INT_CSI_ERR sources.
Reserved	[1:0]	0x0	

Only indirect writing, i.e. write to CSI_CONFW with [Addr] = 0x06.

6.7.5 CSI_ERR Register (CSI_ERR: 0x044C)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						InEr	WCEr
Type	RO						RO	RO
Default	0x00						0	0
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	SynTo	RxFRdEr	TeEr	QUnk	QWrEr	HTxTo	HTxBrk	Cntn
Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0

Table 6-29 CSI_ERR Register

Register Field	Bit	Default	Description
Reserved	[31:10]	0x0	

InEr	9	0x0	**INTERNAL_ERROR** This bit indicates that another internal error occurred.
WCEr	8	0x0	**WC_ERROR** This bit indicates that more bytes than expected were received from the PDIF. Because distinguishing the current data from the next payload data of continuous transfers is difficult when the last payload data is 4-byte aligned, this error is not detected.
SynTo	7	0x0	**SYNC_TO** This bit indicates that a synchronous wait timeout occurred.
RxFRdEr	6	0x0	**RXFIFO_RDERR** This bit indicates that an empty Receive FIFO was read.
TeEr	5	0x0	**TE_ERROR** This bit indicates that the peripheral interface did not transmit the tearing trigger the CSI-TX module is expecting.
QUnk	4	0x0	**CQ_UNKNOWN** This bit indicates that an unknown command or incorrect parameter was detected by the command queue.
QWrEr	3	0x0	**CQ_WRERR** This bit indicates that Write access to a full command queue occurred.
HTxTo	2	0x0	**HTX_TO** This bit indicates that a High-Speed TX timeout occurred.
HTxBrk	1	0x0	**HSTX_BROKEN** This bit indicates that the byte stream was disrupted during High-Speed transfer.
Cntn	0	0x0	**CONTENTION** This bit indicates that a contention was detected during lower power transfer.

The content of the CSI_ERR register is cleared by reading it out.

6.7.6 CSI_ERR_INTENA (CSI_ERR_INTENA: 0x0450)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						CSI_ERR_INTENA[9:8]	
Type	RO						RO	
Default	0x00						0	
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	CSI_ERR_INTENA[7:0]							
Type	RO							
Default	0x00							

Table 6-69 CSI_ERR_INTENA Register

Register Field	Bit	Default	Description
Reserved	[31:10]	0x0	
CSI_ERR_INTENA	[9:0]	0x0 (??)	**CSI_ERR_INTENA** This field controls interrupt generation for when an error has been reported to the CSI_ERR register. Generation of the CSI_ERR_INT interrupt which corresponds to the CSI_ERR register error is enabled.

Only indirect writing, i.e. write to CSI_CONFW with [Addr] = 0x14.

6.7.7 CSI_ERR_HALT Register(CSI_ERR_HALT: 0x0454)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved						CSI_ERR_HALT[9:8]	
Type	RO						RO	
Default	0x00						0	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	CSI_ERR_HALT[7:0]							
Type	RO							
Default	0x00							

Table 6-70 CSI_ERR_HALT Register

Register Field	Bit	Default	Description
Reserved	[31:10]	0x0	
CSI_ERR_HALT	[9:0]	0x0 (??)	**CSI_ERR_HALT** This field controls CSI-TX operation for when an error is reported to the CSI_ERR register. The CSI-TX module stops command processing when it receives an error corresponding to the set bits in the CSI_ERR_INTENA and CSI_ERR_HALT registers. (??)

Only indirect writing, i.e. write to CSI_CONFW with [Addr] = 0x15.

6.7.8 CSI Configuration Register (CSI_CONFW: 0x0500)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	MODE			Address				
Type	WO	WO	WO	WO	WO	WO	WO	WO
Default	0	0	0	0	0	0	0	0
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved[23:16]							
Type	WO	WO	WO	WO	WO	WO	WO	WO
Default	0	0	0	0	0	0	0	0
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	DATA[15:8]							
Type	WO	WO	WO	WO	WO	WO	WO	WO
Default	0	0	0	0	0	0	0	0
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	DATA[7:0]							
Type	WO	WO	WO	WO	WO	WO	WO	WO
Default	0	0	0	0	0	0	0	0

Table 6-71 CSI Configuration Write Register

Register Field	Bit	Description
MODE	[31:29]	**Set or Clear AddrReg (register specified in Address field) Bits** 3'b101: Set Register Bits in AddRegas indicated in DATA field 3'b110: Clear Register Bits in AddRegas indicated in DATA field Others: Reserved
Address	[28:24]	**Address Field** 0x03: CSI_Control Register 0x06: CSI_INT_ENA Register 0x14: CSI_ERR_INTENA Register 0x15: CSI_ERR_ HALT Register Others: Reserved
Reserved	[23:16]	
DATA	[15:0]	**DATA Field** When location DATA[n] is set to '1', the corresponding bit at AddrReg[n] will be cleared or set depending on MODE bits described above. Multiples bits can be set simultaneously

Note: Write to CSI_CONFW Register results to changes in corresponding bit changed in AddrReg Register.

6.7.9 CSI LP Command (CSI_LPCMD: 0x0500)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	LP Command							
Type	WO	WO	WO	WO	WO	WO	WO	WO
Default	0	0	1	1	0	0	0	0
Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved[23:16]							
Type	WO							
Default	0xXX							
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved[15:8]							
Type	WO							
Default	0xXX							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	LANE_ENA					LP_Code		
Type	WO	WO	WO	WO	WO	WO		
Default	0	0	0	0	0	0		

Note: This command share the same register as CSI_CONFW. It is in LP command mode when [31:24] = 0x 30

Table 6-72 CSI Configuration Write Register

Register Field	Bit	Default	Description
LPCommand	[31:24]	0x0	**LP Command Mode Selection** 8'h30: Set Register Bits to this value to enable LP Command mode Others: Reserved
Reserved	[23:8]	0x0	Reserved

LANE_ENA	[7:3]	0x0	**LANE Enable Field** This Lane Enable is only used by LPC_CODE 000 (ULPS transition) and 001 (LP Stop transition). Select the following Lanes within the range of Lanes set to "Enable" by CSI_CONTROL[NOL]. Do not set ULPS transition and LP Stop transition for Lanes that have not been set to "Enable" by the NOL bit. LANE_ENA[3]: Select Clock Lanes LANE_ENA[4]: Select Lane 0 LANE_ENA[5]: Select Lane 1 LANE_ENA[6]: Select Lane 2 LANE_ENA[7]: Select Lane 3
LP_CODE	[2:0]	0x0	000: The Lane indicated by LANE_ENA transitions to ULPS (the ultra low power state). 001: The Lane indicated by LANE_ENA transitions to the LP stop state. 010: A remote application reset trigger is transmitted to Lane 0. Then, Lane 0 returns to the LP stop state. The state of other Lanes is not affected. 011: Bus direction change (BTA) is executed on Lane 0. After BTA, Lane 0 returns to the LP Stop state. Other Lanes are not affected. Others: Reserved

Note: Setting 0x0500 = 0x300000F8 with put the clock lane and 4 data lanes into ULPS mode.
While sending any packet during ULPS mode will cause CSI link to exit ULPS mode

6.7.10 CSI_RESET Register (CSI_RESET: 0x0504)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved						RstCnf	RstMdl
Type	RO						R/W	R/W
Default	0x00						0	0

Table 6-73 CSI_RESET Register

Register Field	Bit	Default	Description
Reserved	[31:2]	0x0	
RstCnf	1	0x0	**RST_CONF** 0: Operation is not affected. 1: The setting register is reset.
RstMdl	0	0x0	**RST_MODULE** Do not set this bit to "1". Perform a hardware reset when a CSITX block reset is necessary. Use this bit when resetting the sub modules inside this block (CSI layer). The PHY layer or the application layer blocks are not reset. 0: Operation is not affected. 1: Modules inside the CSI layer are reset.

6.7.11 CSI_INT_CLR Register(CSI_INT_CLR: 0x050C)

Bit	B31	B30	B29	B28	B27	B26	B25	B24
Name	Reserved							
Type	RO							
Default	0							

Bit	B23	B22	B21	B20	B19	B18	B17	B16
Name	Reserved					ICrAk	Reserved	
Type	RO					WO	RO	
Default	0					0	0	
Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved							
Type	RO							
Default	0							
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved				ICrHlt	ICrEr	Reserved	
Type	RO				WO	WO	RO	
Default	0				0	0	0	

Table 6-74 CSI_INT_CLR Register

Register Field	Bit	Default	Description
Reserved	[31:19]	0x0	
ICrAk	18	0x0	**INTCLR_ACK** 0: Operation is not affected. 1: The INT_ACK interrupt is cleared.
Reserved	[17:4]	0x0	
ICrHlt	3	0x0	**INTCLR_HALTED** 0: Operation is not affected. 1: The INT_HALTED interrupt is cleared.
ICrEr	2	0x0	**INTCLR_CSI_ERR** 0: Operation is not affected. 1: The INT_CSI_ERR interrupt is cleared.
Reserved	[1:0]	0x0	

6.7.12 CSI_START (CSI_START: 0x0518)

Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Reserved[7:1]							Strt
Type	RO	RO	RO	RO	RO	RO	RO	WO
Default	0	0	0	0	0	0	0	0

Table 6-75 CSI2_START

Register Field	Bit	Description
Reserved	[31:1]	

6.8 TxDebug Register

6.8.1 Debug Active Line Count Register (DBG_LCNT: 0x00E0)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	db_wsram	db_cen	Reserved				db_alcnt[9:8]	
Type	R/W	R/W	RO				R/W	
Default	0x0	0x0	0x0				0x1	
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	db_alcnt[7:0]							
Type	R/W							
Default	0x0							

Debug Active Video Line Count Register

Register Field	Bit	Description
db_wsram	[15]	**Debug Video Buffer** 0: normal 1: enable I2C/SPI write to VB sram
db_cen	[14]	**Debug csitx mode enable** 0: Normal mode 1: Debug mode (enable color bar logic)
Reserved	[13:10]	
db_alcnt	[9:0]	Debug Active Line Count 10'h0: 1 line 10'h1: 2 line .. 10'h3FF: 1024 line

6.8.2 Debug Line Width Register (DBG_Width: 0x00E2)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Reserved				Db_width[11:8]			
Type	RO				R/W			
Default	0x0				0x1			
Bit	B7	B6	B5	B4	B3	B2	B1	B0
Name	Db_awcnt[7:0]							
Type	R/W							
Default	0x0							

Debug Video Line Word Count Register

Register Field	Bit	Description
Reserved	[15:12]	
Db_width	[11:0]	Debug Total byte count in a line (include blank period) 12'h0: 1 byte 12'h1: 2 bytes .. 12'hFFF: 4096 bytes

6.8.3 Debug Vertical Blank Line Count Register (DBG_VBlank: 0x00E4)

Bit	B15	B14	B13	B12	B11	B10	B9	B8

Name	Reserved							
Type	RO							
Default	0x0							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Reserved	Db_vb[6:0]						
Type	RO	R/W						
Default	0x0	0x10						

Debug Vertical Blank Register

Register Field	Bit	Description
Reserved	[15:7]	
Db_vb	[6:0]	Debug Vertical Blank line 7'h0: 1 line 7'h1: 2 line .. 7'7F:128 line

6.8.4 Debug Video Data Register (DBG_Data: 0x00E8)

Bit	B15	B14	B13	B12	B11	B10	B9	B8
Name	Db_data[15:8]							
Type	WO							
Default	0xX							
Bit	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Name	Db_data[7:0]							
Type	WO							
Default	0xX							

Debug Video Data Register

Register Field	Bit	Description
Db_data	[15:0]	Data will be written into Video FIFO in continuous. Note: must be in multiple of 4 bytes

Strt	0	**CSI_START** 0: The clock is not supplied to modules other than CONIF. 1: The clock is supplied to all modules. When “1” is written to this bit, the clock is supplied to modules other than the CSI2-TX CONIF. To start CSI2-TX operation, set this bit to “1” after a reset is performed. This bit must be set to “1” even when accessing registers other than CSI2_START. Once this bit is set to “1”, writing of “0” is not allowed. Perform a reset to change this bit from “1” to “0”.

7 Package

7.1 TC358746A Package

The packages for TC358746AXBG are described in the figures below.

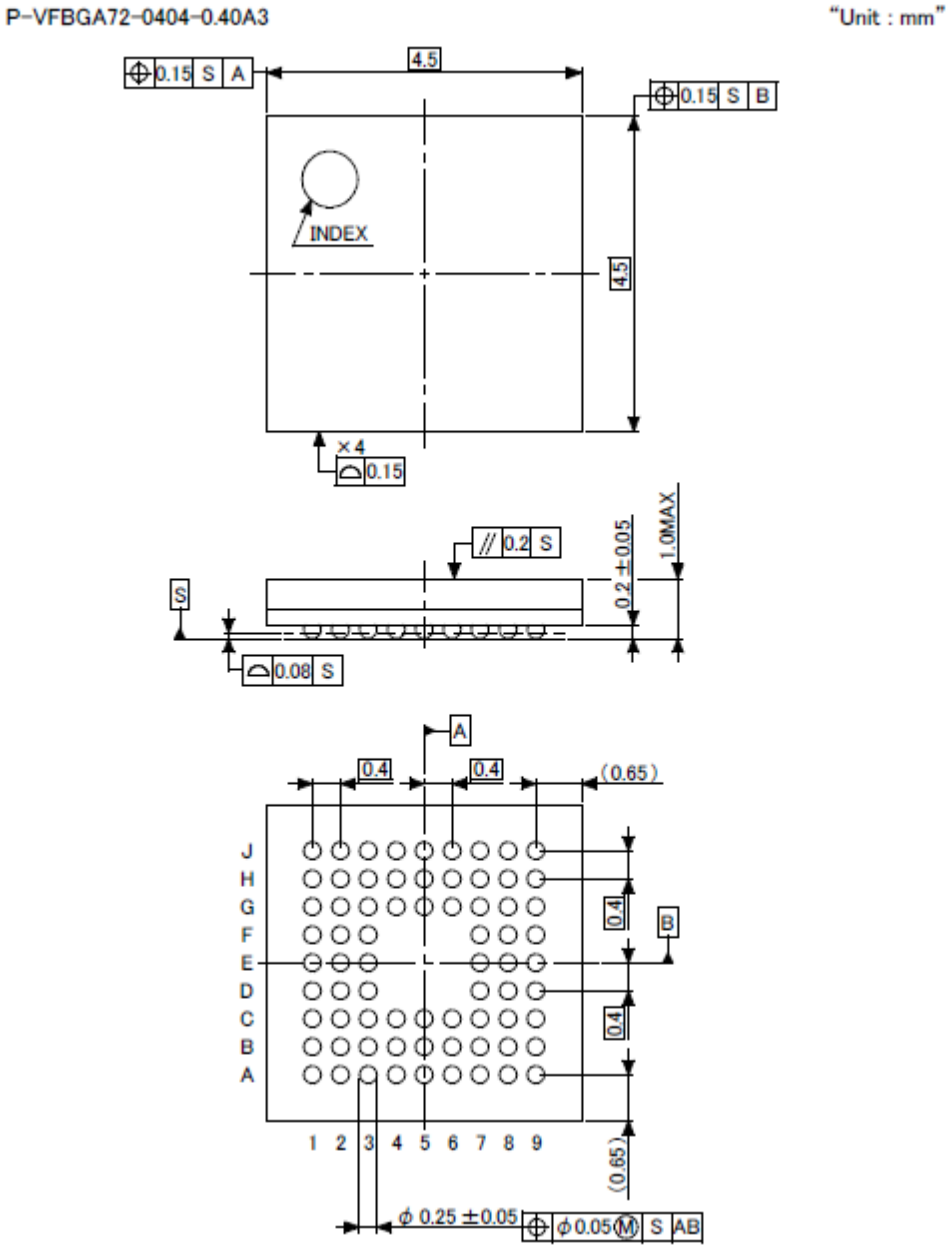

Figure 7-1 P-VFBGA72-0404-0.40A3 package

Table 7-1P-VFBGA72-0404-0.40A3 Mechanical Dimension

Dimension	Min.	Typ.	Max.
Solder ball pitch	---	0.4 mm	---
Solder ball height	0.15 mm	0.2 mm	0.205 mm
Package dimension	---	4.5 x 4.5 mm^2	---
Package height	---	---	1.0 mm

7.2 TC358748 Package

The packages for TC358748XBG are described in the figures below.

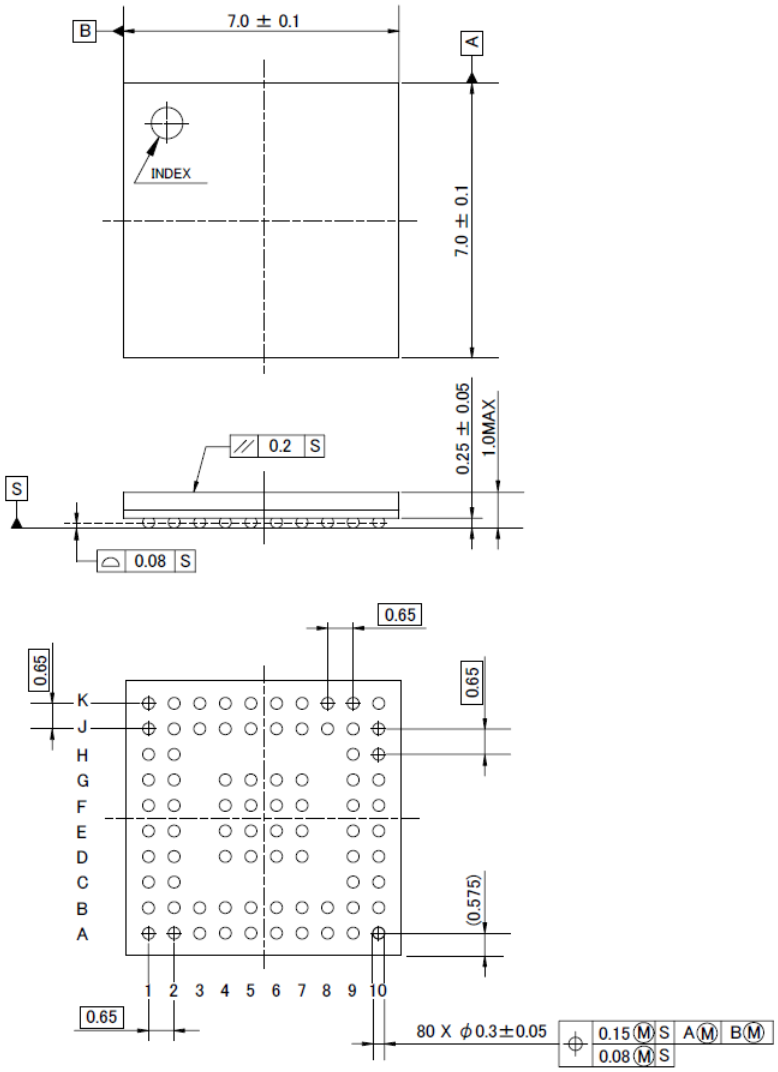

Figure 7-2 P-VFBGA80-0707-0.65 package

Table 7-2 P-VFBGA80-0707-0.65 Mechanical Dimension

Dimension	Min.	Typ.	Max.
Solder ball pitch	---	0.65 mm	---
Solder ball height	0.20 mm	0.25 mm	0.30 mm
Package dimension	---	7.0 x 7.0 mm^2	---
Package height	---	---	1.0 mm

8 Electrical Characteristics

8.1 Absolute Maximum Ratings

VSS= 0V reference

Parameter	Symbol	Rating	Unit
Supply voltage (1.8V - Digital IO)	VDDIO	-0.3 ~ +3.9	V
Supply voltage (1.2V – Digital Core)	VDDC	-0.3 ~ +1.8	V
Supply voltage (1.2V – MIPI CSI PHY)	VDD_MIPI	-0.3 ~ +1.8	V
Input voltage (CSI IO)	V_{IN_CSI}	-0.3 ~ VDD_MIPI+0.3	V
Output voltage (CSI IO)	V_{OUT_CSI}	-0.3 ~ VDD_MIPI+0.3	V
Input voltage (Digital IO)	V_{IN_IO}	-0.3 ~ VDDIO+0.3	V
Output voltage (Digital IO)	V_{OUT_IO}	-0.3 ~ VDDIO+0.3	V
Juntion temperature	Tj	125	^{o}C
Storage temperature	Tstg	-40 ~ +125	^{o}C

8.2 Recommended Operating Condition

VSS= 0V reference

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage (1.8V – Digital IO)	VDDIO	1.65	1.8	1.95	V
Supply voltage (3.3V – Digital IO)	VDDIO	3.0	3.3	3.6	V
Supply voltage (1.2V – Digital Core)	VDDC	1.1	1.2	1.3	V
Supply voltage (1.2V – MIPI CSI PHY)	VDD_MIPI	1.1	1.2	1.3	V
Operating temperature (ambient temperature with voltage applied)	Ta	-30	+25	+85	^{o}C
Supply Noise Voltage	V_{SN}			100	mV_{pp}

8.3 DC Electrical Specification

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input voltage, High levelinput Note1	V_{IH}	0.7 VDDIO		VDDIO	V
Input voltage, Low levelinput Note1	V_{IL}	0		0.3 VDDIO	V
Input voltage High level CMOS Schmitt Trigger Note1,2	V_{IHS}	0.7 VDDIO		VDDIO	V
Input voltage Low level CMOS Schmitt Trigger Note1,2	V_{ILS}	0		0.3 VDDIO	V

Output voltage High level Note1, Note2 **(Condition: I_{OH} = -0.4mA)**	V_{OH}	0.8 VDDIO		VDDIO	V
Output voltage Low level Note1, Note2 **(Condition: IOL = 2mA)**	V_{OL}	0		0.2 VDDIO	V
Input leak current, High level (Normal IO or Pull-up IO) (Condition: V_{IN} = +VDDIO, VDDIO = 3.6V)	I_{ILH1} (Note4)	-10	-	10	uA
Input leak current,High level (Pull-down IO) (Condition: V_{IN} = +VDDIO, VDDIO = 3.6V)	I_{ILH2} (Note4)	-	-	100	uA
Input leak current,Low level (Normal IO or Pull-down IO) (Condition: V_{IN} = 0V, VDDIO = 3.6V)	I_{ILL1} (Note5)	-10	-	10	uA
Input leak current,Low level (Pull-up IO) (Condition: V_{IN} = 0V, VDDIO = 3.6V)	I_{ILL2} (Note5)	-	-	200	uA

Note1 :Each power source is operating within recommended operation condition.

Note2 :Current output value is specified to each IO buffer individually. Output voltage changes with output current value.

Note4 :Normal pin or Pull-up IO pin applied VDDIO supply voltage to Vin (input voltage)

Note5 :Normal pin or Pull-down IO pin applied VSSIO (0V) to Vin (input voltage)

9 Timing Definitions

9.1 MIPI CSI – 2 Timings

Timing specification below has been ported from MIPI Alliance specification for D-PHY version 01-00-00. Timing defined in MIPI Alliance specification for D-PHY version 01-00-00 has precedence over timing described in the sections below.

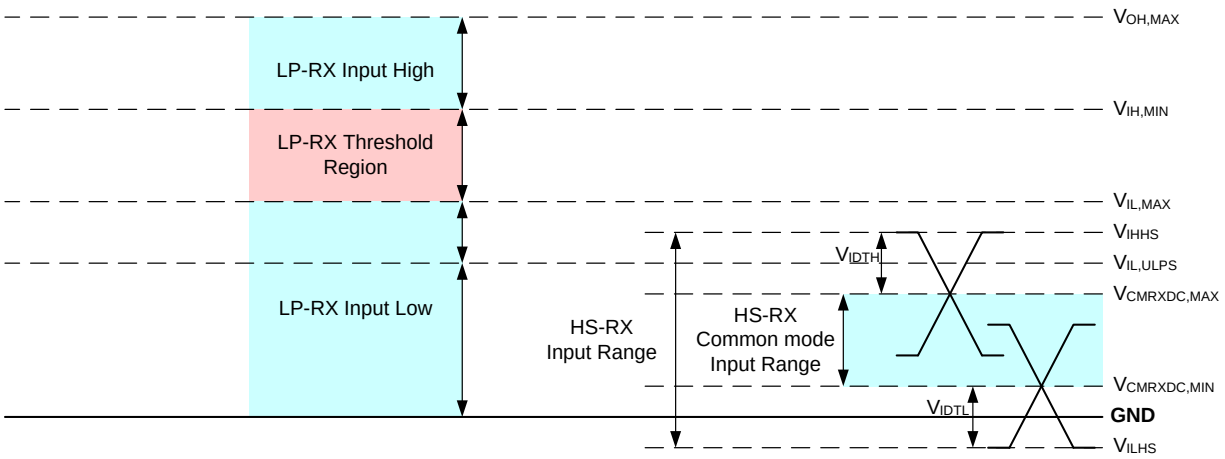

Figure 9-1 Signaling and voltage levels

Table 9-1 MIPI TX DC specifications

Parameter	Description	Min	Nom	Max	Units	Notes
HS mode						
VCMTX	HS transmit static common mode voltage	150	200	250	mV	1
|ΔVCMTX(1,0)|	VCMTX mismatch when output is Differential-1 or Differential-0			5	mV	2
|VOD|	HS transmit differential voltage	140	200	270	mV	1
|ΔVOD|	VOD mismatch when output is Differential-1 or Differential-0			10	mV	2
VOHHS	HS output high voltage			360	mV	
ZOS	Single ended output impedance	40	50	62.5	Ω	
ΔZOS	Single ended output impedance mismatch			10	%	
LP Mode						
VOH	Thevenin output high level	1.1	1.2	1.3	V	
VOL	Thevenin output low level	-50		50	mV	
ZOLP	Output impedance of LP transmitter	110			Ω	3

Notes:

1. Value when driving into load impedance anywhere in the ZID range.
2. It is recommended the implementer minimize ΔVOD and ΔVCMTX(1,0) in order to minimize radiation and optimize signal integrity.

3. Though no maximum value for ZOLP is specified, the LP transmitter output impedance shall ensure the TRLP/TFLP specification is met.

Table 9-2 MIPI Rx DC specifications

Parameter	Description	Min	Nom	Max	Units	Notes
V_{PIN}	Pin signal voltage range	-50		1350	mV	
$V_{PIN(absmax)}$	Transient pin voltage	-0.15		1.45	V	
$T_{VPIN(absmax)}$	Maximum transient time above $V_{PIN(absmax)}$ or below $V_{PIN(absmax)}$.			20	ns	3
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V	
V_{IH}	Logic 1 input voltage	880			mV	
V_{IL}	Logic 0 input voltage, not in ULP State			550	mV	
$V_{IL-ULPS}$	Logic 0 input voltage, ULP State			300	mV	
$V_{CMRX(DC)}$	Common-mode voltage HS receiver mode	70		330	mV	1,2
V_{IDTH}	Differential input high threshold			70	mV	
V_{IDTL}	Differential input low threshold	-70			mV	
V_{IHHS}	Single-ended input high voltage			460	mV	1
V_{ILHS}	Single-ended input low voltage	-40			mV	1

Notes:

4. Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.

5. This table value included a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz.

6. The voltage undershoot or overshoot beyond $V_{PIN}$is only allowed during a single 20 ns window after any LP-0 LP-1 transition or vice versa. For all other situations it must stay within the V_{PIN} range.

Table 9-3 MIPI High Speed Tx AC specifications

Parameter	Description	Min	Nom	Max	Units	Notes
ΔVCMTX(HF)	Common-level variations above 450MHz			15	mVRMS	
ΔVCMTX(LF)	Common-level variation between 50-450MHz			25	mVPEAK	
tR and tF	20%-80% rise time and fall time			0.3	UI	1
		150			ps	

Notes:

1. UI is equal to 1/(2*fh). See section 7.3 for the definition of fh.

Table 9-4 MIPI Low Power Tx AC characteristics

Parameter	Description		Min	Nom	Max	Units	Notes
TRLP/TFLP	15%-85% rise time and fall time				25	ns	1
TREOT	30%-85% rise time and fall time				35	ns	1, 5, 6
	Pulse width of the LP exclusive-OR clock	First LP exclusive-OR clock pulse after Stop state or last pulse before Stop state	40			ns	4
		All other pulses	20			ns	4
TLP-PER-TX	Period of the LP exclusive-OR clock		90			ns	
δV/δtSR	Slew rate @ CLOAD = 0pF		30		500	mV/ns	1,2,3,7
	Slew rate @ CLOAD = 5pF		30		200	mV/ns	1,2,3,7
	Slew rate @ CLOAD = 20pF		30		150	mV/ns	1,2,3,7
	Slew rate @ CLOAD = 70pF		30		100	mV/ns	1,2,3,7
CLOAD	Load capacitance		0		70	pF	1

Notes:

1. CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.
2. When the output voltage is between 15% and below 85% of the fully settled LP signal levels.
3. Measured as average across any 50 mV segment of the output signal transition.
4. This parameter value can be lower than TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters. Any LP exclusive-OR pulse observed during HS EoT (transition from HS level to LP-11) is glitch behavior.
5. The rise-time of TREOT starts from the HS common-level at the moment the differential amplitude drops below 70mV, due to stopping the differential drive.
6. With an additional load capacitance CCM between 0-60pF on the termination center tap at RX side of the Lane.
7. This value represents a corner point in a piecewise linear curve.

Table 9-5 MIPI High Speed Rx AC specifications

Parameter	Description	Min	Nom	Max	Units	Notes
$\Delta V_{CMRX(HF)}$	Common-mode interference beyond 450MHz			100	mV	2
$\Delta V_{CMRX(LF)}$	Common-mode interference 50MHz- 450MHz	-50		50	mV	1,3

Notes:

1. Excluding `static' ground shift of 50mV
2. $\Delta V_{CMRX(HF)}$ is the peak amplitude of a sine wave superimposed on the receiver inputs.

3. Voltage difference compared to the DC average common-mode potential.

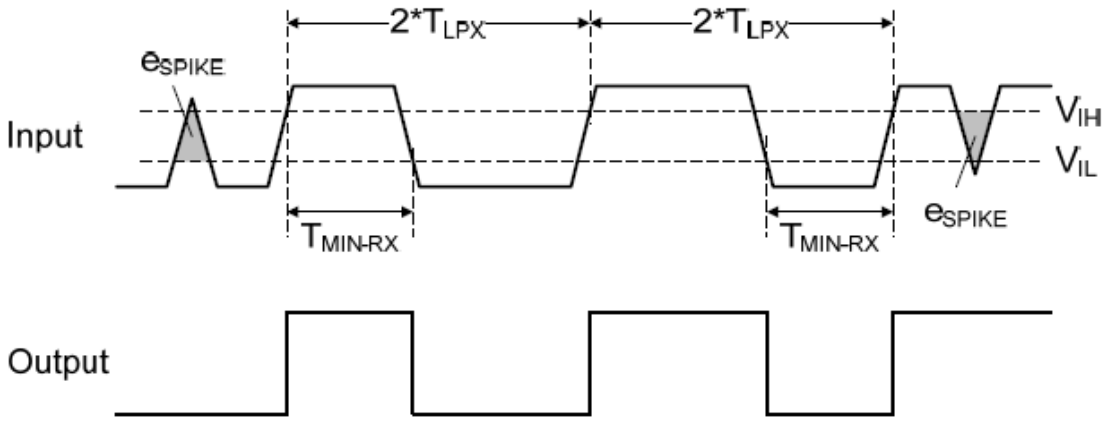

Figure 9-2 Input Glitch Rejection

Table 9-6 MIPI Low Power Rx AC characteristics

Parameter	Description	Min	Nom	Max	Units	Notes
e_{SPIKE}	Input pulse rejection			300	V.ps	1,2,3
T_{MIN-RX}	Minimum pulse width response	20			ns	4
V_{INT}	Peak interference amplitude			200	mV	
F_{INT}	Interference frequency	450			MHz	
T_{LPX}	Length of any Low Power state period	50			ns	

Notes:

1. Time-voltage integration of a spike above V_{IL} when being in LP-0 or below V_{IH} when being in LP-1 state.
2. An impulse less than this will not change the receiver state.
3. In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.
4. An input pulse greater than this shall toggle the output.

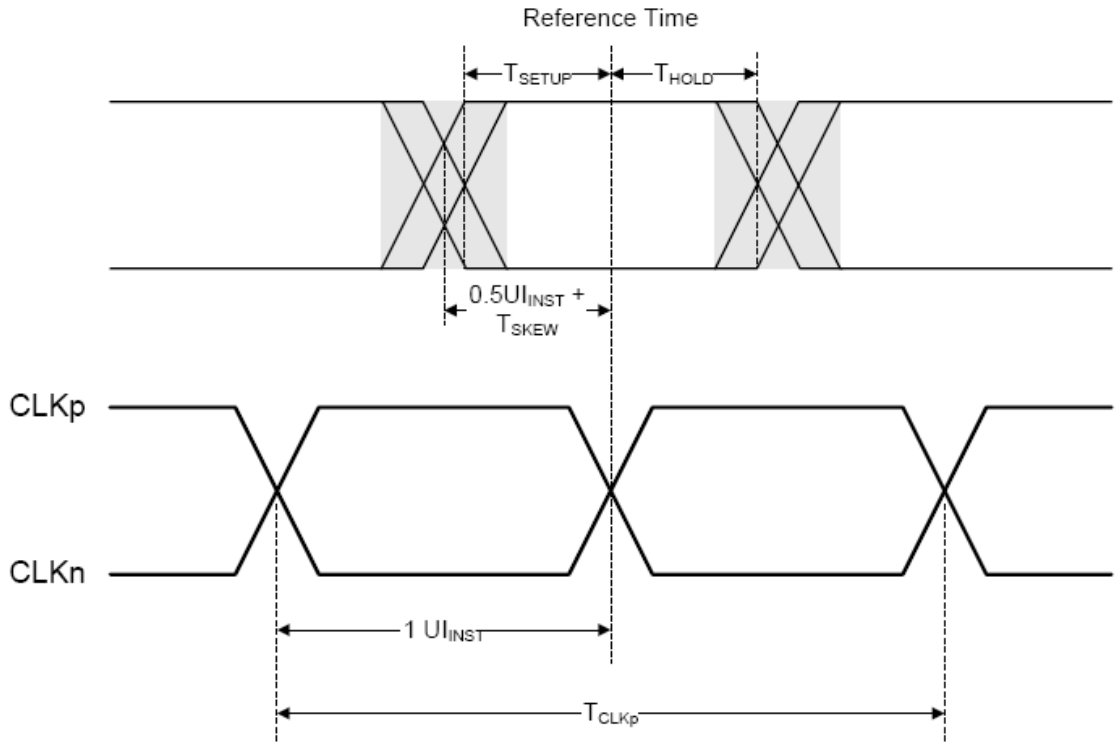

Figure 9-3 Data to clock timing reference

Table 9-7 Data-Clock timing specification

Parameter	Description	Min	Nom	Max	Units	Notes
T_{SKEW}	Data to clock skew measured at the transmitter	-0.15		0.15	UI_{INST}	
T_{SETUP}	Data to clock setup time at receiver	0.15			UI_{INST}	
T_{HOLD}	clock to data hold time at receiver	0.15			UI_{INST}	
UI_{INST}	1 Data bit time (instantaneous)			12.5	ns	
T_{CLKp}	Period of dual data rate clock	2	2	2	UI_{INST}	

9.2 I2C Timings

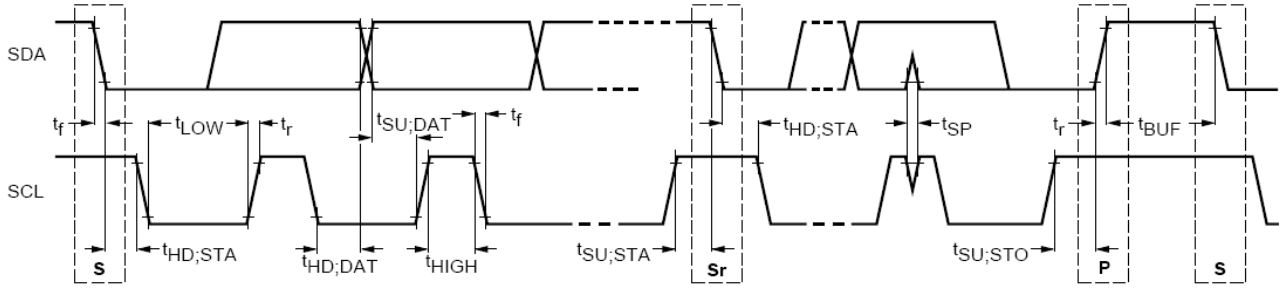

Table 9-8 I2C Timing

Item	Symbol	Min	Max	Unit
SCL clock frequency	f_{SCL}	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	0.6	-	µs
LOW period of the SCL clock	t_{LOW}	1.3	-	µs
HIGH period of the SCL clock	t_{HIGH}	0.6	-	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	0.6	-	µs
Data hold time:for I2C-bus devices	$t_{HD;DAT}$	0	0.9	µs
Data set-up time	$t_{SU;DAT}$	100	-	ns
Rise time of both SDA and SCL signals	t_r	20+0.1Cb	300	ns
Fall time of both SDA and SCL signals	t_f	20+0.1Cb	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	0.6	-	µs
Bus free time between a STOP andSTART condition	t_{BUF}	1.3	-	µs

Note: Cb = Capacitive load for each bus line (400pF max.)

9.3 Parallel Port Output Timings

Table 9-9 Parallel Output timing

Parameter	Description	Min.	Typ.	Max.	Units
T_{pdOUT}	Output data propagation time	1	-	6	ns

Notes: Maximum loading of PCLK, DATA, HVALID, VVALID are 10pF

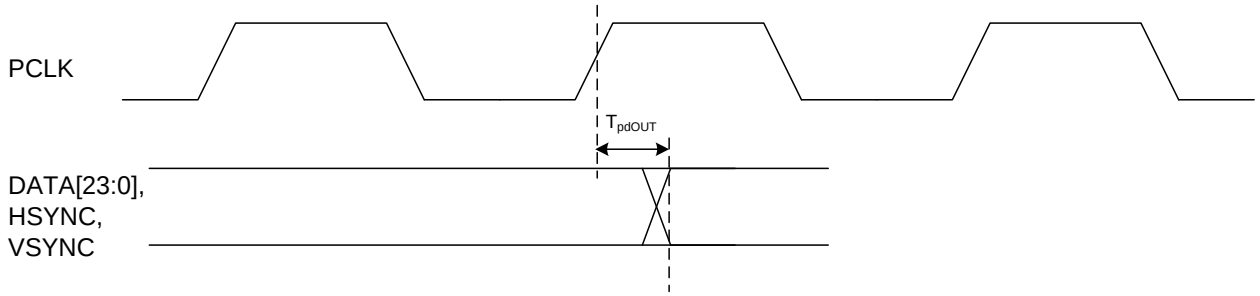

Figure 9-4 Parallel Output timing (ConfCtl.PLCKP = 0)

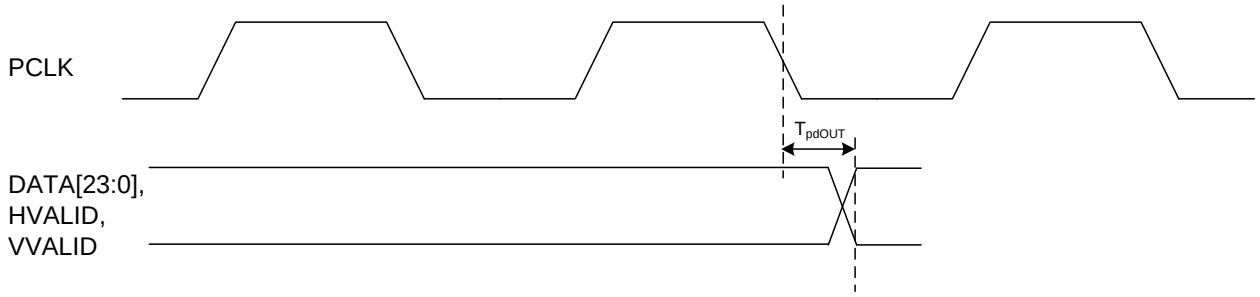

Figure 9-5 Parallel Output timing (ConfCtl.PLCKP = 1)

9.4 Parallel Port Input Timings

Table 9-10 Parallel Input timing

Parameter	Description	Min.	Typ.	Max.	Units
$T_{pd:SU}$	Setup time of data	2.0	-	-	ns
$T_{pd:HD}$	Hold time of data	1.0	-	-	ns
$T_{pd:CLK}$	Clock period	6.0	-	-	ns

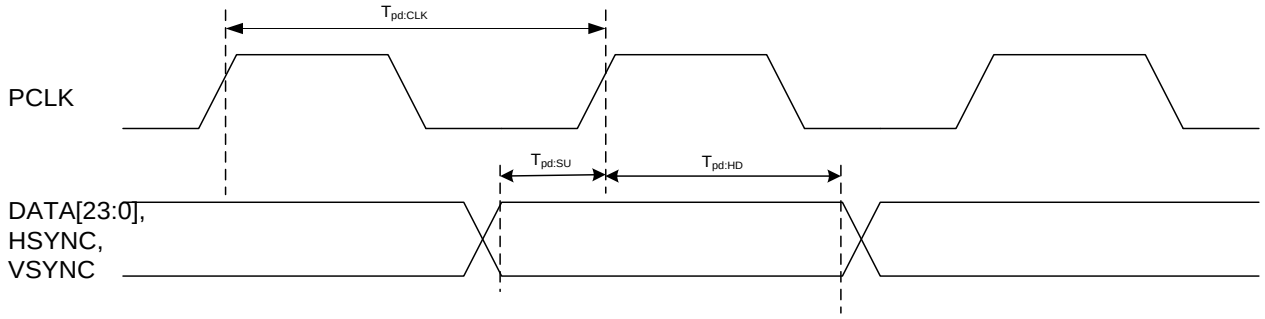

Figure 9-6 Parallel Input timing

9.5 SPI Input/Output Timings

Table 9-11 SPI timing

Parameter	Symbol	Min	Typ	Max	Unit
SPI Clock Frequency	f_{SEIS}	—	—	25	MHz
Clock to Data (MISO) Valid Time	t_{SOD}	—	—	15	ns
Clock to Data (MISO) Invalid Time	t_{SOH}	0	—	—	ns
Data in (MOSI) Setup Time	t_{SIS}	5	—	—	ns
Data in (MOSI) Hold Time	t_{SIH}	5	—	—	ns
Slave Select to Data (MISO) Valid Time	t_{SSDV}	—	—	25[1]	ns
Slave Select to Clock	t_{SSTC}	$3/f_{SYS}$	—	—	ns
Consecutive Transfer Delay Time	t_{CTDT}	$1/f_{SEIS}$	—	—	ns
Load on SEI Interface Signals	C_{IF}	—	—	10	pF

Notes: Maximum loading of MISO is 10pF

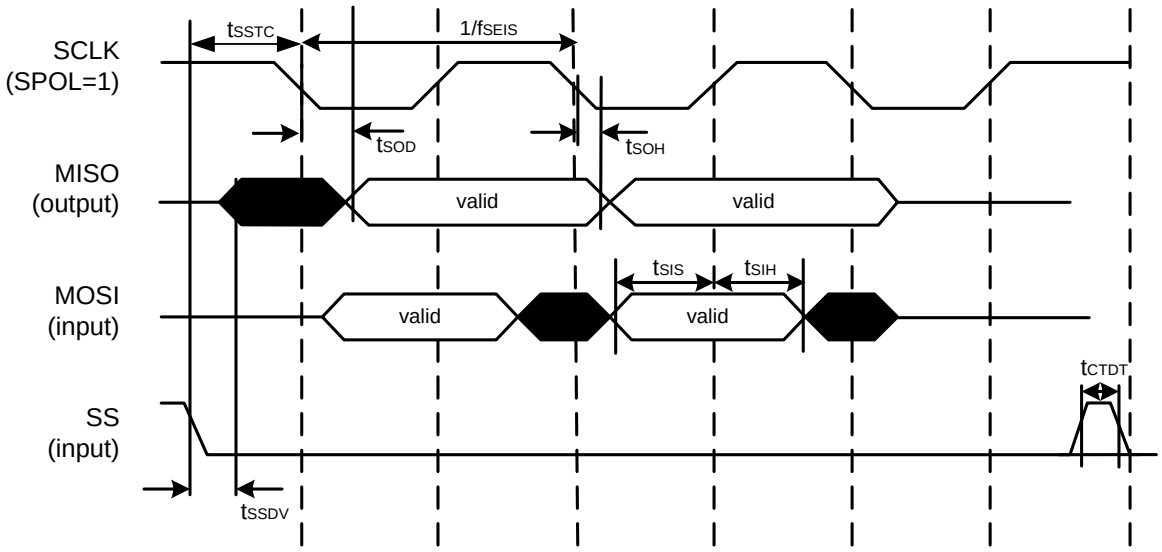

Figure 9-7 SPI timing (data valid on second active clock edge)

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